

## Description

The Si4614 DAB/DAB+ radio processor provides significant advances in size, power consumption, and performance to enable DAB/DAB+ Radio reception in automotive infotainment systems and car radios. It is designed to work with the high-performance automotive Si479x family of radio tuners.

The low power high performance Si4614 DAB/DAB+ Radio processor provides channel demodulation and source decoding of DAB/DAB+ signals delivering audio and data.

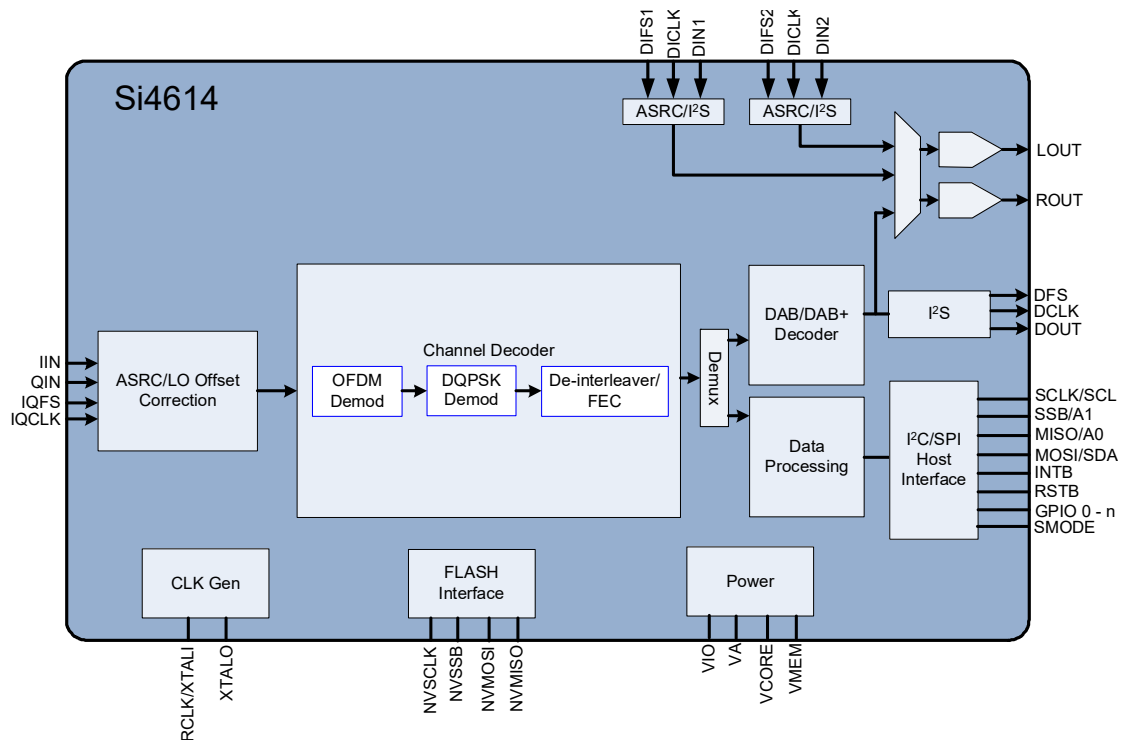
The Si4614 Radio processor provides DAB/DAB+ demodulation and decoding. In addition, the Si4614 provides an integrated clock oscillator or accepts a reference clock and supports a selectable control interface (SPI or I<sup>2</sup>C). The Si4614 processor system specifies a low minimal bill of materials, notably eliminating an external RAM memory module for channel decoding that is typically required in third party DAB/DAB+ Radio processors.

## Features

- DAB/DAB+ demodulator
- Transmission Modes I, II, III, IV detection and decoding
- DAB/DAB+ audio decoder
  - PAD/XPAD outputs available
- FIC decoder
  - Ensemble info
  - Service list
  - Component info
  - Service linking info
- Full support for data services
  - Packet mode
  - Packet mode with Data Groups
  - Enhanced packet mode
  - MOT, TPEG packet outputs
- No external RAM required for channel decoding
- Flash memory interface for application program load
- Support for Si479x Zero-IF digital at 2.048 MS/s
- On-chip crystal oscillator
- Reference clock input
- SPI, I<sup>2</sup>C control interfaces
- 7x7 mm 48-pin QFN package
- Pb-free/RoHS compliant
- AEC-Q100 qualified

## Applications

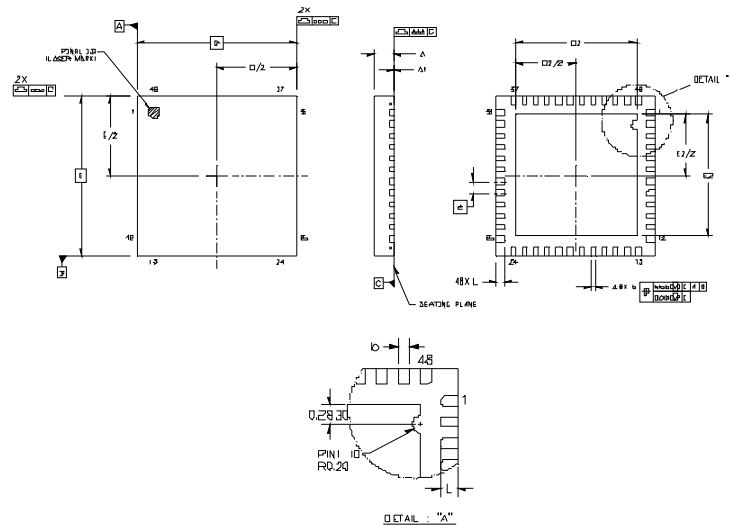
- Aftermarket car radio systems
- OEM automotive infotainment systems
- OEM automotive PND docking systems



**Table 1. Selected Electrical Specifications**

| Parameter                    | Symbol     | Test Condition | Min  | Typ    | Max | Unit |
|------------------------------|------------|----------------|------|--------|-----|------|
| Analog Supply Voltage        | $V_A$      | —              | 1.71 | 1.8    | 2.0 | V    |
| Interface Supply Voltage     | $V_{IO}$   | —              | 1.62 | 1.8    | 3.6 | V    |
| Core Digital Supply Voltage  | $V_{CORE}$ | —              | 1.71 | 1.8    | 2.0 | V    |
| Memory Supply Voltage        | $V_{MEM}$  | —              | 1.71 | 1.8    | 2.0 | V    |
| <b>Reference Clock</b>       |            |                |      |        |     |      |
| Reference Clock Frequency    | RCLK       |                | —    | 36.864 | —   | MHz  |
| Reference Clock Accuracy     |            |                | –100 | —      | 100 | ppm  |
| Reference Clock Duty Cycle   |            |                | 45   | —      | 55  | %    |
| <b>Crystal Oscillator</b>    |            |                |      |        |     |      |
| Crystal Oscillator Frequency |            |                | —    | 36.864 | —   | MHz  |
| Crystal Frequency Tolerance  |            | 37.209 MHz     | –100 | —      | 100 | ppm  |
| Load Capacitance             |            | 37.209 MHz     | —    | —      | 10  | pF   |

**Si4614-A10**



| Dimension | Min      | Nom  | Max  |
|-----------|----------|------|------|
| A         | 0.80     | 0.85 | 0.90 |
| A1        | 0.00     | 0.02 | 0.05 |
| b         | 0.18     | 0.25 | 0.30 |
| D         | 7.00 BSC |      |      |
| D2        | 5.20     | 5.30 | 5.40 |
| e         | 0.50 BSC |      |      |
| E         | 7.00 BSC |      |      |
| E2        | 5.20     | 5.30 | 5.40 |
| L         | 0.30     | 0.40 | 0.50 |
| aaa       | 0.15     |      |      |
| bbb       | 0.10     |      |      |
| ddd       | 0.05     |      |      |
| eee       | 0.08     |      |      |

**Notes:**

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

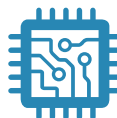


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