DATA SHEET

SKY535x2/x3 Low-Power DC to 3.1 GHz Ultra-Low Additive Jitter Differential Clock Buffers

The SKY53512/82/42 and SKY53513/83/43 family of fanout buffers is ideal for high-frequency, low-jitter clock distribution. These devices feature universal level format translation and ultra-low additive RMS phase jitter over a wide range of conditions, including frequency and input clock slew rate.

Separate core and output voltages are included. These support voltages down to 1.8 V to enable additional power savings.

Built-in LDOs deliver high PSRR performance and reduce the need for external components, simplifying low-jitter clock distribution in noisy environments.

The SKY53512/82/42 and SKY53513/83/43 feature an I^2C interface, which can be used to select the input source to each of the two output banks, the output format for each of the two output banks, as well as the output state for each clock output. The devices support 10, 8, or 4 outputs in two banks, each of which can be set to LVPECL, LVDS, HCSL, 800 mV LVDS, or complementary LVCMOS.

Each output bank has its own dedicated 1.8 V, 2.5 V, or 3.3 V output voltage supply. This buffer family can be paired with the Skyworks NetSync™ family of network synchronizer clocks, jitter attenuators, and clock generators and oscillators to deliver ultra-low-jitter clock tree solutions.

Applications

- 56G/112G/224G PAM4 SerDes clocking
- 400G/800G/1.6T switches and routers
- 5G/6G wireless infrastructure
- Data center switches

Key Features

- Ultra-low additive jitter (156.25 MHz LVPECL)
  - 35 fs RMS typical (12 kHz to 20 MHz)
  - 29 fs RMS typical (12 kHz to 20 MHz, 4 MHz HPF)
  - 47 fs RMS max (12 kHz to 20 MHz)
  - 39 fs RMS max (12 kHz to 20 MHz, 4 MHz HPF)
- 3:1 input multiplexer
  - Two any-format universal inputs supporting LVPECL, LVDS, S-LVDS, HCSL, CML, SSTL, HSTL, and sine waves
  - One crystal input (also accepts single-ended square wave or sine wave clocks)
- Two banks of differential output clocks
  - 10/8/4 output ordering options
  - Output formats selectable via I^2C: LVPECL, LVDS, HCSL, LVCMOS, and 800 mV LVDS
- Frequency range
  - LVPECL: dc to 3.1 GHz
  - LVDS: dc to 3 GHz
  - HCSL: dc to 800 MHz
  - LVCMOS: dc to 250 MHz
- PCIe Gen1/2/3/4/5/6/7 compliant
- Low-power operation (V_{DD}/V_{DDO})
  - 1.8 V, 2.5 V, or 3.3 V
- LVCMOS REF output with synchronous enable/disable
- Temperature range
  - –40 to +95 °C ambient temperature
  - 105 °C max board temperature
- Packages
  - SKY53512/13: 48-pin, 7 x 7 mm QFN
  - SKY53582/83: 40-pin, 6 x 6 mm QFN
  - SKY53542/43: 32-pin, 5 x 5 mm QFN
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

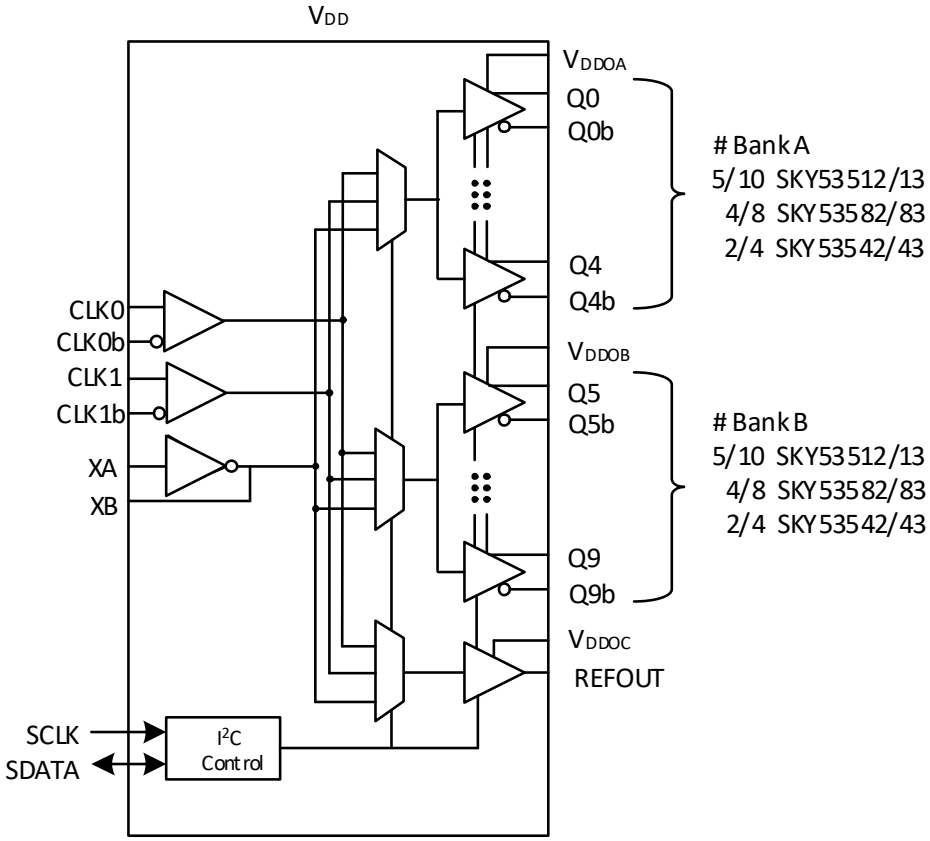


Figure 1. Functional Block Diagram

1. Pin Descriptions

1.1. SKY53512/13 7 x 7 mm 48-QFN Pin Descriptions

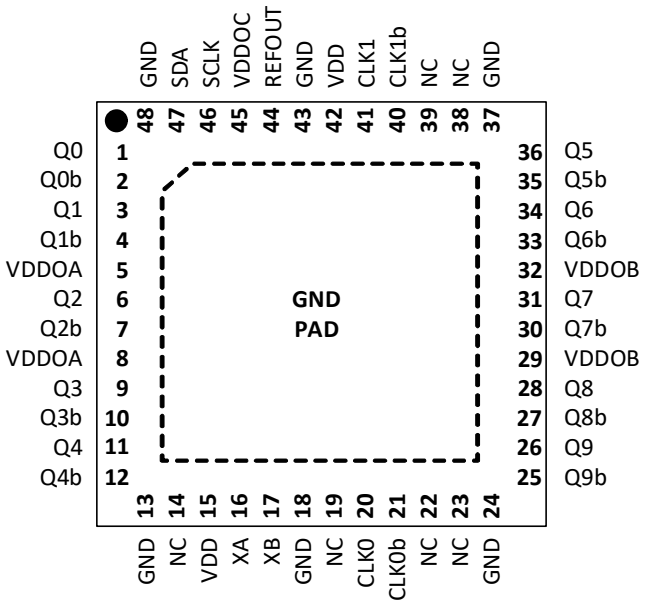


Figure 2. SKY53512/13 7 x 7 mm 48-QFN Pinout

Table 1. SKY53512/13 7 x 7 mm 48-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	Q0	O	Output clock 0
2	Q0b	O	Output clock 0 (complement)
3	Q1	O	Output clock 1
4	Q1b	O	Output clock 1 (complement)
5	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q4) Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
6	Q2	O	Output clock 2
7	Q2b	O	Output clock 2 (complement)
8	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q4) Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
9	Q3	O	Output clock 3
10	Q3b	O	Output clock 3 (complement)
11	Q4	O	Output clock 4
12	Q4b	O	Output clock 4 (complement)
13	GND	GND	Ground
14	NC	—	No connect. Leave this pin floating.

Table 1. SKY53512/13 7 x 7 mm 48-QFN Pin Descriptions (Continued)

Pin	Name	Type[1]	Description
15	VDD	P	Core voltage supply. Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
16	XA	I	Crystal input. Can also be driven by a XO, TCXO, or other external single-ended clock.
17	XB	O	Crystal output. When a crystal is not used, and XA is used as an input, this pin should be left floating.
18	GND	GND	Ground
19	NC	—	No connect. Leave this pin floating.
20	CLK0	I	Input clock 0
21	CLK0b	I	Input clock 0 (complement).
22	NC	—	No connect. Leave this pin floating.
23	NC	—	No connect. Leave this pin floating.
24	GND	GND	Ground
25	Q9b	O	Output clock 9 (complement)
26	Q9	O	Output clock 9
27	Q8b	O	Output clock 8 (complement)
28	Q8	O	Output clock 8
29	VDDOB	P	Output voltage supply: Bank B (outputs: Q5 to Q9) Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
30	Q7b	O	Output clock 7 (complement)
31	Q7	O	Output clock 7
32	VDDOB	P	Output voltage supply: Bank B (outputs: Q5 to Q9) Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
33	Q6b	O	Output clock 6 (complement)
34	Q6	O	Output clock 6
35	Q5b	O	Output clock 5 (complement)
36	Q5	O	Output clock 5
37	GND	GND	Ground
38	NC	—	No connect. Leave this pin floating.
39	NC	—	No connect. Leave this pin floating.
40	CLK1b	I	Input clock 1 (complement).
41	CLK1	I	Input clock 1
42	VDD	P	Core voltage supply. Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
43	GND	GND	Ground
44	REFOUT	O	LVCMOS reference output clock. Enable this output via I^2C control.
45	VDDOC	P	REFOUT buffer supply. Bypass with 0.1 µF capacitor placed as close to the VDDOC pin as possible.
46	SCLK	I	I^2C-compatible SCLOCK
47	SDA	I/O	I^2C-compatible SDATA
48	GND	GND	Ground
GND pad	GND	GND	Power supply ground and thermal relief

1. Pin types are: I = input, O = output, P = power, GND = ground.

1.2. SKY53582/83 6 x 6 mm 40-QFN Pin Descriptions

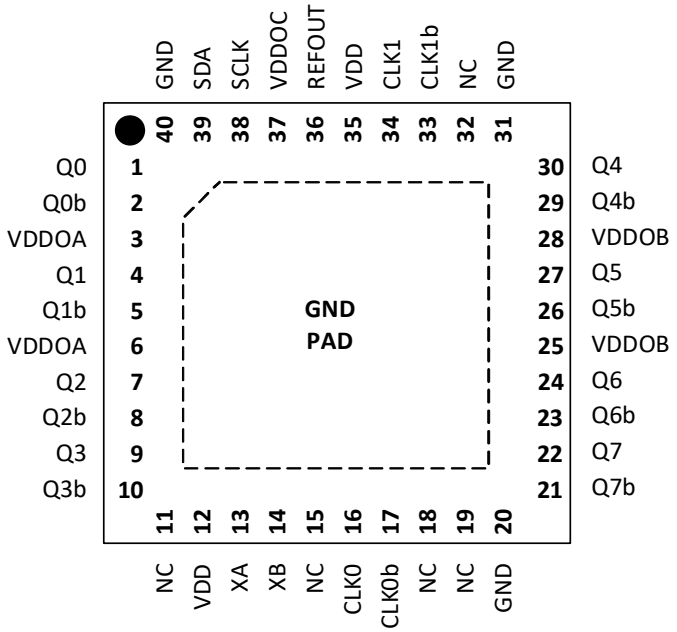


Figure 3. SKY53582/83 6 x 6 mm 40-QFN Pinout

Table 2. SKY53582/83 6 x 6 mm 40-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	Q0	O	Output clock 0
2	Q0b	O	Output clock 0 (complement)
3	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q3). Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
4	Q1	O	Output clock 1
5	Q1b	O	Output clock 1 (complement)
6	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q3). Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
7	Q2	O	Output clock 2
8	Q2b	O	Output clock 2 (complement)
9	Q3	O	Output clock 3
10	Q3b	O	Output clock 3 (complement)
11	NC	—	No connect. Leave this pin floating.
12	VDD	P	Core voltage supply Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
13	XA	I	Crystal input. Can also be driven by a XO, TCXO, or other external single-ended clock.
14	XB	O	Crystal output. When a crystal is not used, and XA is used as an input, this pin should be left floating.

Table 2. SKY53582/83 6 x 6 mm 40-QFN Pin Descriptions (Continued)

Pin	Name	Type[1]	Description
15	NC	—	No connect. Leave this pin floating.
16	CLK0	I	Input clock 0
17	CLK0b	I	Input clock 0 (complement)
18	NC	—	No connect. Leave this pin floating.
19	NC	—	No connect. Leave this pin floating.
20	GND	GND	Ground
21	Q7b	O	Output clock 7 (complement)
22	Q7	O	Output clock 7
23	Q6b	O	Output clock 6 (complement)
24	Q6	O	Output clock 6
25	VDDOB	P	Output voltage supply-Bank B (Outputs: Q4 to Q7). Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
26	Q5b	O	Output clock 5 (complement)
27	Q5	O	Output clock 5
28	VDDOB	P	Output voltage supply-Bank B (Outputs: Q4 to Q7). Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
29	Q4b	O	Output clock 4 (complement)
30	Q4	O	Output clock 4
31	GND	GND	Ground
32	NC	—	No connect. Leave this pin floating.
33	CLK1b	I	Input clock 1 (complement)
34	CLK1	I	Input clock 1
35	VDD	P	Core voltage supply. Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
36	REFOUT	O	LVCMOS reference output clock. Enable this output via I^2C control.
37	VDDOC	P	REFOUT buffer supply. Bypass with 0.1 µF capacitor placed as close to the VDDOC pin as possible.
38	SCLK	I	I^2C-compatible SCLOCK
39	SDA	I/O	I^2C-compatible SDATA
40	GND	GND	Ground
GND pad	GND	GND	Power supply ground and thermal relief

1. Pin types are: I = input, O = output, P = power, GND = ground.

1.3. SKY53542/43 5 x 5 mm 32-QFN Pin Descriptions

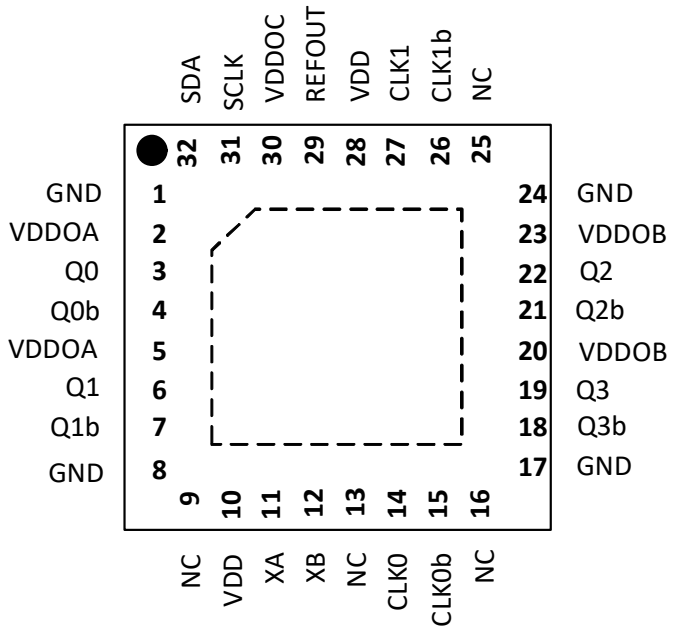


Figure 4. SKY53542/43 5 x 5 mm 32-QFN Pinout

Table 3. SKY53542/43 5 x 5 mm 32-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	GND	GND	Ground
2	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q1). Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
3	Q0	O	Output clock 0
4	Q0b	O	Output clock 0 (complement)
5	VDDOA	P	Output voltage supply: Bank A (outputs: Q0 to Q1) Bypass with 0.1 µF capacitor and place as close to the VDDOA pin as possible.
6	Q1	O	Output clock 1
7	Q1b	O	Output clock 1 (complement)
8	GND	GND	Ground
9	NC	—	No connect. Leave this pin floating.
10	VDD	P	Core voltage supply Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
11	XA	I	Crystal input. Can also be driven by a XO, TCXO, or other external single-ended clock.
12	XB	O	Crystal output. When a crystal is not used and XA is used as an input, this pin should be left floating.
13	NC	—	No connect. Leave this pin floating.
14	CLK0	I	Input clock 0

Table 3. SKY53542/43 5 x 5 mm 32-QFN Pin Descriptions (Continued)

Pin	Name	Type[1]	Description
15	CLK0b	I	Input clock 0 (complement)
16	NC	—	No connect. Leave this pin floating.
17	GND	GND	Ground
18	Q3b	O	Output clock 3 (complement)
19	Q3	O	Output clock 3
20	VDDOB	P	Output voltage supply-Bank B (outputs: Q2 to Q3). Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
21	Q2b	O	Output clock 2 (complement)
22	Q2	O	Output clock 2
23	VDDOB	P	Output voltage supply-Bank B (outputs: Q2 to Q3). Bypass with 0.1 µF capacitor and place as close to the VDDOB pin as possible.
24	GND	GND	Ground
25	NC	—	No connect
26	CLK1b	I	Input clock 1 (complement)
27	CLK1	I	Input clock 1
28	VDD	P	Core voltage supply Bypass with 0.1 µF capacitor placed as close to the VDD pin as possible.
29	REFOUT	O	LVCMOS reference output clock. Enable this output via I^2C control.
30	VDDOC	P	REFOUT buffer supply Bypass with 0.1 µF capacitor placed as close to the VDDOC pin as possible.
31	SCLK	I	I^2C-compatible SCLOCK
32	SDA	I/O	I^2C-compatible SDATA
GND pad	GND	GND	Power supply ground and thermal relief

1. Pin types are: I = input, O = output, P = power, GND = ground.

2. Detailed Description

2.1. Overview

The SKY53512/82/42 and SKY53513/83/43 are a family of ultra-low additive jitter, low-skew, universal/any-format buffers. The devices can operate at up to 3.1 GHz with differential outputs, and up to 250 MHz with LVCMOS outputs. Both devices feature a 3:1 input multiplexer stage that can accept the most common differential, LVCMOS, or sine wave input signals. The output stage includes two banks of outputs, each of which includes I^2C-selectable output format selection and output supply voltage, as well as an LVCMOS reference output. Each bank of outputs can be independently sourced from any of the three input sources. Each output can be independently enabled or disabled via I^2C control.

2.2. Block Diagrams

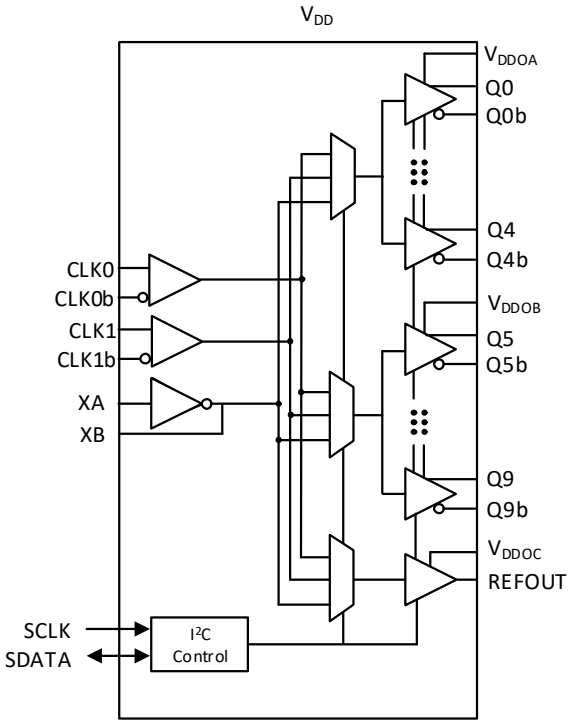


Figure 5. SKY53512/13 Block Diagram

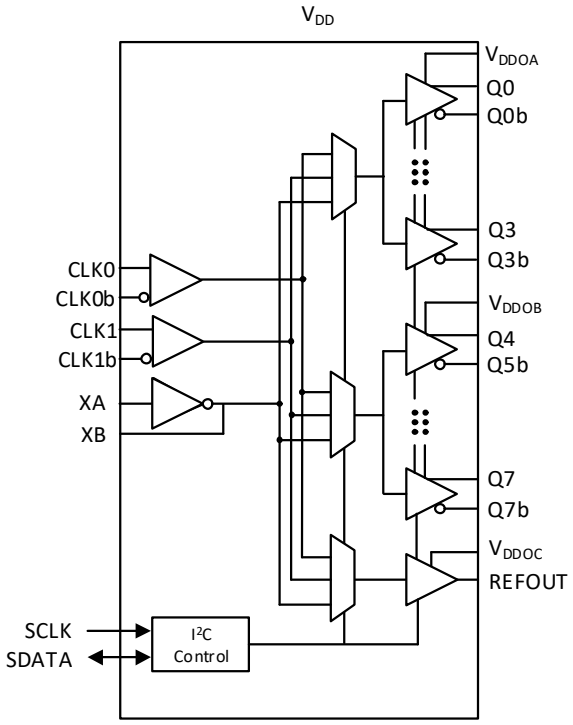


Figure 6. SKY53582/83 Block Diagram

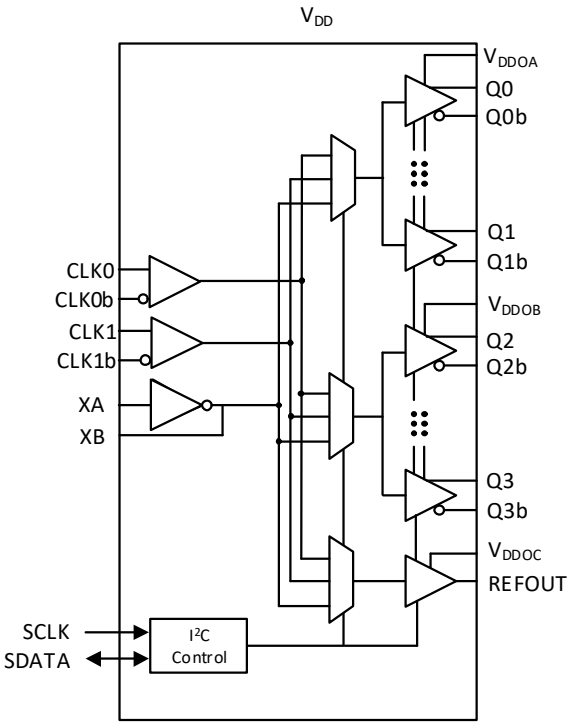


Figure 7. SKY53542/43 Block Diagram

2.3. Modes of Operation

2.3.1. Input Clock Stage

The input stage accepts a wide variety of common clock formats and voltage ranges on CLK0 and CLK1, including LVPECL, LVCMOS, LVDS, HCSL, CML, SSTL, and HSTL. Coupling may exist in the cases where the xtal is selected as the input to an output bank and an input clock is applied to CLK0 or CLK1, and/or when the device is operated in dual 1:n mode. For ac-coupled, sine wave clock inputs, see application note AN1405: SKY535xx Applications Guide. Each bank of outputs can be independently sourced from any of the three input sources; therefore, the devices can be configured to operate as dual 1:2, dual 1:4, or dual 1:5 buffers.
For the best high-speed performance, differential formats are recommended. The SKY535x2/x3 exhibits excellent additive RMS phase jitter across a wide spectrum of input slew rates for both single-ended and differential input clocks.

To achieve optimal performance, a differential slew rate of 3.0 V/ns is recommended for differential formats, and 1.0 V/ns for single-ended formats to meet the max RMS additive phase jitter data sheet specifications. The buffers remain fully functional with slower slew rates, but incur some degradation in jitter performance. See Figure 55 on page 48 for further information on additive RMS phase jitter performance vs. input clock slew rate. For input frequencies below 1 MHz, dc-coupled interfaces are recommended. For more information, see "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance".

Table 4. DC-Coupled Clock Input Options on CLK0/CLK1

Clock Format	V_{DD} = 1.8 V	V_{DD} = 2.5/3.3 V
LVPECL	No	Yes
LVCMOS	Yes	Yes
LVDS/S-LVDS	Yes	Yes
HCSL	Yes	Yes

The input clock can be selected from CLK0/CLK0b, CLK1/CLK1b, or the crystal input (XA/XB). The input source to each bank of outputs, as well as REFOUT, can be selected using the I^2C interface.

Table 5. Clock Input vs. Output States[1, 2]

State of Selected Clock Input	State of Enabled Clock Outputs[2]
CLK0/CLK0b and CLK1/CLK1b inputs shorted together via 100 Ω resistor	Logic low
CLK0/CLK0b or CLK1/CLK1b input logic low.	Logic low
CLK0/CLK0b or CLK1/CLK1b input logic high.	Logic high

1. Upon power up, a single rising edge at the selected input is required for the outputs to reflect the input source.
2. If the selected clock input is not driven, a 100 Ω resistor should be placed between CLKx/CLKxb for the state of enabled outputs to be logic low. Omission of the 100 Ω resistor may result in undesired chatter on enabled outputs.

2.3.2. Clock Outputs

The highly flexible output drivers support a wide range of clock signal formats, including LVPECL, HCSL, LVDS, 800 mV LVDS, and LVCMOS. The output format type for Bank A and Bank B outputs are independently configurable using the I^2C interface. This feature enables the device to be used for format/level translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For applications where all differential outputs are not required, unused Qn/Qnb output pins should be left floating with a minimal copper length to minimize capacitance, potential coupling, and power consumption. It is recommended to disable outputs using the I^2C interface to reduce power. See the termination diagrams in "3.3. Clock Output Termination" on page 18.

The SKY53513/83/43 supports LVDS, 800 mV LVDS, LVPECL, or complementary LVCMOS output signal formats on Bank A and/or Bank B. The output signal format for Bank A and/or Bank B can be chosen independently using the I^2C interface. The output format for Bank A and Bank B can be selected using Byte 315 and 316, respectively. Please reference "7.6. Register Map" on page 55 for further information.

Table 6. SKY53512/82/42 Output Signal Levels

Format_A1 Format_B1[1]	Format_A0 Format_B0[1]	V_{DDOx} = 3.3 V	V_{DDOx} = 2.5 V	V_{DDOx} = 1.8 V
0	0	HCSL 600 mV swing	HCSL 600 mV swing	HCSL 600 mV swing
0	1	HCSL 700 mV swing	HCSL 700 mV swing	HCSL 700 mV swing
1	0	HCSL 800 mV swing	HCSL 800 mV swing	HCSL 800 mV swing
1	1	HCSL 1200 mV swing	HCSL 1200 mV swing	HCSL 1200 mV swing

1. See "7.6. Register Map" on page 55, byte 315 and byte 316.

Table 7. SKY53513/83/43 Output Signal Levels

Format_A1 Format_B1[1]	Format_A0 Format_B0[1]	V_{DDOx}= 3.3 V	V_{DDOx} = 2.5 V	V_{DDOx} = 1.8 V
0	0	800 mV LVDS	800 mV LVDS	N/A[2]
0	1	LVDS	LVDS	S-LVDS
1	0	LVPECL	LVPECL	N/A[2]
1	1	Complementary LVCMOS	Complementary LVCMOS	Complementary LVCMOS

1. See "7.6. Register Map" on page 55, byte 315 and byte 316.
2. The hardware default output format for 1.8 V is undefined.

The device also features an LVCMOS clock output (REFOUT) at the same frequency as the selected clock input, which can be enabled/disabled via the I^2C interface. REFOUT is synchronously enabled within three cycles of the input clock after the output is enabled and meets setup and hold timing requirements.

2.3.2.1. Output Enable

Each output clock can be independently enabled or disabled using the I^2C interface. When REFOUT is disabled, the output is synchronously disabled in a Hi-Z state. This allows the disabled state to be determined by external bias. For example, if a 1 kΩ resistor is connected from REFOUT to ground, REFOUT is pulled low when disabled.

3. Applications Information

3.1. Driving Clock Inputs (CLK0/CLK1)

The SKY53512/82/42 and SKY53513/83/43 families feature two universal, any-format clock inputs that can accept ac-coupled LVPECL, LVDS, HCSL, CML, SSTL, HSTL, and ac-coupled, single-ended square and sine wave clocks, or dc-coupled LVPECL, LVDS, HCSL, or LVCMOS clock inputs. Inputs must not be driven prior to V_{DD} reaching the recommended minimum level as this could affect the reliability of the device. The devices feature excellent additive RMS phase jitter over a wide range of clock input slew rates as shown in Figure 55 on page 48. To achieve the best additive RMS phase jitter performance on the output clocks, Skyworks recommends a differential input with a high differential slew rate of 3 V/ns or higher.

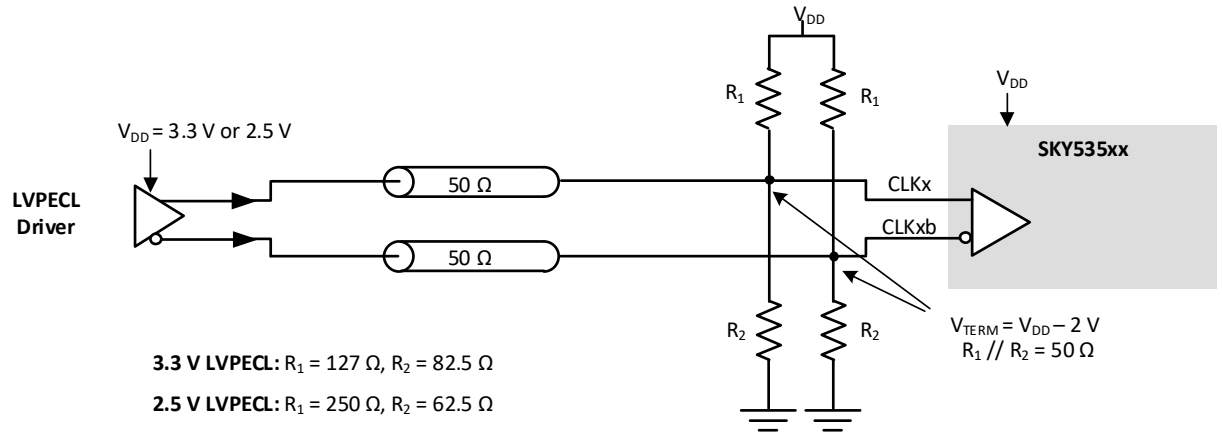


Figure 8. DC-Coupled LVPECL Input Termination Scheme 1

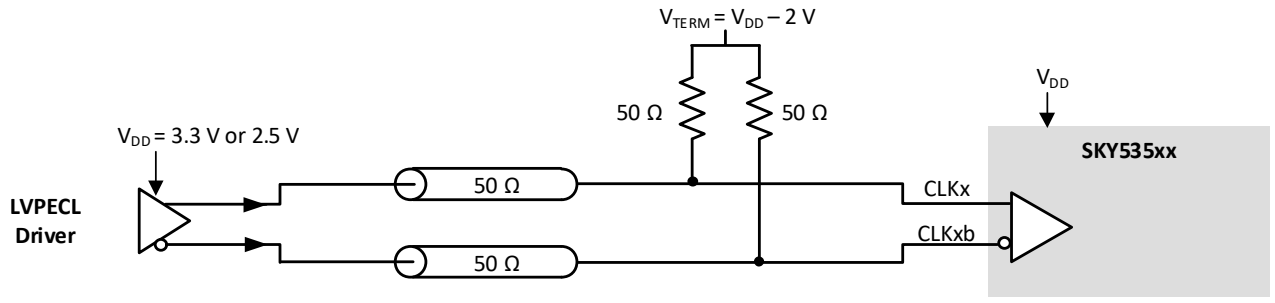


Figure 9. DC-Coupled LVPECL Input Termination Scheme 2

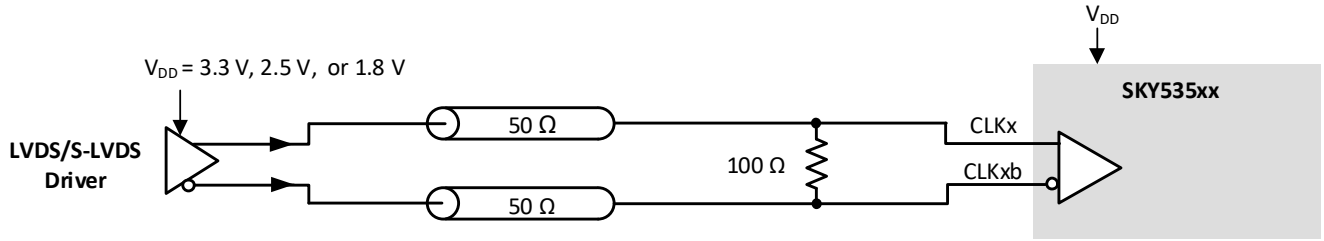
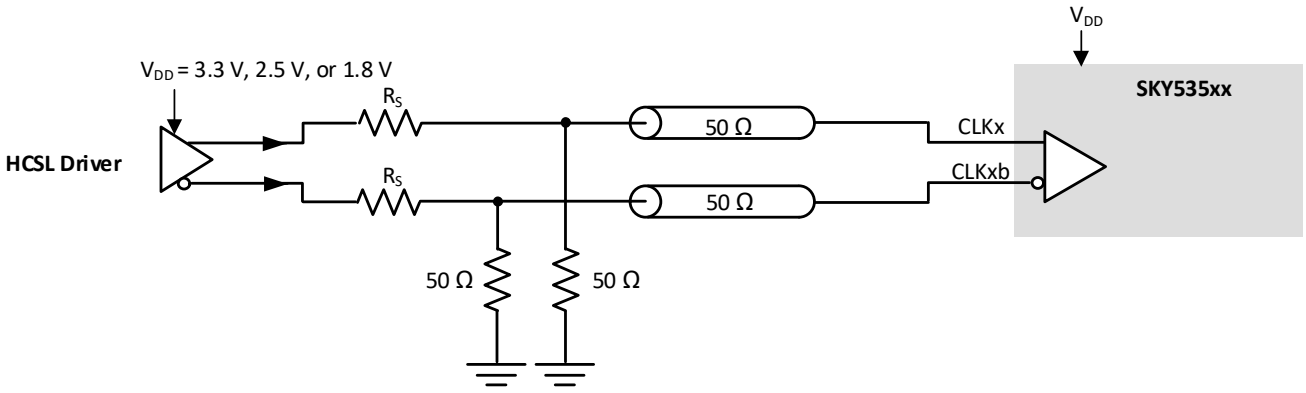


Figure 10. DC-Coupled LVDS/S-LVDS Input Termination



Note: R_S series termination is optional depending on the location of the receiver.
Adding R_S will reduce the amplitude of the output driver swing seen at the receiver.

Figure 11. DC-Coupled HCSL Input Termination

The device features internal common mode biasing to support ac-coupled differential input clocks. Although optimal jitter performance is achieved when using differential inputs, driving the CLK0 or CLK1 input pins with a single-ended clock is possible, as long as the clock conforms to the single-ended input specifications outlined in Table 11, “Input Clock Specifications,” on page 26. Single-ended input clocks can be ac-coupled, using the configurations shown in Figure 12 or Figure 13. The output impedance of the LVCMOS driver plus R_S should be close to 50 Ω to match the characteristic impedance of the transmission line and load termination.

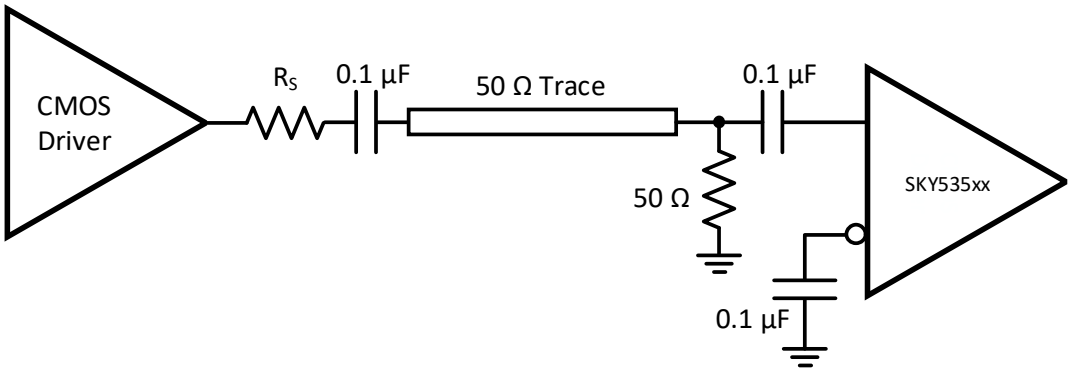


Figure 12. Single-Ended Input Termination Scheme 1 (AC-Coupling)

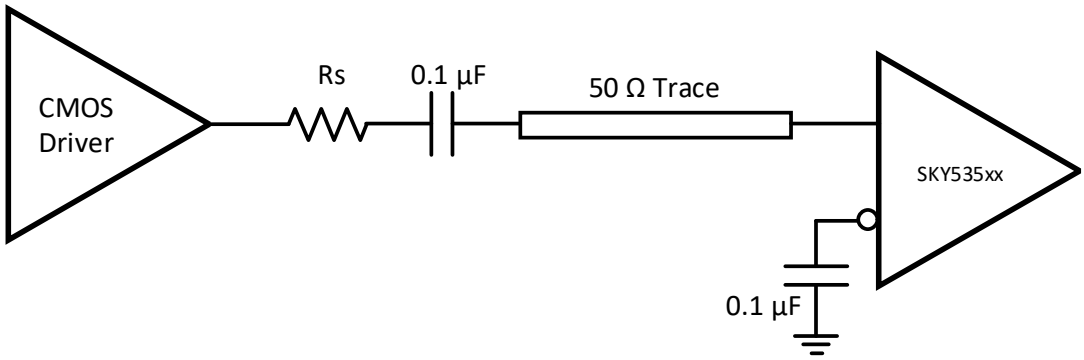


Figure 13. Single-Ended Input Termination Scheme 2 (AC-Coupling)

A single-ended clock may also be dc coupled to CLK0 or CLK1 as shown in Figure 14. Place a 50 Ω load resistor near the CLK0 or CLK1 input pin for signal attenuation and line termination. Half of the single-ended swing of the driver (voltage seen at the 50 Ω load depends on the R_S and CMOS source impedance) drives CLK0 or CLK1, therefore CLK0b or CLK1b should be externally biased to the midpoint voltage of the attenuated input swing ((VO,PP / 2) × 0.5). The external bias voltage should be within the specified input common-mode voltage (V_{CM}) range specified in "5. Electrical Specifications" on page 25. This can be achieved using external biasing resistors in the kΩ range (R_{B1} and R_{B2}) or another low-noise voltage reference. Doing so ensures that the input swing crosses the threshold voltage at a point where the input slew rate is the highest. If the LVCMOS driver cannot achieve sufficient swing with a dc-terminated, 50 Ω load at the CLK0 or CLK1 input as shown in Figure 14, then consider connecting the 50 Ω load termination to ground through a capacitor (CAC). This ac termination blocks the dc load current on the driver, so the voltage swing at the input is determined by the voltage divider formed by the source (Ro + Rs) and 50 Ω load resistors. The value for CAC depends on the trace delay, Td, of the 50 Ω transmission line; CAC ≥ 3 x Td / 50 Ω.

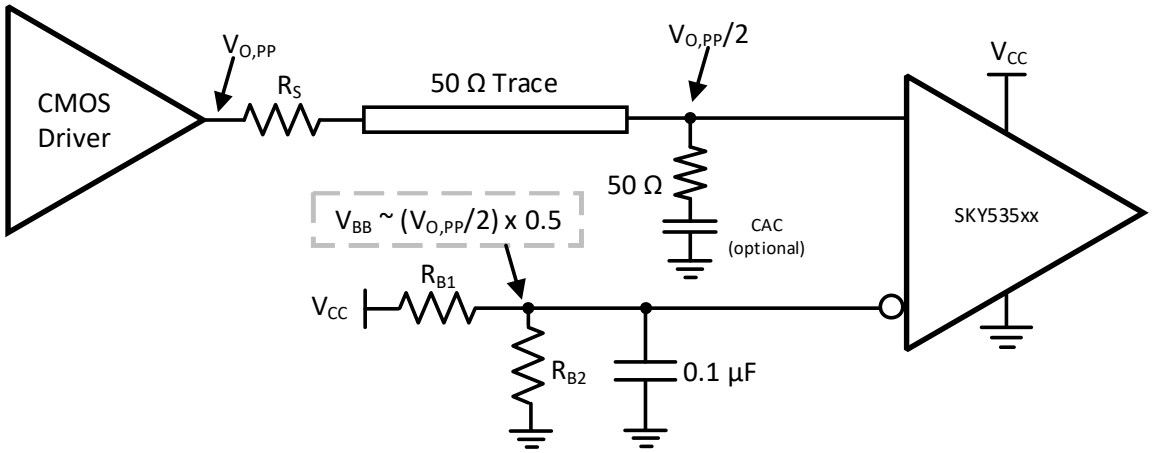


Figure 14. Single-Ended Input with Common-Mode Biasing Option 1, DC Coupling

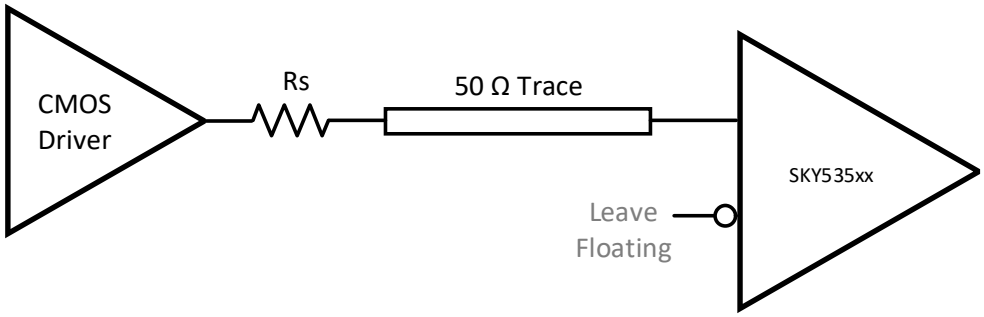


Figure 15. Single-Ended Input Option 2, DC Coupling

The input clock receivers on the SKY535x2/x3 do not have hysteresis; an internal biasing network prevents the receiver from switching due to board noise.

3.2. Crystal Interface (XA/XB)

The SKY53512/82/42 and SKY53513/83/43 families feature an integrated crystal oscillator circuit in the input stage that supports a fundamental mode, AT-cut crystal input. When the device is operated in crystal mode, V_{DDOA} must have a valid voltage applied.

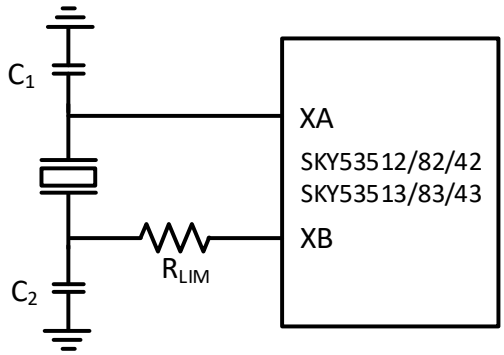


Figure 16. Crystal Interface

The external load capacitors (C_1 and C_2 in the figure above) are a function of capacitive parameters associated with the crystal, the input capacitance of the crystal oscillator circuit, and stray capacitance comprised of the parasitic capacitance of the board trace and bond pad capacitances. Details of how these capacitor values (C_1 and C_2) and the limiting resistor (R_{LIM}) are calculated are provided in Application Note "AN1405: SKY535xx Applications Guide".

If the crystal oscillator is not used, it is possible to drive the XA input with a single-ended external clock as shown in Figure 17 below. The input clock should be ac-coupled to the XA pin, which has an internally-generated input bias voltage, and the XB pin should be left floating. While XA provides an alternative input to multiplex an external clock, it is recommended to alternatively use either universal input (CLK0/CLK1) because the inputs offer higher operating frequency, better common-mode and power supply noise rejection, and greater performance over supply voltage and temperature variations.

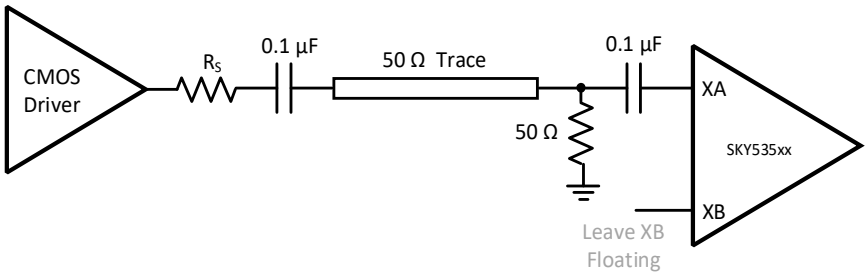


Figure 17. Driving XA with a Single-Ended Input Clock

3.3. Clock Output Termination

A single rising edge on the selected input clock is required for the output to then reflect the input source. All unused outputs should be left unconnected.

3.3.1. DC-Coupled Differential Output Driver Terminations

For dc-coupled terminations, it is important to ensure that the input supply voltage at the downstream receiver matches the supply voltage applied to the SKY535xx output driver (VDDOx). In cases where that is not possible, Skyworks recommends adopting ac-coupling instead. For dc-coupled operation of an LVDS driver, terminate with 100 Ω as close as possible to the LVDS receiver.

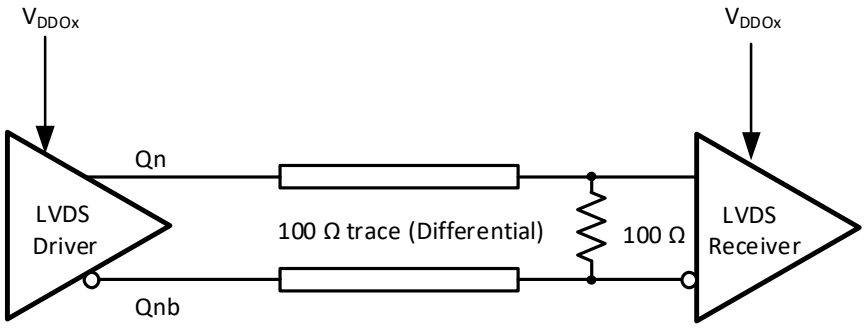


Figure 18. DC-Coupled LVDS Clock Output Termination

For dc-coupled operation of an HCSL driver, terminate with 50 Ω to ground near the receiver as shown in Figure 19.

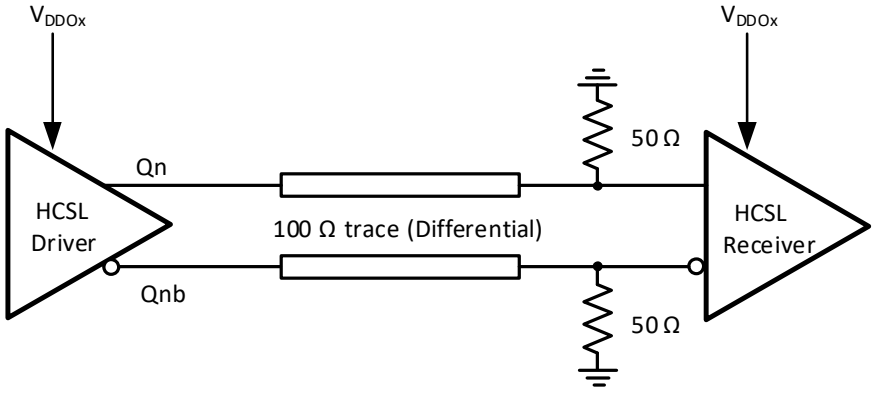


Figure 19. DC-Coupled HCSL Clock Output Termination (Scheme 1)

It is also possible to terminate with 50 Ω to ground near the driver output. Series resistors, R_S, may be used to limit overshoot due to the fast transient current. Because HCSL drivers require a dc path to ground, ac-coupling is not allowed between the output drivers and the 50 Ω termination resistors.

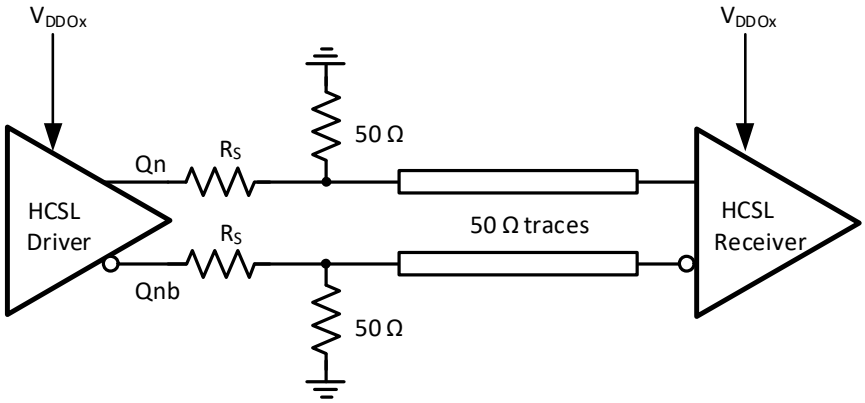


Figure 20. DC-Coupled HCSL Clock Output Termination (Scheme 2)

For dc-coupled operation of an LVPECL driver, terminate with 50 Ω to V_{DDO} – 2 V, as noted in Figure 21 below. Alternatively, terminate with a Thevenin equivalent circuit as shown in Figure 22 on page 20 for V_{DDO} (output driver supply voltage) = 3.3 V and 2.5 V. In the Thevenin equivalent circuit, the resistor dividers set the output termination voltage (V_{TT}) to V_{DDO} – 2 V.

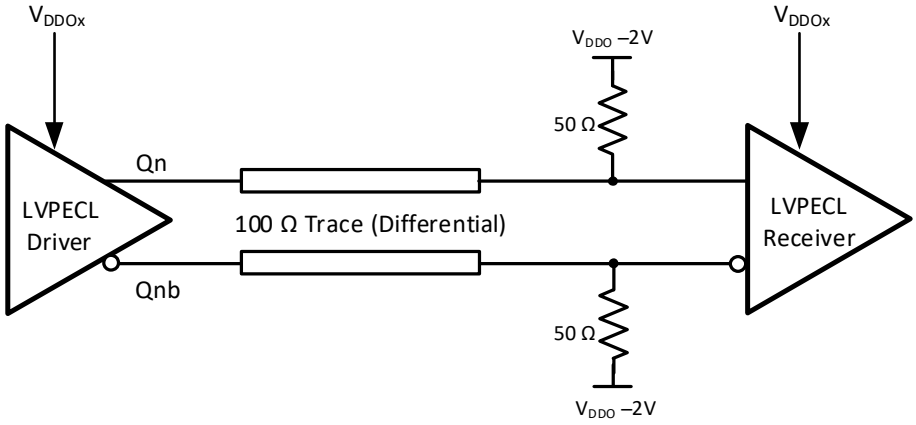
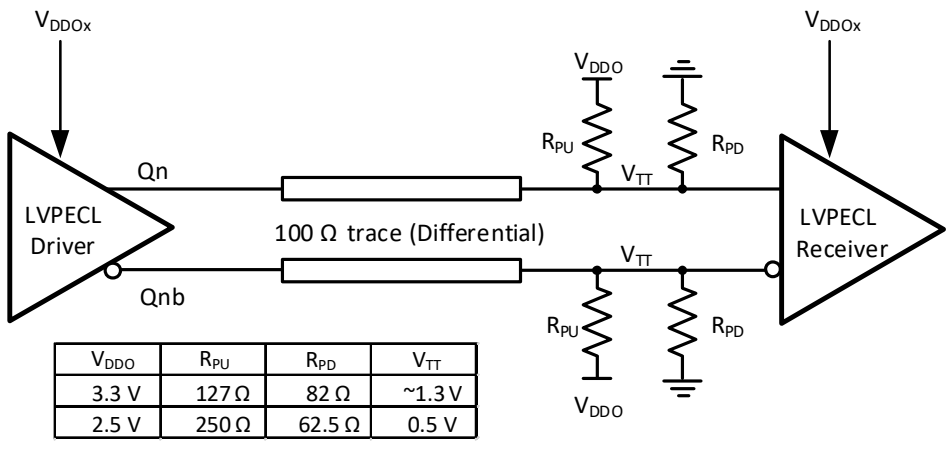


Figure 21. DC-Coupled LVPECL Clock Output Termination



V_{DDO}	R_{PU}	R_{PD}	V_{TT}
3.3 V	127 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 22. DC-Coupled LVPECL Clock Output Termination, Thevenin Equivalent

3.3.2. AC-Coupled Differential Output Driver Terminations

When driving differential receivers with an LVDS driver, the signal may be ac-coupled by adding dc-blocking capacitors. However, the proper dc bias point needs to be established at both the driver side and the receiver side. The recommended termination scheme depends on whether or not the differential receiver has integrated termination resistors.

When driving a differential receiver without internal 100 Ω differential termination, the ac-coupling capacitors should be placed between the load termination resistor and the receiver to allow a dc path for proper biasing of the LVDS driver. This is shown in Figure 23. The load termination resistor and ac-coupling capacitors should be placed as close as possible to the receiver inputs to minimize stub length. The receiver can be biased internally or externally to a reference voltage within the receiver's common mode input range through resistors in the kilo-ohm range.

When using ac-coupling with LVDS outputs, there may be a start-up delay observed in the clock output due to capacitor charging. The examples in Figure 23 and Figure 24 use 0.1 µF capacitors, but this value may be adjusted to meet the startup requirements for the particular application.

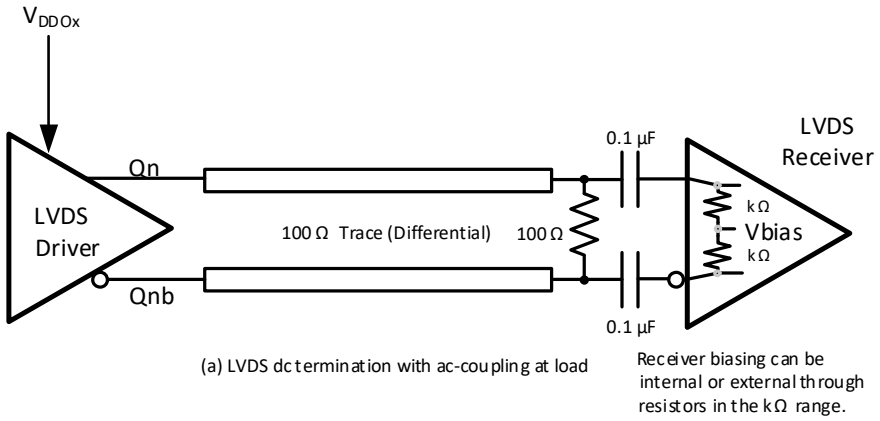


Figure 23. AC-Coupled LVDS Clock Output Coupled to Receivers without Internal 100 Ω Termination

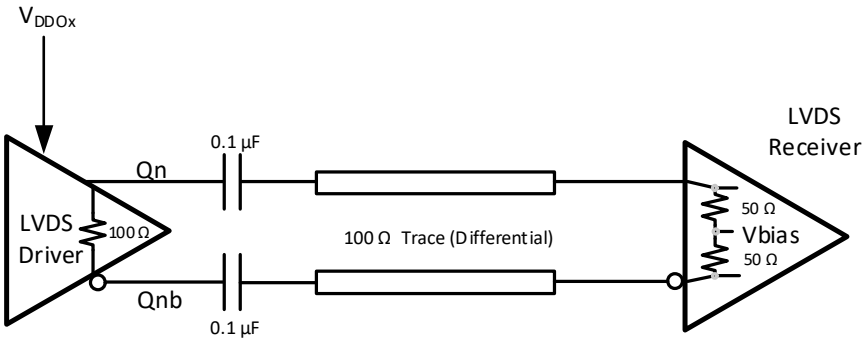


Figure 24. AC-Coupled LVDS Clock Output Coupled to Receivers with Internal 100 Ω Termination

LVPECL drivers require a dc path to ground. When ac-coupling an LVPECL signal, use 160 Ω emitter resistors (or 91 Ω for V_{DDO} = 2.5 V) close to the LVPECL driver to provide a dc path to ground as shown in Figure 25. For proper receiver operation, the signal should be biased to the dc bias level (common-mode voltage) specified by the receiver. The typical dc bias voltage (common-mode voltage) for LVPECL receivers is 2 V. Alternatively, a Thevenin equivalent circuit forms a valid termination as shown in Figure 25 for V_{DDO} = 3.3 V and 2.5 V.

Note: *This Thevenin circuit is different from the dc-coupled example in Figure 22, since the voltage divider is setting the input common-mode voltage of the receiver.*

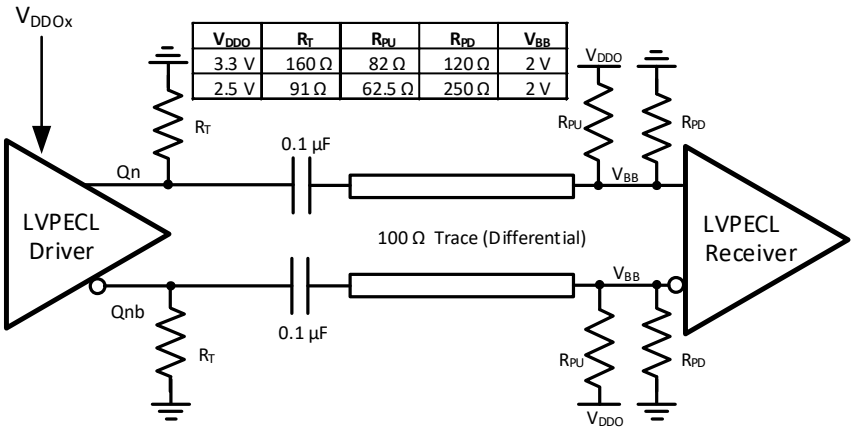


Figure 25. AC-Coupled LVPECL Clock Output Termination (Thevenin Equivalent)

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal. It is possible to use an LVPECL driver as one or two separate 800 mV p-p single-ended signals. When dc-coupling one of the LVPECL drivers of a Qx/Qxb pair, ensure that the unused driver is properly terminated. When dc-coupling an LVPECL driver, the termination should be 50 Ω to V_{DDO} – 2 V as shown in Figure 26. The Thevenin equivalent circuit is also a valid termination as shown in Figure 27 for V_{DDO} = 2.5 V or 3.3 V.

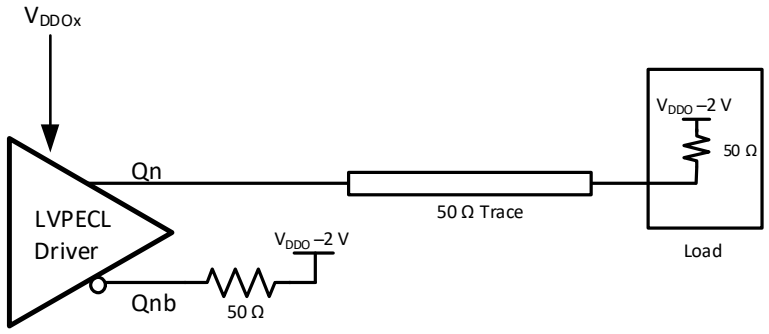
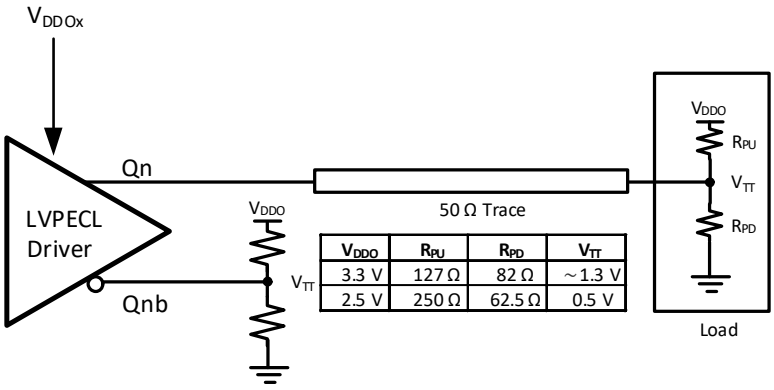


Figure 26. Single-Ended LVPECL Clock Output Termination, DC-Coupling



V_{DDO}	R_{PU}	R_{PD}	V_{TT}
3.3 V	127 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 27. Single-Ended LVPECL Clock Output Termination, DC-Coupling (Thevenin Equivalent)

When ac-coupling an LVPECL driver into a single-ended load, use a 160 Ω emitter resistor for V_{DDO} = 3.3 V to provide a dc path to ground and ensure a 50 Ω termination with the proper dc bias level for the receiver. The typical dc bias voltage for LVPECL receivers is 2 V. If the companion driver is not used, it should be terminated with either a proper ac or dc termination.

This latter example of ac-coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment, a dc voltage level of 0 Vdc is required for safe and proper operation. For internal 50 Ω termination, the test equipment correctly terminates the LVPECL driver being measured, as shown in Figure 28.

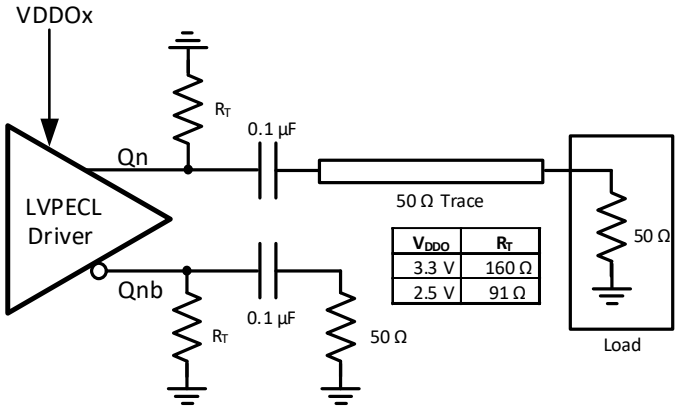


Figure 28. Single-Ended LVPECL Clock Output Termination (AC-Coupling)

3.3.3. LVCMOS Output Termination

The following diagrams provide the recommended LVCMOS output termination for the SKY535x2/x3 REFOUT LVCMOS output. These include LVCMOS outputs on the SKY535x3.

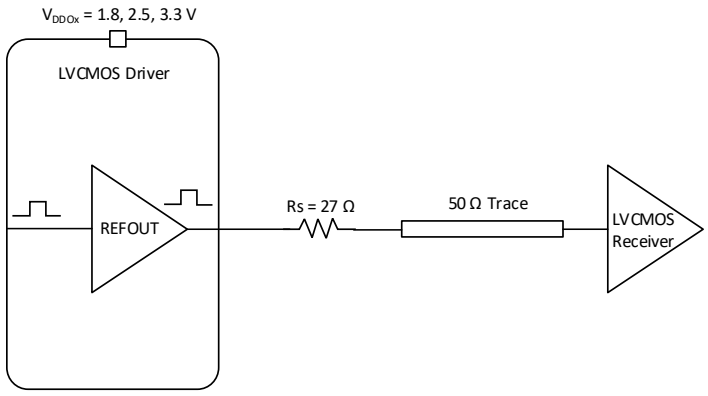


Figure 29. LVCMOS REFOUT

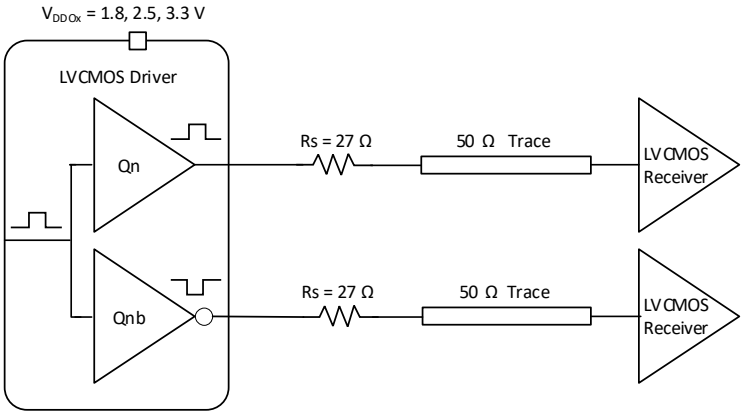


Figure 30. LVCMOS Outputs (Qn/Qnb complementary), Format_A [1:0]/B [1:0] = 11, SKY535x3 only

4. Power Supply (V_{DD} and V_{DDOx})

The device includes separate core (V_{DD}) and output driver supplies (V_{DDOx}). This feature allows the V_{DDO} to operate at a lower voltage than the core V_{DD}, reducing current consumption in mixed supply operations. The core V_{DD} supports 3.3, 2.5, or 1.8 V. Control signals, such as SDA and SCLK, are in the V_{DD} domain. Each output bank has its own V_{DDOx} supply, supporting 3.3, 2.5, or 1.8 V.

4.1. Power Supply Sequencing

All power supplies must ramp in a monotonic, linear fashion. When powering the V_{DD} and V_{DDOx} pins from separate supply rails, it is recommended for the supplies to reach their regulation point at approximately the same time while ramping up, or reach ground potential at the same time while ramping down. Clock inputs should not be driven until V_{DD} has reached the recommended minimum levels. V_{DD} must be equal to, or greater than, V_{DDOx}.

4.2. REFOUT Power Modes and Glitchless Switching

Powering down the REFOUT may enable additional power savings. To ensure that the enable and disable functions are glitchless, the sequencing noted in Table 8 must be followed.

Table 8. Glitchless REFOUT Enable/Disable

REFOUT_PWR	OE_REFOUT	Additional Power Savings	User Action for Glitchless OE
1	0 → 1	No	No extra user action needed
1	1 → 0	No	No extra user action needed
0 → 1	0 → 1	No	REFOUT_PWR should lead OE_REFOUT by 10 ms
1 → 0	1 → 0	Yes	OE_REFOUT should lead REFOUT_PWR by three clock cycles (min)

5. Electrical Specifications

Table 9. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_S		–55	—	150	°C
Supply voltage	V_{DD}, V_{DDOA}, V_{DDOB}, V_{DDOC}		–0.5	—	3.8	V
Input voltage	V_{IN}		–0.5	—	V_{DD} + 0.3	V
Output voltage	V_{OUT}		—	—	V_{DDOx} + 0.3	V
ESD sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	—	—	2000	V
ESD sensitivity	CDM		—	—	500	V
Peak soldering reflow temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum junction temperature	T_J		—	—	125	°C

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 10. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient operating temperature	T_A	JEDEC Board, 4-layer	–40	—	85	°C
		8-layer Board	–40	—	95	°C
Board operating temperature	T_B		–40	—	105	°C
Core supply voltage range[1]	V_{DD}	LVCMOS, S-LVDS, HCSL input clock(s)	1.71	1.8	1.89	V
		LVCMOS, LVDS, LVPECL, HCSL input clock(s)	2.37	2.5	2.63	V
		LVCMOS, LVDS, LVPECL, HCSL input clock(s)	3.13	3.3	3.47	V
Output buffer supply voltage range	V_{DDOA} V_{DDOB}	S-LVDS, HCSL, LVCMOS	1.71	1.8	1.89	V
		LVDS, LVPECL, HCSL, LVCMOS	2.37	2.5	2.63	V
		LVDS, LVPECL, HCSL, LVCMOS	3.13	3.3	3.47	V
Reference output supply voltage range	V_{DDOC}	LVCMOS	1.71	1.8	1.89	V
			2.37	2.5	2.63	V
			3.13	3.3	3.47	V

1. Core supply V_{DD} and output buffer supplies V_{DDOx} are independent. $V_{DDOx} \leq V_{DD}$.

Table 11. Input Clock Specifications

(V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential input common-mode voltage	V_{CM}	V_{DD} = 2.5 V ± 5%, 3.3 V ± 5%	0.25	—	V_{DD} – 1.1	V
		V_{DD} = 1.8 V ± 5%	0.25	—	V_{DD} – 0.8	V
Differential input swing (peak-to-peak)	V_{IN}	V_{DD} = 2.5 V ± 5%, 3.3 V ± 5%	0.20	—	2.2	V
		V_{DD} = 1.8 V ± 5%	0.20	—	V_{DD} + 0.3	V
Input slew rate[1]	SR	Differential input	3.0	—	—	V/ns
		Single-ended input	1.0	—	—	V/ns
LVCMOS input high voltage	V_{IH}		V_{DD} × 0.7	—	—	V
LVCMOS input low voltage	V_{IL}		—	—	V_{DD} × 0.3	V
Input frequency	F_{IN}	CLK0/CLK0b and CLK1/CLK1b, differential Input	DC	—	3100	MHz
		CLK0 and CLK1 pins, Single ended input	DC	—	250	MHz
		XA pin (driven single-ended, ac) input clock duty cycle 50%, output clock duty cycle 45% min/55% max.	0.1	—	100	MHz
		XA pin (driven single-ended, ac) input clock duty cycle 50%, output clock duty cycle 40% min/60% max.	100	—	250	MHz
Crystal frequency	F_{XTAL}	Fundamental mode crystal[2]	24		54	MHz
Input capacitance	C_{IN}	CLK0 and CLK1 pins with respect to GND	—	2.5	—	pF
		XA with respect to GND	—	4	—	pF
Input pulse width	T_W	Applies to low frequency input signals (1PPS, PP2S)	40	—	—	ns

1. Required to meet prop delay and additive jitter specifications (20-80%). The device functions with a slower slew rate but may have increased jitter.
2. Max crystal ESR for 24 MHz = 50 Ω, 54 MHz = 25 Ω; C_L = 8 pF, $C_0 \leq 2$ pF; from Figure 16 on page 17: $C_{1(XA)}$ = 6.8 pF; $C_{2(XB)}$ = 8 pF. These values are based on the PCB layout used for characterization; equations for calculating these values for other layouts are provided in AN1405.

Table 12. DC Common Characteristics

(V_{DD}/V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current	I_{DD}	3.3 V	—	92	120	mA
		2.5 V	—	87	115	mA
		1.8 V	—	78	110	mA
Output buffer supply current (per clock output) at 156.25 MHz (differential)	I_{DDOx}	LVPECL (3.3 V)	—	32	36	mA
		LVDS (3.3 V)	—	10	12	mA
		800 LVDS (3.3V)	—	18	23	mA
		HCSL 600 mV (3.3 V)	—	19	24	mA
		HCSL 700 mV (3.3 V)	—	22	27	mA
		HCSL 800 mV (3.3 V)	—	25	29	mA
		HCSL 1200 mV (3.3 V)	—	27	30	mA
		Single-ended CMOS (1.8 V)	—	9	14	mA
		Single-ended CMOS (2.5 V)	—	12	20	mA
		Single-ended CMOS (3.3 V)	—	15	25	mA
		Dual CMOS complementary or in-phase (1.8 V)	—	17	23	mA
		Dual CMOS complementary or in-phase (2.5 V)	—	23	32	mA
		Dual CMOS complementary or in-phase (3.3 V)	—	29	39	mA
REFOUT buffer supply current at 200 MHz	I_{DDREF}	CMOS (1.8 V)[1]	—	8	11	mA
		CMOS (2.5 V)[1]	—	12	15	mA
		CMOS (3.3 V)[1]	—	18	21	mA
Input high voltage	V_{IH}	SFOUTx, CLK_SELx, OE_REF	0.7 × VDD	—	—	V
Input low voltage	V_{IL}	SFOUTx, CLK_SELx, OE_REF	—	—	0.3 × VDD	V
Internal pull-down resistor	R_{PD}	SFOUTx, CLK_SELx, OE_REF	—	45	—	kΩ

1. Output capacitance load ≤ 5 pF for V_{DDOC} = 1.8 V, C_L ≤ 10 pF for V_{DDOC} = 2.5 V, C_L ≤ 15 pF for V_{DDOC} = 3.3 V

Table 13. LVPECL Output Characteristics[1]

($V_{DDOA/B}$ = 2.5 V ± 5% or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output frequency	F_{OUT}	Full amplitude, $V_{OD} \geq$ 600 mV, V_{DDOx} = 2.5 V	DC	—	1275	MHz
		Full amplitude, $V_{OD} \geq$ 600 mV, V_{DDOx} = 3.3 V	DC	—	1325	MHz
		67% amplitude, $V_{OD} \geq$ 400 mV, V_{DDOx} = 2.5 V	1275	—	2350	MHz
		67% amplitude, $V_{OD} \geq$ 400 mV, V_{DDOx} = 3.3 V	1325	—	3100	MHz
Output rise/fall time	t_R/t_F	LVPECL, 20/80%, 3.3 V	—	200	225	ps
		LVPECL, 20/80%, 2.5 V	—	185	220	ps
Output dc common mode voltage	V_{CMO}		V_{DDOx} – 1.5	V_{DDOx} – 1.3	V_{DDOx} – 1.0	V
Output high voltage	V_{OH}	T_A = 25 °C, dc measurement, R_p = 50 Ω to V_{DDOx} – 2 V	V_{DDOx} – 1.2	V_{DDOx} – 0.9	V_{DDOx} – 0.6	V
Output low voltage	V_{OL}		V_{DDOx} – 2.0	V_{DDOx} – 1.7	V_{DDOx} – 1.4	V
Output voltage swing	V_{OD}		600	800	1000	mV
Output duty cycle	DC	Input clock must have 50% duty cycle	45	50	55	%
Additive noise floor $f_{offset} \geq$10 MHz	NF	F_{OUT} = 156.25 MHz	—	–166	—	dBc/Hz
Propagation delay	T_{PLH}, T_{PHL}	CLK0 or CLK1 input pins to output driver pins	575	765	1070	ps

1. Unused outputs should be left floating. Do not short unused outputs to ground.

Table 14. LVDS Output Characteristics[1]

($V_{DDOA/B}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVDS						
Output frequency	F_{OUT}	Full amplitude, $V_{OD} \geq$ 247 mV	0	—	2200	MHz
		67% amplitude, $V_{OD} \geq$ 167 mV	2200	—	3000	MHz
Delta V_{OD}	ΔV_{OD}		—	—	50	mV
Offset voltage (V_{DDOx} = 2.5 V or 3.3 V)	V_{OS}	V_{DDOx} = 2.37 to 2.63 V, 3.13 to 3.47 V, R_L = 100 Ω across Qn and Qnb	1.15	1.2	1.25	V
Offset voltage (V_{DDOx} = 1.8 V)		V_{DDOx} = 1.71 to 1.89 V, R_L = 100 Ω across Qn and Qnb	0.85	0.9	0.95	V
Delta V_{OS}	ΔV_{OS}		—	—	50	mV
Output rise/fall time[2]	t_R/t_F	LVDS, 20/80%	—	200	260	ps
Output voltage swing	V_{OD}	R_L = 100 Ω across Qn and Qnb	247	390	454	mV
Output duty cycle	DC	$F_{OUT} \leq$ 3000 MHz, Input clock must have 50% duty cycle, 800 mV V_{IN}, ac-coupled	45	50	55	%
Additive noise floor, $f_{offset} \geq$10 MHz	NF	F_{OUT} = 156.25 MHz	—	–165	—	dBc/Hz

Table 14. LVDS Output Characteristics[1] (Continued)

($V_{DDOA/B}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay	T_{PLH}, T_{PHL}	CLK0 or CLK1 input pins to output driver pins	560	825	1145	ps
800 mV LVDS						
Output frequency	F_{OUT}	Full amplitude, V_{OD} > 400 mV	0	—	3000	MHz
Delta V_{OD}	ΔV_{OD}		—	—	50	mV
Offset voltage (V_{DDOx} = 2.5 V or 3.3 V)	V_{OS}	V_{DDOx} = 2.37 to 2.63 V, 3.13 to 3.47 V, R_L = 100 Ω across Qn and Qnb	1.15	1.2	1.25	V
Offset voltage (V_{DDOx} = 1.8 V)		V_{DDOx} = 1.71 to 1.89 V, R_L = 100 Ω across Qn and Qnb	0.85	0.9	0.95	V
Delta V_{OS}	ΔV_{OS}		—	—	50	mV
Output rise/fall time[2]	t_R/t_F	LVDS, 20/80%	—	200	260	ps
Output voltage swing	V_{OD}	R_L = 100 Ω across Qn and Qnb	400	780	910	mV
Output duty cycle	DC	F_{OUT} <= 3000 MHz, input clock must have 50% duty cycle, 800 mV V_{IN}, ac-coupled	45	50	56	%
Additive noise floor, f_{offset} >10 MHz	NF	F_{OUT} = 156.25 MHz	—	–166	—	dBc/Hz
Propagation delay	T_{PLH}, T_{PHL}	CLK0 or CLK1 input pins to output driver pins	560	825	1145	ps

1. Unused outputs should be left floating. Do not short unused outputs to ground.
2. Rise/fall time measurements were taken with the oscilloscope timescale reduced to capture one rising or falling edge within the measurement window. This was done to minimize the impact of the oscilloscope sampling rate and channel memory depth on the measurement. Rise/fall time measurement values will increase if a larger timescale is used without sufficient sampling rate and channel memory depth to maintain a sufficiently small horizontal resolution.

Table 15. HCSL Output Characteristics[1,2]

($V_{DDOA/B}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output frequency[3]	F_{OUT}	Full amplitude	0	—	650	MHz
		67% amplitude	650	—	800	MHz
Output rise/fall time[4]	t_R/t_F	20/80%	—	300	400	ps
Single-ended output swing	V_{SE}	HCSL 600 mV: dc measurement, R_L = 50 Ω to ground	0.40	0.60	0.80	V
		HCSL 700 mV: dc measurement, R_L = 50 Ω to ground	0.50	0.70	0.90	
		HCSL 800 mV: dc measurement, R_L = 50 Ω to ground	0.60	0.80	1.0	
		HCSL 1200 mV: dc measurement, R_L = 50 Ω to ground	1.00	1.20	1.40	
Output duty cycle	DC	Input clock must have 50% duty cycle	45	50	55	%
Additive noise floor, f_{offset} >10 MHz	N_{FLOOR}	F_{OUT} = 156.25 MHz	—	–166	—	dBc/Hz
Propagation delay	T_{PLH}, T_{PHL}	CLK0 or CLK1 input pins to output driver pins; all HCSL swings	575	820	1110	ps

Table 15. HCSL Output Characteristics[1,2] (Continued)

($V_{DDOA/B}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise-fall matching	R/F_{Match}	100 MHz PCIe reference clock as source, with/without spread spectrum[5]	—	10	—	%
Variation of fall time over all falling clock edges	T_{Fall_Delta}		—	20	—	ps
Variation of rise time over all rising clock edges	T_{Rise_Delta}		—	15	—	ps
Absolute crossing point voltage (V)	V_{Cross}		0.33	0.4	0.48	V
Variation of crossing point over all rising clock edges	V_{Cross_Delta}		—	40	—	mV
Overshoot voltage	V_{Ovs}		–20	—	40	mV
Undershoot voltage	V_{Uds}		–20	—	40	mV
Ring-back voltage	V_{Rb}		—	—	80	mV

1. Unused outputs should be left floating. Do not short unused outputs to ground.
2. DC-coupled HCSL clock output termination. See Figure 19 on page 18.
3. Full amplitude, V_{OD} > single-ended output swing minimum. 67% amplitude, V_{OD} > (0.67 x single-ended output swing minimum).
4. Rise/fall time measurements were taken with the oscilloscope timescale reduced to capture one rising or falling edge within the measurement window. This was done to minimize the impact of the oscilloscope sampling rate and channel memory depth on the measurement. Rise/fall time measurement values will increase if a larger timescale is used without sufficient sampling rate and channel memory depth to maintain a sufficiently small horizontal resolution.
5. Parameters measured with Skyworks PCI Express Clock Jitter Tool on a 100 MHz HCSL load-terminated clock waveform with/without spread spectrum, over at least 100,000 clock periods.

Table 16. LVCMOS Output Characteristics

(V_{DDOC} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REFOUT						
Noise floor f_{offset} ≥10 MHz	NF	V_{DDOC} = 3.3 V, F_{out} = 156.25 MHz	—	–164	—	dBc/Hz
REFOUT output enable time[1]	T_{EN_REF}	F ≤250 MHz	—	3	4	Clock cycles
REFOUT output disable time[1]	T_{DIS_REF}	F ≤250 MHz	—	3	4	Clock cycles
Output frequency	F_{OUT}		0	—	250	MHz
Output voltage high	V_{OH}	I_{OUT} = –1 mA	0.9 × V_{DDOC}	—	—	V
		I_{OUT} = –10 mA	0.75 × V_{DDOC}	—	—	V
Output voltage low	V_{OL}	I_{OUT} = 1 mA	—	—	0.1 × V_{DDOC}	V
		I_{OUT} = 10 mA	—	—	0.25 × V_{DDOC}	V
Output rise/fall time[2]	t_R/t_F	20%/80%, 1.8 V, C_L = 5 pF, 50 Ω load impedance	—	640	750	ps
		20%/80%, 2.5 V, C_L = 10 pF, 50 Ω load impedance	—	775	910	ps
		20%/80%, 3.3 V, C_L = 15 pF, 50 Ω load impedance	—	1030	1220	ps
Output duty cycle	DC	C_L = 5 pF, input clock must have 50% duty cycle	45	50	55	%

Table 16. LVCMOS Output Characteristics (Continued)

(V_{DDOC} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay	T_{PLH}, T_{PHL}	V_{DD} = V_{DDOC} = 1.8 V, C_L = 5 pF V_{DD} = V_{DDOC} = 2.5 V, C_L = 10 pF V_{DD} = V_{DDOC} = 3.3 V, C_L = 15 pF CLK0 or CLK1 input pins to REFOUT pin impedance	1200	1825	2370	ps
Qn OUT						
Noise floor f_{offset} ≥10 MHz	NF	$V_{DDOA/B}$ = 3.3 V, F_{out} = 156.25 MHz	—	–165	—	dBc/Hz
Output frequency	F_{OUT}		0	—	250	MHz
Output voltage high	V_{OH}	I_{OUT} = –1 mA	0.9 × V_{DDO}	—	—	V
		I_{OUT} = –10 mA	0.75 × V_{DDO}	—	—	V
Output voltage low	V_{OL}	I_{OUT} = 1 mA	—	—	0.1 × V_{DDO}	V
		I_{OUT} = 10 mA	—	—	0.25 × V_{DDO}	V
Output rise/fall time	t_R/t_F	20%/80%: V_{DD} = V_{DDOx} = 1.8 V, C_L = 5 pF V_{DD} = V_{DDOx} = 2.5 V, C_L = 5 pF V_{DD} = V_{DDOx} = 3.3 V, C_L = 5 pF	—	575	800	ps
Output duty cycle	DC	C_L = 5 pF, input clock must have 50% duty cycle	45	50	55	%
Propagation delay	T_{PLH}, T_{PHL}	V_{DD} = V_{DDOx} = 1.8 V, C_L = 5 pF V_{DD} = V_{DDOx} = 2.5 V, C_L = 5 pF V_{DD} = V_{DDOx} = 3.3 V, C_L = 5 pF CLK0 or CLK1 input pins to output driver pins	800	1100	1350	ps

1. Four clock cycles are only possible when the OE_REF enable signal is asynchronous to the clock input signal.
2. Rise/fall time measurements were taken with the oscilloscope timescale reduced to capture one rising or falling edge within the measurement window. This was done to minimize the impact of the oscilloscope sampling rate and channel memory depth on the measurement. Rise/fall time measurement values will increase if a larger timescale is used without sufficient sampling rate and channel memory depth to maintain a sufficiently small horizontal resolution.

Table 17. Common Output Characteristics

(V_{DD}, $V_{DDOA/B/C}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Buffer mode startup time	T_{SBUF}	From V_{DDOx} = 1.55 V to outputs enabled	—	—	30	ms
Crystal mode startup time[1]	T_{SOSC}	From V_{DD} = 1.55 V to outputs enabled	—	—	100	ms
Crystal mode VDD ramp[2]	T_{ROSC}	From V_{DD} = 1.55 V to outputs enabled	—	—	26	ms
Crystal mode jitter	T_{JXO}	24 MHz fundamental crystal, V_{DD} = 1.8 V ±5% or 2.5 V ±5%, 10 kHz to 1 MHz integration bandwidth	—	96	125	fs
		24 MHz fundamental crystal, V_{DD} = 3.3 V ±5%, 10 kHz to 1 MHz integration bandwidth	—	67	110	fs
		54 MHz fundamental crystal, V_{DD} = 1.8 V ±5% or 2.5 V ±5%, 12 kHz to 20 MHz integration bandwidth	—	150	185	fs
		54 MHz fundamental crystal, V_{DD} = 3.3 V ±5%, 12 kHz to 20 MHz integration bandwidth	—	100	130	fs
Output enable time[3]	T_{EN}	Hi-Z to LVPECL/LVDS/HCSL/LVCMOS	—	—	15	µs
Output disable time	T_{DIS}	LVPECL/LVDS/HCSL/LVCMOS to Hi-Z	—	15	50	ns
Output-to-output skew	T_{Skew}	HCSL	—	3	50	ps
		LVDS	—	3	50	ps
		800 mV LVDS	—	3	50	ps
		LVPECL	—	3	50	ps
		LVCMOS	—	3	75	ps
Supply voltage ramp rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms
Part-to-part skew	T_{PS}	Same differential format, load, temp, voltage, and output channel between devices	—	17	110	ps
Power supply noise rejection[4] F_{IN} = 156.25 MHz	PSNR	HCSL	—	–75	—	dBc
		LVDS	—	–75	—	dBc
		LVPECL	—	–69		dBc
Power supply noise rejection[4] F_{IN} = 312.5 MHz	PSNR	HCSL	—	–69	—	dBc
		LVDS	—	–69	—	dBc
		LVPECL	—	–63	—	dBc
Input-to-output crosstalk, CLKIN0 to CLKIN1	XTALK	F_{OFFSET} ≥50 kHz, Input = LVDS, F_{IN} = 100 MHz	—	–78.5	—	dBc
		F_{OFFSET} ≥50 kHz, Input = LVDS, F_{IN} = 200 MHz	—	–82.5	—	dBc
		F_{OFFSET} ≥50 kHz, Input = LVDS, F_{IN} = 500 MHz	—	–90	—	dBc
		F_{OFFSET} ≥50 kHz, Input = LVDS, F_{IN} = 1000 MHz	—	–78.5	—	dBc

1. Applies any time device is powered up, and/or the input clock source is switched from CLK0/1 to XTAL or ac-coupled XA mode.
2. Applies only when powering up while the crystal oscillator input is selected.
3. When enabling outputs from Hi-Z, the first edge out is a rising edge and the first period out is a full period. Output frequencies <1 MHz may add up to one full period to the enable time given here.
4. Sine wave noise added to V_{DDOx} (100 mVpp at V_{DDOx} = 3.3 V), and noise spur amplitude measured at 100 kHz frequency offset from carrier. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

Table 18. Additive Jitter (Differential Clock Input)

(V_{DD}, V_{DDOx} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%,T_A = –40 to 95 °C)

Clock Frequency (MHz)[1,2]	V_{DD} Nominal	Output Format	Additive Jitter, fs RMS											
			10 kHz to 1 MHz[3]		10 kHz to 20 MHz[3]		12 kHz to 20 MHz[3]		1 MHz to 20 MHz[3]		12 kHz to 20 MHz, 4 MHz HPF[3]		12 kHz to 20 MHz, 4 MHz to 16 MHz BPF[3]	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
SKY535x2														
156.25 MHz	1.8, 2.5, 3.3	HCSL all levels	11	18	37	49	37	49	35	47	31	41	24	33
625 MHz	1.8, 2.5, 3.3	HCSL all levels	9	14	18	26	18	26	16	23	14	20	11	16
SKY535x3														
100 MHz	1.8, 2.5, 3.3	LVCMOS	26	44	47	65	46	65	39	58	33	51	27	41
156.25 MHz	2.5, 3.3	LVPECL	11	17	35	47	35	47	34	45	29	39	23	31
	1.8, 2.5, 3.3	2 x LVDS	13	19	41	52	41	52	39	50	34	43	27	35
	1.8, 2.5, 3.3	800 mV LVDS	9	17	29	46	29	46	27	44	24	39	19	32
	1.8, 2.5, 3.3	LVCMOS	21	32	38	53	37	53	31	46	27	39	22	33
625 MHz	2.5, 3.3	LVPECL	9	14	18	26	18	26	16	23	14	20	11	16
	1.8, 2.5, 3.3	LVDS	9	14	19	28	19	28	16	24	14	21	11	17
	1.8, 2.5, 3.3	800 mV LVDS	8	14	16	26	16	26	14	22	12	20	10	16

1. For best additive jitter results, use the fastest input clock slew rate possible.
   See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. AC-coupled differential inputs, differential amplitude V_{IN} = 0.5 V (single-ended, peak-to-peak), 3 V/ns (20% to 80% slew rate).
3. Measured differentially using a balun at the phase noise analyzer input.

Table 19. Additive Jitter (Single-Ended Clock Input)

(V_{DD}, V_{DDOx} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%,T_A = –40 to 95 °C)

Clock Frequency (MHz)[1,2,3]	V_{DD} Nominal	Output Format	Additive Jitter, fs RMS											
			10 kHz to 1 MHz[4]		10 kHz to 20 MHz[4]		12 kHz to 20 MHz[4]		1 MHz to 20 MHz[4]		12 kHz to 20 MHz, 4 MHz HPF[4]		12 kHz to 20 MHz, 4 MHz to 16 MHz BPF[4]	
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
SKY535x2														
156.25 MHz	1.8, 2.5, 3.3	HCSL all levels	17	30	45	72	45	72	42	76	36	65	29	53
SKY535x3														
100 MHz	1.8, 2.5, 3.3	LVCMOS	29	49	63	142	63	142	56	135	49	117	39	95
156.25 MHz	2.5, 3.3	LVPECL	17	26	45	78	45	78	42	66	36	65	29	53
	1.8, 2.5, 3.3	LVDS	21	31	64	85	64	85	61	82	53	72	43	60
	1.8, 2.5, 3.3	2 x LVDS	13	29	43	84	43	84	41	80	36	70	29	56
	1.8, 2.5, 3.3	LVCMOS	23	36	48	92	48	92	42	86	37	74	30	60

1. For best additive jitter results, use the fastest input clock slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. Measurements taken using input clock termination noted in Figure 13 on page 15 and Figure 15 on page 16.
3. Single-ended clock input, differential amplitude V_{IN} = 2.18 V for V_{DD} = 2.5 V and 3.3 V; V_{IN} = 1.2 V for V_{DD} = 1.8 V (single-ended, peak-to-peak), 1 V/ns (20% to 80% slew rate).
4. Measured differentially using a balun at the phase noise analyzer input.

Table 20. 100 MHz PCIe Jitter Performance Characteristics (with/without Spread Spectrum)[1]

V_{DD} = V_{DDOx} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 5%, T_A = –40 to 95 °C

Parameter	Comment	Min	Typ	Max	PCI-SIG Limit[2]	Units
100 MHz PCIe common-clock jitter performance[3]	Gen 1 (2.5GT/s)	—	13	23	86	ps PTP
	Gen 2 (5GT/s) low band	—	5	6	3000	fs RMS
	Gen 2 (5GT/s) high band	—	68	139	3100	fs RMS
	Gen 3 (8GT/s)	—	14	32	1000	fs RMS
	Gen 4 (16GT/s)	—	14	32	500	fs RMS
	Gen 5 (32GT/s)	—	4	9	150	fs RMS
	Gen 6 (64GT/s)	—	3	7	100	fs RMS
	Gen 7 (128GT/s)	—	2	5	67	fs RMS
100 MHz PCIe separate reference clock jitter performance[2,3]	Gen 2 (5GT/s) low band	—	1	1	2120	fs RMS
	Gen 2 (5GT/s) high band	—	43	99	2190	fs RMS
	Gen 3 (8GT/s)	—	23	47	707	fs RMS
	Gen 4 (16GT/s)	—	25	49	495	fs RMS
	Gen 5 (32GT/s)	—	5	11	177	fs RMS
	Gen 6 (64GT/s)	—	5	10	106	fs RMS
	Gen 7 (128GT/s)	—	3	7	71	fs RMS

1. Results obtained from using a Skyworks Si5361 Jitter Attenuator as a source clock. Clock parameters: 100 MHz HCSL clock, with/without spread spectrum, 4 V/ns slew rate, 800 mVpp se. Jitter specifications derived using Skyworks PCI Express Clock Jitter Tool v.7.1.
2. PCI-SIG does not specify a jitter limit for separate reference clock architectures. Instead, the PCI-SIG specified simulation limit can be split evenly between transmitter and receiver clocks by dividing by the square root of 2, since their jitter is uncorrelated.
3. Jitter integration as specified by PCI-SIG in the PCI Express® Base Specification Revision 7.0.

Table 21. Thermal Characterization Parameters

Package	Parameter	Symbol	Test Condition	Typical Value		Unit
				JEDEC[1]	EVB[2]	
7 x 7 mm QFN	Thermal resistance parameter (junction to ambient)	θ_{JA}	Still air	26.0	10.1	°C/W
			1 m/s	21.7	8.8	°C/W
			2 m/s	20.8	8.7	°C/W
	Thermal characterization parameter (junction to board)	Ψ_{JB}	Still air	10.7	3.5	°C/W
	Thermal characterization parameter (junction to case-top)	Ψ_{JC}	Still air	0.4	0.6	°C/W
6 x 6 mm QFN	Thermal resistance parameter (junction to ambient)	θ_{JA}	Still air	24.8	11.8	°C/W
			1 m/s	18.8	9.3	°C/W
			2 m/s	17.8	9.1	°C/W
	Thermal characterization parameter (junction to board)	Ψ_{JB}	Still air	8.9	4.4	°C/W
	Thermal characterization parameter (junction to case-top)	Ψ_{JC}	Still air	0.4	0.5	°C/W

Table 21. Thermal Characterization Parameters (Continued)

Package	Parameter	Symbol	Test Condition	Typical Value		Unit
				JEDEC[1]	EVB[2]	
5 x 5 mm QFN	Thermal resistance parameter (junction to ambient)	θ_{JA}	Still air	31.5	11.6	°C/W
			1 m/s	26.6	10.2	°C/W
			2 m/s	25.5	10.1	°C/W
	Thermal characterization parameter (junction to board)	Ψ_{JB}	Still air	14.0	4.4	°C/W
	Thermal characterization parameter (junction to case-top)	Ψ_{JC}	Still air	0.5	0.6	°C/W

1. Based on PCB with dimension 4"x 5", thickness of 1.6 mm, with two layers of copper, epad has 16x vias (12 mil).
2. Based on PCB with dimension 9"x 9", thickness of 1.6 mm, with eight layers of copper, epad has 49x vias (8 mil).

Table 22. I^2C Timing Specifications

Parameter	Symbol	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	—	100	—	400	kHz
SM Bus timeout	—	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$	4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
High period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$	100	—	100	—	ns
Data setup time	$t_{SU:DAT}$	250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20	300	ns
Fall time of both SDA ans SCL signals	t_f	—	300	—	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$	—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$	—	3.45	—	0.9	µs

6. Typical Performance Characteristics

Unless otherwise specified: V_{DD} = 3.3 V, V_{DDOx} = 3.3 V, T_A = 25 °C, input clock driven differentially, input slew rate ≥3 V/ns.

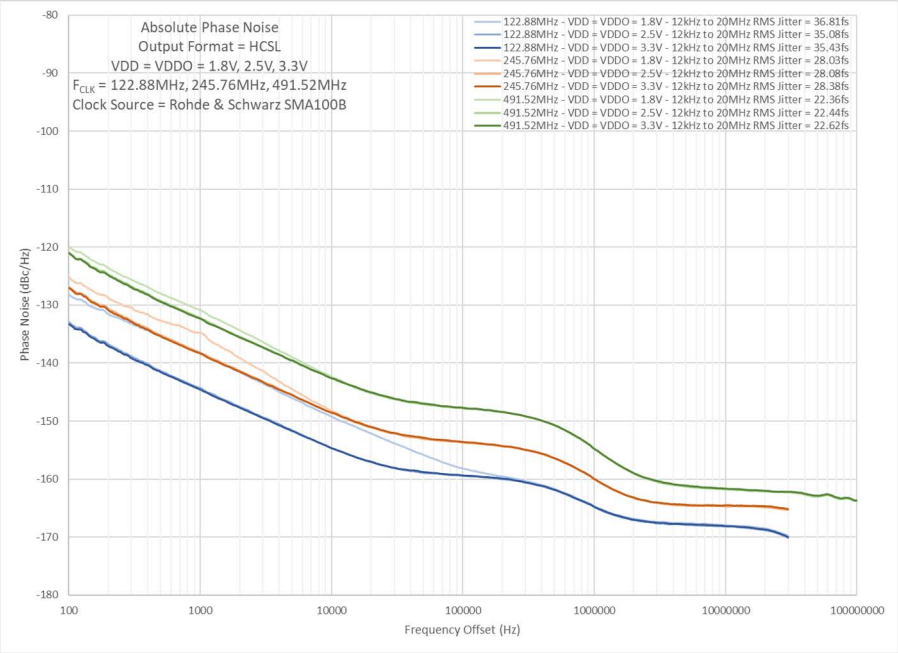


Figure 31. Absolute Phase Noise Differential Input (HCSL: 491.52 MHz, 245.76 MHz, 122.88 MHz)

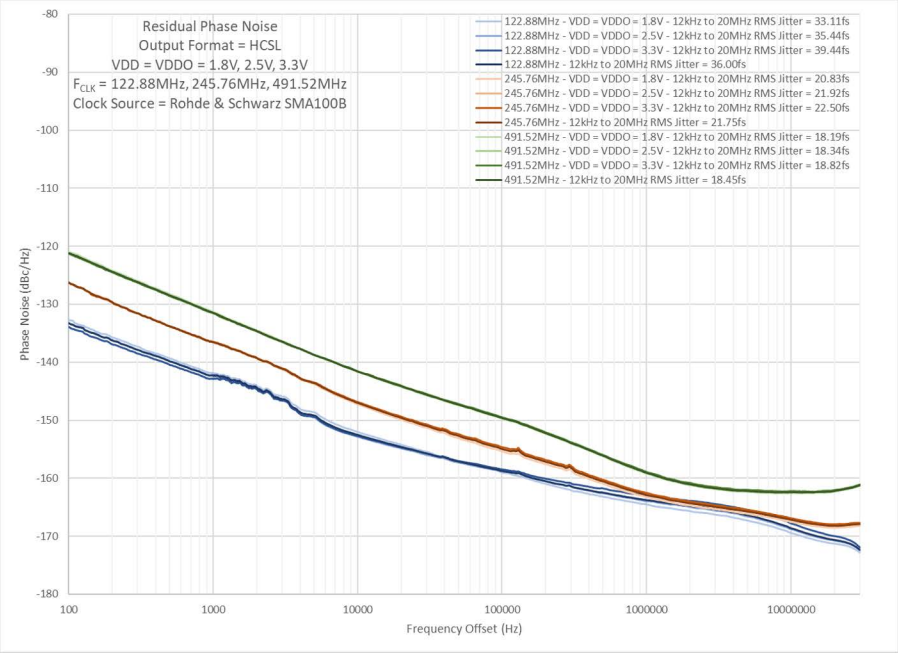


Figure 32. Residual Phase Noise Differential Input (HCSL: 491.52 MHz, 245.76 MHz, 122.88 MHz)

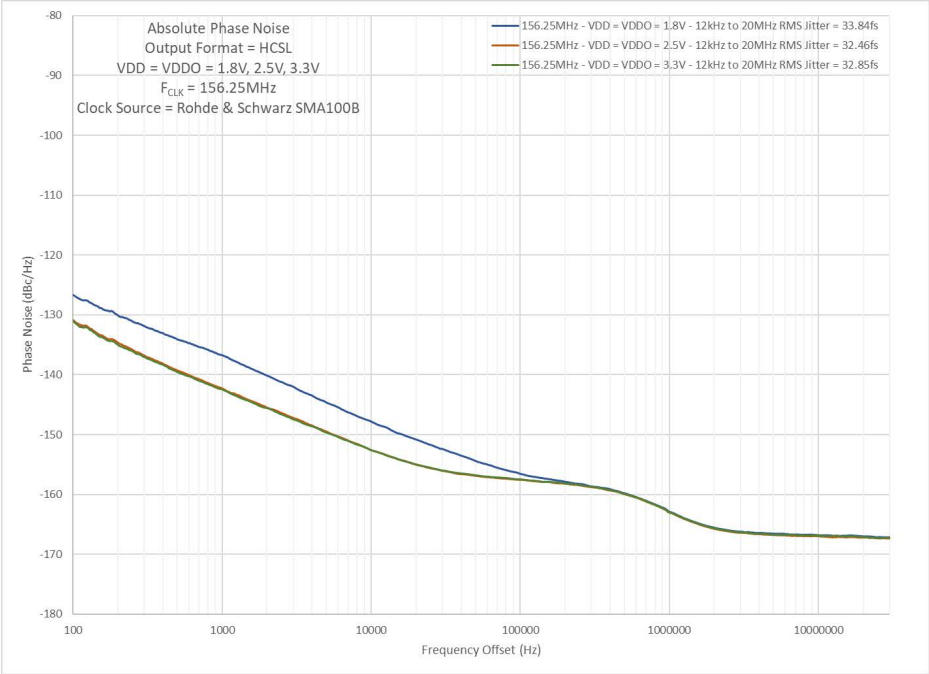


Figure 33. Absolute Phase Noise Differential Input (HCSL: 156.25 MHz)

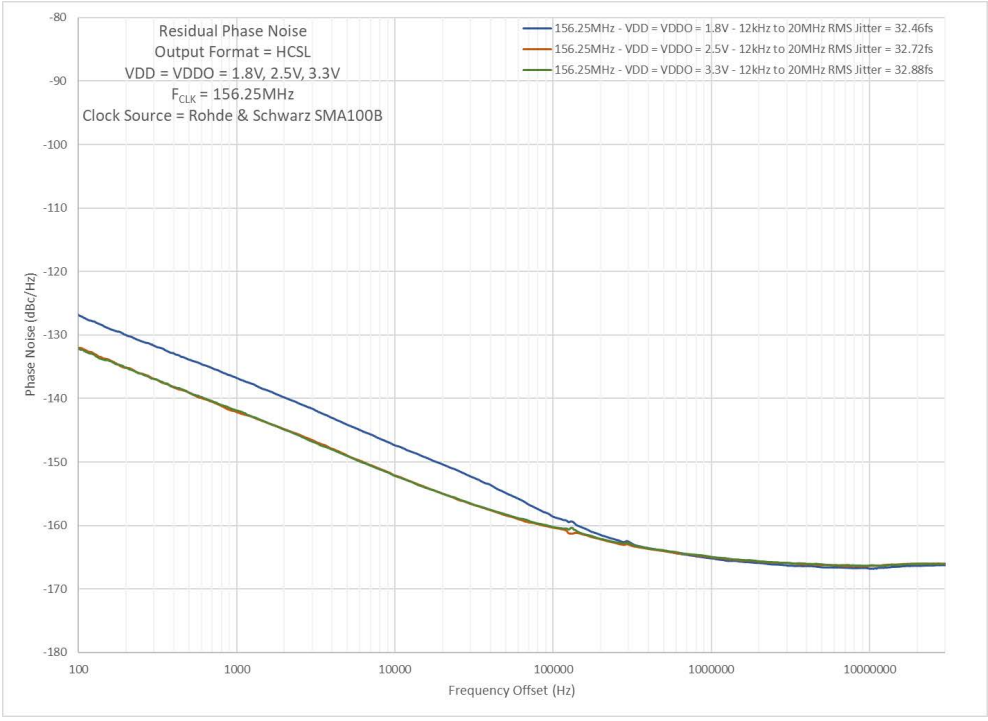


Figure 34. Residual Phase Noise Differential Input (HCSL: 156.25 MHz)

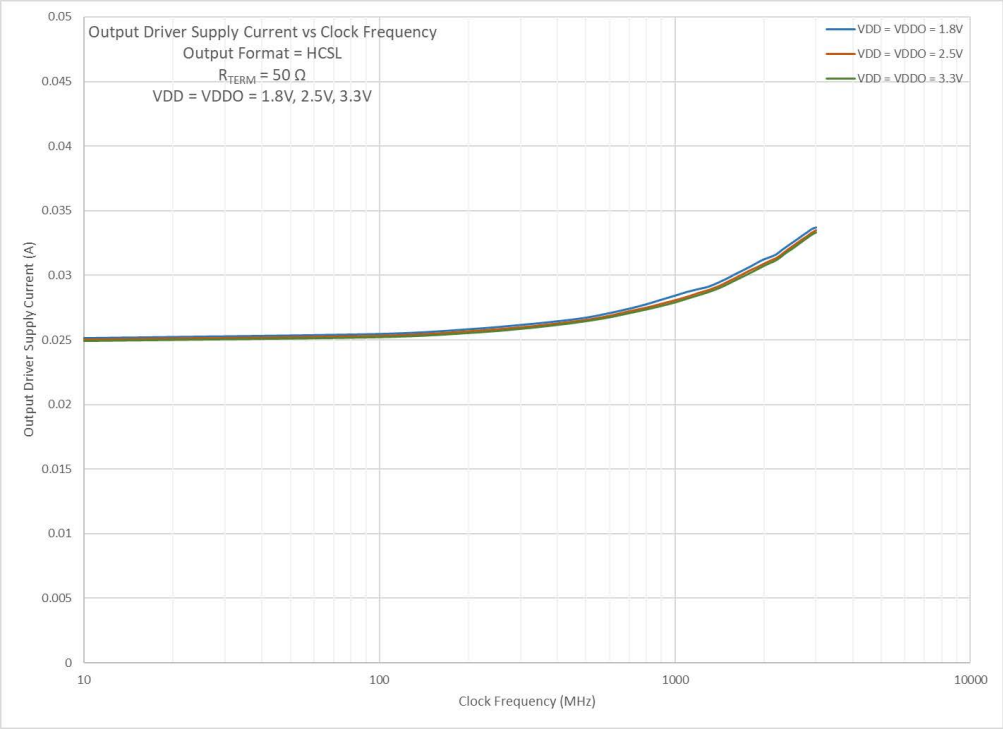


Figure 35. Supply Current Per Output vs. Frequency (HCSL)

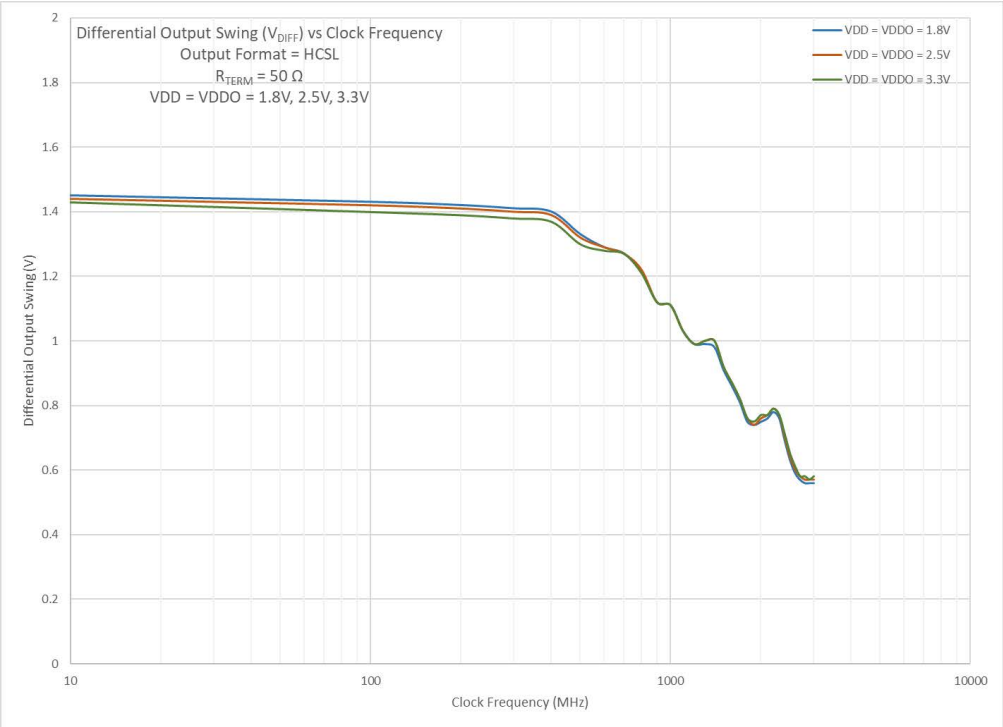


Figure 36. Differential Output Voltage Swing vs. Frequency (1.8 V, 2.5 V, 3.3 V HCSL)

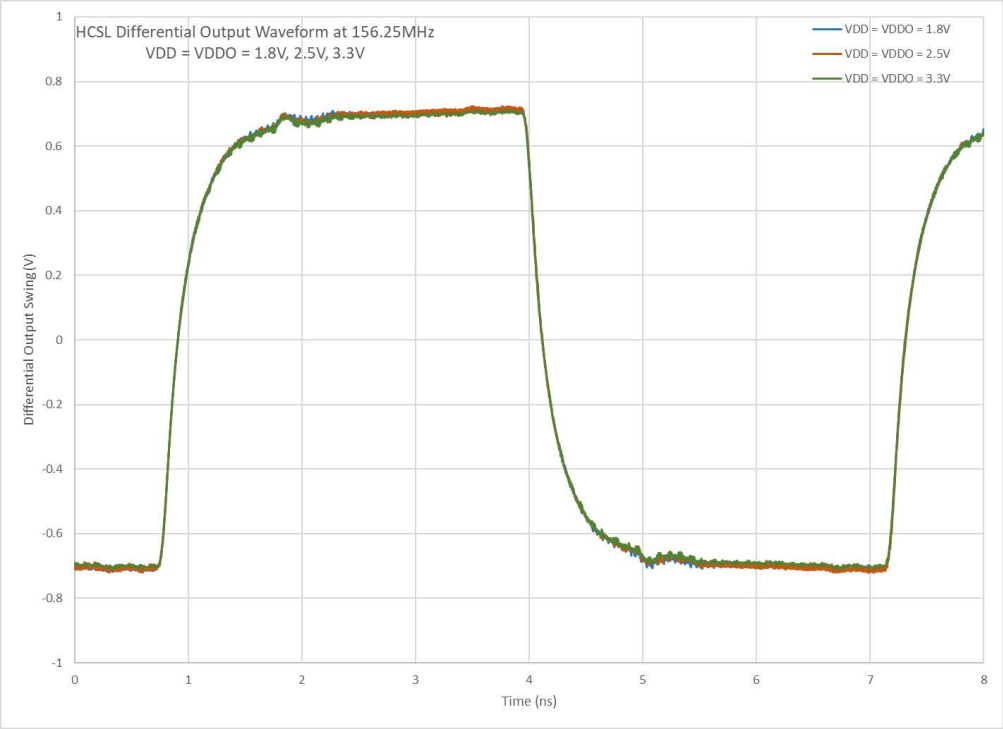


Figure 37. HCSL Differential Output Waveform (156.25 MHz)

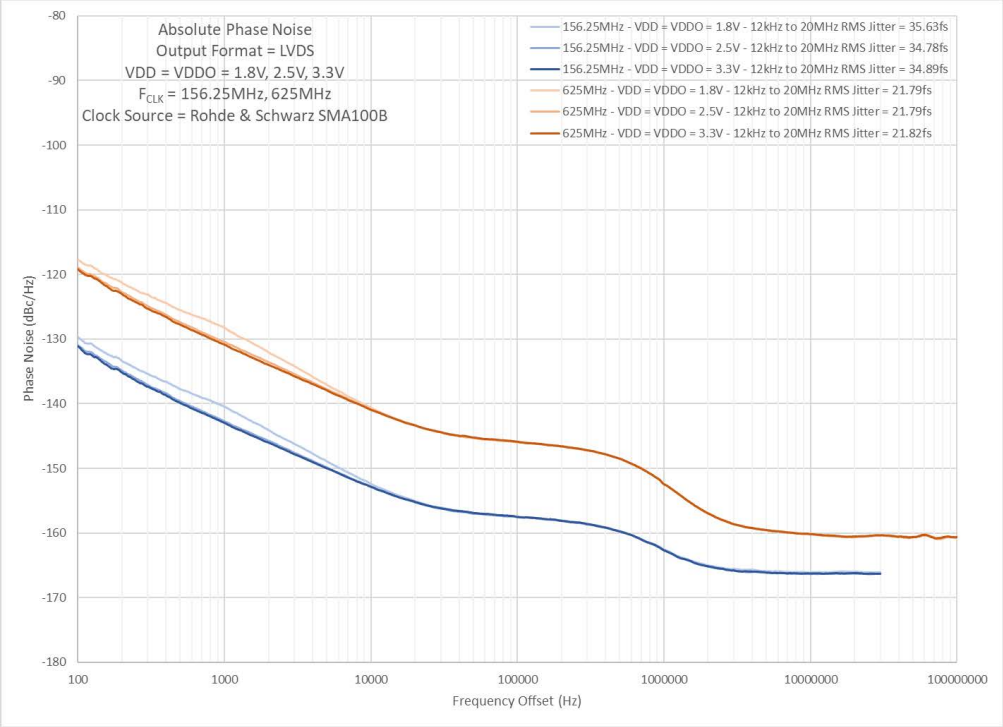


Figure 38. Absolute Phase Noise Differential Input (LVDS: 625 MHz, 156.25 MHz)

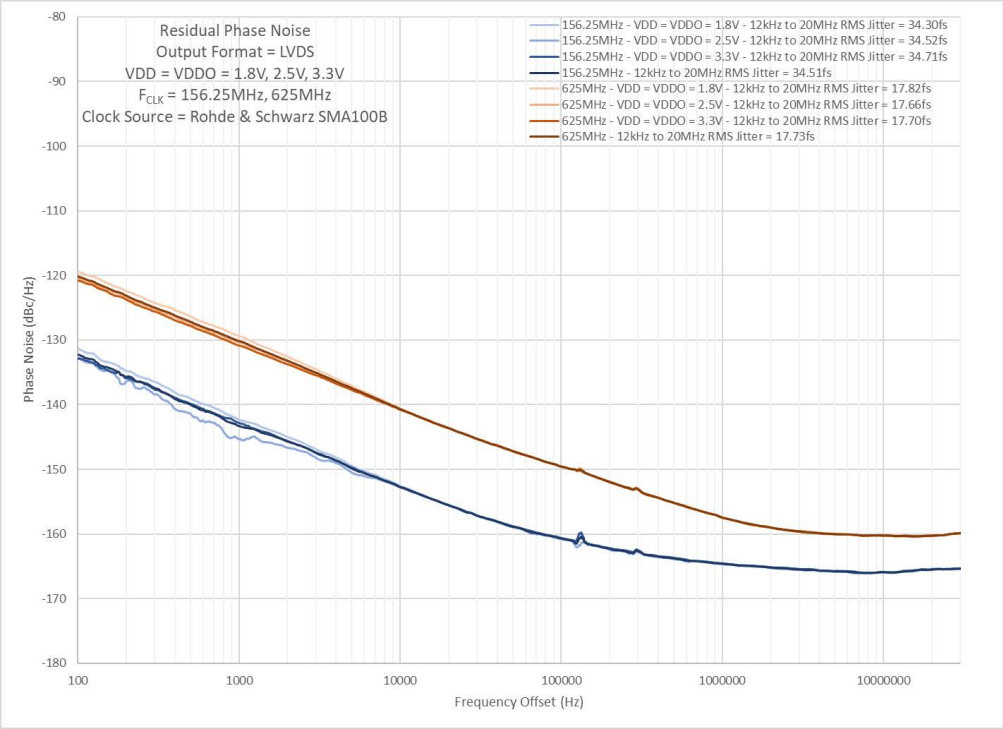


Figure 39. Residual Phase Noise Differential Input (LVDS: 625 MHz, 156.25 MHz)

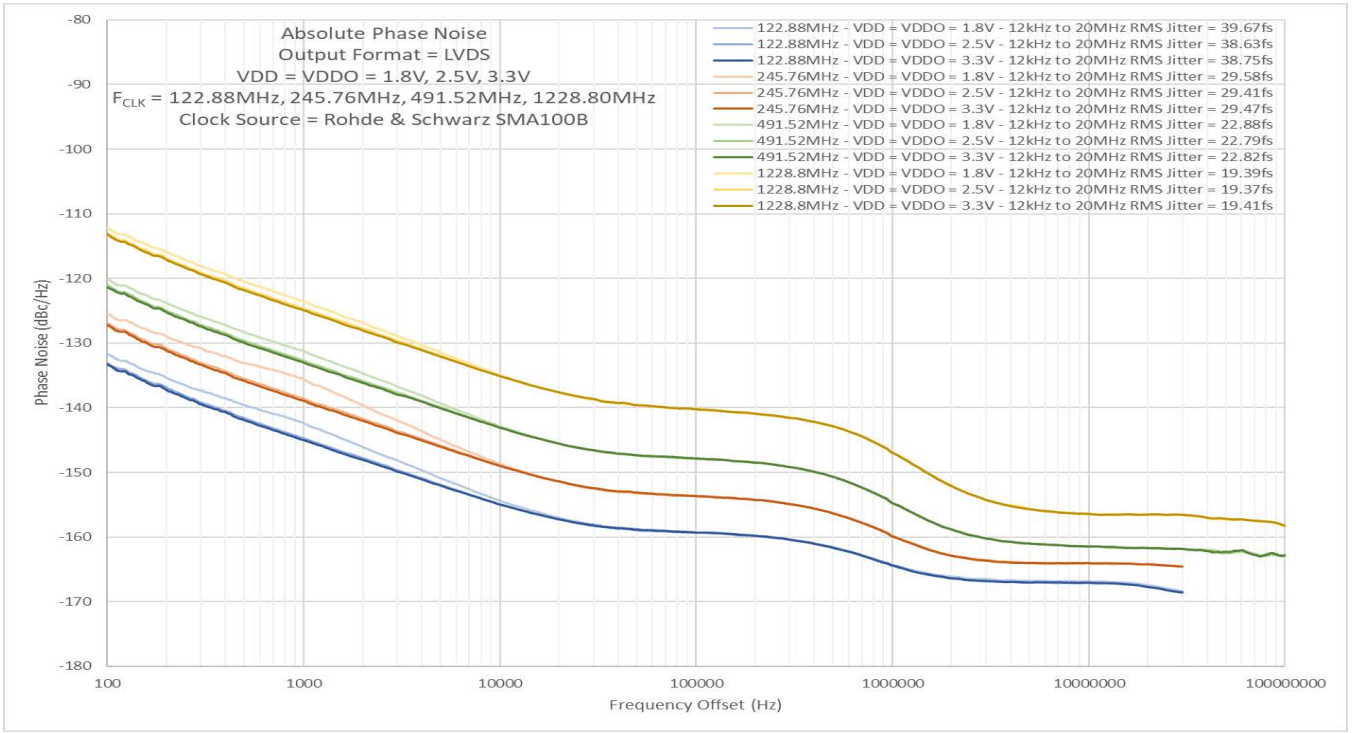


Figure 40. Absolute Phase Noise Differential Input (LVDS: 122.88 MHz, 245.76 MHz, 491.52 MHz, 1228.8 MHz

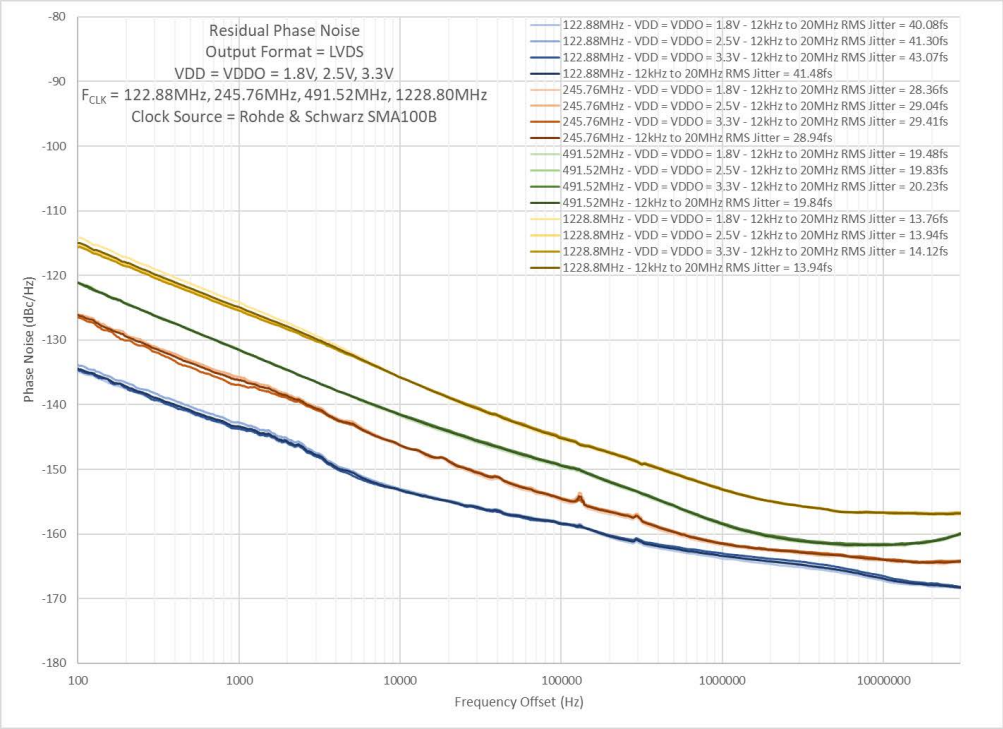


Figure 41. Residual Phase Noise Differential Input (LVDS: 122.88 MHz, 245.76 MHz, 491.52 MHz, 1228.8 MHz)

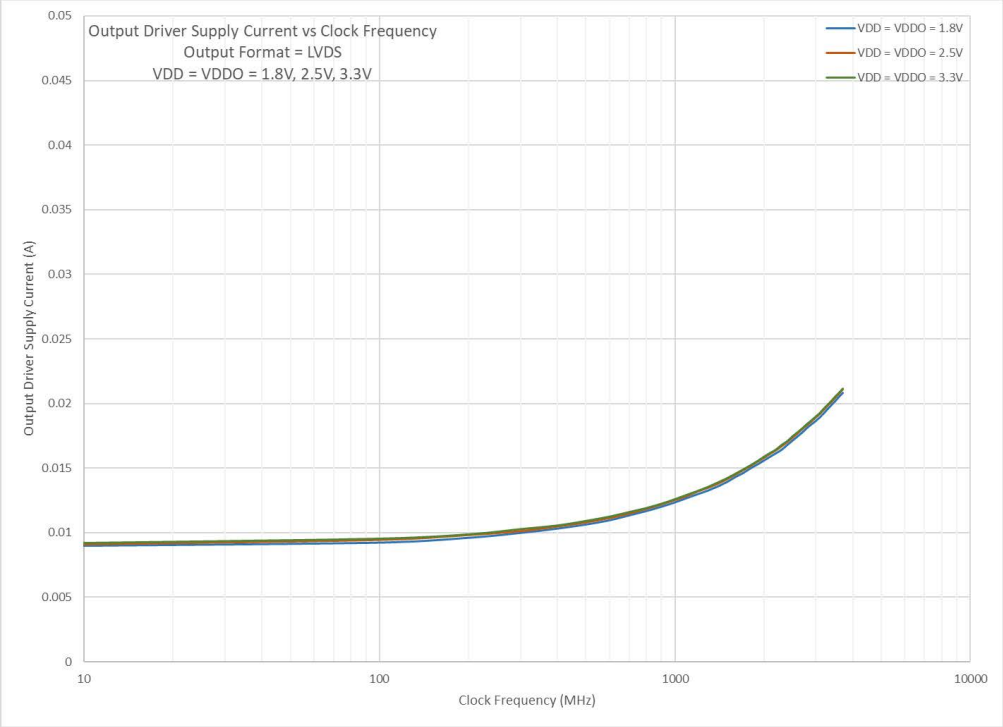


Figure 42. Supply Current Per Output vs. Frequency (LVDS)

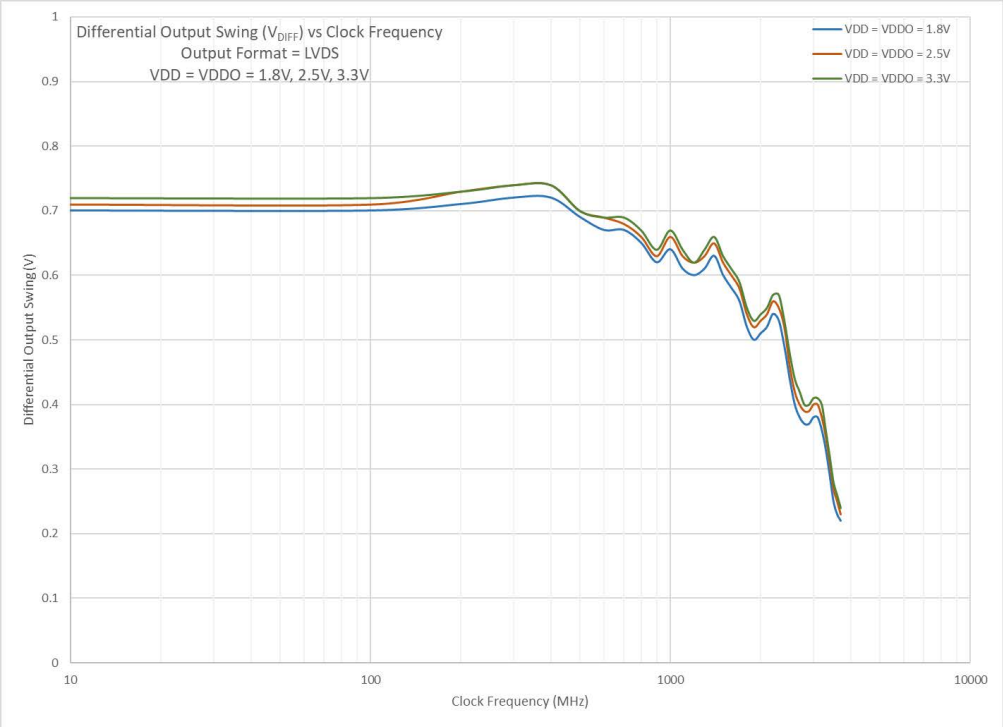


Figure 43. Differential Output Voltage Swing versus Frequency (1.8 V, 2.5 V, 3.3 V LVDS)

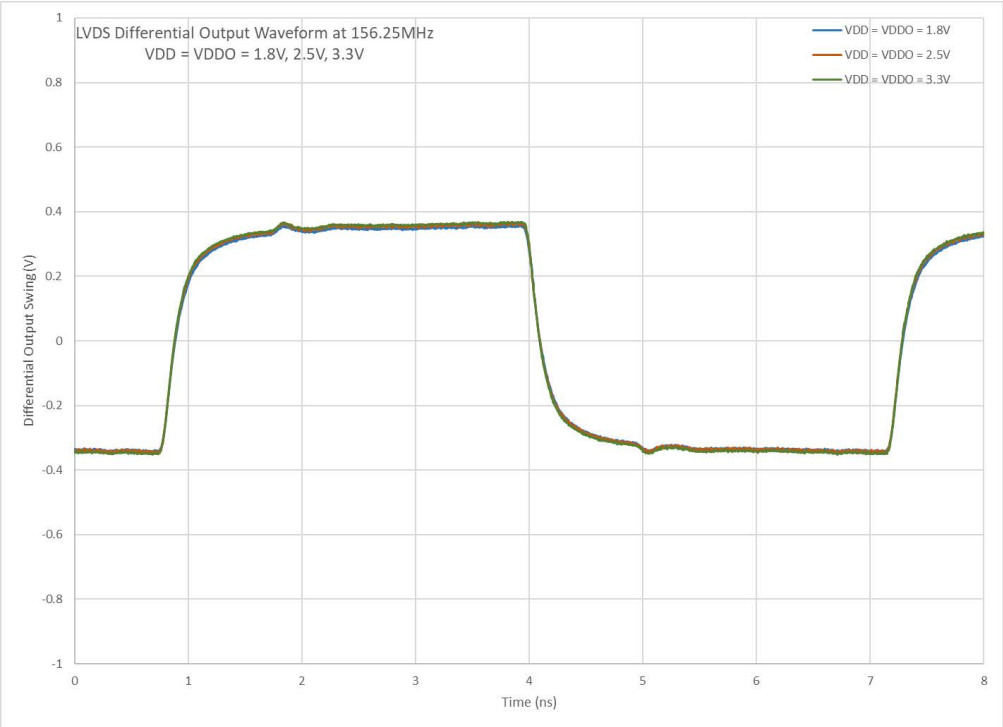


Figure 44. LVDS Differential Output Waveform (156.25 MHz)

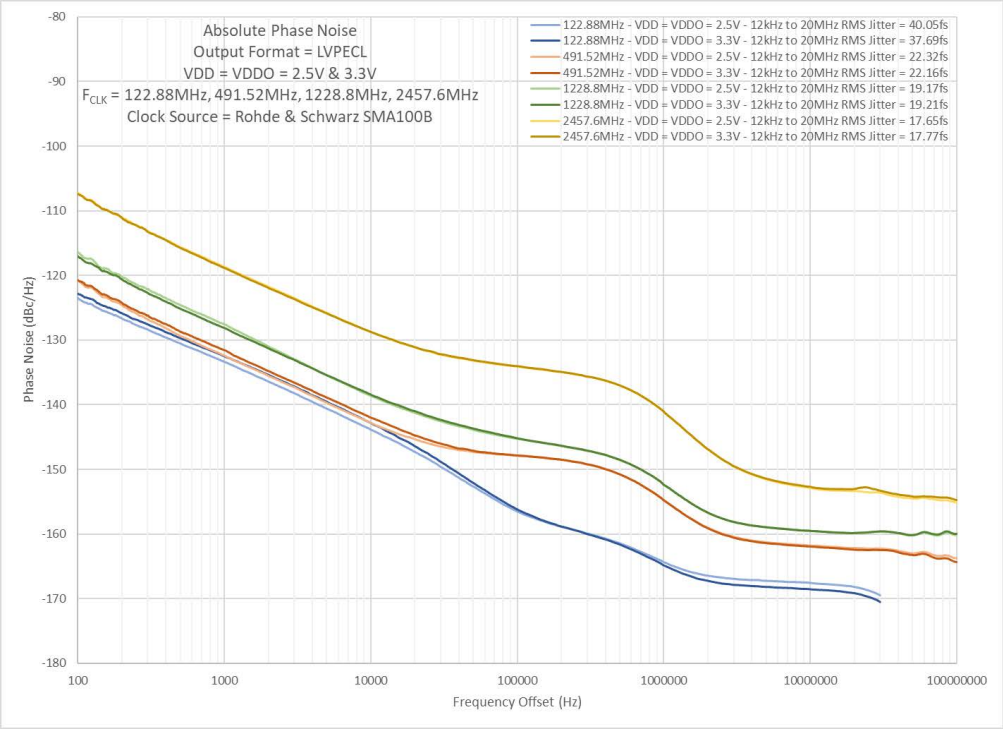


Figure 45. Absolute Phase Noise Differential Input (LVPECL: 2457.6 MHz, 1228.80 MHz, 491.52 MHz, 122.88 MHz)

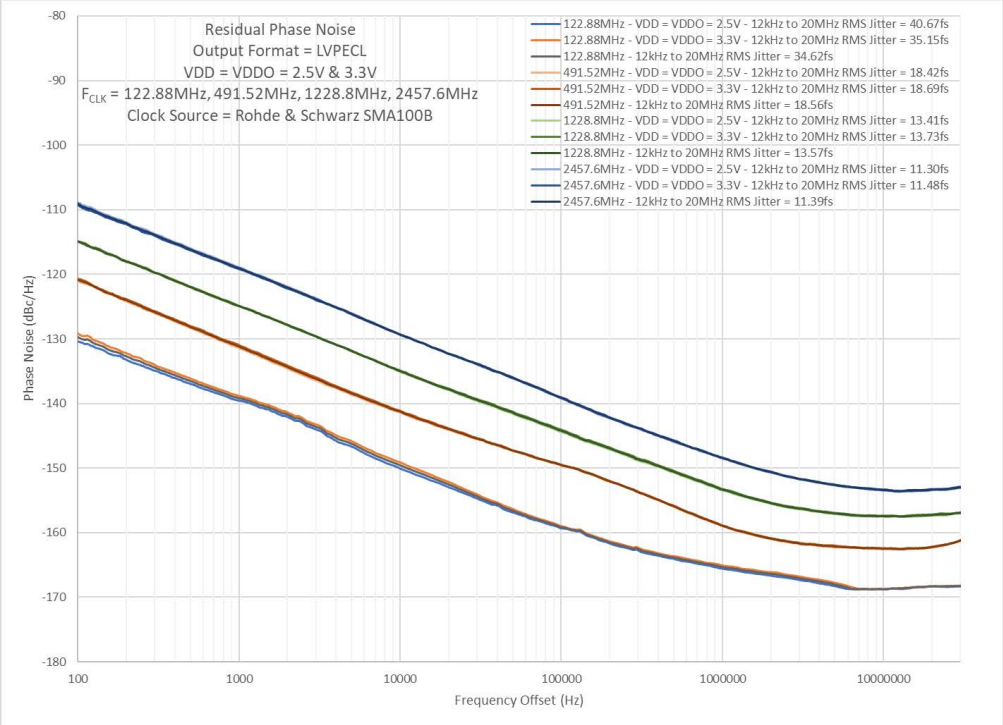


Figure 46. Residual Phase Noise Differential Input (LVPECL: 2457.6 MHz, 1228.80 MHz, 491.52 MHz, 122.88 MHz)

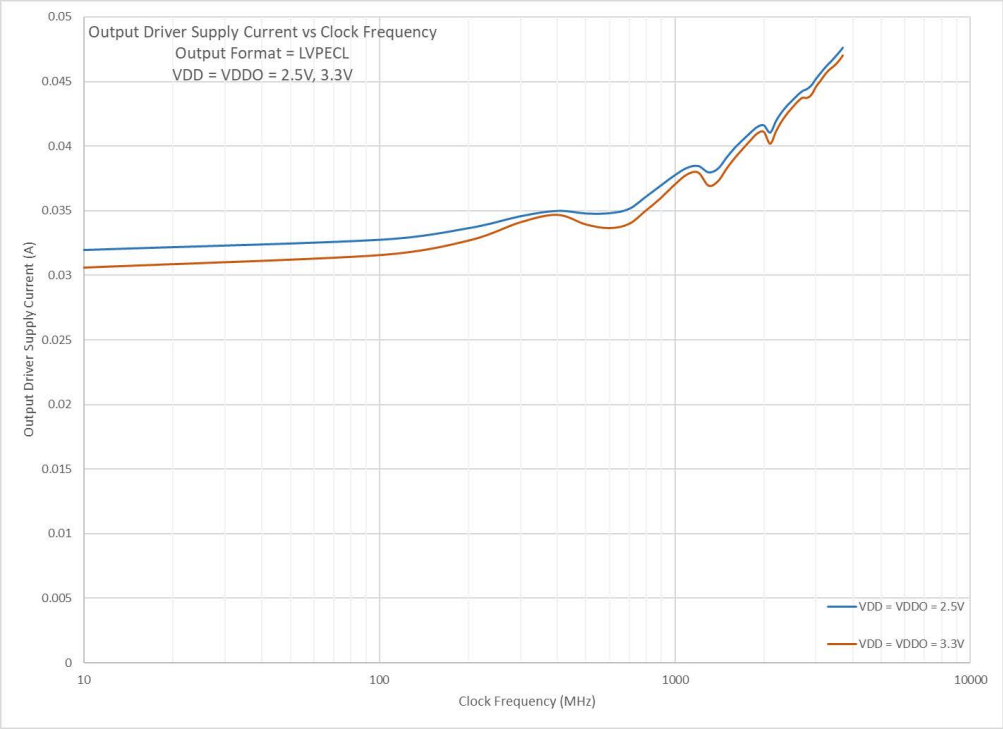


Figure 47. Supply Current Per Output versus Frequency (LVPECL)

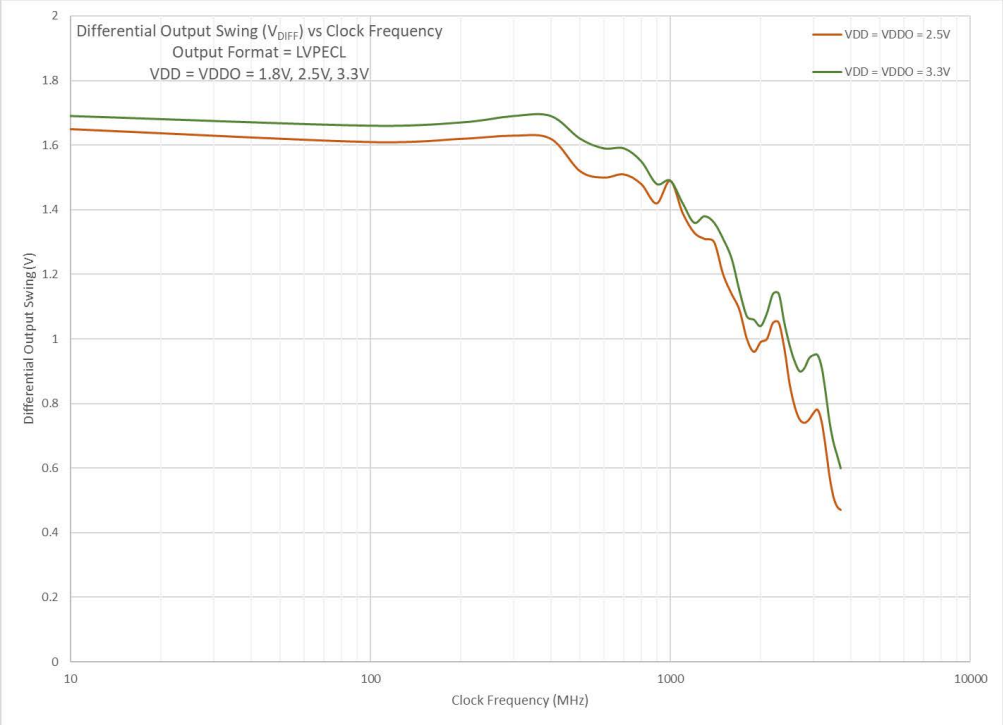


Figure 48. Differential Output Voltage Swing versus Frequency (2.5 V, 3.3 V LVPECL)

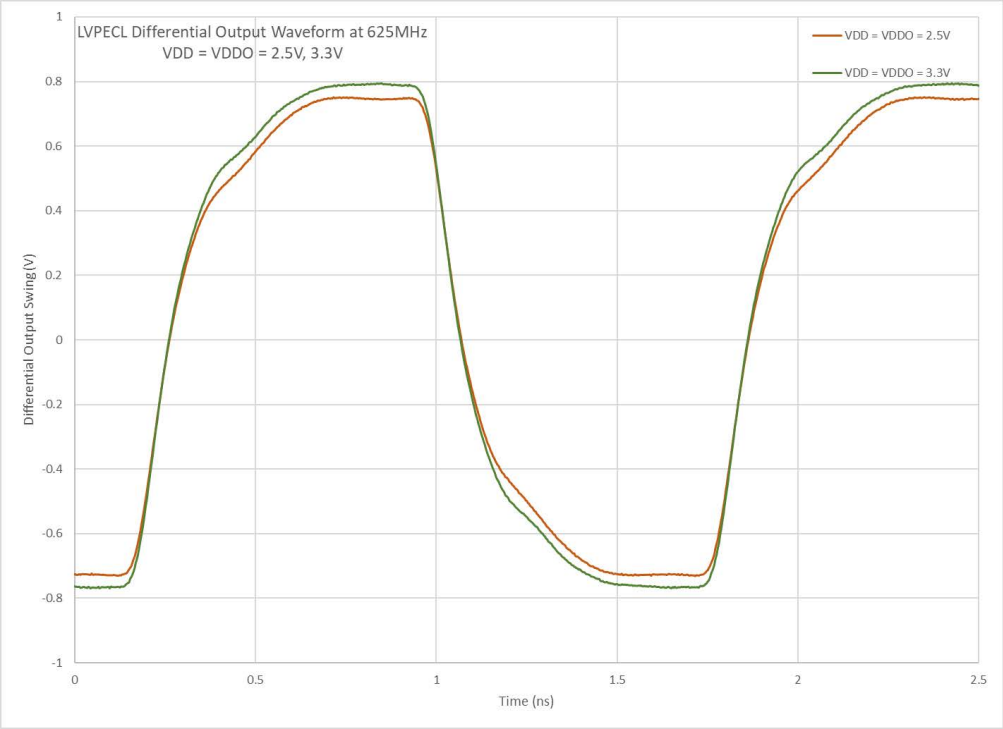


Figure 49. LVPECL Differential Output Waveform (625 MHz)

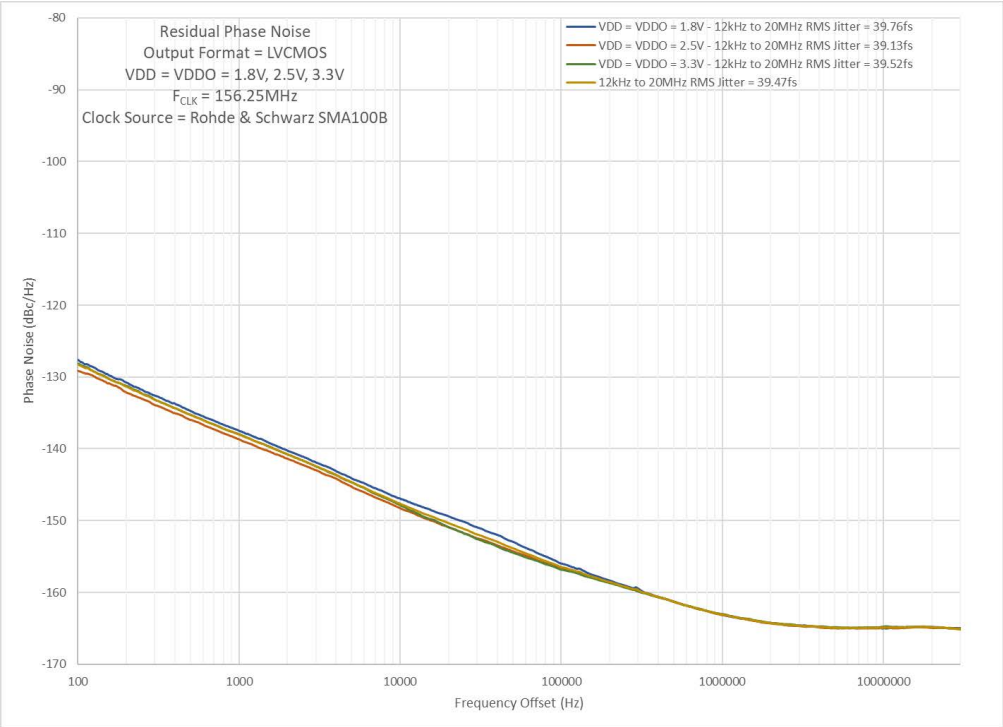


Figure 50. Residual Phase Noise Differential Input (REFOUT: 156.25 MHz)

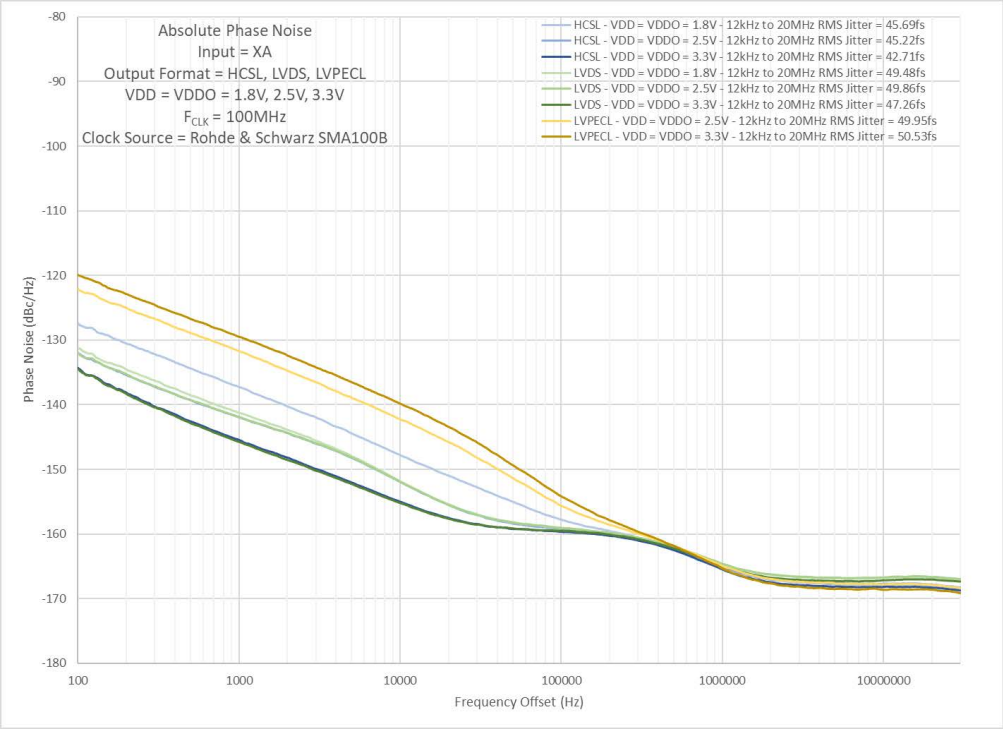


Figure 51. Absolute Phase Noise XA Clock Input (2.5 V, 3.3 V HCSL, LVDS, LVPECL: FOUT = 100 MHz)

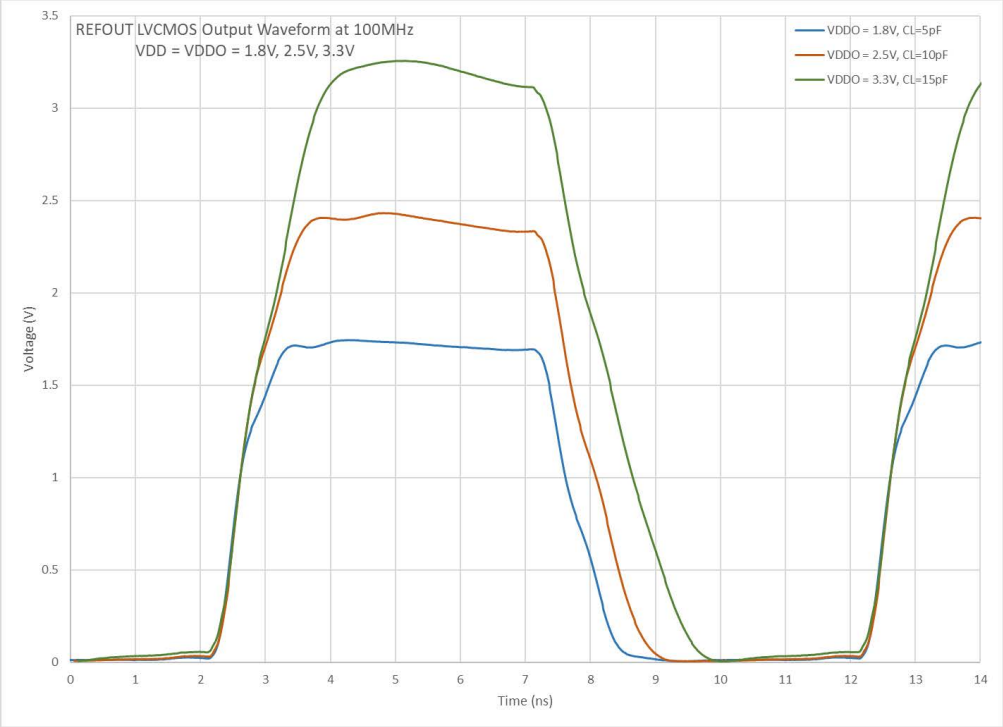


Figure 52. LVCMOS Output Waveform (100 MHz)

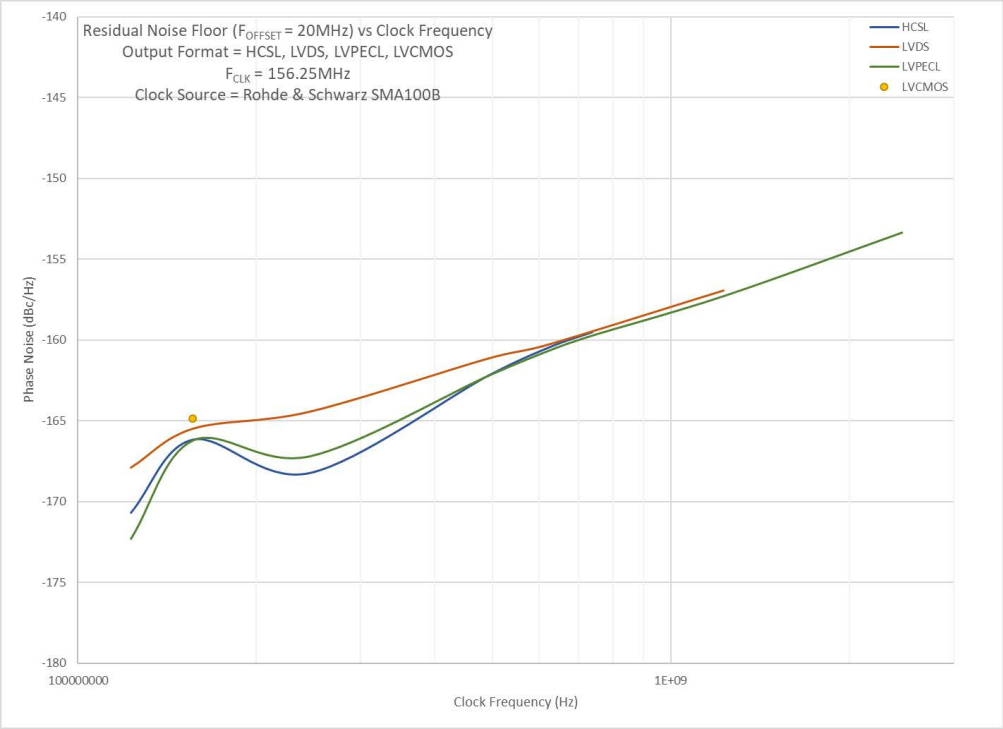


Figure 53. Residual Noise Floor (20 MHz Offset) versus Carrier Frequency (HCSL, LVDS, LVPECL, REFOUT)

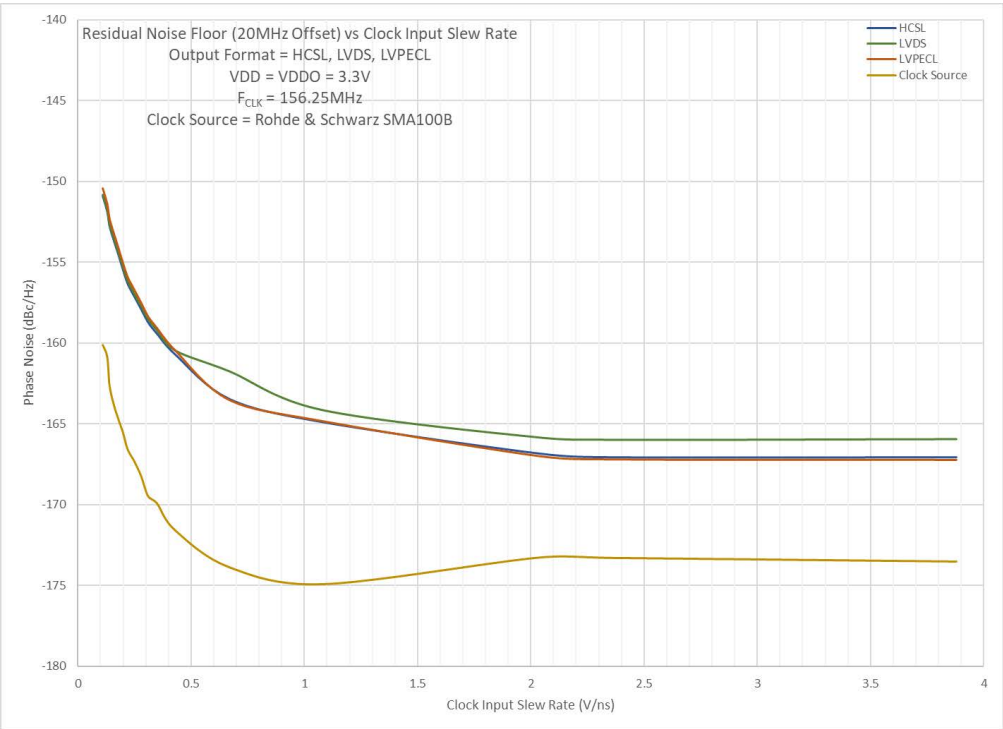


Figure 54. Residual Noise Floor (20 MHz Offset) versus Input Slew Rate (3.3 V LVPECL, LVDS, HCSL)

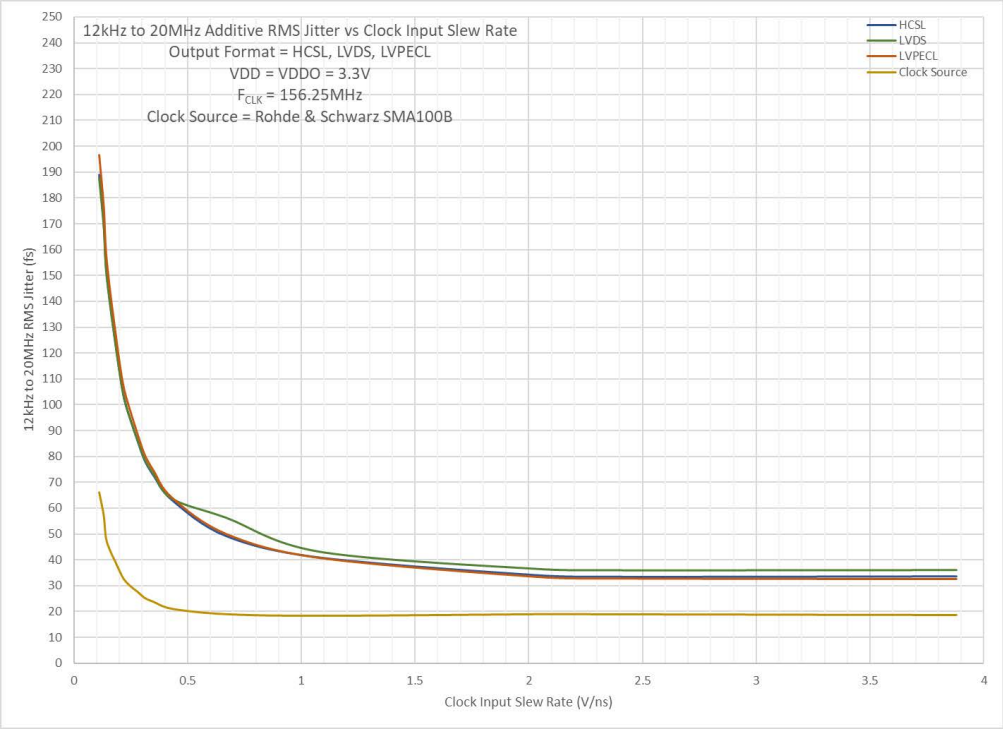


Figure 55. Additive Output Jitter versus Input Slew Rate (3.3 V LVPECL, LVDS, HCSL)

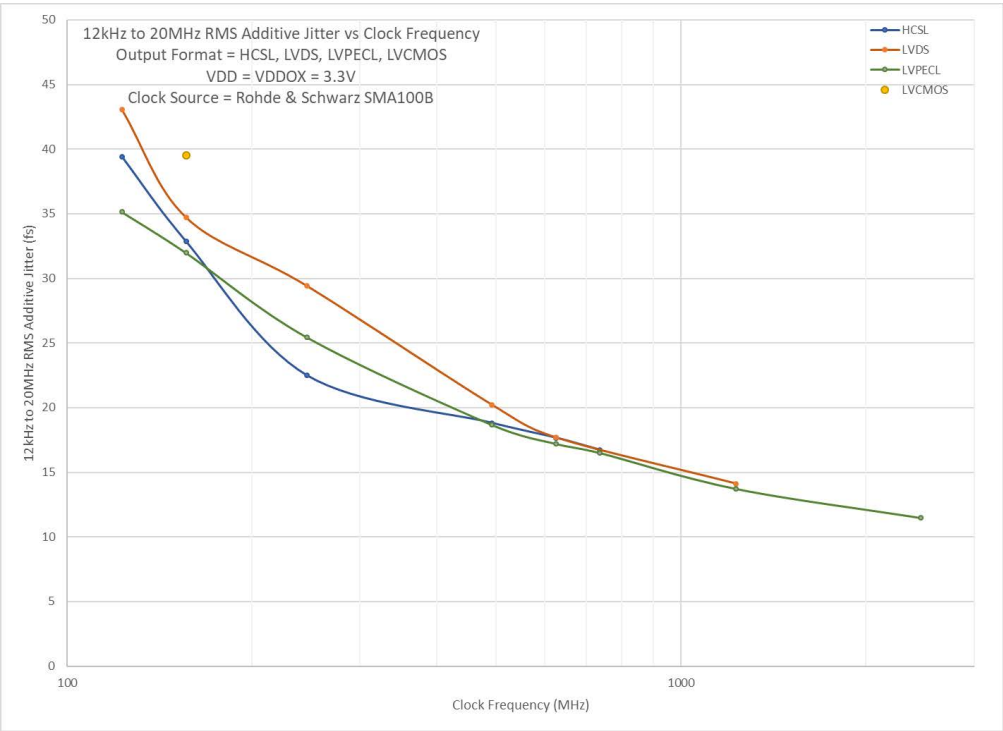


Figure 56. Additive RMS Phase Jitter versus Output Clock Frequency (3.3 V LVCMOS, LVPECL, LVDS, HCSL)

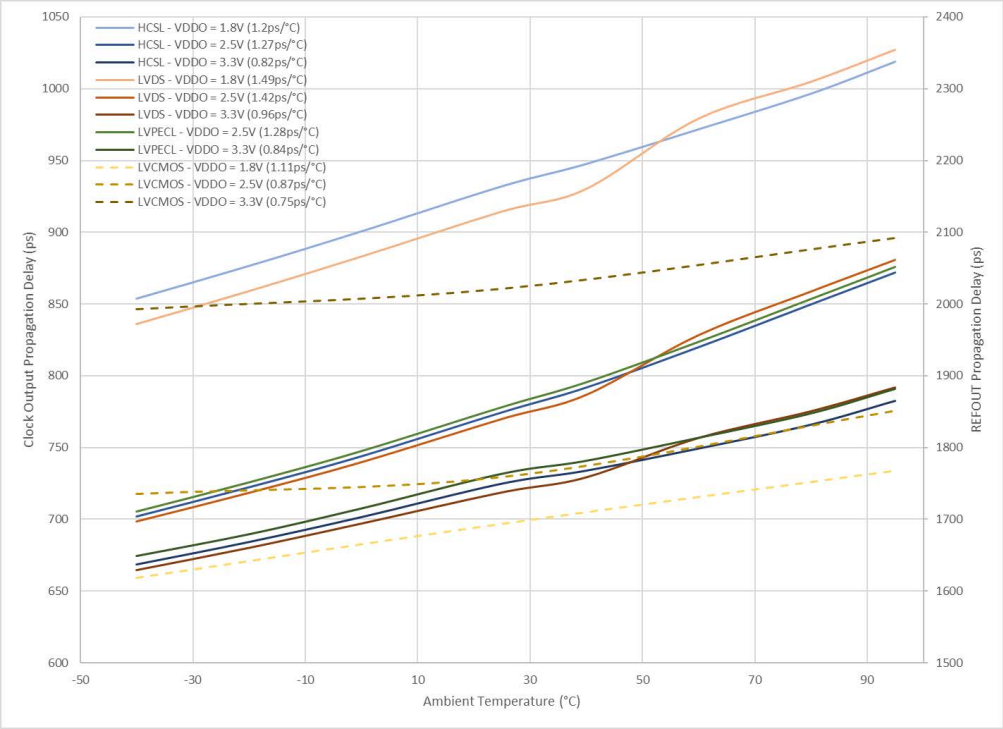


Figure 57. Propagation Delay versus Temperature (HCSL, LVCMOS, LVDS, LVPECL)

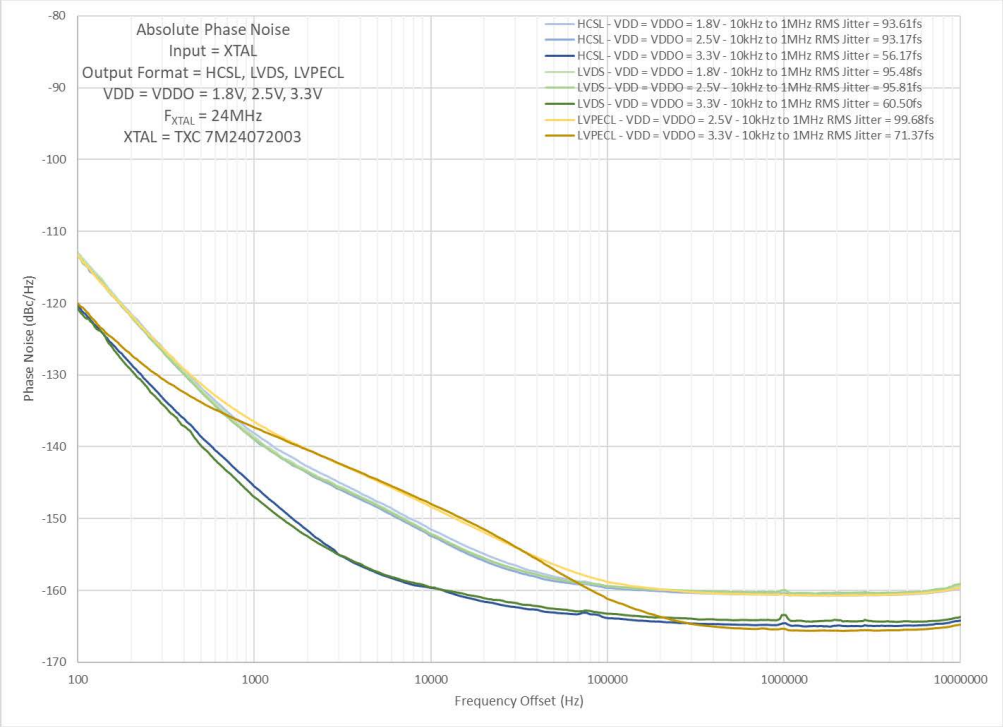


Figure 58. Absolute Crystal Phase Noise (24 MHz)

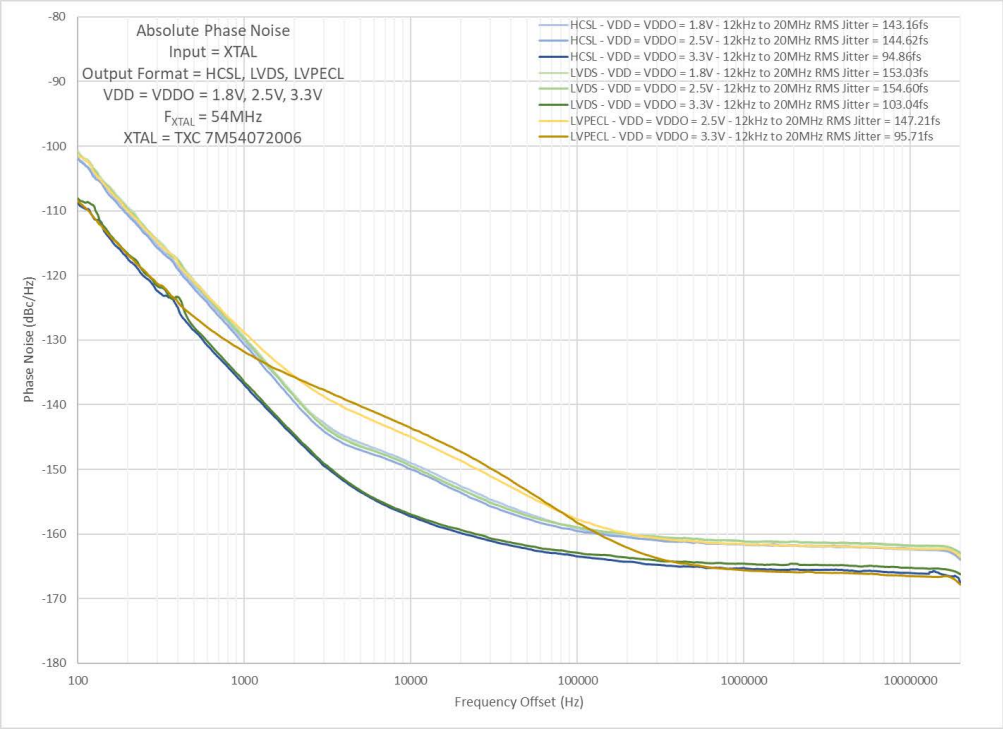


Figure 59. Absolute Crystal Phase Noise (54 MHz)

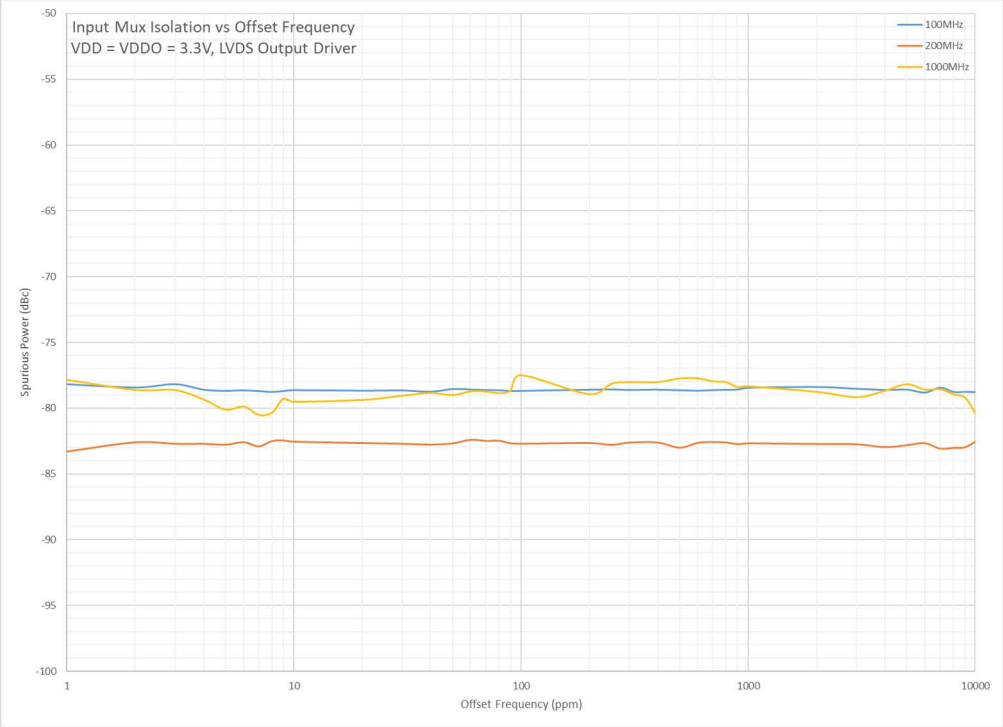


Figure 60. Input Mux Isolation vs. Offset Frequency (3.3 V LVDS)

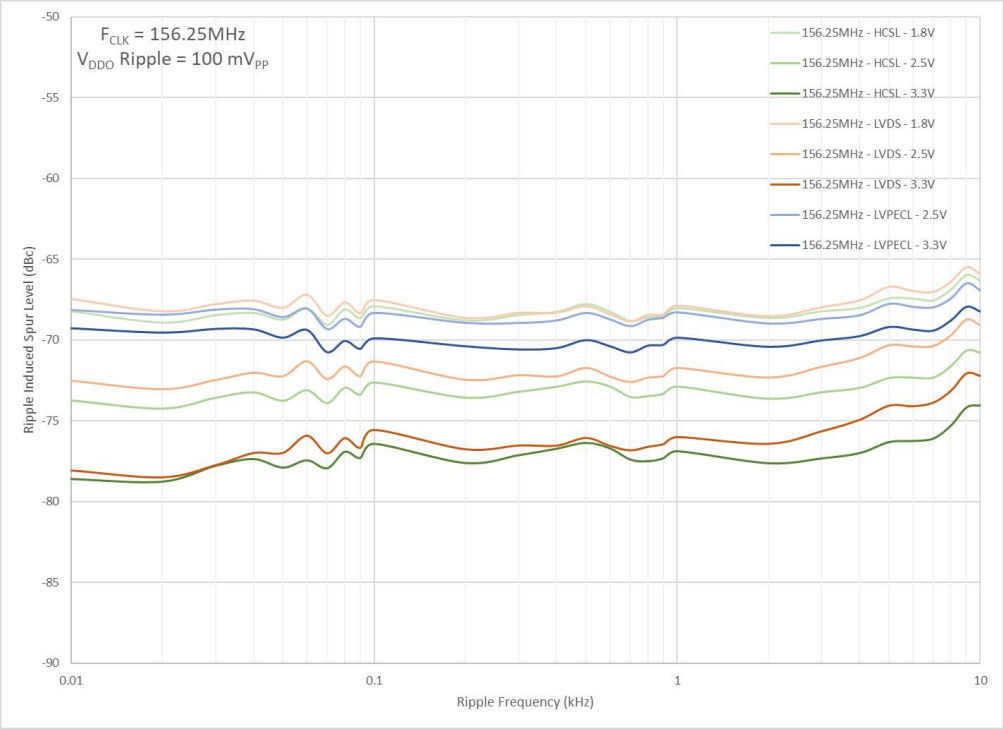


Figure 61. Power Supply Ripple Rejection vs. Offset Frequency

The phase noise and jitter plots shown above were measured using two different setups outlined below.
The setup shown in Figure 62 was used for all absolute phase noise measurements, which measures total phase noise and total jitter of the combined reference clock and clock buffer. This setup:

- Uses the differential square wave of the clock synthesizer option on the Rohde and Schwarz® SMA100B to provide an ultra low phase noise, square wave, differential reference clock to the clock buffer.
- Uses a balun to transform the differential output clock of the clock buffer to a single-ended output clock to be measured by the PNA.

The setup shown in Figure 63 was used for all residual additive phase noise and additive RMS phase jitter measurements, which measures the actual contribution of the clock buffer to the total phase noise and total jitter by removing the contribution of external noise sources (ex: power supplies and reference clock). This is commonly known as the additive RMS phase jitter of the clock buffer. This setup:

- Uses the differential square wave of the clock synthesizer options on the Rohde and Schwarz SMA100B to provide an ultra-low phase noise, square wave reference clock to the clock buffer and the FSWP.
- Uses the additive phase noise measurement option on the Rohde and Schwarz FSWP to extract the residual additive phase noise of the clock buffer and calculate the resulting additive RMS phase jitter.
- Uses baluns to transform between differential and single-ended clock signals to match the expected inputs of the clock buffer, FSWP, and LNAs.

To perform the residual additive phase noise measurements, three matching copies of the reference clock are required with one copy going to the clock buffer and the other two going to the LO Aux inputs on the FSWP.
To achieve this, the reference clock must go through a power divider and then an LNA plus attenuation stage, using matching ultra-low noise LNAs, to provide matching copies of the reference clock with amplitudes scaled to match the requirements of the clock buffer input receiver and the FSWP LO Aux inputs.

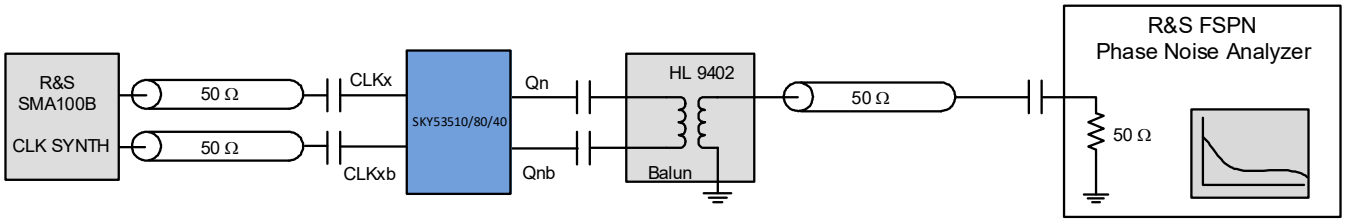


Figure 62. Measurement Setup for Absolute Phase Noise Measurements

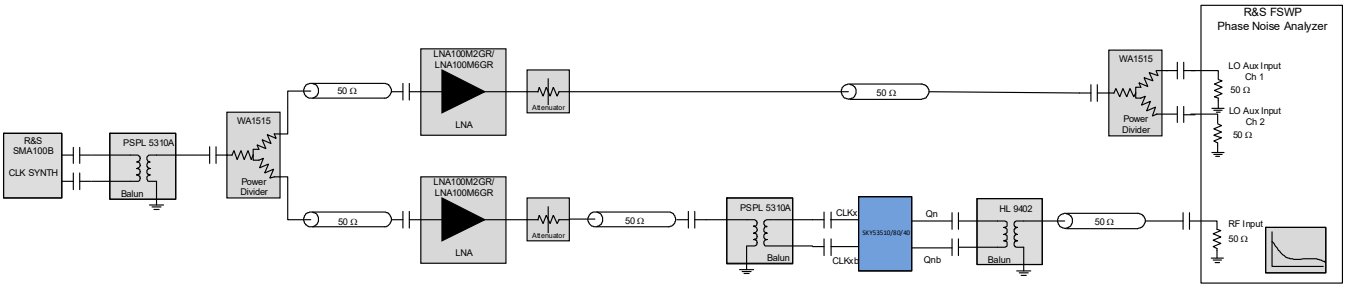


Figure 63. Measurement Setup for Residual Additive Phase Noise Measurements

7. Programming

The SKY535x2/x3 I^2C interface provides user configurability upon power-up and during operation, including input reference source selection, individual output enable/disable, and output clock format selection. Some registers include required bit writes that must be written every time the respective register is updated. These are denoted in the I^2C register map tables with a * character next to the bit number in each register table. Failure to write these required values correctly during register writes causes undesired device functionality. To avoid glitches and runt pulses on outputs during device operation, the outputs impacted by a register write should be disabled before the configuration change, and then re-enabled following the register change. Outputs are asynchronous disable and synchronous enable after the output driver power up time.

7.1. Input Clocks

CLK0/CLK0b and CLK1/CLK1b are powered on at startup, whereas the crystal oscillator is powered down to conserve power.

7.2. Input Clock Select

Input clock select for REFOUT, Bank B, and Bank A are grouped together in register 319, and default to CLK0/CLK0b at power up. The state of all three should be kept in system memory, or a full read-modify-write cycle should be performed when one or more of the input clock sources are modified.

Table 23. REFOUT Source Selection

Register 319, Bit 7	Register 319, Bit 6	REFOUT Source
0	0	CLK0/CLK0b
0	1	CLK1/CLK1b
1	0	XTAL OSC / XA single-ended
1	1	XTAL OSC / XA single-ended

Table 24. BANK B Source Selection

Register 319, Bit 4	Register 319, Bit 3	Bank B Source
0	0	CLK0/CLK0b
0	1	CLK1/CLK1b
1	0	XTAL OSC / XA single-ended
1	1	XTAL OSC / XA single-ended

Table 25. BANK A Source Selection

Register 319, Bit 1	Register 319, Bit 0	Bank A Source
0	0	CLK0/CLK0b
0	1	CLK1/CLK1b
1	0	XTAL OSC / XA single-ended
1	1	XTAL OSC / XA single-ended

7.3. Output Format Select

The SKY53512/82/42 and SKY53513/83/43 each provide four output signal format options to choose from for each bank of outputs. The signal format for both banks defaults to format 00 at power up.

Table 26. Output Format Selection

Bank A		Bank B			
Register 315		Register 316			
Bit 7	Bit 6	Bit 7	Bit 6	SKY53512/82/42	SKY53513/83/43
0	0	0	0	HCSL, 600 mV swing	800 mV LVDS
0	1	0	1	HCSL, 700 mV swing	LVDS
1	0	1	0	HCSL, 800 mV swing	LVPECL
1	1	1	1	HCSL, 1200 mV swing	Complementary LVCMOS

7.4. Output Enable and Disable

All outputs from Bank A and Bank B are disabled by default at power up.

At power up, REFOUT is both powered down and disabled. To avoid output clock glitches during power up, the sequence to enable REFOUT is Powerdown > Disabled > Wait for powerup > Enabled. After this powerup sequence, REFOUT can switch between Enabled or Disabled at any time. When powering down REFOUT, place the output in the Disabled State and wait three clock cycles before powering down REFOUT.

7.5. Reset

Reset is a self-clearing bit. Setting this bit to 1 resets the device back to the power-on state. Refer to “Power Supply Sequencing” on page 24.

7.6. Register Map

Table 27. I²C Register Map[1]

Byte	Register	Name	Bit	Type	Default	Description	Definition
3	Reset	Reserved	7:3	RW	0	Reserved	
		Reserved	2:1*	RW	0	Reserved	These bits must be written as 0
		Reset	0	RW	0	Resets the device	0 = Normal operation 1 = Power on reset
315	Format_A	Format_A1	7	RW	0	Output format selection for Bank A	Sets output signal format for Bank A outputs
		Format_A0	6	RW	0	Output format selection for Bank A	
		Reserved	5	RW	0	Reserved	
		Reserved	4*	RW	1	Reserved	When writing to this register, bit4 must be written to as 1
		Reserved	3:0	RW	0	Reserved	
316	Format_B	Format_B1	7	RW	0	Output format selection for Bank B	Sets output signal format for Bank B outputs
		Format_B0	6	RW	0	Output format selection for Bank B	
		Reserved	5	RW	0	Reserved	
		Reserved	4*	RW	1	Reserved	When writing to this register, bit 4 must be written to as 1
		Reserved	3:0	RW	0	Reserved	
318	REFOUT	Reserved	7*	RW	1	Reserved	When writing to this register, bit 7 must be written to as 1
		Reserved	6*	RW	1	Reserved	When writing to this register, bit 6 must be written to as 1
		Reserved	5*	RW	1	Reserved	When writing to this register, bit 5 must be written to as 1
		Reserved	4:3	RW	0	Reserved	
		Reserved	2*	RW	1	Reserved	When writing to this register, bit 2 must be written to as 1
		OE_REFOUT	1	RW	0	Output enable for REFOUT	0 = REFOUT disabled 1 = REFOUT enabled
		REFOUT_PWR	0	RW	0	Powerup/down REFOUT	0 = REFOUT powered down 1 = REFOUT powered up To avoid glitches: When enabling REFOUT, write REFOUT_PWR=1 at least 10ms before writing OE_REFOUT=1. When disabling REFOUT, write OE_REFOUT = 0 and wait at least three clock cycles if writing REFOUT_PWR=0.

Table 27. I²C Register Map[1] (Continued)

Byte	Register	Name	Bit	Type	Default	Description	Definition
319	IN_SEL	INSEL_REFOUT1	7	RW	0	Input reference source select for REFOUT	Selects input clock source for REFOUT
		INSEL_REFOUT0	6	RW	0	Input reference source select for REFOUT	
		Reserved	5	RW	0	Reserved	
		INSEL_BANKB1	4	RW	0	Input reference source select for Bank B	Selects input clock source for Bank B outputs
		INSEL_BANKB0	3	RW	0	Input reference source select for Bank B	
		Reserved	2	RW	0	Reserved	
		INSEL_BANKA1	1	RW	0	Input reference source select for Bank A	Selects input clock source for Bank A outputs
		INSEL_BANKA0	0	RW	0	Input reference source select for Bank A	
321	OE_0	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_0	0	RW	0	Output enable for: SKY53512/13: Q0/Q0b SKY53582/83: Q0/Q0b	0 = Output disabled 1 = Output enabled
325	OE_1	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_1	0	RW	0	Output enable for: SKY53512/13: Q1/Q1b SKY53582/83: Q1/Q1b SKY53542/43: Q0/Q0b	0 = Output disabled 1 = Output enabled
329	OE_2	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_2	0	RW	0	Output enable for: SKY53512/13: Q2/Q2b SKY53582/83: Q2/Q2b SKY53542/43: Q1/Q1b	0 = Output disabled 1 = Output enabled

Table 27. I²C Register Map[1] (Continued)

Byte	Register	Name	Bit	Type	Default	Description	Definition
333	OE_3	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_3	0	RW	0	Output enable for: SKY53512/13: Q3/Q3b SKY53582/83: Q3/Q3b	0 = Output disabled 1 = Output enabled
337	OE_4	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_4	0	RW	0	Output enable for: SKY53512/13: Q4/Q4b	0 = Output disabled 1 = Output enabled
341	OE_5	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_5	0	RW	0	Output enable for: SKY53512/13: Q5/Q5b SKY53582/83: Q4/Q4b	0 = Output disabled 1 = Output enabled
345	OE_6	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_6	0	RW	0	Output enable for: SKY53512/13: Q6/Q6b SKY53582/83: Q5/Q5b SKY53542/43: Q2/Q2b	0 = Output disabled 1 = Output enabled
349	OE_7	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_7	0	RW	0	Output enable for: SKY53512/13: Q7/Q7b SKY53582/83: Q6/Q6b SKY53542/43: Q3/Q3b	0 = Output disabled 1 = Output enabled

Table 27. I²C Register Map[1] (Continued)

Byte	Register	Name	Bit	Type	Default	Description	Definition
353	OE_8	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_8	0	RW	0	Output enable for: SKY53512/13: Q8/Q8b SKY53582/83: Q7/Q7b	0 = Output disabled 1 = Output enabled
357	OE_9	Reserved	7:6	RW	0	Reserved	
		Reserved	5*	RW	0	Reserved	When writing to this register, bit 5 must be written to as 0
		Reserved	4:2	RW	0	Reserved	
		Reserved	1*	RW	1	Reserved	When writing to this register, bit 1 must be written to as 1
		OE_9	0	RW	0	Output enable for: SKY53512/13: Q9/Q9b	0 = Output disabled 1 = Output enabled

1. Register bits noted with an "*" require bit writes each time the respective register is updated.

7.7. I²C Device Addresses

Table 28. I²C Device Addresses

Part Number	Decimal	Hex
SKY53512	42	2A
SKY53582	40	28
SKY53542	36	24
SKY53513	58	3A
SKY53583	56	38
SKY53543	52	34

8. Package and Handling Information

8.1. Typical Part Marking

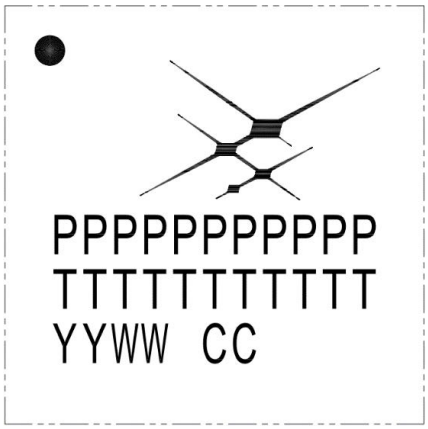


Figure 64. Typical Part Marking

Table 29. Typical Part Marking Explanation

Mark Method	Laser	
Pin 1 Mark	Circle: 0.50 mm diameter	Top-left justified
Skyworks Logo	Logo height: ~2.33	Rightmost edge of Skyworks logo, left-justified with last character of Line 1 text.
Font Size	2.0 point (26 mils)	Left-justified
Line 1 Format	PPPPPPPPPP = Device part number	53512 for SKY53512-A-GM 53582 for SKY53582-A-GM 53542 for SKY53542-A-GM 53513 for SKY53513-A-GM 53583 for SKY53583-A-GM 53543 for SKY53543-A-GM
Line 2 Format	TTTTTTTTTT = Mfg code	Manufacturing code assembly lot number.
Line 3 Format	YY = Calendar year WW = Work week CC = Country code	

8.2. SKY53512/13, 7 x 7 mm, 48-QFN Package Diagram

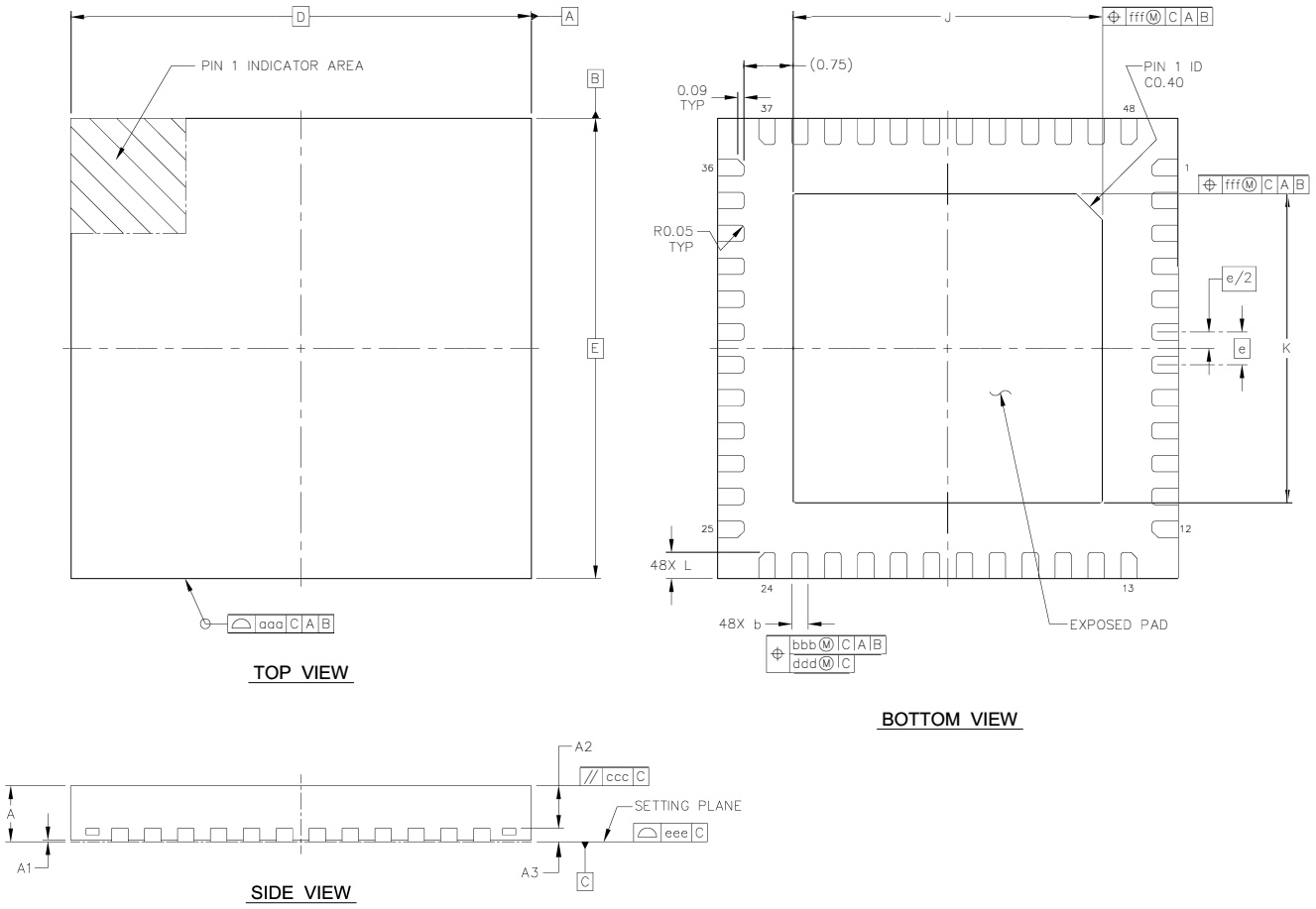


Figure 65. 7 x 7 mm 48-QFN Package

Table 30. 7 x 7 mm 48-QFN Package Dimensions[1,2,3,4,5]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	

Table 30. 7 x 7 mm 48-QFN Package Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Nom	Max
J	4.65	4.70	4.75
K	4.65	4.70	4.75
L	0.35	0.40	0.45
aaa		0.15	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.08	
fff		0.05	

1. Dimensions are in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M.
3. Package dimensions exclusive of burrs and mold flash.
4. Plating requirements per source control drawings: SQ03-0462.
5. Coplanarity applies to terminals and all bottom surface metalization.

8.3. SKY53582/83, 6 x 6 mm, 40-QFN Package Diagram

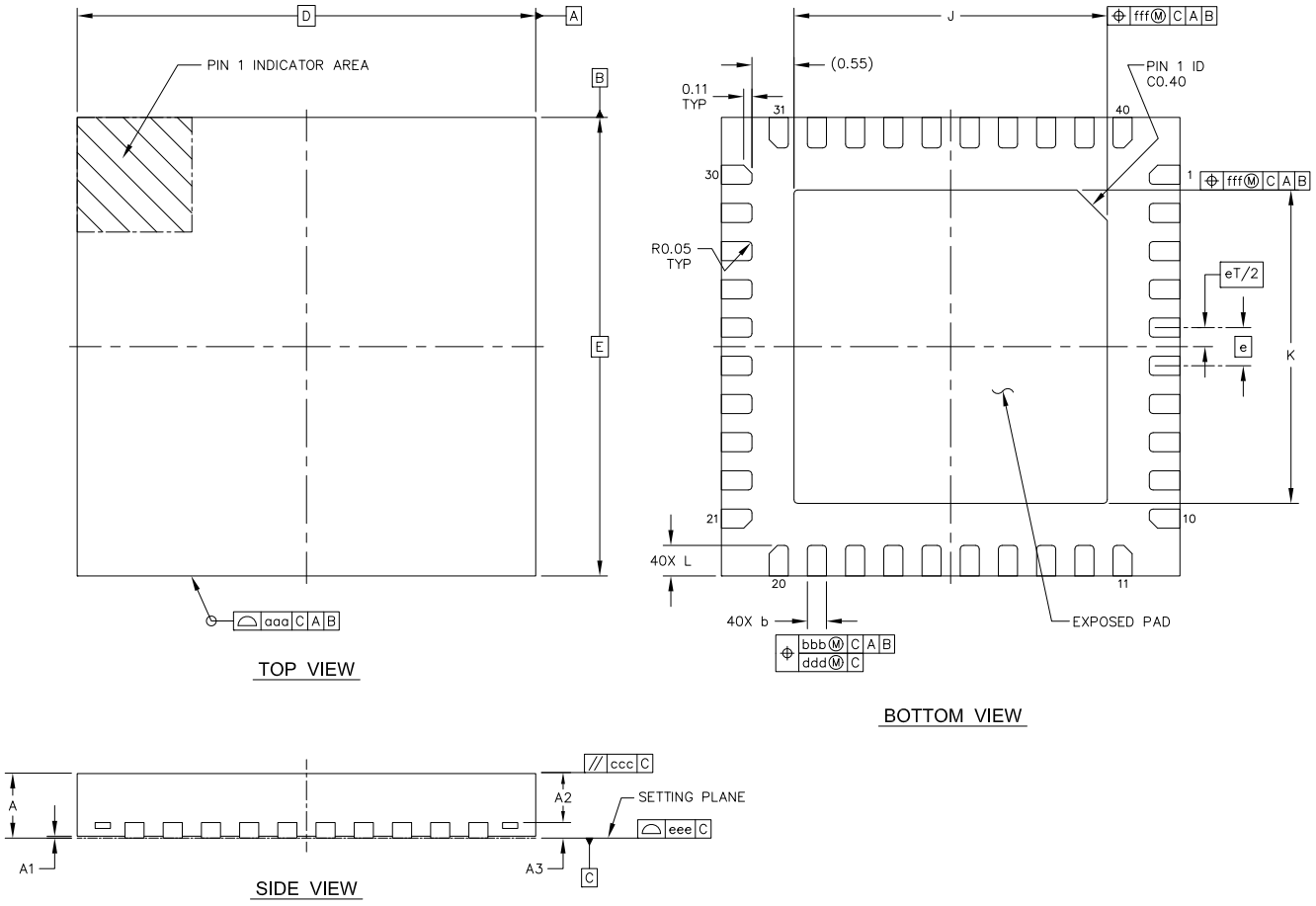


Figure 66. 6 x 6 mm 40-QFN Package

Table 31. 6 x 6 mm 40-QFN Package Dimensions[1,2,3,4,5]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.20	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	

Table 31. 6 x 6 mm 40-QFN Package Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Nom	Max
J	4.05	4.10	4.15
K	4.05	4.10	4.15
L	0.35	0.40	0.45
aaa		0.15	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.08	
fff		0.05	

1. Dimensions are in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M.
3. Package dimensions exclusive of saw burr.
4. Plating requirements per source control drawings: SQ03-0462.
5. Coplanarity applies to leads, corner leads, and exposed die attach pad.

8.4. SKY53542/43, 5 x 5 mm, 32-QFN Package Diagram

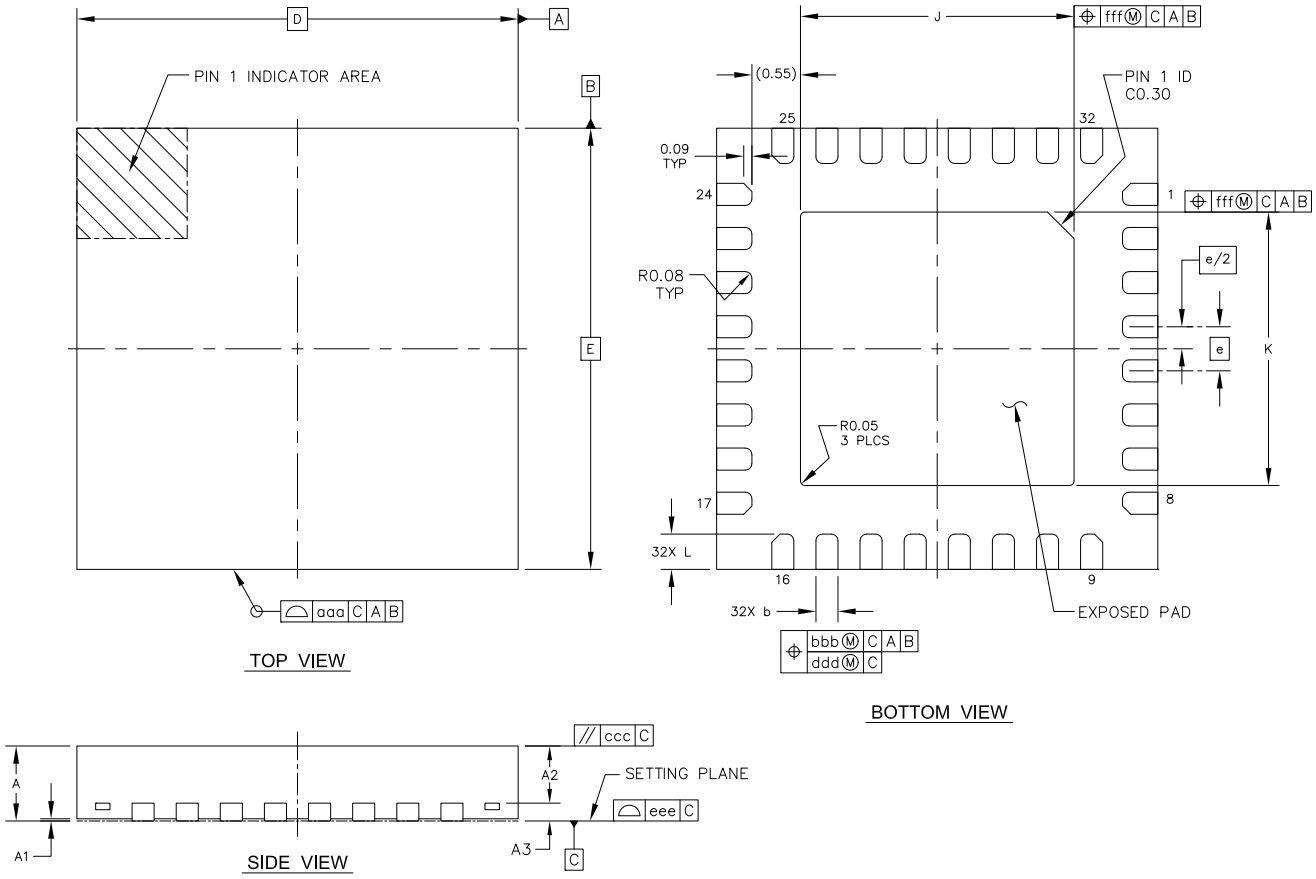


Figure 67. 5 x 5 mm 32-QFN Package

Table 32. 5 x 5 mm 32-QFN Package Dimensions[1,2,3,4,5]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	—	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	

Table 32. 5 x 5 mm 32-QFN Package Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Nom	Max
J	3.05	3.10	3.15
K	3.05	3.10	3.15
L	0.35	0.40	0.45
aaa		0.05	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.08	
fff		0.05	

1. Dimensions are in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M.
3. Package dimensions exclusive of saw burr.
4. Plating requirements per source control drawings: SQ03-0462.
5. Coplanarity applies to leads, corner leads, and exposed die attach pad.

9. Land Patterns

9.1. SKY53512/13, 7 x 7 mm, 48-QFN Land Pattern

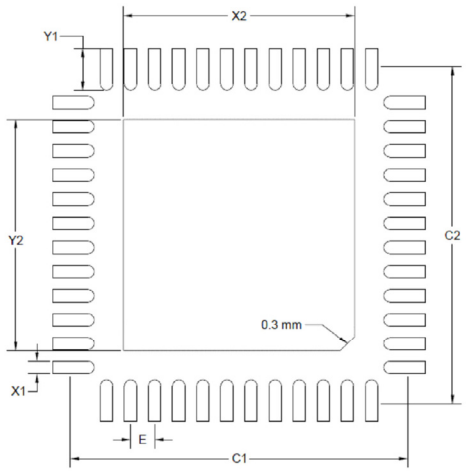


Figure 68. 7 x 7 mm 48-QFN Land Pattern

Table 33. 7 x 7 mm 48-QFN Land Pattern Dimensions

Dimension	mm	Notes
C1	7.00	**General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 2×2 array of 1.35 mm square openings on 1.55 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
C2	7.00	
E	0.50	
X1	0.26	
Y1	0.80	
X2	4.80	
Y2	4.80	

9.2. SKY53582/83, 6 x 6 mm, 40-QFN Land Pattern

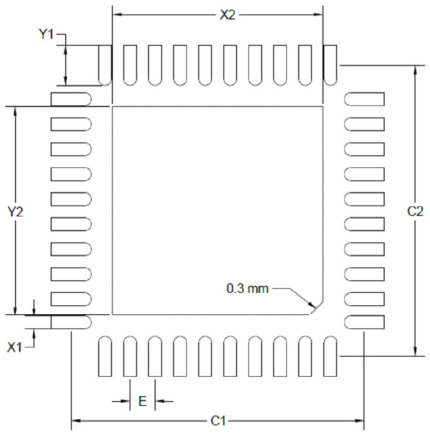


Figure 69. 6 x 6 mm 40-QFN Land Pattern

Table 34. 6 x 6 mm 40-QFN Land Pattern Dimensions

Dimension	mm	Notes
C1	6.00	**General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This land pattern design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 2×2 array of 1.35 mm square openings on 1.55 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	6.00	
E	0.50	
X1	0.26	
Y1	0.80	
X2	4.20	
Y2	4.20	

9.3. SKY53542/43, 5 x 5 mm, 32-QFN Land Pattern

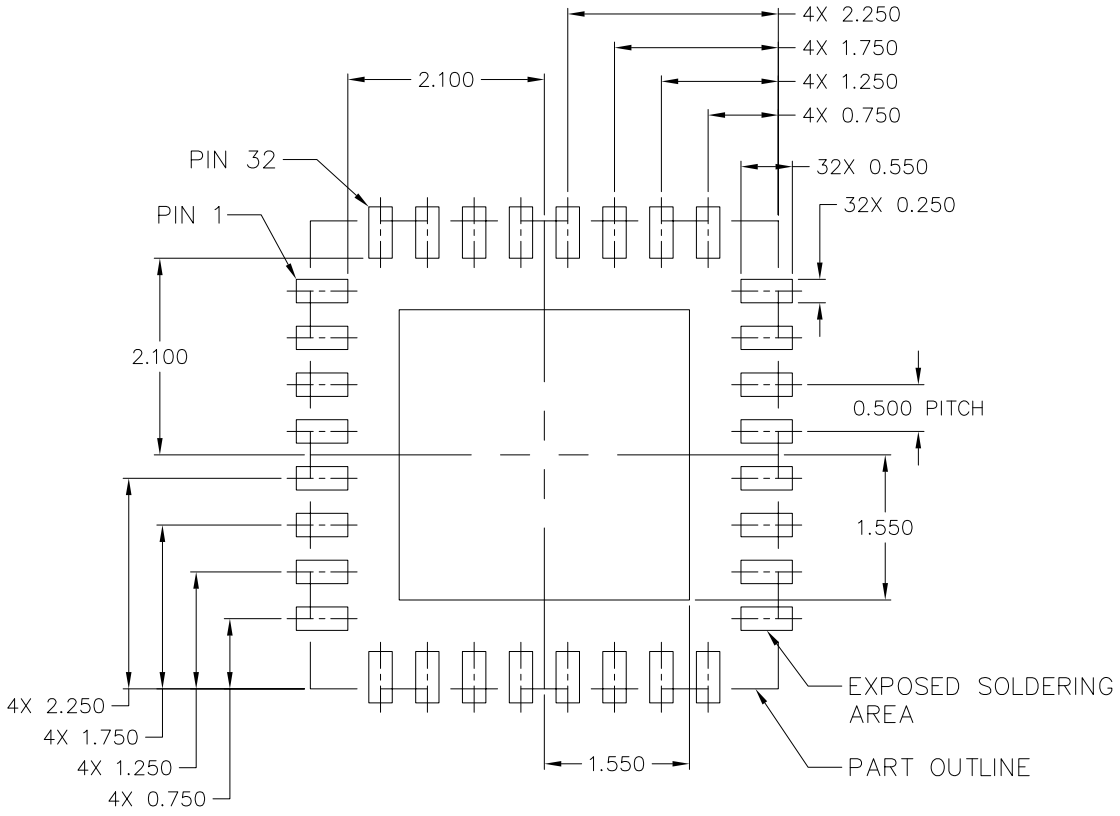


Figure 70. 5 x 5 mm 32-QFN Land Pattern

10. Ordering Guide

Table 35. Product Family Overview

Part Number	Inputs	Outputs	Description
SKY53512-A-GM	2 plus crystal	10 Diff + REFOUT	10-output universal input, HCSL output buffer with 3:1 input mux and I^2C control.
SKY53582-A-GM	2 plus crystal	8 Diff + REFOUT	8-output universal input, HCSL output buffer with 3:1 input mux and I^2C control.
SKY53542-A-GM	2 plus crystal	4 Diff + REFOUT	4-output universal input, HCSL output buffer with 3:1 input mux and I^2C control.
SKY53513-A-GM	2 plus crystal	10 Diff + REFOUT	10-output universal buffer with 3:1 input mux and I^2C control.
SKY53583-A-GM	2 plus crystal	8 Diff + REFOUT	8-output universal buffer with 3:1 input mux and I^2C control.
SKY53543-A-GM	2 plus crystal	4 Diff + REFOUT	4-output universal buffer with 3:1 input mux and I^2C control.

Table 36. SKY535xx Ordering Guide

Part Number	Package	Pb-Free, ROHS-6	Ambient Temperature Range
SKY53512-A-GM SKY53513-A-GM[1]	7 x 7 mm 48-QFN	Yes	–40 to 95 °C
SKY53582-A-GM SKY53583-A-GM[1]	6 x 6 mm 40-QFN	Yes	–40 to 95 °C
SKY53542-A-GM SKY53543-A-GM[1]	5 x 5 mm 32-QFN	Yes	–40 to 95 °C
SKY53512-A-EVB SKY53513-A-EVB	Evaluation board for SKY535x2 Evaluation board for SKY535x3	—	—

1. Add an “R” at the end of the part number to denote tape and reel ordering option.

11. Revision History

Revision	Date	Description
A	January, 2026	Initial release.