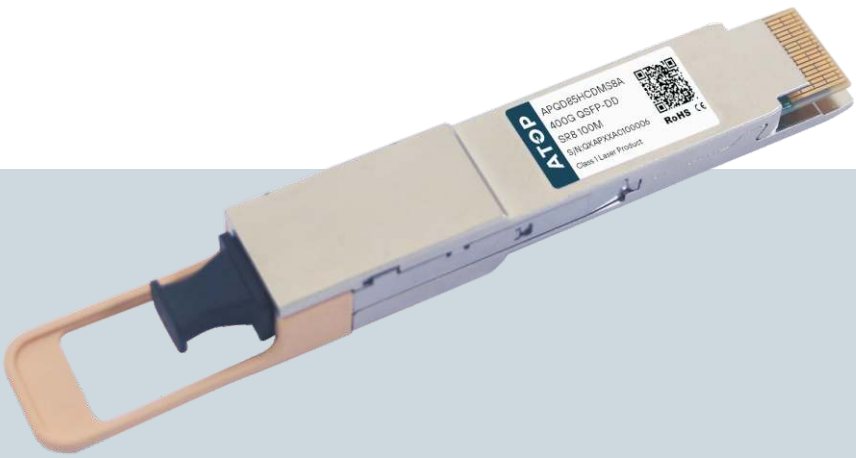
400Gb/s QSFP-DD SR8 Transceiver

APQD85HCDMS8A



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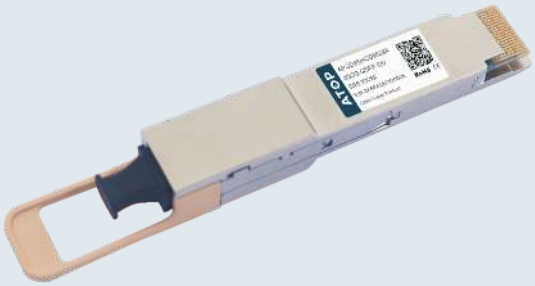
Product Features

- ✓ Compliance to 200GBASE-SR4 of IEEE 802.3 cd Rev. 3.2
- ✓ Compliance to QSFP DD MSA Rev 3.0 (for Memory Map) and 4.0 (for Mechanical QSFP-DD Housing)
- ✓ Supports 400 Gbps data rate links up to 70m/100 m via OM3/OM4, respectively
- ✓ Typical Power Consumption: 10W (each port)
- ✓ Hot pluggable electrical interface
- ✓ Using standard 2 Row by 12 Channel MPO Connector
- ✓ 0 to 70°C case temperature operating range
- ✓ RoHS-6 Compliant (lead-free)



Applications

- ✓ Ethernet for 200GBASE-SR4
- ✓ For 400 Gb/s Ethernet Application
- ✓ HPC Interconnects
- ✓ Proprietary Interconnections

Product Selection

Part Number	Operating Case temperature	DDMI
APQD85HCDMS8A	Commercial(0~70℃)	Yes

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with EN 61000-4-3
- EMI compatible with FCC Part 15 Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 IEC 60950, IEC60825-1,2

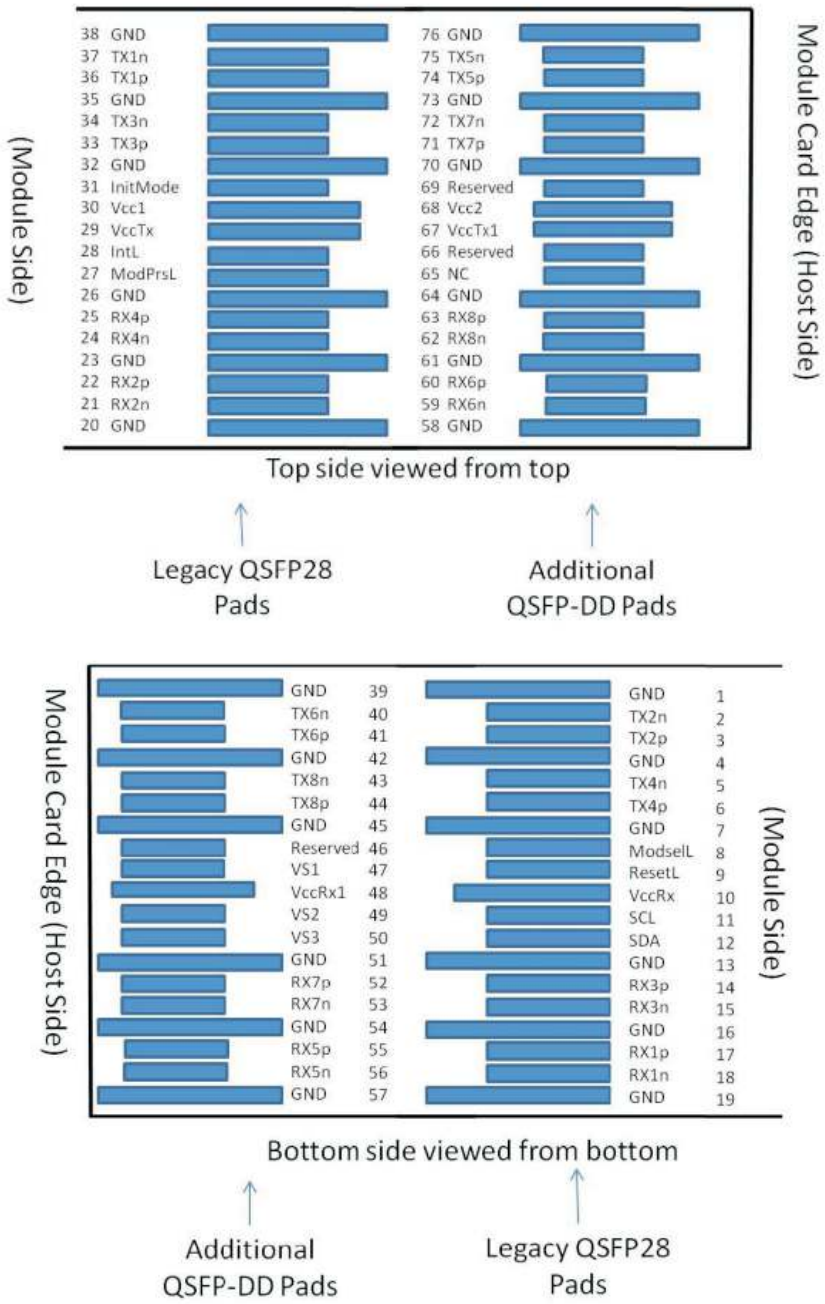
Pin Descriptions

Pin	Logic	Symbol	Description	Plug	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	Init-Mode	Initialization mode, In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3n	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3p	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1

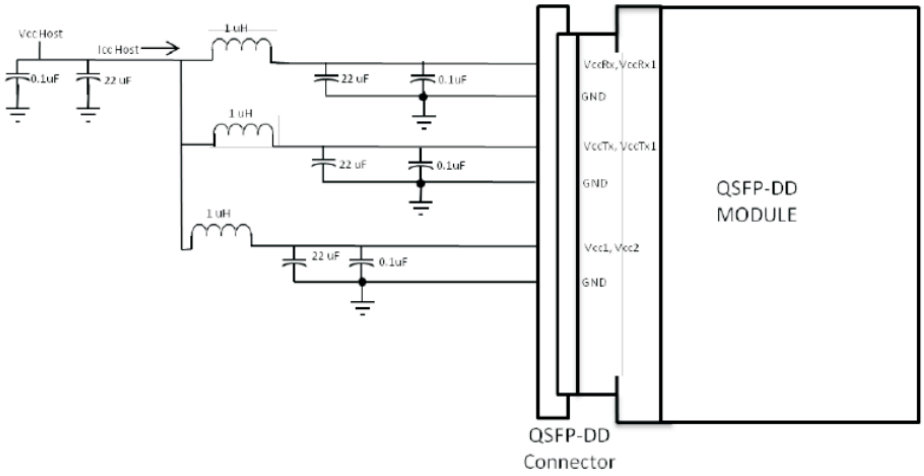
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		Vs2	Module Vendor Specific 2	3A	3
50		Vs3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data input	3A	
76		GND	Ground	1A	1

Notes:

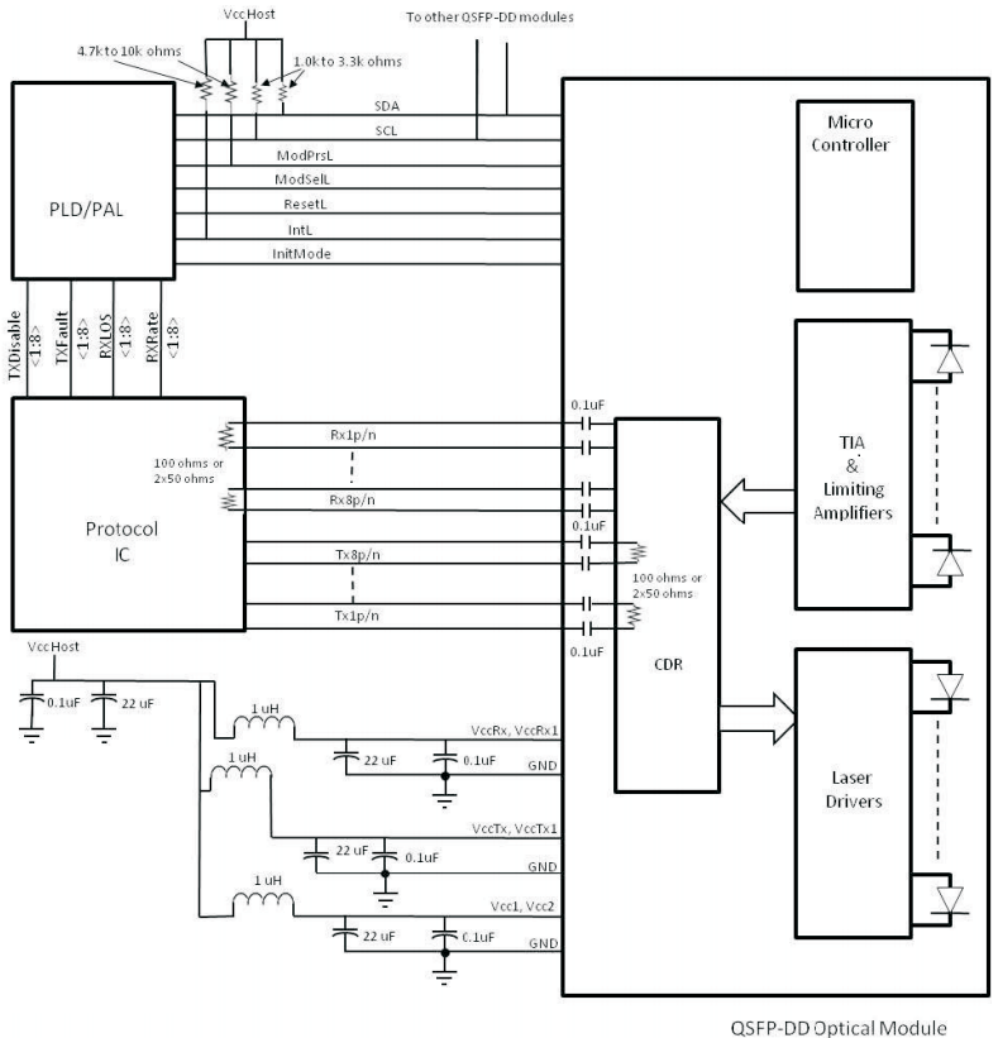
1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal -common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4.Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see the Figure below for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.



Recommended Host Board Power Supply Circuit



Recommended Interface Circuit



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Storage Temperature	TS	-40		+85	℃	
3.3V Power Supply Voltage	Vcc	-0.5		+3.6	V	
Data Input Voltage- Single Ended		-0.5			Vcc+0.5	
Control Input Voltage		-0.5		3.6	V	
Relative Humidity	RH	5		85	%	
Rx Optical Damage Threshold / Lane		5			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Bit Error Ratio (BER)				2.4^{4}x10		1.2
Case Operating Temperature	Tc	0		+70	℃	Commercial
Differential Data Input / Output Load			100		Ohms	+/-10%
Two Wire Serial (TWS) Interface Clock Rate				1	Mhz	
Data Rate per Channel				26.5625	Gbps	
Control Input Voltage High		2		Vcc+0.3	V	
Control Input Voltage Low		-0.3		0.8	V	
Fiber Length: 2000 MHz·km 50/125μm MMF (OM3)				70	m	
Fiber Length: 4700 MHz·km 50/125μm MMF (OM4)				100	m	

Notes:

1. Bit-Error-Rate (BER) is tested with PRBS 31Q pattern.
2. 400G QSFP-DD SR8 requires an electrical connector compliant with QSFP-DD MSA which is used on the host board in order to guarantee its electrical interface specification.

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Trx Power Consumption			10	12	W	
Trx Power-on Initialization Time				2000	ms	
400GAUI-8 Module Electrical Input Characteristics (Tp1)						
Single Ended Input Voltage Tolerance		-0.4		3.3	V	
Differential pk-pk input voltage				880	mV	
Differential Input Return Loss	Sdd_{11}		See Eq. 1		dB	1

Common to differential mode conversion return loss	Scd_{11}	See Eq. 2		dB	2
DC common mode voltage		-0.3	2.8	V	

Notes:

1. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}(f/14) & 8 \leq f < 19 \end{cases} \quad (dB)$$ See Eq. 1

where

f is the frequency in GHz

RLd is the CAUI-4 Chip-to-module input differential return loss

2. $$RLcd(f) \geq \begin{cases} 22 - 20(f/25.78) & 0.01 \leq f < 12.89 \\ 15 - 6(f/25.78) & 12.89 \leq f < 19 \end{cases} \quad (dB)$$ See Eq. 2

where

f is the frequency in GHz

RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
CAUI-4 Module Electrical Output Characteristics (Tp4)						
AC Common-Mode Output Voltage(RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Near-end Eye Height		70			mV	
Far-end Eye Height		30			mV	
Differential Output Return Loss	Sdd_{22}		See Eq. 1		dB	1
Common to Differential Mode Conversion Return Loss	Scd_{22}		See Eq. 2		dB	2
Transition Time (20% to 80%)		9.5			ps	
DC Common Voltage		-350		2850	mV	

Notes:

1. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}(f/14) & 8 \leq f < 19 \end{cases} \quad (dB)$$ See Eq. 1

where

f is the frequency in GHz

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2. $$RLcd(f) \geq \begin{cases} 22 - 20(f/25.78) & 0.01 \leq f < 12.89 \\ 15 - 6(f/25.78) & 12.89 \leq f < 19 \end{cases} \quad (dB)$$ See Eq. 2

where

f is the frequency in GHz

RLdc is the CAUI-4 Chip-to-module output common to differential mode conversion return loss

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver						
Center Wavelength	λ	840		860	nm	
Spectral Width – RMS	Δ λ			0.6	nm	
Average Launch Optical Power, each lane	LOP	-6		4	dBm	
Optical Modulation Amplitude, each lane	OMA	-4		3	dBm	
Launch power in OMA minus TDEC		-5.9			dBm	
Transmitter and dispersion eye closure (TDECQ), each lane	TDECQ			4.9	dB	
Extinction ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane				-30	dBm	
Optical return loss tolerance				12	dB	
Encircled Flux			≥ 86% @ 19um,≤ 30% at 4.5um			
Receiver						
Center wavelength, each lane	λ	840		860	nm	
Damage Threshold		**5**			**dBm**	
Average power at receiver input, each lane		-7.9		4	dBm	1
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				**-12**	**dB**	
Receiver sensitivity (OMAouter)			See Eq. 3		**dBm**	2.3
Stressed receiver sensitivity in OMA				-3	dBm	4
Conditions of stressed receiver sensitivity test:						
Stressed eye closure (SECQ), lane under test			**4.9**		**dB**	
OMA of each aggressor lane			3		dBm	

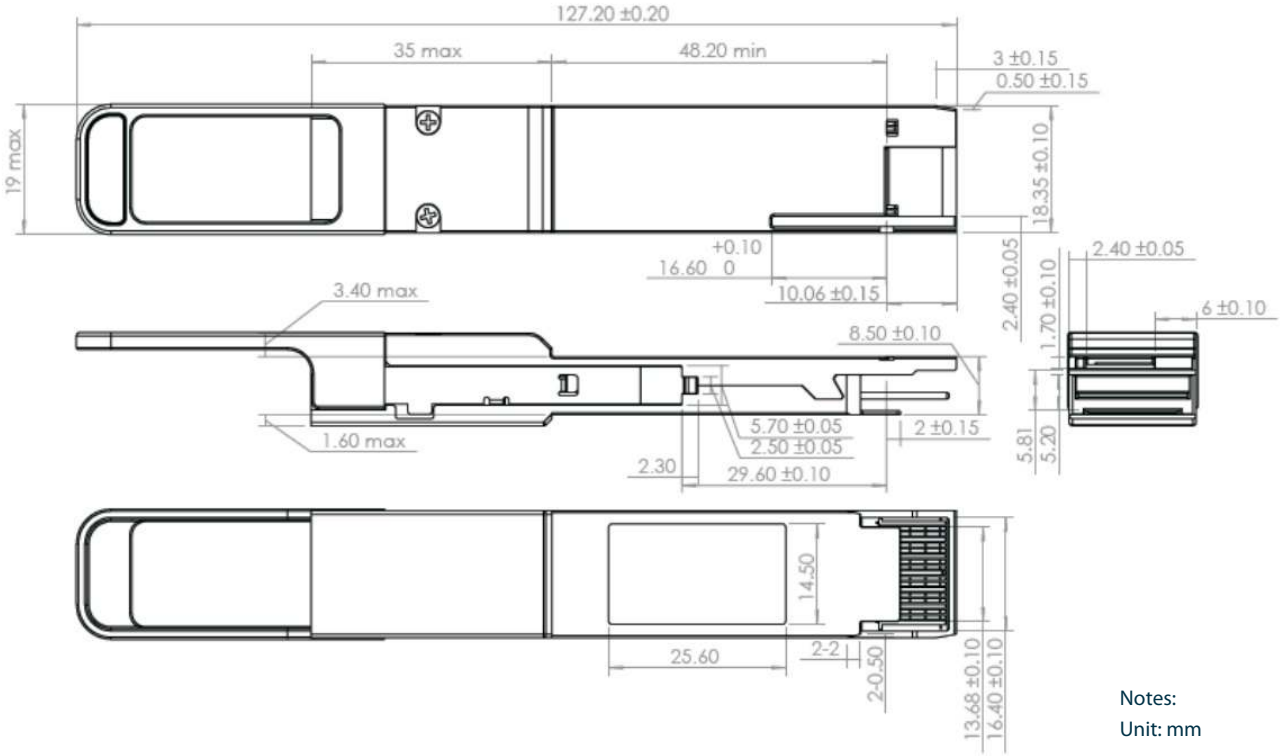
Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. Areceived power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.9 dB.
3. Equation 3: RS= Max (-6, SECQ-7.9) (dBm), where

RS is the receiver sensitivity
SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

4. Measured with conformance test signal at TP3 for the BER of 2.4 E-4

Mechanical Specifications



Notes:
Unit: mm

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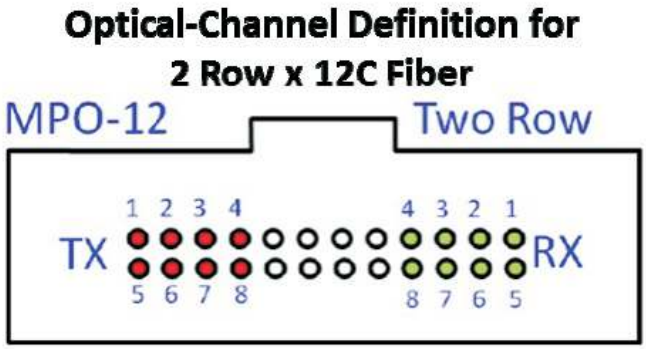
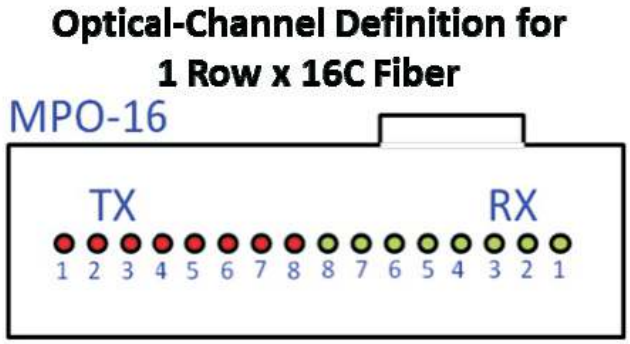
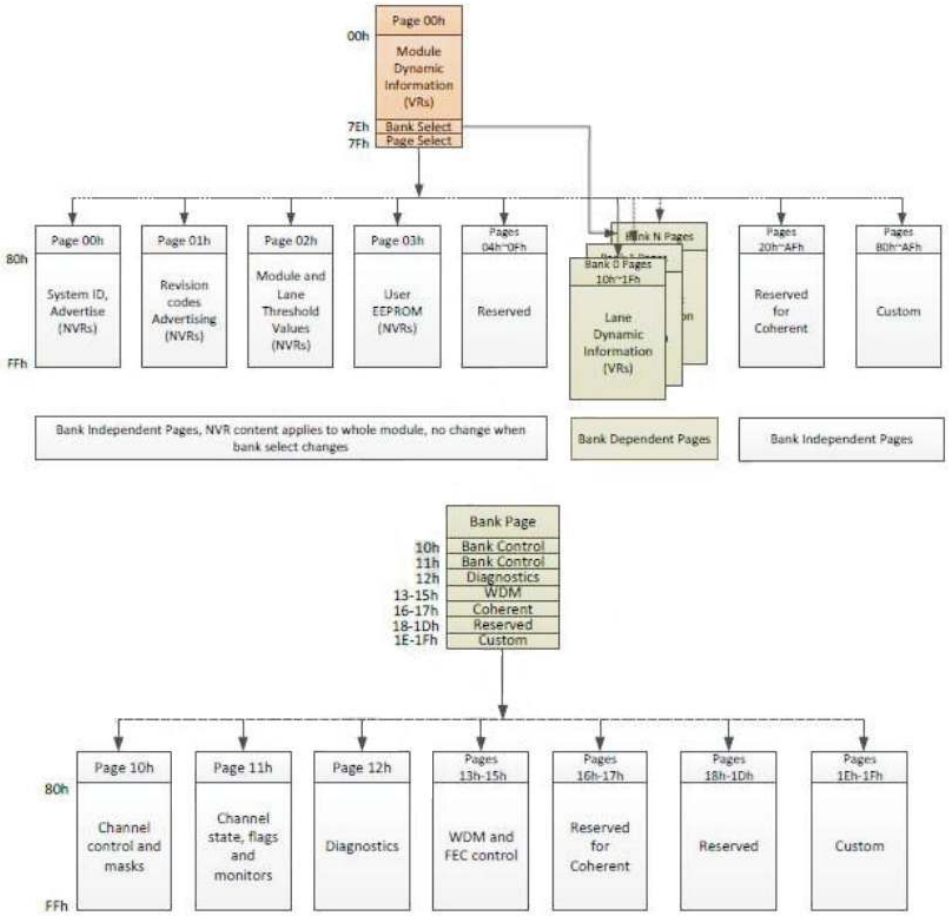




EEPROM Definitions



Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Tang Rong	Xuming Di	DingZheng	New Released.	Aug 11, 2020

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