AHV85003 and AHV85043 Chipset

Self-Powered Isolated SiC Driver Chipset with Bipolar Output

FEATURES AND BENEFITS

- Allegro Power-Thru chipset:
  - Interfaces to external pulse transformers
  - Transmits both PWM signal and bias power
  - Eliminates the need for high-side bootstrap or external bias-supply
- AEC-Q100 Grade 1 Qualification
- Bipolar drive, selectable regulated positive rail and configurable negative rails (secondary)
- Separate output gate pull-up and pull-down pins (6 A each)
- Miller clamp (internal)
- Supply voltage 10.5 V < V_{DRV} < 13.2 V
- UVLO on primary V_{DRV} and secondary V_{SECP} supply rails
- EN (enable) input and $\overline{FAULT}$ output pins
- Overtemperature protection (primary and secondary)
- Wide operating temperature range T_A –40°C to 125°C
- When matched with recommended external transformers:
  - Delivers up to 130 nC gate charge at 21 V (secondary)
  - 85 ns prop delay (typical)
  - < 50 ns skew and pulse-width distortion
  - CMTI > 100 V/ns dV/dt immunity

PACKAGE

20-pin QFN 4 mm × 4 mm
Not to scale

DESCRIPTION

The AHV85003 and AHV85043 gate-driver chipset is optimized for driving discrete SiC FETs in applications such as automotive on-board chargers (OBCs), solar inverters, industrial robotics, data-center power shelves, and general power-supply applications. When combined with one of the recommended external transformers, it provides a self-powered isolated gate-drive solution that is ideal for multiple applications and topologies. For a selection of recommended third-party transformers, as well as key parameters and transformer-qualification methods, see the Allegro application note Design Guide for AHV85003 and AHV85043 Self-Powered Isolated SiC Driver Chipset with Bipolar-Output External Transformer (AN296372). [1]

The chipset transmits both the pulse-width-modulated (PWM) signal and the gate-bias power through the external transformer, which eliminates the need for any external auxiliary bias supply or high-side bootstrap. An isolated bipolar positive/negative output bias supply is generated on the isolated secondary side of the driver, which eliminates the need for external circuitry to generate a split-supply rail. For improved dV/dt immunity, the bipolar output rails feature a selectable regulated positive rail and an adjustable negative off-state rail. This greatly simplifies the system design and reduces electromagnetic interference (EMI) through reduced total common-mode (CM) capacitance. It allows the driving of a floating switch in any location in a

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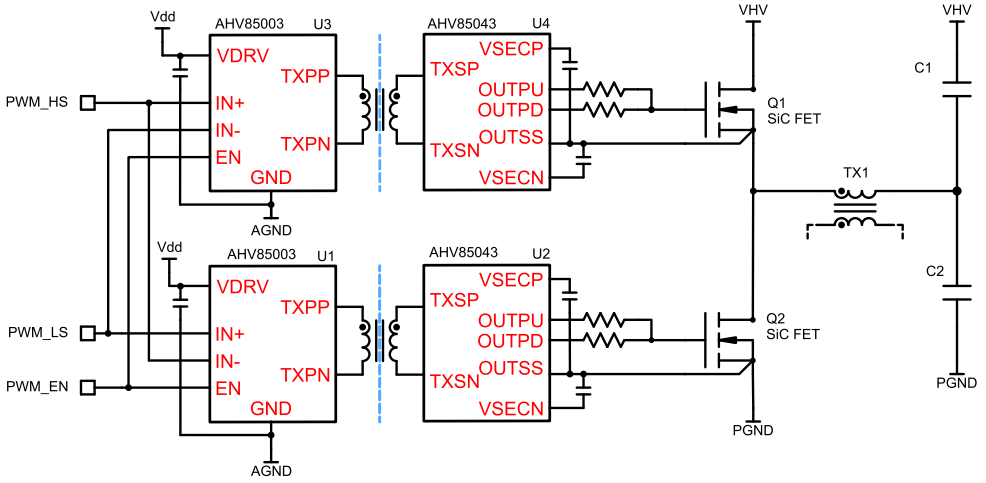

Figure 1: Simplified Typical Application Circuit

[1] https://www.allegromicro.com/-/media/files/application-notes/an296372-ahv85003-and-ahv85043-chipset-external-transformer-design-guidelines

DESCRIPTION (continued)

switching power topology, making it ideal for half-bridge, multi-level topologies, and any topology with a floating or high-side switch.

The chipset has a fast propagation delay and a high-peak source/sink capability to efficiently drive SiC FETs in high-frequency designs. High common-mode transient immunity (CMTI), combined with isolated outputs for both bias power and drive, make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity. Several protection features are integrated, including undervoltage lockout (UVLO) on primary and secondary bias rails, secondary-bias-rail overvoltage, fast-response enable input, and overtemperature shutdown. When the secondary bias rails are in regulation and a fault is not detected, the open-drain $\overline{\text{FAULT}}$ output is de-asserted. Both of the ICs in the chipset are available in a standard 20-pin quad-flat no-lead (QFN) package (4 mm × 4 mm).

SELECTION GUIDE

Part Number	Device	VSECP Setting	Package Description	Packing/Quantity	Package Size (L × W × H)
AHV85003K15ESTR	Primary	15 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm
AHV85043K15ESTR	Secondary	15 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm
AHV85003K18ESTR	Primary	18 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm
AHV85043K18ESTR	Secondary	18 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm
AHV85003K20ESTR	Primary	20 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm
AHV85043K20ESTR	Secondary	20 V	20-Pin QFN	Reel, 1500	4 mm × 4 mm × 0.75 mm

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
AHV85003				
Supply Voltage	V_{DRV}	DRV pin voltage relative to GND	–0.5 to 17	V
Input Logic Positive Voltage	V_{IN+}	IN+ pin voltage relative to GND	–0.5 to 6.5	V
Input Logic Negative Voltage	$V_{IN–}$	IN– pin voltage relative to GND	–0.5 to 6.5	V
Enable Voltage	V_{EN}	EN pin	–0.5 to V_{DRV}	V
Active Fault Voltage	V_{FAULT}	$\overline{\text{FAULT}}$ pin	–0.5 to V_{DRV}	V
Power Throughput	V_{PWRSEL}	PWRSEL pin	–0.5 to V_{DRV}	V
Active Fault Sink Current	I_{FAULT}	$\overline{\text{FAULT}}$ pin	10	mA
Transformer Primary Positive Terminal	V_{TXPP}	TXPP pin ouput; voltage cannot be forced; maximum spike voltage (<20 ns) during switching activity	–5 to 18	V
Transformer Primary Negative Terminal	V_{TXPN}	TXPN pin ouput; voltage cannot be forced; maximum spike voltage (<20 ns) during switching activity	–5 to 18	V
Bootstrap Capacitor Positive Terminal	V_{BSP}	BSP pin voltage relative to TXPP	V_{TXPP} – 0.3 to V_{TXPP} + 3.6	V
Bootstrap Capacitor Negative Terminal	V_{BSN}	BSN pin voltage relative to TXPN	V_{TXPN} – 0.3 to V_{TXPN} + 3.6	V
Operating Ambient Temperature	T_A		–40 to 125	°C
Junction Temperature	$T_{J(max)}$		–40 to 150	°C
Storage Temperature	T_{stg}		–40 to 150	°C
AHV85043				
Output Drive Pull Up	V_{OUTPU}	OUTPU pin output relative to VSECN; cannot be forced; maximum spike voltage (<20 ns) during switching activity	–2 to 35	V
Output Drive Pull Down	V_{OUTPD}	OUTPD pin output relative to VSECN; cannot be forced; maximum spike voltage (<20 ns) during switching activity	–2 to 35	V
Output Drive Clamp	V_{CLAMP}	CLAMP pin output relative to VSECN; cannot be forced; maximum spike voltage (<20 ns) during switching activity	–2 to 35	V
Transformer Secondary Positive Terminal	V_{TXSP}	TXSP pin output relative to VSECN; VSECP refers to the regulated VSECP voltage	–0.5 to V_{SECP} + 0.5	V
Transformer Secondary Negative Terminal	V_{TXSN}	TXSN pin output relative to VSECN; VSECP refers to the regulated VSECP voltage	–0.5 to V_{SECP} + 0.5	V
Secondary Bias Rail Current	I_{VSECP}	VSECP pin output relative to VSECN; cannot be forced; voltage regulated at $I_{VSECP} – I_{VSECN}$	20	mA
Source Connection	V_{SOURCE}	SOURCE pin output relative to VSECN; cannot be forced; voltage regulated at V_{SECN}	20	mA
Voltage Sense Pin	V_{FBN}	FBN pin voltage relative to VSECN	–0.5 to +7.5	V+
Operating Ambient Temperature	T_A		–40 to 125	°C
Junction Temperature	$T_{J(max)}$		–40 to 150	°C
Storage Temperature	T_{stg}		–40 to 150	°C
Charge-Pump Capacitor Positive Terminal	V_{CP}	CP pin voltage relative to VSECP voltage	V_{SECP} – 0.3 to V_{SECP} + 3.6	V

[1] Stresses beyond those listed in this table might cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods might affect device reliability.

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ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}		±2	kV
Charged Device Model	V_{CDM}		±500	V

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1][2]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$		75 to 136	°C/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$		2	°C/W

[1] Additional thermal information is available on the Allegro website.
[2] Standard board.

MSL RATING

Device	MSL Rating	Maximum Floor Life at Standard Ambient (30°C/60%RH)	Maximum Peak Reflow Temperature	Pre-Reflow Bake Requirement
AHV85003 and AHV85043 Chipset	MSL2 [1][2]	1 year	260°C	Per JEDEC J-STD-033C

[1] Per JEDEC J-STD-033C, these devices are rated MSL2. This MSL2 rating means that once the sealed production packaging is opened, if the device is stored in less-than-standard ambient conditions (30°C and 60% relative humidity (RH)), the device must be reflowed within a “floor life” of 1 year. The peak reflow temperature should not exceed the maximum specified in the MSL Rating table.
[2] If the device is exposed to the standard ambient condition for more than 1 year, it must be baked before reflow to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C. If the devices are exposed to higher temperature and/or RH compared to the standard ambient of 30°C/60% RH, the floor-life reduces due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient condition, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow as a precaution to avoid potential device damage during reflow soldering.

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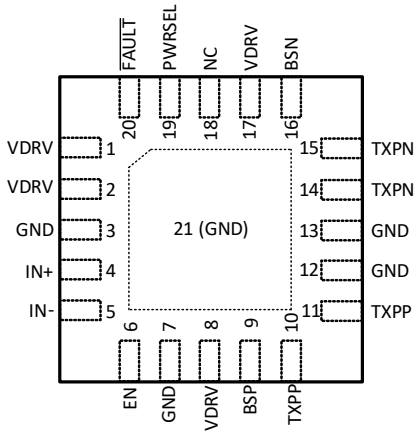
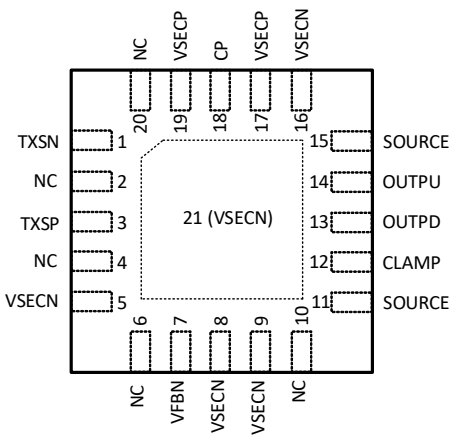
PINOUT DIAGRAM AND TERMINAL LIST

AHV85003
(Top View)



AHV85043
(TOP View)



Driver Chipset Primary IC

Pinout Table [1]

Name	Number	Function
VDRV	1, 2, 8, 17	Primary bias supply voltage
PWRSEL	19	Adjust power throughput
$\overline{\text{FAULT}}$	20	Fault output, open drain
GND	3, 7, 12, 13	Ground
IN+	4	Input PWM signal (positive logic)
IN–	5	Input PWM signal (negative logic)
EN	6	Enable
BSN	16	Bootstrap capacitor (with respect to TXPN)
TXPP	10, 11	Positive connection to external transformer primary winding
TXPN	14, 15	Negative connection to external transformer primary winding
BSP	9	Bootstrap capacitor (with respect to TXPP)
Exposed Pad (GND)	21	Exposed pad (pin 21) is internally connected to GND; the exposed pad does not replace the GND pin

[1] Where multiple power and ground pins are provided (e.g., VDRV, GND, VSECP, VSECN, SOURCE), all pins must be connected

Driver Chipset Secondary IC

Pinout Table [1]

Name	Number	Function
VSECP	17, 19	Positive gate-drive supply rail (referenced to the SOURCE pin), internally rectified and regulated from the power pulses at the TXSP and TXSN pins
TXSP	3	Positive connection to external-transformer secondary winding
TXSN	1	Negative connection to external-transformer secondary winding
VSECN	5, 9, 8, 16	Negative gate-drive supply rail (referenced to the SOURCE pin), internally rectified and regulated from the power pulses at the TXSP and TXSN pins
VFBN	7	Feedback input for the negative-rail regulator (VSECN), connected to an external resistor divider between SOURCE and VSECN.
SOURCE	11, 15	Source connection of the driven SiC FET
CLAMP	12	Miller clamp pull-down to VSECN
OUTPD	13	Output pull-down (turn-off) of the gate driver, referenced to VSECN
OUTPU	14	Output pull-up (turn-on) of the gate driver, referenced to VSECP
CP	18	Charge-pump capacitor positive terminal, referenced to VSECP
Exposed Pad (VSECN)	21	Exposed pad (pin 21) is internally connected to VSECN; the exposed pad does not replace the VSECN pin.

[1] Where multiple power and ground pins are provided (e.g., VDRV, GND, VSECP, VSECN, SOURCE), all pins must be connected

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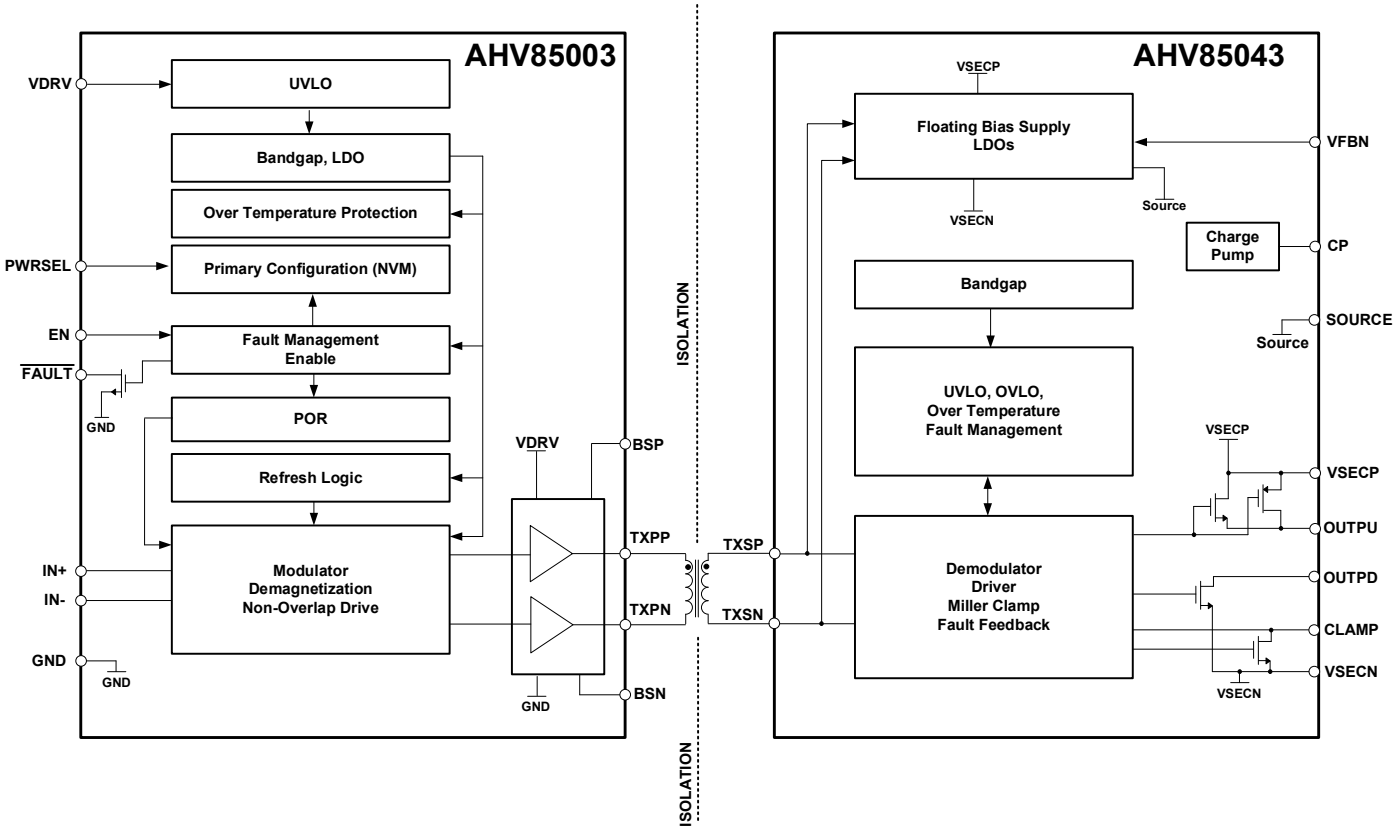

Figure 2: AHV85003/AHV85043 Chipset Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at –40°C < T_J < 150°C, 10.5 V < V_{DRV} < 13.2 V, EN = high, primary/secondary interfaced through external compliant transformer, [1] unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ. [2]	Max.	Unit
AHV85003						
Supply Voltage	V_{DRV}		10.5	12	13.2	V
Undervoltage Lockout	$V_{DRV(UVR)}$	V_{DRV} rising	9.5	10	10.5	V
	$V_{DRV(UVF)}$	V_{DRV} falling	8.5	9	9.5	V
Undervoltage Hysteresis	$V_{DRV(HYS)}$		0.7	1	–	V
Supply Current [3]	$I_{DRV(DIS)}$	Quiescent current, EN = low	–	–	2.5	mA
	$I_{DRV(Q)}$	Quiescent current, EN = high, IN = DC (low or high), PWRSEL = high	–	–	4.3	mA
	$I_{DRV(SW)}$	Switching current, EN = high, IN = 100 kHz (50% duty), PWRSEL = high, load (gate charge) = 0 nC	–	–	12.5	mA
Input Logic Levels (IN+, IN–, EN)	$V_{IN(L)}$	Logic low	–	–	0.8	V
	$V_{IN(H)}$	Logic high	2	–	–	V
	$V_{IN(HYS)}$	Hysteresis	–	0.8	–	V
	R_{IN}	Internal pull-down (IN+) or pull-up (IN–)	–	150	–	kΩ
	R_{EN}	Internal pull-down (EN)	–	300	–	kΩ
EN Deglitch	t_{ENLH}	EN input deglitch, low-to-high transition	–	60	–	µs
	t_{ENHL}	EN input deglitch, high-to-low transition	–	500	–	ns
$\overline{FAULT}$	$V_{FLT(L)}$	4.5 mA sink current (1 kΩ pull-up to 5 V)	–	–	0.5	V
Overtemperature Shutdown	$T_{SDP(R)}$	Primary-side sensor, rising threshold	153	163	173	°C
	$T_{SDP(F)}$	Primary-side sensor, falling threshold	130	140	150	°C

[1] A list of recommended transformers, a transformer selection method, and a validation method are provided in the application note the Allegro application note Design Guide for AHV85003 and AHV85043 Self-Powered Isolated SiC Driver Chipset with Bipolar-Output External Transformer (AN296372).

[2] Typical values are at T_A = 25°C and V_{DRV} = 12 V, unless stated otherwise. Performance might vary for individual units, within the specified maximum and minimum limits.
[3] Supply current is for an AHV85003 and AHV85043 chipset when used with a recommended external transformer.

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ELECTRICAL CHARACTERISTICS: Valid at –40°C < T_J < 150°C, 10.5 V < V_{DRV} < 13.2 V, EN = high, primary/secondary interfaced through external compliant transformer, [1] unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ. [2]	Max.	Unit
AHV85043						
V_{SECP} Regulation Set Point, 15 V Option	V_{SECP_15}	Referenced to SOURCE	14.25	15	15.75	V
V_{SECP} Regulation Set Point, 18 V Option	V_{SECP_18}		17.1	18	18.9	V
V_{SECP} Regulation Set Point, 20 V Option	V_{SECP_20}		19	20	21	V
Undervoltage Lockout	$V_{SECP(UVF)}$	V_{SECP} falling disable threshold, percentage of nominal regulation level	–	80	–	%V
	$V_{SECP(UVR)}$	V_{SECP} rising enable threshold, percentage of nominal regulation level	–	85	–	%V
Undervoltage Deglitch	t_{VSECUV}		–	20	–	µs
Overvoltage Lockout	$V_{SECP(OVR)}$	V_{SECP} rising disable threshold, percentage of nominal regulation level	–	115	–	%µs
Overvoltage Deglitch	$t_{VSECPOV}$		–	20	–	µs
Feedback Reference V_{SECN} [3]	V_{FBP}	VFBN input referenced to V_{SECN}	–	1	–	V
Overvoltage Lockout	$V_{FBP(OV)}$	VFBN overvoltage	–	1.22	–	V
Output Driver Peak Current	I_{SOURCE}	OUTPU	–	6	–	A
	I_{SINK}	OUTPD	–	6	–	A
Output Resistance	R_{PD}	OUTPD pull-down R_{DSON}	–	–	1	Ω
	R_{PU}	OUTPU internal PMOS pull-up R_{DSON}	–	–	10	Ω
Clamp Detection Threshold	V_{CLP}	Referenced to V_{SECN}	–	2	–	V
Clamp Peak Current [4]	I_{CLP}		–	4	–	A
Clamp On-Resistance	$R_{DSON-CLP}$		–	–	1.5	Ω
Overtemperature Shutdown	$T_{SDS(R)}$	Secondary-side sensor, rising threshold	150	160	170	°C
	$T_{SDS(F)}$	Secondary-side sensor, falling threshold	130	140	150	°C

[1] A list of recommended transformers, a transformer selection method, and a validation method are provided in the application note the Allegro application note Design Guide for AHV85003 and AHV85043 Self-Powered Isolated SiC Driver Chipset with Bipolar-Output External Transformer (AN296372).

[2] Typical values are at T_A = 25°C and V_{DRV} = 12 V, unless stated otherwise. Performance might vary for individual units, within the specified maximum and minimum limits.

[3] Parameter is not production-tested; guaranteed by design and characterization.

[4] Supply current is for an AHV85003 and AHV85043 chipset when used with a recommended external transformer.

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ELECTRICAL CHARACTERISTICS: Valid at –40°C < T_J < 150°C, 10.5 V < V_{DRV} < 13.2 V, EN = high, primary/secondary interfaced through external compliant transformer, [1] unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ. [2]	Max.	Unit
TIMING CHARACTERISTICS—AHV85003 AND AHV85043 CHIPSET WITH RECOMMENDED EXTERNAL TRANSFORMER						
Propagation Delay [3][4]	t_{PLH}	Delay from IN+ low-to-high transition to OUTPx low-to-high transition R_{EXT_PU} = 10 Ω, C_{OUT} = 100 pF	–	85	135	ns
	t_{PHL}	Delay from IN+ high-to-low transition to OUTPx high-to-low transition R_{EXT_PD} = 10 Ω, C_{OUT} = 100 pF	–	85	135	ns
Pulse-Width Distortion [3][4]	t_{PWD}	$\lvert t_{PLH} - t_{PHL} \rvert$	–	5	50	ns
Propagation-Delay Matching		Part-to-part variation	–	10	–	ns
PWM Frequency	f_{PWM}	Supported input frequency range at IN+/IN– Can be operated at DC (i.e., IN+/IN– continuously low or high)	DC	–	450	kHz
Output Rise Time	t_r	R_{EXT_PU} = 1 Ω, C_{OUT} = 1 nF, 20–80%	–	10	–	ns
Output Fall Time	t_f	R_{EXT_PD} = 1 Ω, C_{OUT} = 1 nF, 20–80%	–	10	–	ns

[1] A list of recommended transformers, a transformer selection method, and a validation method are provided in the application note the Allegro application note Design Guide for AHV85003 and AHV85043 Self-Powered Isolated SiC Driver Chipset with Bipolar-Output External Transformer (AN296372).

[2] Typical values are at T_A = 25°C and V_{DRV} = 12 V, unless stated otherwise. Performance might vary for individual units, within the specified maximum and minimum limits.

[3] Parameter is not production-tested; guaranteed by design and characterization.

[4] The maximum propagation delay is specified in the event of an overlap of a PWM transition (IN+, IN– pins) with an internally generated refresh pulse

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FUNCTIONAL DESCRIPTION

The AHV85003 and AHV85043 chipset is an isolated SiC FET gate-driver chipset where the AHV85003 is the primary-side IC (transmitter, TX) and the AHV85043 is the secondary-side IC (receiver, RX). The chipset interfaces to an external transformer, connected between the TX and RX ICs, which transmits both the PWM signal and the gate-driver bias power for the isolated side. The required transformer consists of a simple two-winding, four-pin structure.

A selection of recommended third-party transformers, as well as a guideline for selecting transformers, is provided in the Allegro application note Design Guide for AHV85003 and AHV85043 Self-Powered Isolated SiC Driver Chipset with Bipolar-Output External Transformer (AN296372). [1] These transformers have been fully tested and validated for use with the AHV85003 and AHV85043 chipset. The required transformer can be selected to suit different system-design requirements, e.g., the required system creepage distance, isolation rating, and target FET drive voltage and gate charge.

V_{DRV} Supply and UVLO

In conjunction with the external transformer, the AHV85003 and AHV85043 chipset requires a single 12 V supply (V_{DRV}) to power the driver chipset. AHV85003 is powered directly from the 12 V V_{DRV} supply on the primary side. On the isolated secondary-side, bias power for the AHV85043 is generated by internally rectifying and regulating the TXSP/TXSN pulses from the external transformer. A dedicated secondary-side bias supply is not required. Undervoltage protection is provided on the V_{DRV} supply to ensure proper operations. At startup, the primary circuit remains in a low-power standby mode until V_{DRV} exceeds the UVLO rising threshold, $V_{DRV(UVR)}$, and power is not transferred to the secondary circuit. While running, if V_{DRV} reduces to less than the UVLO falling threshold, $V_{DRV(UVF)}$, the $\overline{\text{FAULT}}$ pin is pulled low, the PWM signal and power transfer to the secondary side are halted, and the internal REF regulator is disabled. When the V_{DRV} level recovers and returns greater than the UVLO rising threshold, $V_{DRV(UVR)}$, the system restarts.

Startup

When the primary-supply voltage, V_{DRV}, is applied to the primary-side AHV85003 IC, it remains in low-power mode until V_{DRV} exceeds the UVLO threshold. Once the UVLO threshold is exceeded, the internal low-voltage dropout (LDO) regulators are enabled. If the EN input is held low, the primary side remains in a low-power standby mode, with the $\overline{\text{FAULT}}$ output held low. Once EN is high, or if EN is already high when the V_{DRV} UVLO is released, the primary side of the driver enables power transfer to the secondary side, to charge the secondary-side isolated bias rails. This is achieved by sending pulses to the TXPP and TXPN pins to energize the external transformer. On the secondary-side AHV85043 IC, when the secondary-side bias rails have settled to the target regulation levels, and if a fault is not detected on either the primary side or the secondary side, the open-drain $\overline{\text{FAULT}}$ pin is allowed to go high, via the required external pull-up resistor. This indicates to the system controller that the driver is ready to accept PWM signal inputs. Any PWM signal input at the IN+ or IN– pin is ignored until the internal $\overline{\text{FAULT}}$ pull-down is released.

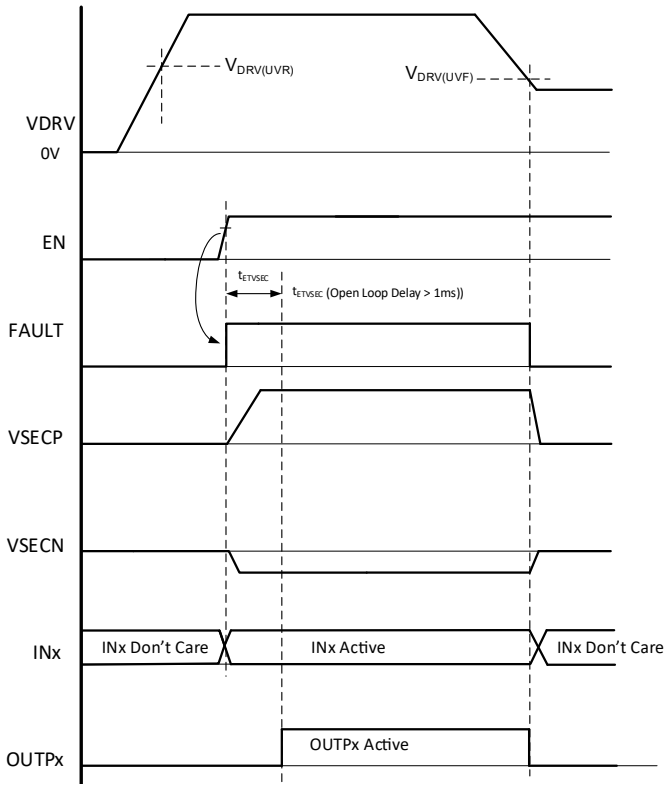

Figure 3: Startup Time and Sequence and V_{DRV} Supply UVLO, AHV85003 and AHV85043 Chipset with Recommended External Transformer

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Isolated Power and PWM Transfer

The secondary side (AHV85043) is powered through the external pulse transformer. The pulse transformer is also used to transfer the encoded PWM data from the primary side. The energy required to power the secondary side is transferred at each transition of the PWM signal (i.e., at the IN– and IN+ inputs). On the isolated side of the external transformer, the TXSP and TXSN pins of the AHV85043 rectify these pulses, to transfer the energy to the VSECP and VSECN rails.

If the PWM signal frequency at the AHV85003 INx pins is too low, or if INx is set to DC in either the high (1) or low (0) state, the AHV85003 transmits a refresh pulse to the external transformer through the TXPP and TXPN pins. This mechanism ensures that the VSECP and VSECN rails do not sag due to the internal bias consumption of the AHV85043 and that regulation is maintained when a PWM signal transition is not present at the AHV85003 INx pins or when transition becomes infrequent due to frequency and/or duty cycle.

When INx is low or high for longer than the refresh timeout period, t_{PER_REF}, the internal logic automatically generates a refresh pulse, and the refresh timer is reset. Each time an edge transition is detected on the INx pins, the refresh timer is also reset.

A benefit of the refresh pulse mechanism is that whenever the INx signal to the AHV85003 is low for a continuous long duration—for example, at startup—energy transfer to the isolated side continues via the AHV85043 TXSP/TXSN pins, to charge the isolated bias rails VSECP and VSECN. As a result, a bootstrap or isolated supply is not required to get the isolated side of the driver chipset started, so the chipset is ready to respond immediately to signals at the INx pins as soon as the $\overline{\text{FAULT}}$ pin pull-down is released.

The PWM pulse (inputs IN+ and IN–) and the internally generated refresh pulses are asynchronous. In the event of an overlap between the PWM pulse and a refresh pulse, the PWM-related pulse (TXPP or TXPN) is delayed by a fixed time (typically 50 ns).

A feed-forward function ensures that a constant amount of power is delivered to the secondary side, independent of V_{DRV} supply variations.

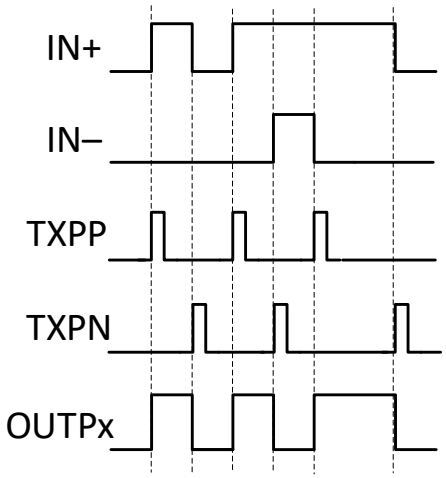

Figure 4: PMW Encoding and Power Transfer

Enable Input

The AHV85003 enable (EN) pin can be pulled low to disable the TXPP and TXPN signals. This disables the PWM signal transfer to the output and forces the AHV85003 into a low-power mode. The isolated secondary bias rails for the AHV85043 are also disabled.

The EN pin includes an internal weak pull-down, and a deglitch filter to minimize false toggling due to noise.

The EN pin is rated up to a maximum, V_{DRV}, so it can be tied high to any system with a 5 V or 3.3 V logic rail, or to V_{DRV}, to enable the AHV85003 driver.

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Fault Output and Fault Conditions

Fault conditions, detected on either the AHV85003 (primary) or AHV85043 (secondary), are reported to the AHV85003 $\overline{\text{FAULT}}$ output pin. The active-low open-drain $\overline{\text{FAULT}}$ pin requires an external pull-up resistor. The pull-up can be tied to any suitable voltage rail (i.e., 3.3 V or 5 V), up to V_{DRV}.

During startup, the $\overline{\text{FAULT}}$ pin is internally pulled low to flag to the external system controller that the driver is not ready to respond to PWM signals at the INx pins. Upon successful startup, without a fault detected, the $\overline{\text{FAULT}}$ pin becomes high impedance to notify the system controller that the driver is ready.

During operation, if any fault is detected by either the primary-side AHV85003 or the secondary-side AHV85043, the $\overline{\text{FAULT}}$ pin is internally pulled low, to alert the system controller. At the same time, the AHV85043 output driver pull-up (OUTPU) is disabled, and the output driver pull-down (OUTPD) pin is held low, regardless of the signal level at the INx pins.

This open-drain configuration allows the $\overline{\text{FAULT}}$ pins of multiple driver channels to be OR-ed together, so that the $\overline{\text{FAULT}}$ bus only becomes high impedance when all driver channels are ready. Alternatively, individual driver $\overline{\text{FAULT}}$ pins can be connected to different digital input pins of the system controller, so that the specific fault source can be determined.

Fault conditions detected on the AHV85043 are transmitted to the primary side through the pulse transformer. A short-duration filter is applied on the primary-side detection. If the $\overline{\text{FAULT}}$ pin functionality is not used or is not required on the primary side, this pin can remain unconnected. Fault conditions are listed in Table 1.

Table 1: Fault Sources and Conditions

Monitor	Function	$\overline{\text{FAULT}}$ Pin
VDRV supply (AHV85003)	Undervoltage lockout	Yes
Junction (AHV85003)	Overtemperature Lockout	Yes
VSECP (AHV85043)	Undervoltage Lockout Overvoltage Lockout	Yes
VFBN (AHV85043)	VSECN Feedback (VFBN) Overvoltage Lockout	Yes
Junction (AHV85043)	Overtemperature Lockout	Yes

PWM Inputs

The AHV85003 includes two general-purpose PWM input pins IN+ and IN–. These pins can be driven with any type of signal, DC (continuous logic low or logic high) or any arbitrary PWM pulse train, as long as the signal timing adheres to the maximum frequency and minimum on-time and off-time specifications.

The IN+ and IN– pins can be used either: with typical positive logic, by using IN+ only, with IN– tied to GND; or with inverted negative logic, by using IN–, with IN+ tied high. Both PWM input pins are compatible with standard 3.3 V or 5 V logic signals from a system controller, and both pins feature Schmitt-type inputs with wide hysteresis for high noise immunity. The truth table for IN+ and IN– is shown in Table 2, and an example timing diagram is shown in Figure 5.

Input pins IN+ and IN– have a 150 kΩ pull-down and pull-up, respectively. These built-in resistors prevent the inputs from floating if they remain open. Nevertheless, any input not used in the application should be tied low (IN–) or high (IN+).

Table 2: AHV85003 Truth Table for IN+ and IN– Input Pins

IN+	IN–	OUTPx
0	0	0
0	1	0
1	0	1
1	1	0

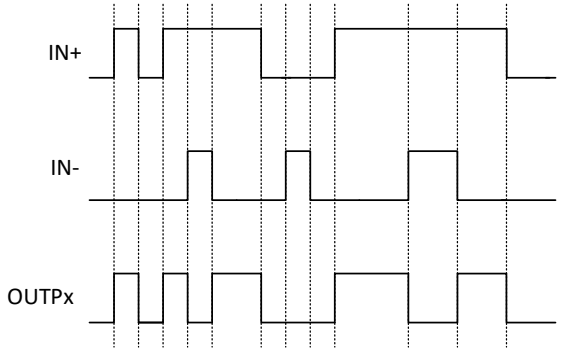

Figure 5: Logic Waveforms for IN+ and IN– to OUTPx Pins, AHV85003 and AHV85043 Chipset with Recommended External Transformer

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Isolated Secondary Bias Rails

The voltage of the positive gate-drive bias rail, V_{SECP}, is fixed (values of +15 V, +18 V or +20 V). The voltage of the negative (relative to the SOURCE pin) off-state gate rail, V_{SECN}, is user-adjustable through a voltage divider.

The negative rail voltage can be configured in the range 0 V to –5 V. The recommended voltage selections for both the positive rail and the negative rail should not exceed 21 V, i.e.:

Equation 1:

$$V_{SECP} - V_{SECN} \leq 21\ V$$

For selection of the voltage divider resistors and decoupling, refer to the Applications Information section.

Output Driver Stage

The AHV85043 output driver stage features separate pull-up (OUTPU) and pull-down (OUTPD) pins to allow separate tuning of turn-on and turn-off speed with external gate resistors.

The pull-up structure consists of parallel N-channel and P-channel MOSFETs. The N-channel device provides the necessary high-peak source current during the initial gate-charging phase, when the high-source current is needed most. The parallel P-channel continues to pull up during the latter portion of the gate-charging phase, to bring the external gate voltage up to the V_{SECP} positive gate drive level, to achieve the lowest R_{DSON} performance in the SiC FET that is being driven.

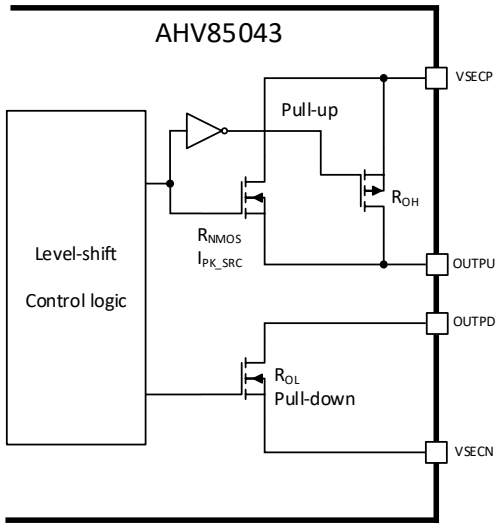

Figure 6: Output Driver Simplified Structure, AHV85043

The pull-down structure consists of a low R_{DSON} N-channel MOSFET for maximum peak sink current, for fast turn-off of the SiC FET.

When not powered or when the device is in a fault condition, the OUTPD is in low-impedance mode to prevent turn-on of the SiC FET.

Miller Clamp

A built-in Miller clamp pull-down is provided on the AHV85043 to increase robustness to false turn-on events arising from fast dV/dt events on the SiC FET drain. The Miller clamp is activated during turnoff, after the OUTPD pin has already discharged the external SiC FET gate capacitance to less than the Miller clamp threshold, relative to V_{SECN}. The Miller clamp provides a low-impedance path directly from the SiC FET gate to V_{SECN}, bypassing the external gate resistor. This low-impedance clamp absorbs current spikes, caused by fast dV/dt on the SiC FET drain, that are injected into the SiC FET gate and otherwise force large current spikes in the FET Miller capacitance, C_{GD}. The Miller clamp pull-down is reset upon each subsequent PWM rising edge.

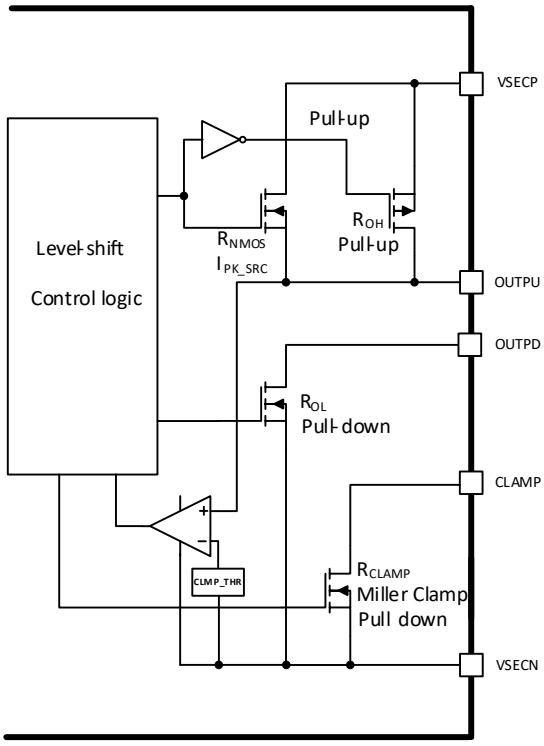

Figure 7: Miller Clamp, Simplified Block Diagram, AHV85043

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Overtemperature Shutdown

The internal overtemperature shutdown feature provides protection if the internal IC temperature of either the AHV85003 or AHV85043 becomes excessive; this protection is nonlatching and recovers once the internal IC temperature cools to less than the recovery level. If an overtemperature condition is detected, the AHV85043 output driver pull-up (OUTPU) pin is disabled, and the output driver pull-down (OUTPD) pin is held low, regardless of the signal level at the INx pins.

If the overtemperature fault is detected on the secondary-side AHV85043, the fault is communicated to the primary-side AHV85003 as described in the Fault Output section.

As with all internal faults, the open-drain $\overline{\text{FAULT}}$ pin is also pulled low, to flag the fault condition to the system controller.

Power Select Pin PWRSEL

The AHV85003 PWRSEL pin allows the user to adjust the rate of energy transfer to the secondary side, to suit load FETs with differing levels of gate charge. Three settings are selectable by connecting the PWRSEL pin to GND or V_{DRV}, or by leaving the PWRSEL pin open (floating). The PWRSEL pin setting is sampled only during startup and is in force until the VDRV pin is power cycled.

If the selected PWRSEL setting is too high compared to the level of the load FET $Q_{G(TOT)}$, excess energy is delivered to the secondary side and is dissipated in the internal regulators, resulting in higher package power dissipation than necessary.

If the PWRSEL setting is too low, insufficient energy is transferred, resulting in a drop in the levels of the secondary-side supply rails (V_{SECP}, V_{SECN}) when the device is enabled, and PWM is applied to the INx pin(s). Eventually, this causes the V_{SECP} UVLO to trigger. If V_{SECP} UVLO repeatedly triggers, a higher PWRSEL setting should be selected. The recommended maximum $Q_{G(TOT)}$ for each PWRSEL setting to assist with choosing the right setting is shown in Table 3.

Table 3: PWRSEL vs. Maximum $Q_{G(TOT)}$, AHV85003 and AHV85043 Chipset with Recommended External Transformer

PWRSEL Connection	Pulse-Width Range	Maximum $Q_{G(TOT)}$ (nC)
GND	Low	50
Open (floating)	Medium	85
VDRV	High	130

Power Dissipation and Derating

Several factors can contribute to the power dissipated in the primary-side and secondary-side ICs. These factors are the power-transfer selection (PWRSEL pin configuration), the PWM frequency, the settings of the secondary-side power rails (VSECP, VSECN), the gate resistors (series resistor between the OUTPU and OUTPD outputs and the gate of the power SiC MOSFET), and the load total gate charge $Q_{G(TOT)}$.

System design must ensure that the ICs are operated within the maximum-power-dissipation safe-operating condition, as a function of ambient temperature. This means that SiC FETS with lower gate charge can be driven to the higher end of the PWM frequency range, subject to package power dissipation. However, if the maximum gate charge capability is used, the PWM maximum frequency must be limited to ensure it remains within the thermal capability of the package.

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APPLICATIONS INFORMATION

Typical Application

A typical application schematic for the driver chipset is shown in the Typical Application section. On the low-voltage primary side, the driver is supplied with a single bias supply voltage, V_{DRV}. On the isolated secondary side, an external bias supply is not required—only decoupling capacitors are required.

Details of the various pins and features of the AHV85003 and AHV850043 gate-driver chipset are provided in the sections that follow. For additional design and layout guidelines, refer to the AHV85003 and AHV85043 Chipset PCB Layout Guide. [2]

Bootstrap and Charge-Pump Capacitors

Generation of the floating bias rails for the internal power stage requires two external bootstrap decoupling capacitors, CBSP and CBSN, for the AHV85003, as shown in the Typical Application section. These capacitors are connected between BSP/TXPP, and BSN/TXPN. For the AHV85043, generation of a floating bias rail requires an external charge-pump decoupling capacitor, CCHP.

Fault Output

The AHV85003 active-low open-drain $\overline{\text{FAULT}}$ pin requires an external pull-up resistor to a suitable rail. This can be any suitable 3.3 V or 5 V rail, or the pin can also be pulled up to the VDRV pin. The recommended value of the pull-up resistor ranges from 15 kΩ to 100 kΩ for < 1 mA sink current. Sinking excessive current on the $\overline{\text{FAULT}}$ pin could result in a low level at the $\overline{\text{FAULT}}$ pin during pull-down. This low level exceeds the logic-low V_{IH} at the system controller input. The fault output allows wired-OR connection to multiple drivers.

Enable Input

The EN pin includes an internal 300 kΩ pull-down, and an internal deglitch filter to minimize false toggling due to noise pick-up. The addition of a low-pass filter, as shown in the Typical Application section, is also recommended, particularly in noisy environments.

The EN pin is rated up to the V_{DRV} maximum, so it can be tied high to any system 5 V or 3.3 V logic rail, or V_{DRV}.

PWM Inputs and Interlock Function

The PWM input pins have a 150 kΩ pull-down (IN+) to GND and a 150 kΩ pull-up (IN–) to the internal 3.3 V bias voltage, to prevent the inputs from floating if they are left open.

If a single PWM input is used in the application, the unused input must be tied high (IN+) or low (IN–).

The two PWM input pins of the AHV85003 can also be used to provide interlock between the two series switches in a half-bridge leg. This configuration can be used to prevent a shoot-through event on the half-bridge leg, which can otherwise be caused by simultaneous or overlapping turn-on commands for the low-side and high-side switches.

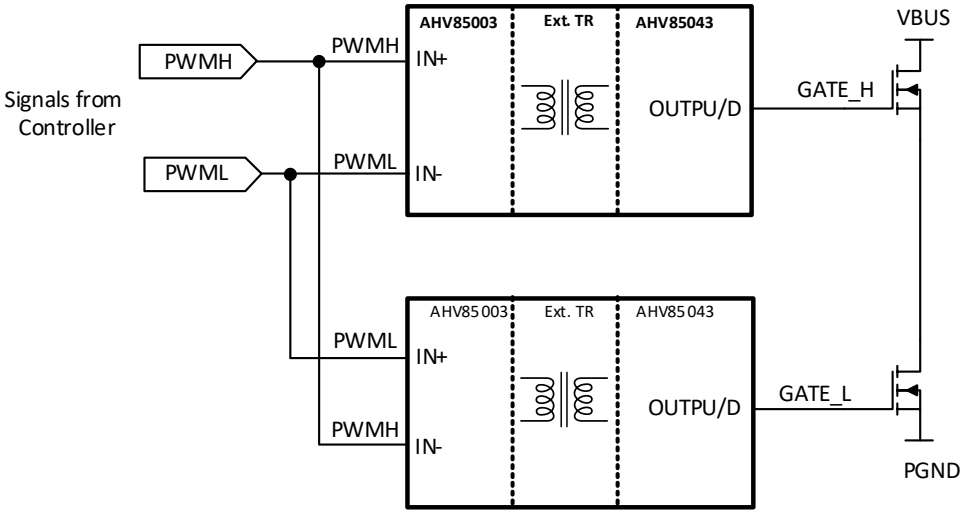

Figure 8: Interlock Connection of PWML and PWMH to IN+ and IN– In Half-Bridge Leg for Shoot-Through Protection, AHV85003 and AHV85043 Chipset with Recommended External Transformer

[2] https://www.allegromicro.com/-/media/files/application-notes/an296376-ahv85003-and-ahv85043-chipset-qfn-pcb-layout-guidelines

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To attain the interlock function:

- For the low-side switch, connect IN+ to the low-side PWML signal, and connect IN– to the corresponding high-side PWMH signal for the same leg, as shown in Figure 9.
- For the high-side switch in the same leg, connect the PWM signals similarly to the low-side switch connections, with IN+ connect to PWMH and IN– connect to PWML.

Example waveforms for the dead time generated at the SOURCE pin by the PWM controller are shown in Figure 9, and example waveforms for the dead time control by use of deliberate PWM overlap is shown in Figure 10.

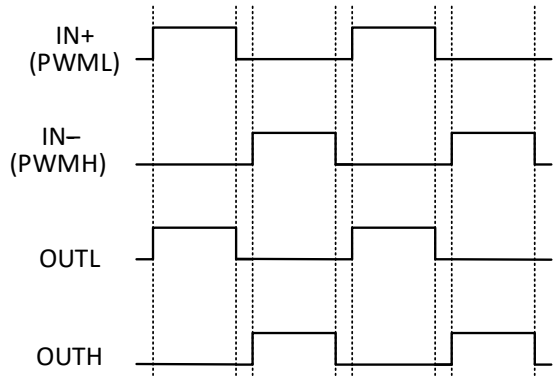

Figure 9: Half-Bridge PWML and PWMH Signals with Dead Time Generated at SOURSE by PWM Controller, AHV85003 and AHV85043 Chipset with Recommended External Transformer

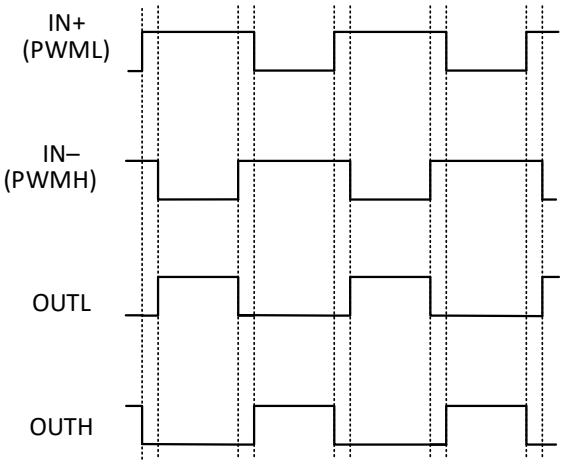

Figure 10: Half-Bridge PWML and PWMH Signals with Deliberate Overlap—Dead-Time Generated by Interlock Connection, AHV85003 and AHV85043 Chipset with Recommended External Transformer

If required, additional dead time between the low-side and high-side switches in a half-bridge leg can be implemented by placing a small external resistor-capacitor (RC) filter on the IN+ and/or IN– pins.

Example waveforms for the generation of PWMH as the inverse of PWML (or vice versa), with virtually no dead-time, are shown in In Figure 11. By adding a small RC delay at the driver IN– pin (or IN+ pin), and using the interlock connection between the low-side and high-side half-bridge drivers, a dead time is introduced by virtue of the short overlap between the IN+ and IN– inputs, which ensures protection against cross conduction.

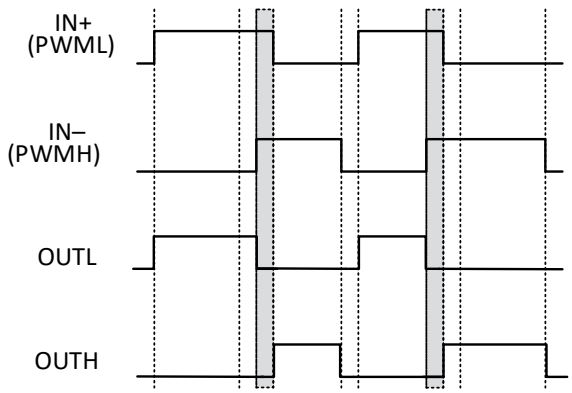

Figure 11: Half-Bridge PWML and PWMH Signals with Erroneous Overlap—Shoot-Through Prevented by Interlock Connection, AHV85003 and AHV85043 Chipset with Recommended External Transformer

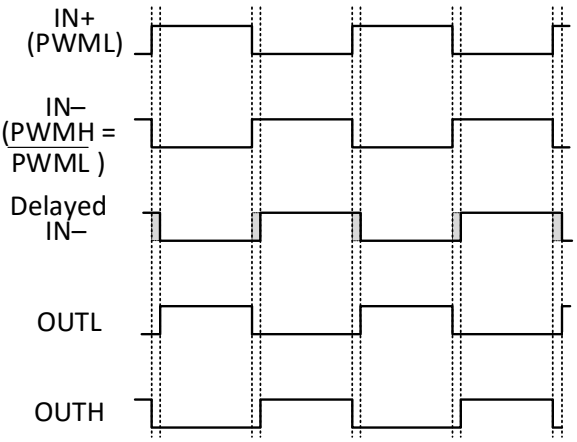

Figure 12: Half-Bridge PWML and PWMH (Derived from Inverted PWML) Signals with Small RC Delay Applied to IN–, Interlock Connection Introduces Dead-Time for Shoot-Through Prevention, AHV85003 and AHV85043 Chipset with Recommended External Transformer

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Secondary Negative Bias Rails

The negative bias rail V_{SECN} can be adjusted by a pair of external resistor dividers, R_{nt} and R_{nb}, on the VFBN pin. The values of the external resistor dividers should be selected using the ratios in Equation 2 or the values in Table 4 to set the commonly used negative voltage levels from 0 V to –5 V.

Equation 2:

$$V_{SECN} = V_{FBN}\left[1 + \frac{R_{nt}}{R_{nb}}\right]$$

or

$$R_{nt} = R_{nb}\left[\frac{V_{SECN}}{V_{FBN}} - 1\right]$$

Table 4: AHV85043 Recommended VSECN Divider Resistor Values [1]

VSECN	R_{nt} (kΩ)	R_{nb} (kΩ)
–5	40.2	10
–4	30.1	10
–3	20	10
–2	10	10
–1	0	10
0	0	0

[1] Continuous total secondary voltage ($V_{SECP} – V_{SECN}$) must not exceed 21 V

To minimize the effect of pollutants on the divider network. The maximum recommended resistor value for the resistor divider is 47 kΩ,

For the special case where a negative gate-drive rail is not required (V_{SECN} = 0 V), the value of each divider resistor should be 0 Ω, to short together the nets SOURCE-VFBN-VSECN, to disable the internal VSECN regulator. Alternatively, the SOURCE, VFBN, and VSECN pins can be shorted together to disable the regulator and achieve a zero-negative-gate-drive rail.

The addition of three decoupling capacitors is recommended as shown in Figure 13, where: capacitor CVSN is connected between V_{SECP} and V_{SECN}; capacitor CVSP is connected between V_{SECP} and SOURCE; and capacitor CVSNS is connected between V_{SECN} and SOURCE. The maximum recommended value for each capacitor is 1 µF.

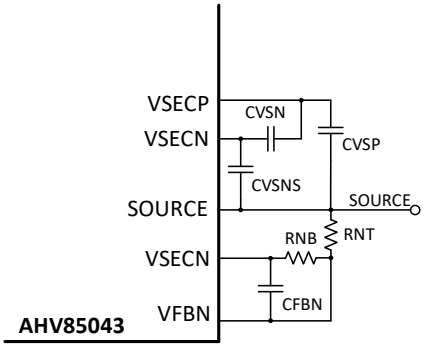

Figure 13: External Resistor Divider Connection for V_{SECN} Regulation Level

Secondary-Side Snubbers

The application diagram in the Typical Application Schematic section shows two snubbers connected between TXSP/VSECN and TXSN/VSECN. The snubbers are required to achieve a higher common-mode transient immunity (CMTI). The values of CSNN/RSNN and CSNP/RSNP are dependent on the desired CMTI level and on the interwinding capacitance of the pulse transformer. In the transformer selection, a transformer with low interwinding capacitance should be selected to obtain high immunity to common-mode transients. For snubber-value calculations, refer to the Allegro application note AHV85003 and AHV85043 Chipset Secondary-Side Snubbers for Improved CMTI Performance (AN296377). [3]

Transformer Selection

The AHV85003 and AHV85043 chipset requires the use of a pulse transformer for the transfer of PWM data and power between the primary and secondary sides. The transformer isolation rating should be determined by the user based on system requirements. For key parameters of the transformer, qualification method, and recommended commercially available transformers, refer to the Allegro application note AHV85003 and AHV85043 Chipset External Transformer Design Guidelines (AN296372). [1]

[3] https://www.allegromicro.com/-/media/files/application-notes/an296377-ahv85003-and-ahv85043-secondary-side-snubbers-for-improved-cmti-performance

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TYPICAL APPLICATION SCHEMATIC

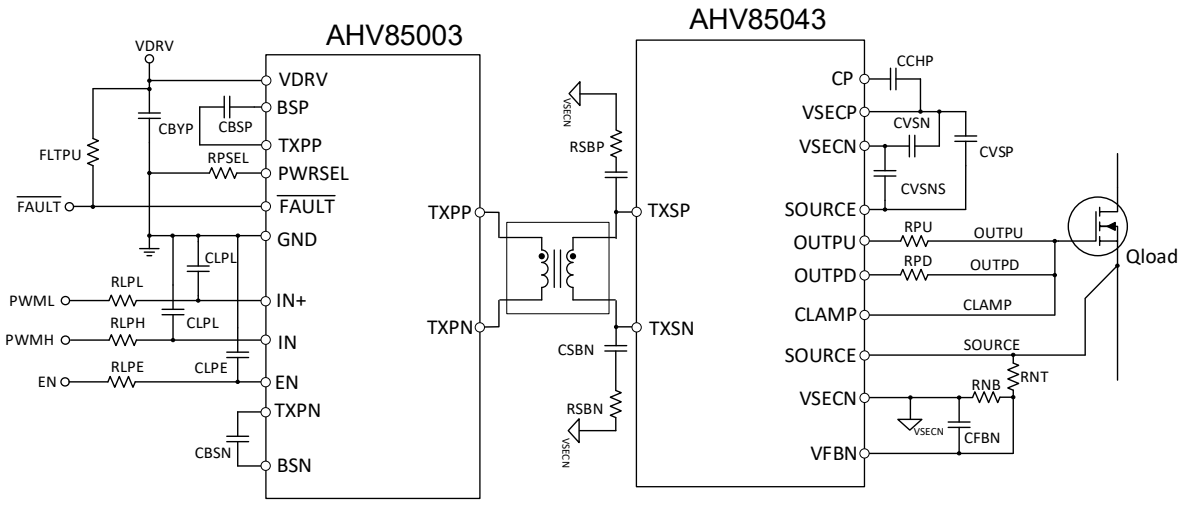

Figure 14: Typical Application Schematic, AHV85003 and AHV85043 Chipset with External Transformer

Designator	Value	Notes
CBSP	22 nF, 25 V, X7R	Boostrap capacitor
RPSEL	0 Ω	Power selection [1]
CBYP [2]	1 µF, 25 V, X7R	Bypass capacitors × 3
FLTPU	100 kΩ	FAULTb pin pull-up
CLPL	100 pF	IN– input filter
RLPL	49.9 Ω	IN– input filter
CLPH	100 pF	IN+ input filter
RLPH	49.9 Ω	IN+ input filter
CLPE	100 pF	Enable (EN) input filter
RLPE	49.9 Ω	Enable (EN) input filter
CSBN	See note [4]	Snubber (negative)
CSBP	See note [4]	Snubber (positive)
CBSN	22 nF, 25 V, X7R	Bootstrap capacitor

Designator	Value	Notes
CCHP	22 nF, 25 V, X7R	Charge-pump capacitor
CVSN	470 nF, 25 V, X7R	
CVSP	470 nF, 25 V, X7R	
CVSNS	470 nF, 25 V, X7R	
RPU	See note [3]	
RPD	See note [3]	
RNT	See note [4]	Secondary negative rail voltage setting
RNB	See note [4]	Secondary negative rail voltage setting
CFBN	22 pF, 25 V, X7R	
RSBN	See note [5]	Snubber (negative)
RSBP	See note [5]	Snubber (positive)

[1] Power selection; to select the three power transfer options, this pin should be tied directly to VDRV or GND, or it should remain floating. Refer to the relevant section.
[2] One bypass capacitor should be used at each VDRV pin, placed as close as practicable to the device.
[3] Gate resistors; the value of these resistors is dependent on the system design and should be rated for surge currents.
[4] The ratio of R_{nt} to R_{nb} sets the level of the secondary-side negative rail (VSECN).
[5] The snubbers on the secondary side of the pulse transformer improve the CMTI performance. To dimension the snubber capacitor and resistor, refer to the relevant application note.
[6] For PCB layout and design guidelines, refer to the Allegro AHV85003 and AHV85043 Chipset PCB Layout Guide.

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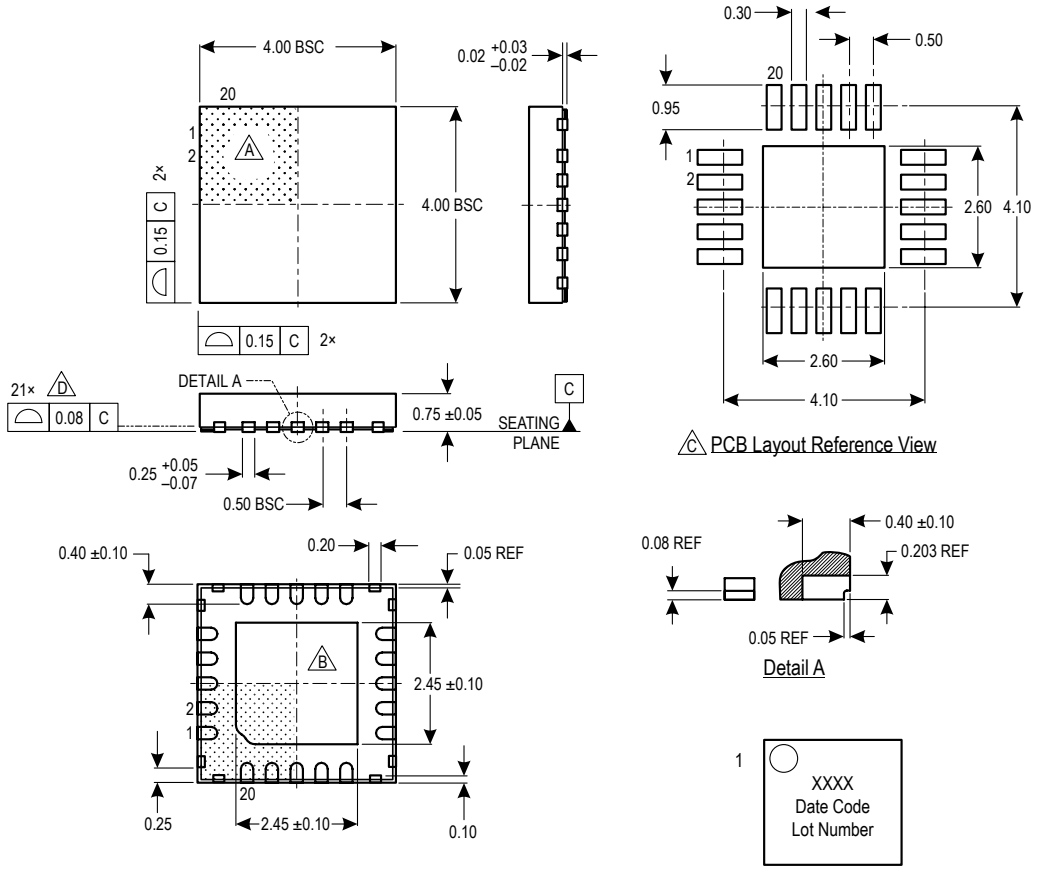
PACKAGE OUTLINE DRAWING

The AHV85003 and AHV85043 IC packages are each provided in a 4 mm × 4 mm-footprint, 20-pin QFN package (Allegro suffix -ES). For additional information, refer to the packaging design support on the Allegro web site. [4]

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Lines 1, 2, 3 = 6 characters

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 15: 20-Pin QFN Package (Suffix -ES)

[4] https://www.allegromicro.com/en/design-support/packaging

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REVISION HISTORY

Number	Date	Description
–	December 2, 2025	Initial release

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