48 V Sensorless Code-Free FOC BLDC Motor Controller

FEATURES AND BENEFITS

- 90 V maximum rating with integrated buck regulator for high efficiency
- Fully integrated single-shunt sensorless FOC controller (code-free)
- Speed, torque, and power mode operation
- Power-loss brake functionality
- Universal speed curve
- Fault mode brake
- Analog/PWM/Clock mode speed control
- Precision speed control
- Configurable RD or FG output
- Slew-rate control for electromagnetic-interference (EMI) mitigation
- Proprietary nonreverse fast startup
- Ultra-quiet low-speed operation
- Current-control soft start
- Windmill startup operation
- No V_{BB} boost on powerup with spinning motor
- I^2C serial port
- Power limit protection
- Configurable current and power limit
- Lock detection
- Overcurrent limit (OCL)
- Overvoltage protection (OVP)
- Short-circuit protection (OCP)
- Logic input compatible with 3.3 V and 5 V

DESCRIPTION

The A89333 is a three-phase, sensorless, brushless DC (BLDC) motor controller. A field-oriented control (FOC) algorithm is fully integrated to achieve the best efficiency and acoustic noise performance. The device also optimizes motor-startup performance in stationary, forward, and reverse windmill conditions.

Programmable profiles and closed-loop controls are included for constant power and constant speed operations. This eliminates the requirement for a microprocessor-based system and minimizes programming requirements.

A simple inter-integrated circuit (I^2C) interface is provided for setting motor-related parameters, control-related parameters, and startup profiles, which are stored in nonvolatile memory (NVM). The I^2C interface can also be used to control the motor directly and to provide speed and status feedback. Password protection is available for stored NVM data.

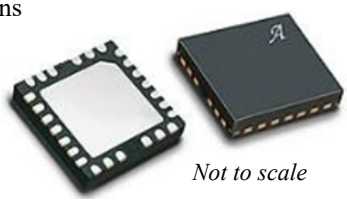
The A89333 is available in a 28-contact 4 mm × 4 mm quad-flat no-leads (QFN) package with exposed thermal pad (suffix EC).

APPLICATIONS

- 48 V server fans
- Telecommunications (telecom) fans
- Home appliance fans

PACKAGE

28-Contact QFN
with exposed pad
(EC package)



Not to scale

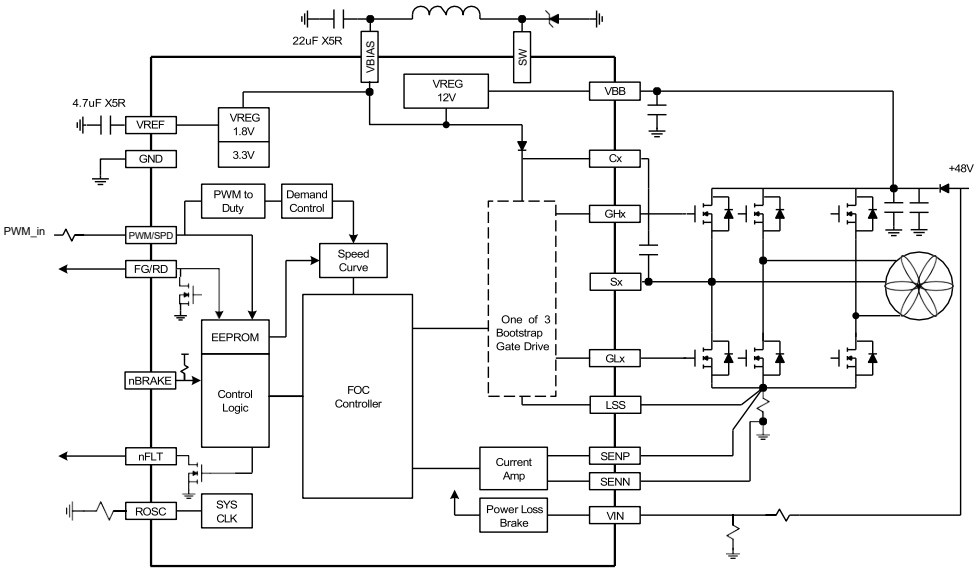


Figure 1: Typical Application

TABLE OF CONTENTS

Specifications 3
Pinout Diagram and Terminal List Table 4
Pin Descriptions 8
VBB 8
VIN 8
VREF 8
VBIAS 8
SW 8
FG/RD 8
PWM/SPD 8
ROSC 8
Sx 8
Cx 8
GHx 8
GLx 8
LSS 8
SENN 8
SENP 8
nBRAKE 8
nFLT 9
Functional Description 10
Powerup and Initialization 10
External Command Source 11
Analog Input Voltage (EXT_CMD_SRC, 0x1). 11
Frequency Mode (EXT_CMD_SRC, 0x3) 12
I²C Mode (EXT_CMD_SRC, 0x0) 12
Universal Curve Controller: UCC 13
Motor Rotation Direction 14
Speed, Torque, or Power Control Modes 15
Speed Mode (0x0) 15
Torque Mode (0x2) 15
Power Mode (0x1) 15
Maximum System Speed 15
Maximum System Current and Bus Current Sensing 15
DC-Link Voltage 16
Maximum Electrical Power 16
Speed Limit 16
Power Limit 16
Current Limit 16
Motor Control Application (MCA) Finite State Machine (FSM) 16
Standby—SBY 17
Windmilling—WNDML 17
IPD and Align 18
Ramp-Up—RAMPUP 18
Drive—DRIVE 19
Regenerative Mode 19
Brake—BRAKE 19
FOC Algorithm Speed and Current Loop 19
Observer 20
Diagnostic and Protection Features 21
VBB Undervoltage—VBB UVS 21
VBB, UV, and NVM Reprogramming 21
OverTemperature Protection—OVT/TSD 21
VBB Overvoltage Protection—VBB OVP 22
Overcurrent Protection—OCP (Short Protection) 22
Loss of Sync (Lock/Stall Detection) 22
No-Motor Start 23
VBB Overvoltage Variable Limiter 23
Overcurrent Limit 23
Maximum Power Limit 23
Application Features 24
EEPROM NVM for Storing Motor Control and Configuration Data 24
FG/RD Pin 24
FG 24
RD 24
FG in VBB UV Condition 24
Dead Time Configuration 25
Slew Rate Control 25
Buck Converter 25
Advanced Features 26
Soft-Off Deceleration 26
Soft Start 26
Quiet Start 26
Forced OL 26
VIN and Power-Loss Brake 27
No-Power Brake 28
AC Loss Function 28
Registers and Nonvolatile Memory (NVM) Map 29
User Registers 39
SW Status Register, SW_STATUS 40
I²C Command Register, REF_CMD 41
SW Fixed-Address Variables 42
FOC Internal Variables 43
Programming the EEPROM 44
I²C Serial Interface 44
I²C Timing Diagrams 44
Read Procedure 44
Write Procedure 45
Operation Modes and Customer Password Protection 46
Application Information 47
Layout Notes 48
Pin Diagram 49
Package Outline Drawing 50

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPECIFICATIONS

SELECTION GUIDE

Part Number	Package	Packing
A89333GECSR	28-lead 4 mm × 4 mm QFN with exposed thermal pad	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS [1][2]

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{BB}	V_{BB} = 90 V	–0.3 to 90	V
Power Loss Brake Terminal	V_I	V_{IN}	–0.3 to 90	V
Speed Control Terminal	V_I	PWM/SPD	–0.3 to 90	V
Logic Input Terminal	V_I	nBRAKE	–0.3 to 6	V
Logic Bidirectional Terminal	V_{IO}	FG/RD	–0.3 to 90	V
Logic Output Terminal	V_O	nFLT	–0.3 to 6	V
Buck Switch Terminal	V_{SW}		–1 to 90	V
		t_W < 0.5 µs	–4 to 90	V
Bootstrap Supply Terminals	V_{CX}	CA, CB, CC	–0.3 to V_{BIAS} + 90	V
Motor-Phase Terminals	V_{SX}	SA, SB, SC	V_{CX} – 4 to V_{CX} + 0.3	V
High-Side Gate Drive Output Terminals	V_{GHX}	GHA, GHB, GHC	V_{SX} – 0.3 to V_{CX} + 0.3	V
Low-Side Gate Drive Output Terminals	V_{GLX}	GLA, GLB, GLC	V_{LSS} – 0.3 to V_{BIAS} + 0.3	V
Input Terminal	V_I	ROSC	–0.3 to 6	V
Output Terminal	V_o	VBIAS	–0.3 to 15	V
Output Terminal	V_O	VREF	–0.3 to 3.4	V
Input Terminal	V_I	SENP, SENN	–4 to 6	V
Bridge Low-Side Source Terminals	V_{LSS}		–500 to 500	mV
		t_w < 200 ns	–4 to 6	V
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_s		–55 to 150	°C

[1] With respect to GND, unless otherwise noted. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in terminal names and symbols indicates a variable sequence character.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information.

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	28-contact QFN (package EC), on 2-sided PCB with 1 in^2 copper	45	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

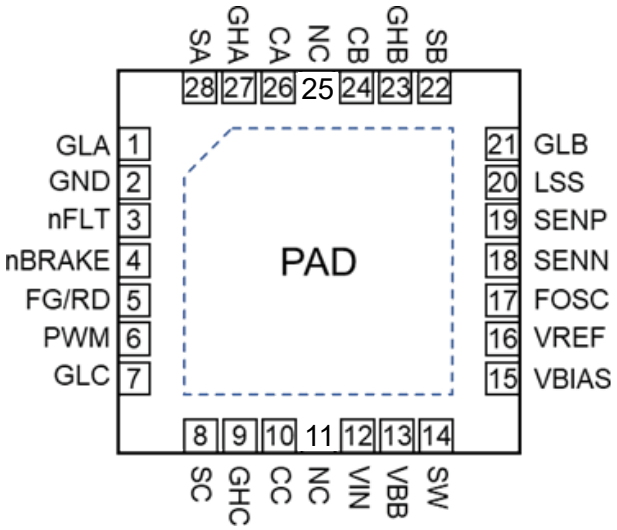
[1] Additional thermal information is available on the Allegro website.

RECOMMENDED OPERATIONAL RANGE

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	V_{BB}	DC	7	48	75	V
Logic Voltage Range	V_I	nBRAKE	–0.3	–	5.5	V
Operating Temperature Range	T_a		–40	–	105	°C

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST TABLE



EC Package (Top View)

Terminal List Table

Number	Name	Function
1	GLA	Gate drive output
2	GND	Ground
3	nFLT	Logic output
4	nBRAKE	Logic input
5	FG/RD	Logic output; also used as SDA for I²C
6	PWM/SPD	Logic input; also used as SCK for I²C
7	GLC	Gate drive output
8	SC	Motor output
9	GHC	Gate drive output
10	CC	$C_{BOOTSTRAP}$
11	NC	No connection
12	VIN	Analog input
13	VBB	Power supply input
14	SW	Switch node

Number	Name	Function
15	VBIAS	Voltage regulator output
16	VREF	Logic supply output
17	ROSC	Analog input
18	SENN	Current sense negative terminal
19	SENP	Current sense positive terminal
20	LSS	Low-side source
21	GLB	Gate drive output
22	SB	Motor output
23	GHB	Gate drive output
24	CB	$C_{BOOTSTRAP}$
25	NC	No connection
26	CA	$C_{BOOTSTRAP}$
27	GHA	Gate drive output
28	SA	Motor output

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS [1]**:** Valid at T_J = 25°C, V_{BB} = 48 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	V_{BB}	V_{BB} = 90 V	7 [2]	48	90	V
VBB Supply Current	I_{BB1}	Standby, $V_{IN} > V_{INTH}$, $V_{BB} > V_{BBUVLO}$	–	6	–	mA
	I_{BB2}	$V_{IN} < V_{INTH}$	–	0.8	3.3	mA
VBIAS Output Voltage	V_{BIAS}	V_{BB} > 13 V, I_{EXT_LOAD} < 10 mA	10	12.5	14	V
VREF	V_{REF}	I_{EXT_LOAD} < 5mA	1.7	1.8	1.9	V
VREF Current Limit	V_{REFOCL}	V_{REF} = 0 V, internal current limit	70	92	135	mA
GATE DRIVER						
High-Side Gate Drive Output	V_{GH}	V_{BB} = 48 V, DC	9.3	11.8	13.3	V
Low-Side Gate Drive Output	V_{GL}	V_{BB} = 48 V, DC	10	12.5	14	V
Gate Drive Source Current	I_{SRC}	PWMGDSLEWRATE = 0, DC, V_{GS_TH} = 3 V	7	8.5	10	mA
		PWMGDSLEWRATE = 1, DC, V_{GS_TH} = 3 V	19	25.5	32	mA
		PWMGDSLEWRATE = 2, DC, V_{GS_TH} = 3 V	31	42	53	mA
		PWMGDSLEWRATE = 3, DC, V_{GS_TH} = 3 V	48	63	78	mA
Gate Drive Sink Current	I_{SNK}	PWMGDSLEWRATE = 0, DC, V_{GS_TH} = 3 V	16	23	30	mA
		PWMGDSLEWRATE = 1, DC, V_{GS_TH} = 3 V	33	46	60	mA
		PWMGDSLEWRATE = 2, DC, V_{GS_TH} = 3 V	50	68	87	mA
		PWMGDSLEWRATE = 3, DC, V_{GS_TH} = 3 V	50	68	87	mA
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0, $V_{GHx} - V_{Sx}$ < 0.1 V	0.5	–	2	MΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0, $V_{GLx} - V_{LSS}$ < 0.1 V	0.5	–	2	MΩ
PROTECTION CIRCUITS						
Lock Protection	t_{OFF}	Relative to programmed target, ROTSTARTRETRYTOUT	–10	–	10	%
Overcurrent Limit	I_{OCL}	Relative to programmed target, SFOCDRVCURRLMT	–15	–	15	%
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing	145	160	175	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
VREF UVLO	$V_{REFUVLO}$	V_{BIAS} rising	1.35	1.45	1.55	V
VBB Overvoltage	V_{BBOVTH}	Relative to programmed target, OVP_TH	–3	–	3	%
VBB UVLO	V_{BBUVLO}	V_{BB} rising, UVSTH = 0	29	30	32	V
		V_{BB} rising, UVSTH = 1	23	24	25	V
		V_{BB} rising, UVSTH = 2	6.2	6.7	7.5	V

[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.
[2] When V_{BB} < 13 V, gate drive output voltage tracks V_{BB} voltage.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (cont.) [1]**:** Valid at T_J = 25°C, V_{BB} = 48 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
POWER LOSS BRAKE						
V_{IN} Logic Threshold	V_{INTH}	V_{IN} falling	–	2.7	–	V
Hysteresis	V_{INHYS}		–	500	–	mV
V_{IN} Pull-Down Resistor	V_{INPD}		–	870	–	kΩ
V_{BB} Regulated Boost Voltage	V_{BOOST}	$V_{IN} < V_{INTH}$	7.4	8.1	8.9	V
V_{BB} Boost Low Threshold	V_{BBTH}		–	1.1	–	V
Boost Switching Frequency	f_{BOOST}		–	40	–	kHz
LOGIC INPUTS AND OUTPUTS						
Logic Input Low Level	V_{IL}	nBRAKE	0	–	0.8	V
Logic Input High Level	V_{IH}	nBRAKE	2	–	6	V
Logic Input Hysteresis	V_{HYS}	nBRAKE	200	300	600	mV
Logic Input Current	I_{IN}	SPD, nBRAKE	–10	< 1	15	µA
Output Saturation Voltage (FG/RD, nFLT)	V_{SAT}	I = 1 mA	–	–	0.3	V
Output Leakage (FG/RD)	I_O	V = 12 V, switch OFF	–	–	5	µA
Output Leakage (nFLT)	I_O	V = 6 V, switch OFF	–	–	10	µA
INTERNAL OPEN-DRAIN PULL-UP						
Internal Pull-Up Voltage		nFLT, nBRAKE	4.25	5	5.75	V
		PWM/SPD	3.75	4	4.25	V
Internal Pull-Up Resistor		PWM/SPD, nFLT, nBRAKE	60	100	140	kΩ
I²C TIMING						
SCL Clock Frequency	f_{CLK}		10	–	400	kHz
Bus Free Time Between Stop/ Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	ms

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (cont.) [1]**:** Valid at T_J = 25°C, V_{BB} = 48 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
SPEED CONTROL						
PWM Duty Input, for PWM Duty Control Mode	f_{PWM}		0.1	–	100	kHz
Duty Cycle On Threshold	DC_{ON}	Relative to programmed target	–0.5	–	0.5	%
Duty Cycle Off Threshold	DC_{OFF}	Relative to programmed target	–0.5	–	0.5	%
Analog SPD Full-Range Voltage, for Analog External Command Source (Analog Control Mode)	$AnaSpd_{MAX}$	I_{LOAD} = 10 µA	0	–	3.6	V
Analog SPD Resolution			–	1	–	mV
Input Clock Frequency Range (Clock Mode)		Relative to programmed target, CLKCOMPREF	0.1	–	1	kHz
Speed Setpoint (Digital, Not Clock Mode)	F_{SPD}	R_{OSC} = 25 kΩ (0.1%)	–2.5	–	2.5	%
Speed Setpoint (Digital, Clock Mode)	F_{SPDClk}	PWM input frequency = CLKCOMPREF ±0.05%	–0.1	–	0.1	%
System Oscillator	f_{OSC}	R_{OSC} = 25 kΩ (0.1%)	24.5	25	25.5	MHz
ID CLOCK TIMING						
Maximum ID Clock Time	t_{idmax}	Relative to programmed target, FGIDDUR	–10%	–	10%	s
ID Clock Frequency	f_{idclk}	Relative to programmed target, FGIDFREQ	–5%	–	5%	Hz
V_{BB} UVLO to ID Clock Delay	t_{dly1}	Relative to programmed target, FGIDFREQ	–	–	5%	s
PWM Rising Edge to End of ID Clock	t_{dly2}	Relative to programmed target, FGIDFREQ	–	–	5%	s
NONVOLATILE MEMORY (NVM) PROGRAMMING						
Minimum V_{BB} for Programming	V_{NVM_Prog}	V_{BB}	25	–	–	V

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PIN DESCRIPTIONS

VBB

Main power supply for internal regulators. Tie the VBB pin to the GND pin using a low-equivalent series resistor (ESR) ceramic bypass capacitor of 0.1 µF. This capacitor should be situated as close as possible to the VBB pin with a thick trace.

VIN

The VIN input is used to sense the supply voltage for the power-loss braking (PLB) function. The PLB function becomes active if the voltage on this input reduces to less than V_{INTH}. VIN must be connected to the power supply on the anode side of the blocking diode shown in Figure 1.

VREF

Voltage reference (1.8 V) to power internal digital logic. A low-ESR ceramic capacitor with 4.7 µF or greater is required on the pin to stabilize the supply. This regulator can supply up to 5 mA externally.

VBIAS

Internal buck regulator output. Connected to external inductor and output capacitor. VBIAS provides supply current for gate drive, digital logic, bootstrap capacitors, and low-voltage analog circuitry. Up to 10 mA can be externally sourced from the VBIAS pin.

SW

Buck regulator switching node connected to inductor and rectifier diode.

FG/RD

FG/RD is an open-drain output that can be pulled up to VBB externally. The selection of function is programmed via NVM parameters as well to provide either speed (FG) or rotation detection (RD) data. For more information, refer to the FG/RD Pin section.

The FG/RD pin is also used as a serial data (SDA) port in the I²C mode.

The I²C command can pass only when this pin is high (open drain).

PWM/SPD

Device control demand input. Supports analog, PWM, or frequency command.

It also has, by default, an internal pullup to 4 V that can be disabled through IPUP_PWMSPD_DIS NVM parameter. The PWM/SPD pin is also used as SCK in the I²C mode.

ROSC

The ROSC terminal is used to improve the accuracy of the internal system clock for better accuracy control of motor speed. To use this feature, connection of a 0.1% 25 kΩ resistor between the ROSC terminal and GND is recommended. A 1% resistor can be used for applications where speed control accuracy is not critical.

Sx

Load phase connections. These terminals are the negative supply connections for the floating high-side drivers and are also connected to the negative side of the bootstrap capacitors.

Cx

High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHx

High-side, gate-drive outputs for external N-channel MOSFETs.

GLx

Low-side, gate-drive outputs for external N-channel MOSFETs.

LSS

Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs through a low-impedance track.

SENN

Current sense negative terminal.

SENP

Current sense positive terminal.

nBRAKE

This is the active low-input signal. It turns on all low sides for the braking function. The brake function overrides input control. Brake input is ignored during a thermal shutdown (TSD) event or if ($V_{BB} > V_{OVP_TH}$) or ($V_{BB} < V_{BBUVLO}$). Care should be taken to avoid stressing the MOSFET when braking while the motor is running. When braking, the current is limited only by V_{BEMF}/R_{MOTOR}. The A89333 includes an optional feature that delays

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

braking until the motor speed reduces to a level that is sufficiently low (configurable BRAKE_FREQ_TOO_HIGH_TH parameter in NVM) that the braking current does not damage the MOSFET.

The nBRAKE pin also has, by default, an internal pull-up to 5 V that can be disabled through the IPUP_NBRAKE_DIS parameter in NVM.

nFLT

This open-drain output provides the fault status of the motor operation.

This pin is internally pulled up to 5 V by default. Pull-up can be disabled through NVM. The default is high when there is no fault. When a fault is detected, the nFLT pin transitions to low and remains active (low) until the fault is cleared according to the latched or not-latched mechanism.

The nFLT fault reporting function is enabled by default, but it can be disabled by selecting NFLT_DIS = 1 in the NVM.

The nFLT feature can be used to indicate a successful software startup after POR by being low for a short period of time as detailed in Figure 2.

This feature can be enabled/disabled in the CONFIG register of the NVM using NFLT_STARTUP_DIS.

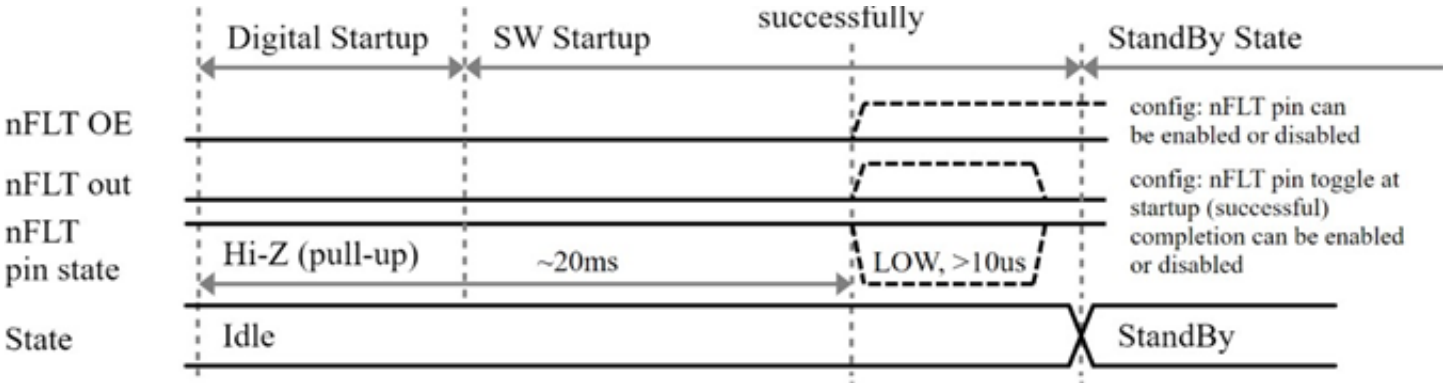


Figure 2: nFLT Pin at Startup

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

The A89333 integrates a sensorless FOC algorithm using single-shunt resistance. The FOC algorithm implements a feedback current loop to control the current during dynamic load conditions, guaranteeing minimum torque ripple and maximum efficiency. The integrated buck converter allows it to operate from maximum V_{BB} with high efficiency and better thermal performance. The A89333 requires minimal external components thanks to the use of the single-shunt technique for current sensing and its advanced algorithm to reconstruct the current of each phase.

Allegro proprietary algorithms have been used to achieve high efficiency, fast start-up, and high dynamic response, minimizing acoustic noise in an easy-to use device.

The A89333 can be controlled through PWM, analog, or I²C, depending on the application, with an easy interface to the most common microcontroller.

The motor can be controlled in speed, torque, or power mode, with the FOC algorithm maintaining regulation in the presence of load and supply voltage change.

The A89333 integrates advanced diagnostics to detect the internal/external power stage and motor faults. Faults are reported through a dedicated fault pin and the detailed diagnostic status of faults are available through the I²C register.

An internal nonvolatile memory (NVM) allows configuration of the motor parameters and the FOC algorithm. The basic FOC control algorithm of A89333 is shown in Figure 3.

Powerup and Initialization

Upon power-up, the A89333 waits for the internal regulators to reach their UVLO levels, then loads the configuration data from the NVM into the internal registers. After the configuration is loaded, the A89333 is in the standby mode and is ready to respond to user input through the PWM/SPD pin or the I²C port, according to the external command source selected. (For more information, refer to the External Command Source section.)

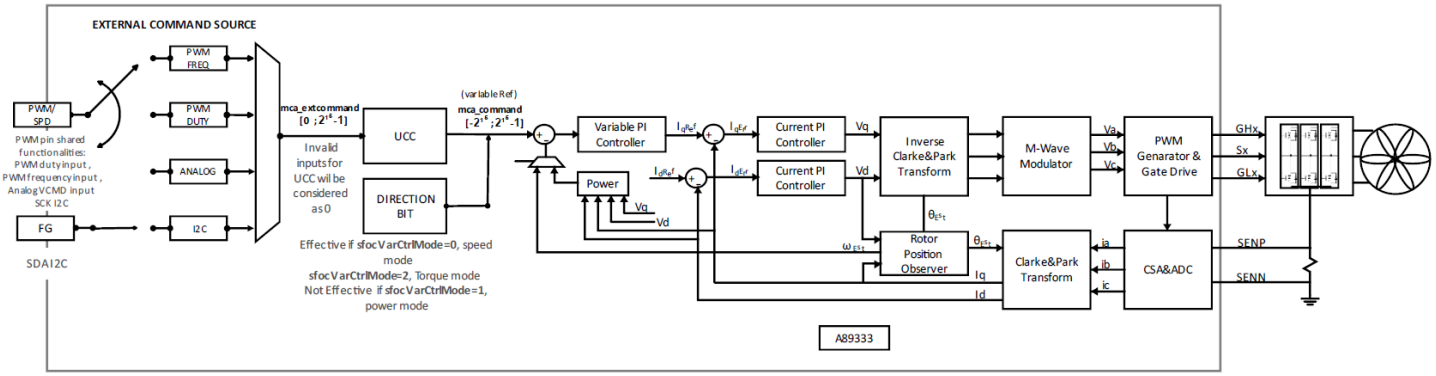


Figure 3: External Command Source and FOC Algorithm

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

External Command Source

The A89333 can be controlled with five different sources of command according to the EXT_CMD_SRC in the NVM register setting.

ANALOG INPUT VOLTAGE (EXT_CMD_SRC, 0X1).

Motor command is proportional to the analog voltage applied on the PWM/SPD pin.

Direction data, when available, is defined in the NVM and the UCC. For further information, refer to the Motor Rotation Direction section.

The analog command is converted into the digital domain and is rescaled according to:

Equation 1:

$$mca_{extcommand} = (2^{15} - 1) \times \frac{V_{PWM/SPD}}{AnaSpdMax},$$

where $AnaSpd_{Max}$ is a fixed voltage equal to 3.6 V. For example, see Table 1.

PWM DUTY CYCLE (EXT_CMD_SRC, 0X2)

Motor control is proportional to the duty cycle applied on the PWM/SPD pin. The frequency range of the input PWM is from 100 Hz to 100 kHz.

Direction data, when available, is defined in the NVM and the UCC. For further information, refer to the Motor Rotation Direction section.

The duty cycle command is converted into the digital domain according to:

Equation 2:

$$mca_{extcommand} = (2^{15} - 1) \times duty.$$

For example, see Table 2.

In this mode, it is possible to enable the clock mode feature to synchronize the internal clock with the external PWM signal frequency. This can provide higher speed accuracy and can eliminate the need for a precision external resistor on the ROSC terminal. The external PWM signal is used to compensate for the inaccuracy of the integrated oscillator, allowing speed accuracy to be achieved down to 0.1%. When this feature is activated (CLK_COMP_ENABLE), the input admissible frequencies of the external PWM signal are fixed and need to be specified in the CLK_COMP_REF register. To detect the frequency, the input duty cycle of the PWM signal must be greater than 0% and less than 99%. If a 0% or 100% duty cycle value is applied, the clock compensation is not applied. Speed accuracy is directly related to the accuracy of the PWM clock frequency to the selected CLK_COMP_REF frequency.

Table 1: Conversion from Analog Input Voltage to Digital Command

$duty_{PWM/SPD}$ (V)	$mca_{extcommand}$ (LSB) $AnaSpd_{Max}$ = 3.6 V
0.5	4551
2.5	22755
3.6	32767

Table 2: Conversion from PWM Input Duty to Digital Command

$duty_{PWM/SPD}$ (%)	$mca_{extcommand}$ (LSB)
25	8192
50	16384
75	24575

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FREQUENCY MODE (EXT_CMD_SRC, 0X3)

Motor control is proportional to the frequency applied on the PWM/SPD pin. The input frequency range needs to be between 44.5 and 2666 Hz (duty cycle is intended to be 50%, but this mode works with any setting other than 0 or 100%).

If PWM input frequency is greater than 2666 Hz, MCA_EX_COMMAND assumes the maximum value equal to 32767 [LSB]. If PWM input frequency is less than 44.5 Hz, MCA_EXT_COMMAND is equal to 0.

Direction data, when available, is defined in the NVM and the UCC. For further information, refer to the Motor Rotation Direction section.

The frequency command is converted into the digital domain according to:

Equation 3:

$$mca_{extcommand} = (pwm_{freq}[Hz] - 44.5) \times map_{coefficient},$$

where $map_{coefficient}$ is a scaling factor equal to 12.496. For example, see Table 3.

Table 3: Conversion from PWM Input Duty to Digital Command

$frequency_{PWM/SPD}$ (Hz)	$mca_{extcommand}$ (LSB)
44.5	0
100	(100 – 44.5) × 12.496 = 694
200	(200 – 44.5) × 12.496 = 1943
2666	(2666 – 44.5) × 12.496 = 32758

I²C MODE (EXT_CMD_SRC, 0X0)

The motor control speed reference command is defined by writing in the REF_CMD register through I²C protocol. The I²C clock, SCK, is mapped on the PWM/SPD pin, and I²C data is mapped on the FG pin. In this mode, the motor electrical frequency can be read through the register, as well as many other internal parameters.

The value selected in REF_CMD is copied into MCA_EXT_COMMAND. Direction data, when available, is defined in the NVM and UCC.

The A89333 can load a predefined command into the MCA_EXT_COMMAND register at power-up (POR) to start the motor without the need for an external command. The default command can be set in DEFAULT_EXT_CMD in the NVM and, at power-up, its value is copied into the MCA_EXT_COMMAND register. To disable this feature, DEFAULT_EXT_CMD must be set to 0.

The command is treated as speed, power, or torque, depending on the mode selected.

When FG is in the high state (not driven) or when the device has been configured in analog, PWM, or frequency external command source, I²C communication is always available.

I²C data is mapped on the FG pin and, because the pin is an open drain, it can be controlled by the I²C when in the high state. The internal NVM register, shadow NVM register, and status register can therefore be read and set during typical operation. However, for reliable communication, use of I²C is recommended when the A89333 is in the standby state (motor stopped).

NOTE 1: The internal NVM register and the shadow NVM register are inaccessible in application operation mode. They can be accessed only in user operation mode or in test operation mode. For more information, refer to the Operation Modes and Customer Password Protection section.

NOTE 2: The I²C SCK signal on the PWM/SPD pin is interpreted to be the maximum command. This is because, during serial transactions, the pin state is high, which is a valid command that is therefore interpreted as the maximum command.

For reliable communication, it is better to use serial communication in the UV mode to prevent issues related to motor start and proper FG/RD pin state.

For more information, refer to the VBB, UV, and NVM Reprogramming section.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Universal Curve Controller: UCC

The MCA_EXT_COMMAND motor command is passed through a universal curve controller to create an arbitrary command profile, then to the FOC algorithm. The input of the UCC is unsigned(MCA_EXT_COMMAND [LSB]) and the output is signed(MCA_EXT_COMMAND [LSB]), as shown in Figure 4.

The UCC is a transformer curve defined by corner points. Each point has a specific input value and corresponding output value. Values between points are calculated using linear interpolation. Up to 10 corner points can be defined in NVM (UCC_X0 to UCC_Y9). Corner points do not all require definition—only as many as are needed for the desired curve.

A closed-loop nonoperational region, defined by the PO_OPER parameter in the NVM, marked in the red hatched rectangular area in Figure 4, defines the minimum speed operation for reliable position-observer estimation and proper FOC functionality. Because operation in this area is not reliable, programming the UCC in this area is not recommended. The easiest way to prevent operation in this area is to use hysteresis, as shown in Figure 4.

Some examples of demand curves using screenshots taken from the GUI application follow.

Example 1: The default setting in which the output (Y axis) is same as the input (X axis) is shown in Figure 5. This curve can be used if the transformer is not needed.

Example 2: When the control loop is set to closed-loop speed, the example shown in Figure 6 can be used to avoid the resonant frequency of the motor, if needed.

Example 3: Hysteresis can be implemented by setting the input value of an address lower than the input value in the previous address. In this example shown in Figure 7, as the input demand rises, the output demand jumps to the next higher level at the vertical lines on the right of each transition. When the input demand falls, the output demand drops to the next lower level following the vertical lines on the left of each transition. This prevents output jitter when the input is around a boundary.

Example 4: In this example shown in Figure 8, the motor does not turn on until the input is approximately 23% and does not turn off until the output falls below about 20%. When the input is between about 90% to 96%, the output is at 10.6% (13002 rpm); when the input is greater than 96%, the motor stops.

Example 5: The curve can be used when bidirectional operation is required. In this case, when input is at 0%, the motor is at the selected maximum speed in the reverse direction; when the input is at 100%, the motor is at the maximum speed in the forward direction; and the motor is stopped when the input is approximately 50%. See Figure 9.

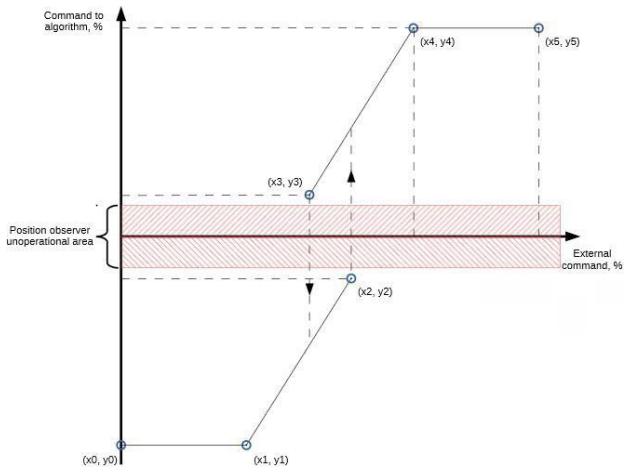


Figure 4: UCC Transfer Function from External Command to FOC Command

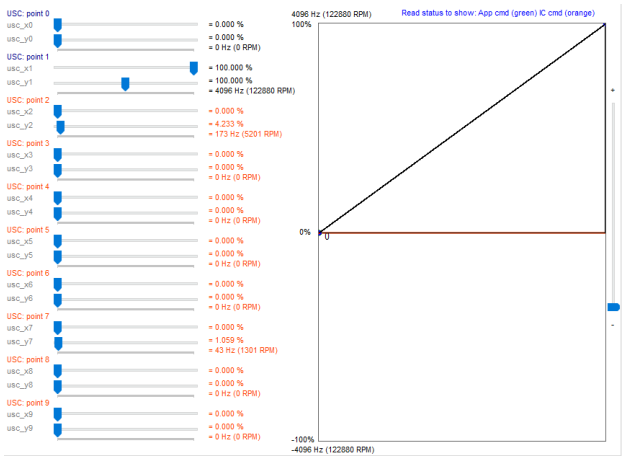


Figure 5: UCC Default Curve, Example 1

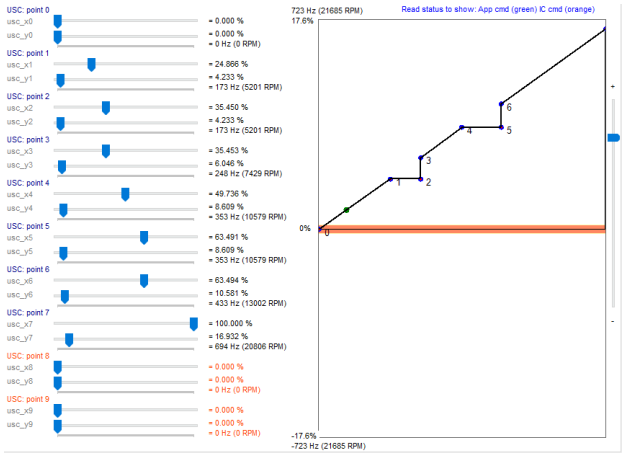


Figure 6: UCC Example 2

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

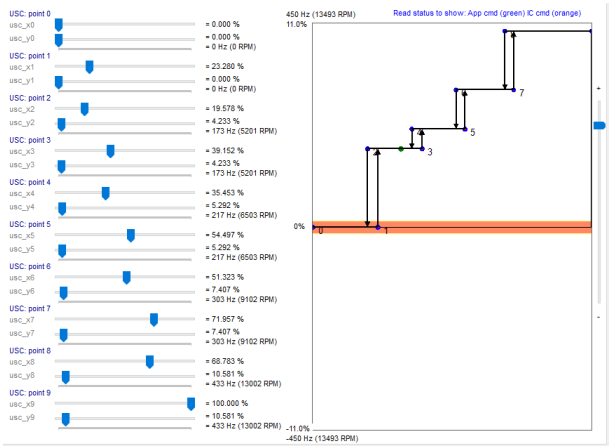


Figure 7: UCC Example 3

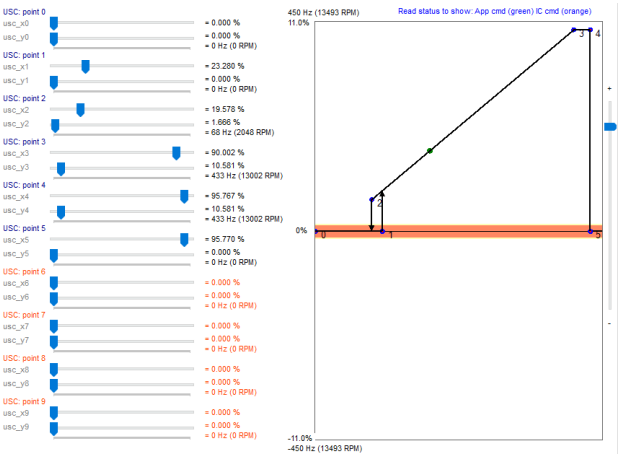


Figure 8: UCC Example 4

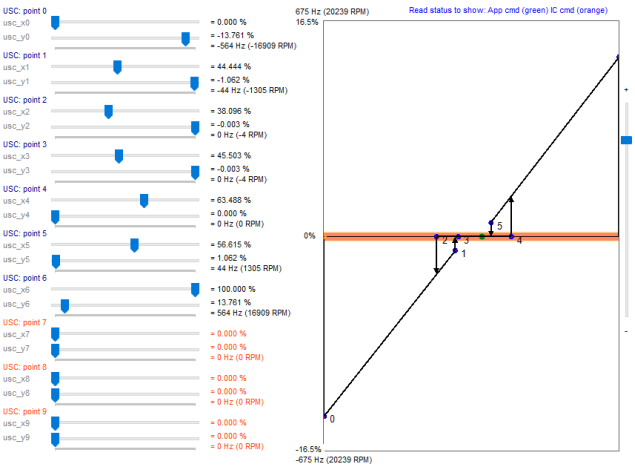


Figure 9: UCC Example 5

Motor Rotation Direction

Information about direction is decoupled from MCA_COMMAND. As shown in Figure 3, the FOC algorithm has two inputs: direction and command.

The direction of the motor depends on:

- Direction bit in the REF_CMD register, REF_CMD[16]
- MSB of MCA_COMMAND, MCA_COMMAND[16]:
  - If the Y values of the UCC are all positive, then MCA_COMMAND[16] = 0; otherwise, MCA_COMMAND[16] = 1
- ROT_DIR_INVERT configurable NVM parameter
- Operation control mode (speed, power, torque mode, selected according to SFOC_VAR_CTRL_MODE).

In speed control mode, motor direction is defined by:

- Motor direction = MCA_COMMAND[16] XOR ROT_DIR_INVERT XOR REF_CMD[16]

In torque and power control mode, motor direction is defined by:

- Motor direction= ROTDIRINVERT XOR REF_CMD[16]
- For torque and power control mode, ensure MCA_COMMAND[16] is 0 by setting Y values to all positive values.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Speed, Torque, or Power Control Modes

A89333 includes a control loop able to support three operational modes for motor control: speed, torque, and power. The control variable can be selected with the SFOC_VAR_CTRL_MODE NVM register setting.

Speed Mode (0x0)

In speed mode, MCA_COMMAND is used as a reference for the FOC speed loop to regulate the motor speed to f_{ref} [Hz].

MCA_COMMAND is scaled to the maximum frequency [Hz] according to the following formula:

Equation 4:

$$f_{ref}[W] = mca_{command}[LSB] \times \frac{f_{max}}{2^{15}-1}\frac{[Hz]}{[LSB]}.$$

Torque Mode (0x2)

In torque mode, MCA_COMMAND is used as reference for the FOC current loop to regulate the motor torque proportional to I_{ref} [A].

In this mode, the FOC speed loop is bypassed and the reference command is compared directly with estimated q axis current, Iq_{ref}.

MCA_COMMAND is scaled to the maximum system current [A] according to:

Equation 5:

$$I_{ref}[W] = mca_{command}[LSB] \times \frac{i_{max}}{2^{15}-1}\frac{[A]}{[LSB]}.$$

In torque control mode, MCA_COMMAND is downscaled to the current fraction length (11 bits). For this reason, the FOC algorithm command changes only if the external command varies for more than 16 units.

Power Mode (0x1)

In power mode, MCA_COMMAND is used as a reference for the FOC power loop to regulate the motor power to P_{ref} [W].

MCA_COMMAND is scaled to the maximum system power [W] according to:

Equation 6:

$$P_{ref}[W] = mca_{command}[LSB] \times \frac{P_{max}}{2^{15}-1}\frac{[W]}{[LSB]}.$$

In power control mode, the command is down-scaled to the voltage fraction length (14 bits) and, for that reason, the FOC algorithm command changes only if the external command varies for more than 2 units.

Maximum System Speed

The maximum system speed (f_{max} [Hz]) is the maximum electrical motor speed that can be commanded. It depends on frequency resolution, f_{res}, according to:

Equation 7:

$$f_{max} = round(2^{15} \times f_{res}),$$

where f_{res} [Hz/LSB] is the frequency resolution, set through the SFOC_FREQ_RES register according to:

Equation 8:

$$f_{res} = \frac{1}{9 \times 2^{sfocFreqRes}}\frac{[Hz]}{[LSB]}.$$

NOTE: The maximum rotation speed can be limited by supply voltage (V_{BB}); therefore, high command speed may not result in high motor rotation due to low V_{BB} voltage.

Maximum System Current and Bus Current Sensing

The maximum system current is typically set to 110% of the motor-rated current.

A single shunt resistor connecting between SENN and SENP is used to measure the bus current for the FOC algorithm and current limit. The resistor value is typically approximately tens of milliohms, depending on the maximum rated current of the system and the selected gain of the current sense amplifier.

Equation 9:

$$i_{max}[A] = \frac{ADC_{VREF}}{R_{shunt} \times CSA_{GAIN}},$$

where ADC_{VREF} is the reference ADC voltage equal to 1.2 V, R_{shunt} [Ω] is the board shunt resistance, and CSA_{GAIN} is the sense amplifier gain that can be set in the SFOC_CSA_GAIN NVM parameter to 10 V/V or 20 V/V.

Use of a Kelvin sensing connection is recommended when using the shunt resistor, as shown in Figure 10.

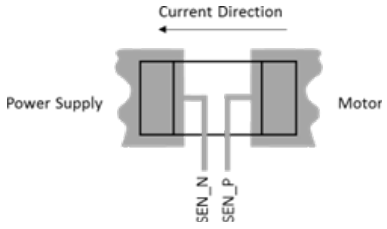


Figure 10: Kelvin Sensing Connection Recommended for Shunt Resistor Setups

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DC-Link Voltage

To enable proper controller operation, set the nominal DC-link voltage in the VBB_NOM NVM parameter according to:

Equation 10:

$$VBB_{nom} = round\left(\frac{VBB_{nom}[V]}{0.515625}\right),$$

where VBB_{nom} [V] is the nominal DC-link voltage and 0.515625 [V] is the scaling factor.

NOTE: Proper functioning of the A89333 requires that the nominal VBB used to power the device is correctly configured in the VBB_NOM NVM.

Maximum Electrical Power

The maximum electrical power value [W] is calculated using:

Equation 11:

$$Pmax[W] = \frac{3}{2} i_{max} 1.1547 \frac{VBB_{nom}[V]}{2}.$$

For example, with maximum system current, I_{Max} , of 6.25 A and VBB_{nom} of 12 V, the maximum electrical power is 64.95 W.

SPEED LIMIT

The SFOC_FREQ_LMT NVM parameter limits the maximum rotation speed. It works for all speed, torque, and power, and it is normally used in power and torque modes.

POWER LIMIT

The SFOC_PWR_LMT parameter in NVM limits the maximum power. This parameter is useful when commanding in torque and speed modes.

CURRENT LIMIT

The SFOC_DRV_CURR_DRV_LMT parameter in NVM limits the Iq, which subsequently limits the I_{BB}. This parameter is useful when commanding in power and speed modes.

Motor Control Application (MCA) Finite State Machine (FSM)

A89333 implements the FOC algorithm through a state machine, composed of four modes and six distinct states. The four modes of the MCA (motor controller application) are:

1. Standby Mode—This mode is activated after completion of the system startup routine or receipt of the command to stop motor driving (motor control application FSM enters SBY state, as described next).
2. Rotate Mode—This mode is activated when a command to start the motor is received (on exit from the SBY state).
3. Brake Mode—This mode is activated when a command to brake the motor is received.
4. Fail Mode—This mode is activated when one of the enabled faults is detected. Active fail mode is reported by activation of the nFLT pin.

The active mode of MCA can be read in the SW status register via I^2C communication.

The distinct states of the MCA FSM are shown in Figure 11:

- A89333 powers up in the standby state (SBY) with external power bridge in tri-state mode.
- After the internal initialization is complete and once a command to run the motor is received, the A89333 transitions to the windmill check state (WNDML) to determine the initial status of motor movement and then start to drive the motor as shown in Figure 11.
- If the motor is stationary or spinning at a very low speed that is considered to be stationary (typical startup), the A89333 enters the IPD state or the align state—depending on the NVM option (ALIGN_TYPE) to determine the initial rotor position or to put rotor into a known position—followed by the open-loop ramp-up (RAMPUP) and drive states.
- If the motor spins in the reverse direction (reverse windmill), braking (BRAKE mode) or deceleration with FOC control is applied to stop the motor.
- Once the motor stops, the typical startup routine can be applied as before.
- If the motor is already rotating in the correct direction (forward windmill), depending on the NVM option (described in the Windmilling—WNDML section), the driver can enter the drive state directly, skipping the IPD/align state and the ramp-up phase, or braking/FOC deceleration can be used to stop the motor, such as the reverse windmill, followed by typical startup.

The active state of the MCA can be read in the SW status register via I^2C communication.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

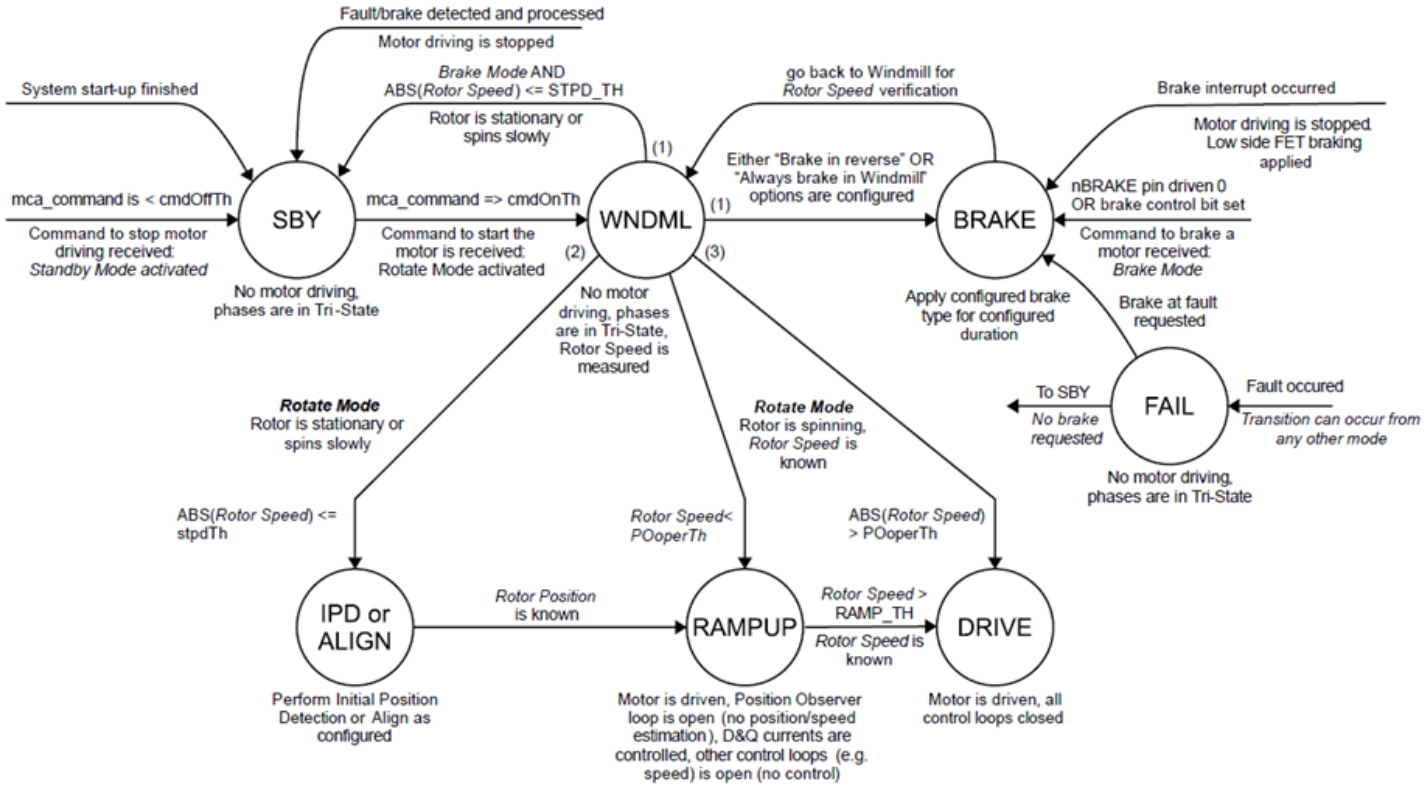


Figure 11: MCA FSM States

STANDBY—SBY

In the SBY state, the motor is not driven, and the power stage is in tri-state, so the motor can be externally rotated.

The A89333 transitions to the windmill (WNDML) state only when MCA_COMMAND exceeds the command on threshold of CMD_ON_TH and returns to standby when MCA_COMMAND is less than the command off threshold of CMD_OFF_TH.

The A89333 enters standby mode when one of the following conditions is verified:

- After completion of the system startup routine.
- At any point in time (independently, based on current state) after a fault is processed in the fail state.
- In brake mode, after the rotor successfully stops.
- If MCA_COMMAND reduces to less than CMD_OFF_TH. This is the procedure for commanding the motor to stop.

WINDMILLING—WNDML

In this state, the motor is not driven; however, the back electromagnetic force (BEMF) signals from the windings of the motor is analyzed to determine the rotation speed of the motor, the position of the rotor, and the direction of movement.

Based on the rotor speed measurement, the state machine reacts as follows:

- If the motor speed is less than the stopped threshold (STPD_TH, NVM parameter) or if an illegal switching sequence is detected, the device enters initial position detection (IPD) or rotor alignment (ALIGN) to determine the rotor position.
- If motor rotation exceeds the stopped threshold (STPD_TH) and:
  - □ Motor rotation is in the proper direction:
    - ♦ If the brake is enabled during the windmill state (BRAKE_IN_WNDML_ALWAYS_EN = 1, NVM parameter), the device enters the BRAKE state to reduce speed. The brake pattern is applied until the rotor is stationary. When speed is less than STPD_TH, the device enters the standby state.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

- ♦ If the brake is not enabled during the windmill state, the device enters the drive or ramp-up state, depending on the absolute value of the speed value with respect to the observer operational threshold (PO_OPER, configurable NVM parameter).

- □ Motor rotation is in the improper direction:

  - ♦ If the brake is enabled in the windmill state (BRAKE_IN_WNDML_ALWAYS_EN = 1 or BRAKE_IN_REVERSE_TYPE = 1), the device enters the brake state to reduce speed. From the brake state, the device returns to the windmill state to verify the speed condition. When the speed is less than STPD_TH, the device enters the standby state.

  - ♦ If the brake is not enabled in the windmill state, the motor is decelerated by FOC. Once it stops, it restarts in the opposite direction.

IPD AND ALIGN

The startup of a motor from stationary requires a known rotor position. A89333 supports both initial position detection (IPD) and alignment techniques.

- IPD (ALIGN_TYPE = 1, configurable NVM parameter), initial rotor position is determined by measuring the stator inductance difference caused by rotor flux. The IPD technique offers smoother and faster startup, without reverse spinning by using salient characteristics and winding saturation characteristics to determine the rotor position. IPD is performed in two stages:

  - □ In the first stage, test-pulse sequences are applied to the motor. If there is sufficient saliency ($L_q \neq L_d$), A89333 locks the rotor position within 30° of 0° to 180° or 180° to 360°.

  - □ When the first stage completes, A89333 applies a test sequence that uses the saturation property of the phase inductances of the motor to determine the current magnetic polarity of the rotor. Once the entire sequences complete, A89333 can determine the rotor angle within 30° accuracy.

- Align mode (ALIGN_TYPE = 0). A89333 supports both AC and DC alignment.

  - □ DC alignment is enabled by configuring SFOC_ACDC_ALIGN_TYPE = 0. A DC current is injected for a fixed length of time that is configured by the SFOC_ALGN_TIME parameter, such that the rotor aligns with the stator in a known position. The current limit during DC alignments is configured through the SFOC_ALGN_D_CURR_REF parameter. The SFOC_ALGN_TIME and SFOC_ALGN_D_CURR_REF parameters are generally related to the inertia of the system, and it is advisable to increase these two parameters if the inertia is large or if a load is applied on the shaft.

  - □ AC alignment is enabled by configuring SFOC_ACDC_ALIGN_TYPE = 1. A low-current-controlled driving frequency is applied to the winding to generate a known-position flux in the rotor. The integrated permanent magnet rotor gravitates to the generated stator flux. The AC alignment mode spins the rotor in open-loop control mode for the configured amount of time (ALGN_DUR, SFOC_ALGN_TIME) with constant frequency (AC_ALGN_FREQ, 1/ALGN _DUR) and current reference (SFOC_ALGN_D_CURR_REF). The alignment period should be chosen to match with the load torque required to gravitate the rotor. Longer alignment periods are more likely to catch the rotor than shorter alignment periods.

In align mode, the rotor may oscillate for some time before it starts to accelerate. This mode is typically used when the rotor position cannot be detected by the IPD. It is also a default action if the IPD fails to detect the initial rotor position (IPD_FAIL_ACTION).

After alignment or IPD completes, the FOC algorithm assumes that the rotor is stationary and is in the expected position, and the device enters the ramp-up state.

RAMP-UP—RAMPUP

During ramp-up, the driving frequency increases in open-loop mode until sufficient BEMF is generated to allow the observer to accurately detect the rotor speed and position for the transition into the closed-loop state (drive state).

Open-loop ramp-up increases rotor frequency up to RAMP_UP_FREQ based on the following parameters:

- SFOC_RAMP_TIME, which defines the length of the ramp-up phase.
- SFOC_RAMP_STEP, which defines the acceleration [freq/s] during the ramp-up phase only.
- SFOC_RUP_D_CURR_REF, which defines the current during ramp-up. Ramp-up speed is not affected by the value of the current. The appropriate current level depends on the properties of the motor and the connected load.

The choice of SFOC_RAMP_STEP and SFOC_RAMP_TIME affects the frequency of occurrences of transitions between open-loop and closed-loop states.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

For reliable start-up, an OL-CL transition frequency greater than 35 Hz is advised. This is achieved by selecting: 1) a RAMP_STEP value that is not excessively large, to allow use of a current equal to 60% of the rated current; and 2) a RAMP_TIME that is not excessively small.

Motors with larger inertia typically require smaller SFOC_RAMP_STEP and longer SFOC_RAMP_TIME.

For fast start-up with minimized start time, the ramp-up time in the open-loop state must be minimized. This may require an OL-CL transition frequency of less than 35 Hz at the expense of reliability. In addition, the value of RAMP_STEP must be increased, the value of the current to start the motor must be increased to the value of 80% to 100% of the nominal current, and the RAMP_TIME value must be reduced.

Generally, fast start-up demands high current.

DRIVE—DRIVE

In the drive state the motor spins using a sensorless field-oriented control (SFOC) technique.

In sensorless operation, the motor angle and speed are estimated based on the motor electrical model (inductance, resistance) and the voltage and current that are applied.

In the drive state, the current can be further controlled and limited by the following parameters:

- SFOC_DRV_CURR_DRV_LMT sets the maximum current driving capability of the Q axis.
- SFOC_DRV_CURR_RATE_LMT and SFOC_DWN_CURR_RATE_LIMIT limit the rate of growth and decrease of the current on the Q axis.

To prevent sudden changes in the torque applied to the motor, which could result in acoustic noise, the A89333 provides the option to limit the maximum rate of change of the speed command by using the SFOC_REF_RATE_LMT parameter.

REGENERATIVE MODE

In case of strong deceleration, the motor can operate as a generator and transfer energy back to the power. If the power supply is not able to absorb the energy, V_{BB} voltage is increased [pumped up; PUP], with the potential to damage the system.

The A89333 can limit the V_{BB} pump-up using the SFOC_VBB_LMT and SFOC_VBB_LMT_TH parameters. Alternatively, the Iq regenerative current can be limited using the SFOC_CURR_GEN_LMT and SFOC_GEN_CURR_RATE_LMT parameters.

BRAKE—BRAKE

Brake mode enables rapid motor shutdown, when desired. During braking, the three low-side drivers—connecting the three motor terminals together and short the motor BEMF—are enabled. In brake mode, the current of the winding is limited only by the motor and the resistance of the external FETs. Because of this, care must be taken to avoid excessive current in the FETs when braking. Several configuration options are available for programming in the NVM to allow for safe braking, such as pulsed braking and braking hold-off based on motor frequency.

In the brake state, the device activates the low-side MOSFET, braking the motor according to these parameters:

- BRAKE_FET_ON_DURATION
- BRAKE_FET_OFF_DURATION

If motor speed exceeds BRAKE_FREQ_TOO_HIGH_TH, the motor coasts before the brake is activated. This prevents generation of excessively high current that could damage the MOSFET or the motor.

The device enters the brake state when one of these conditions is verified:

- Pin nBRAKE is driven low.
- Brake bit is set in the BRAKE_CTRL register.
- Windmill state is active and a braking feature is required, as described in the Windmilling—WNDML section.
- Speed command MCA_COMMAND is less than CMD_OFF_TH and BRAKE_IF_OFF_EN = 1. If BRAKE_IF_OFF_EN = 0, the device enters the standby state and the motor coasts.

If BRAKE_IF_OFF_EN = 1, the device also keeps the motor braked (low-side MOSFET on) after the motor stops.

NOTE: If SOFT_OFF_EN is set, the motor can be decelerated in the closed-loop state (drive state). For more information about soft deceleration of the motor, refer to the APEK89333 user manual available on the Allegro website.

FOC Algorithm Speed and Current Loop

In speed mode, the command from MCA_COMMAND is used as a reference set point to the speed loop, and the output of the speed loop is used as the reference for the Q-axis current in the current loop.

In torque mode, the command from MCA_COMMAND is passed directly to the current loop as the reference for the Q-axis current.

The reference for the D-axis current can be set using the regis-

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ter SFOC_DRV_D_CURR_REF; however—to ensure that the stator and rotor field are 90° out of phase with each other, which allows for the maximum available torque and system efficiency—the recommended setting is zero.

PI controllers, one for speed and one for current loop, can be tuned using SFOC_D_CURR_KP, SFOC_D_CURR_KI, SFOC_Q_CURR_KP, and SFOC_Q_CURR_KI NVM settings.

The A89333 integrates a space-vector modulation (SVM) technique that optimizes use of the supply voltage and increases the base motor speed. The algorithm also implements a V_{BB} compensation feature that automatically adjusts the duty cycle to correct disturbances or sudden voltage variations on the supply voltage. The system works as a percentage of the nominal V_{BB} (VBB_NOM NVM parameter) and calculates the duty cycle, δ, for phase voltages according to:

Equation 12:

$$\delta = \frac{v_{phase}}{VBB_{measured}(\%) \times VBB_{nom}}.$$

Example 1:

VBB_{nom} = 12 V

v_{phase} calculated from FOC algorithm is 50% of VBB_{nom}

$VBB_{measured}$ from ADC = 12 V, so it is 100% of VBB_{nom}

Calculation of δ:

Equation 13:

$$\delta = \frac{v_{phase}}{VBB_{measured}(\%) \times VBB_{nom}} = \frac{50\%\ VBB_{nom}}{100\% \times VBB_{nom}} = 50\%$$

Example 2:

VBB_{nom} = 12 V

v_{phase} calculated from FOC algorithm is 50% of VBB_{nom}

$VBB_{measured}$ from ADC = 6 V, so it is 50% of VBB_{nom}

Calculation of δ:

Equation 14:

$$\delta = \frac{v_{phase}}{VBB_{measured}(\%) \times VBB_{nom}} = \frac{50\%\ VBB_{nom}}{50\% \times VBB_{nom}} = 100\%$$

The compensation of V_{BB} is guaranteed until V_{BB} measured is less than 2 × VBB_{nom}.

OBSERVER

For sensorless-mode operation, the motor angle and speed data are estimated in the observer block—without the need for an external sensor.

The machine parameters required in the A89333 observer are the motor phase inductance, sfocLs, and the motor phase resistance, sfocRs, according to:

Equation 15:

$$\mathbf{sfocLs} = round\left(\frac{2\pi \times i_{max} \times f_{res} \times motorLs \times 2^{(sfocLsFl+21)}}{0.298 \times VBB_{nom}}\right),$$

where:

- sfocLs [unitless] is the stator inductance NVM setting.
- i_{max} [A] is the maximum system current.
- $f_{res} = \frac{1}{9 \times 2^{sfocFreqRes}}\ [Hz/LSB]$ is the frequency resolution.
- motorLs [H] is the motor phase to neutral inductance (phase-to-phase/2).
- sfocLsFl [unitless] is the SFOC stator inductance fractional length NVM setting (signed).
- VBB_{nom} [V] is the nominal DC link voltage (should be in alignment with VBB_NOM setting).

Equation 16:

$$\mathbf{sfocRs} = round\left(\frac{motorRs \times i_{max} \times 2^{(sfocRsFl+11)}}{0.298 \times VBB_{nom}}\right),$$

where:

- sfocRs [unitless] is the stator resistance NVM setting.
- i_{max} [A] is the maximum system current.
- motorRs [Ω] is the motor phase to neutral resistance (phase-to-phase/2).
- sfocRsFl [unitless] is the SFOC stator inductance fractional length NVM setting (signed).
- VBB_{nom} [V] is the nominal DC link voltage (should be in alignment with VBB_NOM setting).

Proper functioning of the observer requires proper tuning of the controller parameters SFOC_PO_FREQ_K and SFOC_PO_THETA_K.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DIAGNOSTIC AND PROTECTION FEATURES

A89333 integrates advanced diagnostics for critical hardware protection and motor control diagnostics. Hardware protections include overvoltage, undervoltage, over temperature, and short-circuit protection. Motor control diagnostics include lock detection (loss of sync) and no-motor start.

If a fault event occurs, the nFLT pin is pulled low to indicate a fault condition. The nFLT pin can also be connected to the nBRAKE pin to brake the motor in case of an overcurrent fault. Braking is not allowed for the OVP, UV, OT, and lock detection states.

Every fault can be enabled or disabled (masked) using the NVM parameters UVS_DISABLE, OVT_DISABLE, OVP_ENABLE, OCP_ENABLE, ROT_STALL_DET_CTR = 0, and NO_MOTOR_START_EN.

Fault data flags can be read in the SW status register via I²C communication.

Table 4: Fault Table

Fault	Fault Action	Latched
V_{BB} Undervoltage	Disable outputs	N
Over Temp. Protection	Disable outputs	N
V_{BB} Overvoltage Protection (VBB OVP)	Disable outputs	N
Overcurrent Protection (OCP)	Disable outputs Latch reset with command off/on sequence or power-cycle	Y
Loss of Sync (Lock Det)	Set lock detect timeout—disable outputs	(SW latched fault)
No-Motor Start	Set lock detect timeout—disable outputs	(SW latched fault)

VBB UNDERVOLTAGE—VBB UVS

When digital logic is running and the supply voltage on the VBB pin reduces to less than the UVS_TH, the A89333 disables the outputs until the supply voltage reduces to less than the operating threshold, which is lower than the V_{BBUVLO} threshold.

After the V_{BB} undervoltage is detected, the outputs are disabled, the controller enters the fail mode, and fault reporting is performed by pulling low the nFLT pin and setting the corresponding fault flag in the SW status register. When the V_{BB} level rises to greater than UVS_TH (plus the hysteresis level), the outputs are re-enabled automatically (not latched), the fault flag is cleared, and the controller transitions to the standby mode and state. In the standby state, the controller verifies that the command exceeds the threshold of CMD_ON_TH, then transitions to the windmill state, where a speed check is performed and used by the device to determine if the start is from a stationary position or with a moving rotor.

The V_{BB} undervoltage protection level is programmable in NVM using the UVS_TH parameter (see Table 5). The V_{BB} undervoltage diagnostic is independently activated by the control method and state. If needed, the fault can be masked using the UVS_DISABLE parameter in NVM.

Table 5: UVS_TH Parameter

UVS_TH	V_{BB} UVS (V)
0	32
1	25
2	7

VBB, UV, AND NVM REPROGRAMMING

When the device is in an undervoltage (UV) state but the V_{BB} exceeds the operating threshold of the supply voltage for digital logic, if in user mode, it is possible to reprogram the NVM (EEPROM) registers regardless of the selected external command source and the state of the FG pin. Changes to NVM take effect only after POR.

The UV condition prevents incorrect transactions that can result from FG/RD pin toggling and guarantees that the FG/RD pin is in the proper state for I²C for any NVM configuration. To program the EEPROM, increase V_{BB} beyond 25 V after I²C communication is established.

If the FG/RD pin configuration cannot cause toggling (FG/RD pin is in the high state), it is possible to use I²C without UV and the EXT_CMD_SRC is not I²C. This allows NVM shadow programming when in user mode or SW status register consultation for diagnostic purposes. In this case, serial communication should be performed when the controller is in the standby state (motor stopped), and it can lead to unexpected motor starts.

OVERTEMPERATURE PROTECTION—OVT/TSD

The A89333 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the upper threshold T_{J_TSD}, when the OVT is detected, the outputs are disabled, the controller enters the fail mode, and fault reporting is performed by pulling low the nFLT pin and setting the corresponding fault flag in the SW status register.

When device temperature returns to less than the T_{J_TSD} threshold minus the hysteresis level, ΔT_J, the outputs are re-enabled automatically (not latched), the fault flag is cleared, and the controller transitions to the standby mode and state. In the standby state, the controller verifies that the command exceeds the threshold of CMD_ON_TH, then transitions to the windmill state, where a

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

speed check is performed and used for the device to determine if the start is from a stationary position or with a moving rotor.

The over-temperature protection diagnostic is independently activated by the control method and state. If not needed, the fault can be masked using the OVT_DISABLE parameter in NVM.

VBB OVERVOLTAGE PROTECTION—VBB OVP

Overvoltage protection is intended to protect the IC and the three-phase inverter in applications where the motor could be rotated at high velocity or where quick decelerations of motor speed are needed, which can result in significant energy fed back from motor coils to the power supply. Overvoltage could also be relevant when low-side FET braking is applied; because the A89333 switches the low-side FETs during braking, during the off time (t_{off}) the voltage generated on the inductors of the motor force the current to flow in the body diode of the high-side FETs, charging the capacity of the DC-link and generating a pump-up of V_{BB}.

When V_{BB} voltage exceeds OVP_TH, A89333 disables the outputs. After the V_{BB} overvoltage is detected, the outputs are disabled, the controller enters the fail mode, and fault reporting is performed by pulling low the nFLT pin and setting the corresponding fault flag in the SW status register. When the V_{BB} level reduces to less than the OVP_TH, the outputs are re-enabled automatically (not latched), the fault flag is cleared, and the controller transitions to the standby mode and state. In the standby state, the controller verifies that the command exceeds the threshold of CMD_ON_TH, then transitions to the windmill state, where a speed check is performed and used by the device to determine if the start is from a stationary position or with a moving rotor.

The V_{BB} overvoltage protection level is programmable using the OVP_TH parameter in NVM, in the range of approximately 0 V to 80 V. The V_{BB} overvoltage diagnostic is independently activated by the control method and state. If needed, the fault can be masked using the OVP_EN parameter in NVM.

OVERCURRENT PROTECTION—OCP (SHORT PROTECTION)

Overcurrent protection is intended to protect the power FETs from application conditions of shorted load, motor short to ground, and motor short to battery that can damage the system.

The V_{DS} voltages across each power MOSFET are monitored by the A89333. If any V_{DS} exceeds a predefined threshold (OCP_TH), when the corresponding MOSFET is in the conduction mode (turned ON), an OCP fault is triggered and the output becomes disabled.

OCP_TH	V_{DS} Threshold (V)
0	0.5
1	0.75
2	1.0
3	1.5

The V_{DS} threshold needs to be set as a function of the MOSFET (R_{DSON}) and to the maximum current that can be driven.

In case of a fault, the nFLT pin is pulled low, the fault flag is set in the SW status registers, and the output motor coasts (output disabled) or brakes using the low-side FETs (if the nFLT pin is connected to the nBRAKE pin). After braking completes (command off received; command is less than CMD_OFF_TH), a restart can be performed.

If braking is not configured, the bridge remains off and the restart procedure can be performed after the off command (the command is less than CMD_OFF_TH) is received.

Overcurrent protection (OCP) is a latched event and the output remains off until an off/on cycle command is received or the device is power-cycled.

OCP is independently activated by the control method and state. If not needed, the fault can be masked using the OCP_ENABLE parameter in NVM.

LOSS OF SYNC (LOCK/STALL DETECTION)

A89333 implements three stall detection mechanism selected by the ROT_STALL_DET_CTRL parameter in NVM:

- Frequency estimation: The rotation frequency estimated by the observer, f_{est}, is compared to the predefined threshold configured in the ROT_STALL_TOO_LOW_SPEED_TH. When abs(f_{est}) < ROT_STALL_TOO_LOW_SPEED_TH, the stall state is detected immediately.
- V_q estimation: The estimated V_q is compared to a range defined by ROT_STALL_DET_HIGH_TH and ROT_STALL_DET_LOW_TH. If the estimated V_q < ROT_STALL_DET_LOW_TH or V_q > ROT_STALL_DET_HIGH_TH for a duration exceeding ROT_STALL_DET_TIME_TH, the stall state is detected. For this estimate, the values of the motor phase resistance (SFOC_RS) and the motor BEMF constant (SFOC_KE) must be set. The motor BEMF constant (SFOC_KE) is set according to:

  Equation 17:

$$\mathbf{sfocKe} = round\left(\frac{2\pi \times f_{res} \times motorKe \times 2^{(4+(8+\mathbf{sfocKeFl}))}}{0.298 \times VBB_{nom}}\right)$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

where:

- □ sfocKe [unitless] is the motor BEMF NVM setting.
- □ i_{max} [A] is the maximum system current.
- □ $f_{res} = \frac{1}{9 \times 2^{sfocFreqRes}}$ $[Hz/LSB]$ is the frequency resolution.
- □ motorKe [V/(rad/s)] is the motor BEMF constant.
- □ sfocKeFl [unitless] is the SFOC stator inductance fractional length NVM setting (signed).
- □ VBB_{nom} is the nominal DC link voltage (should be in alignment with the VBBNOM setting).

- BEMF estimation: The estimated BEMF is compared to the predefined threshold in ROT_STALL_TOO_LOW_V_BEMF_TH. If abs(bemf) < abs(threshold), the stall state is detected immediately. The greater the value of ROT_STALL_TOO_LOW_VBEMF_TH, the faster the BEMF stall detection feature will detect the stall; however, the chances of a false stall detection increase.

After the first rotor stall is detected, the outputs are disabled, the controller enters the fail mode, and the fault is reported, pulling low the nFLT pin and setting the corresponding fault flag in the SW status register. The controller remains in the fail mode until the stall condition is absent, including during retries. Once the rotor is stalled, the controller tries to restart the motor for a total number of attempts set by ROT_START_RETRY_MAX_ATTEMPTS, with a delay of ROT_STALL_RETRY_T_OUT between each retry.

If the rotor is no longer in the stall state during the retries, the outputs are re-enabled automatically, the fault flag is cleared (not latched), and the controller transitions to the standby mode and state. In the standby state, the controller verifies that the command exceeds the threshold of the CMD_ON_TH parameter, then transitions to the windmill state, where a speed check is performed and used by the device to determine if the start is from a stationary position or with a moving rotor.

Alternatively, after the retry attempts complete, if the motor is still stalled, the controller checks if command < CMD_OFF_TH and, if not, remains in the fail mode and the standby state with the RS flag in the SW status register set. Otherwise, the fault and flag are cleared, and the MCA mode is changed to standby mode.

NOTE: Stall detection is masked during the open-loop (ramp-up) state and starts working only after the controller transitions to the closed-loop (drive) operation and ROT_STALL_BLANK_DUR elapses.

NO-MOTOR START

The no-motor start diagnostic detects a fault when a command to start the motor is applied without the motor connected to the board. The fault handling mechanism is the same as the stall detection fault.

VBB OVERVOLTAGE VARIABLE LIMITER

If enabled (OVVL_ENABLE), A89333 enters the OVVL condition when the voltage increases to greater than OVVL_VOLT_TH and it exits the condition when the voltage reduces to less than OVVL_VOLT_TH.

If the voltage increases to greater than OVVL_VOLT_TH, the command is overwritten by the OVVL_VAR_LMT value. This prevents a further increase in voltage and does not trigger any faults.

To enter the OVVL condition, OVVL_VOLT_TH must be less than OVP_TH (else, the OV fault is triggered first).

Overvoltage detection is not considered a fault, and it greatly influences the maximum power limit function.

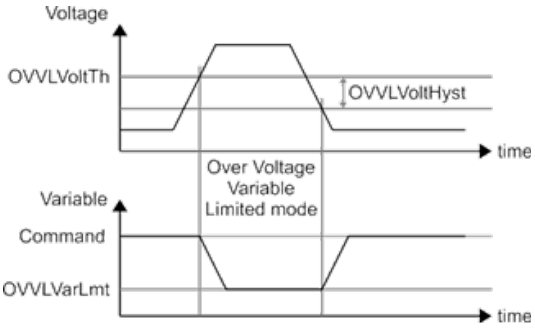


Figure 12: OVVL Timing Diagram

OVERCURRENT LIMIT

A89333 can limit the maximum Q-axis current setting using the SFOC_DRV_CURR_DRV_LMT parameter in NVM as a percentage of the maximum current (I_{max}) that the system can handle. The Q-axis current limit is also designed to avoid demagnetization of permanent magnets. This is not considered a fault.

MAXIMUM POWER LIMIT

By monitoring V_{BB} and I_{BB}, the A89333 reduces the output current when the maximum power limit is exceeded and regulates the power around the NVM-programmed maximum power limit (SFOC_PWR_LMT). The maximum power limit can be applied in all control modes: speed, torque, and power. This limit is set as a percentage of the maximum power (P_{max}) that the system can manage. For details, refer to the APEK89333 user manual available on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION FEATURES

EEPROM NVM for Storing Motor Control and Configuration Data

Motor control and configuration data are user-programmable and stored in the EEPROM of the IC.

Upon power-up, the A89333 waits for the internal regulators to reach their UVLO levels, then loads the configuration data from the EEPROM. After the configuration is loaded, the A89333 is in standby mode and is ready to respond to user input through the PWM/SPD pin or I²C port. The A89333 power-up and initialization sequence is shown in Figure 13.

FG/RD Pin

A89333 FG/RD pin can be configured in the four states described in this section.

FG

When EN_FG_FUNC is set, a square wave representing the electrical rotation frequency is generated on the FG/RD pin to attain the motor speed according to:

- If FG_PP = 0 (NVM parameter) is selected:

  Equation 18:

$$FG_{freq}[Hz] = 0.00390625 \times (FGgain + 1) \times f_{elect}[Hz].$$

- If FG_PP = 1...7 (NVM parameter) is selected:

  Equation 19:

$$FG_{freq}[Hz] = \frac{0.00390625 \times (FGgain + 1)}{FGpp + 1} \times f_{elect}[Hz],$$

where FG_{gain} is an NVM parameter that can assume integer values between 0 and 1023.

Typical configuration is to set FG_GAIN = 255 and FG_PP to number of motor pole-pairs. With such a configuration, the FG pin toggles with electrical frequency normalized to pp/2.

According to FG_START_TYPE, the FG signal can be generated once FOC starts, during ramp-up or after rotor synchronization (drive state).

RD

When the RD feature is enabled (EN_RD_FUNC), the stalled condition is reported on the FG/RD pin according to the RD_ACTIVE_LEVEL parameter in NVM:

- RD_ACTIVE_LEVEL = 0: If a stall condition occurs, the FG/RD pin is set high.
- RD_ACTIVE_LEVEL = 1: If a stall condition occurs, the FG/RD pin is set low.

The pin remains in the active level throughout the duration of the presence of the stalled latch.

FG IN VBB UV CONDITION

Because the FG pin shares the SDA pin of the I²C serial communication, if an undervoltage fault is present, the FG pin is set to a high (logic 1) state, enabling I²C communication. For more information, refer to the VBB, UV, and NVM Reprogramming section.

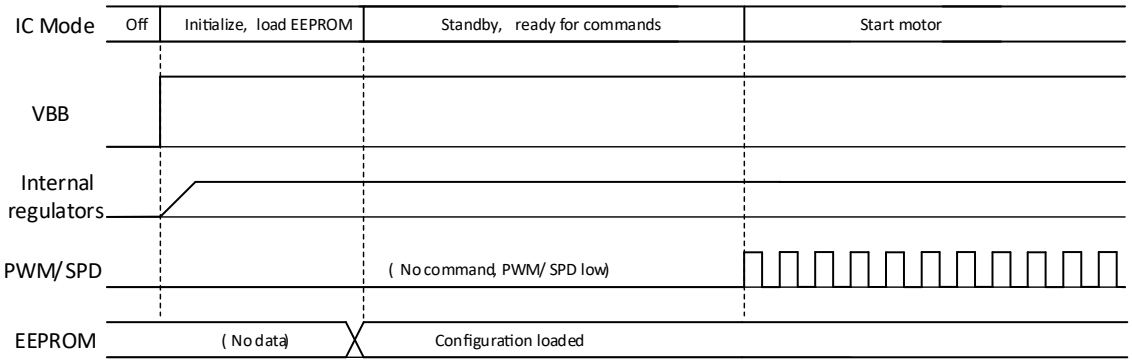


Figure 13: Power-Up and Initialization Sequence

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Dead Time Configuration

To avoid shoot-through current in the H-bridge, dead-time is implemented, which delays the high side from turning on after the low side turns off and delays the low side from turning on after the high side turns off.

The desired dead time can be programmed using the PWM_DEAD_TIME parameter:

Equation 20:

$$DeadTime\ [s] = \mathbf{pwmDeadTime} \times t_{clk}\ [s]\ ,$$

where PWM_DEAD_TIME is configurable in NVM with values of [0:255], t_{clk} = 40 [ns] (T_J = 25°C, R_{OSC} = 25 kΩ).

Slew Rate Control

A89333 can control the MOSFET gate charge and discharge without the need for external components.

Output slew rate can be estimated by the Q_{GD} specification of MOSFET and chosen gate drive current according to:

Equation 21:

$$dt = Q_{GD}/(I_{SRC} \text{ or } I_{SNK}).$$

PWM_GD_SLEW_RATE	I_{SRC} (mA) (I_{HS})	I_{SNK} (mA) (I_{LS})
0	9	25
1	25	45
2	42	68
3	63	68

Buck Converter

A89333 integrates a buck converter to generate the V_{REG} supply voltage for internal regulators and gate drivers from the V_{BB} supply voltage. The regulated voltage supplies the gate drive circuit, charges the bootstrap capacitors, and powers external circuits with a total consumption of up to 50 mA.

The buck regulator requires a single inductor (L = 10 µH ± 20%, I_{SAT} ≥ 970 mA; a high value of inductor can be used if the inductor is not saturated) mounted between the SW and the VBIAS terminals and a Schottky diode (V_R ≥ 100 V, I_F ≥ 1 A) between the SW and GND terminals. A ceramic decoupling capacitor of at least 10 µF should be connected between VBIAS and GND, close to the terminals. The switching frequency of the buck regulator is not fixed: It depends on the V_{BB} supply voltage.

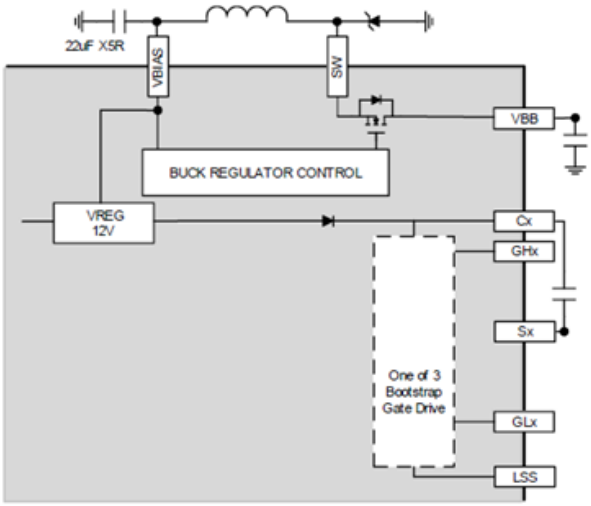


Figure 14: Buck Converter

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Advanced Features

SOFT-OFF DECELERATION

A89333 implements the soft-off deceleration feature, which allows selection of motor deceleration method before it stops. For more information about this advanced feature, refer to the APEK89333 user manual available on the Allegro website.

SOFT START

Soft start allows for the quiet application of current before the align or ramp-up state: It avoids the onset of the inrush current, which is caused by the presence of current-scaling references required in the align and ramp-up states.

For more information about this advanced feature, refer to the APEK89333 user manual available on the Allegro website.

QUIET START

To achieve a quieter OL-CL transition, A89333 implements a quiet start feature. The A89333 allows selection of a phase-current limit at the OL-CL transition.

Current can also be reduced in the ramp-up (SFOC_RUP_D_CURR_REF), toward the end of the open-loop ramp-up period, by properly configuring the OL-CL transition duration.

When the level of current is close to the level of current required by the feedback control, the transition noise may be able to be minimized.

For more information about this advanced feature, refer to the APEK89333 user manual available on the Allegro website.

FORCED OL

The forced OL feature allows the A89333 to switch from speed control to power or torque control when the external command exceeds a configurable threshold. Above the selected threshold, the reference can be selected to reach a specific desired value of power or torque, or the power/torque reference can be calculated from the applied PWM duty cycle/I²C command.

For more information about this advanced feature, refer to the APEK89333 user manual available on the Allegro website.

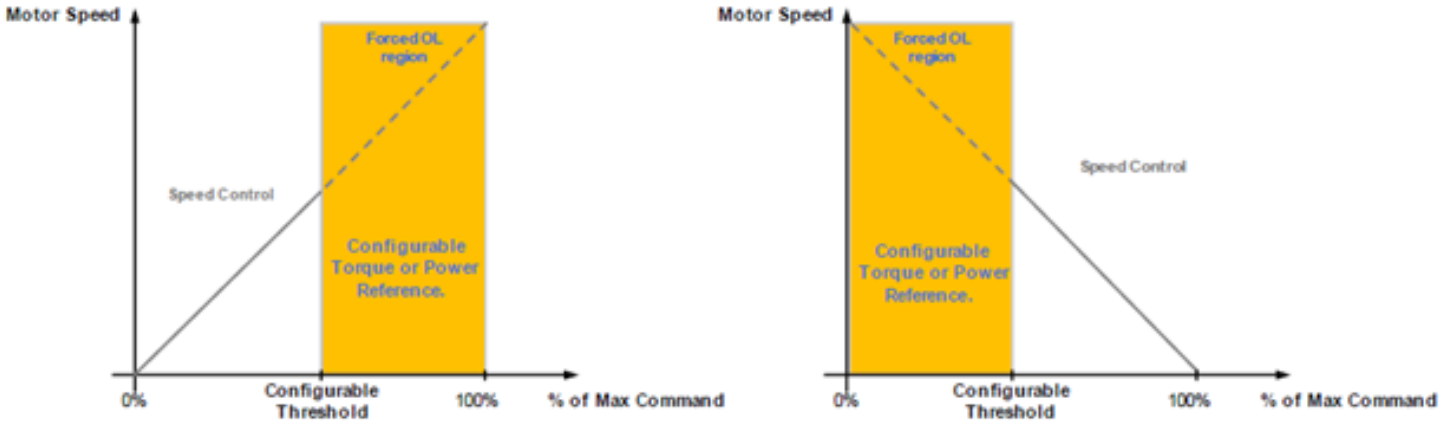


Figure 15: Forced OL High-Level Description

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

VIN and Power-Loss Brake

The A89333 can detect a power loss by monitoring the VIN pin, and the brake function can be applied to slow the motor. When the motor spins, the BEMF voltage generated is rectified by the body diodes of the output DMOS devices and the V_{BB} power supply capacitor is charged. If adequate voltage can be stored on the V_{BB} capacitor, the low-side MOS devices can be turned on to provide braking force to the motor. When the motor slows, the generated BEMF voltage is reduced, eventually resulting in insufficient voltage on the V_{BB} line to power the low-side MOSFETS; thus, the braking force is not applied and the motor coasts.

When the motor spins, the A89333 power-loss brake circuitry boosts the voltage on the V_{BB} line by pulsing the motor windings off. If the motor is rotating, current is present in the motor winding when the brake is applied. This current can be used to charge up V_{BB} capacitor and boost the V_{BB} voltage by pulsing off the brake mode for a short time, similar to hysteretic boost converter operation. This, in turn, allows the IC to brake the motor at a much lower speed than otherwise possible.

Modes of operation depending on the state of the VBB and VIN pins are detailed in Table 6 and Figure 16.

Table 6: Operation Modes Based on VBB and VIN Pin States

VIN [1]	VBB	Mode of Operation	Notes
Low	< V_{BBTH}	Coast—No braking	
Low	> V_{BBTH} and < V_{BOOST}	Brake PWM	If motor spin is sufficiently fast, V_{BB} ramps up to V_{BOOST}
Low	= V_{BOOST}	Brake—Hysteretic boost	V_{BB} is regulated to V_{BOOST}
Low	> V_{BOOST}	Brake	V_{BB} decays depending on I_{BB2} and V_{BB} capacitance
High	< V_{BBUVLO}	Coast—No braking	Power-up or power-down
High	> V_{BBUVLO}	Run	V_{REF} powers up logic; motor starts if PWM signal is valid

[1] V_{IN} < V_{INTH} = Low; V_{IN} > V_{INTH} = High

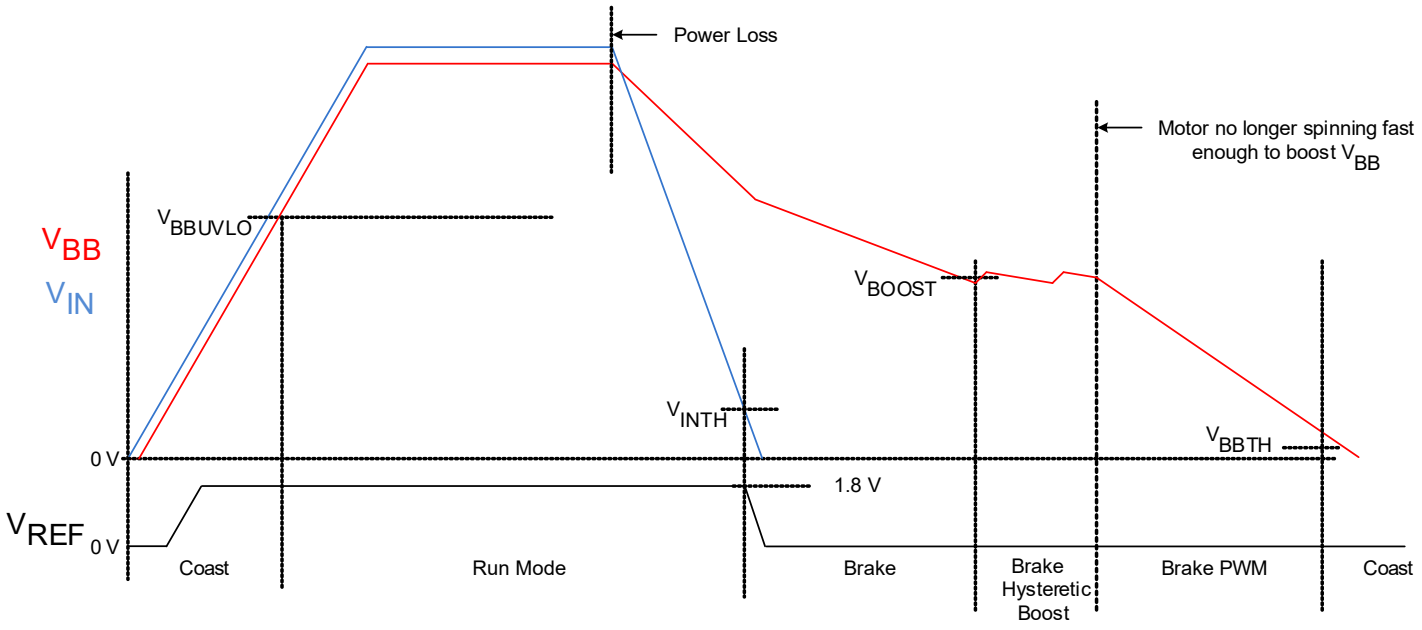


Figure 16: Typical Power-Up and Power-Loss Sequence

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

No-Power Brake

Braking is also possible when power is not supplied to the module and the motor is spun by external force (i.e., windmill situation), as shown in Figure 17. In this case, the generated BEMF voltage increases V_{BB} beyond the V_{BBTH}, which enables the braking process.

For more information, refer to the APEK89333 user manual available on the Allegro website.

AC Loss Function

When a loss of the AC main supply occurs, the system switches to battery power. During this period, the AC loss function option in the NVM can be used to maintain a minimum required motor speed with a much-reduced I_{BB} level. If the PWM input is stuck low or high—depending on the NVM option AC_PWRLOSS_PWM_STATE—for more than a programmable time (AC_PWRLOSS_START_DUR), the A89333 enters AC loss mode. In this mode, the A89333 limits the Q-axis current and thereby limits the I_{BB} current. The Q-axis current is programmable via the NVM parameter AC_PWRLOSS_QCURR_LMT. For the case of zero current, the IC coasts. The typical PWM pattern for entrance to the AC loss function is shown in Figure 18.

The AC_PWRLOSS_RELEASE_SEL in NVM is programmable to exit AC loss mode either:

- after a programmable time; or
- based on the motor speed, where the IC exits AC loss mode if the motor speed is less than or equal to the speed set by the AC loss duty.

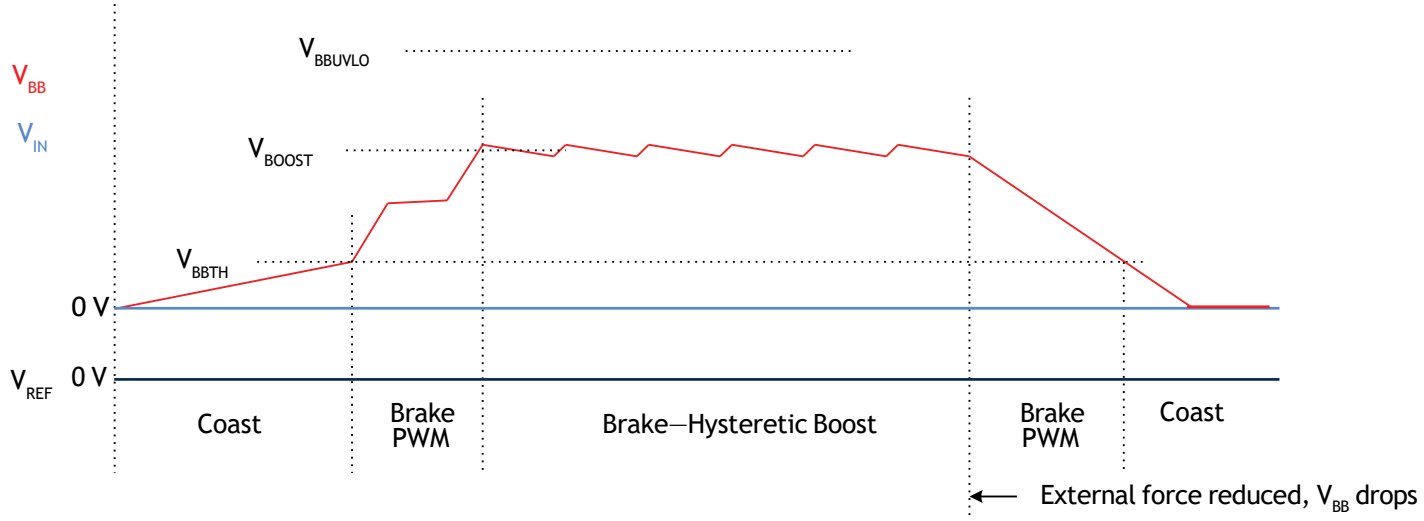


Figure 17: Motor Spinning By External Force, Power Not Applied to Fan Module

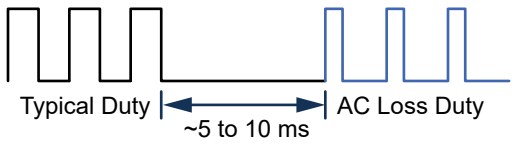


Figure 18: PWM Pattern for Entering AC Loss Function

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

REGISTERS AND NONVOLATILE MEMORY (NVM) MAP

A89333 uses NVM to store configuration data. Configuration data can be adjusted for a particular application. Upon power-up, the contents of the NVM are copied into registers (often called shadow registers) before they can be accessed by the logic circuits and used to control the motor operation. Direct access to shadow registers is also allowed through I²C interface. Writing to the shadow registers typically changes the operation of the driver immediately. (Some settings, the A89333 must enter standby mode, and the motor must be restarted before changes take effect). Changes made to NVM do not affect device operation until power is cycled.

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4C0	460	0	0	2:0	WNDML_MAX_ERR_ATTEMPTS	0x0	Maximum number of errors before exit to windmill error state (N + 1)
				5:3	WNDML_MAX_TO_ATTEMPTS	0x0	Maximum number of timeouts before rotor is considered to be stationary (N + 1)
				8:6	WNDML_NUMBER_OF_ASSESSMENTS	0x0	Quantity of windmill assessments to perform (N + 1)
				9	WNDML_TIMER_PRESCALER	0x0	Windmill timer prescaler: t_{tick} = (1 + TIMER_PRESCALER) × t_{clk}
				12:10	WNDML_TIMEOUT_PERIOD	0x0	Windmill timeout (1/2 of rotor period): For WNDML_TIMER_PRESCALER = 0 (frequency range 3000 Hz to 2 Hz): 0 = 20 ms 1 = 40 ms 2 = 81 ms 3 = 121 ms 4 = 162 ms 5 = 202 ms 6 = 243 ms 7 = 562 ms For WNDML_TIMER_PRESCALER = 1 (frequency range 750 Hz to 0.5 Hz): x2
				13	AC_POWERLOSS_PWM_STATE	0x0	0 = AC power-loss mode is entered when PWM state is low 1 = AC power-loss mode is entered when PWM state is high
				18:14	WNDML_EDGE_GLITCH_TIME	0x0	Edge glitch blanking time (N + 1) × 135 × (WNDML_TIMER_PRESCALER + 1) × t_{clk}
				21:19	WNDML_DEBOUNCE_TICK	0x0	Debounce tick: 0 = 40 ns 1 = 1 µs 2 = 11 µs 3 = 115 µs 4 = 1.1 ms 5 = reserved 6 = reserved 7 = reserved
				26:22	WNDML_DEBOUNCE_DELAY	0x0	Debounce time in debounce tick: 2^N
				31:27	SFOC_REF_RATE_LIMIT	0x0	Reference rate limit, [0.09312u% × 2^N] of maximum (system) speed per VCL update

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4C1	461	1	1	4:2	IPD_MAX_ERR_ATTEMPTS	0x0	maximum number of errors before return of error code, for Stage 1 and Stage 2
				7:5	IPD_NMBR_OF_EXCIT_ELEMENTS	0x0	Number of Stage 1 Base excitation elements to perform
				10:8	IPD_PWM_PERIOD	0x0	Duration of PWM period for IPD; 0 - 750 clk (33.33 kHz): 1 = 875 clk (28.57 kHz) 2 = 1000 clk (25 kHz) 3 = 1125 clk (22.22 kHz) 4 = 1250 clk (20 kHz) 5 = 1375 clk (18.18 kHz) 6 = 1500 clk (16.67 kHz) 7 = 1625 clk (15.38 kHz)
				12:11	IPD_STG1_ROUND_PAUSE	0x0	Pause after rounds of stage 1: 0 = 18 µs 1 = 36 µs 2 = 72 µs 3 = 144 µs
				13	IPD_STG2_CSA_GAIN	0x0	IPD stage 2, current sense amplifier (CAS) gain: 0 = 20 V/V 1 = 10 V/V
				14	IPD_STG2_TYPE	0x0	IPD stage 2 type: 0 = constant-current (IPD comparator) mode 1 = constant time (ADC current measurement) mode
				20:15	IPD_IPDDAC_CODE	0x0	Configuration of IPD DAC output signal for stage 2 of IPD: 2.4 V – N × 37.5 mV
				22:21	IPD_BLANKING_TIME	0x0	IPD comparator blanking time: 560 ns + (N × 2.88 µs)
				25:23	IPD_STG2_ROUND_PAUSE	0x0	Pause after rounds of stage 2: (2^N) × 90 µs
				30:26	IPD_STG2_PULSE_DURATION	0x0	Stage 2 pulse duration [maximum value (timeout) in constant-current mode, pulse duration in constant time mode]: 0 = 14 µs 1 = 17 µs 2 = 22.5 µs 3 = 33.5 µs 4 = 45 µs 5 = 56 µs 6 = 67.5 µs 7 = 90 µs 8 = 112 µs 9 = 135 µs 10 = 225 µs 11 = 281 µs 12 = 394 µs 13 = 562 µs 14 = 843 µs 15 = 1.1 ms 16 = 2.2 ms 17 = 4.5 ms 18:31 = reserved
				31	IPD_STG2_SATURATION_TH	0x0	Stage 2 measurement equality threshold: 0 = 3.125% 1 = 6.25%

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4C2	462	2	2	7:0	PWM_PERIOD	0x0	PWM period duration: (N × 16 + 800) × t_{clk}
				15:8	PWM_DEAD_TIME	0x0	PWM dead time pause duration: N × t_{clk}
				17:16	RESERVED	0x0	Reversed
				20:18	RESERVED	0x0	Reserved
				21	PWM_HIGH_RES	0x0	PWM high-resolution mode: 1 = enable 0 = disable
				23:22	PWM_REFRESH_PERIODICITY	0x0	Periodicity of bootstrap refresh pulse insertion, PWM periods: 0 = 4th PWM period 1 = 6th PWM period 2 = 8th PWM period 3 = 10th PWM period
				26:24	PWM_REFRESH_PULSE_DURATION	0x0	Bootstrap refresh pulse duration, N × t_{clk}: 0 = off 1 = 12 (0.48 µs) 2 = 23 (0.92 µs) 3 = 34 (1.36 µs) 4 = 68 (2.72 µs) 5 = 101 (4 µs) 6 = 141 (5.6 µs) 7 = 197 (7.9 µs)
				29:27	PWM_REFRESH_THRESHOLD	0x0	Bootstrap refresh threshold, duty cycle that enables bootstrap refresh feature, % of PWM period: 0 = 100% 1 = 99.21875% 2 = 98.4375% 3 = 97.65625% 4 = 96.875% 5 = 96.09375% 6 = 95.3125% 7 = 94.53125%
				31:30	PWM_GD_SLEW_RATE	0x0	Gate driver slew current setting, four settings: 0 = 10 mA for HS, 30 mA for LS 1 = 30 mA for HS, 50 mA for LS 2 = 50 mA for HS, 70 mA for LS 3 = 70 mA for HS, 70 mA for LS
4C3	463	3	3	0	SFOC_CSA_GAIN	0x0	SFOC CSA (current sense amplifier) gain: 0 = 20 V/V 1 = 10 V/ V
				3:1	SFOC_VCL_UPDATE_RATE	0x0	SFOC VCL update rate in number of PWM periods: 2^N
				5:4	SFOC_FREQUENCY_RES	0x0	SFOC frequency resolution: 0 = 0.111 Hz 1 = 0.056 Hz 2 = 0.028 Hz 3 = 0.014 Hz
				14:6	SFOC_RAMP_TIME	0x0	Ramp-up time: [40 + 256 × N] VCL updates
				24:15	SFOC_RAMP_STEP	0x0	Ramp-up frequency (speed) rate: [(N + 1) × 0.0244140625% of maximum (system) speed] per second
				31:25	SFOC_FREQUENCY_LMT	0x0	Speed limit: (N + 1) × 0.78125% of maximum (system) speed
4C4	464	4	4	3:0	SFOC_BRAKE_ALGN_CONST_DQ_CURR_KP	0x0	Brake align constant D/Q current PI controller proportional gain (signed): 2^N
				9:4	SFOC_BRAKE_ALGN_CONST_DQ_CURR_KI	0x0	Brake align constant D/Q current PI controller integral gain (signed): 2^N
				12:10	SFOC_RD_OL_SPD_ENTRY_TH	0x0	Reverse-drive open-loop entry frequency threshold: (N + 1) × 0.390625% of maximum (system) speed
				15:13	SFOC_RD_OL_SPD_EXIT_TH	0x0	Reverse-drive open-loop exit frequency threshold: (N + 1) × 0.1953125% of maximum (system) speed
				17:16	SFOC_RD_OL_RAMP_STEP_COEFF	0x0	Reverse-drive open-loop ramp step coefficient: (N + 1)/4
				27:18	FG_GAIN	0x0	FG (frequency generation) gain, FG_PP: 0 = 0.00390625 × (N + 1) 1:7 = 0.00390625 × (N + 1) × 2/(FG_PP + 1)
				30:28	FG_PP	0x0	Number of pole-pairs: (N + 1)
				31	NO_MOTOR_START_EN	0x0	No-motor start detection enable: 0 = disabled 1 = enabled

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4C5	465	5	5	11:0	SFOC_LS	0x0	Stator inductance constant, unitless
				15:12	SFOC_LS_FL	0x0	Stator inductance constant FL (signed), 5 + N
				16	ACPWRLOSSEN	0x0	AC power-loss function enable: 0 = disabled 1 = enabled
				20:17	ACPWRLOSSQCURRLMT	0x0	AC power-loss Q current limit: N = 0: zero current N ≠ 0: (N + 2) × 3.125% of maximum current
				25:21	SFOC_RUP_D_CURR_REF	0x0	Ramp-up D current reference; (N + 1) × 3.125% of maximum current
				29:26	SFOC_DRV_D_CURR_REF	0x0	Drive D current reference: –1 × (N × 1.5625)% of maximum current
				31:30	ACPWRLOSSOFFDUR	0x0	With AC power loss, the PWM low duration (for inverted PWM, the PWM high duration) that is considered for the off command: (24 + 2 × N) of the AC power-loss start duration
4C6	466	6	6	4:0	SFOC_D_CURR_KP	0x0	D current PI controller proportional gain (signed), 2^N
				10:5	SFOC_D_CURR_KI	0x0	D current PI controller integral gain (signed), 2^N
				15:11	SFOC_Q_CURR_KP	0x0	Q current PI controller proportional gain (signed), 2^N
				21:16	SFOC_Q_CURR_KI	0x0	Q current PI controller integral gain (signed), 2^N
				27:22	SFOC_PO_THETA_K	0x0	Position observer theta gain (signed), 2^N
				31:28	AC_PWRLOSS_START_DUR	0x0	The PWM low duration (for inverted PWM, the PWM high duration) that is required to start in the AC power-loss mode—should be configured to ~500 µs: N + 2 V_{CL} updates
4C7	467	7	7	5:0	SFOC_PO_FREQ_K	0x0	Position observer frequency gain (signed), 2^N
				8:6	SFOC_PO_ERR_LMT	0x0	Position observer error limit, 2^N
				10:9	SFOC_VAR_CTRL_MODE	0x0	Variable control mode (variable select): 0 = speed control 1 = power control 2 = torque control 3 = reserved
				16:11	SFOC_VAR_KI	0x0	Variable control (speed/power) integral gain (signed), 2^N
				21:17	SFOC_VAR_KP	0x0	Variable control (speed/power) proportional gain (signed), 2^N
				31	SFOC_PWM_OVERMOD_EN	0x0	PWM over-modulation factor: 0 = disabled (100%) 1 = enabled (115.625%)
4C8	468	8	8	4:0	SFOC_D_CURR_GEN_LMT	0x0	Generator (regenerative brake) D current limit: N × 3.125% of maximum current
				8:5	SFOC_ALGN_DQ)_CURR_KP	0x0	Align D/Q current PI controller proportional gain (signed), 2^N
				14:9	SFOC_ALGN_DQ_CURR_KI	0x0	Align D/Q current PI controller integral gain (signed), 2^N
				19:15	SFOC_DRV_CURR_DRV_LMT	0x0	Drive Q current limit: (N + 1) × 3.125% of maximum current
				24:20	SFOC_QCURR_GEN_LMT	0x0	Generator (regenerative brake) Q current limit: N × 3.125% of maximum current
				31:25	SFOC_VBB_LMT	0x0	Voltage limit: 7.0546875 V + N × 1.0078125 V
4C9	469	9	9	5:0	SFOC_VBB_LMT_TH	0x0	Voltage limit threshold (below voltage limit): (N + 1) × 1.0078125 V
				11:6	SFOC_PWR_LMT	0x0	Power limit: N × 1.5625% of {(3/2) × [(maximum current) × 1.1547 × (nominal voltage)/2]}
				17:12	SFOC_FREQUENCY_LMT_TH	0x0	Speed limit threshold (below speed limit): (N + 1) × 0.78125% of speed limit
				21:18	SFOC_VAR_ERR_LMT	0x0	Variable error limit (speed or power): 2^N
				22	SFOC_ACDC_ALIGN_TYPE	0x0	AC/DC align type: 0 = DC align 1 = AC align
				31:29	AC_PWRLOSS_RELEASE_SEL	0x0	AC power-loss release condition: 0 = speed is less than or equal to the PWM duty cycle 1:7 = [(4 + N) × 4000] of the AC power-loss start duration
4CA	46A	10	10	4:0	SFOC_ALGN_D_CURR_REF	0x0	Align D current reference: (N + 1) × 3.125% of maximum current
				10:5	SFOC_ALGN_TIME	0x0	Align time: 2048 × (N + 1) VCL updates
				15:11	SFOC_BRAKE_ALGN_CONST_D_CURR_REF	0x0	Brake align constant D current reference; (N + 1) × 3.125% of maximum current
				20:16	DTC_GAIN	0x0	Dead time compensation (DTC) gain
				27:21	DTC_MAX_TIME	0x0	Dead time compensation (DTC) maximum compensation time, in units of 6.25%
				31:28	SFOC_DWN_CURR_RATE_LIMIT	0x0	Down current rate limit, [$2^{(N + 11)}$ × 0.745 µ%] of maximum current per VCL update

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4CB	46B	11	11	7:0	MSQ_CST	0x0	Measurement-sequencer current-measurement settling time: N × t_{clk}
				9:8	EXT_CMD_SRC	0x0	External command source: 0 = I²C 1 = VCMD 2 = duty cycle (PWM) 3 = frequency (SPD)
				11	ALIGN_TYPE	0x0	Align type: 0 = align 1 = IPD
				12	IPD_FAIL_ACTION	0x0	IPD fail action: 0 = perform alignment 1 = start from 0 angle
				13	EN_RD_FUNC	0x0	Enable rotation detection (RD) functionality: 0 = disabled 1 = enabled
				14	EN_FG_FUNC	0x0	Enable frequency generation (FG) functionality: 0 = disabled 1 = enabled
				15	PWM_MOD_MODE	0x0	PWM switching pattern configuration: 0 = edge start with compensation 1 = edge start without compensation
				23:16	VBB_NOM	0x0	Nominal V_{BB} voltage; N × 0.515625 V
				26:24	SYSTEM _TIMER_UPDATE_RATE	0x0	System timer update rate: N = 0:5, 1188 ms/$2^{(N \times 2)}$ N = 6:7, 1.16 ms
				27	FG_START_TYPE	0x0	FG start type: 0 = after FOC starts 1 = after rotor synchronizes
				28	RD_ACTIVE_LEVEL	0x0	Set rotation detection (RD) active high/low: 0 = high 1 = low
				30:29	CAT_DUR	0x0	Current acquisition time duration: 0 = 1/16 t_{PWM} 1 = 1/20 t_{PWM} 2 = 1/32 t_{PWM} 3 = 1/40 t_{PWM}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4CC	46C	12	12	0	OCP_AUTORELEASE	0x0	OCP is latched or autorelease: 0 = OCP is a latched fault 1 = OCP is an autorelease fault
				1	FORCED_OL_EN	0x0	Forced OL enable: 0 = disabled 1 = enabled
				2	FORCED_OL_MODE_SEL	0x0	Forced OL mode select: 0 = torque 1 = power
				5:3	FORCED_OL_HYST	0x0	Forced OL torque/power hysteresis; 0.78125 × N% of maximum command
				6	ROSC_EXT_DIS	0x0	Disconnects external resistor from base OSC block, and connects digital test/debug input buffer; typical application configuration is ROSC_EXT_DIS = 0 (enabled, base RCO fully operational)
				7	NBRAKE_IN_DIS	0x0	Disables brake request via pin functionality: 0 = enabled 1 = disabled
				8	IPUP_NFLT_DIS	0x0	Internal pull-up resistor on nFLT pin disable: 0 = enabled 1 = disabled
				9	IPUP_FGRD_DIS	0x0	Internal pull-up resistor on FG/RD pin disable: 0 = enabled 1 = disabled
				10	IPUP_PWMSPD_DIS	0x0	Internal pull-up resistor on PWM/SPD pin disable: 0 = enabled 1 = disabled
				11	IPUP_NBRAKE_DIS	0x0	Internal pull-up resistor on nBRAKE pin disable: 0 = enabled 1 = disabled
				12	IPUP_DIR_DIS	0x0	Internal pull-up resistor on DIR pin disable: 0 = enabled 1 = disabled
				13	IPUP_SCLSEL_DIS	0x0	Internal pull-up resistor on SCLSEL pin disable: 0 = enabled 1 = disabled
				16:14	OVP_TH	0x0	Overvoltage protection threshold: 80 V – N × 5 V
				17	OVP_ENABLE	0x0	Overvoltage protection enable: 0 = disabled 1 = enabled
				18	EN_PWMSPD_FILT	0x0	PWM/SPD pin filter enable: 0 = disabled 1 = enabled
				20:19	OCP_BLANK_TIME	0x0	Overcurrent protection VDS comparator blanking time: (N + 1) × 800 ns
				22:21	OCP_TH	0x0	Overcurrent protection VDS comparator threshold: 0 = 0.5 V 1 = 0.75 V 2 = 1 V 3 = 1.5 V
				24:23	OCP_DEB_TIME	0x0	Overcurrent protection VDS comparator debounce time: 0 = 10 × t_{clk} 1 = 18 × t_{clk} 2 = 25 × t_{clk} 3 = 32 × t_{clk}
				25	OCP_ENABLE	0x0	Overcurrent protection enable: 0 = disabled 1 = enabled
				27:26	UVS_TH	0x0	Undervoltage shutdown threshold: 0 = 32 V 1 = 25 V 2 = 7 V
				28	UVS_DISABLE	0x0	Undervoltage shutdown disable: 0 = enabled 1 = disabled
				29	OVT_DISABLE	0x0	Overtemperature shutdown disable: 0 = enabled 1 = disabled
				30	NO_DRIVE_TELEMETRY_DIS	0x0	Disable telemetry measurements when motor is not being driven: 0 = enabled 1 = disabled
				31	I2C_RESPONSE_MODE	0x0	I²C protocol response mode: 0 = in frame 1 = out of frame

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4CD	46D	13	13	1	BOOTSTRAP_PRECHARGE_THETA_CORRECTION_EN	0x0	Bootstrap precharge theta correction feature enable: 0 = disabled 1 = enabled
				2	BOOTSTRAP_PRECHARGE_DRIVER_AMPUP_EN	0x0	Bootstrap precharge procedure performed before start of ramp-up or drive: 0 = disabled 1 = enabled
				3	BOOTSTRAP_PRECHARGE_BRAKE_EN	0x0	Bootstrap precharge procedure performed before brake is applied: 0 = disabled 1 = enabled
				10:4	FORCED_OL_CMD_REF	0x0	Forced OL torque/power command: 0 = not applied 1..127 = [25 + 0.5859375 × (N + 1)]% of maximum command
				16:11	FORCED_OL_TH	0x0	Forced OL torque/power threshold: Inversion disabled = [50 + 0.78125 × (N + 1)]% of maximum command Inversion enabled = [50 – 0.78125 × (N + 1)]% of maximum command
				20:17	ROT_STALL_TOO_LOW_VBEMF_TH	0x0	Stall detection BEMF low threshold: (N + 1) × 0.78125% of [1.1547 × (nominal voltage/2) × (I_q/maximum current)]
				23:21	ROT_STALL_DET_CTRL	0x0	Rotor stall detection control: 0th bit = V_q estimate 1st bit = frequency estimate 2nd bit = BEMF Rotor stall detection control settings: 0 = disabled 1:7 = combination of stall detection options
				25:24	ROT_STALL_BLANK_DUR	0x0	Rotor stall blanking time duration: [(rotor synchronization timeout)/2^N]
				29:26	ROT_SYNC_TOUT	0x0	Rotor synchronization timeout, in amount of VCL updates: $2^{(N + 8)}$
				30	NFLT_DIS	0x0	Disables fault indication via pin functionality: 0 = enabled 1 = disabled
				31	NFLT_STARTUP_DIS	0x0	Pull nFLT to zero during startup: 0 = enable 1 = disable
4CE	46E	14	14	5:2	ROT_STALL_DET_TIME_TH	0x0	Rotor stall detection time threshold, in amount of VCL updates: $2^{(N + 6)}$
				8:6	ROT_STALL_DET_HIGH_TH	0x0	Rotor stall detection high threshold: 100% + (N + 1) × 12.5%
				11:9	ROT_STALL_DET_LOW_TH	0x0	Rotor stall detection low threshold: (N + 1) × 12.5%
				15:12	ROT_STALL_TOO_LOW_SPEED_TH	0x0	Rotor stall too low speed threshold: (N + 1) × 0.09765625% of maximum (system) speed
				31:16	CUSTOMER_PASSWORD	0x0	Customer EEPROM password, 16 bit: 0x0000 and 0xFFFF are invalid password options (used to disable password protection)
4CF	46F	15	15	11:0	SFOC_RS	0x0	Stator resistance, unitless
				14:12	SFOC_RS_FL	0x0	Stator resistance FL (signed), 6 + N
				27:16	SFOC_KE	0x0	Motor electrical constant, unitless
				30:28	SFOC_KE_FL	0x0	Motor electrical constant FL (signed), 8 + N
4D0	470	16	16	2:0	EXT_CMD_FILTER_TAU	0x0	External command filter time constant, $2^{(14 – N)}$ samples: 0 = disabled
				3	ROT_DIR_INVERT	0x0	Rotation direction inversion: 0 = no inversion 1 = inversion
				4	EXT_CMD_AVERAGE_EN	0x0	External command average enable: 0 = disabled 1 = enabled
				7:5	STAT_START_ADVANCE_ANGLE	0x0	Stationary-start rotor-advance angle: N × 5.625°
				17:8	THETA_FREQ_CORRECTION	0x0	Signed 10-bit calibration offset for the initial theta calculation
				20:18	WNDML_START_ADVANCE_ANGLE	0x0	Windmill-start rotor-advance angle: N × 5.625°
				22:21	ALIGN_START_ANGLE	0x0	Align-start rotor angle: N × 16.875°
				23	BOOTSTRAP_PRECHARGE_DURATION	0x0	Duration of bootstrap precharge procedure performed before start from stationary position: 0 = 36 µs 1 = 72 µs
				31:24	SHI1_COMP	0x0	Single-shunt I1 current compensation: 2 × N

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4D1	471	17	17	0	BRAKE_TYPE	0x0	Brake type: 0 = low-side FET 1 = constant current
				2	BRAKE_IN_REVERSE_TYPE	0x0	Brake in reverse type: 0 = FOC decelerate 1 = brake
				3	BRAKE_IN_WNDML_ALWAYS_EN	0x0	Brake in windmill always enable: 0 = disabled 1 = enabled
				4	BRAKE_IF_OFF_EN	0x0	Brake if off enable: 0 = disabled 1 = enabled
				7:5	BRAKE_SEQ_LENGTH	0x0	Brake sequence length: $2^{(N+1)} - 1$
				10:8	BRAKE_FET_PULSE_AMOUNT	0x0	Brake by FET pulses amount: $2^{(N+1)}$
				13:11	BRAKE_FET_ON_DURATION	0x0	Brake by FET on duration: $(2^N) \times 11.24$ µs
				15:14	BRAKE_FET_OFF_DURATION	0x0	Brake by FET off duration: N × BRAKE_FET_ON_DURATION
				20:16	BRAKE_FREQUENCY_TOO_HIGH_TH	0x0	Brake frequency too high threshold: (N + 1) × 3.125% of maximum (system) speed
				23:21	BRAKE_FREQUENCY_TOO_HIGH_COAST_TIME	0x0	Brake frequency too high coast time: $2^{(N+1)}$ of system-timer interrupts
				25:24	STRONG_ALGN_CURR_GAIN	0x0	Align current reference gain in brake in windmill condition: N + 1
				28:26	ROT_STALL_DET_TIME_REVERSE	0x0	Additional rotor-stall detection time while in reverse, in amount of V_{CL} updates: $2^{(N+6)}$
				31:29	UVLO_BLANK_TIME	0x0	Undervoltage-lockout blanking time: 37 × (2^N) times the V_{CL} update rate
4D2	472	18	18	6:0	STPD_TH	0x0	Stopped threshold, below which this speed level, the rotor is considered stationary: (N + 1) × 0.0244140625% of maximum (system) speed
				9:7	PO_OPER	0x0	Position observer operational, below which speed, the position observer operates unreliably: (N + 1) × 0.1953125% of maximum (system) speed
				15:10	DEFAULT_EXT_CMD	0x0	Default external command value: N × 1.5625% of maximum command
				21:16	CMD_ON_TH	0x0	Command on threshold: (N + 1) × 0.390625% of maximum command
				27:22	CMD_OFF_TH	0x0	Command off threshold: N × 0.390625% of maximum command
				28	RESERVED	0x0	Reserved
				30:29	RESERVED	0x0	Reserved
				31	SOFT_OFF_BRAKE_EN	0x0	Soft-off brake enable: 0 = disabled 1 = enabled

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4D3	473	19	19	2:0	SFOC_DECEL_OL_SPEED_TH	0x0	Deceleration open-loop speed threshold: (N + 1) × 0.390625% of maximum (system) speed
				3	SOFT_OFF_EN	0x0	Soft-off enable: 0 = disabled 1 = enabled
				9:4	SOFT_OFF_FREQUENCY_TH	0x0	Soft-off frequency threshold: (N + 1) × 0.1953125% of maximum (system) speed
				11:10	PIN_DIR_D_EB	0x0	DIR pin debounce time 0 = 0 ns 1 = 840 ns 2 = 12.76 µs 3 = 127.6 µs
				13:12	PIN_NBRAKE_D_EB	0x0	nBRAKE pin debounce time: 0 = 0 ns 1 = 840 ns 2 = 12.76 µs 3 = 127.6 µs
				14	DEFAULT_NBRAKE	0x0	Default nBRAKE bit value (inverse): 0 = no brake 1 = brake
				19:15	SFOC_DECEL_RATE	0x0	Deceleration rate: 0.0244140625% of maximum (system) speed during (N + 1) × 32 VCL updates
				24:20	SFOC_DECEL_OL_D_CURR_REF	0x0	Deceleration open-loop D current reference: (N + 1) × 3.125%of maximum current
				29:25	RESERVED	0x0	Reserved
				30	SFOC_QUIET_START_EN	0x0	Enable quiet start: 0 = disabled 1 = enabled
				31	SFOC_SOFT_START_EN	0x0	Enable soft start: 0 = disabled 1 = enabled
4D4	474	20	20	6:0	OVVL_VOLT_TH	0x0	Overvoltage variable limiter voltage threshold: 7.21875 V + N × 1.03125 V
				14:7	OVVL_VAR_LMT	0x0	Overvoltage variable limiter, variable limit: (N + 1) × 0.390625% of maximum variable value
				15	OVVL_ENABLE	0x0	Overvoltage variable limiter enable: 0 = disabled 1 = enabled
				22:16	ROT_START_RETRY_TOUT	0x0	Rotor start retry timeout: N of system timer interrupts
				26:23	ROT_START_RETRY_MAX_ATTEMPTS	0x0	Rotor start retry maximum attempts: 0 = infinite number of attempts 1:15 = N attempts
				27	CLK_COMP_ENABLE	0x0	Clock-compensation feature enable
				31:28	CLK_COMP_REF	0x0	Clock-compensation carrier frequency: 0 = 88.9 Hz 1 = 133.3 Hz 2 = 177.7 Hz 3 = 222.2 Hz 4 = 266.7 Hz 5 = 311.1 Hz 6 = 355.5 Hz 7 = 400 Hz 8 = 444.4 Hz 9 = 488.9 Hz 10 = 533.3 Hz 11 = 577.8 Hz 12 = 622.2 Hz 13 = 666.7 Hz 14 = 711.1 Hz 15 = 888.9 Hz

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C EEPROM NVM Register (Hex)	I²C Shadow Register (Hex)	EE Address (Hex)	NVM	Bits	Name	Default	Description
4D5	475	21	21	11:0	SENSE_RESISTOR_VAL	0x0	Sense-resistor value: [(N + 1) × 500/(2^{12})] mΩ; reserved for GUI use
				17:13	SFOCSTARTCURRLMT	0x0	Phase current limit at the transition to the closed-loop: (N + 1) × 3.125% of maximum current
				20:18	SFOCSOFTSTARTTIME	0x0	Soft start time: 256 × (N + 1) VCL updates
				23:21	SFOCQUIETSTARTTIME	0x0	Quiet start (OL→CL transition) duration: 512 × (N + 1) VCL updates
				27:24	SFOCDRVCURRRATELMT	0x0	Current rate limit in drive mode: [$2^{(N + 11)}$ × 0.745 µ%] of maximum current per VCL update
				31:28	SFOCGENCURRRATELMT	0x0	Current rate limit in generator mode: [$2^{(N + 11)}$ × 0.745 µ%] of maximum current per VCL update
4D6	476	22	22	15:0	UCC_X0	0x0	UCC: × point 0
				31:16	UCC_X1	0x0	UCC: × point 1
4D7	477	23	23	15:0	UCC_X2	0x0	UCC: × point 2
				31:16	UCC_X3	0x0	UCC: × point 3
4D8	478	24	24	15:0	UCC_X4	0x0	UCC: × point 4
				31:16	UCC_X5	0x0	UCC: × point 5
4D9	479	25	25	15:0	UCC_X6	0x0	UCC: × point 6
				31:16	UCC_X7	0x0	UCC: × point 7
4DA	47A	26	26	15:0	UCC_X8	0x0	UCC: × point 8
				31:16	UCC_X9	0x0	UCC: × point 9
4DB	47B	27	27	15:0	UCC_Y0	0x0	UCC: Y point 0
				31:16	UCC_Y1	0x0	UCC: Y point 1
4DC	47C	28	28	15:0	UCC_Y2	0x0	UCC: Y point 2
				31:16	UCC_Y3	0x0	UCC: Y point 3
4DD	47D	29	29	15:0	UCC_Y4	0x0	UCC: Y point 4
				31:16	UCC_Y5	0x0	UCC: Y point 5
4DE	47E	30	30	15:0	UCC_Y6	0x0	UCC: Y point 6
				31:16	UCC_Y7	0x0	UCC: Y point 7
4DF	47F	31	31	15:0	UCC_Y8	0x0	UCC: Y point 8
				31:16	UCC_Y9	0x0	UCC: Y point 9

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

USER REGISTERS

Registers not shown are not for user access. Any change to a value in the undocumented registers may cause a malfunction or damage to the part.

I²C Address (Hex)	Field Name	Bits	Read/Write [1]	Default Value	Description
0x0	REG: SW_STATUS	31:0	RO	0x0	Refer to the SW Status Register, SW_STATUS section
0x1	REG: REF_CMD	16:0	RW	0x0	Refer to the I²C Command Register, REF_CMD section
0x2	REG: BRAKE_CTRL	0:0	RW	0x0	0 = brake is applied (via register or via nBRAKE pin) 1 = brake is not applied

[1] RO = Read-Only; RW = Read/Write

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SW Status Register, SW_STATUS

The software status read-only register at address (0x0000) contains the motor control mode, state, fault, and status flags.

Address 0x0000, Read-Only				
Variable Name	**Bits**	**Size**	**Type**	**Description**
Controller Mode				
MCA_MODE	7:0	8 bits	MC_MODE_T	Motor control mode OFF_MC_MODE STANDBY_MC_MODE ROTATE_MC_MODE BRAKE_MC_MODE FAIL_MC_MODE DEBUG_MC_MODE
Controller State				
MCA_FSMSTATE	15:8	8 bits	MC_FSMSTATE_T	Motor control FSM state IDLE_MC_FSMSTATE SBY_MC_FSMSTATE WNDML_MC_FSMSTATE BRAKE_MC_FSMSTATE FAIL_MC_FSMSTATE IPDORALIGN_MC_FSMSTATE RAMPUP_MC_FSMSTATE DRIVE_MC_FSMSTATE
Fault Status				
OV	16	1 bit	fault/status flag	Over voltage
UV	17	1 bit	fault/status flag	Under voltage
OT	18	1 bit	fault/status flag	Over temperature
OC	19	1 bit	fault/status flag	Over current latch
EE	20	1 bit	fault/status flag	EEPROM error
RS	21	1 bit	fault/status flag	Rotor stalled latch
NMS	22	1 bit	fault/status flag	No-motor start detection
OK	23	1 bit	fault/status flag	System OK
Motor Control Status				
VQ_LIM	24	1 bit	fault/status flag	V_q limit
VD_LIM	25	1 bit	fault/status flag	V_d limit
SPD_LIM	26	1 bit	fault/status flag	Speed limit
PWR_LIM	27	1 bit	fault/status flag	Power limit
VGEN_LIM	28	1 bit	fault/status flag	Voltage (generator mode) limit
OVV_LIM	29	1 bit	fault/status flag	Over voltage variable limit
ROT_SYNC	30	1 bit	fault/status flag	Rotor synchronized
[Reserved (zero)]	31	1 bit	zero	Reserved—reads as zero

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

I²C Command Register, REF_CMD

This register is used with the I²C external command source to set the demand value and to control the motor direction.

I²C Address (Hex)	Bits	Value	Name	Description
0001	15:0	[0 … 32767]	demand	Sets the speed control demand
	16	[0 … 1]	direction	Sets the motor spin direction

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SW FIXED-ADDRESS VARIABLES

With I²C, it is possible to access status variables that reside at fixed addresses. Addresses of these variables, their types, and sizes are provided in the table that follows.

Variable Name	Address	Size	Type	Description
MPCI_VALUE	0x03850x0E14	4B	UINT32_T	Interface variable of multi-purpose control interface (MPCI): Bits [15:0] = Data written into MPCI Bits [31:16] = MPCI Instruction (code of functionality to execute)
MCA_THETA	0x03E186 [LSB, 15:0]	2B	INT16	Start rotor position, 9-bit resolution (0.3515625° per bit): –512 (sign extended to 16 bits) = –180° 511 = 179.99° 0 = 0°
MCA_FREQ	0x03860x0E1A [MSB, 31:16]	2B	INT16	Start rotor frequency, SFOC_FREQ_RES (NVM parameter) resolution, sign represents rotation direction: Negative = Clockwise Positive = Counterclockwise Zero = Stationary
MCA_COMMAND	0x03870x0E1C [LSB, 15:0]	2B	INT16	Current value of command after UCC; 15-bit resolution, signed: –32768 = Maximum negative command (–100%) 32767 = Maximum positive command (99.99%) 0 = 0 command (0%)
IPD_ERRSTATUS	0x03870x0E1E [bit position, 23:26]	1B	IPD_ERRSTATUS_T	IPD execution status: 0 = OK (IPD finished successfully) 1 = STG1_ERROR_INDUCT_EQUAL_IPD 2 = STG2_ERROR_TIMEOUT_IPD 3 = STG2_ERROR_EQUAL_SATURATION_IPD
WNDML_ERRSTATUS	0x03870x0E1F [MSB, 31:24]	1B	WNDMLERRSTATUS_T	Windmill execution status: 0 = OK (windmill completed successfully) ERR_BEMF_SEQUENCE_WNDML ERR_BEMF_VALUE_WNDML
MCA_EXTCMD	0x03880x0E22 [LSB, 15:0]	2B	UINT16	Input of the curve transformer
V_BUS	0x03E28A [LSB, 15:0]	2B	UINT16	V_{BB} voltage: V_{BB} = (value) × [(2 × 1.2/4096) × 40] [V]
V_CMD	0x038E2A [MSB, 31:16]	2B	UINT16	Voltage command, 12-bit resolution
I_BUS	0x038B0x0E2C [LSB, 15:0]	2B	INT16	I_{BB} current, signed: I_{BB} = 1.5 × (value/2048) × (0.57735) × maximum current [A]
FG_FREQ	0x0E38C0	4B	INT32	FG frequency, SFOC_FREQ_RES resolution, sign represents rotation direction: Negative = Clockwise Positive = Counterclockwise Zero = Stationary
VBEMF	0x0E38D4 [LSB, 15:0]	2B	INT16	Back-EMF voltage (available in position-observer closed-loop mode of operation), signed: V_{BEMF} = (value/16384) × (0.57735) × (nominal voltage, V) [V]

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FOC INTERNAL VARIABLES

Variable Name	Address	Size	Type	Description
THETA_EST	0x04A1	4B	INT32	Start rotor position, 9-bit resolution (0.3515625° per bit): –512 (sign extended to 32 bits) = –180° 511 = 179.99° 0 = 0°
FREQ_EST	0x04A0	4B	INT32	Current rotor frequency, SFOC_FREQ_RES resolution, sign represents rotation direction: Negative = Clockwise Positive = Counterclockwise Zero = Stationary
ID	0x04A2	4B	INT32	D-axis current, signed: I_D = (value/2048) × maximum current [A]
IQ	0x04A3	4B	INT32	Q-axis current, signed: I_q = (value/2048) × maximum current [A]
VD	0x04A4	4B	INT32	D-axis voltage, signed: V_d = (value/16384) × (0.57735) × (nominal voltage, V) [V]
VQ	0x04A5	4B	INT32	Q-axis voltage, signed: V_q = (value/16384) × (0.57735) × (nominal voltage, V) [V]
HSD	0x04B1	4B	INT32	D-axis duty cycle, signed: HS_d = (value)/{(PWM period, in clock periods) × [1 + (PWM high-resolution mode, 0/1 if disabled/enabled)] × (0.57735)}, in parts
HSQ	0x04B2	4B	INT32	Q-axis duty cycle, signed: HS_q = (value)/{(PWM period, in clock periods) × [1 + (PWM High Resolution mode, 0/1 if disabled/enabled)] × (0.57735)}, in parts

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PROGRAMMING THE EEPROM

The NVM is read and written using the I²C interface.

I²C SERIAL INTERFACE

The A89333 uses a standard fast-mode I²C serial port format to program the EEPROM or to control the IC operation serially. With the help of the GUI, the user can adjust configuration register values for a particular application before programming these parameters into EEPROM. The A89333 7-bit peripheral address is 0x55.

The I²C interface shares pins with PWM/SPD or FG/RD. The PWM/SPD pin functions as the clock (SCL) input, and the FG/RD pin is the data line (SDA). A special sequence is not needed to begin transferring data. If the motor is running, the FG may pull the data line low while trying to initialize in serial port mode. Once an I²C command is sent, the PWM input is ignored. For more information, refer to the VBB, UV, and NVM Reprogramming section.

Because RD is typically low when faults are not present, if the FG/RD option is set to RD, the establishment of an I²C communication requires the RD pull-down to be disabled by reducing V_{BB} to less than V_{BBUVLO}. For more information, refer to the VBB, UV, and NVM Reprogramming section.

I²C Timing Diagrams

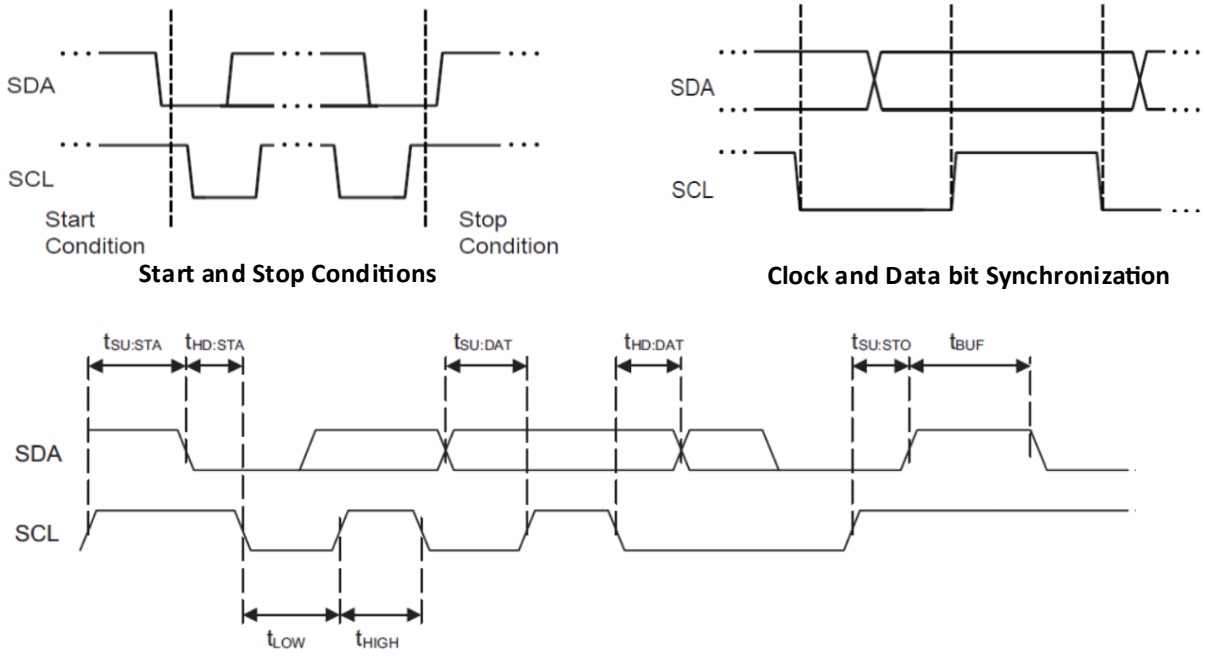


Figure 19: I²C-Compatible Timing Requirements

READ PROCEDURE

1. Start condition

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

2. (1 byte) 7-bit I²C peripheral address (device ID) 1010101, R/W bit = 1
3. (1 byte) Fixed bit = 1, bits [6:0] of the internal register address
4. (1 byte) Fixed bit = 1, bits [13:7] of the internal register address
5. (4 bytes) read four data bytes, least significant byte first, the last byte should be NACK'd by the controller
6. Stop condition

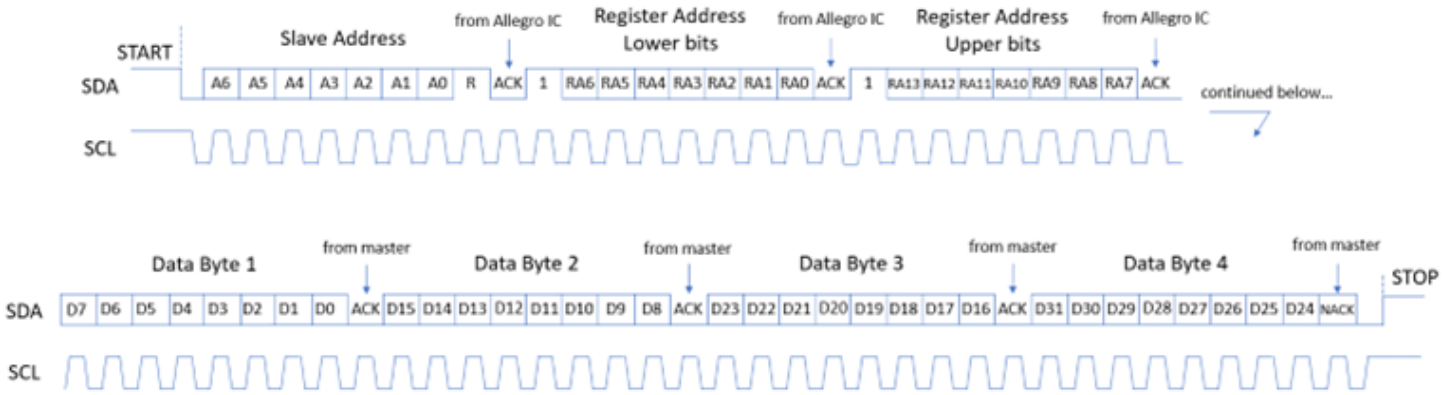


Figure 20: Read Procedure

WRITE PROCEDURE

1. Start condition
2. (1 byte) 7-bit I²C peripheral address (device ID) 1010101, R/W Bit = 0
3. (1 byte) Fixed bit = 1, bits [6:0] of the internal register address
4. (1 byte) Fixed bit = 1, bits [13:7] of the internal register address
5. (4 bytes) four data bytes, least significant byte first
6. Stop condition

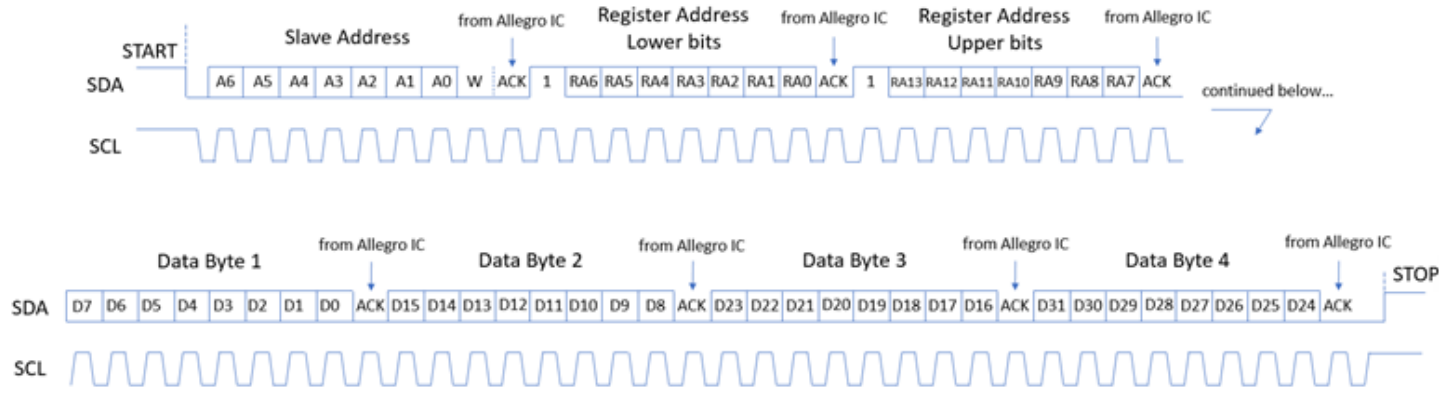


Figure 21: Write Procedure

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Operation Modes and Customer Password Protection

A89333 implements customer password protection of I²C access to certain regions of memory space—foremost, the copy of customer settings in shadow registers.

The A89333 operation modes are:

Name	Description
Application Mode (AM)	I²C has access to user registers and fixed-address variables Default mode after power up
User Mode (UM)	I²C has access to user registers, fixed-address variables, FOC internal variables, shadow registers, and NVM EEPROM configuration registers

The password length is 16 bits, and the password is set by the customer by configuring the corresponding parameter (CUSTOMER_PASSWORD) in the NVM. (Alternatively, the password can be set by Allegro, upon first-part configuration.)

All combinations other than 0x0000 and 0xFFFF are considered valid passwords.

If a password combination is set to 0x0000 or 0xFFFF, the customer password is not configured and the part enters user mode after POR. In this way, when the part arrives, the customer has access to NVM EEPROM to set the user mode password (by configuring the corresponding parameter, CUSTOMER_PASSWORD, in NVM). Once the user mode password is configured, the part enters application mode after POR and the EEPROM NVM and shadow registers are protected.

To change the operation mode, write to the MPCI_VALUE_GLOBAL variable via the I²C 32-bit frame. The variable (MPCI_VALUE_GLOBAL) consists of two parts, each 16 bits wide:

1. Instruction code is contained in the MSBs [31:16]; the instruction code for the customer password check is 0x01.
2. Data (i.e., password combination) is contained in the LSBs [15:0].

Functionality	Instruction Code	Example of Transaction Content Value [1]	Execution
Customer Password Check	0x01	Bits [31:16] = 0x01, instruction code Bits [15:0], password to be entered	The device acknowledges Customer password entry by rewriting Instruction code and Data (bits [31:0]) with zero (0x00) and performs password check. Customer password entry and check can be executed in any state of the motor controller.

[1] This is the value written into the MPCI_VALUE_GLOBAL variable via the I²C 32-bit frame.

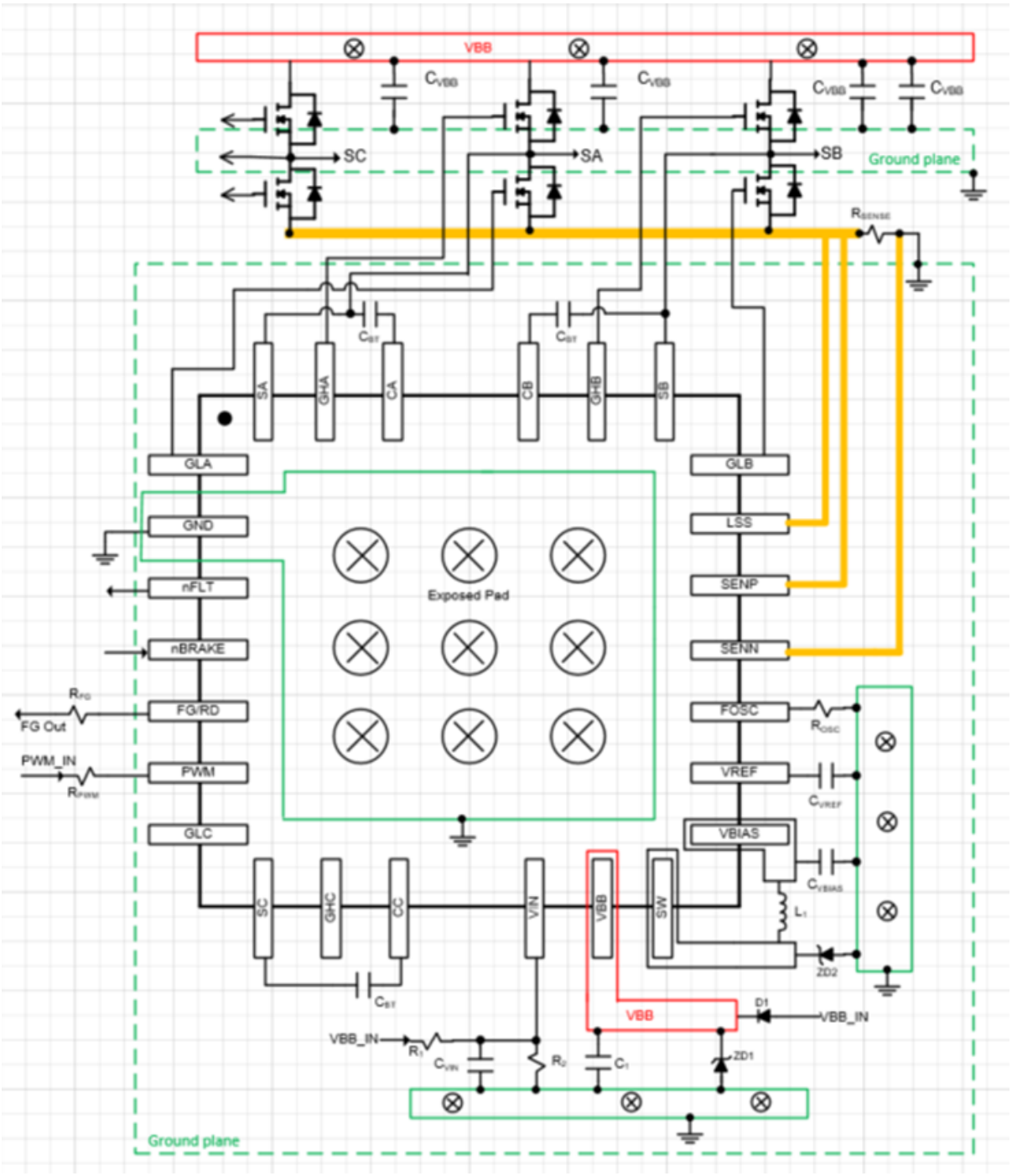
If a valid customer password is configured, the controller remains in the application operation mode, where user registers and fixed-address variables can be accessed, until the configured password is correctly entered with MPCI_VALUE_GLOBAL.

Once the password is entered correctly, the controller enters the user operation mode and the following configuration registers can be accessed: user registers, fixed-address variables, FOC internal variables, shadow registers, and NVM EEPROM.

If an incorrect combination is entered three times in a row using MPCI_VALUE_GLOBAL, the controller must be rebooted (by POR) before further checks of the customer password can be performed.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

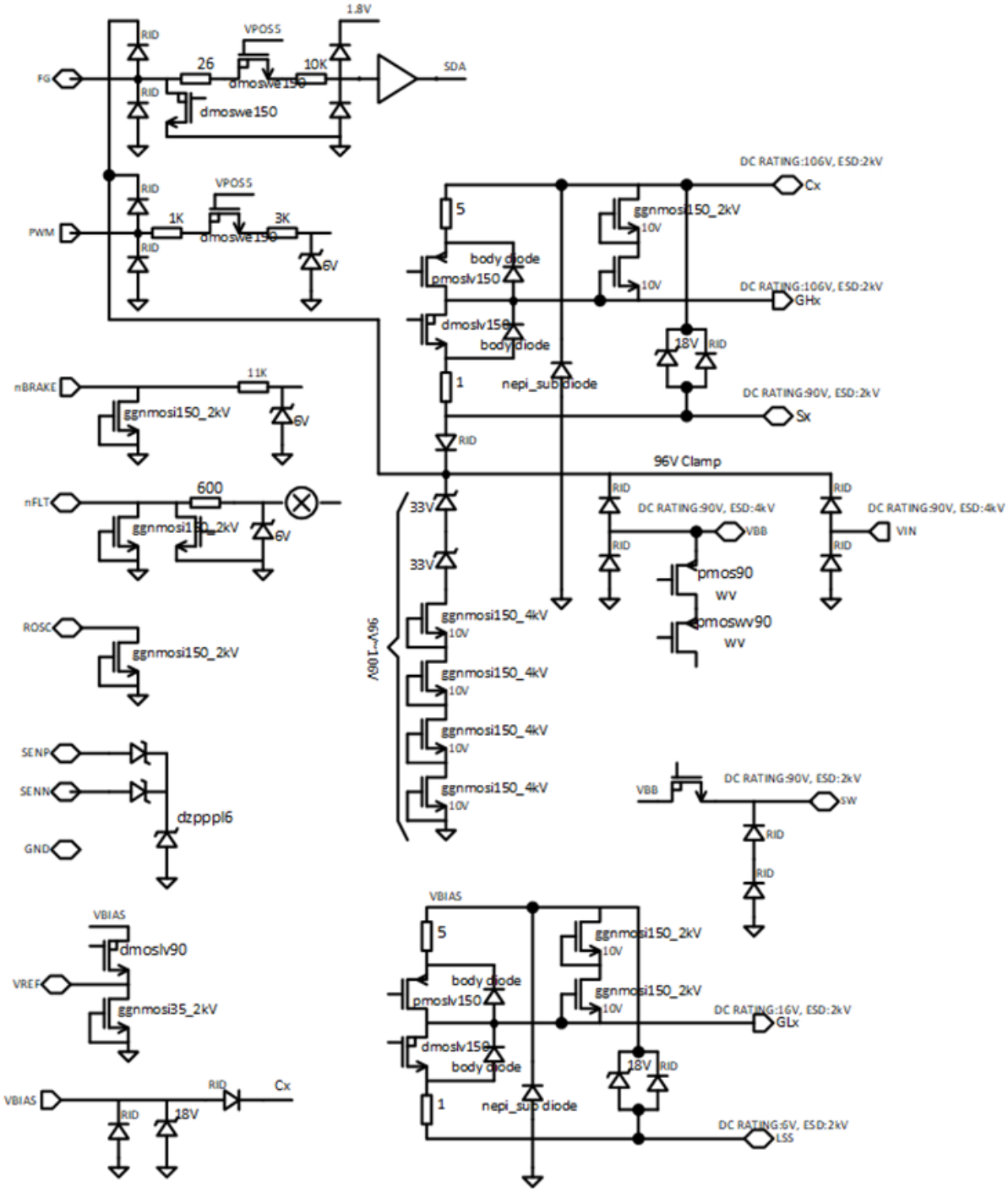
Name	Suggested	Comment
C_{VREF}	4.7 µF/X5R/10 V	Ceramic capacitor required
C_{VBB}	10 µF – 47 µF/100 V	Power-supply stabilization; electrolytic or ceramic OK
R_{PU}, R_{FGPU}	10 kΩ	Pull-up resistors to VREF
C_{BT}	0.22 µF/50 V	Bootstrap capacitor, ceramic capacitor required
C_{VBIAS}	10 µF/25 V	Ceramic capacitor required
C1	0.1 – 0.47 µF/100 V	Ceramic capacitor required
D1	HSM8100JE3/TR13	Required to isolate motor for reverse-polarity protection
ZD1	SMBJ48A	TVS to limit maximum V_{BB} due to transients due to motor generation on power line
L1	10 µH (994-PFL4514-103MEC)	Higher value of inductor can also be used; ensure inductor is not saturated
ZD2	SDM1100LP-7	Schottky diode required; ensure current rating is high enough to handle the inductor current
R_{FG}, R_{PWM}	500 Ω	Isolate IC pins from noise or overvoltage transients or protect from connector issues
R_{OSC}	25 kΩ ± 0.1%	Required for better oscillator accuracy
R_{sense}	100 mΩ ± 1%	Current sense resistor and value depends on the maximum current of the system
R1	10 kΩ	Required for reverse polarity protection VIN pin
R2	10 kΩ	Pull-down for VIN
C_{VIN}	0.1 µF	Noise filter for hot-swap events

LAYOUT NOTES

1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place R_{sense} close to the bridge and use Kelvin sensing.
4. Place C_{VREF} and C1 as close as practical to the IC, connected to the GND plane.
5. Place L1, ZD2 and C_{VBIAS} as close as practical to the IC, connected to the GND plane.
6. Place C_{BT} as close as practical to the IC.
7. Place C_{VBB} close to the V_{BB} power rail of the external FETs.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

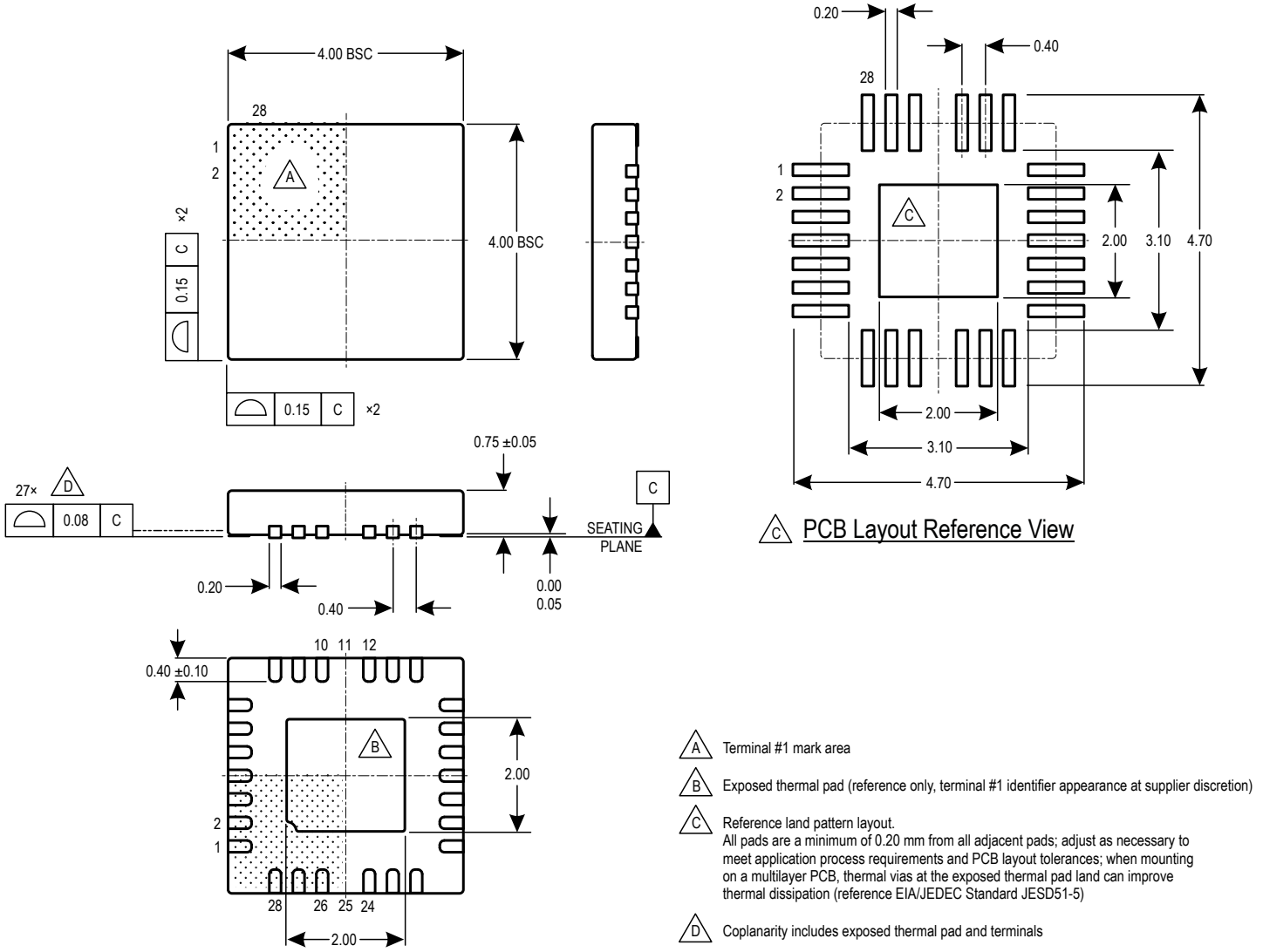
PIN DIAGRAM



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222, Rev. 4)
NOT TO SCALE
All dimensions nominal unless otherwise stated – Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout.
All pads are a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 22: EC Package, 28-Pin QFN with Exposed Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	July 24, 2024	Initial release
1	October 25, 2024	Updated Speed Setpoint and System Oscillator characteristic values (page 7)
2	January 31, 2025	Updated PWM/SPD section (page 8)
3	March 26, 2025	Updated features and benefits (page 1), V_{BB} (changed from 75 V to 90 V) (pages 1, 3, and 5), power loss brake characteristics (page 6), speed control characteristics (page 7), PWM duty cycle description (page 11), FOC algorithm speed and current loop example (page 20), and V_{BB} overvoltage detection description (page 22)
4	May 26, 2026	Removed FG/RD condition from internal pull-up Voltage and resistor characteristics (page 6) and modified FG/RD description (page 8)
5	September 1, 2026	Removed FG ID pattern generation feature (page 24), removed BEMF compensation feature (page 26), added AC loss function feature (page 28), modified Registers and Nonvolatile Memory (NVM) Map section (pages 29 – 38), modified SW Fixed-Address Variables section (page 42), and made minor editorial corrections (pages 13, 14, 25, and 28)

Copyright 2026, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:
www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com