

SD9650 OVERVIEW

The SD9650 uses a multistage pipeline architecture to provide 16-bit accuracy at 65MSps data rates over the full operating temperature range.

The SD9650 features internal references and can operate without an external reference or external common-mode bias.

The device can be set to operate using either CMOS or LVDS output data formats. Programming for configuration and control is accomplished using a 3-wire SPI-compatible interface. The digital output data can be programmed to be delivered in offset binary, gray code, or twos complement format. Further, to decrease EMI, the output data can be scrambled. A data output clock (DCO+/DCO-) is provided for each ADC channel to ensure proper timing at the receiver.

FEATURES

- SNR: 76.2dBFS at $f_{IN} = 30.2\text{MHz}$ at $f_s = 65\text{MSps}$
- SFDR: 91.0dBc at $f_{IN} = 30.2\text{MHz}$ at $f_s = 65\text{MSps}$
- -155.2dBFS/Hz input-noise at $f_{IN} = 30.2\text{MHz}$ at $f_s = 65\text{MSps}$
- 2.0V_{p-p} nominal input
- Typical power consumption: 339mW at 65MSps
- Integer 1-to-8 input clock divider (520MHz maximum input)
- Sample rates of up to 65MSps
- 1.8V analog supply voltage
- LVDS (ANSI-644 levels) outputs
- Internal ADC voltage reference
- ADC clock duty cycle correction
- Serial port control
- Energy saving power-down modes

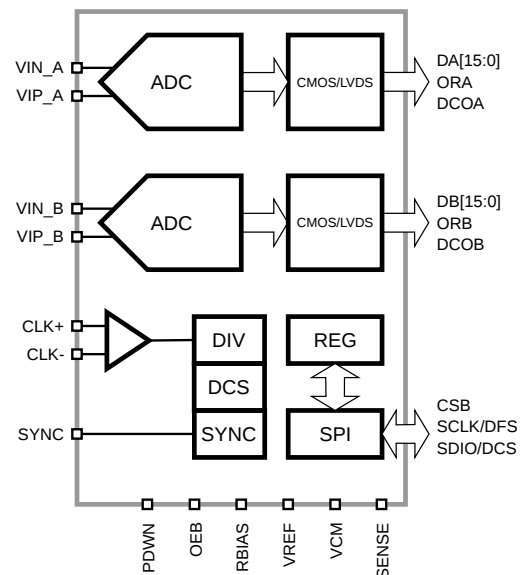


Figure 1: SD9650 Functional Block Diagram.

APPLICATIONS

- Communications
- General-purpose software radios
- I/Q demodulation systems
- Diversity radio systems
- Smart antenna systems
- Multimode digital receivers
- Ultrasound equipment
- Radar/LiDAR applications
- Test and Measurement

Table of Contents

SPECIFICATIONS	1
DC Specifications	1
AC Specifications	2
Digital Specification	3
Switching Specifications	5
ABSOLUTE MAXIMUM RATINGS	7
PACKAGE	8
TYPICAL PERFORMANCE CHARACTERISTICS	12
EQUIVALENT CIRCUITS	14
THEORY OF OPERATION.....	16
ADC Architecture	16
Stand-by and Power-Down Modes	17
Pin Functions	17
SERIAL PORT INTERFACE.....	19
OUTPUT MODE	21
Data Scrambler	21
Alternate Bit Polarity.....	21
Output Test Modes	21
CONTROL REGISTERS.....	23
ORDERING INFORMATION	29
PACKAGE DRAWING.....	30
REVISION HISTORY	31

SPECIFICATIONS

DC Specifications

At $T_A = 25^\circ\text{C}$, $V_{AVDD} = 1.8\text{V}$, $V_{DRVDD} = 1.8\text{V}$, $F_{CLK} = 65\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled sine wave external clock source, LVDS mode, unless otherwise noted.

Table 1. DC Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Resolution			16		bits
Accuracy					
Offset Error	Full	-0.50		0.50	%FSR
Gain Error	Full		1.50		%FSR
DNL	Full			± 2.9	LSB
INL	Full			± 8.0	LSB
Matching					
Offset Error	25°C	-0.70		0.70	%FSR
Gain Error	25°C		0.75		%FSR
Temperature Drift					
Offset Error	Full		0.05		ppm/ $^\circ\text{C}$
Gain Error	Full		1.50		ppm/ $^\circ\text{C}$
Internal Voltage Reference					
Output Voltage	Full	0.99	1.02	1.05	V
External Voltage Reference					
Range	Full	0.90		1.05	V
Input Referred Noise					
$V_{REF} = 1.0\text{V}$	25°C		3.23		LSB(rms)
Analog Input					
Input Span, $V_{REF} = 1.0\text{V}$	Full		2.0		V
Input Capacitance	Full		6.0		pF
Input Resistance	Full		2.0		k Ω
Input Common-Mode Voltage	Full		0.70		V
Input Common-Mode Range	Full	0.65		0.75	V
VCM Voltage	Full		0.70		V
VCM Current Capability	Full		100		μA
Reference Input Resistance	Full		50		k Ω
Power Supply					
V_{AVDD}	Full	1.7	1.8	1.9	V
V_{DRVDD}	Full	1.7	1.8	1.9	V
$I_{AVDD} @ 1.8\text{V}$	Full		167.0		mA
$I_{DRVDD} @ 1.8\text{V (CMOS)}$	Full		20.0		mA
$I_{DRVDD} @ 1.8\text{V (LVDS)}$	Full		62.0		mA
Power Consumption					
Sine Wave Input	Full		338.6		mW
Standby ¹	Full		55.6		mW
Power Down	Full		8.0		mW

¹ Standby power is measured with a sinewave input and active clock.

AC Specifications

At $T_A = 25^\circ\text{C}$, $V_{AVDD} = 1.8\text{V}$, $V_{DRVDD} = 1.8\text{V}$, $F_{CLK} = 65\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled sine wave external clock source, LVDS mode, unless otherwise noted.

Table 2. AC Specifications.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Signal-to-Noise Ratio (SNR)					
$f_{IN} = 6.55\text{MHz}$	25°C		76.3		dBFS
$f_{IN} = 30.2\text{MHz}$	25°C	75.7	76.2		dBFS
	Full	75.3			dBFS
$f_{IN} = 70.2\text{MHz}$	25°C		75.1		dBFS
$f_{IN} = 220\text{MHz}$	25°C		70.0		dBFS
Signal-to-Noise and Distortion Ratio (SNDR)					
$f_{IN} = 6.55\text{MHz}$	25°C		76.0		dBFS
$f_{IN} = 30.2\text{MHz}$	25°C	75.3	75.8		dBFS
	Full	74.8			dBFS
$f_{IN} = 70.2\text{MHz}$	25°C		74.8		dBFS
$f_{IN} = 220\text{MHz}$	25°C		68.1		dBFS
Effective Number of Bits (ENOB)					
$f_{IN} = 6.55\text{MHz}$	25°C		12.3		bits
$f_{IN} = 30.2\text{MHz}$	25°C		12.3		bits
$f_{IN} = 70.2\text{MHz}$	25°C		12.1		bits
$f_{IN} = 220\text{MHz}$	25°C		11.0		bits
Worst Harmonic Power					
$f_{IN} = 6.55\text{MHz}$	25°C		-93.0		dBc
$f_{IN} = 30.2\text{MHz}$	25°C		-91.0	-85.0	dBc
$f_{IN} = 70.2\text{MHz}$	25°C		-89.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		-72.0		dBc
Worst non-Harmonic Power					
$f_{IN} = 6.55\text{MHz}$	25°C		-95.0		dBc
$f_{IN} = 30.2\text{MHz}$	25°C		-94.0	-88.0	dBc
$f_{IN} = 70.2\text{MHz}$	25°C		-89.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		-79.0		dBc
Spurious-Free Dynamic Range ¹ (SFDR)					
$f_{IN} = 6.55\text{MHz}$	25°C		93.0		dBc
$f_{IN} = 30.2\text{MHz}$	25°C	85.0	91.0		dBc
	Full	84.0			dBc
$f_{IN} = 70.2\text{MHz}$	25°C		89.0		dBc
$f_{IN} = 220\text{MHz}$	25°C		72.0		dBc
Two-Tone SFDR					
$f_{IN1} = 29.1\text{MHz}$, $f_{IN2} = 30.6\text{MHz}$	25°C		89.5		MHz
Crosstalk ²	25°C		-105.0		dBc
Analog Input Bandwidth	Full		650.0		MHz

¹ SFDR excludes the DC and $f_s/2$ bins.

² Crosstalk is measured at 100MHz with -1.0dBFS on one channel and no input on the alternate channel.

Digital Specification

$V_{AVDD} = 1.8V$, $V_{DRVDD} = 1.8V$, $F_{CLK} = 65MHz$, $A_{IN} = -1dBFS$, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.

Table 3. Differential Clock Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full	CMOS/LVDS/LVPECL			
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V _{p-p}
Input Voltage Range	Full	$V_{AGND}-0.3$		$V_{AVDD}+0.2$	V
Input Common-Mode Range	Full	0.75		1.05	V
High Level Input Current	Full	-10		10	μA
Low Level Input Current	Full	-10		10	μA
Input Capacitance	Full		1.7		pF
Input Resistance	Full		6		kΩ

Table 4. SYNC Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Logic Compliance	Full		CMOS		
Input Voltage Range	Full	V_{AGND}		V_{AVDD}	V
High Level Input Voltage	Full	1.22		V_{AVDD}	V
Low Level Input Voltage	Full	V_{AGND}		0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		100		kΩ

Table 5. CSB Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		15		kΩ

Table 6. SCLK/DFS Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		15		kΩ

Table 7. SDIO/DCS Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		15		kΩ

Table 8. OEB Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		15		kΩ

Table 9. PDWN Input.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
High Level Input Voltage	Full	1.22			V
Low Level Input Voltage	Full			0.6	V
High Level Input Current	Full	-1		1	μA
Low Level Input Current	Full	-1		1	μA
Input Capacitance	Full		1.5		pF
Input Resistance	Full		15		kΩ

Table 10. CMOS Outputs (DATA and OR).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
DRVDD = 1.8V					
High Level Output Voltage @50μA	Full	1.75			V
High Level Output Voltage @0.5mA	Full	1.7			V
Low Level Output Voltage @50μA	Full			0.05	V
Low Level Output Voltage @1.6mA	Full			0.2	V

Table 11. LVDS Outputs (DATA and OR).

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	300	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full		1.13		V
Differential Output Voltage (V_{OD}), Reduced Swing	Full		200		mV
Output Offset Voltage (V_{OS}), Reduced Swing	Full		1.15		V

Switching Specifications

$V_{AVDD} = 1.8V$, $V_{DRVDD} = 1.8V$, $F_{CLK} = 65MHz$, $A_{IN} = -1dBFS$, differential AC-coupled sine wave external clock source, DCS enabled, unless otherwise noted.

Table 12. Clock Input Timing.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
Input Clock Rate	Full			520.0	MHz
Conversion Rate (after clock divider)	Full	3.0		65.0	MHz
CLK Pulse Width High (t_{CH})					
Divide-by-1 Mode, DCS Enabled	Full	1.5			ns
Divide-by-1 Mode, DCS Disabled	Full	6.9	7.7	8.5	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	1.0			ns
Aperture Delay (t_A)	Full		0.5		ns
Aperture Uncertainty (Jitter, t_J)	Full		140.0		fs

Table 13. SYNC Timing Requirements.

PARAMETER	MIN	TYP	MAX	UNIT
Set-Up Time ($t_{S,SYNC}$)		0.35		ns
Hold Time ($t_{H,SYNC}$)		0.35		ns

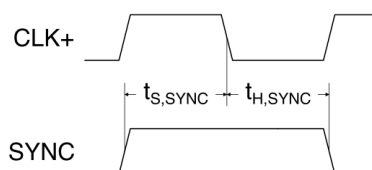


Figure 2: SYNC Input Timing.

Table 14. Data Output.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
CMOS Mode					
Data Propagation Delay (t_{PD})	Full		5.5		ns
DCO Propagation Delay (t_{DCO})	Full		6.5		ns
DCO to Data Skew (t_{SKEW})	Full		-1.0		ns
Pipeline Delay (Latency, L)	Full		35		Cycles
LVDS Mode					
Data Propagation Delay (t_{PD})	Full		7.5		ns
DCO Propagation Delay (t_{DCO})	Full		7.7		ns
DCO to Data Skew (t_{SKEW})	Full		-0.1		ns
Pipeline Delay (Latency, L) Channel A/Channel B	Full		35		Cycles
Wake-Up Time (from sleep)	Full		5		μs
Wake-Up Time (from power down)	Full		500.0		μs
Out-of-Range Recovery Time	Full		3		Cycles

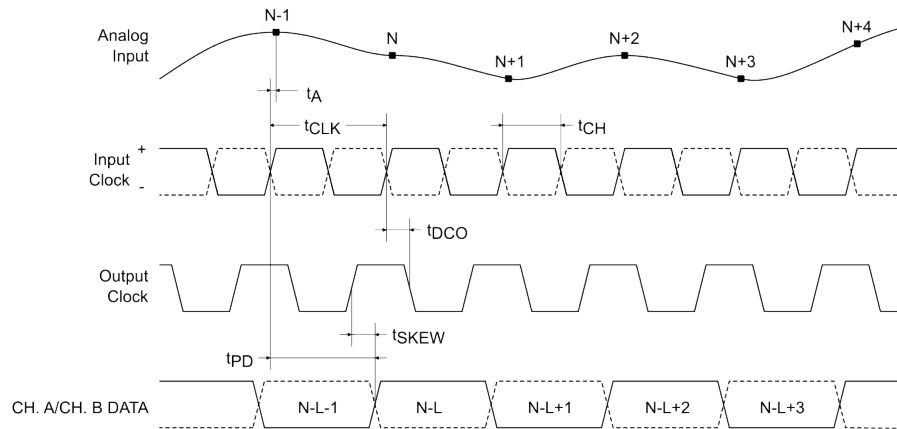


Figure 3: Parallel CMOS Output Mode Timing.

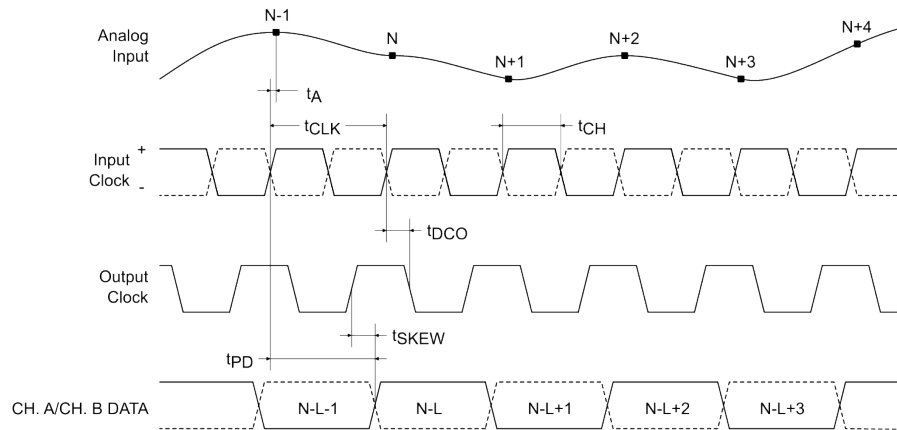


Figure 4: Parallel LVDS Output Mode Timing.

ABSOLUTE MAXIMUM RATINGS

Table 15. Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise specified).

Parameter	Symbol	Conditions	Min	Max	Units
AVDD	V_{AVDD}	Relative to AGND	-0.3	2.0	V
DRVDD	V_{DRVDD}	Relative to AGND	-0.3	2.0	V
VINAP/VINBP, VINAM/VINBM		Relative to AGND	-0.3	2.0	V
CLK+, CLK-		Relative to AGND	-0.3	2.0	V
SYNC		Relative to AGND	-0.3	2.0	V
RBIAS		Relative to AGND	-0.3	2.0	V
SENSE		Relative to AGND	-0.3	2.0	V
VCM		Relative to AGND	-0.3	2.0	V
VREF		Relative to AGND	-0.3	2.0	V
CSB		Relative to AGND	-0.3	2.0	V
SCLK/DFS		Relative to AGND	-0.3	2.0	V
SDIO/DCS		Relative to AGND	-0.3	2.0	V
OEB		Relative to AGND	-0.3	2.0	V
PDWN		Relative to AGND	-0.3	2.0	V
DA0, ..., DA15 DB0, ..., DB15		Relative to AGND	-0.3	2.0	V
DCO+, DCO-		Relative to AGND	-0.3	2.0	V
Operating Temperature Range (Ambient)			-40	85	°C
Maximum Junction Temperature Under Bias				125	
Storage Temperature Range (Ambient)			-65	150	

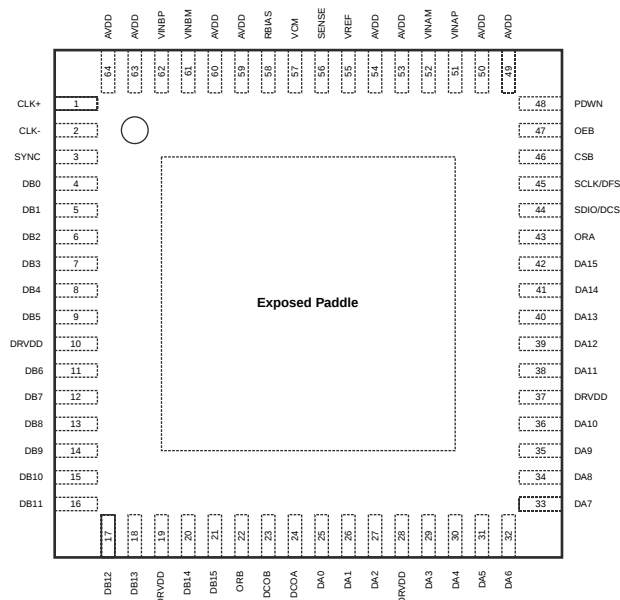
Notes:

- Stresses beyond those listed under Table 15 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD CAUTION.

	Electrostatic Discharge Sensitive Device. Proper ESD precautions should be observed to prevent performance degradation or loss of functionality.
---	---

PACKAGE



Number	Name	Type	Comment
22	ORB	Output	Channel B Overrange Output.
23	DCOB	Output	Channel B Data Clock Output.
24	DCOA	Output	Channel A Data Clock Output.
25	DA0	Output	Channel A CMOS Output Data (LSB).
26	DA1	Output	Channel A CMOS Output Data 1.
27	DA2	Output	Channel A CMOS Output Data 2.
28	DRVDD	Power	Digital I/O Supply.
29	DA3	Output	Channel A CMOS Output Data 3.
30	DA4	Output	Channel A CMOS Output Data 4.
31	DA5	Output	Channel A CMOS Output Data 5.
32	DA6	Output	Channel A CMOS Output Data 6.
33	DA7	Output	Channel A CMOS Output Data 7.
34	DA8	Output	Channel A CMOS Output Data 8.
35	DA9	Output	Channel A CMOS Output Data 9.
36	DA10	Output	Channel A CMOS Output Data 10.
37	DRVDD	Power	Digital I/O Supply.
38	DA11	Output	Channel A CMOS Output Data 11.
39	DA12	Output	Channel A CMOS Output Data 12.
40	DA13	Output	Channel A CMOS Output Data 13.
41	DA14	Output	Channel A CMOS Output Data 14.
42	DA15	Output	Channel A CMOS Output Data 15.
43	ORA	Output	Channel A Overrange Output.
44	SDIO/DCS	InOut	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
47	OEB	Input	Output Enable Input (Active low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
49	AVDD	Power	Analog Power Supply (1.8 V Nominal).
50	AVDD	Power	Analog Power Supply (1.8 V Nominal).
51	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
52	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
53	AVDD	Power	Analog Power Supply (1.8 V Nominal).
54	AVDD	Power	Analog Power Supply (1.8 V Nominal).
55	VREF	InOut	Voltage Reference Input/Output.
56	SENSE	Input	Reference Programming Pin.
57	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
58	RBIAS	InOut	External Reference Bias Resistor. Connect to 30 k Ω (1% tolerance) resistor to ground.
59	AVDD	Power	Analog Power Supply (1.8 V Nominal).
60	AVDD	Power	Analog Power Supply (1.8 V Nominal).
61	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
62	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.
63	AVDD	Power	Analog Power Supply (1.8 V Nominal).
64	AVDD	Power	Analog Power Supply (1.8 V Nominal).

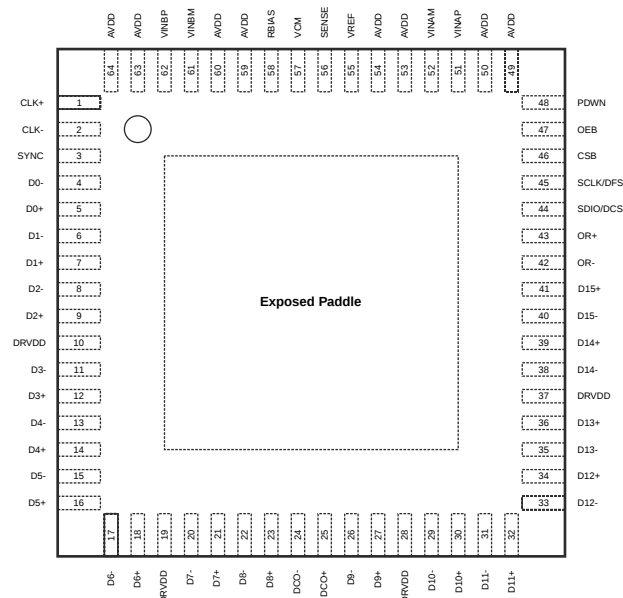


Figure 6: SD9650 Package Top View for Parallel LVDS Configuration.

1. NC = No Connect.
2. The exposed thermal pad on the bottom of the package provides the analog ground for the part and must be connected for proper operation.

Table 17. Pin Descriptions for Parallel LVDS Configuration.

Number	Name	Type	Comment
0	AGND	Ground	Exposed Paddle, Analog Ground.
1	CLK+	Input	ADC Clock Input (Plus).
2	CLK-	Input	ADC Clock Input (Minus).
3	SYNC	Input	Digital Synchronization Pin.
4	D0-	Output	Channel A/Channel B LVDS Output Data 0 (Minus).
5	D0+	Output	Channel A/Channel B LVDS Output Data 0 (Plus).
6	D1-	Output	Channel A/Channel B LVDS Output Data 1 (Minus).
7	D1+	Output	Channel A/Channel B LVDS Output Data 1 (Plus).
8	D2-	Output	Channel A/Channel B LVDS Output Data 2 (Minus).
9	D2+	Output	Channel A/Channel B LVDS Output Data 2 (Plus).
10	DRVDD	Power	Digital I/O Supply.
11	D3-	Output	Channel A/Channel B LVDS Output Data 3 (Minus).
12	D3+	Output	Channel A/Channel B LVDS Output Data 3 (Plus).
13	D4-	Output	Channel A/Channel B LVDS Output Data 4 (Minus).
14	D4+	Output	Channel A/Channel B LVDS Output Data 4 (Plus).
15	D5-	Output	Channel A/Channel B LVDS Output Data 5 (Minus).
16	D5+	Output	Channel A/Channel B LVDS Output Data 5 (Plus).
17	D6-	Output	Channel A/Channel B LVDS Output Data 6 (Minus).
18	D6+	Output	Channel A/Channel B LVDS Output Data 6 (Plus).
19	DRVDD	Power	Digital I/O Supply.
20	D7-	Output	Channel A/Channel B LVDS Output Data 7 (Minus).
21	D7+	Output	Channel A/Channel B LVDS Output Data 7 (Plus).
22	D8-	Output	Channel A/Channel B LVDS Output Data 8 (Minus).

Number	Name	Type	Comment
23	D8+	Output	Channel A/Channel B LVDS Output Data 8 (Plus).
24	DCO-	Output	LVDS Data Clock Output (Minus).
25	DCO+	Output	LVDS Data Clock Output (Plus).
26	D9-	Output	Channel A/Channel B LVDS Output Data 9 (Minus).
27	D9+	Output	Channel A/Channel B LVDS Output Data 9 (Plus).
28	DRVDD	Power	Digital I/O Supply.
29	D10-	Output	Channel A/Channel B LVDS Output Data 10 (Minus).
30	D10+	Output	Channel A/Channel B LVDS Output Data 10 (Plus).
31	D11-	Output	Channel A/Channel B LVDS Output Data 11 (Minus).
32	D11+	Output	Channel A/Channel B LVDS Output Data 11 (Plus).
33	D12-	Output	Channel A/Channel B LVDS Output Data 12 (Minus).
34	D12+	Output	Channel A/Channel B LVDS Output Data 12 (Plus).
35	D13-	Output	Channel A/Channel B LVDS Output Data 13 (Minus).
36	D13+	Output	Channel A/Channel B LVDS Output Data 13 (Plus).
37	DRVDD	Power	Digital I/O Supply.
38	D14-	Output	Channel A/Channel B LVDS Output Data 14 (Minus).
39	D14+	Output	Channel A/Channel B LVDS Output Data 14 (Plus).
40	D15-	Output	Channel A/Channel B LVDS Output Data 15 (Minus).
41	D15+	Output	Channel A/Channel B LVDS Output Data 15 (Plus).
42	OR-	Output	Channel A/Channel B LVDS Overrange (Minus).
43	OR+	Output	Channel A/Channel B LVDS Overrange (Plus).
44	SDIO/DCS	InOut	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
47	OEB	Input	Output Enable Input (Active low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
49	AVDD	Power	Analog Power Supply (1.8 V Nominal).
50	AVDD	Power	Analog Power Supply (1.8 V Nominal).
51	VINAP	Input	Differential Analog Input Pin (Plus) for Channel A.
52	VINAM	Input	Differential Analog Input Pin (Minus) for Channel A.
53	AVDD	Power	Analog Power Supply (1.8 V Nominal).
54	AVDD	Power	Analog Power Supply (1.8 V Nominal).
55	VREF	InOut	Voltage Reference Input/Output.
56	SENSE	Input	Reference Programming Pin.
57	VCM	Output	This pin outputs the common-mode voltage that can be used externally to bias the analog input pins.
58	RBIAS	InOut	External Reference Bias Resistor. Connect to 30 kΩ (1% tolerance) resistor to ground.
59	AVDD	Power	Analog Power Supply (1.8 V Nominal).
60	AVDD	Power	Analog Power Supply (1.8 V Nominal).
61	VINBM	Input	Differential Analog Input Pin (Minus) for Channel B.
62	VINBP	Input	Differential Analog Input Pin (Plus) for Channel B.
63	AVDD	Power	Analog Power Supply (1.8 V Nominal).
64	AVDD	Power	Analog Power Supply (1.8 V Nominal).

TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_{AVDD} = 1.8\text{V}$, $V_{DRVDD} = 1.8\text{V}$, $F_{CLK} = 65\text{MHz}$, $A_{IN} = -1\text{dBFS}$, differential AC-coupled clock source, LVDS mode, unless otherwise noted.

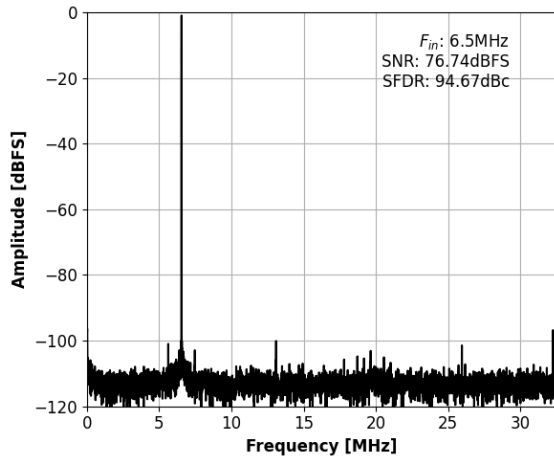


Figure 7: Single-Tone FFT with $f_{IN}=6.55\text{MHz}$.

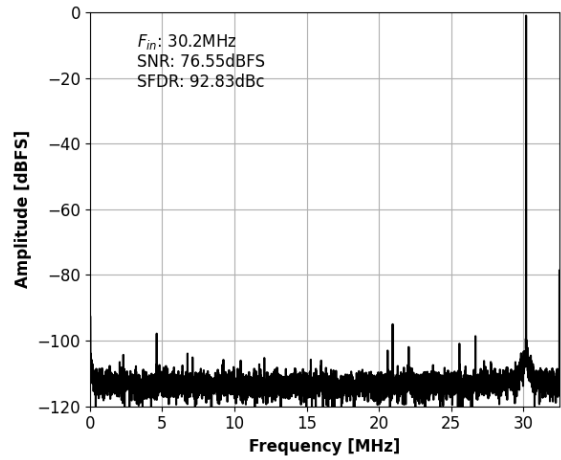


Figure 8: Single-Tone FFT with $f_{IN}=30.2\text{MHz}$.

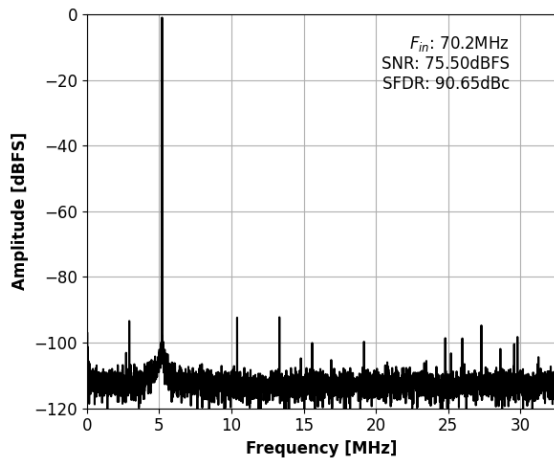


Figure 9: Single-Tone FFT with $f_{IN}=70.2\text{MHz}$.

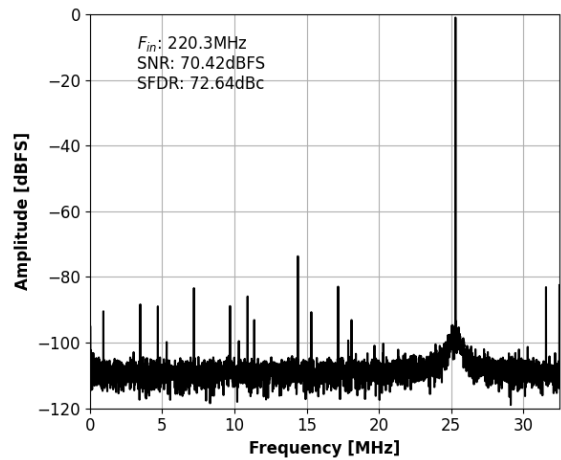


Figure 10: Single-Tone FFT with $f_{IN}=220\text{MHz}$.

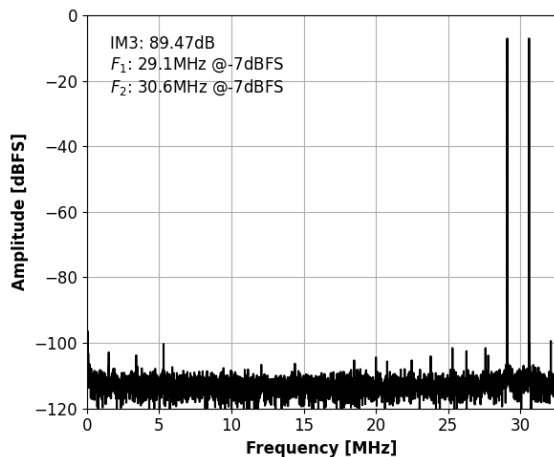


Figure 11: Two-Tone FFT with $f_{IN1}=29.1\text{MHz}$, $f_{IN2}=30.6\text{MHz}$.

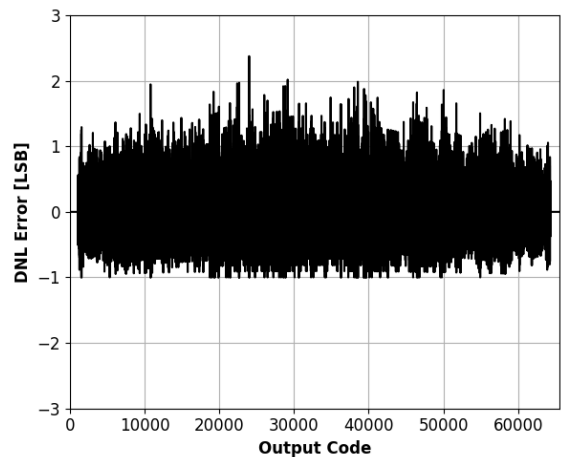


Figure 12: DNL Error with $f_{IN}=6.55\text{MHz}$.

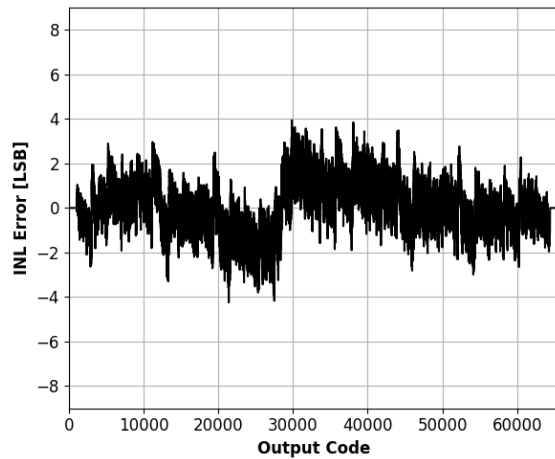


Figure 13: INL Error with $f_{IN}=6.55\text{MHz}$.

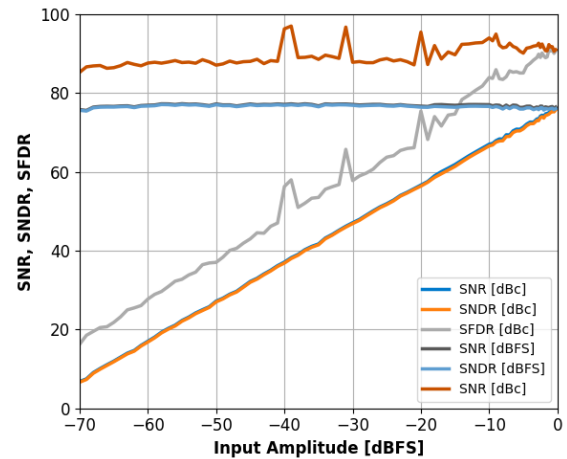


Figure 14: Single-Tone SNR, SNDR and SFDR vs. Input Amplitude with $f_{IN}=30.2\text{MHz}$.

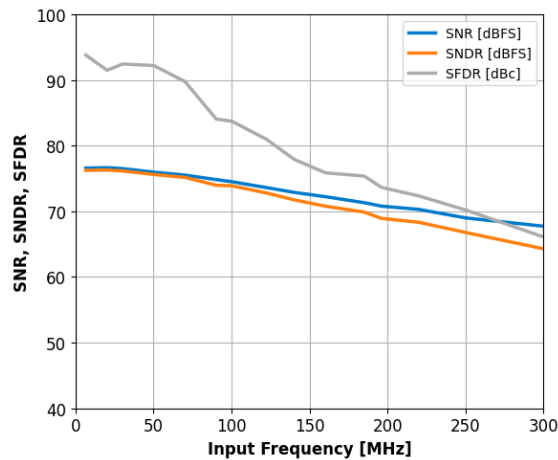


Figure 15: Single-Tone SNR, SNDR and SFDR vs. Input Frequency with $f_S=65\text{MHz}$.

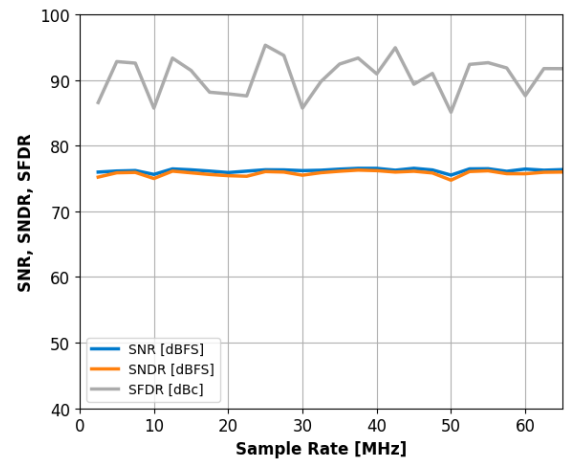


Figure 16: Single-Tone SNR, SNDR and SFDR vs. Sample Rate with $f_{IN}=30.2\text{MHz}$.

EQUIVALENT CIRCUITS

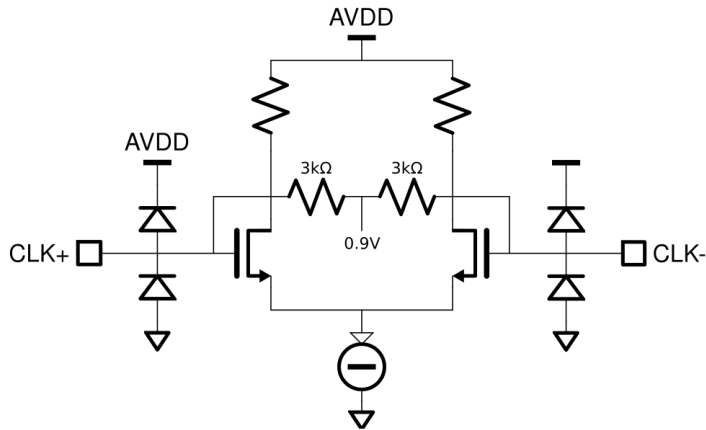


Figure 17: Equivalent Clock Input Circuit.

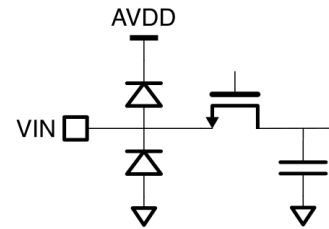


Figure 18: Equivalent Analog Input Circuit.

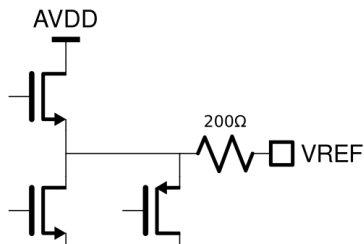


Figure 19: Equivalent VREF Circuit.

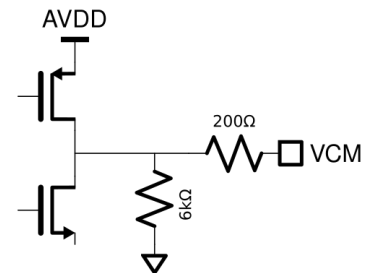


Figure 20: Equivalent VCM Circuit.

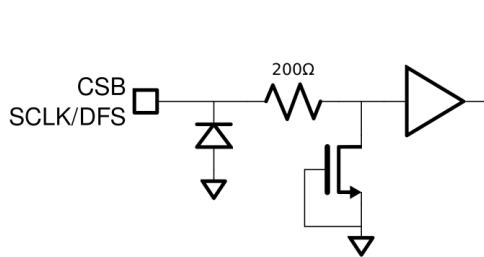


Figure 21: Equivalent CSB or SCLK/DFS Input Circuit.

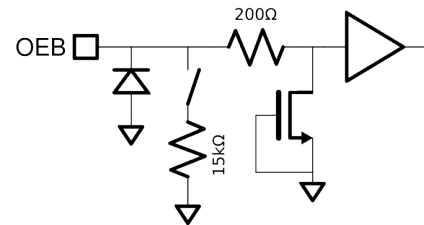


Figure 22: Equivalent OEB Input Circuit.

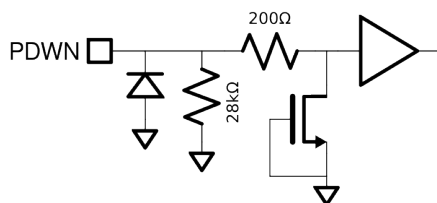


Figure 23: Equivalent PDWN Input Circuit.

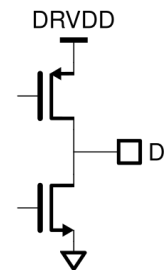


Figure 24: Equivalent Digital Output Circuit.

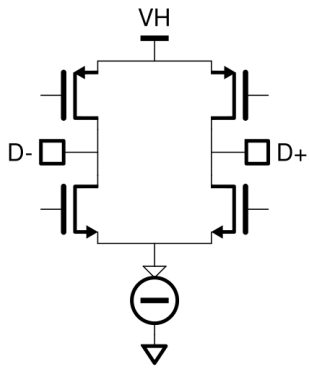


Figure 25: Equivalent LVDS output Circuit.

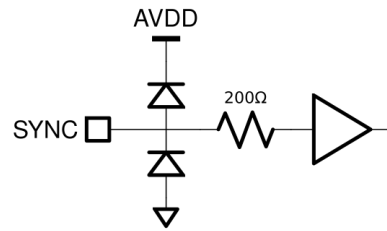


Figure 26: Equivalent SYNC Input Circuit.

THEORY OF OPERATION

ADC Architecture

The ADC uses a pipelined architecture and innovative patented switched-capacitor circuits. The differential implementation makes it highly immune to power supply noise and reference voltage self-modulation.

Analog Input

The input stage behaves as a switched-capacitor network, presenting itself to the driving circuit as a combination of a switch and a sampling capacitor. The capacitor is reset prior to each conversion cycle, effectively eliminating non-linear memory effects commonly observed in some pipelined ADC architectures. The ADC does not include an internal common-mode bias therefore, the driving source must provide an appropriate common-mode voltage.

Differential Clock Input

The SD9650 features a differential clock receiver with an integrated common-mode bias. For proper operation, the clock inputs should be AC-coupled using 10nF capacitors.

Differential Clock Configuration. For optimal jitter performance, a differential clock source is recommended. Connect the differential clock signals to CLK+ and CLK- through 10nF AC-coupling capacitors.

Single-Ended Clock Configuration. If a single-ended clock source is used, AC-couple the signal to the CLK+ pin. In this configuration, connect a 10nF capacitor between the CLK- pin and analog ground to maintain proper biasing.

Clock Jitter Considerations. Clock jitter has a significant impact on the ADC's signal-to-noise ratio (SNR). The sensitivity to jitter increases with input signal frequency. For best performance, use a low-noise differential clock with fast edge transitions.

Note: In some conditions the part can enter in manufacturing test mode if both differential clock inputs are held low for more than 1ms. This behavior can be blocked by writing 1 to register *0x4cf*, bit[15].

Clock Divider

The ADC includes a programmable clock divider that allows the input clock to be divided by integer values from 2 to 8. The divider is configured by setting register *0x463*, bits [7:5], to the desired division value. A value of 0 (default) bypasses the divider entirely.

By default, the divider starts asynchronously. If the application requires synchronization across multiple devices, the SYNC input is designed to synchronize the internal state of the clock dividers.

To synchronize the divider:

- Use a common SYNC signal for all ADCs in a synchronized system.
- Ensure low skew and matched trace lengths for the SYNC signal.
- Apply a rising edge to the SYNC pin. This edge will align the internal divider state to the external timing reference.

The divider will restart its cycle aligned to the SYNC event, ensuring deterministic phase alignment with the external system. The SYNC signal should be applied after all devices are configured via SPI and before data acquisition begins. If multiple SYNC pulses are used, the last pulse will determine the synchronization event.

Clock Duty-Cycle Requirements. The ADC utilizes both the rising and falling edges of the input clock (or the divided clock, if the divider is enabled) for internal sampling operations. To achieve optimal performance — especially at the maximum sampling rate — the clock duty cycle should be as close to 50% as possible.

When the divider is enabled with an even divisor, a 50% duty cycle is guaranteed by design. If the application uses a clock with a non-ideal duty cycle, a Duty Cycle Stabilizer (DCS) can be enabled to improve performance.

ADC Self-Calibration

The ADC includes an automatic calibration mechanism that is executed at power-up to ensure optimal performance. For best results, calibration should be performed at the actual sampling rate used during operation. To support this, the device continuously monitors the sampling clock frequency and automatically re-triggers calibration if a significant change is detected. This feature can be disabled by setting bit[0] of the *0x4c9* register to 1.

Manual calibration can also be initiated by toggling both *0xdc1*, bit[4] and *0xcc1*, bit[4] from 0 to 1. The calibration process is implemented using a state-machine architecture, ensuring a deterministic and predictable calibration time.

In addition, the ADC supports a Background Calibration (BGC) mode, which is disabled by default. BGC is beneficial in environments with large temperature variations near the extremes of the specified operating temperature range. When enabled, BGC injects a dither signal into the ADC input path, improving performance under thermal stress. However, this dither consumes approximately 0.8dB of the ADC's input range, resulting in earlier clipping compared to when BGC is disabled.

To enable BGC, set the following bits to 1:

- *0xde1*, bit[15]
- *0xce1*, bit[15]
- *0xde3*, bit[3]
- *0xce3*, bit[3]

After enabling these bits, manually trigger calibration as described above.

Stand-by and Power-Down Modes

The SD9650 supports two power-saving modes that can be used when the ADC is not actively sampling. In both modes, the SPI interface (if enabled) remains operational.

Power-Down Mode. This mode disables most of the internal circuitry, resulting in the lowest residual supply current. It is ideal for applications requiring minimal power consumption during idle periods. Power-down mode can be enabled via:

- The PDWN pin (when available), or
- Setting register *0x457*, bit[7], to 1.

Standby Mode. Standby mode offers a faster wake-up time compared to power-down mode, at the cost of slightly higher residual current. It is suitable for applications that require rapid recovery from idle states. To enable standby mode, set register *0x457*, bits [3] and [8], to 1.

Note: It is recommended to disable the ADC auto-calibration when using standby mode to avoid unintended calibration cycles during transitions.

Pin Functions

The SD9650 offers several functions available via dual function pin controls (external pin mode vs. SPI mode). The SD9650 detects the SPI mode during the first SPI transaction after power-up. If the user does not want to program the device via the SPI interface, the dual function is available.

DCS

The Duty-Cycle Stabilizer retimes the falling edge of the clock thus providing an internal clock signal with a 50% duty cycle. The DCS is useful in systems where the input clock has an uneven duty cycle. It can be enabled in the following ways:

- Via the DCS pin (if available).
- Via register control by setting register *0x457*, bit[1], to 1.

DFS

Data Format Select can be used to select between offset binary or two's complement when operating in the external pin mode.

OEB

Output Enable (active-low). If the OEB pin is low, the output data drivers and output clock are enabled. If the OEB pin is high, the CMOS output data drivers and clock are placed in a high impedance state; while the LVDS drivers are switched off.

The OEB function is not intended for rapid access to the data bus.

RBIAS

External Reference Bias Resistor. The SD9650 requires a 30k Ω , 1% resistor, between pin RBIAS and AGND to set the default bias current for the ADC.

SYNC

Digital Synchronization Pin. The clock divider can be synchronized using the external SYNC input. Register 0x463, bit [10], enables the clock divider to be re-synchronized across multiple parts and have their clock dividers aligned to enable simultaneous input sampling.

Procedure for Synchronizing Two or More ADC Devices. To synchronize multiple ADC components, follow these steps:

- Ensure the SYNC pin is set to 0.
- Configure the 0x463 register by setting bit [10] to 1.
- Set the SYNC pin to 1. This action will automatically set bit [10] in register 0x4ff.

Note: If multiple SYNC pulses are used, the last pulse will determine the synchronization event.

VCM

Common-Mode Level Bias Output for Analog Input. The VCM pin provides a DC voltage that can be used to bias the ADC input common-mode level, either directly using a passive circuit or indirectly as a common-mode reference voltage for the driving active device. In most use cases, the default common-mode voltage level is optimal.

VREF

The ADC supports both internal (default) and external voltage reference sources, selectable via the VREF pin. The selection between internal and external reference voltage can be made in one of two ways:

- Using the SENSE pin: a logic high level selects the external reference.
- Via register control: setting register 0x45d, bit[5] to 1 selects the external reference.

Internal Reference Output. When the internal voltage reference is used, the VREF pin can function as a reference output. This output can be enabled by setting register 0x45d, bits [11:10], to 0x3.

If the SENSE pin is held low, the reference output is enabled by default. To disable the reference output in this configuration, set register 0x45d, bits [11:10], to 0x2.

SERIAL PORT INTERFACE

The SD9650 uses a 3-wire Serial Port Interface (SPI) that gives the user flexibility to configure the converter for specific functions, depending on the application, through a register space provided inside the ADC.

The interface signals are:

- SCLK defines the bit rate at which serial data is driven onto, and sampled from, the bus;
- CSB defines the boundaries of a basic data 'unit', comprised of multiple serial bits;
- SDIO is the serial data IO wire;

The read and write cycles are described in the figure below. The complete instruction cycle is 32-bits long. The falling edge of CSB combines with the rising edge of SCLK marks the start of the instruction cycle. The address space is 13 bits long ($A<12:0>$) and the data is 16 bits wide ($D<15:0>$).

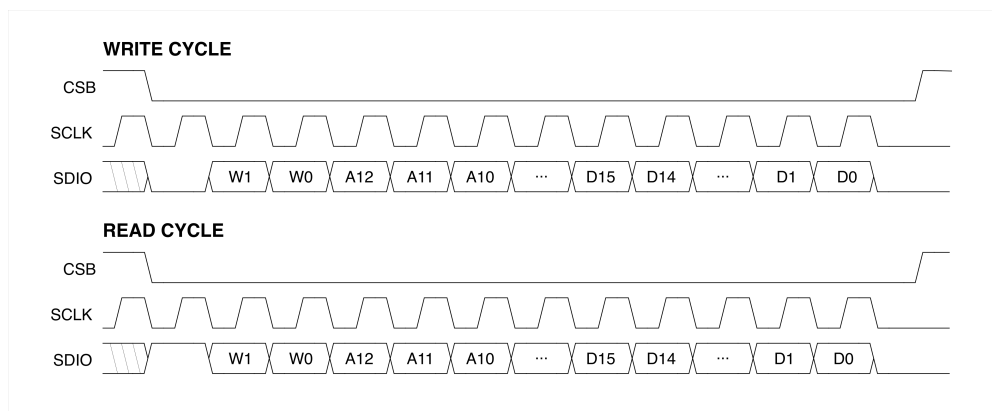


Figure 27: 3-wire SPI timing.

Table 18. SPI Timing.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup time between the data and the rising edge of SCLK	t_{DS}	2			ns
Hold time between the data and the rising edge of SCLK	t_{HD}	2			ns
Period of the SCLK	t_{SCLK}	40			ns
Setup time between CSB and SCLK	$t_{S,CSB-SCLK}$	2			ns
Hold time between CSB and SCLK	$t_{H,CSB-SCLK}$	2			ns
Minimum period that SCLK should be in a logic high state	$t_{SCLK,high}$	10			ns
Minimum period that SCLK should be in a logic low state	$t_{SCLK,low}$	10			ns
Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	$t_{SDIO,EN}$	10			ns
Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	$t_{SDIO,DIS}$	10			ns

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing.

Two bits, W1 and W0, determine how many bytes of data that can be transferred in the same write cycle (see Table 19). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.



Table 19. SPI Word Length.

[W1,W0]	Data length
00	Not supported
01	Two bytes of data can be transferred
10	Not supported
11	Four bytes of data can be transferred

The SPI pins should not be active when the full dynamic performance of the ADC is required. Noise from SCLK, CSB and the data transactions can degrade ADC performance.

OUTPUT MODE

Data Scrambler

Interference originating from the digital outputs of the ADC can be difficult to eliminate entirely. Such interference may result from capacitive or inductive coupling mechanisms, or from shared impedance paths in the ground plane. Even minimal coupling coefficients can introduce deterministic spurious tones into the ADC's output frequency spectrum. To mitigate this, digital output scrambling techniques can be employed prior to off-chip transmission. By randomizing the bit patterns, the spectral energy of these spurs is dispersed, effectively reducing their peak amplitudes and minimizing their impact on signal integrity.

The SD9650 can apply an exclusive-OR logic operation between the LSB and all other data output bits, while the LSB, overflow and clock outputs are not affected.



When this function is used, the receiver must apply the same function to unscramble the received data.

The data scrambler is enabled by programming control register *0x4b5*, bit[13].

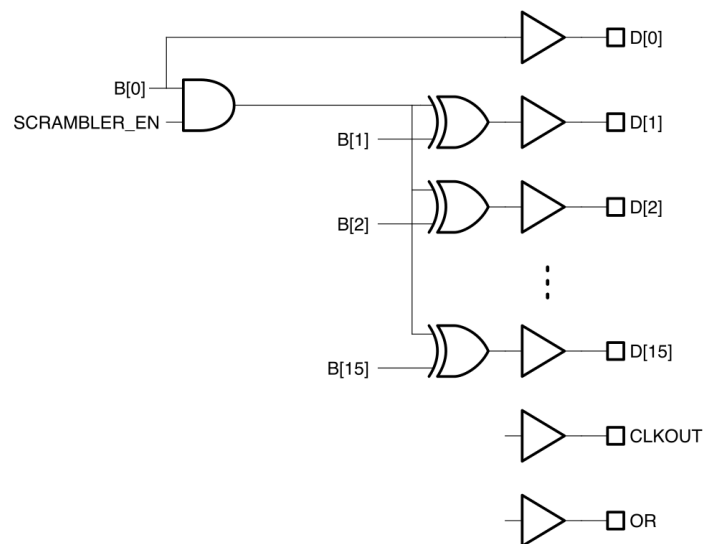


Figure 28: SD9650 Data Scrambler.

Alternate Bit Polarity

The alternate bit polarity is particularly effective to suppress digital feedback and minimize noise coupling on the PCB when the ADC input signal is near mid-scale and of very small amplitude. In this case, the digital output tends to toggle between patterns dominated by either logic high or logic low states. This synchronized switching of multiple bits can induce significant transient currents in the ground plane, leading to increased digital noise. This mode, when activated, inverts all odd-numbered data output bits prior to the output buffer stage while even-numbered bits, along with the overflow and clock output, remain unaffected thus ensuring that approximately half of the output bits transition are high while the other half transition are low. This balanced switching behavior helps cancel out opposing current flows in the ground return path, thereby reducing overall ground noise. At the receiving end, the original data can be reconstructed by inverting the same odd-numbered bits. This mode operates independently of the digital output randomization feature—both functions can be enabled or disabled separately. The Alternate Bit Polarity mode is configured via serial programming of control register *0x4b5*, bit[14].

Output Test Modes

The output test options are described in Table 20 and are selected via SPI programming at register *0x4b5*, bits [5:2].

When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. These tests require an active input clock.

There are two pseudo-random number generators available, PN23 and PN9. The PN23 generator ($X^{23}+X^{18}+1$), selected by register $0x4b5$, bits [5:2], set to 0x5, can be reset by setting register $0x4b5$, bit [12], low; while the PN9 generator (X^9+X^5+1), selected by register $0x4b5$ set to 0x6, can be reset by setting register $0x4b5$, bit [11], low.

Table 20. Output Test Modes.

Mode	Function
0	Pass-Through
1	Midscale
2	+FS
3	-FS
4	Checkerboard
5	PN23
6	PN9
7	1/0 word toggle
8	User input
9	1/0 bit toggle
10	1x sync
11	1-bit high
12	Mixed frequency
13	Unused
14	Unused
15	Ramp

Pass-through and test patterns 1, 2, 3, 5 and 6 are subject to output formatting, while the other test modes are not. Test patterns 1, 8 and 15 can be applied to either one channel or both channels using $0x4b5$, bit[7:6]. Patterns 4 and 7 can be toggled between the pattern and its inverse while test pattern 8 can be selected using registers $0x4bb$, $0x4bd$, $0x4bb$ and $0x4bb$.

CONTROL REGISTERS

The following tables describe the control registers. The tables describe the registers as follows:

Address: <HEX value>	RW or RO	Default: <HEX value>
bit field	default value	field description.

where: **RW** indicates a Read/Write register and **RO** indicates a Read-Only register. If the register is read-only, the default value is omitted.

Registers not explicitly described in the following tables should not be written.



When changing control register values, read-modify-write procedure should be used. Some registers contain reserved bit fields for engineering purposes. This avoids inadvertently changing the values of those bits.

Address: 0x455	RW	Default: 0x1
[0]	0x1	Soft reset (active low).

Address: 0x457	RW	Default: 0x015
[0]	0x1	Duty Cycle Stabilizer enable.
[1]	0x0	Duty Cycle Stabilizer.
[2]	0x1	External output enable (OE/OEB) control 0: Output Enabled 1: Output depends on pin OE/OEB
[3]	0x0	Output disable 0: Output depends on oeb_en_reg (default) 1: Disabled
[4]	0x1	Reserved.
[6:5]	0x0	Reserved.
[7]	0x0	Software power down.
[8]	0x0	Software sleep mode.

Address: 0x45d	RW	Default: 0x0095
[0]	0x1	Reference enable.
[4:1]	0xa	Reference value.
[5]	0x0	Set reference. 0: Internal 1: External
[9:6]	0x2	Reserved.
[11:10]	0x0	Reserved.
[14:12]	0x0	Reserved.

Address: 0x463		RW	Default: 0x019
[0]	0x1		Enable clock receiver.
[2:1]	0x0		Clock RX common-mode bias.
[4:3]	0x3		Clock RX bias.
[7:5]	0x0		Clock RX divider control. 0: Bypass 1: Divide by 2 2: Divide by 3 3: ... 7: Divide by 8
[8]	0x0		Enable on-chip termination.
[9]	0x0		Clock RX polarity.
[10]	0x0		Enable SYNC pin synchronization.

Address: 0x465		RW	Default: 0x0
[2:0]	0x0		Output data interleaver. 0: pass through, no interleaving 1: pass through, channels swapped, no interleaving 2: N/A 3: N/A 4: parallel ADC_A/ADC_B interleaving 5: parallel ADC_B/ADC_A interleaving 6: even-odd interleaving 7: odd-even interleaving

Address: 0x473		RW	Default: 0x0000
[4:0]	0x00		DDR clock delay.
[9:5]	0x00		Output data delay.
[14:10]	0x00		Output clock delay.

Address: 0x475		RW	Default: 0x1
[0]	0x1		Enable VCM.

Address: 0x4b5		RW	Default: 0x18c0
[1:0]	0x0		Output format. 0: Signed binary 1: Offset binary 2: Gray code 3: N/A
[5:2]	0x0		Output test mode select (see Table 20).
[6]	0x1		Output test channel CH. A 0: Disable 1: Enable
[7]	0x1		Output test channel CH. B 0: Disable 1: Enable
[8]	0x0		Output test toggle mode. Toggle between user test pattern 0 and 1.
[10:9]	0x0		Output data Output mux control 2'h0: Disabled (default) 2'h1: ... 2'h2: ... 2'h3: ...
[11]	0x1		PN9 generator reset (active low)
[12]	0x1		PN23 generator reset (active low)
[13]	0x0		Enable the output data scrambler.
[14]	0x0		Enable alternate bit polarity switch.

Address: 0x4b7		RW	Default: 0x0092
[15:0]	0x0092		PN9 initial seed.

Address: 0x4b9		RW	Default: 0x3aff
[15:0]	0x3aff		PN9 initial seed.

Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 0 (CH. A).

Address: 0x4bb		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 1 (CH. A).

Address: 0x4bf		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 0 (CH. B).

Address: 0x4c1		RW	Default: 0x0000
[15:0]	0x0000		User test pattern 1 (CH. B).

Address: 0x4c9		RW	Default: 0x0000
[0]	0x0		Disable auto-recalibration.
[15:1]	0x0000		Reserved.

Address: 0x4cf		RW	Default: 0x0035
[14:0]	0x0035		Reserved.
[15]	0x0035		Disable test mode.

Address: 0x4fd	RO	Default: N/A
[2:0]	Chip revision.	
[6:3]	Label ID.	
[7]	Reserved.	
[8]	Performance ID for device 0: Low-power LVDS 1: High-speed LVDS	
[10:9]	Resolution ID for device 0: 10-bit 1: 12-bit 2: 14-bit 3: 16-bit	
[13:11]	Speed ID for device.	

Address: 0x4ff	RO	Default: N/A
[0]	Reserved.	
[1]	Analog Supply Ready.	
[2]	Digital Supply Ready.	
[3]	I/O Supply Ready.	
[4]	Sense pin status.	
[5]	SPI enabled.	
[6]	Power down pin status.	
[7]	Reserved.	
[8]	Reserved.	
[9]	SYNC pin status.	
[10]	Synchronization done.	

Address: 0xf03	RW	Default: 0x7f8
[0]	0x0	Enable top level bias.
[1]	0x0	Enable clock skew control DAC.
[2]	0x0	Reserved.
[3]	0x1	Reserved.
[4]	0x1	Reserved.
[10:5]	0x3f	Mask for enable pin.

Address: 0xf05	RW	Default: 0x30
[5:0]	0x30	Mask for sleep pin.
[6]	0x0	Sleep ADC_B.
[7]	0x0	Sleep ADC_A.

Address: 0xf07		RW	Default: 0x40
[0]	0x0		Enable primary clock.
[1]	0x0		Analog clock enable.
[2]	0x0		ADC top level clock divider.
[3]	0x0		Clock select. 0: ADC_B 1: ADC_A
[4]	0x0		Reserved.
[5]	0x0		Reserved.
[6]	0x1		ADC clock generator reset.
[7]	0x0		Reserved.

Address: 0xf0b		RW	Default: 0x24
[2:0]	0x4		Clock receiver bias.
[5:3]	0x4		ADC master bias.

Address: 0xf0f		RW	Default: 0x28
[1:0]	0x0		Clock divider.
[3:2]	0x2		Clock delay.
[5:4]	0x2		Reserved.

Address: 0xf11		RW	Default: 0x0b
[2:0]	0x3		Main bias.
[4:3]	0x1		Input common mode level.

Address: 0xf27		RW	Default: 0x04
[5:0]	0x04		Dither enable.

Address: 0xdc1		RW	Default: 0xbfff
[0]	0x1		Enable.
[1]	0x1		Clock enable.
[2]	0x1		Soft reset.
[3]	0x1		Reserved.
[4]	0x1		Calibration soft reset.
[5]	0x1		Reserved.
[6]	0x1		Reserved.
[10:7]	0xf		Enable mask for en_adc pin.
[15:11]	0x17		Sleep mask for sleep pin.

Address: 0xdc3		RW	Default: 0x0000
[3:0]	0x0		Clock phase.
[11:4]	0x00		Clock fine delay.
[12]	0x0		Enable fine delay register control.
[13]	0x0		Input clock polarity switch.
[14]	0x0		Output clock polarity switch.

Address: 0xde1		RW	Default: 0xbb28
[7:0]	0x28		Calibration length.
[8]	0x1		Enable calibration.
[9]	0x1		Foreground calibration.
[14:10]	0x0		Reserved.
[15]	0x1		Enable retain mode.

Address: 0xde3		RW	Default: 0x8
[2:0]	0x0		Reserved.
[3]	0x1		Enable stage calibration.

Address: 0xcc1		RW	Default: 0xbfff
[0]	0x1		Enable.
[1]	0x1		Clock enable.
[2]	0x1		Soft reset.
[3]	0x1		Reserved.
[4]	0x1		Calibration soft reset.
[5]	0x1		Reserved.
[6]	0x1		Reserved.
[10:7]	0xf		Enable mask for en_adc pin.
[15:11]	0x17		Sleep mask for sleep pin.

Address: 0xcc3		RW	Default: 0x0000
[3:0]	0x0		Clock phase.
[11:4]	0x00		Clock fine delay.
[12]	0x0		Enable fine delay register control.
[13]	0x0		Input clock polarity switch.
[14]	0x0		Output clock polarity switch.

Address: 0xce1		RW	Default: 0xbb28
[7:0]	0x28		Calibration length.
[8]	0x1		Enable calibration.
[9]	0x1		Foreground calibration.
[14:10]	0x0		Reserved.
[15]	0x1		Enable retain mode.

Address: 0xce3		RW	Default: 0x8
[2:0]	0x0		Reserved.
[3]	0x1		Enable stage calibration.

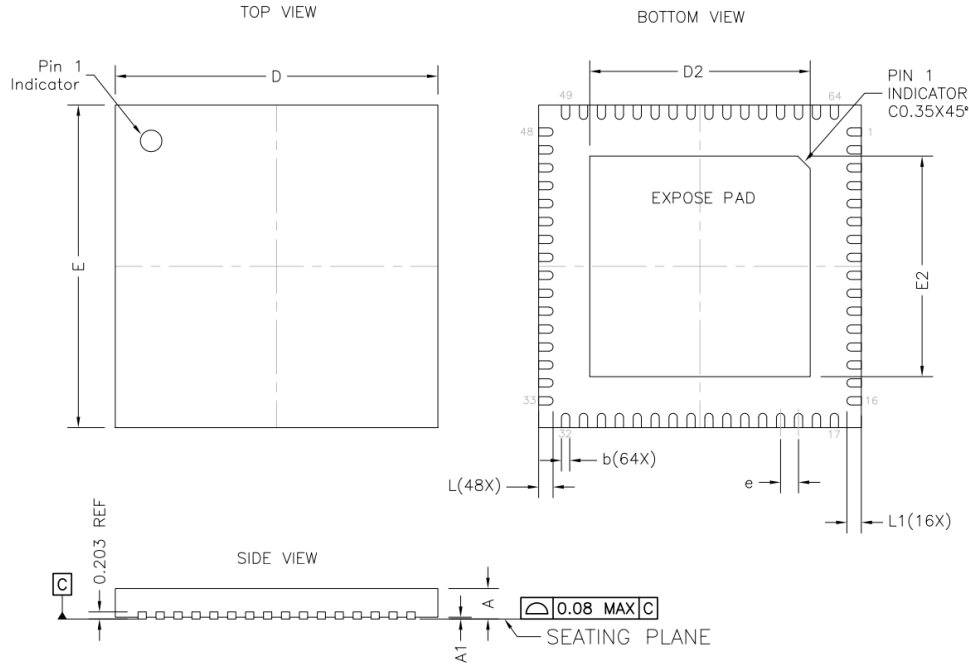
ORDERING INFORMATION

Base Part No.	Orderable Part No. Full Tray	Orderable Part No. Tray with 50Pcs	Orderable Part No. Reel with 750pcs
SD9650-65	SD9650-65-A-QC9-TB	SD9650-65-A-QC9-TA	SD9650-65-A-QC9-RD

EVK	Part No.
CMOS	SDE1121-C
LVDS	SDE1121-L

This product is protected by several U.S. Patents (www.silannasemi.com/patents).

PACKAGE DRAWING



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	8.90	9.00	9.10
D2	6.10	6.15	6.20
E	8.90	9.00	9.10
E2	6.10	6.15	6.20
e	0.50 BSC		
L	0.35	0.40	0.45
L1	0.33	0.38	0.43

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pad as well as the terminals
5. Lead Finish: 100% Sn

Figure 29: Package Dimensions.

REVISION HISTORY

Version	Date	Comment
1.0	June 19, 2025	Initial Release.
2.0	July 30, 2025	Filled missing specifications. Changed RBIAS resistor to 30k Ω . Improved timing diagrams. Fixed typos.

Silanna Semiconductor Proprietary and Confidential

Information furnished by Silanna Semiconductor is believed to be accurate and reliable. However, no responsibility is assumed for its use. Silanna Semiconductor makes no representation that the interconnection of its circuits as described herein will not infringe on existing patents rights. Specifications subject to change without notice.