Highly Efficient, Regulated Dual-Output, Ambient Energy Manager for TEG with Optional Primary Battery

Features

Maximum Power Point Tracking

- Open-circuit voltage sensing for MPPT every 21s.
- Selectable MPPT ratio to 50%, 55% or 75%.
- Harvesting input voltage range from 80 mV to 3.5 V.
- Constant impedance matching (ZMPPT).

Ultra-low power start-up

- Cold start from 80 mV input voltage and 650 µA input current (typical) using the cold-start module.

Integrated low-voltage LDO regulator

- Up to 20 mA load current.
- Output voltage selectable at 1.2 V or 1.8 V.
- Dynamically power-gated by external control.

Integrated high-voltage LDO regulator

- Up to 80 mA load current with 300 mV drop-out.
- Output voltage selectable at 1.8 V, 2.5 V or 3.3 V.
- Dynamically power-gated by external control.

Flexible energy storage management

- Selectable overcharge and over-discharge protection for various types of rechargeable storage elements.
- Fast supercapacitor charging.
- Status signal when storage element is running low.
- Status signal when LDO outputs are available.

Optional primary battery

- Automatic switching to primary battery when the storage element is depleted.

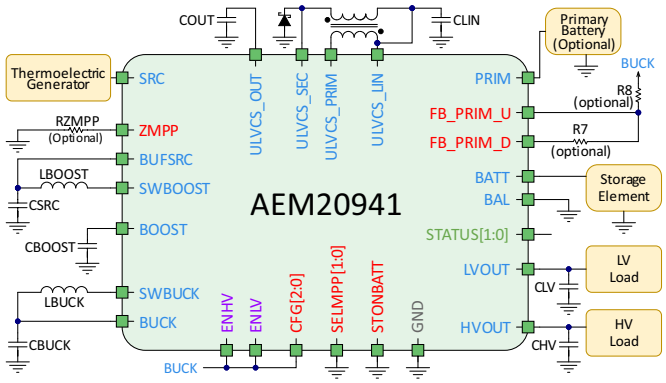
Start-up from storage element

- Possibility to start-up from the storage element.

Integrated storage element balancing circuit for dual-cell supercapacitor

Applications

Smart home	Industrial sensor
Smart building	Retail
Edge IoT	PC accessories



Description

The AEM20941 is an integrated energy management circuit that extracts DC power from a TEG to simultaneously store energy in a rechargeable element and supply the system with two independent regulated voltages. The AEM20941 allows to extend battery lifetime and ultimately eliminate the primary energy storage element in a large range of wireless applications such as industrial monitoring, home automation and smart agriculture.

The AEM20941 harvests the available input current up to 110 mA while regulating the source to a voltage configured by the user. It integrates an ultra-low power boost converter to charge a storage element, such as a Li-ion battery, a thin film battery, a supercapacitor or a conventional capacitor. The boost converter operates with input voltages ranging from 80 mV to 3.5 V.

With its unique cold-start circuit, it can start operating with empty storage elements at an input voltage as low as 380 mV and an input power of only 40 µW. Thanks to an optional cold-start module, the input voltage for coldstart lowers to 80 mV with a minimum input current of 650 µA.

The low-voltage supply typically drives a microcontroller at 1.2 V or 1.8 V. The high-voltage supply typically drives a radio transceiver at 1.8 V, 2.5 V or 3.3 V. Both are driven by highly-efficient LDO (Low Drop-Out) linear regulators for low noise and high stability.

Configuration pins determine various operating modes by setting predefined conditions for the energy storage element (overcharge or over-discharge voltages), and by selecting the voltage of the high-voltage supply and the low-voltage supply.

The chip integrates all active elements for powering a typical wireless sensor. Five capacitors and two inductors are required, all available in small packages. With only seven external components (optional cold-start module components not included), integration is maximized, footprint and BOM are minimized, optimizing the time-to-market and the costs of designs.

Device Information

Part Number	Package	Body Size
10AEM20941C0001	QFN 28-pin	4 x 4 mm

Evaluation Board

Part Number
2AAEM20941C001

List of Figures

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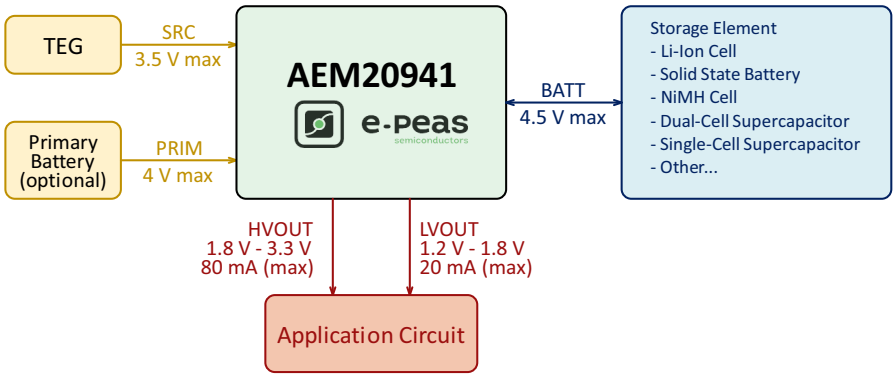


Figure 1: Simplified schematic view

1. Introduction

The AEM20941 is a full-featured energy efficient power management circuit capable of charging a storage element (battery or supercapacitor, connected to BATT) from an energy source (connected to SRC) as well as supplying loads at different operating voltages through two power supplying LDO regulators (LVOUT and HVOUT).

The heart of the AEM20941 is a cascade of two regulated switching converters, namely the boost converter and the buck converter, both with high power conversion efficiencies (See Section 3.6).

At first start-up, as soon as a required cold-start voltage of 380 mV and a scant amount of power of only 40 µW are available from the harvested energy source, the AEM coldstarts. With the optional internal cold-start module and the addition of 4 external components, the cold-start voltage can be reduced to 80 mV with a minimum input current of 650 µA. After the cold start, the AEM can extract the power available from the source as long as the input voltage is within 80 mV to 3.5 V range. Note that the STONBATT pin makes it possible to bypass the cold start procedure using the pre-charged storage element to start the AEM20941 (see Section 6.5).

Through three configuration pins (CFG[2:0]), the user can select a specific operating mode from a range of seven modes that covers most application requirements without any dedicated external component. These operating modes define the LDO output voltages and the storage element protection thresholds.

The Maximum Power Point Tracking (MPPT) ratio can be configured using two configuration pins (SELMPP[1:0]) (See Section 6.2).

Two logic control pins (ENLV and ENHV) allow to dynamically activate or deactivate the LDO regulators that supply the low and high voltage loads. The status pin STATUS[0] alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the storage element voltage gets depleted, LVOUT and HVOUT are power-gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin STATUS[1] alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected to PRIM, the AEM20941 automatically uses it as a source to recharge the storage element before switching back to the ambient source connected to SRC. This guarantees continuous operation even under the most adverse conditions (See Section 5.2.4). STATUS[1] is asserted when the primary battery is providing power.

2. Pin Configuration and Functions

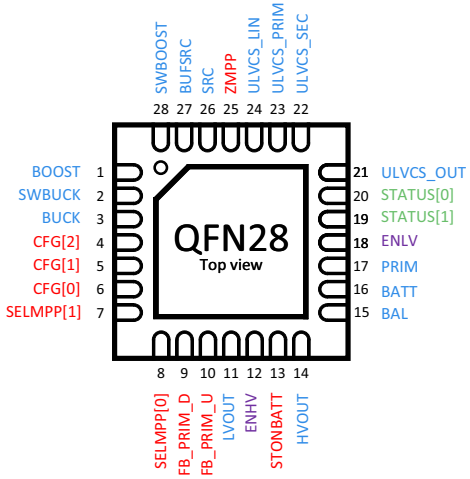


Figure 2: Pinout diagram QFN 28-pin

Name	Pin Number	Function
Power pins		
BOOST	1	Output of the boost converter.
SWBUCK	2	Switching node of the buck converter.
BUCK	3	Output of the buck converter.
LVOUT	11	Output of the low voltage LDO regulator.
HVOUT	14	Output of the high voltage LDO regulator.
BAL	15	Connection to the mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.
SRC	26	Connection to the harvested energy source.
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.
SWBOOST	28	Switching node of the boost converter.
ULVCS_OUT	21	Connection to the ULVCS buffer capacitor.
ULVCS_SEC	22	Connection to the secondary of the cold-start module transformer.
ULVCS_PRIM	23	Connection to the primary of the cold-start module transformer.
ULVCS_LIN	24	Input of the cold-start module transformer.

Table 1: Pins description (part 1)

Name	Pin Number	Logic Level		Function
		LOW	HIGH	
Configuration pins				
CFG[2]	4	GND	BUCK	Used to configure the storage element protection thresholds and the LDOs output voltages.
CFG[1]	5	GND	BUCK	
CFG[0]	6	GND	BUCK	
SELMPP[1]	7	GND	BUCK	Used to configure the MPPT ratio.
SELMPP[0]	8	GND	BUCK	
FB_PRIM_D	9	Analog Pin		Used to configure the primary battery overdischarge voltage (optional). Must be connected to GND if not used.
FB_PRIM_U	10	Analog Pin		
STONBATT	13	GND	BATT	Used to configure the cold start from the storage element (optional). Must be connected to GND if not used.
ZMPP	25	Analog Pin		Used to configure the ZMPPT (optional). Must be left floating if not used.
Control pins				
ENHV	12	GND	BUCK	Enabling pin for the high-voltage LDO (See Table 8).
ENLV	18	GND	BUCK to BOOST	Enabling pin for the low-voltage LDO (See Table 8). HIGH level is any voltage between BUCK and BOOST.
Status pins				

STATUS[1]	19	GND	BATT	Logic output.
				- HIGH:
				  - during T_{CRIT} when in SHUTDOWN MODE.
				  - as long as in PRIMARY BATTERY MODE.
				- LOW otherwise.

STATUS[0]	20	GND	BATT	Logic output. Asserted when the LDOs can be enabled.
Other pins				
GND	Exposed Pad			Ground connection, must be strongly tied to the PCB ground plane.

Table 2: Pins description (part 2)

3. Specifications

3.1. Absolute Maximum Ratings

Parameter		Min	Max	Unit
Operating junction temperature T_J		-40	85	°C
Storage temperature T_{stg}		-65	150	°C
Input voltage	BATT, BAL, PRIM, BOOST, SWBOOST, HVOUT, ENLV, STONBATT	-0.3	5.50	V
	SRC, BUFSRC, ZMPP	-0.3	3.50	V
	BUCK, SWBUCK, LVOUT, ULVCS_LIN, ULVCS_OUT, ULVCS_PRIM, ULVCS_SEC, CFG[2:0], FB_PRIM_U, FB_PRIM_D, SELMPP[1:0], ENHV	-0.3	2.75	V

Table 3: Absolute maximum ratings

3.2. ESD Ratings

Parameter		Value	Unit
Electrostatic discharge V_{ESD}	Human-Body Model (HBM)	TBD	V
	Charged-Device Model (CDM)	TBD	V

Table 4: Absolute maximum ratings

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

3.3. Thermal Resistance

Package	θJA	θJC	Unit
QFN 28-pin 4 x 4 mm	60	6	°C/W

Table 5: Thermal data

3.4. Electrical Characteristics at 25 °C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input voltage and input power						
$V_{SRC,CS}$	Minimum source voltage required to coldstart.	Without the optional cold-start circuit.		380		mV
		With the optional cold-start circuit.		80		mV
$I_{SRC,CS}$	Minimum source current required to coldstart.	Without the optional cold-start circuit.		105		µA
		With the optional cold-start circuit.		650		µA
V_{SRC}	Input voltage of the energy source (maximum given by the open-circuit voltage).	After cold start.	0.08[1]		3.5	V
I_{SRC}	Harvested current from the energy source.	L_{BOOST} = 10 µH.			110	mA
		L_{BOOST} = 22 µH.			50	
V_{MPP}	Target regulation voltage on SRC when extracting power.	After cold start.	0.08		3.5[2]	V
DC-DC converters						
V_{BOOST}	Output voltage of the boost converter.	During normal operation.	2.2		4.5	V
V_{BUCK}	Output voltage of the buck converter.		2	2.2	2.5	
$V_{BUCK,RESET}$	Minimum voltage on BUCK before switching to DEEP SLEEP MODE (from any other mode).			1.8		V
I_{BUCK}	Total load current supplied by the BUCK converter (including LVOUT current I_{LV}).	L_{BUCK} = 10 µH.	0		20	mA
		L_{BUCK} = 4 µH.	0		50	mA
Storage element						
V_{BATT}	Voltage on the storage element.		0[3]		4.5	V
$V_{BAL,MIN}$	Minimum voltage required on the BAL pin for the balancing circuit to operate.			0.9		V
V_{PRIM}	Voltage on the primary battery.		0.6		V_{OVDIS} + 0.4 V	V
I_{PRIM}	Current from the primary battery.			20		mA
$V_{FB\_PRIM\_U}$	Feedback for defining the overdischarge voltage level on the primary battery.		0.15		1.1	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling the boost converter.	See Table 9.	2.70		4.50	V
V_{CHRDY}	Minimum voltage required on the storage element before enabling the LDO when coming from WAKE-UP MODE.	After cold start See Table 9.	2.30		4.04	V
V_{OVDIS}	Minimum voltage accepted on the storage element before switching to primary battery or entering SHUTDOWN MODE.	See Table 9.	2.20		3.60	V
I_Q	Quiescent current on BATT when the boost converter is not running.	V_{BATT} = 3 V; LDOs disabled.		400		nA
		V_{BATT} = 3 V; LDOs enabled.		600		nA
Low-Voltage LDO regulator						
V_{LV}[4]	Output voltage of the low-voltage LDO (see Table 9).		1.2		1.8	V
I_{LV}	Load current supplied by the low-voltage LDO.		0		20	mA

Table 6: Electrical characteristics (Part 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
High-Voltage LDO regulator						
V_{HV}[5]	Output voltage of the high-voltage LDO (see Table 9).		1.8		3.3	V
I_{HV}	Load current supplied by the high-voltage LDO.		0		80	mA
Timing						
$T_{MPPT,WAIT}$	Time during which the AEM20941 stops pulling current on SRC before measuring the harvester open circuit voltage (V_{OC}).			328		ms
$T_{MPPT,MEASURE}$	Duration of V_{OC} measurement during MPP evaluations.			1.2		ms
$T_{MPPT,PERIOD}$	Period of the MPPT V_{OC} evaluations.			21		s
T_{CRIT}	Time before shutdown once STATUS[1] has been asserted (see Section 5.2.5 and Figure 2).		400	600	800	ms

Table 6: Electrical characteristics (Part 2)

1. Minimum V_{SRC} value for harvesting capabilities after coldstart.
2. Maximum V_{MPP} value only when the MPPT is configured on ZMPP. Otherwise, maximum V_{MPP} = 0.75 x V_{OC} (see Section 6.2).
3. To stay in NORMAL MODE, V_{BATT} minimum voltage must stay above V_{OVDIS}.
4. The variability of V_{LV} at 1 mA is 1% (typical and preliminary result from simulations).
5. The variability of V_{HV} at 1 mA is 1.3% (typical and preliminary result from simulations).

3.5. Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External components						
C_{SRC}	BUFSRC pin decoupling capacitor.		10	22	22[1]	µF
C_{BOOST}	Output capacitor of the boost converter.		10	22		µF
L_{BOOST}	Inductor of the boost converter.		4	10[2]		µH
C_{BUCK}	Output capacitor of the buck converter.		8	10		µF
L_{BUCK}	Inductor of the buck converter.		4	10	25	µH
C_{LV}	Low-voltage LDO regulator decoupling capacitor.		8	10	14	µF
C_{HV}	High-voltage LDO regulator decoupling capacitor.		8	10	14	µF
C_{BATT}	Capacitor connected on BATT if no storage element is connected (see Section 3.5.3).	LDOs disabled.	22			µF
		LDOs enabled.	150			µF
L_{CS}	Transformer of the optional cold-start module.	Primary inductance:		25		µH
		Turns ratio:		1:20		
C_{LIN}	Input capacitor of the optional cold-start module.			2.2		µF
C_{OUT}	Output capacitor of the optional cold-start module.			220		nF
R_{ZMPP}	Optional - Resistor for the ZMPPT configuration (see Section 6.4).		10		1M	Ω
R_P	Optional - Sum of resistors used to define the primary battery minimum voltage. R_P = R7 + R8 (see Section 6.3).		100		500	kΩ

Table 7: Recommended operating conditions

1. For source voltages below 300 mV, a higher capacitor value may be used if the source voltage ripple is too high.
2. For better efficiency, a 22 µH inductor can be used on LBOOST, although this will result in a lower maximum current.

3.5.1. External Inductors Information

The AEM20941 operates with two external inductors. All inductors must support a minimum switching frequency of 10 MHz. Using inductors with low equivalent series resistance (ESR) improves the power-conversion efficiency of both the boost and buck converters.

L_{BOOST}

The AEM20941 circuit is typically implemented with one of the following values on L_{BOOST}:

- 22 µH (peak current min. 115 mA) allows better efficiencies, especially at low SRC voltages.
- 10 µH (peak current min. 250 mA) allows higher current from SRC to BATT.

L_{BUCK}

With the recommended operating condition (10 µH inductor), the buck inductor L_{BUCK} must support a minimum peak current of 50 mA.

L_{CS}

The cold-start transformer L_{CS} is used in fly-back mode to power the internal cold-start module. See Table 11 for recommended L_{CS}.

3.5.2. External Capacitors Information

The AEM20941 operates with 8 external miniature capacitors to ensure stable operation of the boost converter, buck converter, storage element output, cold-start module, and LDO outputs. Each capacitor serves as a local energy buffer that limits voltage fluctuations caused by switching activity or dynamic load transition.

To maintain optimal performances and minimized quiescent current, all capacitors must exhibit a low leakage current and follow the recommended nominal values listed in Table 7, with a tolerance of ± 20 %.

3.5.3. Storage Element Information

The energy storage element of the AEM20941 can be a rechargeable battery, a supercapacitor or a large capacitor. It should be selected so that its voltage never fall below V_{OVDIS} even during occasional peaks of the load current.

Connecting a decoupling capacitor (C_{BATT}) on the BATT pin is needed if:

- The internal resistance of the storage element cannot sustain V_{OVDIS} with the load current peaks;
- The application expects a disconnection of the storage element (e.g., because of a user removable connector, or during manufacturing), as the BATT pin cannot be left floating;
- The application does not require a storage element (see Section 6.6).

If the AEM20941 is used with no storage element or with a high-ESR storage element, the minimum C_{BATT} value required for optimal operation without voltage drops below V_{OVDIS} is:

- 150 µF if the LDOs are used.
- 22 µF is the LDOs are not used.

3.6. Typical Characteristics

3.6.1. Boost Conversion Efficiency for LBOOST = 10 µH

The following graph shows the boost converter efficiency from SRC to BATT, with L_{BOOST} = 10 µH (Coilcraft LPS4018-103MRB), including the loss of efficiency due to the AEM20941 quiescent current.

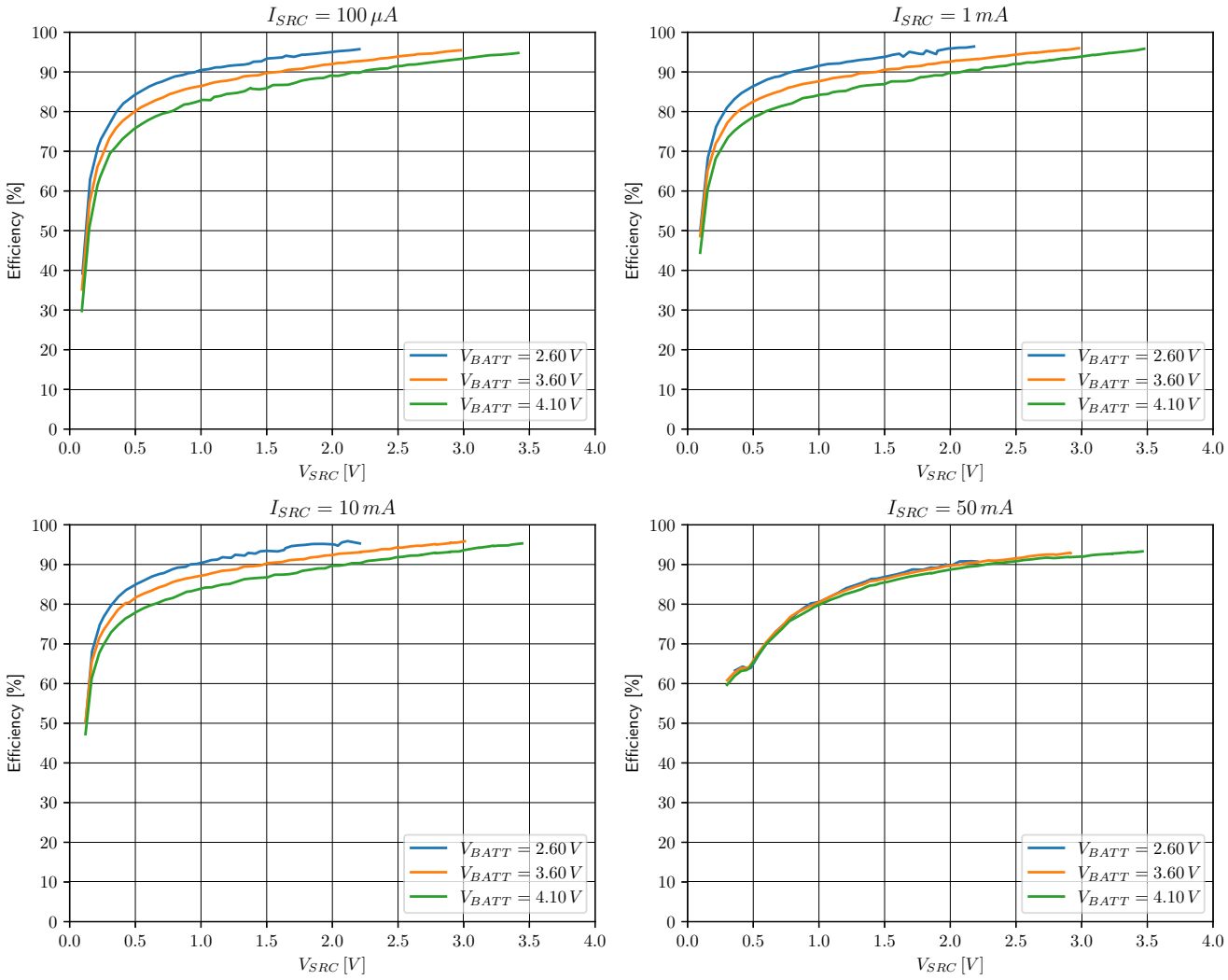


Figure 3: AEM20941 boost converter efficiency with LBOOST = 10 µH (Coilcraft LPS4018-103MRB)

3.6.2. Boost Conversion Efficiency for LBOOST = 22 µH

The following graph shows the boost converter efficiency from SRC to BATT, with L_{BOOST} = 22 µH (Coilcraft LPS4018-223MRB), including the loss of efficiency due to the AEM20941 quiescent current.

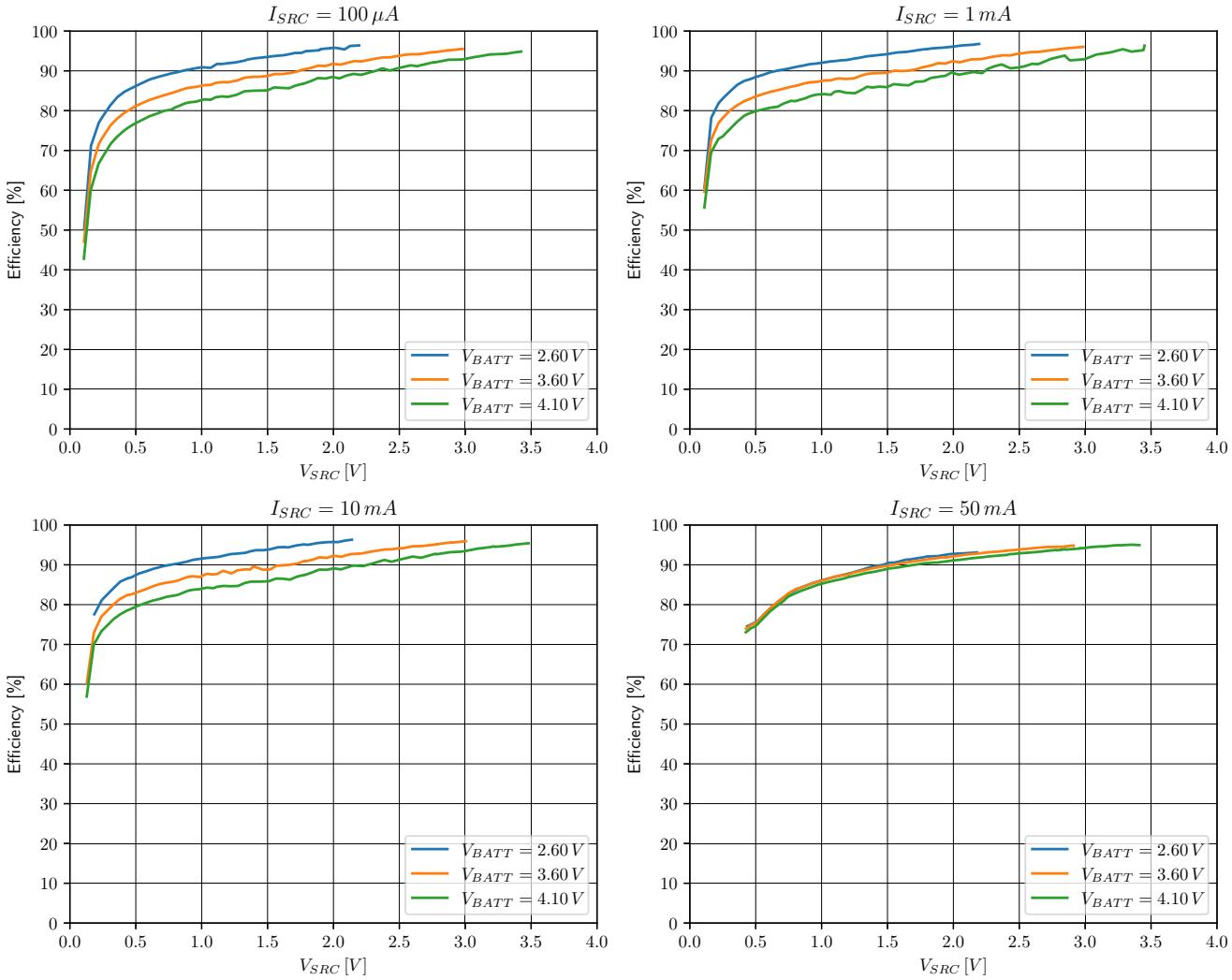


Figure 4: AEM20941 boost converter efficiency with LBOOST = 22 µH (Coilcraft LPS4018-223MRB)

3.6.3. Buck Conversion Efficiency

The following graph shows the buck converter efficiency from BATT to BUCK, with L_{BUCK} = 10 µH (TDK MLZ1608N100LT000), with the AEM20941 quiescent current I_Q subtracted.

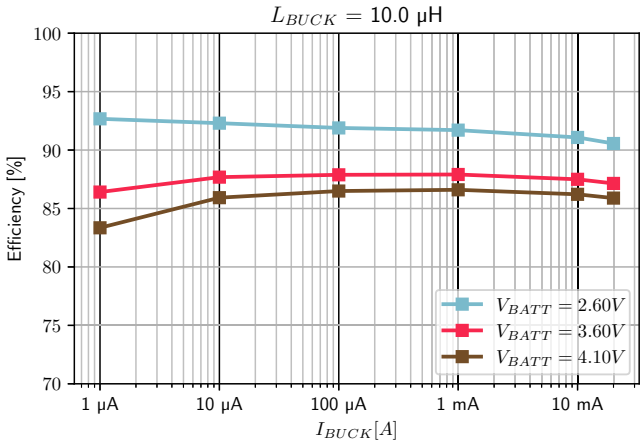


Figure 5: Buck converter efficiency with LBUCK = 10 µH (TDK MLZ1608N100LT000)

3.6.4. Quiescent Current

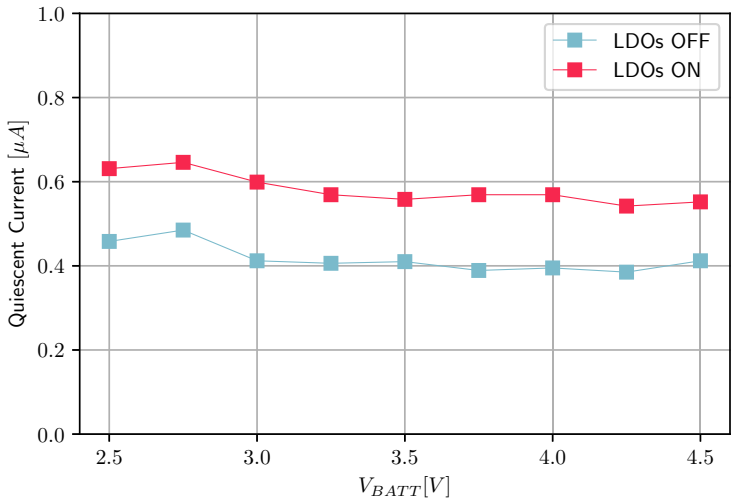


Figure 6: Quiescent current with LDOs on and off

3.6.5. High-voltage LDO Regulation

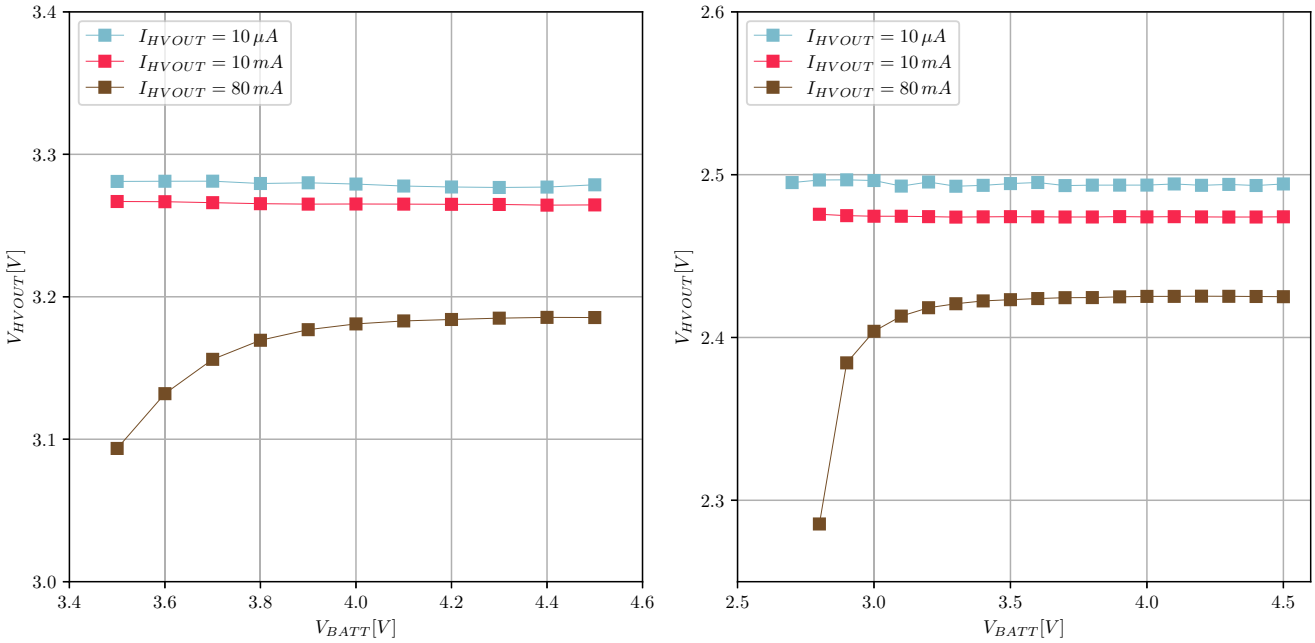


Figure 7: HVOUT at 3.3 V and 2.5 V

3.6.6. Low-voltage LDO Regulation

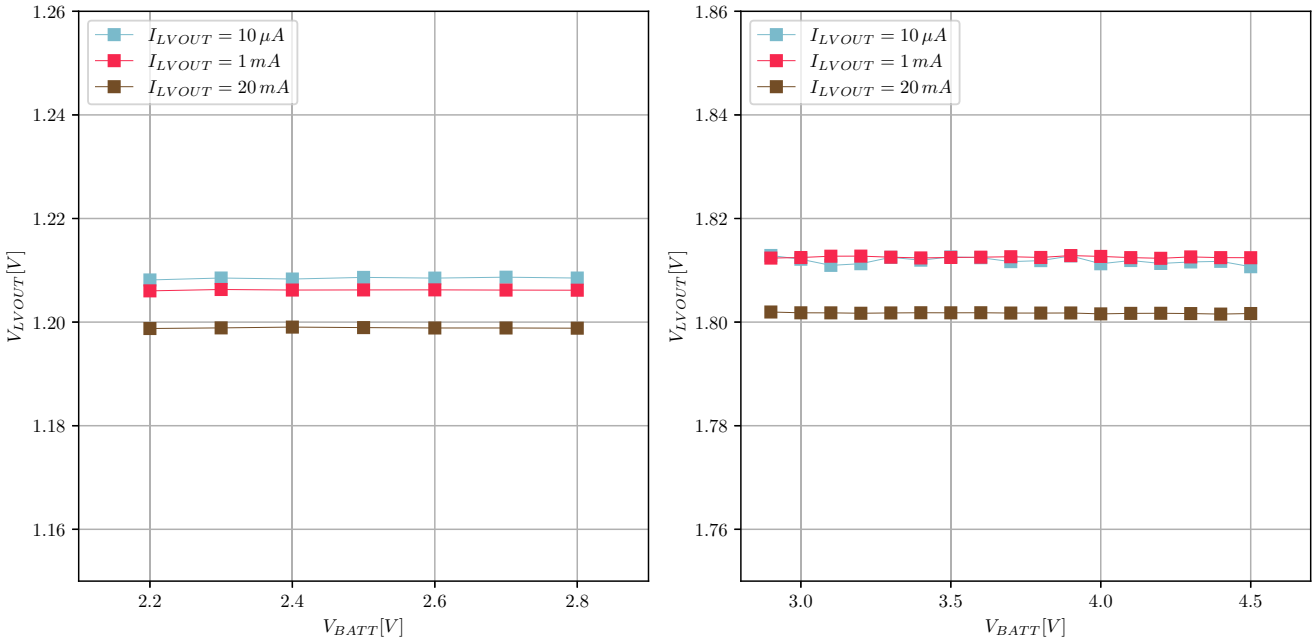


Figure 8: LVOUT at 1.2 V and 1.8 V

3.6.7. High-voltage LDO Efficiency

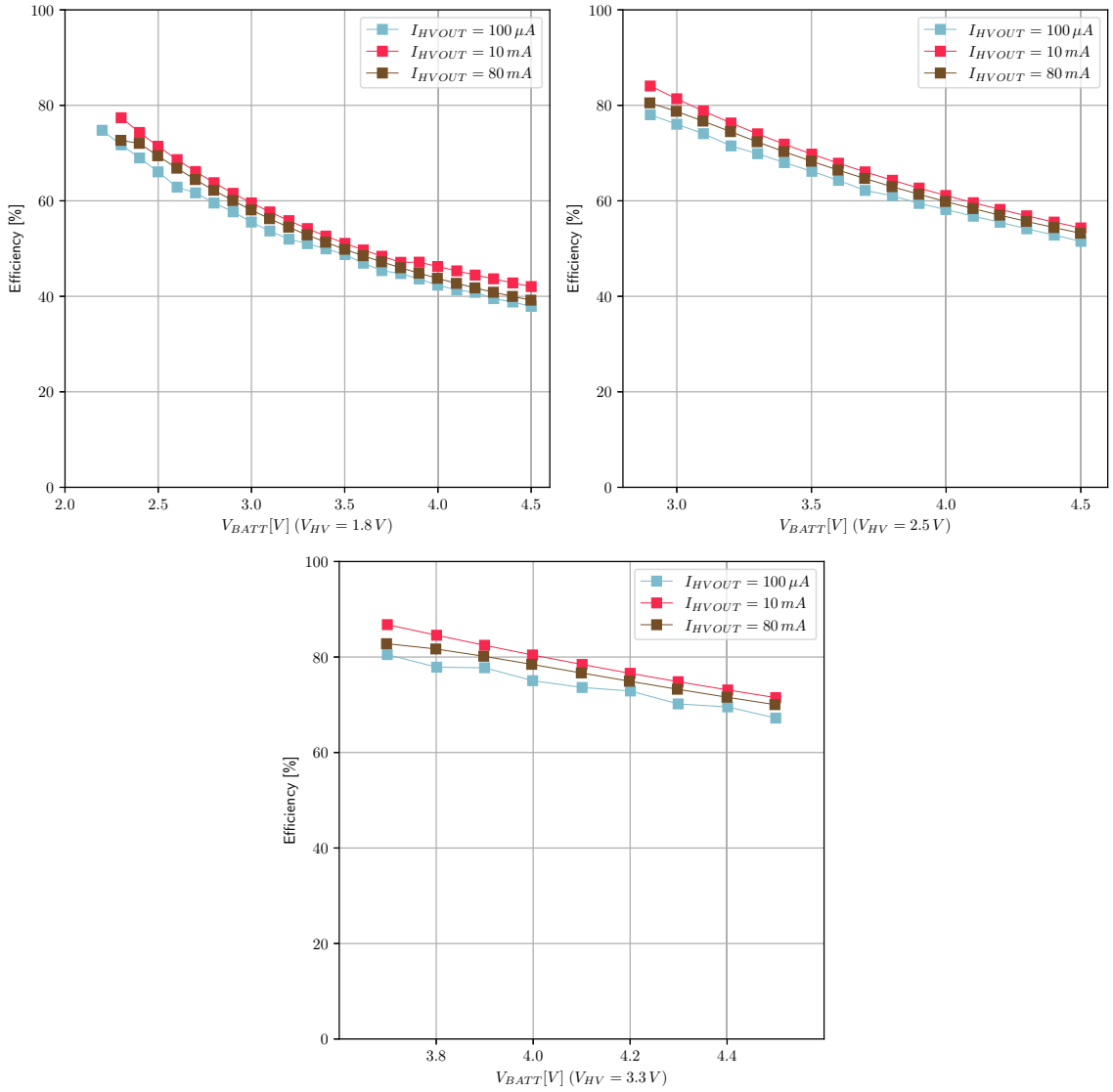


Figure 9: HVOUT efficiency at 1.8V, 2.5V and 3.3 V

The theoretical efficiency of an LDO can be calculated as Vout / Vin if quiescent current can be neglected with regards to the output current. For the high-voltage LDO, the theoretical efficiency is equal to V_{HV} / V_{BATT}.

3.6.8. Low-voltage LDO Efficiency

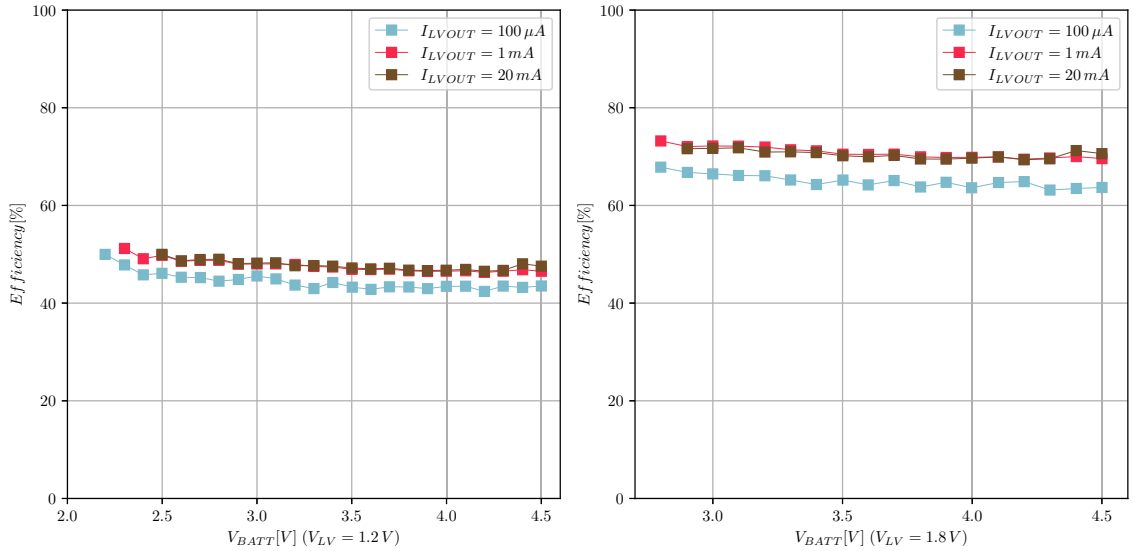


Figure 10: Efficiency of buck cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of an LDO can be calculated as V_{LV} / V_{BUCK}. Starting from the battery, the efficiency of the buck converter (ηbuck) has to be taken into account (see Figure 12).

The efficiency between V_{BATT} and V_{LV} is therefore equal to:

$$\eta_{BUCK} \cdot \frac{V_{LV}}{V_{BUCK}}$$

4. Functional Block Diagram

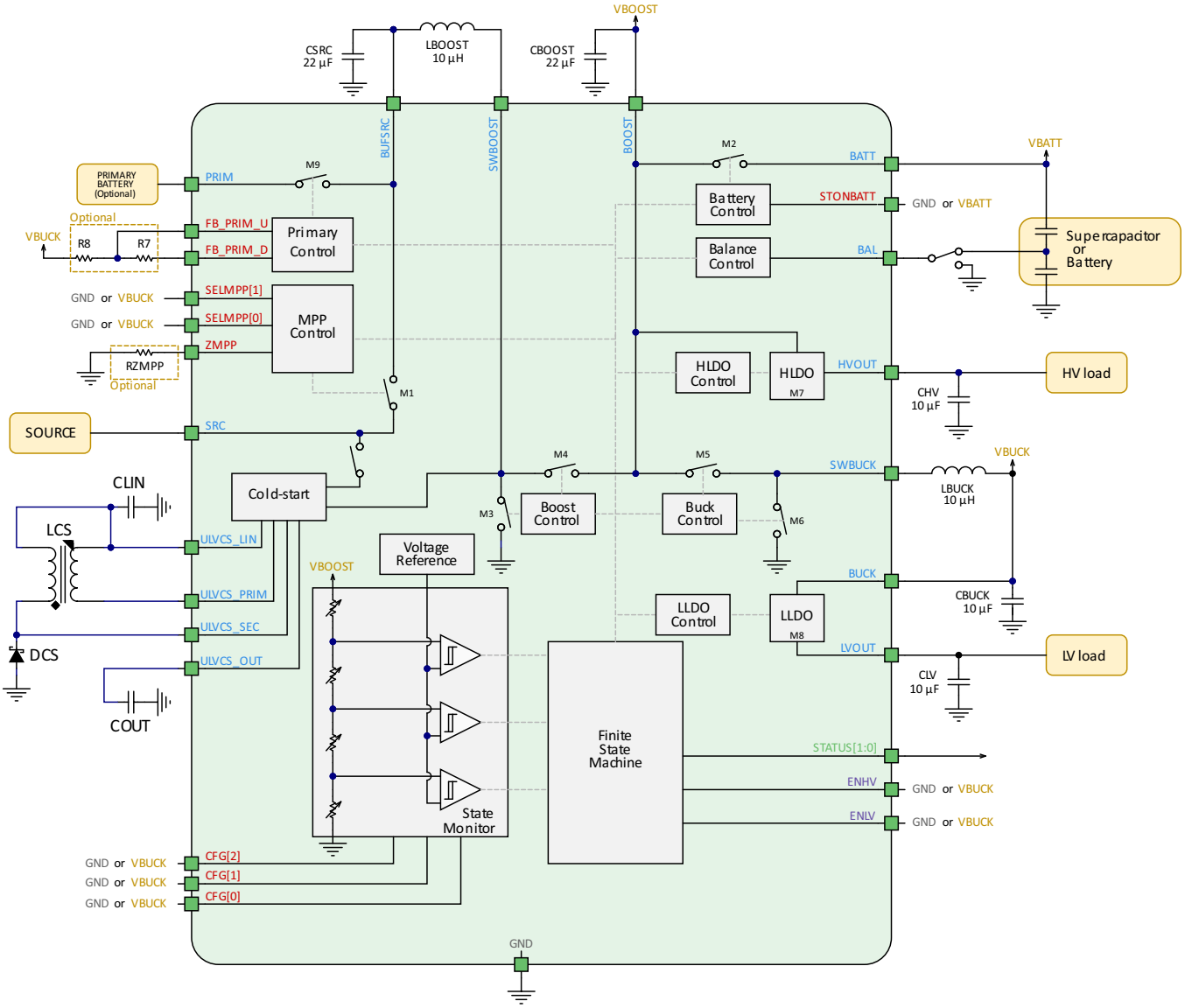


Figure 11: Functional block diagram

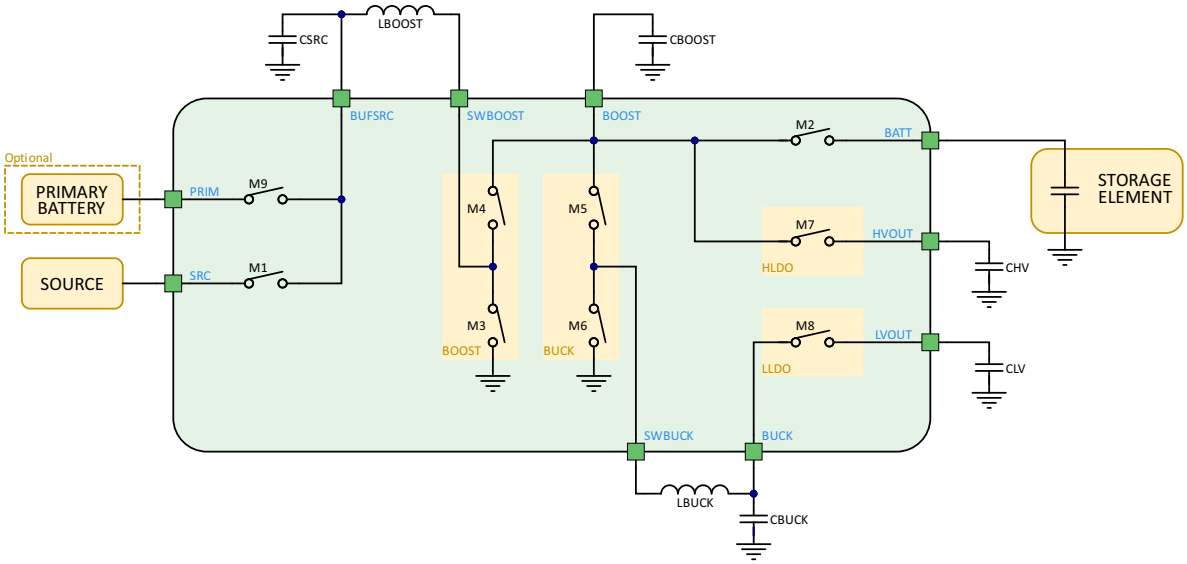


Figure 12: Simplified schematic view of the AEM20941

5. Theory of Operation

5.1. Power Converters

5.1.1. Boost Converter

The boost (or step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (V_{BOOST}) is available at the BOOST pin.

The switching transistors of the boost converter are M3 and M4, with the switching node available externally at SWBOOST. The reactive power components of this converter are the external inductor L_{BOOST} and the external capacitor C_{BOOST}.

The MPPT control circuit (see Section 5.3) periodically disconnects the source on SRC pin from the BUFSRC pin with the transistor M1 during $T_{MPPT,WAIT}$ in order to let the SRC voltage rise to the open-circuit voltage (V_{OC}). The AEM20941 then measures the open-circuit voltage of the harvester on SRC during $T_{MPPT,MEASURE}$ and define the new optimal SRC regulation voltage. This MPP evaluation is repeated every $T_{MPPT,PERIOD}$.

BUFSRC is decoupled by the capacitor C_{SRC}, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the BATT pin. Its voltage is named V_{BATT}. This node is linked to BOOST through the transistor M2. In NORMAL MODE (see Section 5.2.2), this transistor effectively shorts the battery to the BOOST node (V_{BATT} = V_{BOOST}). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the LDOs. M2 is opened to disconnect the storage element when V_{BATT} reaches V_{OVDIS}. However, in such a scenario, the AEM20941 offers the possibility of connecting a primary battery to recharge V_{BATT} up to V_{CHRDY}. In this case, the transistor M9 connects PRIM to BUFSRC and the transistor M1 is opened to disconnect the SRC input pin as explained in the PRIMARY BATTERY MODE section.

To ensure the boost converter operates correctly:

- when using PRIM as input of the boost converter (in PRIMARY BATTERY MODE), the voltage of the primary battery must remain below V_{OVDIS} + 0.4 V (see Table 6).
- when using SRC as input of the boost converter, the harvester maximum current must not exceed I_{SRC} maximum value (see Table 6).

More explanations about the different modes can be found in Section 5.2.

5.1.2. Buck Converter

The buck (or step-down) converter lowers the voltage from V_{BOOST} to a constant V_{BUCK} value of 2.2 V. This voltage is available at the BUCK pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at SWBUCK. The reactive power components of the buck converter are the external inductor L_{BUCK} and the external capacitor C_{BUCK}.

5.1.3. LDO Outputs

Two Low Drop-Out linear regulators are available to supply loads at different operating voltages:

- Through M7, BOOST supplies the high-voltage LDO that powers its load through HVOUT. This regulator delivers a clean voltage named V_{HV} of 1.8 V, 2.5 V or 3.3 V configured through CFG[2:0]. The output is decoupled by the external capacitor C_{HV}.
- Through M8, V_{BUCK} supplies the low-voltage LDO that powers its load through LVOUT. This regulator delivers a clean voltage named V_{LV} of 1.2 V or 1.8 V configured through CFG[2:0]. The output is decoupled by the external capacitor C_{LV}.

See Table 6 for HVOUT and LVOUT maximum current values (respectively I_{HV} and I_{LV}).

Both the high-voltage and the low-voltage outputs can be dynamically enabled or disabled respectively with the logic control pins ENHV and ENLV (see table below).

ENLV	LVOUT
L	Disabled
H	Enabled

ENHV	HVOUT
L	Disabled
H	Enabled

Table 8: LDOs configurations

5.2. Operating Modes

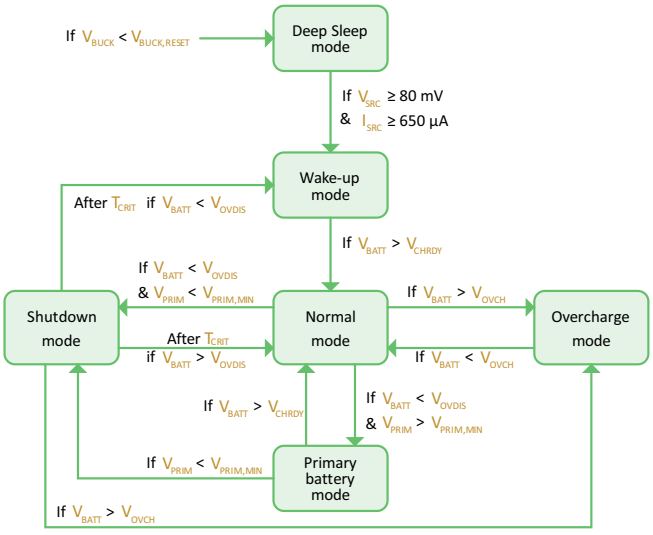


Figure 13: Diagram of the AEM20941 modes

5.2.1. Deep Sleep & Wake Up Modes

The DEEP SLEEP MODE is a state where all nodes are deeply discharged and there is no available energy to be harvested.

The AEM20941 enters DEEP SLEEP MODE if V_{BUCK} falls below $V_{BUCK,RESET}$ (see Table 6).

In this mode, as soon as the required cold-start voltage of 80 mV and the required current of 650 µA becomes available on SRC (with optional cold-start module), the WAKE-UP MODE is activated. V_{BOOST} and V_{BUCK} rise up to a voltage of 2.2 V. V_{BOOST} then rises up to V_{OVCH}.

At this stage, both LDOs are internally disabled. Therefore, STATUS[0] is low as shown in Figure 17 and Figure 18.

When V_{BOOST} reaches V_{OVCH}, two scenarios are possible:

- In the first scenario, a supercapacitor or a capacitor having a voltage lower than V_{CHRDY} is connected to the BATT node (see Section 5.2.1.2).
- In the second scenario, a charged battery is connected to the BATT node (see Section 5.2.1.3).

5.2.1.1. Wake Up Mode with the Optional Cold Start Module

The optional cold-start module is an internal self-oscillating circuit which allows to reduce the minimum input voltage required to coldstart the AEM.

During the cold start, the optional cold-start module input (ULVCS_LIN) is internally connected with the energy source (SRC). Once 80 mV and 650 µA are available on SRC, the cold-start module generates at least 380 mV on ULVCS_OUT to allow waking up the AEM.

Once V_{BOOST} and V_{BUCK} rise up to a voltage of 2.2 V (see Section 5.2.1), the AEM disconnects the link between ULVCS_LIN and SRC, and extract power directly from the input energy source through SRC.

If the optional cold-start module is not used on the application, ULVCS_OUT and SRC must be shorted and ULVCS_SEC, ULVCS_PRIM, and ULVCS_LIN left floating. In this condition, 380 mV and 105 µA are required to cold start the AEM.

5.2.1.2. Supercapacitor as a Storage Element

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges BATT from the input source and by modulating the conductance of M1 and M2. During the charge of the BATT node, both LDOs are disabled and STATUS[0] is low. When V_{BATT} reaches V_{CHRDY}, the circuit enters NORMAL MODE, STATUS[0] is asserted and the LDOs can be enabled by the user using ENLV and ENHV control pins as shown in Figure 17.

5.2.1.3. Battery as a Storage Element

If the storage element is a battery but its voltage is lower than V_{CHRDY}, the storage element first needs to be charged until it reaches V_{CHRDY}. This allows a safety margin to ensure that the storage element is able to provide the required power before enabling the outputs (LDOs).

Once V_{BATT} exceeds V_{CHRDY}, or if the battery was initially charged above V_{CHRDY}, the circuit enters NORMAL MODE. STATUS[0] is asserted and the LDOs can be dynamically enabled or disabled through ENLV and ENHV as shown in Figure 18.

5.2.2. Normal Mode

Once the AEM enters NORMAL MODE, it stays in this mode as long as the following condition is met:

$$V_{OVDIS} < V_{BATT} < V_{OVCH}$$

The AEM20941 will switch to another mode in the following cases:

- V_{BATT} increases above V_{OVCH} because the source provides more power than the load consumes. The circuit enters OVERCHARGE MODE, as explained in Section 5.2.3.
- V_{BATT} falls below V_{OVDIS} due to a lack of power from the source. In this case, either the circuit enters SHUTDOWN MODE as explained in Section 5.2.5, or, if a charged primary battery is connected on PRIM, the circuit enters PRIMARY BATTERY MODE as explained in Section 5.2.4.

5.2.3. Overcharge Mode

When V_{BATT} reaches V_{OVCH}, the battery charge is complete. The AEM maintains V_{BATT} around V_{OVCH}, with an hysteresis of a few mV as shown in Figure 19, to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain V_{BATT} and the LDO output voltages are available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 12 is opened to prevent current from the source to the storage element when V_{SRC} is higher than V_{OVCH}.

5.2.4. Primary Battery Mode

When V_{BATT} drops below V_{OVDIS}, the circuit compares the voltage on PRIM with the voltage on FB_PRIM_U to determine whether a charged primary battery is connected on PRIM. The voltage on FB_PRIM_U is set thanks to two optional resistors as explained in Section 6.3.

If the following formula is true, the circuit considers the primary battery as available and the circuit enters PRIMARY BATTERY MODE.

$$\frac{V_{PRIM}}{4} > V_{FB\_PRIM\_U}$$

In that mode, transistor M1 is opened and the primary battery is connected to BUFSRC through transistor M9 to become the source of energy of the AEM20941. STATUS[1] is asserted as long as the chip is in PRIMARY BATTERY MODE.

The AEM remains in this mode until:

- V_{BATT} reaches V_{CHRDY}. At that point, the circuit enters NORMAL MODE.
- The primary battery is depleted (above formula becomes false). The circuit switches to SHUTDOWN MODE.

If no primary battery is used in the application, PRIM, FB_PRIM_U and FB_PRIM_D must be tied to GND.

5.2.5. Shutdown Mode

When V_{BATT} drops below V_{OVDIS} and no power is available from a primary battery, the circuit enters SHUTDOWN MODE, as shown in Figure 20, to prevent deep discharge that could damage the storage element and make the LDOs unstable. The circuit asserts STATUS[1] to warn the application that a shutdown may occur. Both LDO regulators remain enabled during T_{CRIT} (about 600 ms).

If no primary battery is used, this mechanism allows the application circuit, whether it is powered on LVOUT or HVOUT, to trigger an interrupt by the low to-high transition of STATUS[1], and to take all appropriate actions before LVOUT and HVOUT are disabled.

After T_{CRIT}:

- If V_{BATT} has recovered above V_{OVDIS}, the AEM switches back to NORMAL MODE.
- If V_{BATT} has not recovered above V_{OVDIS}, the circuit enters WAKE-UP MODE. Both LDOs are disabled and BATT is disconnected from BOOST to avoid damaging the battery due to the over-discharge. From now on, the AEM must go through the wake-up procedure described in the Section 5.2.1.

If V_{BATT} reaches V_{OVCH} while in SHUTDOWN MODE, the AEM20941 switches directly to OVERCHARGE MODE without waiting the end of T_{CRIT}.

5.3. Maximum Power Point Tracking

During NORMAL MODE, SHUTDOWN MODE and a part of WAKE-UP MODE, the boost converter is regulated thanks to an internal MPPT (Maximum Power Point Tracking) module. V_{MPP} is the voltage level of the MPP, and depends on the input power available at the source.

The MPPT module evaluates V_{MPP} as a constant fraction of the open-circuit voltage of the source V_{OC}. The ratio between V_{MPP} and V_{OC} can be configured with the SELMPP[1:0] pins.

The AEM20941 periodically measures V_{OC} by stopping to pull current from the source (SRC) during $T_{MPPT,WAIT}$ (328 ms), thus, letting the source rise to its open-circuit voltage, then measures V_{OC} during $T_{MPPT,MEASURE}$ (1.2 ms). The source target regulation voltage V_{MPP} is then redefined as a fraction of the measured V_{OC}. The evaluation is repeated every $T_{MPPT,PERIOD}$ (21 s). This way, the MPPT module adapts to the harvester variations due to varying ambient conditions.

With the exception of this MPP evaluation process, the source voltage V_{SRC} is continuously compared to V_{MPP}:

- When V_{SRC} exceeds V_{MPP} by a small hysteresis, the boost converter is switched on, extracting electric charges from the source, thus lowering its voltage.
- When V_{SRC} falls below V_{MPP} by a small hysteresis, the boost converter is switched off, allowing the harvester to accumulate new electric charges into C_{SRC}, which voltage rises.

This way, the boost converter regulates its input voltage so that the electric current (or flow of electric charges) that enters the boost converter yields the best power transfer from the harvester under any ambient conditions. The AEM20941 supports any V_{MPP} level in the range from 80 mV to 3.5 V. It offers a choice of three values for the V_{MPP} / V_{OC} ratio through the configuration pins SELMPP[1:0] as shown in Table 10. It is also possible to regulate the source voltage by matching the input impedance of the BOOST converter with an impedance connected to the ZMPP terminal thanks to the ZMPPT feature, by setting SELMPP[1:0] to HH (see Section 6.4).

5.4. Storage Element Balancing Circuit for Dual-cell Supercapacitor

When using a dual-cell supercapacitor (with the cells in series) it is necessary to keep both cells at similar voltages to avoid damage due to a potential over-voltage on one cell. This is ensured by the AEM20941 storage element balancing circuit (BAL pin).

If a battery, a capacitor or a single-cell supercapacitor is connected on BATT, the balancing circuit is not needed. BAL must be connected to GND to disable the storage element balancing circuit.

If a dual-cell supercapacitor is connected on BATT, BAL must be connected to the node between the two cells of the supercapacitor. The storage element balancing circuit compensates for any mismatch of the two cells that could overcharge one of the two cells. It ensures that BAL voltage remains close to V_{BATT} / 2.

The balancing circuit works as follows:

- The balancing circuit is enabled only when $V_{BAL} > V_{BAL,MIN}$ (see Table 6).
- If $V_{BAL} > \frac{V_{BATT}}{2}$: the AEM20941 enables a switch between BAL and GND to momentarily discharge the bottom cell to GND until balance is restored.
- If $V_{BAL} < \frac{V_{BATT}}{2}$: the AEM20941 enables a switch between BATT and BAL to transfer charge from the top cell to the bottom cell until balance is restored.

6. System Configuration

6.1. Battery and LDOs Configuration

Configurations pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell supercapacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Reserved for future use.					

Table 9: Usage of CFG[2:0]

DISCLAIMER: storage element thresholds provided in the table above are indicative to support a wide range of storage element variants. They are provided as is to the best knowledge of e-peas's application laboratory. They should not replace the actual values provided in the storage element manufacturer's specifications and datasheet.

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, as shown in Table 9, without any dedicated external component. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling the boost converter.
- V_{CHRDY}: minimum voltage required on the storage element after a cold start before enabling the LDOs.
- V_{OVDIS}: minimum voltage accepted on the storage element before considering the storage element as depleted.

See Section 5 for more information about the purposes of these thresholds.

The two LDOs output voltages are called V_{HV} and V_{LV} for the high and low output voltages respectively. Seven combinations of these voltage levels are hard-wired and selectable through the CFG[2:0] configuration pins, covering most application cases.

6.2. MPPT Configuration

Two dedicated configuration pins, SELMPP[1:0], allow selecting the MPP tracking ratio based on the characteristic of the input power source.

Configuration pins		MPPT ratio
SELMPP[1]	SELMPP[0]	V_{MPP} / V_{OC}
L	L	50%
L	H	55%
H	L	75%
H	H	ZMPPT

Table 10: Usage of SELMPP[1:0]

6.3. Primary Battery Configuration

To use the primary battery, it is mandatory to determine $V_{PRIM,MIN}$, the voltage at which the primary battery is considered as fully depleted. The circuit uses a resistive divider between BUCK and FB_PRIM_D to define the voltage on FB_PRIM_U as $V_{PRIM,MIN}$ divided by 4. During $V_{PRIM,MIN}$ evaluation, the circuit connects FB_PRIM_D to GND. When $V_{PRIM,MIN}$ is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. The resistors are calculated as follows:

- $R_P = R7 + R8$
- $100k\Omega \leq R_P \leq 500k\Omega$
- $R7 = \frac{V_{PRIM\_MIN}}{4} \cdot R_P \cdot \frac{1}{2.2V}$
- $R8 = R_P - R7$

NOTE: FB_PRIM_U, FB_PRIM_D and PRIM must be tied to GND if no primary battery is used.

6.4. ZMPPT Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM20941 can regulate the input impedance of the BOOST converter so that it matches a constant impedance (R_{ZMPP}) connected between the ZMPP pin and GND. In this case, the AEM20941 regulates V_{SRC} at a voltage equal to the product of the ZMPP impedance and the current available at the SRC input.

- $10\Omega \leq R_{ZMPP} \leq 1M\Omega$

6.5. Start-on-battery Configuration

Alternatively to the cold start procedure described in Section 5.2.1, by connecting STONBATT to BATT, the circuit can also start with the energy provided by the storage element connected on BATT if its voltage is higher than V_{CHRDY}.

NOTE: When using start-on-battery feature and no power is available on the SRC, the AEM20941 will not start if the voltage on BATT is lower than V_{CHRDY}.

6.6. No-battery Configuration

If the application does not use a storage element, the PCB must include a capacitor on the BATT pin. See Section 3.5.3 for C_{BATT} value.

The storage element may not be necessary in the following cases:

- If the harvested energy source is permanently available and covers the application purposes.
- If the application does not need to store energy when the harvested energy source is not available.

6.7. Supplying an Application Circuit with BUCK

It is possible to supply an application circuit directly from BUCK, with the benefit of high BATT to BUCK efficiency, provided that the following conditions are met:

- The application circuit can be supplied from a voltage in the 2.0 V - 2.5 V range (V_{BUCK} is typically 2.2 V with ripple, see Table 6).
- The sum of the following currents must be below the maximum I_{BUCK} value (see Table 6):
  - Current of the load connected to BUCK.
  - Current of the load connected to LVOUT.
- The application circuit on BUCK does not pull current during the AEM20941 cold start.

To satisfy the last condition, the following circuit may be implemented:

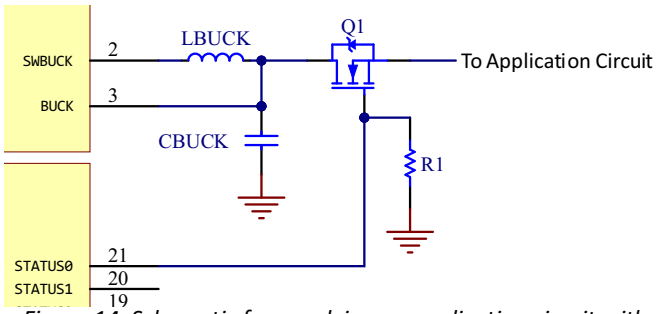


Figure 14: Schematic for supplying an application circuit with BUCK

Q1 is a N-MOSFET, whose gate is driven by STATUS[0] with R1 as a pull-down resistor. When the AEM20941 is in DEEP SLEEP MODE or in WAKE-UP MODE, STATUS[0] is LOW (see Section 5.2), ensuring that Q1 is non-conducting, and thus that the application circuit is not supplied.

When the AEM20941 switches from WAKE-UP MODE to NORMAL MODE, STATUS[0] is HIGH, making Q1 conducting. The application circuit is then supplied by BUCK, and remains so when the AEM20941 is in NORMAL MODE, OVERCHARGE MODE, PRIMARY BATTERY MODE and SHUTDOWN MODE.

Q1 must be chosen as follows:

- Low Gate-Source Leakage I_{GSS}.
- Low Zero Gate Voltage Drain Current I_{DSS}.
- Drain-Source On-State Resistance $R_{DS(on)}$ low enough to supply application circuit with an acceptable voltage drop.
- V_{GS} maximum voltage must be above V_{OVCH} (STATUS[0] HIGH voltage is V_{BOOST}).
- Maximum gate-source threshold voltage $V_{GS(th),MAX}$ matches the following, with $V_{BUCK,MAX}$ being V_{BUCK} maximum value stated in Table 6:

$$V_{GS(th),MAX} < V_{OVDIS} - V_{BUCK,MAX}$$

7. Typical Application Circuits

7.1. Example Circuit 1

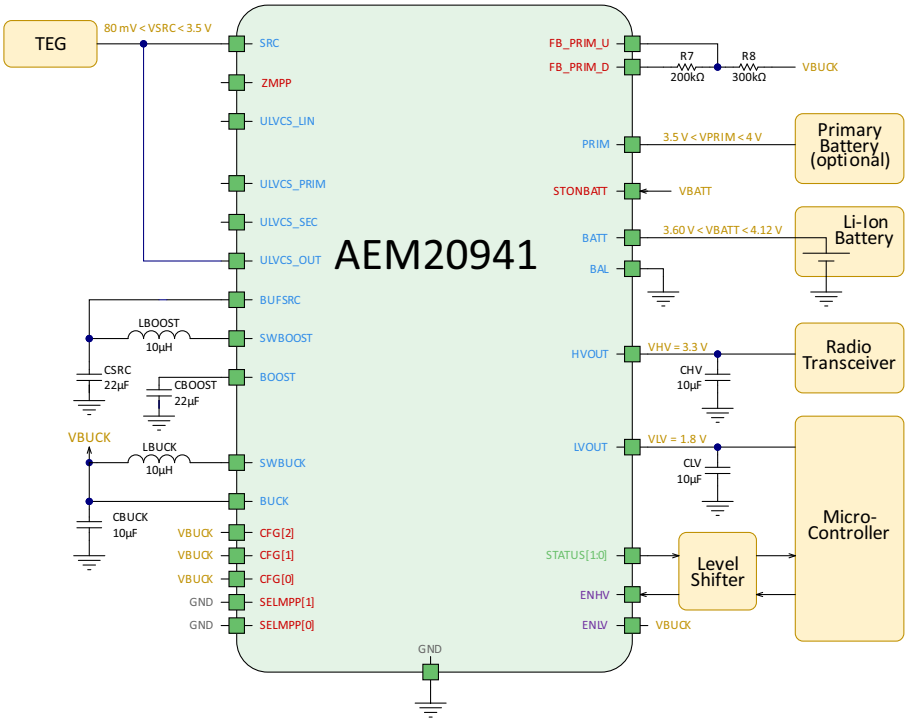


Figure 15: Typical application circuit 1

The energy source is a thermoelectric generator and the storage element is a standard Li-ion battery cell. The radio communication is supplied by HVOUT set at 3.3 V. The micro-controller that controls the application is supplied by LVOUT set at 1.8 V.

STONBATT is tied to V_{BATT}, bypassing the cold-start procedure, to start thanks to the energy stored in the pre-charged Li-ion battery cell.

With the start-on-battery feature enabled, the optional cold-start module is not useful for this application, ULVCS_OUT and SRC are shorted and ULVCS_SEC, ULVCS_PRIM, and ULVCS_LIN are left floating.

This circuit uses a pre-defined AEM configuration, typical of systems that use standard components for radio and energy storage.

The operating mode pins are set as follows:

- CFG[2:0] = HHH (all to V_{BUCK})

Referring to Table 9, in this mode, the threshold voltages are:

- V_{OVCH} = 4.12 V
- V_{CHRDY} = 3.67 V
- V_{OVDIS} = 3.60 V

Moreover, the LDOs output voltages are:

- V_{HV} = 3.3 V
- V_{LV} = 1.8 V

A primary battery is also connected as a back-up solution. The minimal level allowed on this battery is set at 3.5 V. Following equations from Section 6.3:

- $R_P = 0.5M\Omega$
- $R7 = \frac{3.5V}{4} \cdot 0.5M\Omega \cdot \frac{1}{2.2V} = 200k\Omega$
- $R8 = 0.5M\Omega - 200k\Omega = 300k\Omega$

The MPPT configuration pins SELMPP[1:0] are tied to GND (logic LOW), thus, selecting an MPPT ratio of 50%.

The LVOUT LDO output is enabled by tying ENLV to V_{BUCK}.

The micro-controller is supplied by LVOUT, that is enabled when V_{BATT} and V_{BOOST} voltage rise above V_{CHRDY}.

The application software can enable or disable the radio transceiver supply with a GPIO connected to ENHV.

7.2. Example Circuit 2

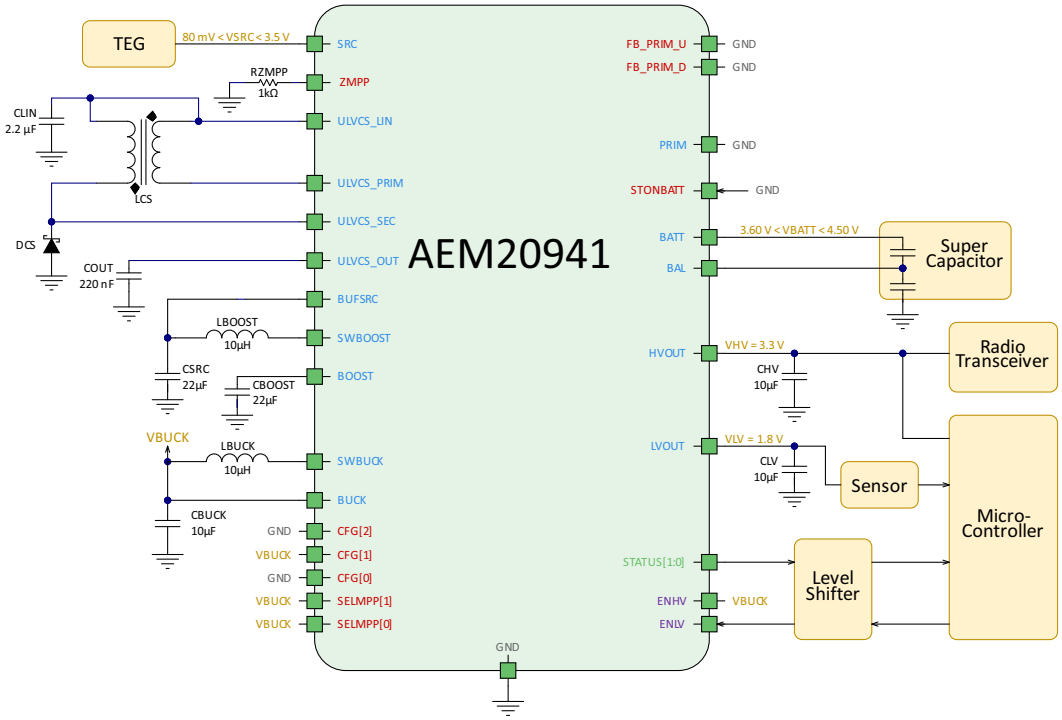


Figure 16: Typical application circuit 2

The energy source is a thermoelectric generator and the storage element is a dual-cell supercapacitor. Please note that the supercapacitor might be completely depleted during the cold start. Consequently, STONBATT is tied to GND to use the SRC energy only.

To decrease the minimum voltage required to coldstart, the optional cold-start module is used.

Moreover, BAL is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and, in that way, protect the supercapacitor.

A micro-controller acts as the application master. The operating mode pins are set as follows:

- CFG[2:0] = LHL

Referring to Table 9, in this mode, the threshold voltages are:

- V_{OVCH} = 4.50 V
- V_{CHRDY} = 3.92 V
- V_{OVDIS} = 3.60 V

The LDO voltages are set as follows:

- V_{HV} = 3.3 V
- V_{LV} = 1.8 V

LVOUT output enabling/disabling is controlled by the application circuit with a micro-controller GPIO connected to ENLV.

ENHV is tied to V_{BUCK} so that HVOUT is always on.

The micro-controller is supplied by HVOUT, which is enabled when V_{BATT} and V_{BOOST} voltages rise above V_{CHRDY}.

The MPPT configuration pins SELMPP[1:0] are tied to V_{BUCK} (logic HIGH), thus, selecting the ZMPPT configuration to match a 1-kΩ impedance.

No primary battery is connected: PRIM, FB_PRIM_U and FB_PRIM_D pins are tied to GND.

8. Circuit Behavior

8.1. Cold-start Behavior with a (Super)Capacitor as Storage Element

8.1.1. Configuration

- CFG[2:0] = LHL
  - V_{OVCH} = 4.50 V
  - V_{CHRDY} = 3.92 V
  - V_{OVDIS} = 3.60 V
  - V_{HV} = 3.3 V
  - V_{LV} = 1.8 V
- C_{BATT} = 4.85 mF
- SELMPP[1:0] = HL
  - V_{MPP}/V_{OC} ratio = 75%
- SRC: 1 mA current source with 3 V voltage compliance
  - V_{OC} = 3.0 V
  - V_{MPP} = 2.25 V
  - I_{SRC} = 1 mA
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

8.1.2. Observations

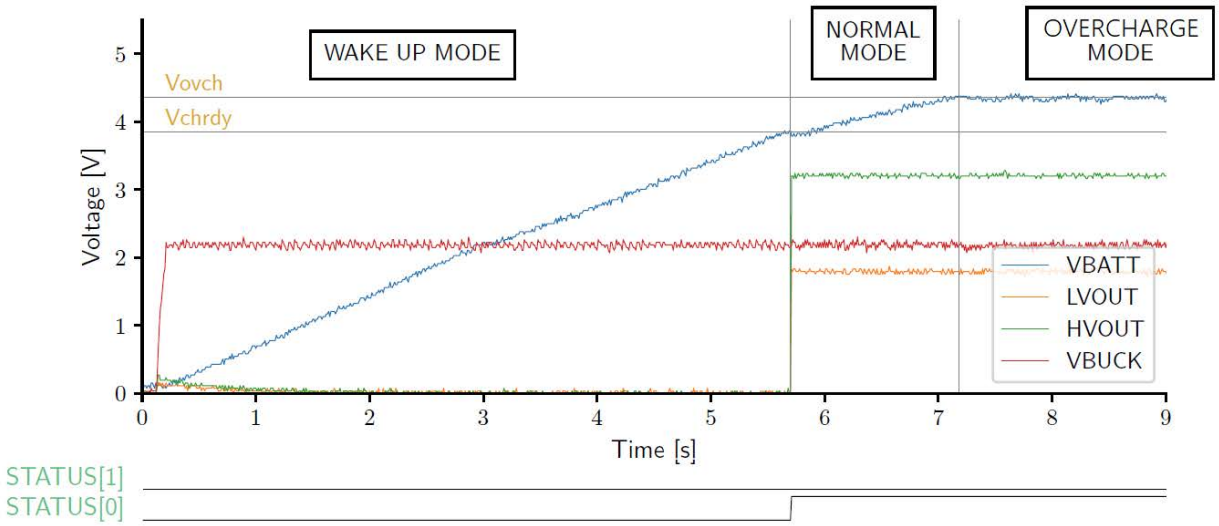


Figure 17: Cold start with a capacitor connected to BATT

- The AEM20941 is initially in DEEP SLEEP MODE with all nodes fully discharged. As soon as the current source is connected on SRC, the AEM20941 switches to WAKE-UP MODE, V_{BUCK} rises to its regulation voltage (around 2.2 V), and the storage element connected on BATT starts to be charged.
- Once V_{BATT} reaches V_{CHRDY}, the AEM20941 switches to NORMAL MODE, STATUS[0] is asserted and the LDOs are enabled. V_{HV} and V_{LV} are respectively regulated to 3.3 V and 1.8 V.
- Once V_{BATT} reaches V_{OVCH}, the AEM20941 switches to OVERCHARGE MODE. The voltage on BATT is maintained around V_{OVCH}. V_{BUCK}, V_{HV} and V_{LV} remain regulated.

8.2. Cold-start Behavior with a Battery as Storage Element

8.2.1. Configuration

- CFG[2:0] = HHH
  - V_{OVCH} = 4.12 V
  - V_{CHRDY} = 3.67 V
  - V_{OVDIS} = 3.60 V
  - V_{HV} = 3.3 V
  - V_{LV} = 1.8 V
- C_{BATT} = 4.85 mF (pre-charged capacitor acting as a battery
- SELMPP[1:0] = HL
  - V_{MPP}/V_{OC} ratio = 75%
- SRC: 1 mA current source with 3 V voltage compliance
  - V_{OC} = 3.0 V
  - V_{MPP} = 2.25 V
  - I_{SRC} = 1 mA
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

8.2.2. Observations

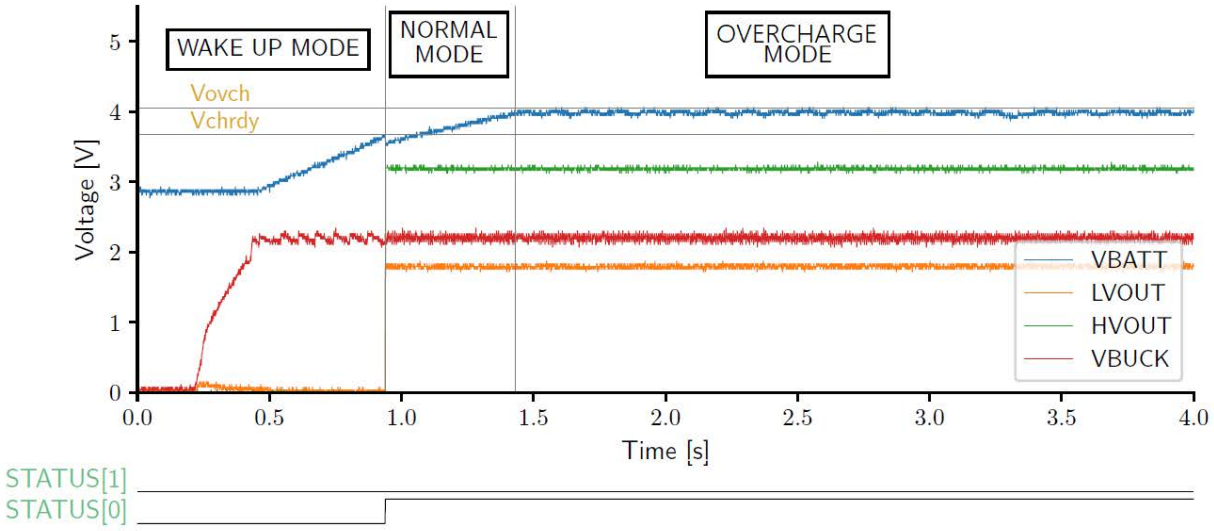


Figure 18: Cold start with a battery connected to BATT

- The AEM20941 is initially in DEEP SLEEP MODE with all nodes fully discharged except V_{BATT} which is pre-charged. As soon as the current source is connected on SRC, the AEM20941 switches to WAKE-UP MODE, V_{BUCK} rises to its regulation voltage (around 2.2 V), and the storage element connected on BATT starts to be charged.
- Once V_{BATT} reaches V_{CHRDY}, the AEM20941 switches to NORMAL MODE, STATUS[0] is asserted and the LDOs are enabled. V_{HV} and V_{LV} are respectively regulated to 3.3 V and 1.8 V.
- Once V_{BATT} reaches V_{OVCH}, the AEM20941 switches to OVERCHARGE MODE. The voltage on BATT is maintained around V_{OVCH}. V_{BUCK}, V_{HV} and V_{LV} remain regulated.

8.3. Overcharge Mode Behavior

8.3.1. Configuration

- CFG[2:0] = HHH
  - V_{OVCH} = 4.12 V
  - V_{CHRDY} = 3.67 V
  - V_{OVDIS} = 3.60 V
  - V_{HV} = 3.3 V
  - V_{LV} = 1.8 V
- C_{BATT} = 4.85 mF
- SELMPP[1:0] = HL
  - V_{MPP}/V_{OC} ratio = 75%
- SRC: 1 mA current source with 3 V voltage compliance
  - V_{OC} = 3.0 V
  - V_{MPP} = 2.25 V
  - I_{SRC} = 1 mA
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT

8.3.2. Observations

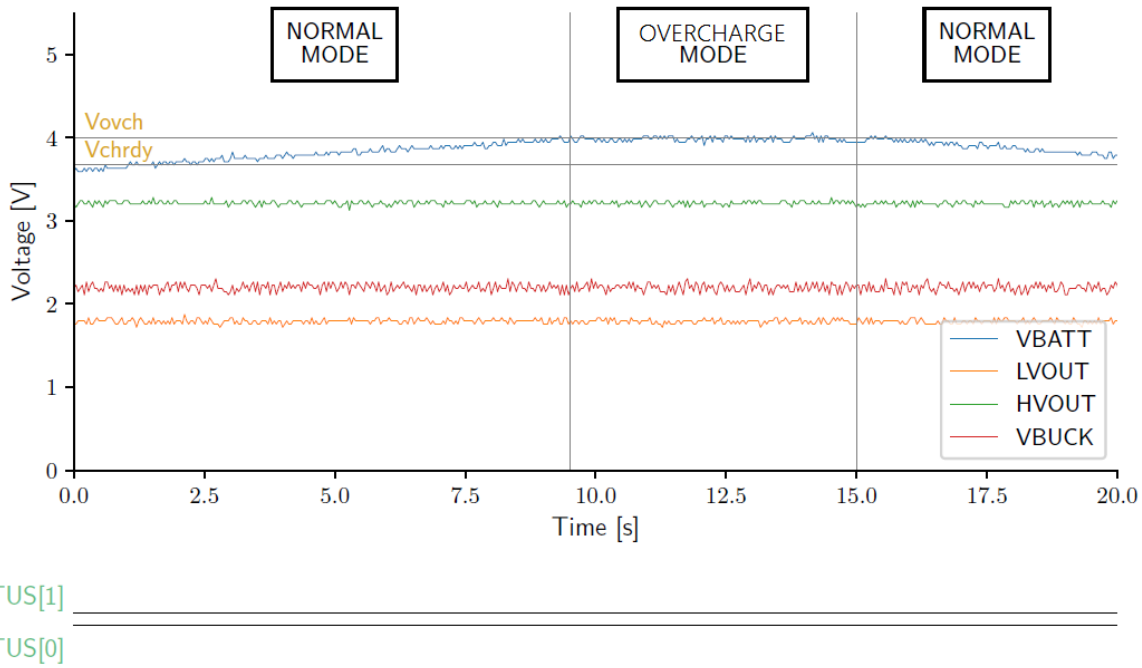


Figure 19: Overcharge mode

- The AEM20941 is initially in NORMAL MODE, with STATUS[0] asserted, and V_{BUCK}, V_{HV} and V_{LV} regulated.
- Thanks to the current source connected on SRC, V_{BATT} is being charged.
- Once V_{BATT} reaches V_{OVCH}, the AEM20941 enters OVERCHARGE MODE and maintain V_{BATT} around V_{OVCH} to avoid damaging the storage element.
- Near 15 s, the current source is disconnected from SRC. The AEM20941 maintain the two LDOs supplied, causing the storage element to discharge. The AEM20941 switches back to NORMAL MODE.

8.4. Shutdown Mode Behavior

8.4.1. Configuration

- CFG[2:0] = LHL
  - V_{OVCH} = 4.50 V
  - V_{CHRDY} = 3.92 V
  - V_{OVDIS} = 3.60 V
  - V_{HV} = 3.3 V
  - V_{LV} = 1.8 V
- C_{BATT} = 4.85 mF
- SELMPP[1:0] = HL
  - V_{MPP}/V_{OC} ratio = 75%
- SRC: left floating to let the storage element on BATT discharge
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT
- PRIM, FB_PRIM_U and FB_PRIM_D connected to GND (no primary battery)

8.4.2. Observations

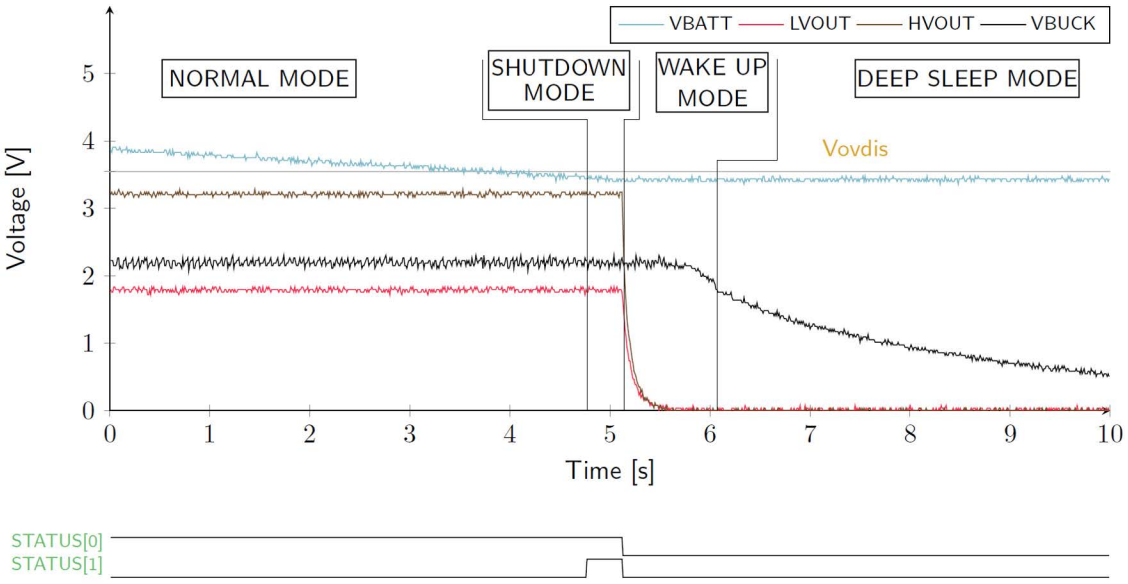


Figure 20: Shutdown mode (without primary battery)

- The AEM20941 is initially in NORMAL MODE, with STATUS[0] asserted, V_{BUCK}, V_{HV} and V_{LV} regulated. The SRC pin is left floating, which result in the storage element discharging through the loads.
- Once V_{BATT} reaches V_{OVDIS}, the AEM20941 enters SHUTDOWN MODE and maintain the load outputs regulated. STATUS[1] is asserted to warn the user that a shutdown may occur.
- After T_{CRIT} (approximately 600 ms), V_{BATT} has not recovered above V_{OVDIS}. The AEM20941 disables the LDOs and enters WAKE-UP MODE. To avoid further discharging the storage element, BATT is disconnected from BOOST. The pins STATUS[1] and STATUS[0] are set LOW.
- Near 6.1 s, V_{BUCK} falls below $V_{BUCK,RESET}$. The AEM20941 enters DEEP SLEEP MODE and must go through the cold-start procedure again.

8.5. Primary Battery Mode Behavior

8.5.1. Configuration

- CFG[2:0] = HHH
  - V_{OVCH} = 4.12 V
  - V_{CHRDY} = 3.67 V
  - V_{OVDIS} = 3.60 V
  - V_{HV} = 3.3 V
  - V_{LV} = 1.8 V
- C_{BATT} = 4.85 mF
- SELMPP[1:0] = HL
  - V_{MPP}/V_{OC} ratio = 75%
- SRC: 1 mA current source with 3 V voltage compliance (initially disconnected)
  - V_{OC} = 3.0 V
  - V_{MPP} = 2.25 V
  - I_{SRC} = 1 mA
- ENHV = ENLV = H
- 22 kΩ resistive load on LVOUT
- 2 kΩ resistive load on HVOUT
- PRIM: 3 V voltage source with 1 mA current compliance
  - R7 = 68 kΩ
  - R8 = 330 kΩ
  - $V_{PRIM,MIN}$ = 1.50 V

8.5.2. Observations

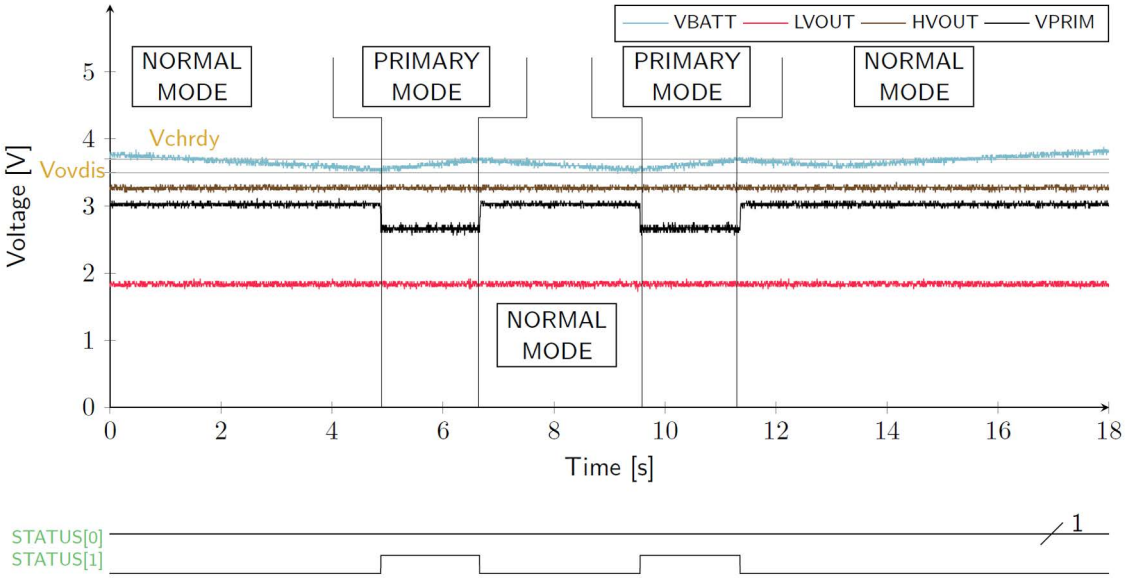


Figure 21: Switching to primary battery when battery is overdischarged

- The AEM20941 is initially in NORMAL MODE, with STATUS[0] asserted, V_{BUCK}, V_{HV} and V_{LV} regulated.
- The SRC is left floating, causing the storage element to discharge.
- Once V_{BATT} reaches V_{OVDIS}, the AEM20941 compares the voltage on PRIM to $V_{PRIM,MIN}$. Since V_{PRIM} is higher, the AEM enters PRIMARY BATTERY MODE and, the primary battery is used to recharge the storage element until V_{BATT} reaches V_{CHRDY} again.
- STATUS[1] is asserted as long as the AEM20941 is in PRIMARY BATTERY MODE.
- Once V_{BATT} reaches V_{CHRDY}, the AEM20941 goes back into NORMAL MODE. Since the SRC is still floating, the same behavior repeats.
- Near 13 s, while the storage element is discharging in NORMAL MODE, the current source is connected on SRC. This allows charging the storage element so the primary battery is not used anymore.

9. Schematic

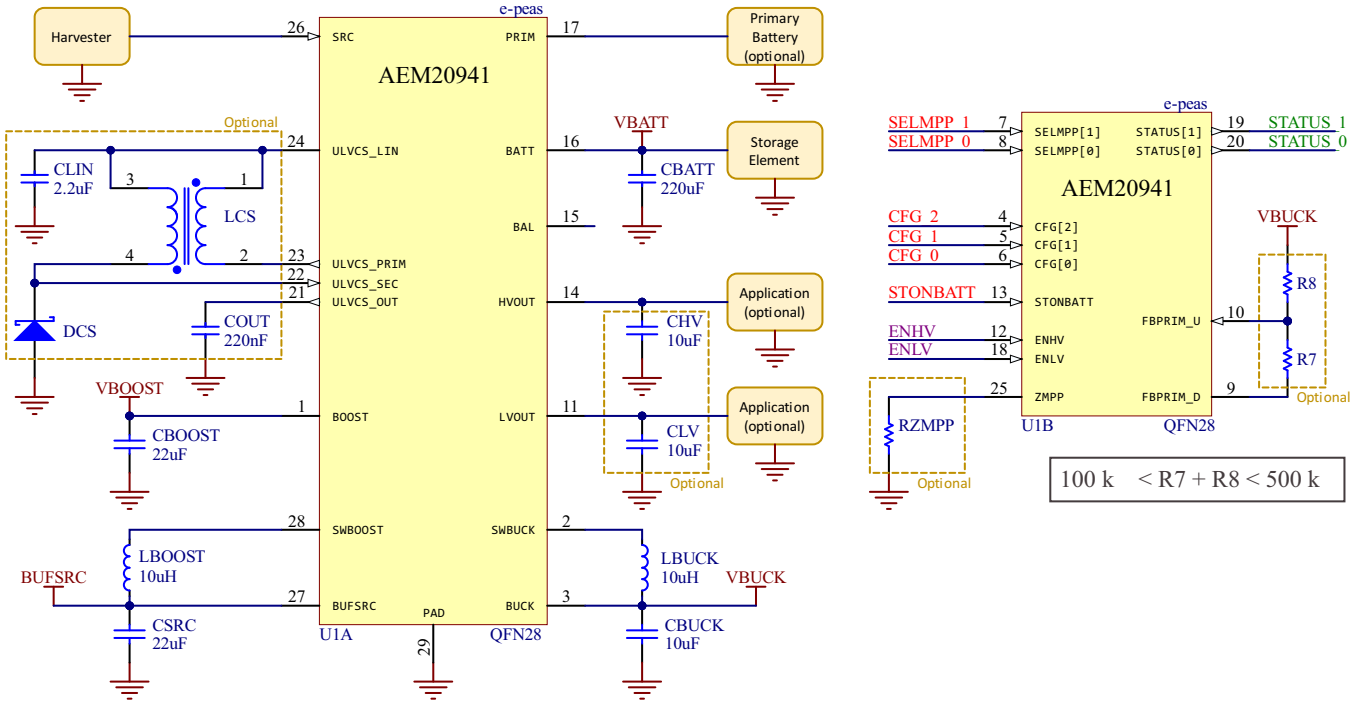


Figure 22: Schematic example

Designator	Description	Quantity	Manufacturer	Part Number
U1	AEM20941, QFN28	1	e-peas	order at sales@e-peas.com
C_{SRC}	Ceramic Cap 22 µF, 10 V, 20 %, X5R, 0603	1	Murata	GRM188R61A226ME15D
C_{BOOST}	Ceramic Cap 22 µF, 10 V, 20 %, X5R, 0603	1	Murata	GRM188R61A226ME15D
L_{BOOST}	Power Inductor 10 µH, 0.90 A, LPS4018	1	Coilcraft	LPS4018-103MRB
L_{BOOST} (alt.)	Power Inductor 10 µH, 0.84 A, 3015	1	Würth	744 040 321 00
L_{BOOST} (alt.)	Power Inductor 22 µH, 0.65 A, LPS4018	1	Coilcraft	LPS4018-223MRB
C_{BUCK}	Ceramic Cap 10 µF, 10 V, 20 %, X5R, 0603	1	TDK	C1608X5R1A106M080AC
L_{BUCK}	Power Inductor 10 µH, 0.25 A, 0603	1	TDK	MLZ1608N100LT000
C_{LV}	Ceramic Cap 10 µF, 10 V, 20 %, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{HV}	Ceramic Cap 10 µF, 10 V, 20 %, X5R, 0603	1	TDK	C1608X5R1A106M080AC
C_{BATT}	Ceramic Cap 220 µF, 6.3 V, 20 %, X5R, 1206	1	Murata	GRM31CR60J227ME11L
L_{CS}	Coupled inductor 25 µH, 1:20, LPR6532	1	Coilcraft	LPR6235-253PMRB
C_{LIN}	Ceramic Cap 2.2 µF, 35 V, 10 %, X5R, 0603	1	Murata	GRM188R6YA225KA12D
C_{OUT}	Ceramic Cap 220 nF, 10 V, 10 %, X5R, 0402	1	Yageo	CC0402KRX5R6BB224
D_{CS}	Schottky diode, 30 V, 200 mA, SOD-323	1	Infineon	BAT5403WE6327HTSA1

Table 11: BOM example for AEM20941 and its required passive components

10. Layout

10.1. Guidelines

Good layout practices are mandatory in order to obtain good AEM20941 stability, best efficiency and avoid EMI problems.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM20941:

- The switching nodes (BUFSRC, SWBOOST, SWBUCK and BUCK) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between these switching nodes and the AEM20941 pins. Minimal capacitance is obtained by maintaining a large distance between the switching nodes and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under L_{BOOST} and L_{BUCK} footprints, as well as adding distance between BUFSRC/SWBOOST and the top ground pour, as shown in Figure 23.
- The decoupling capacitors (C_{BOOST} - C_{BUCK} - C_{SRC} - C_{HV} - C_{LV} - C_{BATT}) must be placed as close as possible to the AEM20941, with direct connection and minimum track resistance for the corresponding power nodes (BOOST, BUCK, BUFSRC, HVOUT, LVOUT and BATT).
- The GND return path between the decoupling capacitors and the AEM20941 thermal pad, which is the AEM20941 main GND connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance. In Figure 23, this GND return path is done on an internal plane.
- The external DC power connections (SRC, HVOUT, LVOUT and BATT) must be connected to the AEM20941 with low resistance tracks.
- If used, ZMPP must be connected to the AEM20941 with a low resistance track, according to the expected SRC power.
- The BAL pin connection track must be able to handle at least 40 mA.
- The configuration pins and the status pins have minimal layout restrictions.

10.2. Layout Example

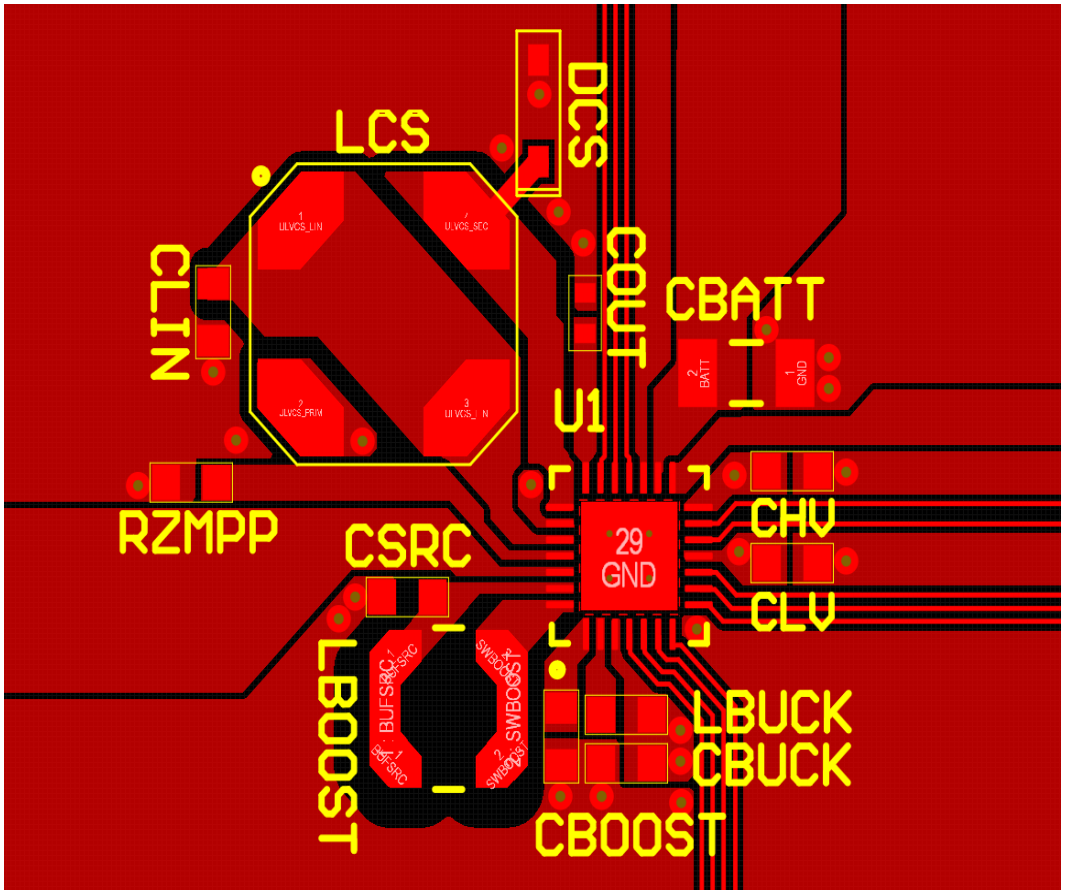


Figure 23: Layout example for the AEM20941 and its passive components

11. Package Information

11.1. Moisture Sensitivity Level

Package	Moisture Sensitivity Level (MSL)[1]
QFN 28-pin	Level 1

Table 12: Moisture sensitivity level

1. According to JEDEC 22-A113 standard.

11.2. RoHS Compliance

e-peas product complies with RoHS requirement.

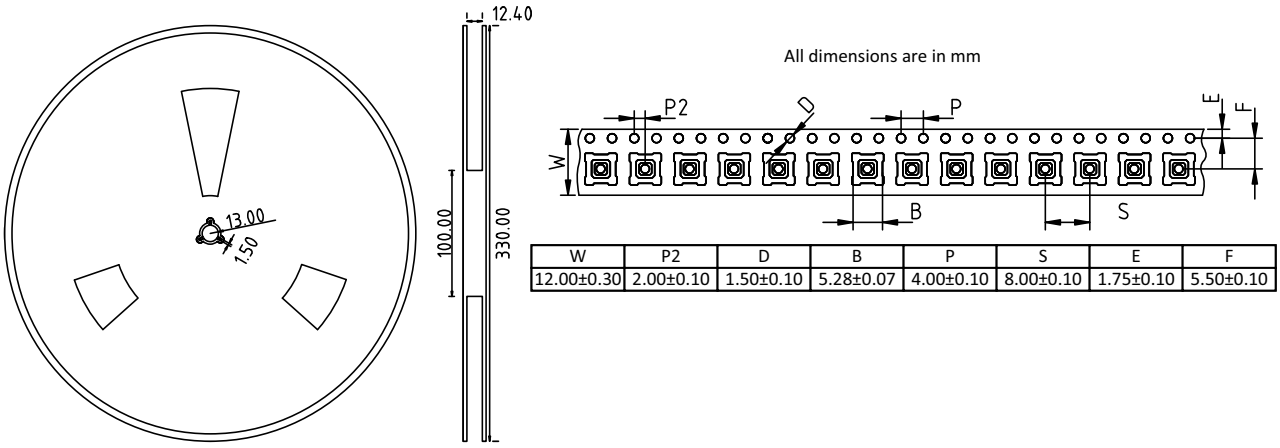
e-peas defines “RoHS” to mean that semiconductor end-products are compliant with RoHS regulation for all 10 RoHS substances.

This applies to silicon, die attached adhesive, gold wire bonding, lead frames, mold compound, and lead finish (pure tin).

11.3. REACH Compliance

The component and elements used by e-peas subcontractors to manufacture e-peas PMICs and devices are REACH compliant. For more detailed information, please contact e-peas sales team.

11.4. Tape and Reel Dimensions



W	P2	D	B	P	S	E	F
12.00±0.30	2.00±0.10	1.50±0.10	5.28±0.07	4.00±0.10	8.00±0.10	1.75±0.10	5.50±0.10

Figure 24: Tape and reel dimensions

11.5. Package Dimensions (QFN 28-pin 4 x 4 mm)

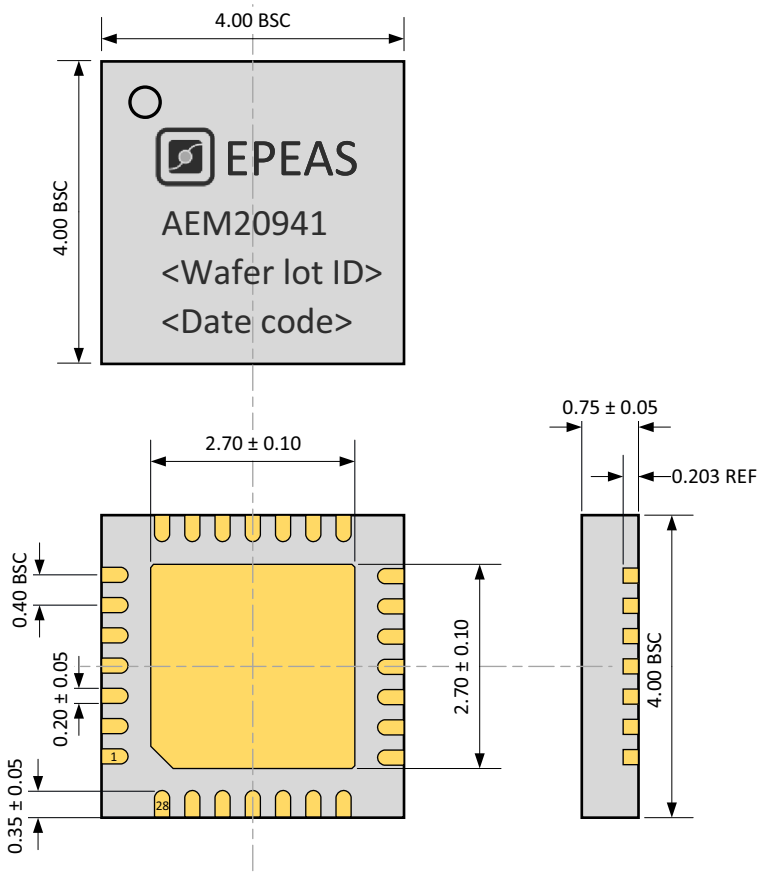


Figure 25: QFN 28-pin 4 x 4 mm drawing (all dimension in mm)

11.6. Board Layout (QFN 28-pin 4x4mm)

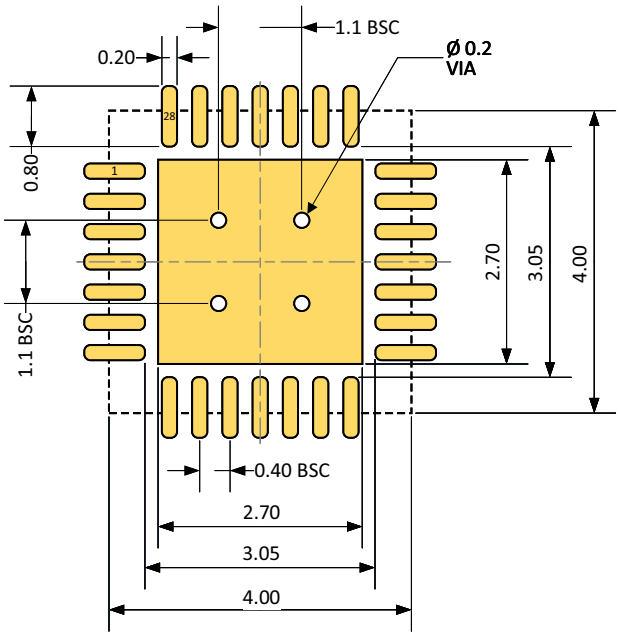


Figure 26: Recommended board layout for QFN 28-pin 4x4mm (all dimension in mm)

12. Glossary

AEM

Ambient Energy Manager.

BOM

Bill Of Materials.

C_{BATT}

Capacitor connected on the BATT pin (if no storage element connected).

C_{BOOST}

Output capacitor of the BOOST converter.

C_{BUCK}

Output capacitor of the BUCK converter.

C_{HV}

High-voltage LDO regulator decoupling capacitor.

C_{LV}

Low-voltage LDO regulator decoupling capacitor.

C_{SRC}

BUFSRC pin decoupling capacitor.

GPIO

General Purpose Input / Output.

I_{BUCK}

Total load current supplied by the BUCK converter (including the LVOUT current I_{LV}).

I_{HV}

Load current supplied by the high-voltage LDO regulator.

I_{LV}

Load current supplied by the low-voltage LDO regulator.

I_{PRIM}

Current from the primary battery.

I_{Q}

Quiescent current on BATT when no energy is available on SRC.

I_{SRC}

Harvested current from the energy source.

$I_{SRC,CS}$

Minimum current on SRC for the AEM20941 to coldstart.

L_{BOOST}

BOOST converter inductor.

L_{BUCK}

BUCK converter inductor.

LDO

Low Drop-Out linear regulator.

MPPT

Maximum Power Point Tracking.

PCB

Printed Circuit Board.

R_P

Sum of resistors for setting the primary battery minimum voltage. R_P = R7 + R8.

R_{ZMPP}

Resistor that defines the AEM20941 BOOST converter input resistance when used in ZMPP mode.

T_{CRIT}

Time during which the AEM stays in SHUTDOWN MODE before returning to NORMAL MODE or going to DEEP SLEEP MODE.

TEG

Thermoelectric Generator.

$T_{MPPT,MEASURE}$

Duration of V_{OC} measurement during MPP evaluations.

$T_{MPPT,PERIOD}$

Time between two MPP evaluations.

$T_{MPPT,WAIT}$

Time during which the AEM20941 stops pulling current on SRC before measuring the harvester open circuit voltage (V_{OC}).

V_{BAL}

Voltage on the BAL pin.

$V_{BAL,MIN}$

Minimum voltage on the BAL pin for the balancing circuit to operate.

V_{BATT}

Voltage on the BATT pin.

V_{BOOST}

Output voltage of the BOOST converter.

V_{BUCK}

Output voltage of the BUCK converter.

$V_{BUCK,RESET}$

Minimum voltage on BUCK before switching to DEEP SLEEP MODE (from any other mode).

V_{CHRDY}
Charge ready voltage on the BATT pin.

$V_{FB\_PRIM\_U}$
Feedback for the minimal voltage level on the primary battery.

V_{HV}
Output voltage of the high-voltage LDO regulator.

V_{LV}
Output voltage of the low-voltage LDO regulator.

V_{MPP}
Target regulation voltage on SRC when extracting power.

V_{OC}
Open-circuit voltage of the harvester connected to the SRC pin.

V_{OVCH}
Over-charge voltage on the BATT pin.

V_{OVDIS}
Over-discharge voltage on the BATT pin.

V_{PRIM}
Voltage on the primary battery.

$V_{PRIM,MIN}$
Voltage at which the primary battery is considered fully depleted.

V_{SRC}
Voltage on the SRC pin.

$V_{SRC,CS}$
Minimum voltage on SRC for the AEM20941 to coldstart.

ZMPPT
Maximum Power Point Tracking with constant impedance.

13. Revision History

Revision	Date	Description
1.0	December, 2025	Initial release.

Table 13: Revision history