iC-TW29 26-BIT ENCODER PROCESSOR WITH INTERPOLATION AND BiSS INTERFACE

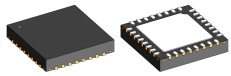
FEATURES

- Any output resolution with any input resolution
- Independently-programmed ABZ, UVW, and BiSS resolutions
- Absolute data interface for external revolution counters
- BiSS C-Mode interface (Encoder Profiles 3, 3S, and 4)
- 26-bit singleturn position and 32-bit revolution count via SPI
- Four capture registers for coded reference marks and touch-probe applications
- Eccentricity compensation
- Input frequency up to 700 kHz
- AB output frequency of up to 12.5 MHz
- Differential RS422 line driver outputs for ABZ or UVW
- Simultaneous single-ended outputs for ABZ, UVW, BiSS
- Automatic compensation of amplitude, offset, and phase errors
- Digital filtering for ultra-low output jitter
- Encoder Link interface for in-field re-configuration
- Internal EEPROM and oscillator
- LED intensity control by PWM output
- Low latency (2.4 µs or 5.0 µs)
- Pin-compatible with iC-TW28

APPLICATIONS

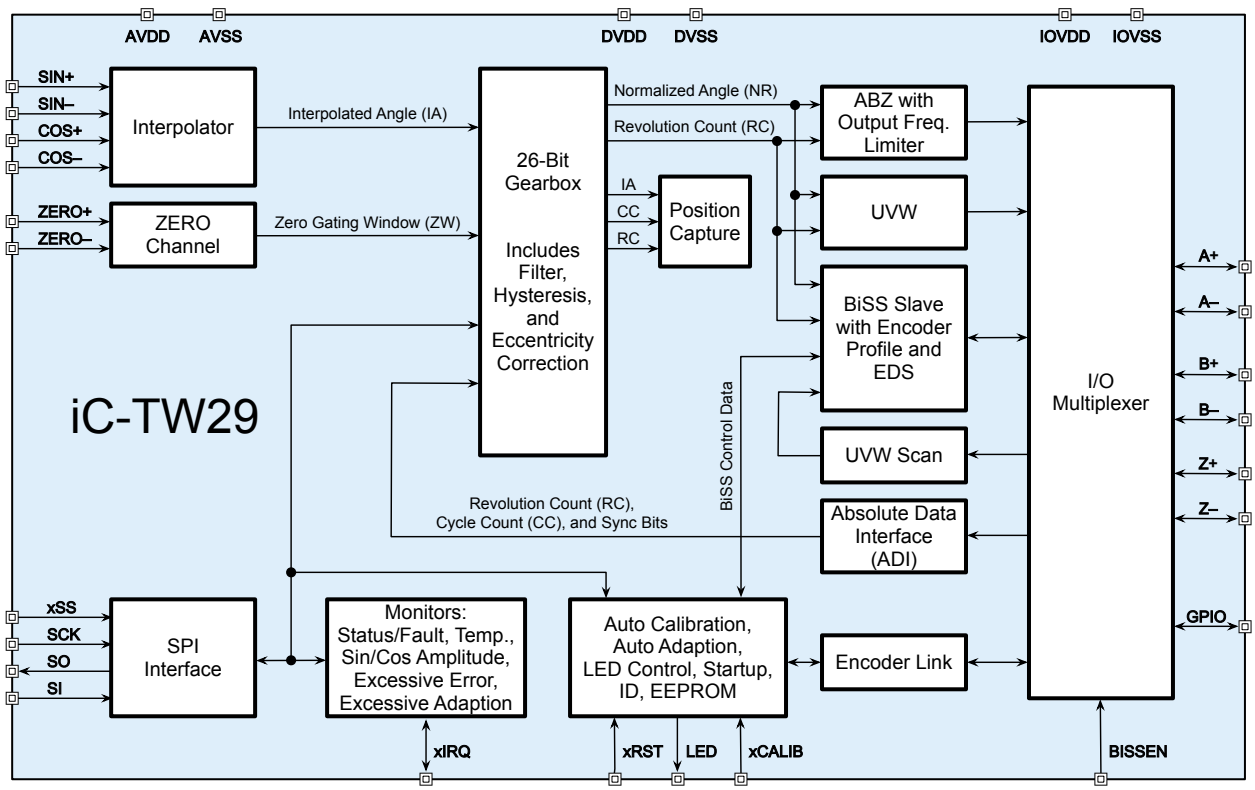
- Rotary and linear incremental or absolute encoders
- Magnetic or optical sin/cos sensor interface
- Brushless motor commutation (2...64 poles)
- Imbedded motion control

PACKAGES



32-pin QFN
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-TW29 is a system-on-chip for encoder applications. The integration of a 14-bit interpolator with a 26-bit gearbox and a resolution-enhancing digital filter provides a complete solution for arbitrary resolution single and multiturn encoders. Independent I/O modules with individually programmed resolutions provide BiSS C, standard encoder quadrature (ABZ), or commutation (UVW) outputs separately or in combination.

The iC-TW29 accepts 20 mV to 2 V differential sin/-cos input signals directly from magnetic or optical sensors—no external signal conditioning is required in most applications. The differential zero input accepts a wide range of digital and analog index gating sources such as Hall or MR sensor bridges. Automatic calibration and adaption (correction during operation) of sensor offset, sin/cos amplitude match, and phase quadrature provide and maintain minimum angular error and jitter. Additionally, automatic calibration of gain, offset, and phase of the zero input allows for rapid commissioning.

The gearbox tracks input cycles (up to 4096 per revolution) and provides output resolutions of up to 26 bits per revolution. Auto-calibrated eccentricity compensation increases achievable angular accuracy by correcting for off-center optical discs or magnetic pole-wheels. When combined with an external revolution counting device (such as the iC-PVL) communicating via its absolute data interface, the iC-TW29 provides a complete BiSS multiturn absolute encoder solution.

The differential zero input can be used with a traditional index sensor to generate an incremental Z output or to clear the gearbox counter in singleturn absolute applications. It can also be used as a position capture input with a four-word FIFO to allow decoding distance-coded reference marks in hosted applications.

In addition to industry-standard incremental ABZ quadrature output, the iC-TW29 also provides UVW commutation output modes for 1 to 32 pole-pair motors as well as BiSS and SPI interfaces. The BiSS interface provides BiSS encoder profiles 3, 3S (safety), or 4 as well as optional electronic data sheet EDS SE functionality. BiSS passthrough mode allows a host processor to implement any BiSS encoder profile or EDS.

Extensive status/fault and signal quality monitoring capabilities allow detection and notification of poor operating conditions.

The iC-TW29 is configured via SPI and via the bi-directional BiSS or Encoder Link interfaces if configured accordingly. Encoder link uses the incremental quadrature outputs to implement a SPI-like serial interface for field re-configuration or diagnostics.

The iC-TW29 requires minimal external components for operation. An EEPROM for storage of configuration and calibration data, and RS422 line drivers for the ABZ or UVW outputs are already integrated on-chip. An external line driver/receiver is required for BiSS applications. An integrated power-on reset circuit can be overridden by an external hardware reset signal if necessary.

General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.

For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

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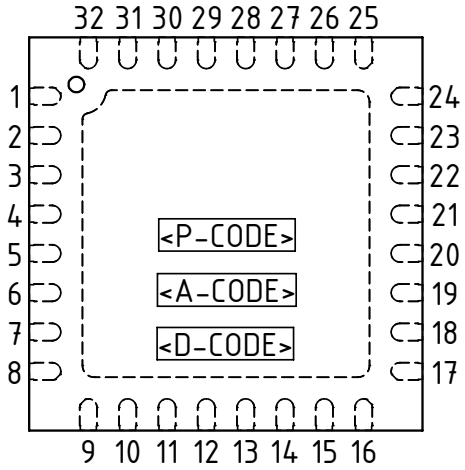
PACKAGING INFORMATION (Compatible with iC-TW28)

PIN CONFIGURATION QFN32-5x5



PIN FUNCTIONS

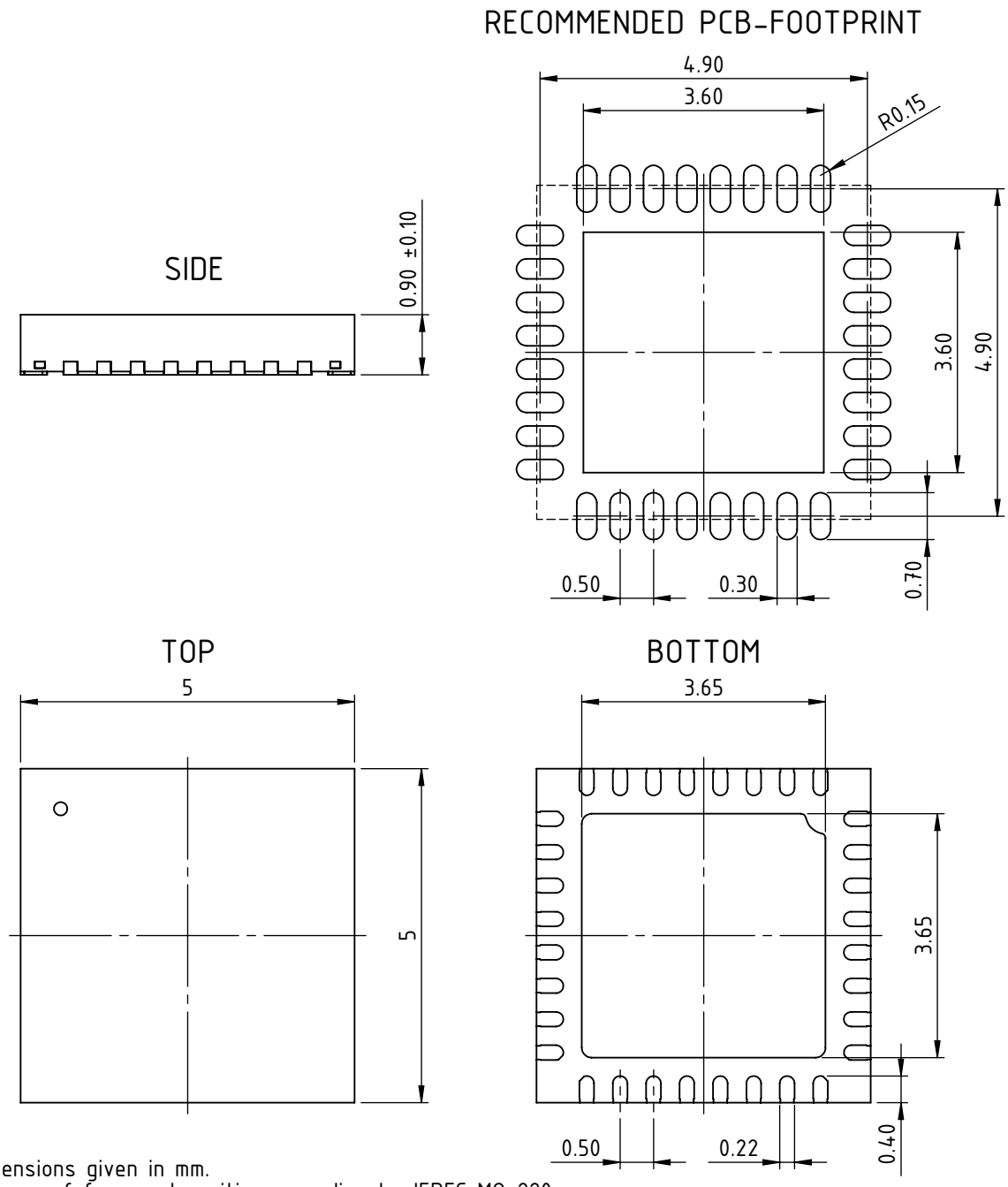
No.	Name	Function
1	SIN+[3]	+ Differential Sine Input
2	SIN–[3]	– Differential Sine Input
3	AVDD	+3.3 V Analog Power Supply Input
4	COS+[3]	+ Differential Cosine Input
5	COS–[3]	– Differential Cosine Input
6	AVSS	Analog Ground
7	ZERO+[5]	+ Differential Zero (Index) Input
8	ZERO–[5]	– Differential Zero (Index) Input
9	VREF[7]	ADC Reference Voltage Output
10	VC[7]	Bias Output (VDD/2)

PIN FUNCTIONS

No.	Name	Function
11	Reserved[1]	
12	Reserved[1]	
13	GPIO[3]	General Purpose I/O
14	xRST[4]	Reset Input (low active)
15	xCALIB[4]	Auto-Calibration Input (low active)
16	xIRQ[4]	Interrupt Request (active-low) Input/Output or Fault Output
17	Z–	– Differential RS422 Z Output or Multifunction I/O
18	Z+	+ Differential RS422 Z Output or Multifunction I/O
19	IOVSS	I/O Ground
20	B–	– Differential RS422 B Output or Multifunction I/O
21	B+	+ Differential RS422 B Output or Multifunction Output
22	IOVDD	+3.3 V I/O Power Supply Input
23	A–	– Differential RS422 A Output or Multifunction I/O
24	A+	+ Differential RS422 A Output or Multifunction I/O
25	DVDD	+3.3 V Digital Power Supply Input
26	LED[4]	LED Intensity Control Output or General-Purpose I/O
27	DVSS	Digital Ground
28	SO	SPI Slave Output (Master Input)
29	SI[3]	SPI Slave Input (Master Output)
30	SCLK[3]	SPI Clock Input
31	xSS[4]	SPI Slave Select Input
32	BISSEN[6]	BiSS Interface Enable
	TP[2]	Backside paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] Must be connected to ground.
[2] Must be connected to a ground plane at AVSS potential. Can also be used to connect DVSS.
[3] Do not allow to float. Connect to ground via 10 kΩ resistor if not used.
[4] Do not allow to float. Connect to 3.3 V via 10 kΩ resistor if not used.
[5] Do not allow to float. Connect ZERO+ to 3.3 V and ZERO- to ground via 10 kΩ resistor if not in use. Alternatively, program MAIN_CFG.zero = 1 for internal biasing of unconnected pins.
[6] Connect to 3.3 V (to DVDD to enable BiSS interface) or ground (to DVSS to disable BiSS interface). Do not allow to float.
[7] Decouple with 100 nF capacitor to AVSS. Do not inject noise.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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PIN FUNCTIONS

No.	Name	I/O	Function	Description
1	SIN+	Analog in	Sine Input +	Differential sine signal input. For single ended sensors SIN– must be biased to an appropriate DC level.
2	SIN–	Analog in	Sine Input –	
3	AVDD	Supply	Analog Power Supply	+3.1 V to +3.6 V supply voltage input for analog circuitry. AVDD should be tied together with DVDD and IOVDD and supplied from a clean source.
4	COS+	Analog in	Cosine Input +	Differential cosine signal input. For single ended sensors COS– must be biased to an appropriate DC level.
5	COS–	Analog in	Cosine Input –	
6	AVSS	Ground	Analog Ground	AVSS must be tied to high quality ground, usually a solid PCB plane.
7	ZERO+	Analog in	Zero Input +	Differential Zero Gating Input. If single ended signal sources are used, the unused terminal (either ZERO+ or ZERO–) must be tied to an appropriate DC bias.
8	ZERO–	Analog in	Zero Input –	
9	VREF	Analog out	Bias Output	Decouple with 100 nF capacitor to AVSS. Do not inject noise into this pin as it directly impacts ADC conversion quality.
10	VC	Analog out	Bias Output	Decouple with 100 nF capacitor to AVSS. Do not inject noise into this pin as it directly impacts ADC conversion quality.
11	Reserved	Digital in	Test Input	Reserved pins; must be connected to DVSS for normal operation.
12	Reserved	Digital in	Test Input	
13	GPIO	Digital in/out	General-Purpose I/O	Connect to AVSS if not used.
14	xRST	Digital in, active low	Reset Input	The device is held in reset (low power mode) as long as xRST is low.
15	xCALIB	Digital in, active low	Calibration Control	Device enters calibration mode on falling edge of CALIB. This pin must be tied high if not used.
16	xIRQ	Digital out, active low or input	IRQ or Fault Output or IRQ input	Interrupt request output to external micro controller or interrupt request input. Output can also be used to directly drive a fault LED in stand-alone applications. Can be configured as push-pull or open-drain.
17	Z–	Digital/RS422 out	Z– or W– Output	In ABZ output modes these are the differential Z outputs. In UVW output modes these are the W outputs. In **BiSS mode** (BISSEN pin high), pin Z+ is the data input SLI. If daisy chaining is not required, Z+ can be grounded (IOVSS). In other modes, these are multifunction I/O.
18	Z+	Digital/RS422 out	Z+ or W+ Output	
19	IOVSS	Ground	I/O Ground	All ground pins must be connected to a high quality ground, usually a solid PCB plane.
20	B–	Digital/RS422 out	B– or V– Output	In ABZ output modes these are the differential B outputs. In UVW output modes these are the V outputs. In **BiSS mode** (BISSEN pin high), pin B+ is the data output SLO. In other modes, these are multifunction I/O. In **Z test mode** these show the Z gating window.
21	B+	Digital/RS422 out	B+ or V+ Output	
22	IOVDD	Supply	Output Drivers Power Supply	+3.1 V to +3.6 V voltage terminal supplying all pin output drivers including the RS422 drivers and LED current. IOVDD and DVDD must be the same voltage level. IOVDD can require up to 100mA depending on loads. It is usually sufficient to tie IOVDD to the same supply as AVDD and DVDD.
23	A–	Digital/RS422 out	A– or U– Output	In ABZ output modes these are the differential A outputs. In UVW output modes these are the U outputs. In **BiSS mode** (BISSEN pin high), pin A+ is the clock input MA. In other modes, these are multifunction I/O. In **Z test mode** these show the un-gated Z signal once per input period. With **Encoder Link** active, A+ is the ELCLK input and A– is ELIN input or ELOUT output.
24	A+	Digital/RS422 out	A+ or U+ Output	
25	DVDD	Supply	Digital Power Supply	+3.1 V to +3.6 V supply voltage terminal for digital circuits. DVDD should be tied together with AVDD and IOVDD to a high quality supply.
26	LED	Digital input or output	LED PWM Output	Used to supply the illumination LED of optical sensors to maintain constant intensity and constant Sin/Cos sensor amplitude. Can be configured as push-pull or open-drain. If not required for LED control, it is a general purpose I/O.
27	DVSS	Ground	Digital Ground	Pin must tied to high quality ground, usually a solid PCB plane.
28	SO	Digital out	SPI Slave Output	Connect to SPI master MI pin.

PIN FUNCTIONS

No.	Name	I/O	Function	Description
29	SI	Digital in	SPI Slave Input	Connect to SPI master MO pin.
30	SCLK	Digital in	SPI Slave Clock Input	Connect to SPI master clock output pin.
31	xSS	Digital in	SPI Slave Select Input	Connects to SPI master slave select output pin.
32	BISSEN	Digital in	BiSS Interface Enable	Connect to DVDD to enable the BiSS/SSI interface. The I/O pins A+, B+, Z+ are used for MA, SLO, SLI.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these values damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at DVDD, AVDD, and IOVDD	Referenced to DVSS, AVSS, and IOVSS respectively	–0.3	4.1	V
G002	Vpin	Pin Voltage at any pin	Referenced to DVSS, AVSS, and IOVSS	–0.3	AVDD + 0.3	V
G003	Ipin	Input Current into any pin		–2	2	mA
G004	Vesd1	ESD Susceptibility	HBM, 100 pF discharged through 1.5 kΩ CDM (JEDEC Standard No. 22-C101F)		4000 500	V V
G005	Tj	Junction Temperature		–40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		–40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN32-5x5 surface mounted to PCB according to JEDEC 51		40		K/W
T03	Ts	Storage Temperature		–40		150	°C

All voltages are referenced to pin AVSS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: AVDD = DVDD = IOVDD = 3.1...3.6 V, Tj = –40...+125 °C, reference point AVSS unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage AVDD, DVDD, IOVDD		3.1		3.6	V
002	I_{AVDD}	Supply Current into AVDD	AVDD, DVDD, IOVDD = 3.3 V, fin = 1 kHz, inter = x256, ABZ and UVW outputs active			16	mA
003	I_{DVDD}	Supply Current into DVDD	AVDD, DVDD, IOVDD = 3.3 V, fin = 1 kHz, inter = x256, ABZ and UVW outputs active			30	mA
004	I_{IOVDD}	Supply Current into IOVDD	RS422 drivers enabled (MAIN_CFG.rs422 = 1); quadrature outputs terminated with 120 Ω quadrature outputs open			85 2	mA mA
005	I_{RST}	Reset Current (I_{AVDD} + I_{DVDD} + I_{IOVDD})	xRST low		1		mA
Signal Inputs and Amplifiers: SIN+, SIN–, COS+, COS–							
101	Vin()	Permissible Input Voltage	Refer to Figure 1 Low Input Range (MAIN_CFG.input = 0 or 1) High Input Range (MAIN_CFG.input = 3) For High Input Range and MAIN_CFG.input = 2 refer to Figure 1.	 0.35 1.0		 AVDD – 1.1 AVDD	 V V
102	Ain()diff	Permissible Differential Input Amplitude, Max(SIN+ – SIN–) or Max(COS+ – COS–)	Refer to Figure 2 Low Input Range (MAIN_CFG.input = 0 or 1) High Input Range (MAIN_CFG.input = 2 or 3)	 20 65		 700 2000	 mVpp mVpp
103	Vcm()	Permissible Input Common Mode Range, (SIN+ + SIN–)/2 or (COS+ + COS–)/2	Refer to Figure 3 Minimum gain (MAIN_CFG.input ≠ 3) Maximum gain (MAIN_CFG.input ≠ 3) Minimum gain (MAIN_CFG.input = 3) Maximum gain (MAIN_CFG.input = 3)	 0.7 0.35 2.0 1.0		 AVDD – 1.45 AVDD – 1.1 AVDD AVDD	 V V V V
104	fin()	Sin/Cos Input Frequency				700	kHz
105	Vos()	Amplifier Input Offset Voltage				±20	mV
106	Ilk()	Input Leakage Current				±50	nA
108	OFFcorr	Correctable Input Offset Voltage	As percentage of input signal amplitude; input offset voltage is the sum of sensor offset plus amplifier offset (item 105); (step size: 3.9 mV / gain)	±25			%
109	Acorr	Correctable Balance (Amplitude) Mismatch	Max(Asin, Acos) / Min(Asin, Acos), where Asin and Acos are the SIN/COS input amplitudes respectively. (step size 0.02%)	±25			%
110	PHIcorr	Correctable Phase Error	(step size 0.014°)		±26		°
111	Rin()diff	Differential Input Resistance	Low range (MAIN_CFG.input = 0) Low r. with loss detect. (MAIN_CFG.input = 1) High range (MAIN_CFG.input = 2) High r. and 2.5 Vcm (MAIN_CFG.input = 3)	10	1000 0.220 0.640 0.310		MΩ MΩ MΩ MΩ
Zero Signal Inputs and Amplifier: ZERO+, ZERO–							
201	Vin()	Permissible Input Voltage		0		AVDD	V
202	Vcm()	Permissible Input Common Mode Voltage	Refer to Figure 3 Minimum gain (MAIN_CFG.zero = 0) Maximum gain (MAIN_CFG.zero = 0) Minimum gain (MAIN_CFG.zero = 1) Maximum gain (MAIN_CFG.zero = 1)	 0.7 0.35 2.0 1.0		 AVDD – 1.45 AVDD – 1.1 AVDD AVDD	 V V V V
203	Vos()	Input Referenced Offset Voltage				±20	mV
204	Ilk()	Input Leakage Current				±50	nA

ELECTRICAL CHARACTERISTICS

Operating conditions: AVDD = DVDD = IOVDD = 3.1...3.6 V, Tj = –40...+125 °C, reference point AVSS unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
205	OFFcorr	Correctable Input Offset Voltage	As percentage of input signal amplitude; input offset voltage is the sum of sensor offset plus amplifier offset (item 105); (step size 60 mV / gain)	±100			%
206	Rin()diff	Differential Input Resistance	Low range (MAIN_CFG.zero = 0) High r. and 2.5 Vcm (MAIN_CFG.zero = 1)	10	1000 0.310		MΩ MΩ
Converter Performance							
304	INL	Integral Nonlinearity (over one input SIN/COS cycle)	Refer to Figure 5, 1 Vpp-diff SIN/COS input with compensated offset, gain and phase			0.1	°
305	DNL	Differential Nonlinearity (over one input SIN/COS cycle)	Refer to Figure 5, 1 Vpp-diff SIN/COS input with compensated offset, gain and phase			0.01	°
307	t_{AB}	Output Phase A vs. B	Refer to Figure 4		25		%
308	t_{whi}	Duty Cycle at Output A, B	Refer to Figure 4		50		%
310	t_{MTD}	Time Between AB Edges (Minimum Transition Distance)	Refer to Figure 4, ABLIMIT = 0	1/fosc	20		ns
Internal Oscillator							
401	fosc	Oscillator Frequency	Tj = 27 °C; AVDD, DVDD = 3.1 V AVDD, DVDD = 3.6 V	48 48		51 52	MHz MHz
402	TCf	Temperature Coefficient			150		ppm/K
Internal EEPROM							
501	Nwrite	Permissible Number of Write Cycles	Tj = –40 °C...85 °C	1000			
502	Tjw	Write Temperature Range		–40		85	°C
503	Tjr	Read Temperature Range		–40		125	°C
504	DRTraw	Raw Data Retention Time *	Tj = –40 °C...85 °C Tj = –40 °C...125 °C	20 10			years years
Reset and Start-Up: xRST							
601	DVDDonoff	DVDD Power-On/Off Threshold	xRST tied to DVDD	2.5	2.7	3.0	V
603	tstart	Startup Time	Valid EEPROM configuration, until AB output function; START.wait = 0 (0 ms) START.wait = 3 (10 ms)		 7 17		 ms ms
604	td()lo	Recommended Reset Activation Time	input xRST is digitally debounced	100			ns
Digital Input Pins: xRST, xCALIB, A+/– (Encoder Link active), A– and B– (BiSS mode), SI, SCLK, xSS,GPIO, BISSEN							
701	Vt()hi	Input Logic Threshold High	DVDD = 3.6 V			1.9	V
702	Vt()lo	Input Logic Threshold Low	DVDD = 3.3 V	0.8			V
703	Ilk()	Input Leakage Current at SI, SCLK, xSS				±50	nA
704	f(SCLK)	Permissible SPI Clock Frequency at SCLK	TEST.spi = 0 TEST.spi = 1			20 40	MHz MHz
705	fin(MA)	Permissible Clock Frequency at MA (A+)	BiSSEN = high; BISS_CFG0.ssi = 0 (BiSS) BISS_CFG0.ssi = 1 (SSI)			10 4	MHz MHz
706	t_{RQ}	Request Time at MA (A+)	BiSSEN = high; for SSI data output to SLO, see Figure 9		24 / fosc		
Digital Output Pins: xIRQ, SO, A+/A–, B+/B–, Z+/Z– (CMOS drivers enabled: MAIN_CFG.rs422 = 0), Z– (BiSS mode)							
801	I()max	Permissible Output Current	Per pin, indefinite			±10	mA
802	Vout()hi	Output Voltage High	I() = –4 mA, MAIN_CFG.irqpp = 1 (for xIRQ push-pull)	2.4			V
803	Vs()hi	Saturation Voltage High	Vs()hi = IOVDD - V(); I() = -4 mA, MAIN_CFG.irqpp = 1 (for xIRQ push-pull)			0.7	V
804	Vs()lo	Saturation Voltage Low	I() = 4 mA			0.7	V
805	Isc()hi	Short-Circuit Current High	Any pin shorted to DVSS	–30	–16		mA
806	Isc()lo	Short-Circuit Current Low	Any pin shorted to DVDD		16	30	mA

* The implemented error correction can extend the data retention significantly.

ELECTRICAL CHARACTERISTICS

Operating conditions: AVDD = DVDD = IOVDD = 3.1...3.6 V, Tj = –40...+125 °C, reference point AVSS unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
807	tr()	Rise Time	DVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
808	tf()	Fall Time	DVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
809	t_{TO}(), t_{TOA}()	Slave Timeout at SLO (B+)	BiSSEN = high for BiSS & SSI; BiSS_CFG0.at = 0 (fixed), see Fig. 9, 10; BiSS_CFG0.at = 1 (adaptive), see Figure 11	8 / fosc	1024 / fosc t_{init} + 4 / fosc	1024 / fosc	
RS422 Drivers: A+/A–, B+/B–, Z+/Z– (RS422 drivers enabled: MAIN_CFG.rs422 = 1)							
901	Idrv()	Nominal RS422 Driver Current	RL() = 120 Ω between + and – terminals	20		27	mA
902	Isc()hi	Short Circuit Current High	+ or – pin shorted to IOVSS	–55			mA
903	Isc()lo	Short-Circuit Current Low	+ or – pin shorted to IOVDD			35	mA
LED Output (enabled: LED_CFG.en = 1)							
A01	I()max	Permissible Output Current	for continuous operation			±15	mA
A02	Vout()hi	Output Voltage High	VDD = 3.3 V, Tj = 27 °C, I() = –10 mA		2.7		V
A03	Vs()hi	Saturation Voltage High	Vs()hi = DVDD – V(LED); I() = –10 mA			1	V
A04	Vs()lo	Saturation Voltage Low	I() = 10 mA			1	V
A05	Isc()hi	Short-Circuit Current High	LED pin shorted to DVSS	–40			mA
A06	Isc()lo	Short-Circuit Current Low	LED pin shorted to DVDD			42	mA
Bias Outputs: VC, VREF							
B01	VC	Bias Voltage VC	I(VC) = 0		50		%AVDD
B02	dVREF	ADC Reference Voltage VREF versus VC	dVREF = V(VREF) - V(VC); I(VREF) = 0	–1.1	–1	–0.9	V
Temperature Sensor							
C01	Tacc	Temperature Sensor Accuracy	Tj = 100 °C		±2	±5	°C °C

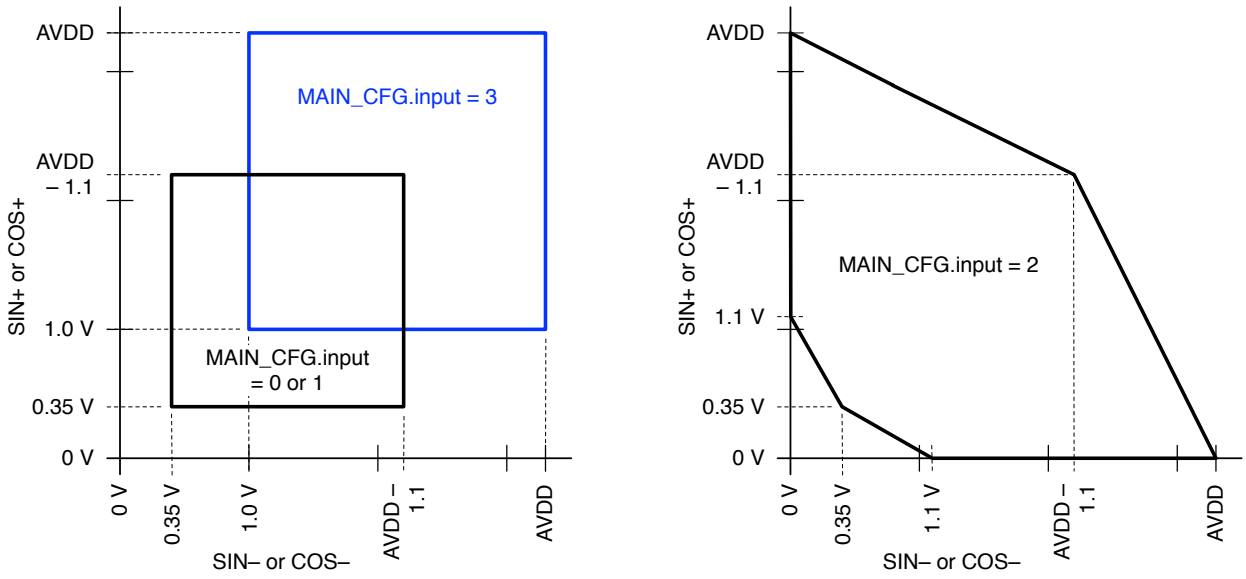

Figure 1: Input Voltage Range (Vin())

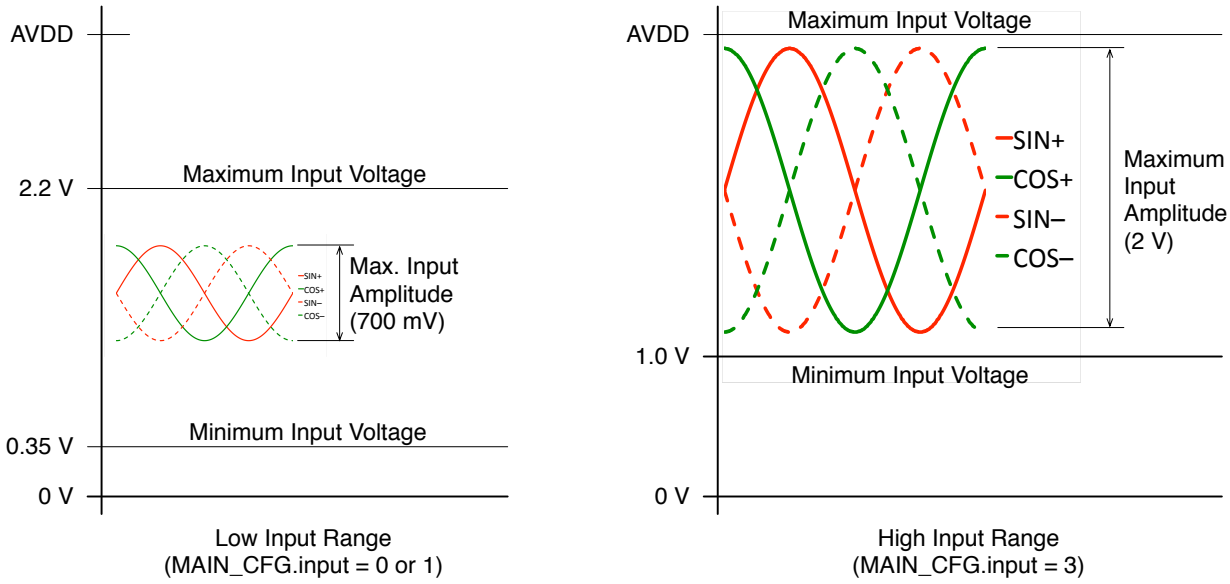

Figure 2: Differential Input Amplitude (Ain()diff), Max(SIN+ – SIN–) or Max(COS+ – COS–)

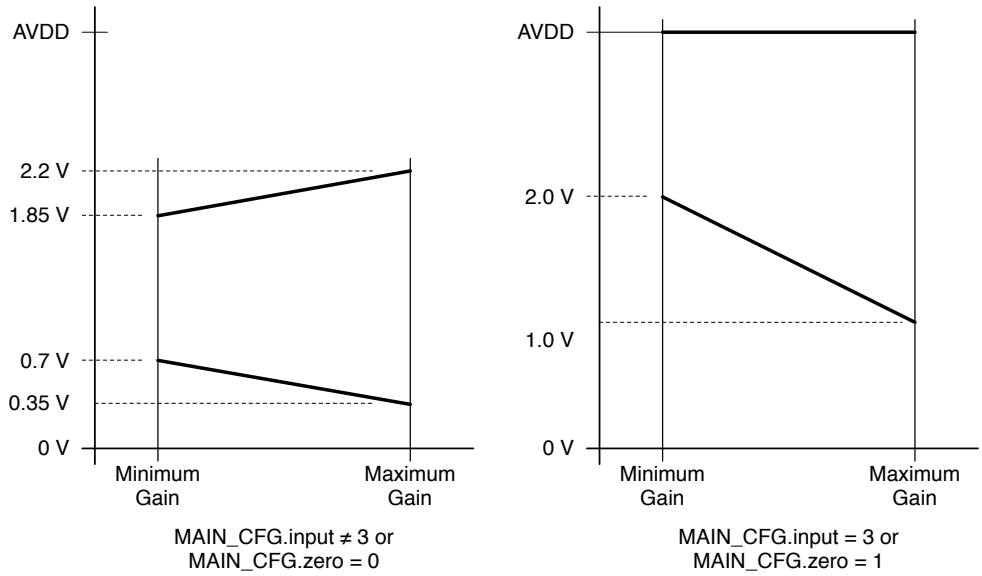

Figure 3: Input Common Mode Range, (SIN+ + SIN–)/2, (COS+ + COS–)/2, or (ZERO+ + ZERO–)/2

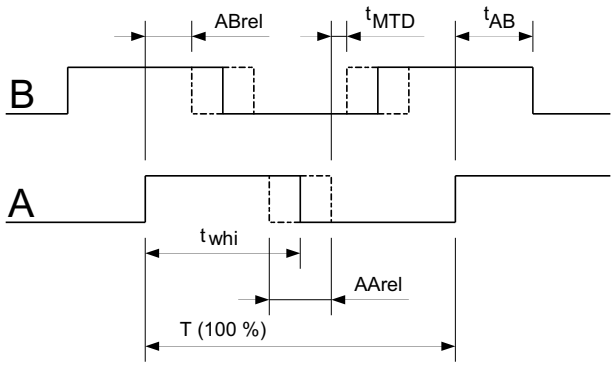

Figure 4: Description of AB output signals

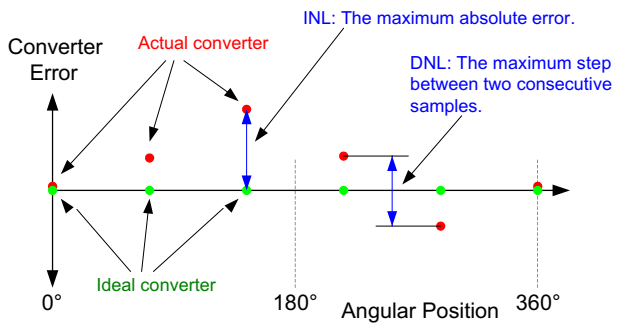

Figure 5: Definition of integral and differential nonlinearity

OPERATING REQUIREMENTS: SPI Interface

Operating conditions: AVDD = DVDD = IOVDD = +3.1...+3.6 V, AVSS = DVSS = IOVSS = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Interface Timing						
I001	t_{C1}	Permissible Clock Cycle Time	TEST.spi = 0 (see Elec. Char. 704) TEST.spi = 1	50 25		ns ns
I002	t_{D1}	Clock Signal Lo Level Duration	TEST.spi = 0 TEST.spi = 1	15 7.5		ns ns
I003	t_{D2}	Clock Signal Hi Level Duration	TEST.spi = 0 TEST.spi = 1	15 7.5		ns ns
I004	t_{S1}	Setup Time: xSS lo before SCLK lo → hi		80		ns
I005	t_{H1}	Hold Time: xSS lo after SCLK hi → lo		50		ns
I006	t_{W1}	Wait Time: between xSS lo → hi and xSS hi → lo		200		ns
I007	t_{S2}	Setup Time: SI stable before SCLK lo → hi		5		ns
I008	t_{H2}	Hold Time: SI stable after SCLK lo → hi		10		ns
I009	t_{P1}	Propagation Delay: SO stable after xSS hi → lo			60	ns
I010	t_{P2}	Propagation Delay: SO high impedance after xSS lo → hi			25	ns
I011	t_{P3}	Propagation Delay: SO stable after SCLK hi → lo			20	ns

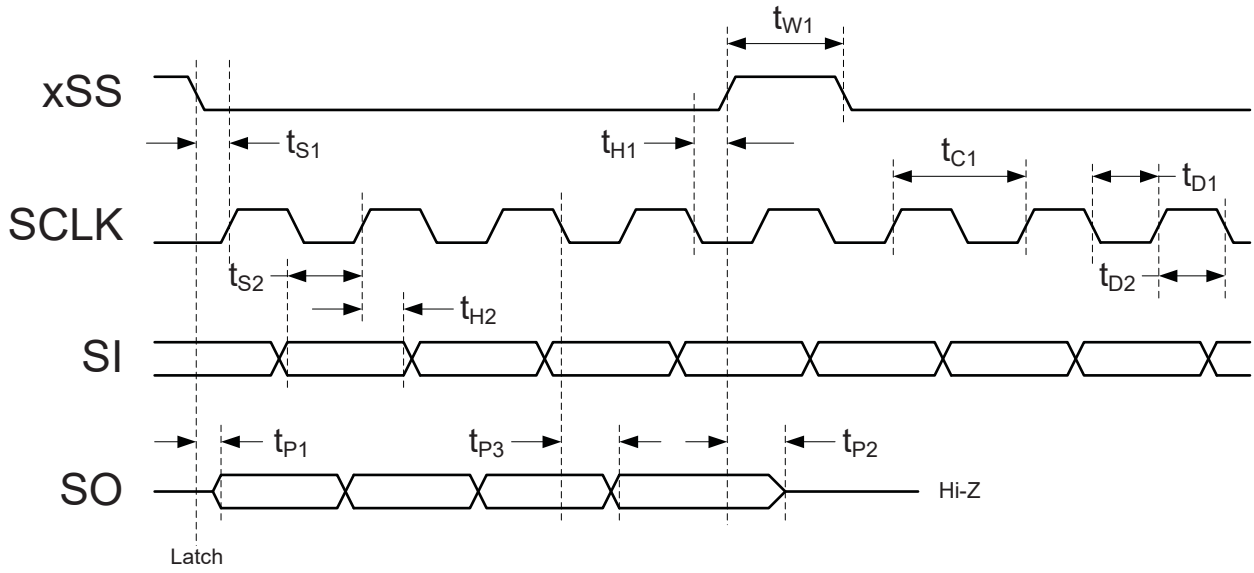

Figure 6: SPI Timing

OPERATING REQUIREMENTS: Encoder Link Interface

Operating conditions: AVDD = DVDD = IOVDD = +3.1...+3.6 V, AVSS = DVSS = IOVSS = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Encoder Link Activation Sequence Timing (RS422 drivers enabled: MAIN_CFG.rs422 = 1)						
I101	T1	Activation Sequence Interval 1	A+ > 2.4 V, A– > 2.4 V	0.25	2	ms
I102	T2	Activation Sequence Interval 2	A+ < 0.8 V, A– > 2.4 V	T1 – 10%	T1 + 10%	ms
I103	T3	Activation Sequence Interval 3	A+ < 0.8 V, A– < 0.8 V	T1 – 10%	T1 + 10%	ms
I104	T4	Activation Sequence Interval 4	A+ > 2.4 V, A– < 0.8 V	T1 – 10%	T1 + 10%	ms
Encoder Link Interface Timing (after activation) (RS422 drivers enabled: MAIN_CFG.rs422 = 1)						
I105	fclk(A+)	ELink Clock Frequency	Signal driven into A+		1.0	MHz
I106	t_{D1}(A+)	ELink Clock Signal Hi Level Duration	Signal driven into A+	200		ns
I107	t_{D2}(A+)	ELink Clock Signal Lo Level Duration	Signal driven into A+	200		ns
I108	t_S(A–)	ELink Input Setup Time	Signal driven into A–	200		ns
I109	t_H(A–)	ELink Input Hold Time	Signal driven into A–	200		ns
I110	t_P(A–)	ELink Output Propagation Delay	Signal driven out on A–		200	ns

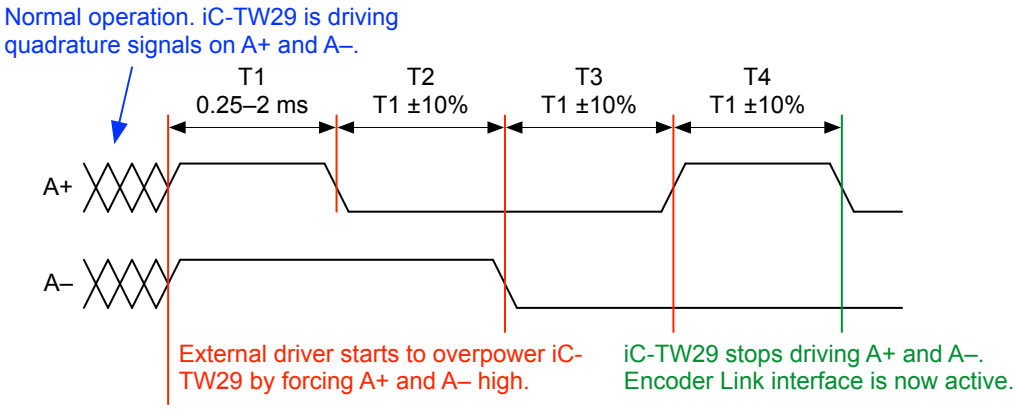

Figure 7: Encoder Link Activation Sequence

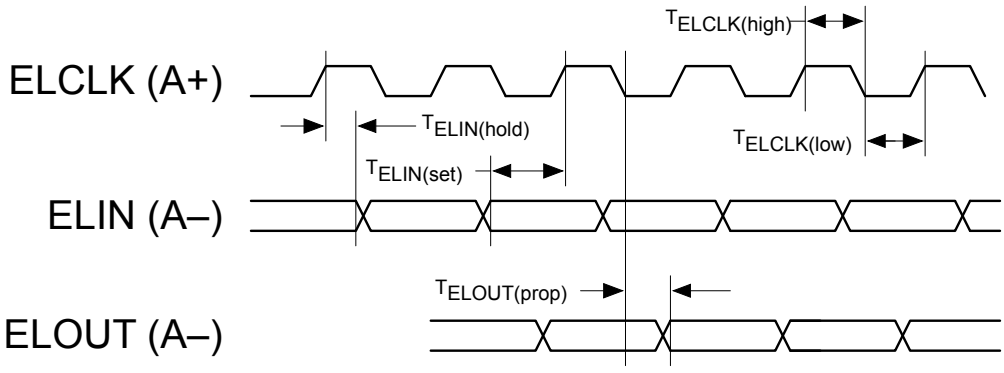

Figure 8: Encoder Link Read and Write Timing

OPERATING REQUIREMENTS: BiSS Interface

Operating conditions: AVDD = DVDD = IOVDD = +3.1...+3.6 V, AVSS = DVSS = IOVSS = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI protocol (BiSSEN pin high and BISS_CFG0.ssi = 1)						
I201	t_C	Permissible Clock Period	see Elec. Char. 705; with t_{RQ} according to I204	250		ns
I202	t_{L1}	Clock Signal Hi-Level Duration		125	t_{TO}	ns
I203	t_{L2}	Clock Signal Lo-Level Duration		125	t_{TO}	ns
I204	t_{RQ}	Request Time	Clock low-level duration at MA input (due to Elec. Char. 706)	500		ns
I205	t_{P3}	Output Propagation Delay			50	ns
I206	t_{TO}	Slave Timeout		see Elec. Char. 809		
I207	t_{Cycle}	Permissible Clock Cycle Time		*	indefinite	
BiSS C protocol (BiSSEN pin high and BISS_CFG0.ssi = 0)						
I208	t_C	Permissible Clock Period	see Elec. Char. 705	100		ns
I209	t_{L1}	Clock Signal Hi-Level Duration		40	t_{TO}	ns
I210	t_{L2}	Clock Signal Lo-Level Duration		40	t_{TO}	ns
I211	t_{busy}	Minimum Data Output Delay		2 t_C		
I212	t_{busy}	Maximum Data Output Delay			400	ns
I213	t_{P3}	Output Propagation Delay			50	ns
I214	t_{TO}	Slave Timeout		see Elec. Char. 809		
I215	t_{S1}	Setup Time: SLI stable before MA hi → lo		25		ns
I216	t_{H1}	Hold Time: SLI stable after MA hi → lo		10		ns
I217	t_{Cycle}	Permissible Clock Cycle Time		*	indefinite	

Note: * Allow t_{TO} to elapse.

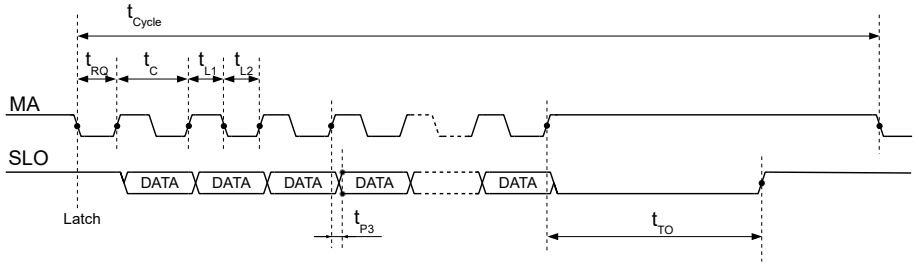

Figure 9: SSI protocol timing

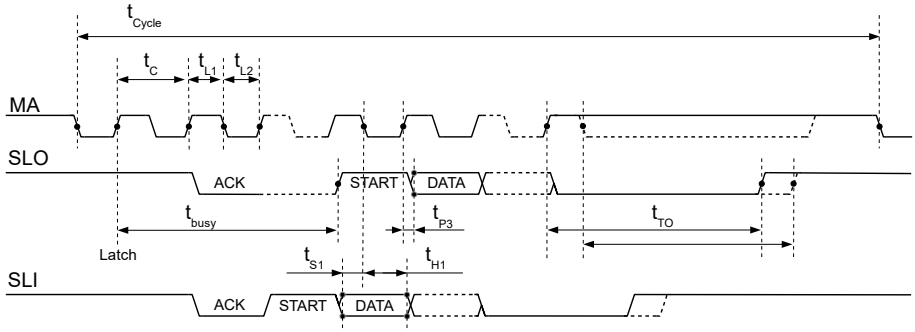

Figure 10: BiSS protocol timing

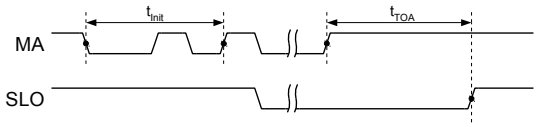

Figure 11: BiSS slave timeout

OPERATING REQUIREMENTS: ADI Interface

Operating conditions: AVDD = DVDD = IOVDD = +3.1...+3.6 V, AVSS = DVSS = IOVSS = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS Protocol (ADI_CFG.biss = 1)						
I301	t_C	Clock Period	ADI_CFG.freq = 0 ADI_CFG.freq = 1	5.9 0.59	7.7 0.77	µs µs
I302	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I303	t_{busy}	Permissible Processing Time	relative to clock period		∞	% t_C
I304	t_{P0}	Permissible Propagation Delay (Line Delay Compensation)	not supported (data is captured on next rising clock edge)	0		ns
I305	Δt_P	Permissible Propagation Delay Variance	not supported (refer to t_S and t_H)			% t_C
I306	t_S	Setup Time: Data stable before clock edge lo → hi	without line delay compensation (t_{P0} = 0)	100		ns
I307	t_H	Hold Time: Data stable after clock edge lo → hi	without line delay compensation (t_{P0} = 0)	0		ns
I308	t_{TO}	Permissible Slave Timeout		t_C		µs
I309	t_{Cycle}	Clock Cycle Time	Note: This value can vary during operation.	1	3	ms
SSI Protocol (ADI_CFG.biss = 0)						
I310	t_C	Clock Period	ADI_CFG.freq = 0 ADI_CFG.freq = 1	5.9 0.59	7.7 0.77	µs µs
I311	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I312	t_S	Setup Time: Data stable before clock edge lo → hi		100		ns
I313	t_H	Hold Time: Data stable after clock edge lo → hi		0		ns
I314	t_{TO}	Permissible Slave Timeout		t_C		µs
I315	t_{Cycle}	Clock Cycle Time	Note: This value can vary during operation.	1	3	ms

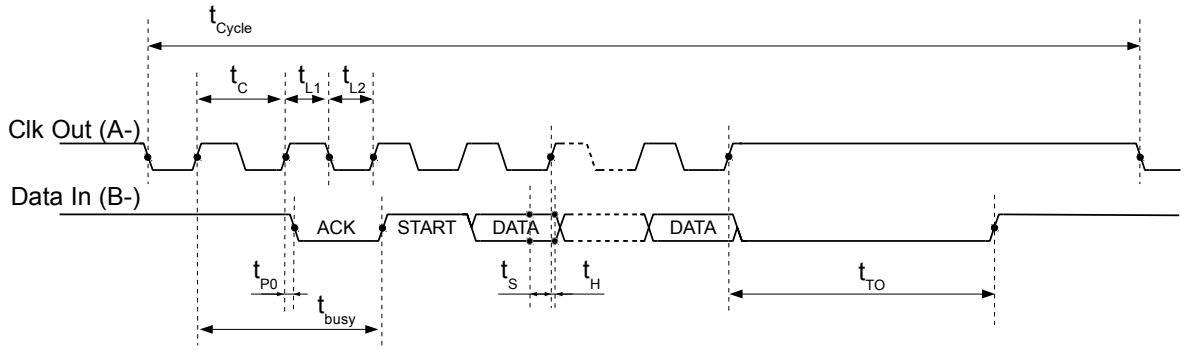

Figure 12: ADI timing with BiSS protocol

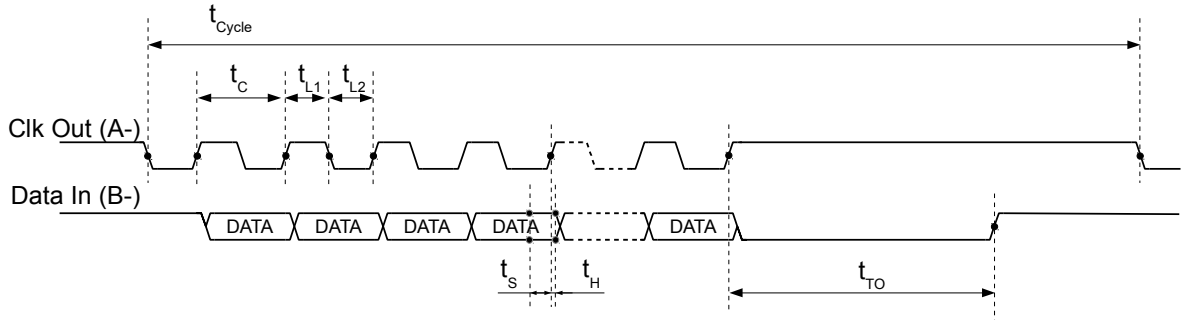

Figure 13: ADI timing with SSI protocol

FUNCTIONAL BLOCK DIAGRAM

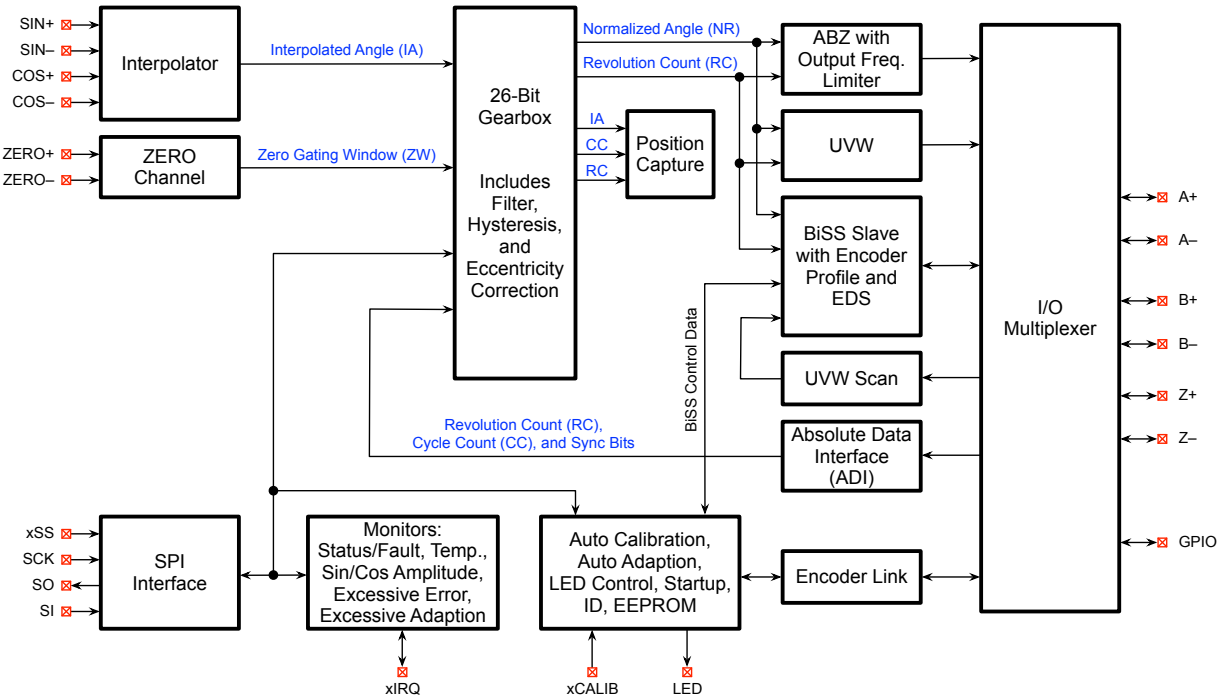

Figure 14: Functional Block Diagram

The iC-TW29 uses a modular architecture as shown in Figure 14.

Differential sine and cosine sensor signals are converted to a 14-bit interpolated angle (IA) within one input cycle by the interpolator. The interpolator also provides complete analog and digital error correction for the input signals to ensure lowest angular error and jitter. A sophisticated digital filter with fixed or variable bandwidths improves performance with noisy inputs.

The zero channel generates the zero gating window (ZW) from analog or digital zero or index sensors which can be used to generate a traditional once-per-revolution Z output. The ZERO input can also be used to reset the gearbox counter and to capture the current full absolute position of the iC-TW29.

The gearbox tracks the input cycles within a revolution and provides a normalized 26-bit output representing the angle within one output revolution (NR). This is synchronized with the revolution count (RC) and the cycle count (CC) from the absolute data interface (ADI) or SPI port to form the complete absolute position. A programmable noise and jitter filter increases angle resolution by two or more bits depending on configuration. Hysteresis and eccentricity correction

The full absolute position value of the iC-TW29 can be captured and read out over the SPI port. This position capture takes place on the rising edge of the zero gating window and can also be configured to generate an interrupt. The most recent four absolute position values are saved in a FIFO. This allows touch-probe or distance-coded index applications to be easily implemented.

Traditional encoder quadrature (ABZ) outputs are available as RS-422 compatible differential or single-ended signals depending on device configuration. The ABZ output resolution (edges or AB cycles per revolution) is programmable and independent of the input resolution (input cycles per revolution). The zero gating window (ZW) from the zero signal path can be used to generate a programmable-width Z output synchronized with the AB outputs. The Z output can also be synthesized from absolute position data when the ZERO input is not used.

The ABZ output module incorporates a programmable AB output frequency limiter that guarantees a minimum separation time between AB edges. This is useful to avoid counting errors with PLCs or counters with input frequency limits less than the 12.5 MHz maximum AB output frequency of the iC-TW29.

When the AB output frequency is being limited, the AB outputs lag behind the sin/cos inputs. If this condition is temporary or transient, the AB outputs catch up when the limiter is no longer active. If this condition persists, however, a fatal fault is generated and the iC-TW29 stops operating. The AB output frequency limiter can also be programmed to activate xIRQ.

3-phase UVW outputs for commutation of brushless motors with up to 64 poles (32 pole pairs) per revolution are also available as RS-422 compatible differential or single-ended signals depending on device configuration.

A BiSS Slave interface provides BiSS C-Mode bidirectional communication of output angle (with independently programmable resolution), revolution count, and configuration data. Encoder Profiles 3, 3S (Safety), and 4 are implemented in the iC-TW29 or a custom profile may be defined using a host processor. BiSS protocol commands are not executed by the iC-TW29 in stand-alone applications. Also in hosted applications, BiSS protocol commands are not passed onto the external microprocessor via the SPI port. However, user-defined system commands could be implemented on the microprocessor and called up by the BiSS control data communication.

The BiSS interface can be configured to implement BiSS Standard Encoder Electronic Data Sheet (EDS) SE. This allows the BiSS master to read the encoder configuration over the BiSS interface at startup. In hosted applications, the host processor can implement any BiSS EDS.

UVW scan mode allows external UVW signals to be read by the iC-TW29 and sent to the BiSS master with the BiSS single cycle data (BP4 or custom encoder profile only). This allows commutation of a brushless motor over BiSS before absolute position is synchronized.

The absolute data interface (ADI) is a BiSS/SSI master for reading revolution and cycle count information from an external absolute position system (such as iC-PVL). Up to four synchronization bits can be used.

The I/O multiplexer determines which signals are transferred to the output pins. One of 23 output modes (combinations of output types) can be selected. Up to two different output types may be used simultaneously.

The SPI port is available for use by an external host processor for initial calibration or general communication.

The iC-TW29 provides comprehensive monitoring functions for status and faults, chip temperature and sin/cos input signal quality.

The status/fault monitor monitors 16 internal conditions, each of which can be individually configured to activate a fault output to notify an external system during operation. The fault output is the active-low interrupt request output (xIRQ) pin. In stand-alone applications, xIRQ can be used to directly drive a fault LED. In hosted applications, xIRQ is typically used to interrupt the host when a fault occurs. In addition, real-time status and fault information is available over the SPI and BiSS interfaces.

The iC-TW29 incorporates an on-chip temperature sensor. The temperature monitor can provide real-time chip temperature data to a host processor or BiSS master. The temperature monitor can be configured to activate a status bit when chip temperature exceeds a programmable limit. This condition can also activate xIRQ.

The sin/cos amplitude monitor continuously monitors the amplitude of the sin/cos input signals by calculating the quantity $\sqrt{sin^2 + cos^2}$. If the input amplitude is outside configured limits, a status bit is activated and an interrupt can be generated.

The excessive error monitor continuously calculates the residual offset, balance, and phase error of the corrected sin/cos signals. These residues represent the uncorrected signal error of the sin and cos channels, and are typically zero (or near zero) when auto adaption is used. If any of the error residues exceeds configured limits, a status bit is set and an interrupt can be generated. In applications where auto adaption cannot be used, the residues allow sensor signal quality to be monitored by a host processor.

The excessive adaption monitor continuously compares the current offset, balance, and phase correction parameter values to baseline values store in the EEPROM during device configuration. If any of the correction values deviate from the base values (due to auto adaption) by more than the configured limits, a status bit is set and an interrupt can be generated.

Auto calibration is used at initial device commissioning to automatically determine gain, offset, channel balance, and phase compensation values for the sin, cos, and zero channels. Auto calibration is initiated using the xCALIB input pin or via a serial command. Calibrated values can be stored in the internal EEPROM for use on subsequent startups.

Auto adaption maintains optimal offset, channel balance, and phase compensation values for the sin and cos channels during operation to ensure maximum interpolator accuracy and lowest jitter under all operating conditions.

A configurable LED intensity control uses the calculated sin/cos amplitude value to control the intensity of an optical sensor LED via the pulse-width modulated LED output (pin 26). This maintains the sin/cos signals at their calibrated amplitude in the presence of LED ageing and varying application conditions.

Device startup can proceed automatically for stand-alone applications or under the control of a host processor in hosted applications. In general, outputs are not enabled until the appropriate position (relative or absolute) is established.

Device and chip identification is provided in the form of a unique factory-programmed chip serial number as well as a chip ID and revision code. In BiSS applications, user-programmable manufacturer ID, product ID, device serial number, and production date are available.

The iC-TW29 incorporates an internal write-protected EEPROM to store configuration and initial calibration data for use at startup. In addition to a standard checksum on the EEPROM data, sophisticated data encoding allows detection and correction of single-bit errors and detection of two-bit errors for enhanced application security. The EEPROM can be unlocked using the SPI, and using BiSS or the Encoder Link interfaces if configured.

The Encoder Link interface provides read/write access to the iC-TW29's internal registers using the A+ and A– outputs in ABZ or UVW output modes. This is useful for field reconfiguration or diagnostics of products incorporating the iC-TW29. Encoder Link can only be used for configuration and diagnostics, it cannot be used to read position. Encoder Link can be disabled to eliminate tampering with finished products.

ELECTRICAL CONNECTIONS

The basic electrical connections for an incremental stand-alone application with differential ABZ outputs are shown in Figure 15. Other than the sin/cos sensor, only a few bypass capacitors and other components are required for operation.

Application Hint
The input voltages must not exceed the chip's supply voltage (3.3 V).

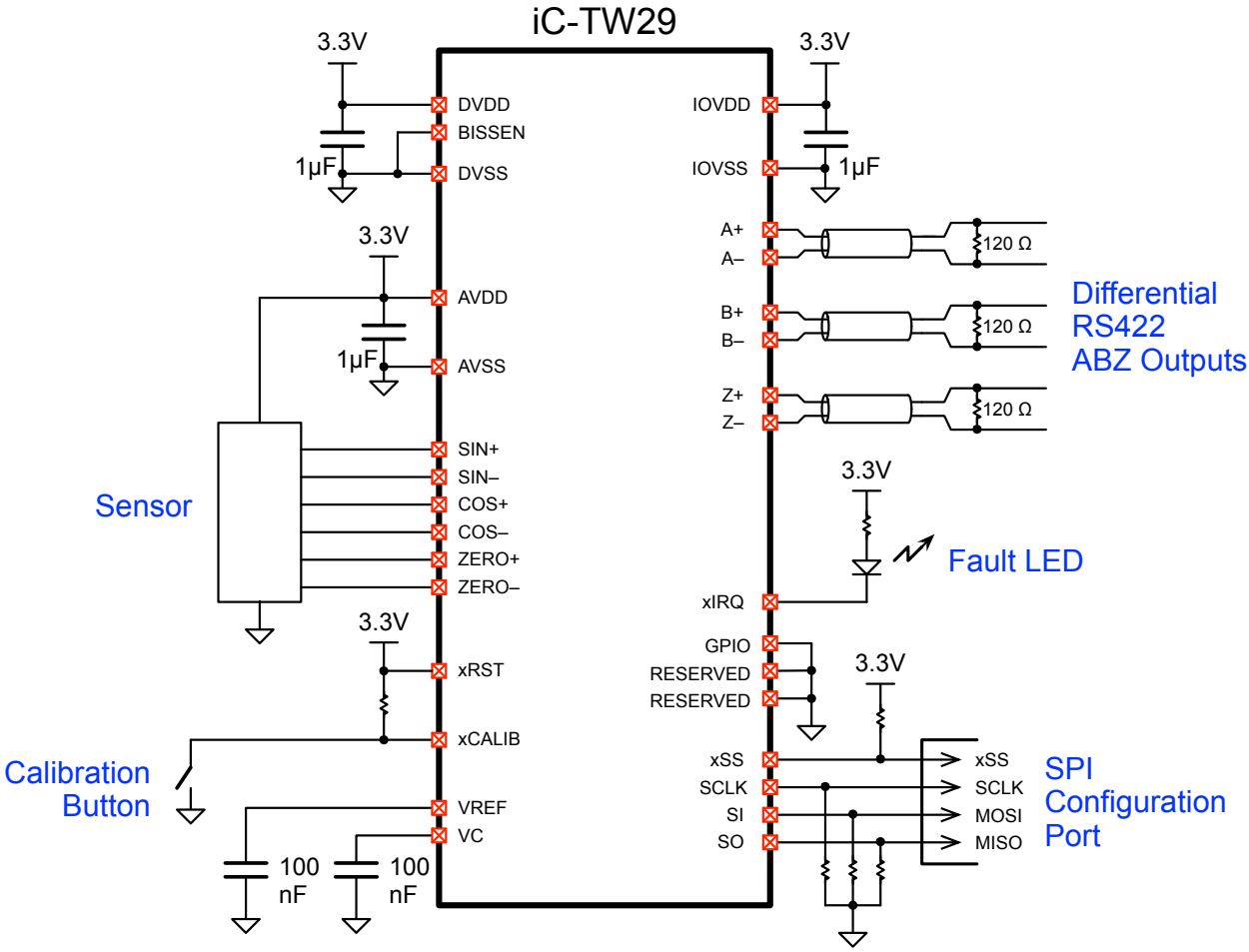

Figure 15: Typical Electrical Connections For Incremental Stand-Alone Application

The basic electrical connections for an absolute multiturn stand-alone application using BiSS are shown in Figure 16. An external RS422-compatible driver/receiver, such as the iC-HF, and a 5 V-to-3.3 V level shifter, such as the TXS0104E, is required. An external multiturn device, such as the iC-PVL, is connected to the absolute data interface.

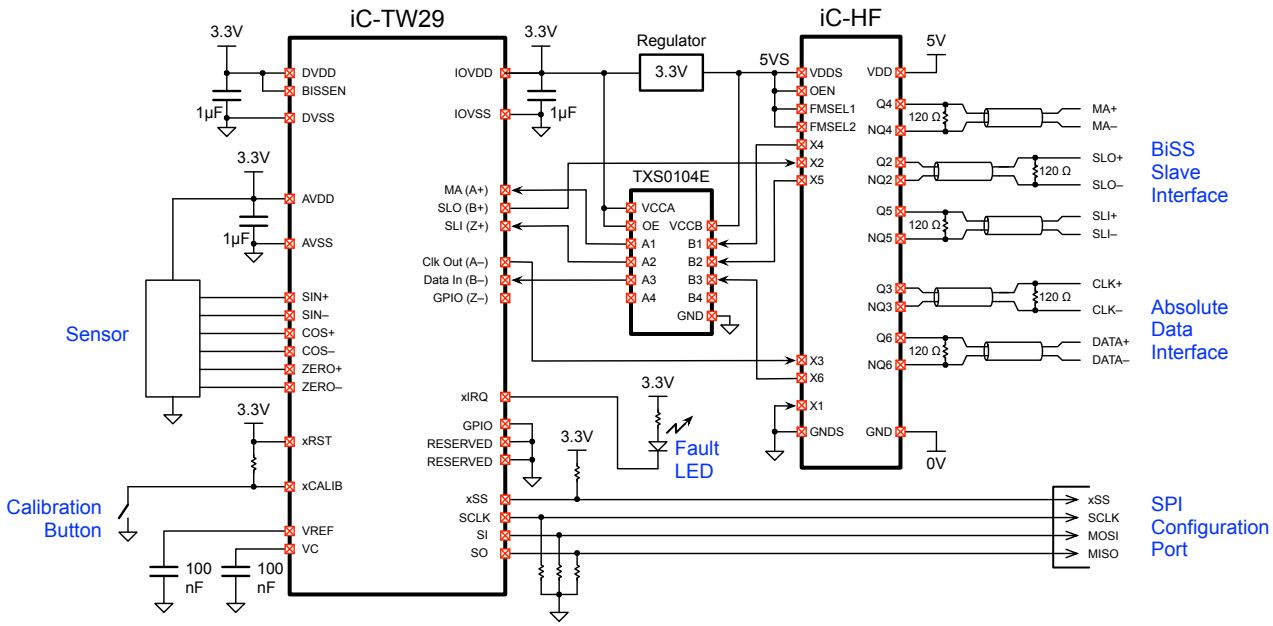

Figure 16: Typical Electrical Connections For Absolute BiSS Stand-Alone Application

Alternatively, resistive voltage dividers can be used instead of an explicit level shifter chip. In this case, values of 470 Ω and 560 Ω are recommended to drive MA (A+), SLI (Z+), and Data In (B–). This will add 15 mA of current consumption.

The BiSS interface is enabled by connecting the BiSSEN input pin to 3.3 V as shown. The iC-HF is used in BiSS bus structure mode. See the iC-HF data sheet for more information.

The basic electrical connections for an incremental hosted application using a single iC-TW29 are shown in Figure 17. Multiple iC-TW29s can also be bussed or chained together using the same SPI port on the host processor.

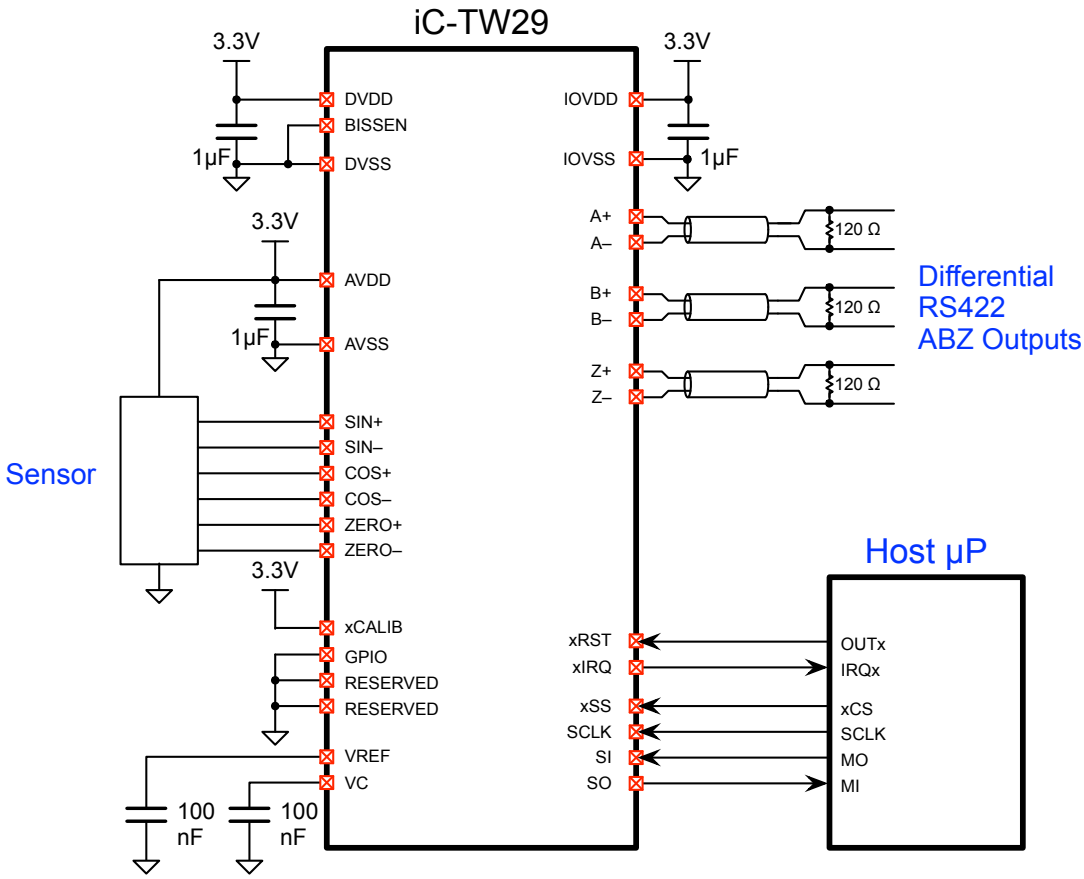

Figure 17: Typical Electrical Connections For Hosted Application

Power and Ground
The iC-TW29 requires a high quality ground and clean 3.3 V power supplies. There are three separate power/ground pin pairs, one each for the analog (AVDD/AVSS), digital (DVDD/DVSS), and I/O (IOVDD/IOVSS) circuitry.

In most cases, it is sufficient to connect all three power pins to the same low-impedance power source, preferably an on-board voltage regulator. Likewise, the three ground pins can usually be connected to the same solid ground plane on the PC board. If necessary, separate voltage regulators can be used to power each section to provide enhanced noise immunity. In all cases, each power pin should have a dedicated 1µF decoupling capacitor placed as close to the iC-TW29 as possible.

Reference Outputs
The reference outputs VREF and VC must each be decoupled to ground with separate 100 nF capacitors placed as close to the iC-TW29 as possible. VC should not be used to bias external circuitry or the sin/cos or ZERO inputs with single-ended sensors.

xCALIB Input
The active-low xCALIB input is used to activate the auto-calibration feature of the iC-TW29. A push-button and pull-up resistor can be connected to this input as shown for easy manual calibration. xCALIB can also be controlled by a host processor output, if desired.

If push-button calibration is not required, xCALIB should be connected to 3.3 V to avoid spurious calibration.

SIN and COS Inputs
The iC-TW29 connects directly to magnetic (such as iC-SM2L or iC-SM5L) and optical (such as iC-LSHB or iC-PT...H series) sensors providing differential sin/cos outputs, as shown in Figure 18 and Figure 19.

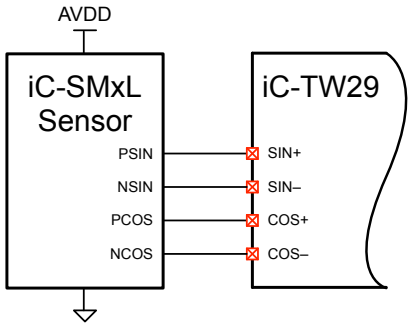

Figure 18: Magnetic Sensor Connection

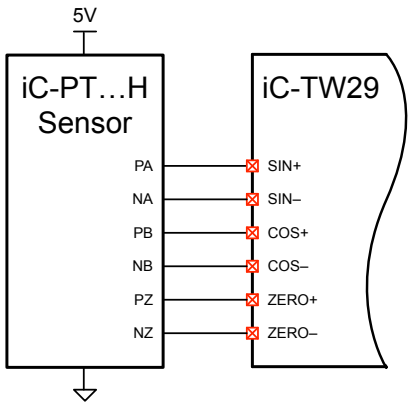

Figure 19: Optical Sensor Connection

Nominal differential signal amplitudes between 20 mV and 2.0 V in two ranges can be accommodated.

ZERO Inputs

The iC-TW29 can interface to a wide range of differential or single-ended index or zero sensors to provide a Z output which is synchronized with the AB outputs or to reset the gearbox counter. Optical sensors usually provide differential zero or index signals along with the sin/cos signals. In magnetic systems, a separate zero sensor is usually required.

Digital zero sensors (Hall, MR, and others) typically provide a single-ended active-low signal via an open-drain output that pulls low in the presence of a magnetic field. Connect active-low (open drain) digital index sensors to the iC-TW29 ZERO– input and connect the ZERO+ input to VDD/2 using a resistive voltage divider as shown in Figure 20.

For active-high (open source) digital index sensors, reverse the ZERO+ and ZERO– connections.

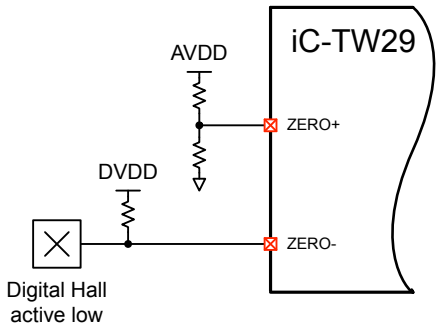

Figure 20: Digital Index Sensor Connection

Analog-output zero sensors, such as MR bridges, can also be used with the iC-TW29 as shown in Figure 21.

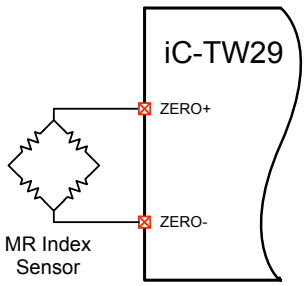

Figure 21: Analog Index Sensor Connection

If no zero sensor is available, it is recommended to link the ZERO+ and ZERO– inputs to fixed potentials.

Connecting ZERO+ to ground and ZERO– to 3.3 V is useful in on-axis applications, where an input revolution produces only a single input cycle that is absolute in angle. In this case, a synthetic Z output can be generated and revolution counting is operational.

Connecting ZERO+ to 3.3 V and ZERO– to ground generates a zero gating window (ZW) that is permanently high, which enables a gated Z output, but may clear the gearbox counter (no revolution counting).

It is possible, however, to invert the generated zero gating window (ZW) by configuration.

ABZ Outputs
The iC-TW29 can be configured to provide differential ABZ outputs capable of driving 20 mA into a terminated RS422 line. The A+, A–, B+, B–, Z+, and Z– outputs can be directly connected to the RS422 line as shown in Figure 22.

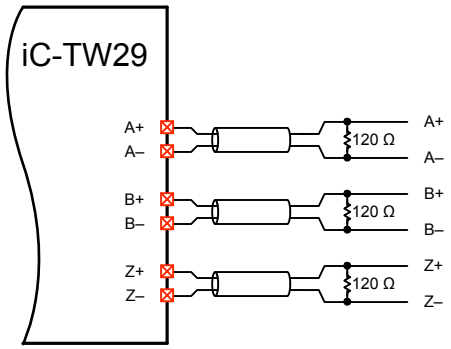

Figure 22: ABZ Output Connection

The three signal pairs should be terminated with a 120 Ω resistor at the far (receiving) end of the cable as shown. The RS422-compatible line driver can be disabled to save power for local or short-run applications. In this case, termination resistors should not be used.

UVW Outputs
The iC-TW29 can be configured to provide differential UVW outputs or simultaneous single-ended ABZ and UVW outputs.

xRST Input
The iC-TW29 contains a built-in power-on-reset (POR) circuit that controls the safe startup of the device. In most applications, no external components are required and xRST can be connected directly to 3.3 V.

Alternatively, an RC network with recommended values of 47 kΩ and 100 nF can be connected to the active-low xRST input to extend device reset in case of a slow-rising supply as shown in Figure 23.

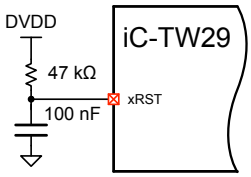

Figure 23: xRST Connection

In stand-alone applications, it is recommended to always provide for an RC network on the PC board and only populate the capacitor if required. Without the capacitor, the resistor provides the necessary pull-up.

In hosted applications, the xRST input is best controlled by the host. For battery-powered applications, the host can hold xRST low to reduce power consumption (low power mode). See spec. item 005.

xIRQ
In stand-alone applications, xIRQ functions as an active-low fault output. It can be used to directly drive an LED with an appropriate current-limiting resistor for fault indication.

In hosted applications, xIRQ can be connected to an interrupt request input on the host processor. In this way, when a warning or fault occurs, the host processor can query the iC-TW29 to determine what action to take. xIRQ can also be configured as an external fault input.

xIRQ can be configured as an open-drain output allowing a wired-OR connection of multiple iC-TW29s to a single interrupt request input on the host processor.

Finally, xIRQ can be configured as an external interrupt request input.

LED Output
The iC-TW29 can be configured to provide LED intensity control for optical sensors. The LED output functions as a high-current output to drive the illumination LED used with an optical sensor.

If the LED intensity control functionality is not needed, the LED output can be configured for use as general-purpose I/O.

BiSSEN Input
The BiSSEN input is used to enable the TW29's BiSS interface. Connect BiSSEN to 3.3 V to enable the BiSS interface; connect BiSSEN to ground to disable the BiSS interface. Regardless of the EEPROM configuration data, the I/O pins A+, B+, Z+ are used for MA, SLO, SLI.

General-Purpose I/O
The GPIO pin can be configured as a general-purpose input or output. If configured as an input, it can be further configured as a BiSS position preset input. In this case, a push-button and pull-up resistor can be connected to this input for easy manual presetting.

SPI Port
The iC-TW29 provides a standard SPI (Serial Peripheral Interface) slave port that can be used for device configuration and communication with a host processor. Connect the SPI port pins to the host processor as shown in Figure 24.

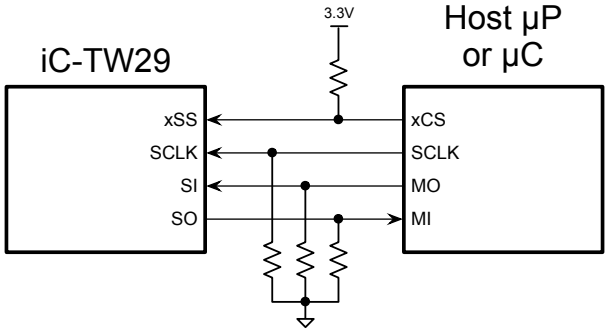

Figure 24: SPI Port Connection

If the host processor or microcontroller can be disconnected, the SPI port pins must be pulled up or down as shown in Figure 24. Do not allow any of the SPI port pins to float.

Although Figure 24 shows a single-device application, multiple iC-TW29's can also communicate over a single SPI channel to a host processor.

Reserved Pins
All reserved pins must be tied to ground as shown in Figures 15, 16, and 17 for proper operation.

CONFIGURATION AND CALIBRATION

Introduction

The iC-TW29 uses a modular architecture. This means that only the enabled modules and required features need to be configured. For example, if ABZ outputs are not enabled, the ABZ output module does not need to be configured.

Configuration values for enabled modules and required features must be written to the TW29's internal EEPROM using the BiSS or SPI ports or the Encoder Link interface before the device can be used. For stand-alone applications, the easiest way to accomplish this is to use one of the iC-TW29 demo boards and the free Graphical User Interface (GUI) software.

The iC-TW29 EVAL TW29_1D evaluation board implements the iC-TW29 and a USB interface for direct communication with the GUI software for ABZ and UVW applications. The iC-TW29 EVAL TW29_3D evaluation board implements the iC-TW29 and a USB interface for direct communication with the GUI software for BiSS and SSI applications. Using one of these boards, a functional prototype encoder can be quickly assembled and configured. See the iC-TW29 EVAL TW29_1D and 3D datasheet for more information.

The TW29_1D evaluation board includes a break-away programmer that can be used for prototype development to configure an external iC-TW29 via the SPI or Encoder Link interfaces using the free GUI software. In series production, this programmer can be employed to download pre-engineered configurations to iC-TW29s embedded in products.

In hosted applications (where the SPI port is used to communicate with the host processor), the iC-TW29 must be configured via the host, or through the BiSS or Encoder Link interfaces.

The remainder of this section assumes use of a TW29_1D (ABZ) or TW29_3D (BiSS) demo board in a rotary application with or without a zero sensor. The GUI software is used for configuration and calibration via SPI communication.

Default Configuration

To ensure known starting conditions, load the default configuration file using the File menu in the GUI. This sets all parameters to their default or recommended values and disables the monitors to avoid nuisance faults during configuration and calibration. Once the iC-TW29 is configured and calibrated, the monitors and other advanced features can be enabled as needed.

Click on the EEPROM block in the block diagram on the main GUI window to open the EEPROM tab and save the default configuration to EEPROM. Finally, restart the iC-TW29 by clicking the play button (▷) on the main GUI window.

Note: iC-TW29 QFN32-5x5 devices as shipped are not pre-programmed to allow operation. A predefined application configuration file or the default configuration file must be loaded to an as-shipped chip and saved to EEPROM before attempting any additional configuration.

Input Configuration and Calibration

Click on the AFE-IPO (Analog Front End and Interpolator) tab. Select the signal range that corresponds to the attached sin/cos and zero sensors. In general, use low range for passive sensors (like AMR and un-amplified Hall) and high range for powered (amplified Hall or photo diode) sensors. See Figures 2 and 3 for more information on signal ranges. The other parameters can be left at their default values.

In the Calibration tab, check "Auto calibrate sine/cosine offsets, gains, and phase" and "Automatically store calibrated values to EEPROM." If a zero sensor is connected, also check "Auto calibrate zero analog offset and gain" and "Auto calibrate IA phase shift."

With the sin/cos and zero (if used) sensors generating signals, click the Auto-calibration "Start" button in the GUI or the xCALIB button on the demo board to begin auto calibration. When the values in the signal path diagram on the Calibration tab have settled to non-zero values, click the Auto-calibration "Stop" button. This stops auto calibration and stores the calibrated values to EEPROM.

With the sensors still generating signals, click the Adaption tab. The Sine and Cosine Amplitude bar graphs should show signal amplitudes of 2400±100. If not, change the input range settings (AFE-IPO tab) as required and re-run auto calibration.

Once the signal path has been successfully calibrated, enable auto adaption in the adaption tab for offset, balance, and phase as required. Save these configuration values to EEPROM using the EEPROM tab. With auto adaption enabled and the sensors generating signals, the correction values on the signal path diagram in the calibration tab should be changing by small amounts.

In the Gearbox tab, set the Revolution Counter Length as required. If revolution counting is not needed, set the counter length to zero.

Set the Input Cycles per Revolution to match the number of sin/cos cycles generated by the sensor per output revolution. Save these values to EEPROM. The other parameters in this tab can be left at their default values.

ABZ/UVW Configuration
To provide differential and line driver ABZ or UVW outputs, the iC-TW29 must not be in BiSS mode. Confirm that BISSEN = 0 in the main GUI window. This is the case with the TW29_1D demo board.

In the I/O tab, select the desired functionality of the positive and negative outputs. For example, for differential RS-422 ABZ outputs, select "A+, B+, Z+" for the positive outputs, select "A–, B–, Z–" for the negative outputs, and enable the RS422 line driver. The other parameters in this tab can be left at their default values.

In the ABZ/UVW tab, enter the resolution for the AB outputs as the desired number of increments (edges) per output revolution. Enter the desired number of UVW cycles per output revolution if the UVW outputs are used. The other parameters in this tab can be left at their default values. Save the configuration to EEPROM using the EEPROM tab, and restart the iC-TW29 by clicking the play button (▷) in the main GUI window.

BiSS/SSI Configuration
To use BiSS or SSI output, the iC-TW29 must be in BiSS mode. Confirm that BISSEN = 1 in the main GUI window. This is the case with the TW29_3D demo board.

The default BiSS configuration uses BP3 (Standard Encoder Profile), 4 096 increments per singleturn revolution, and no multiturn bits. This configuration may be changed as desired, but the iC-TW29 must be restarted by clicking the play button (▷) in the main GUI window for any changes to be recognized by the BiSS Master.

REVISION HISTORY

Rel.	Rel. Date†	Chapter	Modification	Page
A1	2019-01-25	...	Initial release	all

Rel.	Rel. Date†	Chapter	Modification	Page
B1	2019-09-24		Refer to the revision history of the release.	

Rel.	Rel. Date†	Chapter	Modification	Page
C1	2020-06-08		Refer to the revision history of the release.	

Rel.	Rel. Date†	Chapter	Modification	Page
C2	2021-02-03		Refer to the revision history of the release.	

Rel.	Rel. Date†	Chapter	Modification	Page
C3	2021-09-29		Refer to the revision history of the release.	

Rel.	Rel. Date†	Chapter	Modification	Page
D1	2022-12-12	ABSOLUTE MAXIMUM RATINGS	Item G004: CDM added	8
		ELECTRICAL CHARACT.	Items 003, 004: max limits Items 111, 206: condition and typical value Item 705 added for clarity Item 809: symbol name, condition	9, 10
		OP. REQ.: Encoder Link	Condition RS422 added in headlines	14
		OP. REQ.: BiSS Interface	Update of parameter and symbol names (I207, I217) and Figures 9, 10, 11	15
		OP. REQ.: ADI Interface	Items I001, I201, I208: links to Elec.Char. added Items moved: I101→I109, I110→I115 Update of parameter and symbol names (I309, I315) and Figures 12, 13	16
		General Notice	The longform datasheet may contain further changes.	

Rel.	Rel. Date†	Chapter	Modification	Page
D2	2023-03-28	ELECTRICAL CHARACT.	Items 304, 305: update of INL/DNL	9ff
		General Notice	The longform datasheet may contain further changes.	

Rel.	Rel. Date†	Chapter	Modification	Page
D3	2025-01-08	PACKAGING INFORMATION	Footnote 7 added.	4
		ELECTRICAL CONNECTIONS	Description added to ZERO input wiring	23
		CONFIGURATION AND CALIBRATION	Setting of RC counter length	26
		General Notice	The longform datasheet may contain further changes.	

† Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-TW29	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant		iC-TW29 QFN32-5x5
ABZ Evaluation Board and SPI Programmer	PCB, approx. 50 mm x 123 mm		iC-TW29 EVAL TW29_1D
BiSS Evaluation Board	PCB, approx. 50 mm x 123 mm		iC-TW29 EVAL TW29_3D
iC-TW29 GUI		Evaluation software for Windows PC (entry of IC parameters, file storage, and transfer to DUT)	For download link refer to www.ichaus.com/tw29

Please send your purchase orders to our order handling team:

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E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

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