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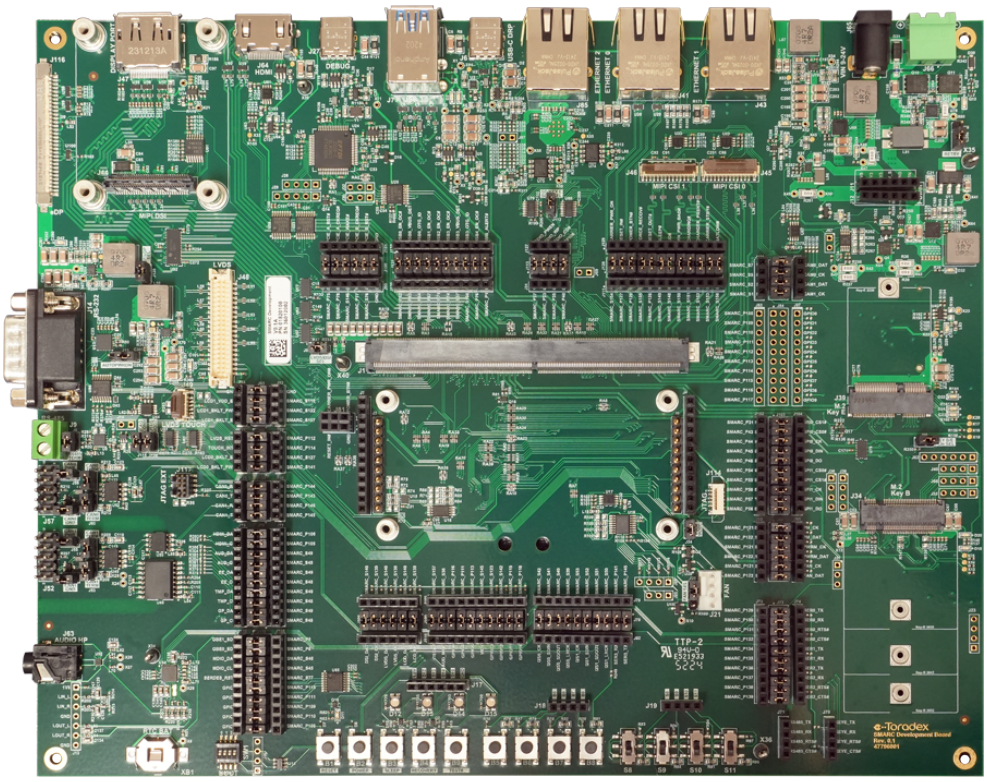
SMARC Development Board

Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
30-May-2025	Rev. 0.1	V1.1A	Initial release.
11-Jul-2025	Rev. 0.2	V1.1B	Updated to reflect hardware revision V1.1B. No changes to technical content.
08-Sep-2025	Rev. 0.3	V1.1B	Section 3.2: add Power Supply block diagram on Figure 3 Section 3.5: added Ethernet Interface section Section 3.6: added PCIe Interface section Section 3.7: added USB section Section 3.12: added Temperature Sensor section Section 3.13: added EEPROM section Section 3.14: added Backup Battery section Section 3.16: add USB Debugger block diagram on Figure 6 Section 3.17: added SD Card Interface section Section 3.19: added Audio section

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1 Introduction

The SMARC Development Board is a flexible development board to explore and evaluate the functionality and performance of the SMARC product family.

Complementing the SMARC computer on module, the SMARC Development Board supports a wide variety of industry-standard interfaces while at the same time providing advanced multimedia and high-speed connectivity options, making it suitable for an almost unlimited number of applications. SMARC interfaces can be easily accessed using physical connectors and standard pitch headers.

1.1 Reference Documents

For detailed technical information, please refer to the documents listed below.

1.1.1 SMARC Computer on Module family overview

https://www.toradex.com/computer-on-modules/smarc-arm-family

1.1.2 Toradex Developer Website – SMARC Computer on Module documents

https://developer.toradex.com/hardware/smarc-som-family/modules/

1.1.3 Carrier Board Layout Guide

https://developer.toradex.com/carrier-board-design/carrier-board-design-guides/

1.1.4 Toradex Developer Website – SMARC Development Board Design Resources

https://developer.toradex.com/hardware/smarc-som-family/carrier-boards/smarc-development-board/#design-resources

1.1.5 EEPROM datasheet

https://www.st.com/resource/en/datasheet/m24c01-w.pdf

1.1.6 Temperature Sensor datasheet

https://www.ti.com/lit/ds/symlink/tmp1075.pdf

1.1.7 USB HUB datasheet

https://cdn.amphenol-cs.com/media/wysiwyg/files/documentation/datasheet/inputoutput/io_usb_3_1_gen2_gsb4x.pdf

1.1.8 Gigabit Ethernet Transceiver datasheet

https://www.ti.com/lit/ds/symlink/dp83867ir.pdf

1.1.9 RS232 Transceiver datasheet

https://www.ti.com/lit/ds/symlink/trs3122e.pdf

1.1.10 RS485 Transceiver datasheet

https://www.ti.com/lit/ds/symlink/sn65hvd01.pdf

1.1.11 CAN Transceiver datasheet

https://www.ti.com/lit/ds/symlink/tcan1044-q1.pdf

1.1.12 Audio Codec datasheet

https://statics.cirrus.com/pubs/proDatasheet/WM8904_Rev4.1.pdf

1.1.13 Fan Controller datasheet

https://www.ti.com/lit/ds/symlink/amc6821.pdf

1.1.14 USB Type-C Configuration Channel Logic IC datasheet

https://www.ti.com/lit/ds/symlink/tusb320li.pdf

1.1.15 UV/OV and Reverse Protection Controller datasheet

https://www.analog.com/media/en/technical-documentation/data-sheets/ltc4368.pdf

1.2 Abbreviations

Table 1: Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity

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Table 1: Abbreviations (Continued)

Abbreviation	Explanation
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

2 Features

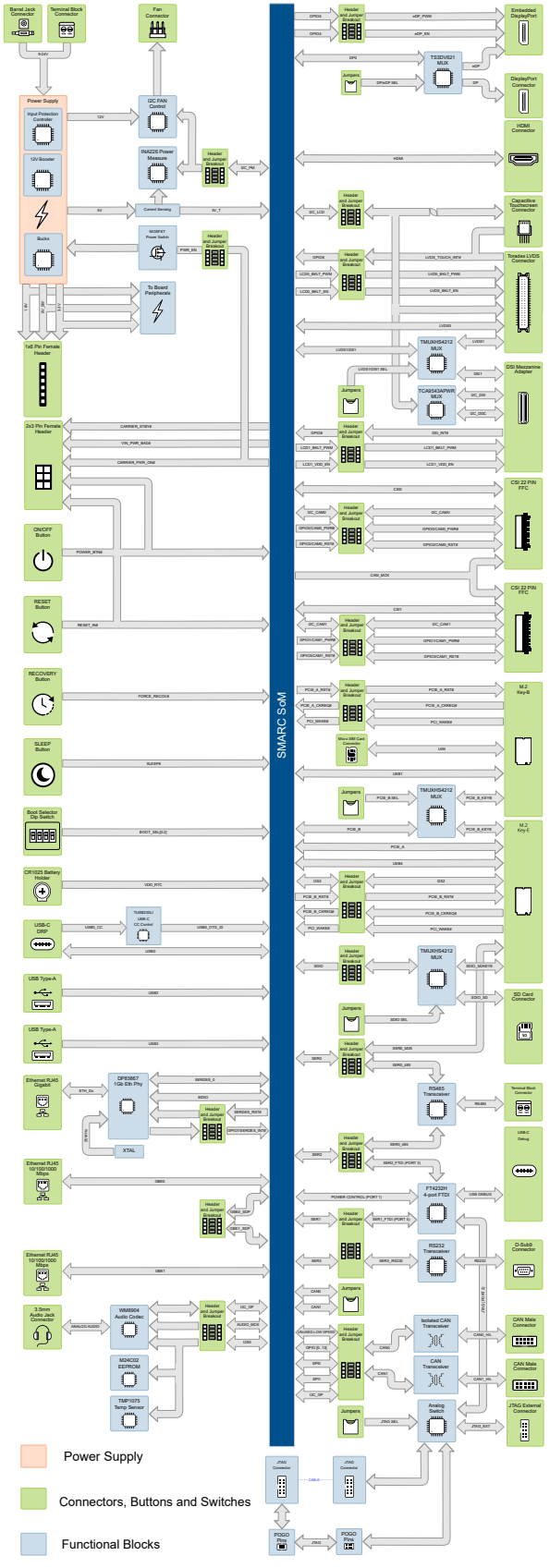
2.1 Main Features

The SMARC Development Board provides the following features and communication interfaces:

- 1x stacked USB 3.0 Type-A connector, featuring 2x USB ports through the on-board USB HUB
- 1x USB-C connector providing USB Dual-Role-Port (DRP) or host/client functionality
- 1x USB-C debug connector (optionally connected to UART3, UART4, and JTAG through the multi-purpose USB to serial converter based on the FT4232HL IC)
- 2x RJ45 connectors featuring 10/100/1000 Mbps Ethernet interfaces (1x Ethernet transceiver placed on the Development Board)
- 1x PCIe M.2 B-Key connector
- 1x PCIe M.2 E-Key connector
- 1x HDMI Type A connector
- 1x SMARC module edge connector
- 2x MIPI® CSI Camera Interface connectors
- 1x MIPI DSI Display interface with a board-to-board connector which allows for connecting the Toradex DSI to HDMI adapter card
- 1x LVDS connector compatible with the Toradex Capacitive Touch Display 10.1" LVDS
- 1x JTAG connector
- 1x 4-bit SD® Card connector
- 1x I^2C 2Kb EEPROM IC
- 1x Digital Temperature Sensor
- 1x Analog Audio Output on 3.5mm stereo jack
- 1x RS232 Serial Interface on a 9-pin D-Sub connector
- 1x RS485 Serial Interface on a Screw Terminal Block connector
- 5x I^2C, 2x SPI and 3x PWM interfaces
- 1x DisplayPort connector
- 1x Embedded DisplayPort (eDP) connector
- 2x CAN interface headers, both supporting regular CAN (up to 1Mbps) and CAN FD (up to 5Mbps)
- 1x Real-time clock backup battery holder
- 14x dedicated GPIOs
- 4x general-purpose LEDs, switches and push buttons
- 1x Reset, recovery, sleep, power, and test buttons
- 1x Reset Indicator LED
- Undervoltage, overvoltage, overcurrent and reverse voltage protected power input

2.2 Hardware Architecture Block Diagram

Figure 1: SMARC Development Board Hardware Architecture



2.3 Physical Drawing

2.3.1 Top Side Connectors

Figure 2: SMARC Development Board connectors and controls

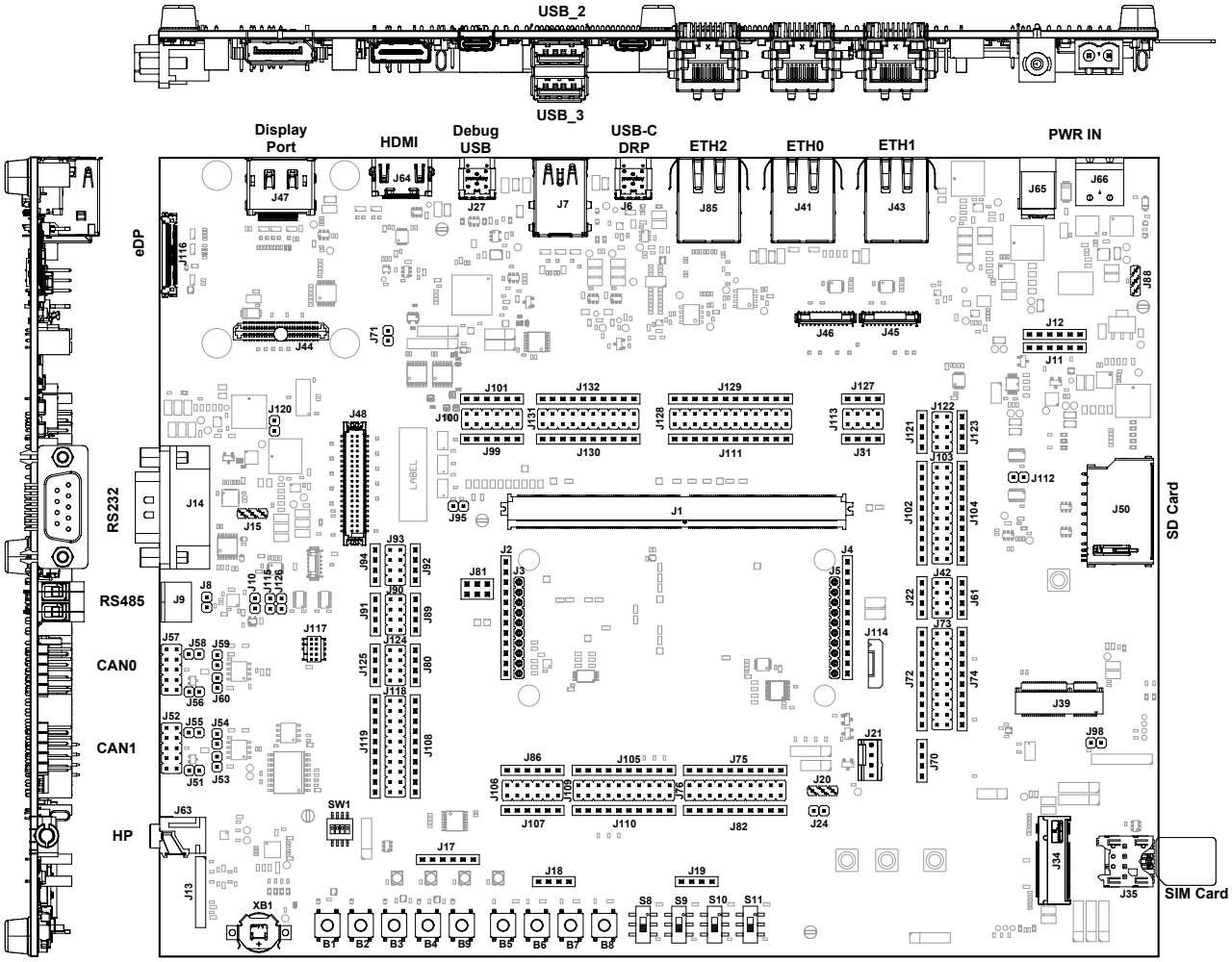


Table 2: Top Side Connectors

Designator	Description	Remarks
J1	SMARC module edge connector ()	
J6	USB DRP Connector	USB-C (USB 2.0 only)
J7	2x USB3.0 HOST connector	UPPER: USB_3 - LOWER: USB_2
J9	RS485 Connector	2-pin Terminal Block
J14	RS232 Connector	9-pin D-Sub
J21	Fan Connector	
J27	USB to Serial, USB to JTAG interface connector	USB-C (USB 2.0 only)
J34	PCIe M.2 B-Key connector	
J35	SIM Card Holder	Micro SIM

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Table 2: Top Side Connectors (Continued)

Designator	Description	Remarks
J39	PCIe M.2 E-Key connector	
J41	Ethernet connector	Ethernet_0
J43	Ethernet connector	Ethernet_1
J44	MIPI DSI Display Adapter connector	
J45	MIPI CSI Camera connector	CSI0
J46	MIPI CSI Camera connector	CSI1
J47	DisplayPort Connector	
J48	LVDS Connector	
J50	SD Card 4-bit connector	
J52	CAN1 interface header	Isolated
J57	CAN0 interface header	Non-isolated
J63	Analog audio HEADPHONE OUT Jack	Stereo
J64	HDMI Connector	
J65	Barrel Jack Power Supply connector	9-24V ±10%
J66	Terminal Block Power Supply connector	9-24V ±10%
J85	Ethernet connector	Ethernet_2, SGMII
J116	eDP Connector	
J117	JTAG Connector	
XB1	CR1025 Battery Holder	

3 Interface Description

3.1 SMARC System-On-Module

Connector Type: 314 pin PCIe MXM 3.0 socket

Manufacturer: Amphenol

Part Number: 10151114-001TLF

For the pinout of the SMARC module, please refer to the applicable SMARC module datasheet or to the SMARC Family Specification / SMARC Carrier Board Design guide for the abstract pinout. Stand-offs are available on SMARC Development Board for affixing the SMARC module to the Development Board. It is recommended to use M2.5×6mm size screws to fasten the SMARC module with the stand-offs.

3.2 Power Supply

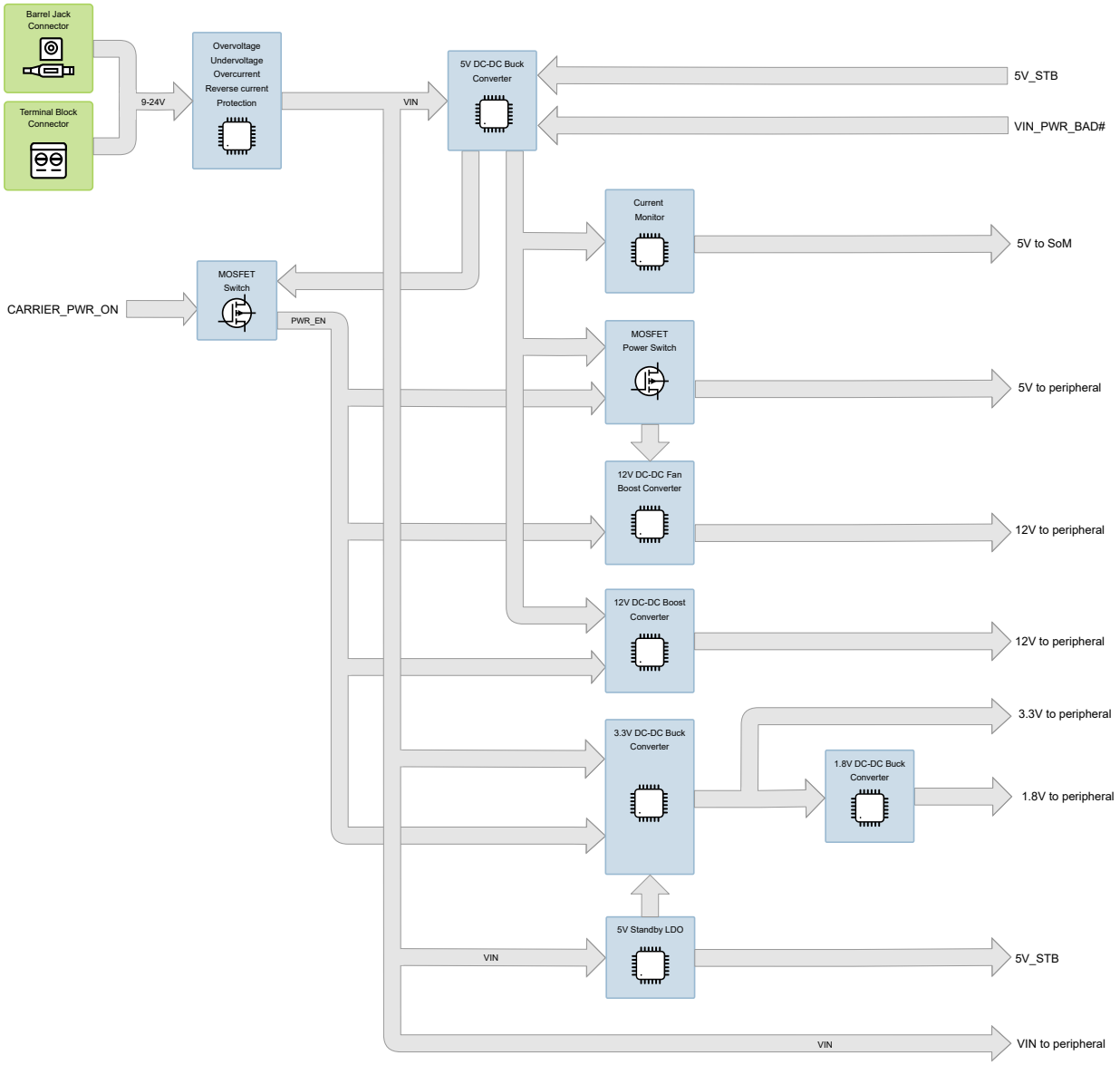
The SMARC Development Board has two different power connectors that can power the board: J65 and J66. Both are wide input range connectors tied together.

The Barrel Jack Power Connector J65 and the Terminal Block Power Connector J66 are electrically connected, and only one of these connectors should be used for powering the board. The simultaneous connection of two power supplies is not allowed. Violating this requirement may cause damage to the power supplies or to the Development Board.

Input voltage can vary across a range of 9-24V ±10%. The maximum input current is limited to 5A via Fuse F1. Power usage is estimated around 10-20W, though power consumption varies with type of SOM and connected peripherals (especially type and number of connected USB devices). If your application dissipates more than 35W, please work with a higher input voltage, up to 24V.

Several power domains are available on the Development Board. The board's power supply architecture is shown in the picture below.

Figure 3: SMARC Development Board Power supply Architecture



The on-board power supplies provide the following nominal voltages and currents.

Table 3: On-Board Power Supplies

Nominal voltage	Maximum current	Maximum power
12V	5A	40W
3.3V	8A	26.4W
1.8V	2A	3.6W

3.2.1 Barrel Jack Power Supply Connector (J65)

Connector Type: Barrel Jack

Manufacturer: Same Sky (former CUI Devices)

Part Number: PJ-059A

Table 4: Barrel Jack Power Supply Connector (J65)

Pin	Description	Voltage / Range
1	V+_IN	9-24V ±10%
2	GND	

3.2.2 Terminal Block Power Supply Connector (J66)

Connector Type: Terminal Block

Manufacturer: Phoenix Contact

Part Number: 1923759

Table 5: Terminal Block Power Supply Connector (J66)

Pin	Description	Voltage / Range
1	GND	
2	V+_IN	9-24V ±10%

3.2.3 Power Out Header (J11, J12)

Two female pin headers J11, J12, with main system voltages are available on it, can be used for powering external boards and modules. Pinout of the J11, J12 connectors is identical.

Connector Type: 1×6 Pin Header Female, 2.54mm pitch

Table 6: Power Out Header (J11, J12)

Pin	Description	Remarks
1	VIN	
3	GND	
4	+5V_SW	
5	+3V3	
5	+3V3	
6	+1V8	

3.2.4 Power Control

The SMARC Development Board power control is implemented by assigning the buttons B1, B2 to the RESET and POWER functions, respectively. The B3 button is used to put the SOM in SLEEP mode, while the B4 button is used to put the installed SMARC Computer Module into RECOVERY mode.

3.2.5 Power Supply Input Protection

Supply input is protected against ESD strikes, reverse voltage polarity, overvoltage, undervoltage, and short circuits. The protection circuit is based on an LTC4368 IC from Analog Devices. For detailed information, please refer to the LTC4368 datasheet.

Table 7: Power Supply Input Ratings

Parameter Name	Min	Typ	Max	Unit
Input voltage (Absolute maximum, limited with an ESD diode)	9 ±10%	12	24 ±10%	V
Undervoltage threshold	7.49	7.6	7.71	V
Overvoltage threshold	27.09	27.5	27.91	V
Overcurrent protection	4.5	5	5.5	A
Reverse current protection		-1.5	-2.5	mA

Jumper J88 can be used to turn ON or OFF the retry function of the power supply input protection circuit.

Connector Type: 1×3 Pin Header Male, 2.54 mm pitch

Table 8: Jumper Position (J88)

Jumper Position	Description
1-2	Power supply input will restart automatically after a forward overcurrent fault. The restart delay time is defined by capacitor C266 $5.5ms/nF$. The typical value for the SMARC Development Board is 550ms.
2-3	Power supply input stays OFF after a forward overcurrent fault. The external power supply should be switched OFF and ON to restore the board power.

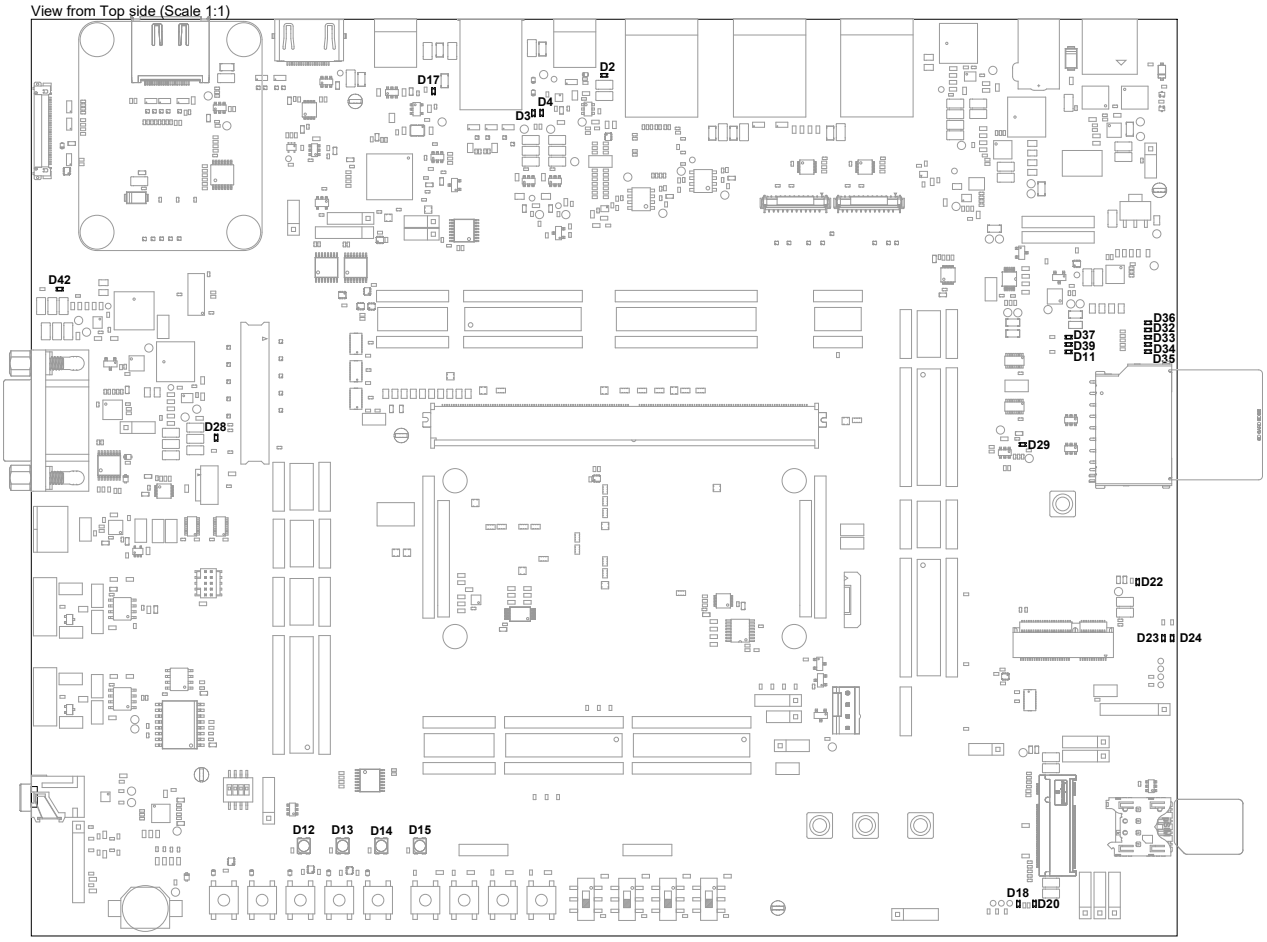
By default, jumper J88 is in position 1-2.

A current, voltage and power measurement IC INA226A (U66) is also available on SMARC Development Boards. This IC provides an option to measure the power consumption of SMARC modules. U66 is accessible on the I^2C_1 bus at address 0×40.

3.3 Indicator LEDs

The SMARC Development Board features 24 LEDs. These LEDs indicate the statuses of the main power supplies, all power gated peripherals. LEDs are also used for indicating the activity of some peripherals.

Figure 4: SMARC Development Board Indicator LEDs



The LEDs and their functions are listed in the table below.

Table 9: LEDs Functions

Designator	Color	Description
D2	Green	LED is lit when USB_0 port power is ON (Connector J6)
D3	Green	LED is lit when USB_3 Host power is ON (Connector J7 UPPER)
D4	Green	LED is lit when USB_2 Host power is ON (Connector J7 LOWER)
D11	Red	LED is lit when SoM and board is in a “RESET” state (RST_OUT# is LOW).
D12	Red/Green/Blue	User LED. It is lit when the LED_1 signal is High
D13	Red/Green/Blue	User LED. It is lit when the LED_2 signal is High
D14	Red/Green/Blue	User LED. It is lit when the LED_3 signal is High
D15	Red/Green/Blue	User LED. It is lit when the LED_4 signal is High
D17	Green	LED is lit when USB Debugger (J27) power is available - USB Debugger is connected to the PC
D18	Green	PCIe M.2 B-Key Rail
D20	Green	PCIe M.2 B-Key LED_1#

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Table 9: LEDs Functions (Continued)

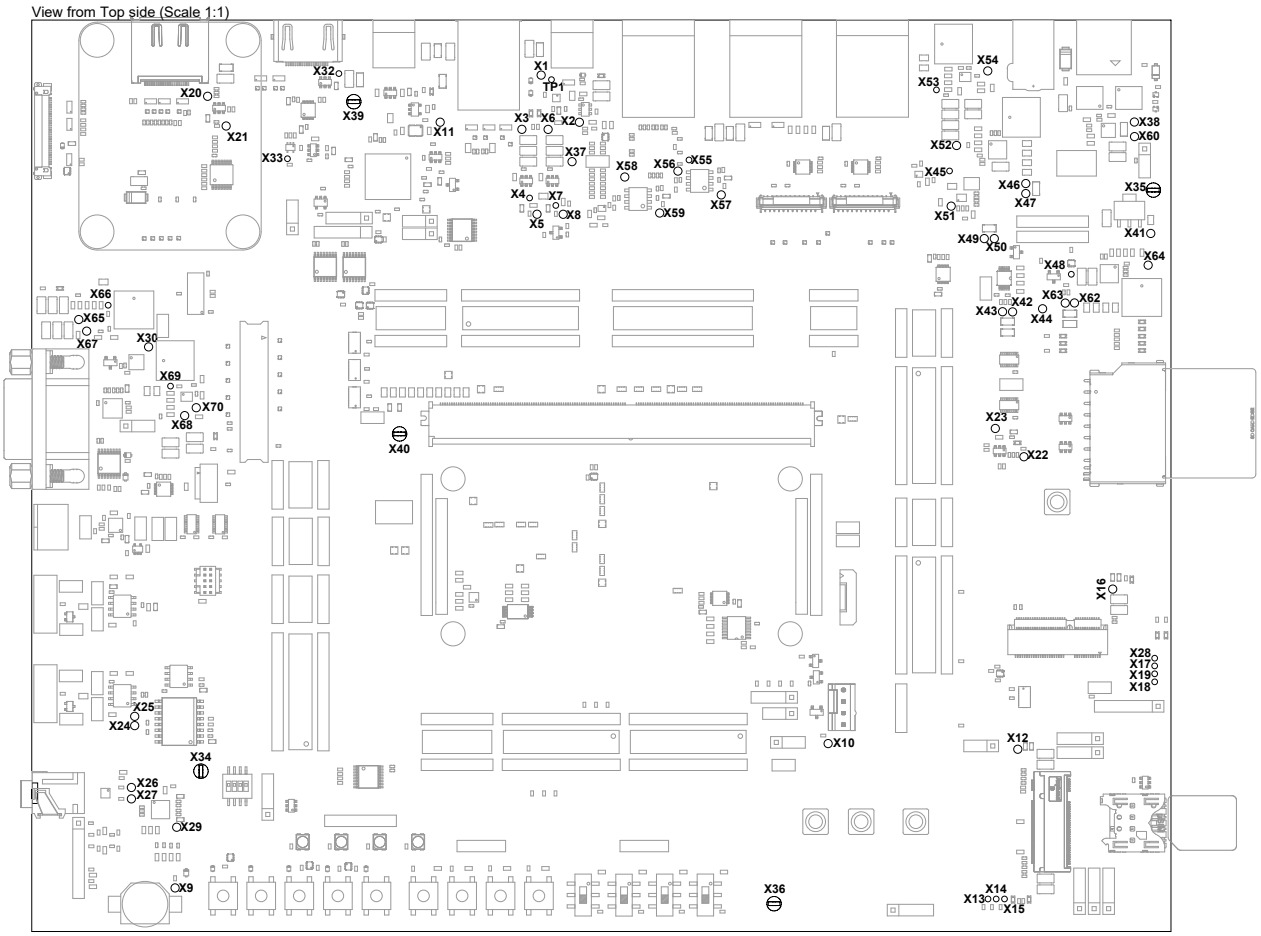
Designator	Color	Description
D22	Green	PCIe M.2 E-Key Rail
D23	Green	PCIe M.2 E-Key LED_1#
D24	Green	PCIe M.2 E-Key LED_2#
D28	Green	12V LVDS Backlight Boost Converter
D29	Green	LED is lit when SD Card power is ON
D32	Green	LED is lit when +5V power is available
D33	Green	LED is lit when +5V_SW power is available
D34	Green	LED is lit when +3V3 power is available
D35	Green	LED is lit when +1V8 power is available
D36	Green	12V Fan Boost Converter
D37	Green	Peripheral Power Enable
D39	Red	LED is lit when there is a Power Fault
D42	Green	12V eDP Backlight Boost Converter

More details are available in the SMARC Development Board Schematics.

3.4 Test Points

SMD and through-hole test points are available on the SMARC Development Board to allow customers to measure critical signals during the development and debugging process.

Figure 5: SMARC Development Board Test Points



The Test Points and their purposes are listed in the table below.

Table 10: Test Points

Designator	Description
TP1	SD Card Serial Data 0
TP2	SD Card Serial Data 1
TP3	SD Card Serial Data 2
TP4	SD Card Serial Data 3
TP5	SD Card Command Line
TP6	SD Card Serial Clock
TP7	SD Card Detection

Continued on next page

Table 10: Test Points (Continued)

Designator	Description
TP8	SD Card Write Protection Input
TP9	SoM Power Supply Voltage
TP10	Through-hole test point pin (GND)
TP11	
TP12	
TP13	
TP14	
TP15	
TP16	
TP17	
TP18	
TP19	
TP20	
TP21	SoM power supply current sensing resistor (High side)
TP22	SoM power supply current sensing resistor (Low side)
TP23	SD Card power supply
TP24	Open Drain “ALERT” output of the temperature sensing IC50
TP25	RLIN/GPIO3 pin of the Audio Codec IC28
TP26	Open Drain “VCONN_FAULT” output of the IC53 pulled up to +V1.8_SW with 100k resistor
TP27	Open Drain “OUT2” output of the IC53 for the current mode detection logic
TP28	Open Drain “OUT1” output of the IC53 for the current mode detection logic
TP29	Open Drain “DIR” output of the IC53 for the USB-C plug orientation indication
TP30	CSB/GPIO1 pin of the Audio Codec IC28
TP31	CDBUS2 pin of the universal USB converter IC41 (USB Debugger 3.3V RTS output)
TP32	CDBUS3 pin of the universal USB converter IC41 (USB Debugger 3.3V CTS input)
TP33	DDBUS2 pin of the universal USB converter IC41 (USB Debugger 3.3V RTS output)
TP34	DDBUS3 pin of the universal USB converter IC41 (USB Debugger 3.3V CTS input)
TP35	HDMI eARC differential line positive signal
TP36	HDMI eARC differential line negative signal
TP37	Ethernet_2 transceiver interrupt output. It can be used as a regular GPIO if R332 is removed
TP38	Ethernet_2 transceiver MDIO data signal. It can be used as a regular GPIO if R150 is removed
TP39	Ethernet_2 transceiver MDIO clock signal. It can be used as a regular GPIO if R147 is removed

3.5 Ethernet Interface

The SMARC Development Board provides three RJ45 connectors with integrated magnetics for 10/100/1000 Mb Ethernet. The Ethernet_0 and Ethernet_1 transceivers are located on the SoM while the Ethernet_2 transceiver is placed on the SMARC Development Board.

3.5.1 Ethernet_0 Connector (J41)

Connector Type: RJ45, Pulse JXD0-0025NL

Table 11: Ethernet_0 Connector (J41)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
1	GND		PWR		
2	GBE0_MDI3_N	P19	I/O		Media Dependent Interface
3	GBE0_MDI3_P	P20	I/O		Media Dependent Interface
4	GBE0_MDI2_N	P23	I/O		Media Dependent Interface
5	GBE0_MDI2_P	P24	I/O		Media Dependent Interface
6	GBE0_MDI1_N	P26	I/O		Media Dependent Interface
7	GBE0_MDI1_P	P27	I/O		Media Dependent Interface
8	GBE0_MDI0_N	P29	I/O		Media Dependent Interface
9	GBE0_MDI0_P	P30	I/O		Media Dependent Interface
10	NC				Not connected
11	3V3		PWR	+3.3V	Power supply for the indication LEDs
12	GBE0_LINK_ACT#	P25			LED for indication Ethernet activity
13	3V3		PWR	+3.3V	Power supply for the indication LEDs
14	GBE0_LINK_MAX#	P22			LED for indication established Ethernet link
15	NC				Not connected
16	NC				Not connected
17	NC				Not connected
S1/S2	GND		PWR		

3.5.2 Ethernet_1 Connector (J43)

Connector Type: RJ45, Pulse JXD0-0025NL

Table 12: Ethernet_1 Connector (J43)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
1	GND		PWR		
2	GBE1_MDI3_N	S27	I/O		Media Dependent Interface
3	GBE1_MDI3_P	S26	I/O		Media Dependent Interface
4	GBE1_MDI2_N	S24	I/O		Media Dependent Interface
5	GBE1_MDI2_P	S23	I/O		Media Dependent Interface
6	GBE1_MDI1_N	S21	I/O		Media Dependent Interface
7	GBE1_MDI1_P	S20	I/O		Media Dependent Interface
8	GBE1_MDI0_N	S18	I/O		Media Dependent Interface
9	GBE1_MDI0_P	S17	I/O		Media Dependent Interface
10	NC				Not connected
11	3V3		PWR	+3.3V	Power supply for the indication LEDs

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Table 12: Ethernet_1 Connector (J43) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
12	GBE1_LINK_ACT#	S31			LED for indication Ethernet activity
13	3V3		PWR	+3.3V	Power supply for the indication LEDs
14	GBE1_LINK_MAX#	S22			LED for indication established Ethernet link
15	NC				Not connected
16	NC				Not connected
17	NC				Not connected
S1/S2	GND		PWR		

3.5.3 Ethernet_2 Connector (J85)

The Ethernet_2 interface is based on the DP83867IR 10/100/1000 Mbps Ethernet PHY which is using the ETH_2_RGMII interface of the module. For more information, refer to the Gigabit Ethernet Transceiver datasheet.

Connector Type: RJ45, Pulse JXD0-0025NL

Table 13: Ethernet_2 Connector (J85)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
1	GND		PWR		
2	ETH2_D3_N		I/O		Media Dependent Interface
3	ETH2_D3_P		I/O		Media Dependent Interface
4	ETH2_D2_N		I/O		Media Dependent Interface
5	ETH2_D2_P		I/O		Media Dependent Interface
6	ETH2_D1_N		I/O		Media Dependent Interface
7	ETH2_D1_P		I/O		Media Dependent Interface
8	ETH2_D0_N		I/O		Media Dependent Interface
9	ETH2_D0_P		I/O		Media Dependent Interface
10	NC				Not connected
11	3V3		PWR	+3.3V	Power supply for the indication LEDs
12	ETH2_LINK				LED for indication established Ethernet link
13	3V3		PWR	+3.3V	Power supply for the indication LEDs
14	ETH2_ACT				LED for indication Ethernet activity
15	NC				Not connected
16	NC				Not connected
17	NC				Not connected
S1/S2	GND		PWR		

3.6 PCIe Interface

The SMARC Development Board makes the standard PCIe interface on the SMARC SoMs available on two M.2 PCIe slots, with Key E and B socket types. It provides multiple connections and buses, such as listed below:

- PCI Express 1 lane (with SMBus)
- USB 2.0
- Indication LEDs for wireless network status
- Micro SIM card for cellular applications

3.6.1 M.2 Key B PCIe Connector (J34)

Connector Type: M.2 Key B PCIe Connector, Amphenol MDT420B01001

Table 14: M.2 Key B PCIe Connector (J34)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	M2_KEYB_CONFIG_3			+3.3V		
3	GND		PWR			
5	GND		PWR			
7	USB1_P	P65		+3.3V		Positive differential USB 2.0 data signal
9	USB1_N	P66		+3.3V		Negative differential USB 2.0 data signal
11	GND		PWR			
21	M2_KEYB_CONFIG_0			+3.3V		
23	M2_KEYB_GPIO_11			+1.8V		PCIe General-purpose
25	M2_KEYB_DPR					
27	GND		PWR			
29	KEY_B_RX_N	S88		+3.3V		Negative differential PCIe receive signal
31	KEY_B_RX_P	S87		+3.3V		Positive differential PCIe receive signal
33	GND		PWR			
35	KEY_B_TX_N	S91		+3.3V		Negative differential PCIe transmit signal
37	KEY_B_TX_P	S90		+3.3V		Positive differential PCIe transmit signal
39	GND		PWR			
41	PCIE_A_RX_P	P86		+3.3V		Positive differential PCIe transmit signal
43	PCIE_A_RX_N	P87		+3.3V		Negative differential PCIe transmit signal
45	GND		PWR			
47	PCIE_A_TX_N	P90		+3.3V		Negative differential PCIe transmit signal
49	PCIE_A_TX_P	P89		+3.3V		Positive differential PCIe transmit signal
51	GND		PWR			
53	PCIE_A_REFCK_N	P84		+3.3V		Negative differential PCIe reference clock signal
55	PCIE_A_REFCK_P	P83		+3.3V		Positive differential PCIe reference clock signal
59	M2_KEYB_ANTCTL0			+1.8V		
61	M2_KEYB_ANTCTL1			+1.8V		
63	M2_KEYB_ANTCTL2			+1.8V		
65	M2_KEYB_ANTCTL3			+1.8V		
67	RST_OUT#	\verify[?]		+1.8V		
69	M2_KEYB_CONFIG_1			+3.3V		

Continued on next page

Table 14: M.2 Key B PCIe Connector (J34) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
75	M2_KEYB_CONFIG_2			+3.3V		
2	M2B_3V3		PWR	+3.3V		+3.3V Power input
4	M2B_3V3		PWR	+3.3V		+3.3V Power input
6	M2_KEYB_POWER_OFF#			+3.3V	27k to +3.3V	
8	M2_KEYB_WDISABLE#			+3.3V	27k to +3.3V	PCIe Wireless interface disable
10	M2_KEYB_LED#			+3.3V		LED
20	M2_KEYB_GPIO_5			+1.8V		PCIe General-purpose
22	M2_KEYB_GPIO_6			+1.8V		PCIe General-purpose
24	M2_KEYB_GPIO_7			+1.8V		PCIe General-purpose
26	M2_KEYB_GPIO_10			+1.8V		PCIe General-purpose
28	M2_KEYB_GPIO_8			+1.8V		PCIe General-purpose
30	UIM_RST			+3.3V		Micro SIM Card Reset
32	UIM_CLK			+3.3V		Micro SIM Card Clock
34	UIM_DATA			+3.3V		Micro SIM Card Data
36	UIM_PWR			+3.3V		Micro SIM Card Power
38	GND		PWR			
40	M2_KEYB_SMB_CLK			+1.8V		PCIe SMBus Clock
42	M2_KEYB_SMB_DATA			+1.8V		PCIe SMBus Data
44	M2_KEYB_ALERT#			+1.8V		
46	M2_KEYB_GPIO_3			+1.8V		PCIe General-purpose
48	M2_KEYB_GPIO_4			+1.8V		PCIe General-purpose
50	PCIE_A_RST#	P75		+3.3V	100k to +3.3V	
52	PCIE_A_CKREQ#	P78		+3.3V	100k to +3.3V	
54	PCI_WAKE#_JMP			+3.3V	100k to +3.3V	
56	NC					Not connected
58	NC					Not connected
60	NC					Not connected
62	NC					Not connected
64	NC					Not connected
66	UIM_PWR			+3.3V		
68	NC					Not connected
70	M2B_3V3		PWR	+3.3V		+3.3V Power input
72	M2B_3V3		PWR	+3.3V		+3.3V Power input
74	M2B_3V3		PWR	+3.3V		+3.3V Power input

3.6.2 M.2 Key E PCIe Connector (J39)

Connector Type: M.2 Key E PCIe Connector, TE Connectivity 2199230-4

Table 15: M.2 Key E PCIe Connector (J39)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
3	USB4_P			+3.3V		Positive differential USB 2.0 data signal
5	USB4_N			+3.3V		Negative differential USB 2.0 data signal
7	GND		PWR			
9	M2E_SDIO_CLK	P36		+1.8V		PCIe SDIO Clock
11	M2E_SDIO_CMD	P34		+1.8V		PCIe SDIO Command
13	M2E_SDIO_D0	P39		+1.8V		PCIe SDIO Data 0
15	M2E_SDIO_D1	P40		+1.8V		PCIe SDIO Data 1
17	M2E_SDIO_D2	P41		+1.8V		PCIe SDIO Data 2
19	M2E_SDIO_D3	P42		+1.8V		PCIe SDIO Data 3
21	NC					Not connected
23	SDIO_RST#	P119		+1.8V		
33	GND		PWR			
35	KEY_E_TX_P	S90		+3.3V		Positive differential PCIe transmit signal
37	KEY_E_TX_N	S91		+3.3V		Negative differential PCIe transmit signal
39	GND		PWR			
41	KEY_E_RX_P	S87		+3.3V		Positive differential PCIe receive signal
43	KEY_E_RX_N	S88		+3.3V		Negative differential PCIe receive signal
45	GND		PWR			
47	PCIE_B_REFCK_P			+3.3V		Positive differential PCIe reference clock signal
49	PCIE_B_REFCK_N			+3.3V		Negative differential PCIe reference clock signal
51	GND		PWR			
53	PCIE_B_CKREQ#	P77		+3.3V	100k to +3.3V	
55	PCI_WAKE#_JMP	S146		+3.3V		Wake-up to SoM
57	GND		PWR			
59	NC					Not connected
61	NC					Not connected
63	GND		PWR			
65	NC					Not connected
67	NC					Not connected
69	GND		PWR			
71	NC					Not connected
73	NC					Not connected
75	GND		PWR			
2	M2_3V3		PWR	+3.3V		+3.3V Power input
4	M2_3V3		PWR	+3.3V		+3.3V Power input
6	LED_1#		PWR	+3.3V		LED
8	I2S2_CK	S53		+1.8V		

Continued on next page

Table 15: M.2 Key E PCIe Connector (J39) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
10	I2S2_LRCK	S50		+1.8V		
12	I2S2_SDIN	S52		+1.8V		
14	I2S2_SDOUT	S51		+1.8V		
16	LED_2#		PWR	+3.3V		LED
18	GND		PWR			
20	UART WAKE#		O			Connected to Test Point X28
22	SER0_M2E_RX			+1.8V		
32	SER0_M2E_TX			+1.8V		
34	SER0_M2E_CTS#			+1.8V	100k to +1.8V	
36	SER0_M2E_RTS#			+1.8V		
38	NC					Not connected
40	NC					Not connected
42	NC					Not connected
44	NC					Not connected
46	NC					Not connected
48	COEX_TXD					Connected to Test Point X17
50	NC					Not connected
52	PCIE_B_RST#	S76		+3.3V	100k to +3.3V	
54	M2_KEYE_WDISABLE2#			+3.3V		PCIe Wireless interface disable
56	M2_KEYE_WDISABLE1			+3.3V		PCIe Wireless interface disable
58	NC					Not connected
60	NC					Not connected
62	M2_KEYE_ALERT#			+3.3V		
64	NC					Not connected
66	M2_KEYE_PERST1#			+3.3V		
68	M2_KEYE_CLKREQ1#			+3.3V		
70	M2_KEYE_PEWAKE1#			+3.3V		
72	M2_3V3		PWR	+3.3V		+3.3V Power input
74	M2_3V3		PWR	+3.3V		+3.3V Power input

3.6.3 Micro SIM Card Holder (J35)

Connector Type: MICRO SIM, Molex 0787231001

Table 16: Micro SIM Card Holder (J35)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
C1	UIM_PWR	PWR	+3.3V		Micro SIM Card Power
C2	UIM_RST	I	+3.3V		Micro SIM Card Reset
C3	UIM_CLK	I	+3.3V		Micro SIM Card Clock

Continued on next page

Table 16: Micro SIM Card Holder (J35) (Continued)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
C4	NC				Not connected
C5	GND	PWR			
C6	NC				
C7	UIM_DATA	I/O	+3.3V		Micro SIM Card Data
C8	NC				Not connected
C9	GND	PWR			

3.7 USB

3.7.1 SMARC USB_1 Port

The SMARC Development Board integrates a USB-C connector (J6), connected to the SMARC USB_1 port (USB 2.0 interface only). This port is usually used in the Recovery Mode for loading new software onto the module and can work as a dual-role-port (DRP), which means Host or Device. This behaviour is similar to the On-The-Go (OTG) functionality, but the term USB OTG is only used in conjunction with the USB Micro-AB or the obsolete USB Mini-AB receptacle. ID pin is absent on the USB Type-C receptacle. The determination of Host or Device functionality is handled differently in Type-C using the configuration channel (CC) pins. The CC pins perform the same functions that the ID pin previously performed: they indicate the role of equipment as host, device, or both. The CC pins also detect if the connection is being made or if it is broken.

To handle all the operations required for the USB dual-role-port TUSB320LI chip has been used. It can function as an upstream-facing port (UFP), downstream-facing port (DFP), or a dual-role port (DRP) product based on a pin configuration. The device handles all aspects of the USB Type-C connection process (including the CC pins that mirror the micro-A/B ID pin behavior) to determine the port role. When connected as a peripheral (UFP), the TUSB320LI indicates the VBUS current provided by the attached host through the general-purpose input/output (GPIO) pins. When connected as a DFP, these devices advertise VBUS current to the attached peripheral. For the details, please check the TUSB320LI datasheet.

On the SMARC Development Board, this port is configured as a dual-role port (DRP) by default, and its output current is limited to 1A.

3.7.1.1 USB_1 Connector (J6)

Connector Type: USB-C, Amphenol 12401826E412A

Table 17: USB_1 Connector (J6)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
A1	GND		PWR		
A2	NC				Not connected
A3	NC				Not connected
A4	USB0_VBUS	P63	PWR	+5V	+5V USB power output
A5	USB0_CC1				Type-C configuration channel signal 1
A6	USB_OTG_P	P60	I/O		Positive differential USB 2.0 Signal
A7	USB_OTG_N	P61	I/O		Negative differential USB 2.0 Signal

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Table 17: USB_1 Connector (J6) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Description
A8	NC				Not connected
A9	USB0_VBUS	P63	PWR	+5V	+5V USB power output
A10	NC				Not connected
A11	NC				Not connected
A12	GND		PWR		
B1	GND		PWR		
B2	NC				Not connected
B3	NC				Not connected
B4	USB0_VBUS	P63	PWR	+5V	+5V USB power output
B5	USB0_CC2				Type-C configuration channel signal 2
B6	USB_OTG_P	P60	I/O		Positive differential USB 2.0 Signal
B7	USB_OTG_N	P61	I/O		Negative differential USB 2.0 Signal
B8	NC				Not connected
B9	USB0_VBUS	P63	PWR	+5V	+5V USB power output
B10	NC				Not connected
B11	NC				Not connected
B12	GND				
SH1/SH2	GND		PWR		
SH3/SH4	GND		PWR		

3.7.2 SMARC USB_3 Port

On the SMARC Development Board, USB Ports 2 and 3 are routed to a stacked USB 3.1 Type-A connector (J7). Maximum data rate for this connector is 10Gbit/s. For further information about the USB connector, please refer to its datasheet.

3.7.2.1 USB_3 Connector (J7)

Connector Type: Stacked USB 3.1 Type-A, Amphenol GSB4112312HR (Pins starting with U connect to the UPPER, pins starting with L connect to the LOWER port)

Table 18: USB_3 Connector (J7)

Pin	Signal name	I/O Type	Voltage	Description
U1	USBH1_3	PWR	+5V	+5V USB power output
U2	USB_3_N	I/O		Negative differential USB 2.0 signal
U3	USB_3_P	I/O		Positive differential USB 2.0 signal
U4	GND	PWR		
U5	USB_3_SSRX_N	I		Negative differential USB 3.x receive signal
U6	USB_3_SSRX_P	I		Positive differential USB 3.x receive signal
U7	GND	PWR		

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Table 18: USB_3 Connector (J7) (Continued)

Pin	Signal name	I/O Type	Voltage	Description
U8	USB_3_SSTX_N	O		Negative differential USB 3.x transmit signal
U9	USB_3_SSTX_P	O		Positive differential USB 3.x transmit signal
L1	USB2_5V	PWR	+5V	+5V USB power output
L2	USB_2_N	I/O		Negative differential USB 2.0 signal
L3	USB_2_P	I/O		Positive differential USB 2.0 signal
L4	GND	PWR		
L5	USB_2_SSRX_N	I		Negative differential USB 3.x receive signal
L6	USB_2_SSRX_P	I		Positive differential USB 3.x receive signal
L7	GND	PWR		
L8	USB_2_SSTX_N	O		Negative differential USB 3.x transmit signal
L9	USB_2_SSTX_P	O		Positive differential USB 3.x transmit signal
S1/S2	GND	PWR		
S3/S4	GND	PWR		

3.8 Boot Configuration

The SMARC Computer Module boot mode can be selected through the switches in SW1 (Section 3.8.1). The boot modes are mapped in Table 19.

Table 19: Boot Mode Selection

Boot 0	Boot 1	Boot 2	Mode
0	0	0	Boot from Carrier SATA
1	0	0	Boot from Carrier SD
0	1	0	Boot from Carrier eSPI
1	1	0	Boot from Carrier SPI
0	0	1	Boot from Module Device
1	0	1	Boot using Remote Boot
0	1	1	Boot from Module eMMC
1	1	1	Boot from Module SPI

Switch position: 1 = ON; 0 = OFF

3.8.1 Boot Mode DIP Switch (SW1)

Table 20: Boot Modes 4-Way DIP Switch

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	BOOT_SEL0#	P123	I/O	0V		Boot mode selection switch 0
2	BOOT_SEL1#	P124	I/O	0V		Boot mode selection switch 1
3	BOOT_SEL2#	P125	I/O	0V		Boot mode selection switch 2
4	NC					Not connected

3.9 Digital and Analog I/O

3.9.1 Communication Interface

3.9.1.1 CAN

The SMARC Development Board uses the Texas Instruments TCAN1044VDRQ1 CAN transceiver to implement two CAN FD interfaces, isolated and non-isolated, in conjunction with the two CAN interface on the SMARC module.

The CAN ports provide an isolated 5V power supply output with a load capacity of 126 mA for each port.

The CAN interfaces are available on connectors J52 and J57. Pin header-to-DSUB9 adapters can be used with J52, J57 connectors.

The jumpers J53, J54, J59, J60 provide hardware configuration for these interfaces:

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 21: Jumpers for CAN Interface

Jumper	Status	Function
J59, J60	CLOSED	CAN0 split terminated.
J53, J54	CLOSED	CAN1 split terminated.

By default, the jumpers J53, J54, J59, J60 are closed.

3.9.1.1.1 CAN0 Connector (J57)

Connector Type: 2×5 Pin Header Male, 2.54 mm pitch

Table 22: CAN0 Connector (J57)

Pin	Signal Name	I/O Type	Voltage	Description
1	NC			Not connected
2	GND Jumper	PWR		
3	CAN_0_L	I/O		
4	CAN_0_H	I/O		
5	GND	PWR		Connected through 120 Ohm
6	NC			Not connected
7	NC			
8	5V_CAN_A	PWR	+5V	
9	NC			Not connected
10	NC			

3.9.1.1.2 CAN1 Connector (J52)

Connector Type: 2×5 Pin Header Male, 2.54 mm pitch

Table 23: CAN1 Connector (J52)

Pin	Signal Name	I/O Type	Voltage	Description
1	NC			Not connected
2	GND Jumper	PWR		
3	CAN_1_L	I/O		
4	CAN_1_H	I/O		
5	GND_ISO1	PWR		Connected through 120 Ohm
6	NC			Not connected
7	NC			
8	5V_ISO1	PWR	+5V	
9	NC			Not connected
10	NC			

3.9.1.2 UART Interfaces

The SMARC Development Board features 4 UART interfaces that are connected to the following connectors:

- UART1 to the connector J9 through an RS485 transceiver.
- UART2 to the connector J14 through an RS232 transceiver.
- UART3 to a built-in USB to Serial transceiver (Primary debug log output for Cortex-A cores).
- UART4 to a built-in USB to Serial transceiver (Primary debug log output for Cortex-M core).

3.9.1.2.1 RS485 Connector (J9)

Connector Type: Screw Terminal Block

Manufacturer: Wurth Electronics

Part Number: 691137710002

Table 24: RS485 Connector (J9)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	S0_RS485_A	I/O			Digital bus I/O, A
2	S0_RS485_B	I/O			Digital bus I/O, B

Jumper J10 provide hardware configuration for this interface:

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 25: Jumper Position (J10)

Jumper Position	Description
1-2	Disable Driver Enable terminal (DE), A/B on high-impedance state

Continued on next page

Table 25: Jumper Position (J10) (Continued)

Jumper Position	Description
Disconnected	Driver enabled, receiver enabled (normal operation)

By default, the jumper J10 is closed.

3.9.1.2.2 RS232 Connector (J14)

Connector Type: D-Sub 9-pin Male

Manufacturer: Assmann WSW Components

Part Number: A-DS 09 A/KG-T2S

Table 26: RS232 Connector (J14)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC				Not connected
2	RS232_RX	I			RS232 Receive Data
3	RS232_TX	O			RS232 Transmit Data
4	NC				Not connected
5	GND	PWR			
6	NC				Not connected
7	NC				Not connected
8	NC				Not connected
9	NC				Not connected
10	GND	PWR			
11	GND	PWR			

By using the jumper J15, it is possible to configure the Auto Powerdown Plus function of the RS232 transceiver. The following table shows the J15 connection possibilities.

Connector Type: 1×3 Pin Header Male, 2.54 mm pitch

Table 27: Jumper Position (J15)

Jumper position	Description
1 - 2	Auto Powerdown Plus disabled
2 - 3	Auto Powerdown Plus enabled

By default, the jumper J15 is installed in position 1-2.

For detailed information about the Auto Powerdown Plus function, please refer to the TRS3122ERGER transceiver datasheet (FORCEON and FORCEOFF# pins functions).

3.10 Peripherals to SMARC Standard Interfaces

The SMARC Development Board features a variety of peripherals that communicate with the SoM via the SMARC Standard Interfaces. The peripherals available and their functions are listed in the table below.

Table 28: Top Side Connectors

Peripheral	Part Number	SMARC Interface	Remarks
Ethernet	N/A	GBE0, GBE1	
Ethernet 2	DP83867	SERDES_0	Address 0x04, autoneg, 2ns RX clock skew
Display Port / Embedded Display Port	N/A	DP0	DP0 muxed between DP and eDP connectors
DSI Mezzanine / LVDS1/DSI1	N/A	LVDS1/DSI1	LVDS1/DSI1 muxed between DSI mezzanine and LVDS connectors
CSI1	N/A	CSI0	
CSI2	N/A	CSI1	
USB-C DRP	N/A	USB0	
Audio	WM8904	I2S0/I2C_GP	I2C Address: 0x1A
EEPROM	M24C02-FDW6TP	I2C_GP	I2C Address: 0x57
Temperature Sensor	TMP1075DSGR	I2C_GP	I2C Address: 0x4F
USB 3.0 Type A	N/A	USB2	
USB 3.0 Type A	N/A	USB3	
M.2 B-Key	N/A	PCIE_A, USB1, PCIE_B	PCIE_B muxed between M.2 B-Key and M.2 E-Key
M.2 E-Key	N/A	PCIE_B, I2S2, SER0, SDIO	PCIE_B muxed between M.2 B-Key and M.2 E-Key; SDIO muxed between M.2 E-Key and SD card connector
SD Card	N/A	SDIO	
RS232	TRS3122ERGER	SER3	
RS485	SN65HVD01DRCR	SER0	
JTAG	N/A	JTAG	
Isolated CAN	ISO6721FBDR, TCAN1044VDRQ1	CAN1	
Non-isolated CAN	TCAN1044VDRQ1	CAN0	
HDMI	HDMI		
Fan	AMC6821SDBQR	I2C_PM	I2C Address: 0x18

3.11 MUX Modes

There are a few interfaces on the SMARC Development Board that are multiplexed such that multiple peripherals can be accessed through a single interface, allowing for more functionality and flexibility in the evaluation process. The multiplexing mode can be selected by connecting/disconnecting the interface-related jumper.

3.11.1 LVDS/DSI MUX

The LVDS1 interface on SMARC Development Board allows for software configuration of LVDS or DSI interfacing. The LVDS1 interface on the SMARC Development Board can be switched between the DSI

Mezzanine connector (J44) and the LVDS connector (J48) through the jumper header J95.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 29: Jumper Position (J95)

Jumper Position	Description
1-2	Select DSI Mezzanine
Disconnected	Select LVDS Connector

3.11.2 PCIe MUX

The PCIE_B interface on the SMARC Development Board can be switched between the M.2 B-Key connector (J34) and the M.2 E-Key connector (J39) through the jumper header J98.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 30: Jumper Position (J98)

Jumper Position	Description
1-2	Select M.2 B-Key
Disconnected	Select M.2 E-Key

3.11.3 DisplayPort MUX

The DP0 interface on the SMARC Development Board can be switched between the DisplayPort connector (J47) and the Embedded DisplayPort (eDP) connector (J116) through the jumper header J120.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 31: Jumper Position (J120)

Jumper Position	Description
1-2	Select DisplayPort
Disconnected	Select Embedded DisplayPort (eDP)

3.11.4 SDIO MUX

The SDIO interface on the SMARC Development Board can be switched between the SD Card connector (J35) and the M.2 E-Key connector (J39) through the jumper header J112.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 32: Jumper Position (J112)

Jumper Position	Description
1-2	Select SD Card
Disconnected	Select M.2 E-Key

3.12 Temperature Sensor

The SMARC Development Board provides the Digital Temperature Sensor feature (U15) with an I²C interface. The sensor is connected to the general-purpose I2C_1 bus. The default I²C address of the sensor is 0×4F. For details, please check the TMP1075DSGR sensor datasheet.

3.13 EEPROM

A 2-Kbit EEPROM (U16) with an I²C interface is installed on the SMARC Development Board to store important data or for board identification purposes.B The EEPROM is accessible at the address 0×57 on the general-purpose I2C_1 bus.

By design, the EEPROM's "Write Control" (WC) pin is driven "Low". Therefore, write operations are enabled.

For the EEPROM technical details, please check the M24C02-FDW6TP datasheet.

3.14 Backup Battery

A backup battery holder (XB1) is available on the SMARC Development Board to provide backup power to the RTC of a SMARC module when the main power is turned off.

For more details on how the backup voltage is used, please refer to the respective SMARC computer-on-module datasheet.

3.14.1 Battery Holder (XB1)

A 10 mm (diameter) coin cell/battery should be used with the Battery Holder (XB1). A coin-cell battery can be used to provide power backup to the SMARC module RTC circuit when an external power supply is not available. Supported batteries: CR1025 or CR1016 coin-cell batteries.

Connector Type: Keystone Electronics 3030TR

Table 33: Battery Holder (XB1)

Pin	Voltage	Description
1	+3.0V	+VDD_RTC
2		GND

3.15 JTAG

The SMARC Development Board provides a JTAG port to the JTAG interface available on SMARC modules. Connector J117 provides an interface to an external JTAG device via a Cortex Debug Connector, which is a 2×5-pin 1.27mm header. The SMARC Development Board also has an on-board JTAG debugger feature. Please check the USB Debugger section of this datasheet and the SMARC Development Board schematic file for detailed information. This document is available on the Toradex Developer Website, on the Development Board Design page.

3.15.1 JTAG Breakout

The SMARC standard does not allow for JTAG connections to be brought to the edge connector to be used on the carrier board. Hence, the SMARC Development Board provides two alternatives to route the JTAG signals from the SMARC SoM, as described below.

3.15.1.1 JTAG Pogo Pins (J5)

The SMARC Development Board features Pogo pin connectors that are associated with contact pads routed to the SMARC SoM JTAG interface.

3.15.1.2 JTAG FPC Connector (J114)

On both the SMARC Development Board and SMARC SoM, there are matching FPC connectors that can be used with a same-side flat cable to break out the JTAG interface from the SoM to the Development Board.

3.15.1.3 JTAG Breakout Selector (J115)

The JTAG interface breakout method on the SMARC Development Board can be switched between the Pogo pins and the FPC Connector through jumper header J115.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 34: Jumper Position (J115)

Jumper Position	Description
1-2	Select FPC Connector
Disconnected	Select Pogo Pins

3.15.2 JTAG Access

The SMARC Development Board provides two alternatives to access the JTAG interface, as described below.

3.15.2.1 FTDI JTAG (J27)

The JTAG interface can be accessed through the FTDI FT4232HL Port 2, available on USB-C debug connector (J27).

3.15.2.2 External JTAG Connector (J117)

The JTAG interface can be accessed through the External JTAG connector (J117).

Connector Type: 2×5 Pin Shrouded Header Male, 1.27mm

Manufacturer: Samtec Inc.

Part Number: FTSH-105-01-L-DV-007-K

Table 35: JTAG Connector (J117)

Pin	Signal Name	JTAG FPC Pin	JTAG POGO Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	VDD_JTAG			PWR	+1.8V		1.8V reference output for JTAG adapter
2	TMS	8	5	I	+1.8V		Test Mode Select
3	GND			PWR			

Continued on next page

Table 35: JTAG Connector (J117) (Continued)

Pin	Signal Name	JTAG FPC Pin	JTAG POGO Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
4	TCK	5	3	I	+1.8V	Pull-down on SoM	Test Clock
5	GND			PWR			
6	TDO	7	2	O	+1.8V		Test Data Out
7	NC						Not connected
8	TDI	6	1	I	+1.8V		Test Data In
9	NC						Not connected
10	RESET_OUT#	9	4	I (OD)	+1.8V		Reset

3.15.2.3 JTAG Access Selector (J126)

The JTAG access method on the SMARC Development Board can be switched between the FTDI JTAG and External JTAG connector through jumper header J126.

Connector Type: 1×2 Pin Header Male, 2.54 mm pitch

Table 36: Jumper Position (J126)

Jumper Position	Description
1-2	Select External JTAG Connector
Disconnected	Select FTDI JTAG

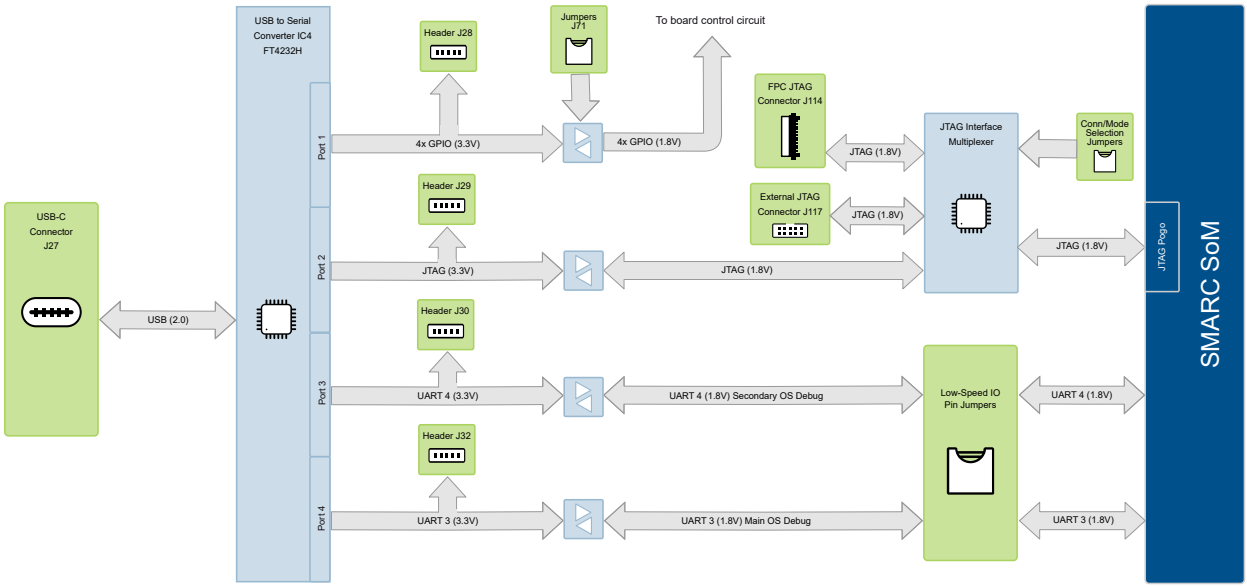
3.16 USB Debugger - FTDI

The SMARC Development Board provides an on-board Universal USB Debugger (U24). The debugger is based on the FT4232HL chip and provides the following features:

- 2x UART ports connected to SMARC Module Cortex-A and Cortex-M core debug outputs
- JTAG Debugger/Programmer
- 4x GPIO used for performing basic Development Board control features: Power ON/OFF, Reset etc.

Simplified USB Debugger architecture is shown below.

Figure 6: SMARC Development Board USB Debugger Architecture



The pin assignments of the FT4232HL are shown in the table below.

Table 37: FT4232HL pin assignments

Pin	Pin Name	I/O Type	Interface	Connected/Controlled Net	Description
21	ADBUS4	I/O	GPIO	CARRIER_PWR_ON_FTDI#	SMARC Development Board POWER ON/OFF
22	ADBUS5	I/O		RESET_IN_FTDI#	SMARC Module RESET
23	ADBUS6	I/O		POWER_BTN_FTDI#	SMARC Development Board POWER ON/OFF
24	ADBUS7	I/O		FORCE_RECOV_FTDI#	SMARC Module RECOVERY mode
26	ACBUS0	I/O	JTAG	TCK	JTAG Test Mode Select
27	ACBUS1	I/O		TDI	JTAG Test Data Input
28	ACBUS2	I/O		TDO	JTAG Test Data Output
29	ACBUS3	I/O		TMS	JTAG Test Mode Select
30	ACBUS4	I/O		TRST#	JTAG Test Mode Reset
38	BDBUS0	I/O	UART	CONSOLE_ALT_RX	Receiver Data of Cortex-M debug UART
39	BDBUS1	I/O		CONSOLE_ALT_TX	Transmitter Data of Cortex-M debug UART
48	BCBUS0	I/O		CONSOLE_RX	Receiver Data of Cortex-M debug UART
52	BCBUS1	I/O		CONSOLE_TX	Transmitter Data of Cortex-A debug UART

The debug interface is accessible via the separate USB-C connector J27.

3.16.1 USB Debugger Connector (J27)

Connector Type: USB 3.1 Connector (Type C)

Manufacturer: Amphenol

Part Number: 12401826E412A

Table 38: USB Debugger Connector (J27)

Pin	Signal Name	I/O Type	Voltage	Pull-up/Pull-down	Description
A4	+FT_3V3	PWR	+5V		FTDI debugger power supply input
A9	+FT_3V3	PWR	+5V		
B4	+FT_3V3	PWR	+5V		
B9	+FT_3V3	PWR	+5V		
A6	FTDI_DEBUG_P	I/O			Positive Differential USB 2.0 Signal
A7	FTDI_DEBUG_N	I/O			Negative Differential USB 2.0 Signal
B6	FTDI_DEBUG_P	I/O			Positive Differential USB 2.0 Signal
B7	FTDI_DEBUG_N	I/O			Negative Differential USB 2.0 Signal
A2	NC				Not Connected
A3	NC				
A10	NC				
A11	NC				
B2	NC				
B3	NC				
B10	NC				
B11	NC				Not Connected
A5	USB_DBG_CC1			Pull-down to GND (5.1kΩ)	Type-C configuration channel signal 1
B5	USB_DBG_CC2			Pull-down to GND (5.1kΩ)	Type-C configuration channel signal 2
A8	NC				Not Connected
B8	NC				
A1	GND	PWR			
A12	GND	PWR			
B1	GND	PWR			
B12	GND	PWR			
SH1/SH2	GND_CHASSIS				
SH3/SH4	GND_CHASSIS				

3.16.1.1 FTDI GPIO Power Selector (J71)

The FTDI GPIO Power Supply Source pins on the SMARC Development Board are connected via the J71 pin header. For details, please refer to the jumper header J71 pinout.

Connector type: 1×2 Pin Header Male, 2.54 mm pitch

Table 39: Jumper Position (J71)

Jumper Position	Description
1-2	Use +1.8V supplied from the USB-C connector
2-3	Use +1.8V supplied from the Carrier Board

3.17 SD Card Interface

The SMARC Development Board has a 4-bit SDIO interface and a hardware-supported card detection function (CD). If the SD card itself supports the Low Voltage Signalling mode, then communication will start at 3.3V and switch to 1.8V after the card has been initialized. The SD_PWR_EN signal allows to power ON and OFF SD the Card power supply (+V3.3_SD).

3.17.1 SD Card 4-bit Connector (J50)

Connector Type: SD Card, Same Sky SD-4-B

Table 40: SD Card 4-bit Connector (J50)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	SD_SDIO_D3		I/O	+1.8/3.3V	Pull-up on a SoM	Serial Data 3
2	SD_SDIO_CMD		I/O	+1.8/3.3V	Pull-up on a SoM	Command
3	GND		PWR			
4	3V3_SD		PWR	+3.3V		SD Card power input
5	SD_SDIO_CLK		O	+1.8/3.3V	Pull-up on a SoM	Serial Clock
6	GND		PWR			
7	SD_SDIO_D0		I/O	+1.8/3.3V	Pull-up on a SoM	Serial Data 0
8	SD_SDIO_D1		I/O	+1.8/3.3V	Pull-up on a SoM	Serial Data 1
9	SD_SDIO_D2		I/O	+1.8/3.3V	Pull-up on a SoM	Serial Data 2
10	SD_SDIO_CD#		I	+1.8/3.3V	Pull-up on a SoM	Card Detect
11	SD_SDIO_WP		I	+1.8/3.3V	Pull-up on a SoM	Write Protection
12	GND		PWR			

3.18 Display Interface

The SMARC Development Board provides five options for connecting LCD panels and monitors via the following supported interfaces:

- HDMI
- DisplayPort
- Embedded DisplayPort (eDP)
- MIPI DSI
- LVDS

Almost any TFT display can be connected to the SMARC module by HDMI port J64 or via the DSI interface connector J44. J44 features a universal mezzanine board connector. This solution allows for connecting various types of display interface mezzanine boards and converters, e.g., DSI to HDMI, DSI to LVDS, DSI to RGB, etc. Custom boards with the appropriate MIPI DSI connector can also be used.

3.18.1 HDMI Connector (J64)

Connector Type: HDMI Connector Right Angle

Manufacturer: Amphenol

Part Number: 10029449-111RLF

Table 41: HDMI Connector (J64)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	HDMI1_CON_D2_P	92	O			HDMI/DVI differential data lane 2, positive
2	GND		PWR			
3	HDMI1_CON_D2_N	93	O			HDMI/DVI differential data lane 2, negative
4	HDMI1_CON_D1_P	95	O			HDMI/DVI differential data lane 1, positive
5	GND		PWR			
6	HDMI1_CON_D1_N	96	O			HDMI/DVI differential data lane 1, negative
7	HDMI1_CON_D0_P	98	O			HDMI/DVI differential data lane 0, positive
8	GND		PWR			
9	HDMI1_CON_D0_N	99	O			HDMI/DVI differential data lane 0, negative
10	HDMI1_CON_CLK_P	101	O			HDMI/DVI differential clock positive
11	GND		PWR			
12	HDMI1_CON_CLK_N	102	O			HDMI/DVI differential clock negative
13	NC					Not connected
14	NC					Not connected
15	I2C_HDMI_CK	105	O	+5V	Pull-up to 4.7k to +5V_HDMI	DDC Interface Clock
16	I2C_HDMI_SDA	106	I/O	+5V	Pull-up to 4.7k to +5V_HDMI	DDC Interface Data
17	GND		PWR			
18	+5V_HDMI		PWR	+5V		HDMI power out
19	HDMI_HPD	104	I	+5V		Hot Plug Detect
MTG1	GND		PWR			
MTG2	GND		PWR			
MTG3	GND		PWR			
MTG4	GND		PWR			

3.18.2 DisplayPort Connector (J47)

Connector Type: DisplayPort Receptacle Connector 20 Position Surface Mount, Right Angle

Manufacturer: Molex

Part Number: 0472720001

Table 42: DisplayPort Connector (J47)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	DP_CON_LANE0_P	93	I/O	3.3V		DisplayPort Lane 0 Positive
2	GND		PWR	0V		
3	DP_CON_LANE0_N	94	I/O	3.3V		DisplayPort Lane 0 Negative
4	DP_CON_LANE1_P	96	I/O	3.3V		DisplayPort Lane 1 Positive
5	GND		PWR	0V		

Continued on next page

Table 42: DisplayPort Connector (J47) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
6	DP_CON_LANE1_N	97	I/O	3.3V		DisplayPort Lane 1 Negative
7	DP_CON_LANE2_P	99	I/O	3.3V		DisplayPort Lane 2 Positive
8	GND		PWR	0V		
9	DP_CON_LANE2_N	100	I/O	3.3V		DisplayPort Lane 2 Negative
10	DP_CON_LANE3_P	102	I/O	3.3V		DisplayPort Lane 3 Positive
11	GND		PWR	0V		
12	DP_CON_LANE3_N	103	I/O	3.3V		DisplayPort Lane 3 Negative
13	DP0_AUX_SEL	95	I/O	3.3V	Pull-down to GND (1MΩ)	DisplayPort AUX Channel Selector
14	GND		PWR	0V	Pull-down to GND (100KΩ)	
15	DP_CON_AUX_P	105	I/O	3.3V	Pull-down to GND (100KΩ)	DisplayPort AUX Channel Positive
16	GND		PWR	0V		
17	DP_CON_AUX_N	106	I/O	3.3V	Pull-up to 3V3 (100KΩ)	DisplayPort AUX Channel Negative
18	DP0_MUX_HPD	98	I/O	3.3V	Pull-down to GND (100KΩ)	Hot Plug Detect
19	GND		PWR	0V	Grounded with 0Ω resistor	
20	DP_3V3		PWR	3.3V		Power for DP

3.18.3 Embedded DisplayPort (eDP) Connector (J116)

Connector Type: Receptacle Connector 30 Position Surface Mount, Right Angle

Manufacturer: I-PEX

Part Number: 20455-030E-76

Table 43: Embedded eDP (eDP) Connector (J116)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC					Not Connected
2	GND		PWR	0V		
3	eDP_CONN_1_N	97	I/O	3.3V		eDP Lane 1 Negative
4	eDP_CONN_1_P	96	I/O	3.3V		eDP Lane 1 Positive
5	GND		PWR	0V		
6	eDP_CONN_0_N	94	I/O	3.3V		eDP Lane 0 Negative
7	eDP_CONN_0_P	93	I/O	3.3V		eDP Lane 0 Positive
8	GND		PWR	0V		
9	eDP_CONN_AUX_P	105	I/O	3.3V		eDP AUX Channel Positive
10	eDP_CONN_AUX_N	106	I/O	3.3V		eDP AUX Channel Negative
11	GND		PWR	0V		
12	+LCD_VCC		PWR	3.3V		Power for LCD
13	+LCD_VCC		PWR	3.3V		

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Table 43: Embedded eDP (eDP) Connector (J116) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
14	NC					Not Connected
15	GND		PWR	0V		
16	GND		PWR	0V		
17	eDP_MUX_HPD	98	I/O	3.3V		eDP Hot Plug Detect
18	GND		PWR	0V		
19	GND		PWR	0V		
20	GND		PWR	0V		
21	GND		PWR	0V		
22	eDP_CTRL_EN	117	I/O	3.3V		eDP Control Enable
23	eDP_CTRL_PWM	113	I/O	3.3V		eDP Control PWM
24	NC					Not Connected
25	NC					
26	eDP_BL_PWR		PWR	3.3V		eDP Backlight Power
27	eDP_BL_PWR		PWR	3.3V		
28	eDP_BL_PWR		PWR	3.3V		
29	eDP_BL_PWR		PWR	3.3V		
30	NC					Not Connected

3.18.4 DSI Display Adapter Connector (J44)

Connector Type: Connector Header 10 Position Surface Mount

Manufacturer: Samtec

Part Number: LSS-130-03-L-DV-A-K-TR

Table 44: DSI Display Adapter Connector (J44)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	NC					Not connected
2	NC					
3	GND		PWR			
4	I2C_DSI_SDA	140	I/O	+1.8V	1.8k to +1V8	Generic I^2C bus Data
5	NC					Not connected
6	I2C_DSI_SCL	139	I/O	+1.8V	1.8k to +1V8	Generic I^2C bus Clock
7	+VIN_DSI		PWR	7-24V ±10%		7-24V power supply output
8	DSI_INT#	116	I/O	+1.8V		Dedicated general-purpose I/O for the DSI display adapters
9	+VIN_DSI		PWR	7-24V ±10%		7-24V power supply output
10	GND		PWR			

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Table 44: DSI Display Adapter Connector (J44) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
11	+VIN_DSI		PWR	7-24V ±10%		7-24V power supply output
12	DSI_D0_P	111	I/O			DSI Interface differential data lane 0, positive
13	+VIN_DSI		PWR	7-24V ±10%		7-24V power supply output
14	DSI_D0_N	112	I/O			DSI Interface differential data lane 0, negative
15	+VIN_DSI		PWR	7-24V ±10%		7-24V power supply output
16	GND		PWR			
17	NC					Not connected
18	DSI_D1_P	114	I/O			DSI interface differential data lane 1, positive
19	+5V_S		PWR	+5V		+5V power supply output
20	DSI_D1_N	115	I/O			DSI interface differential data lane 1, negative
21	+5V_S		PWR	+5V		+5V power supply output
22	GND		PWR			
23	+5V_S		PWR	+5V		+5V power supply output
24	DSI_CLK_P	108	I/O			DSI interface differential clock, positive
25	+5V_S		PWR	+5V		+5V power supply output
26	DSI_CLK_N	109	I/O			DSI interface differential clock, negative
27	+5V_S		PWR	+5V		+5V power supply output
28	GND		PWR			
29	NC					Not connected
30	DSI_D2_P	117	I/O			DSI interface differential data lane 2, positive
31	+3V3		PWR	+3.3V		+3.3V power supply output
32	DSI_D2_N	118	I/O			DSI interface differential data lane 2, negative
33	+3V3		PWR	+3.3V		+3.3V power supply output
34	GND		PWR			
35	+3V3		PWR	+3.3V		+3.3V power supply output
36	DSI_D3_P	120	I/O			DSI Interface differential data lane 3, positive
37	+3V3		PWR	+3.3V		+3.3V power supply output
38	DSI_D3_N	121	I/O			DSI Interface differential data lane 3, negative
39	+3V3		PWR	+3.3V		+3.3V power supply output
40	GND		PWR			
41	NC					Not connected
42	NC					
43	+1V8		PWR	+1.8V		+1.8V power supply output
44	NC					Not connected
45	+1V8		PWR	+1.8V		+1.8V power supply output
46	NC					Not connected
47	+1V8		PWR	+1.8V		+1.8V power supply output
48	NC					Not connected

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Table 44: DSI Display Adapter Connector (J44) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
49	+1V8		PWR	+1.8V		+1.8V power supply output
50	GND		PWR			
51	+1V8		PWR	+1.8V		+1.8V power supply output
52	I2C_DDC_SCL	139	I/O	+1.8V	1.8k to +1V8	DSI adapters DDC Clock
53	NC					Not connected
54	I2C_DDC_SDA	140	I/O	+1.8V	1.8k to +1V8	DSI adapters DDC Data
55	GND		PWR			
56	DSI_BKLT_EN_JMP	107	I/O	+1.8V		Dedicated general-purpose I/O for DSI display adapters
57	RESET_OUT#	126	I/O	+1.8V	10k to +3V3	Board peripheral RESET
58	DSI_BKLT_PWM_JMP	122	I/O	+1.8V		DSI Display adapters PWM brightness control
59	CARRIER_PWR_ON	154	I/O	+1.8V		DSI Adapter power enable
60	GND		PWR			

3.18.5 LVDS Connector (J48)

Connector Type: Connector Header 40 position Through Hole, Right Angle

Manufacturer: Hirose

Part Number: DF13E-40DP-1.25V(52)

Table 45: LVDS Connector (J48)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	LVDS_A_TX3_P	137	I/O	3.3V		LVDS interface differential data lane 3, positive
2	GND		PWR			
3	LVDS_A_TX3_N	138	I/O	3.3V		LVDS interface differential data lane 3, negative
4	LVDS_B_CLK_N	109	I/O	3.3V		LVDS interface differential clock, negative
5	GND		PWR			
6	LVDS_B_CLK_P	108	I/O	3.3V		LVDS interface differential clock, positive
7	LVDS_A_TX2_P	131	I/O	3.3V		LVDS interface differential data lane 2, positive
8	GND		PWR			
9	LVDS_A_TX2_N	132	I/O	3.3V		LVDS interface differential data lane 2, negative
10	LVDS_B_TX0_N	112	I/O	3.3V		LVDS interface differential data lane 0, negative
11	GND		PWR			
12	LVDS_B_TX0_P	111	I/O	3.3V		LVDS interface differential data lane 0, positive
13	LVDS_A_TX1_P	128	I/O	3.3V		LVDS interface differential data lane 1, positive
14	GND		PWR			
15	LVDS_A_TX1_N	129	I/O	3.3V		LVDS interface differential data lane 1, negative

Continued on next page

Table 45: LVDS Connector (J48) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
16	LVDS_B_TX1_N	115	I/O	3.3V		LVDS interface differential data lane 1, negative
17	GND		PWR			
18	LVDS_B_TX1_P	114	I/O	3.3V		LVDS interface differential data lane 1, positive
19	LVDS_A_TX0_P	125	I/O	3.3V		LVDS interface differential data lane 0, positive
20	GND		PWR			
21	LVDS_A_TX0_N	126	I/O	3.3V		LVDS interface differential data lane 0, negative
22	LVDS_B_TX2_N	118	I/O	3.3V		LVDS interface differential data lane 2, negative
23	GND		PWR			
24	LVDS_B_TX2_P	117	I/O	3.3V		LVDS interface differential data lane 2, positive
25	LVDS_A_CLK_P	134	I/O	3.3V		LVDS interface differential clock, positive
26	GND		PWR			
27	LVDS_A_CLK_N	135	I/O	3.3V		LVDS interface differential clock, negative
28	LVDS_B_TX3_N	121	I/O	3.3V		LVDS interface differential data lane 3, negative
29	GND		PWR			
30	LVDS_B_TX3_P	120	I/O	3.3V		LVDS interface differential data lane 3, positive
31	LVDS_TOUCH_INT#_3V	114	I/O		Pull-up to 3.3V (100kΩ)	
32	+3V3		PWR			+3.3V power supply output
33	LVDS_RST#_3V	112	I/O	3.3V		LVDS interface reset
34	+5V_S		PWR			+5V power supply output
35	LVDS_BKLT_PWM_3V	141	I/O	3.3V		LVDS interface backlight PWM control
36	I2C_LVDS_3V3_SDA	140	I/O		Pull-up to 3.3V (4.7kΩ)	
37	LVDS_BKLT_EN_3V	127	I/O	3.3V		LVDS interface backlight enable
38	I2C_LVDS_3V3_SCL	139	I/O		Pull-up to 3.3V (4.7kΩ)	
39	LVDS_BL_PWR		I/O	3.3V		LVDS interface backlight power
40	LVDS_BL_PWR		I/O	3.3V		LVDS interface backlight power

3.19 Audio

The SMARC Development Board offers two audio interfaces: an analog audio interface and a digital audio interface.

3.19.1 Analog Audio

The analog audio interface is based on the WM8904CGEFL/RV audio codec IC from Cirrus Logic. The analog audio interface is available on the connector J63 which is a standard 3.5mm stereo connector for AUX OUT, HEADPHONE OUT, AUX IN, and MIC IN. The WM8904CGEFL/RV audio codec IC also contains a speaker driver, and its output is available on the header J13.

3.19.1.1 3.5mm Stereo Audio Jack (J63)

Connector Type: 3.5mm Jack, Same Sky SJ-43515TS

Table 46: 3.5mm Stereo Audio Jack (J63)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	HP_MICIN_CONN	PWR			Microphone input
2	HP_LEFT_CONN	O (Analog)			Auxiliary output 2 / Line out Left
3	HP_RIGHT_CONN	O (Analog)			Auxiliary output 1 / Line out Right
4	HP_FB	PWR			Auxiliary feedback path
5	HP_LEFT_CONN	O (Analog)			Auxiliary output 2 / Line out Left

3.19.1.2 SPEAKER OUT 7-pin Header (J13)

Connector Type: 1×7 Pin Header Male, 2.54 mm pitch

Table 47: SPEAKER OUT 7-pin Header (J13)

Pin	Signal name	I/O Type	Voltage	Pull-up/Pull-down	Description
1	1V8	PWR			
2	AAP_LIN_CONN_L	O (Analog)			Left speaker input
3	AAP_LIN_CONN_R	O (Analog)			Right speaker input
4	GND	PWR			
5	AAP_LOUT_CONN_L	O (Analog)			Left speaker output
6	AAP_LOUT_CONN_R	O (Analog)			Right speaker output
7	GND	PWR			

3.20 MIPI CSI Camera Interface

The MIPI CSI Camera Interface on connectors J45, J56 is intended for applications requiring image capture capability from CMOS or CDD image sensors. For details, please see the relevant SMARC module datasheet.

3.20.1 MIPI CSI0 Camera Connector (J45)

Connector Type: 24 Position FFC, FPC, vertical 0.5mm

Manufacturer: Hirose

Part Number: FH12-24S-0.5SVA(54)

Table 48: MIPI CSI0 Camera Connector (J45)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_C0_D0_N	S12	I/O			CSI0 differential data lane 0, negative
3	CSI_C0_D0_P	S11	I/O			CSI0 differential data lane 0, positive
4	GND		PWR			
5	CSI_C0_D1_N	S15	I			CSI0 differential data lane 1, negative

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Table 48: MIPI CSI0 Camera Connector (J45) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
6	CSI_C0_D1_P	S14	I			CSI0 differential data lane 1, positive
7	GND		PWR			
8	CSI_C0_CLK_N	S9	I			CSI0 differential clock, negative
9	CSI_C0_CLK_P	S8	I			CSI0 differential clock, positive
10	GND		PWR			
11	CAM_0_CON_RST	P110	O			Camera RESET
12	CAM0_MCK	S6	O			CSI0 Camera Master Clock
13	CSI0_SCL	S5	O	+3.3V	Pull-up to 3.3V (4.7kΩ)	CSI0 Camera I^2C bus Clock
14	CSI0_SDA	S7	I/O	+3.3V	Pull-up to 3.3V (4.7kΩ)	CSI0 Camera I^2C bus Data
15	+3V3		PWR	+3.3V		+3.3V power output
16	NC					Not connected
17	NC					Not connected
18	GND		PWR			
19	NC					Not connected
20	NC					Not connected
21	+5V_S		PWR	+5V		+5V power output
22	NC					Not connected
23	NC					Not connected
24	CAM_0_CON_PWRCTRL	P108	O	+3.3V		Power Supply Control

3.20.2 MIPI CSI1 Camera Connector (J46)

Connector Type: 24 Position FFC, FPC, vertical 0.5mm

Manufacturer: Hirose

Part Number: FH12-24S-0.5SVA(54)

Table 49: MIPI CSI1 Camera Connector (J46)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
1	GND		PWR			
2	CSI_C1_D0_N	P8	I/O			CSI1 differential data lane 0, negative
3	CSI_C1_D0_P	P7	I/O			CSI1 differential data lane 0, positive
4	GND		PWR			
5	CSI_C1_D1_N	P11	I			CSI1 differential data lane 1, negative
6	CSI_C1_D1_P	P10	I			CSI1 differential data lane 1, positive
7	GND		PWR			
8	CSI_C1_CLK_N	P4	I			CSI1 differential clock, negative
9	CSI_C1_CLK_P	P3	I			CSI1 differential clock, positive
10	GND		PWR			

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Table 49: MIPI CSI1 Camera Connector (J46) (Continued)

Pin	Signal name	SODIMM Pin	I/O Type	Voltage	Pull-up/Pull-down	Description
11	CAM_1_CON_RST	P111	O			Camera RESET
12	CAM1_MCK	S6	O			CSI1 Camera Master Clock
13	CSI1_SCL	S1	O	+3.3V	Pull-up to 3.3V (4.7kΩ)	CSI1 Camera I^2C bus Clock
14	CSI1_SDA	S2	I/O	+3.3V	Pull-up to 3.3V (4.7kΩ)	CSI1 Camera I^2C bus Data
15	+3V3		PWR	+3.3V		+3.3V power output
16	CSI_C1_D2_N	P14	I			CSI1 differential data lane 2, negative
17	CSI_C1_D2_P	P13	I			CSI1 differential data lane 2, positive
18	GND		PWR			
19	CSI_C1_D3_N	P17	I			CSI1 differential data lane 3, negative
20	CSI_C1_D3_P	P16	I			CSI1 differential data lane 3, positive
21	+5V_S		PWR	+5V		+5V power output
22	NC					Not connected
23	NC					Not connected
24	CAM_1_CON_PWRCTRL	P109	O	+3.3V		Power Supply Control

4 Operating Conditions

4.1 Operating Temperature Range

Operating temperature range: 0°C to 70°C

5 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Minerals, REACH, etc. can be found on our website at http://www.toradex.com/support/product-compliance.

6 Device and Documentation Legal Information

6.1 Trademarks

DisplayPort™ is a registered trademark of project VESA.

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