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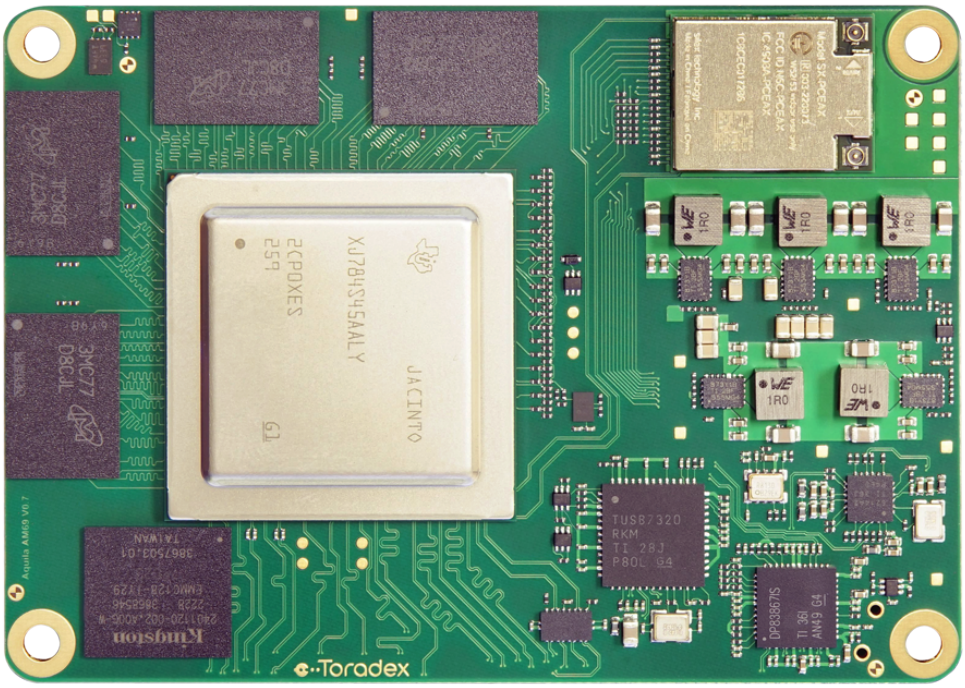
Aquila AM69/TDA4

HW Errata



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
28-Nov-2024	Rev. 0.1	V1.0	Initial documentation Section 1: Added HAR-11637 Section 2: Added HAR-11135 Section 3: Added HAR-10963
18-Jun-2025	Rev. 0.2	V1.0	Section 4: Added HAR-10972 Section 5: Added HAR-12387
15-Jan-2026	Rev. 0.3	V1.1	Section 2: Fixed typo in 'Fixed in' field for HAR-11135 Section 5: Updated 'Fixed in' field for HAR-12387
09-Mar-2026	Rev. 0.4	V1.0, V1.1	Update product name to Aquila AM69/TDA4 to reflect the updated hardware.
25-Mar-2026	Rev. 0.5	V1.0, V1.1	Section 6: added Section 7: added

Contents

1 Errata #1: HAR-11637 – The 25MHz clock jitter is too high to pass the Ethernet Compliance

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69/TDA4 V1.1

1.1 Customer Impact

The onboard Ethernet interface currently does not meet Ethernet compliance due to high jitter from the 25MHz clock. This issue will be resolved in the next module revision.

1.2 Description

The Ethernet interface on the module uses the 25MHz clock directly from the SoC. The jitter introduced by the clock is too high to pass Ethernet Compliance.

1.3 Workaround

There is no identified workaround.

2 Errata #2: HAR-11135 – USB_2_EN signal needs to be inverted (by default it's active low output from the bridge)

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69 V1.0

2.1 Customer Impact

Customers cannot use the USB_2 interface with BSP 6-based software, including the Toradex Easy Installer. The interface functions properly with operating systems based on BSP 7

2.2 Description

The USB_2_EN# pin is designed to be active low but is currently active high. In the current revision, this requires an additional transistor or inverter on the carrier board. A software fix addressing this issue has been implemented in BSP 7.

2.3 Workaround

Use VNC (Virtual Network Computing) to access Toradex Easy installer and install an operating system based on BSP 7.

3 Errata #3: HAR-10963 – The series capacitors are missing on the USB_2_SS_TX lines

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69/TDA4 V1.1

3.1 Customer Impact

The USB_2 interface lacks serial capacitors on the USB_2_SS_TX lines. This does not affect usage with the Aquila Development Board V1.2, as it includes the necessary capacitors. However, when designing custom carrier boards for the AM69 V1.0 revision, customers must account for this limitation by adding serial capacitors. The next module revision will address this issue.

3.2 Description

The USB_2_SS_TX lines lack the required 100nF serial capacitors. The Aquila Development Board V1.2 addresses this by replacing the R461 and R462 resistors with capacitors. Customers should account for this limitation when designing custom carrier boards for the AM69 V1.0 revision.

3.3 Workaround

When designing custom carrier boards for the AM69 V1.0 revision, customers must include 100nF serial capacitors on the USB_2_SS_TX lines. These capacitors can later be replaced with 0R resistors to ensure compatibility with future AM69/TDA4 module revisions.

4 Errata #4: HAR-10972 – VBUS input is not 5V tolerant

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69/TDA4 V1.1

4.1 Customer Impact

Customers should implement voltage divider on the carrier board to make USB_1 compatible with 5V on carrier boards compatible with Aquila AM69 V1.0.

4.2 Description

The VBUS input - USB_1_VBUS - is only compatible with 3.3V. It requires a voltage divider to be 5V tolerant.

4.3 Workaround

Add a voltage divider on the carrier board for the USB_1_VBUS signal.

5 Errata #5: HAR-12387 – The (V1.0A) module does not comply with the Aquila Family Specification concerning the CTRL_RESET_MICO# signal

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69/TDA4 V1.1

5.1 Customer Impact

The Aquila AM69 (V1.0A) module does not properly comply with the CTRL_RESET_MICO# signal as defined in the Aquila Family Specification. As a result, carrier boards cannot reliably extend the reset period of the module, which may lead to undesired or premature boot behavior in some system designs.

5.2 Description

Due to a deviation from the specification, the module exits reset and begins the boot sequence immediately after the falling edge of CTRL_RESET_MICO#, instead of remaining in reset while the signal stays low. This prevents proper synchronization of reset timing between the module and the carrier board.

5.3 Workaround

There is no identified workaround.

6 Errata #6: HAR-13508 – The AM69/TDA4 X1 connector might be affected by a minor bowing issue

Affected version:

Aquila AM69/TDA4 V1.1A

Fixed in:

not scheduled

6.1 Customer Impact

None. The observed bending does not impact the functionality or electrical performance of the module. All shipped units have successfully passed the standard production functional test.

6.2 Description

A slight bending of the X1 connector relative to the PCB surface may be present on some modules. This condition is related to the current SMT assembly process. Process improvements are currently being implemented on the production line to further optimize the connector coplanarity during assembly.

6.3 Workaround

No action is required from the user. The modules can be used as intended.

7 Errata #7: HAR-11843 – USB_2_OC# is not in line with the Aquila family Specs

Affected version:

Aquila AM69 V1.0

Fixed in:

Aquila AM69/TDA4 V1.1

7.1 Customer Impact

No functionality impact is expected from this issue. USB_x_OC# and USB_x_EN signal level (3.3V) is not in line with the Family specification (1.8V).

7.2 Description

The USB_x_OC# and USB_x_EN signals of the USB bridge are operating at 3.3V instead of the 1.8V level defined in the module family specification.
This deviation does not affect the functionality of the USB interface in typical use cases. However, designs expecting strict 1.8V logic levels on these signals should take this into account.
The issue was fixed in the V1.1 board revision.

7.3 Workaround

If your design depends on 1.8V logic levels for USB_x_OC# or USB_x_EN, consider the following options: (1) Use a level shifter to translate the 3.3V signals to 1.8V or (2) if the signal is not used, it can be left unconnected or pulled up to 3.3V using a resistor (e.g., 10kΩ), depending on your design requirements.

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