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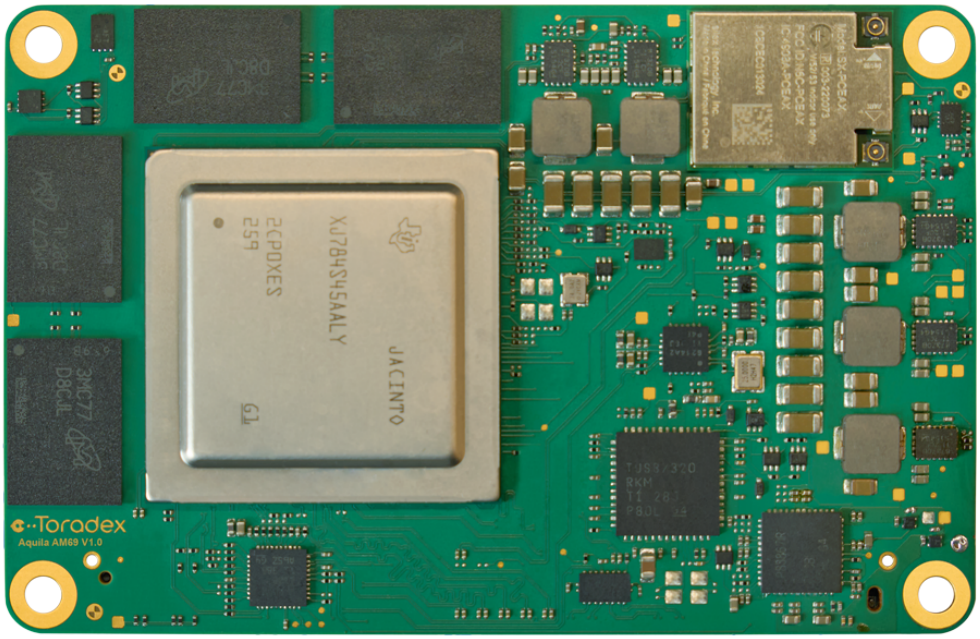
Aquila AM69/TDA4

Datasheet

Preliminary – Subject to Change



Revision History

Document Revisions

Date	Doc. Revision	Product Version	Changes
24-Jun-2024	Rev. 0.1	V1.0	Initial documentation
15-Aug-2025	Rev. 0.2	V1.1	Section 2: Updated block diagram on Figure 1 Section 3: Updated pin assignments on Table 3, Table 4 and Table 5 on Section 3.1 Section 4: Updated alternate functions tables on Section 4.1.1 Minor fixes.
13-Mar-2026	Rev. 0.3	V1.1	Update document layout following the new standard template Update product name to Aquila AM69/TDA4 to reflect the updated hardware Section 1.8: Added GPU information on Table 2 Section 3.1: Updated primary function names for pins A19 on Table 3 and C26 on Table 4 Section 4: Removed duplicate Abbreviations table Section 5: Added interfaces section Section 6: Added test points section Minor fixes.
20-Mar-2026	Rev. 0.4	V1.1	Section 1.3: Updated link to TDA4VH SoC page on TI website Section 1.8: Updated CPU name to TDA4VH on Table 2
31-Mar-2026	Rev. 0.5	V1.1	Section 2.1: Added legend to block diagram in Figure 1

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Abbreviations

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Abbreviation	Explanation
ADC	Analog to Digital Converter
BTB	Board To Board
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant.
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GND_CHASSIS	Chassis Ground
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GSM	Global System for Mobile Communications
HDA	High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec
I2C	Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals
I2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
I/O	Input-Output
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.

Continued on next page

Abbreviations (Continued)

Abbreviation	Explanation
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
NC	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	The physical layer of the OSI model
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
PWR	Power
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGMII	Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	The single-ended serial port interface
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used in x86 designs for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SoM	System on a Module, PCB which integrates the main component of a computer on a single board
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals

1 Introduction

1.1 Purpose of the Datasheet

The datasheet represents the hardware capabilities of the Aquila AM69/TDA4. For information on the actual features supported by software, please refer to the relevant SoM product page on the Toradex Developer website:

https://developer.toradex.com/hardware/aquila-som-family/modules/aquila-am69

1.2 Aquila SoM Family

The Aquila System on Module (SoM) family targets modern applications dealing with computationally intensive, demanding workloads. Aquila modules differentiate themselves from other SoMs with their increased CPU, GPU, NPU, and ISP performance, a modern, rich, future-proof feature set, provided on a board-to-board physical interface featuring approx. 400 pins, for state of the art robustness and reliability. Industrial temperature range support, high quality, and exceptional value for the price make Aquila SoMs a compelling choice for high-performance edge computing, Industrial IoT, edge AI, computer/machine vision, and real-time processing/control applications.

1.3 TI AM69/TDA4 SoC

https://www.ti.com/product/AM69A

https://www.ti.com/product/TDA4VH-Q1

1.4 Aquila AM69/TDA4 SoM

The Aquila AM69/TDA4 targets a wide variety of applications, including high-performance edge computing, Artificial Intelligence (AI), Machine Learning (ML), image processing, computer and machine vision, automated and autonomous vehicles and robots, smart gateways, real-time processing and control, and many more.

The SoM is available with an optional Wi-Fi and Bluetooth interface.

The module offers a wide range of interfaces ranging from simple GPIOs, industry-standard I2C, SPI, USB, CAN FD, and UART buses to MIPI-CSI camera interfaces. An optional MIPI-DSI display interface is available on all SoM configurations. The Aquila AM69/TDA4 module features a Gigabit Ethernet PHY with IEEE 1588 support on the module. The SoC features a 8-port Serial Ethernet with an SGMII interface, of which 5 are available on the Aquila AM69/TDA4 SoM.

1.5 Interface Overview

Features of the Aquila module are split into three distinct categories: “Always Compatible”, “Reserved”, and “Module-specific”. The “Always Compatible” and “Reserved” pins are also referred to as the “Aquila Standard” pins.

“Always Compatible” interfaces are features that shall be present on each SoM in the Aquila Family. Customers can count on upgradeability and maximum scalability regarding these interfaces.

“Reserved” interfaces are features that are defined and reserved but possibly missing on some SoM models due to lack of availability. It could be that a particular SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any Aquila SoM can be reliably inserted into any Aquila carrier board without causing damage due to incompatible “Reserved” pins.

A “Module-specific” feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Aquila module family do not provide these features and instead provide other features on the associated pins. In this case, Aquila modules that are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM or the carrier board. The use of these pins could make upgrades impossible.

Additionally to this definition, the AM69/TDA4 SoC allows for “Alternate Functions”. As an example, many pins can, apart from their primary function, also work as GPIOs. The “Alternate Functions” group means that an interface is provided as an additional function on an “Always Compatible”, “Reserved”, or “Module-specific” pin. These functions can only be used if the primary function of the pin is not used.

Table 1 shows the interfaces that are supported on the Aquila AM69/TDA4 module along with the group in which that feature is provided: “Always Compatible”, “Reserved”, “Module-specific”, or alternate function.

Table 1: Connector Aquila AM69/TDA4

Feature	Total	"Always Compatible"	"Reserved"	"Module-specific"	"Alternate Function"
USB 2.0 DRD	1x	1x			
USB 2.0 Host	1x	1x			
Gigabit Ethernet	1x	1x			
SGMII (for additional Ethernet interfaces)	5x		1x[1]	4x	
PCIe (Gen3)	3x	1x (x2)[2]	1x (x2)	1x (x1)	
SDIO/SD/MMC	1x	1x			
I2C	8x	1x	4x		2x
I2C/I3C	1x	1x			
SPI	7x	1x	1x		5x
QSPI	1x		1x		
OSPI	1x		1x[3]		
UART	11x	3[4]	1x		7x
PWM	12x	2x	2x		8x
GPIO	110x	8x	13x		89x
JTAG	1x	1x			
USB-C 3.x (2x SuperSpeed + AUX)	1x		1x[5]		
USB-C 3.x (1x SuperSpeed)	1x		1x[6]		
MIPI DSI (quad lane)	2x		1x	1x	
DisplayPort	1x		1x		
MIPI CSI-2(quad lane)	3x		2x	1x	
I2S	5x		1x		4x
CAN FD	19x		4x		15x
ADC	8x		4x	4x	

[1] Usable in USXGMII mode at 10G speed as well
[2] x1 in the “Always Compatible”, complemented to x2 with an optional additional lane in the “Reserved” class
[3] Complementing the QSPI instance in the “Reserved” class to OSPI
[4] 2x instances complemented by optional flow control pins in the “Reserved” class
[5] Complementing the USB 2.0 DRD instance in the “Always Compatible” class
[6] Complementing the USB 2.0 Host instance in the “Always Compatible” class

1.6 Reference Documents

1.6.1 Aquila Carrier Board Design Guide

A custom carrier board should follow the Aquila Carrier Board Design Guide to make the board compatible with the Aquila module family. Please study this document in detail before starting your carrier board design.

https://docs.toradex.com/116803-aquila_carrier_board_design_guide.pdf

1.6.2 Aquila Family Specification

This document outlines the specification which defines the Aquila Computer-on-Module family. It describes the interfaces in terms of functional and electrical characteristics, signal definitions, and pin assignments. It also defines other specifications to consider when integrating the Aquila System-on-Module into your product, such as power consumption, mechanical form factor, and key dimensions.

https://docs.toradex.com/116801-aquila_family_specification.pdf

1.6.3 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.

https://docs.toradex.com/115265-layout_design_guide.pdf

1.6.4 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there.

Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Aquila AM69/TDA4.

http://www.developer.toradex.com

1.6.5 Aquila Carrier Board Schematics

We provide complete schematics plus an Altium project file which includes library symbols and footprints for the Aquila Development Board, as well as other carrier boards, free of charge. This resource is of great help when designing your own carrier board.

https://developer.toradex.com/carrier-board-design/reference-designs/#aquila-family

1.6.6 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, Colibri, and Aquila Modules. The tool allows comparing the interfaces across different modules.

http://developer.toradex.com/knowledge-base/pinout-designer

1.7 Naming Convention

Missing Content
More information about naming convention will be available on the next release of the datasheet.

1.8 Concept Configurations

Table 2 provides information about different **conceptual configurations** for the Aquila AM69/TDA4. This means that these configurations are **not yet committed to launch**, but we intend to provide our customers with the most valuable selection of configurations.

Table 2: Product Configurations

	Octa 32GB WB IT	Octa 32GB ET	Octa 16GB WB IT	Octa 16GB ET	Octa 8GB WB IT	Octa 8GB CT
CPU Details						
CPU Name	TI AM69A98/ TDA4VH	TI AM69A98/ TDA4VH	TI AM69A98/ TDA4VH	TI AM69A98/ TDA4VH	TI AM69A98/ TDA4VH	TI AM69A58/ TDA4VH
CPU Type	8x Arm® Cortex®-A72	8x Arm® Cortex®-A72	8x Arm® Cortex®-A72	8x Arm® Cortex®-A72	8x Arm® Cortex®-A72	8x Arm® Cortex®-A72
Microcontroller	2x Arm® Cortex®-R5F	2x Arm® Cortex®-R5F	2x Arm® Cortex®-R5F	2x Arm® Cortex®-R5F	2x Arm® Cortex®-R5F	2x Arm® Cortex®-R5F
CPU Clock (A72)	2.0 GHz	2.0 GHz	2.0 GHz	2.0 GHz	2.0 GHz	2.0 GHz
CPU Clock (R5F)	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz	1.0 GHz
Security (HSM)	Yes	Yes	Yes	Yes	Yes	Yes
L1 Instruction Cache	A72: 32KB	A72: 32KB	A72: 32KB	A72: 32KB	A72: 32KB	A72: 32KB
L1 Data Cache	A72: 48KB	A72: 48KB	A72: 48KB	A72: 48KB	A72: 48KB	A72: 48KB
L2 Cache	A72: 2MB	A72: 2MB	A72: 2MB	A72: 2MB	A72: 2MB	A72: 2MB
GPU Details						
GPU	Yes	Yes	Yes	Yes	Yes	Yes
2D Acceleration	Yes	Yes	Yes	Yes	Yes	Yes
3D Acceleration	Yes	Yes	Yes	Yes	Yes	Yes
GPU Model	BXS-4-64	BXS-4-64	BXS-4-64	BXS-4-64	BXS-4-64	BXS-4-64
OpenGL ES	3.1	3.1	3.1	3.1	3.1	3.1
Vulkan	1.2	1.2	1.2	1.2	1.2	1.2
Memory						
RAM (LPDDR4 with inline ECC)	32GB (128bit)	32GB (128bit)	16GB (128bit)	16GB (128bit)	8GB (128bit)	8GB (128bit)
Flash (eMMC)	128GB	128GB	64GB	64GB	32GB	32GB
Connectivity						
Wi-Fi	Wi-Fi 6	-	Wi-Fi 6	-	Wi-Fi 6	-
Bluetooth	Bluetooth 5.2	-	Bluetooth 5.2	-	Bluetooth 5.2	-
Other IPs and Peripherals						
3D Graphics Accelerator	Yes	Yes	Yes	Yes	Yes	Yes
Deep Learning Accelerator	4x	4x	4x	4x	4x	-
Vision Processing Accelerator	2x	2x	2x	2x	2x	-
Video Encoder/Decoder	2x	2x	2x	2x	2x	2x
Security Accelerator	Yes	Yes	Yes	Yes	Yes	Yes

Continued on next page

Table 2: Product Configurations (Continued)

	Octa 32GB WB IT	Octa 32GB ET	Octa 16GB WB IT	Octa 16GB ET	Octa 8GB WB IT	Octa 8GB CT
Trusted Platform Module	Yes	Yes	Yes	Yes	Yes	Yes
Eletrical						
Input voltage	5V ±10%					
IO voltage level	1.8V					
Thermal Design Power (TDP)	< 25W	< 25W	< 25W	< 25W	< 25W	< 15W
Mechanical						
Dimensions	85mm x 55mm x 9mm					
Shock and vibration resistance	Yes					
Environmental						
Operating temperature range	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C	-25°C to 85°C	-40°C to 85°C	0°C to 70°C

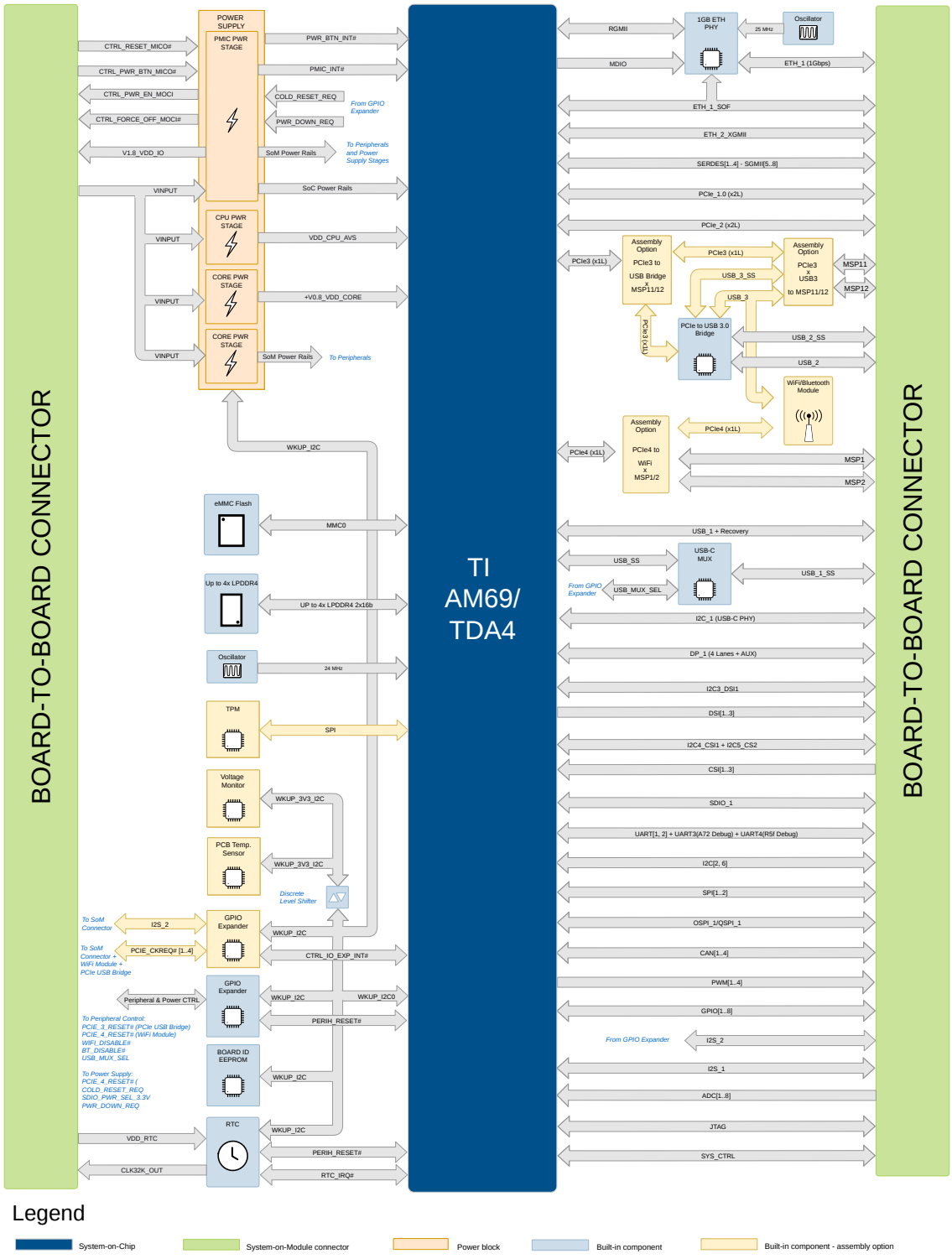
1.9 Configure-To-Order (CTO) Options

Missing Content
More information about CTO options will be available on the next release of the datasheet.

2 Architecture Overview

2.1 Block Diagram

Figure 1: Block Diagram



3 Aquila AM69/TDA4 Connector

Connector type: Samtec APF6-100-03.5-L-04-0-A-x (mating part for carrier boards: APM6-100-01.5-L-04-0-A-x)

The connector is available in Toradex Webshop.

https://www.toradex.com/accessories/aquila-carrier-board-connector

3.1 Pin Assignment

The following tables describe the Board-to-Board connector pinout.

- X1 Pin: pin number on the Board-to-Board connector.
- Aquila Pin Name: the name of the signal according to the Aquila form factor definition.
- Primary: this name corresponds to the default usage of the pin. Some of the pins also have an alternate function.

Table 3: Pin Map Column A and Column B

Column A				Column B			
X1 Pin	Aquila Pin Name	Primary	Remarks	X1 Pin	Aquila Pin Name	Primary	Remarks
A1	SD_1_CD#	TIMER_IO0		B1	GND		
A2	SD_1_D1	MMC1_DAT1		B2	CSI_2_D3_P	CSI1_RXP3	
A3	SD_1_D0	MMC1_DAT0		B3	CSI_2_D3_N	CSI1_RXN3	
A4	GND			B4	GND		
A5	SD_1_CLK	MMC1_CLK		B5	CSI_2_D2_P	CSI1_RXP2	
A6	SD_1_PWR_EN	SPI0_CS1		B6	CSI_2_D2_N	CSI1_RXN2	
A7	SD_1_CMD	MMC1_CMD		B7	GND		
A8	SD_1_D3	MMC1_DAT3		B8	CSI_2_CLK_P	CSI1_RXCLKP	
A9	GND			B9	CSI_2_CLK_N	CSI1_RXCLKN	
A10	SD_1_D2	MMC1_DAT2		B10	GND		
A11	GPIO_11_CSI_1	MCASP1_AFSX		B11	CSI_2_D1_P	CSI1_RXP1	
A12	I2C_4_CSI1_SDA	MCAN16_TX		B12	CSI_2_D1_N	CSI1_RXN1	
A13	I2C_4_CSI1_SCL	MCAN15_RX		B13	GND		
A14	CTRL_MCLK_MOCI	WKUP0_GPIO_11		B14	CSI_2_D0_P	CSI1_RXP0	
A15	GND			B15	CSI_2_D0_N	CSI1_RXN0	
A16	CSI_1_D3_P	CSI0_RXP3		B16	GND		
A17	CSI_1_D3_N	CSI0_RXN3		B17	GPIO_09_CSI_1	MCAN12_TX	
A18	GND			B18	GPIO_10_CSI_1	MCAN12_RX	
A19	CSI_1_D2_P	CSI0_RXP2		B19	GPIO_12_CSI_1	MCASP1_AXR0	
A20	CSI_1_D2_N	CSI0_RXN2		B20	I2S_1_BCLK	EXT_REFCLK1	
A21	GND			B21	I2S_1_SYNC	MCAN1_TX	
A22	CSI_1_CLK_P	CSI0_RXCLKP		B22	I2S_1_D_OUT	MCAN0_RX	
A23	CSI_1_CLK_N	CSI0_RXCLKN		B23	I2S_1_D_IN	ECAP0_IN_APWM_OUT	

Continued on next page

Table 3: Pin Map Column A and Column B (Continued)

Column A				Column B			
X1 Pin	Aquila Pin Name	Primary	Remarks	X1 Pin	Aquila Pin Name	Primary	Remarks
A24	GND			B24	I2S_1_MCLK	MCAN2_RX	
A25	CSI_1_D1_P	CSI0_RXP1		B25	GND		
A26	CSI_1_D1_N	CSI0_RXN1		B26	I2S_2_BCLK	GPIO Expander	
A27	GND			B27	I2S_2_SYNC	GPIO Expander	
A28	CSI_1_D0_P	CSI0_RXP0		B28	I2S_2_D_OUT	GPIO Expander	
A29	CSI_1_D0_N	CSI0_RXN0		B29	I2S_2_D_IN	GPIO Expander	
A30	GND			B30	GND		
A31	DSI_1_D3_N	DSI0_TXN3		B31	UART_2_RXD	WKUP_UART0_RXD	
A32	DSI_1_D3_P	DSI0_TXP3		B32	UART_2_CTS	WKUP_GPIO0_6	
A33	GND			B33	UART_2_TXD	WKUP_UART0_TXD	
A34	DSI_1_D2_N	DSI0_TXN2		B34	UART_2_RTS	WKUP_GPIO0_7	
A35	DSI_1_D2_P	DSI0_TXP2		B35	UART_1_RXD	MCASP0_AXR7	
A36	GND			B36	UART_1_CTS	MCASP0_AXR9	
A37	DSI_1_CLK_N	DSI0_TXCLKN		B37	UART_1_TXD	MCASP0_AXR8	
A38	DSI_1_CLK_P	DSI0_TXCLKP		B38	UART_1_RTS	MCASP0_AXR10	
A39	GND			B39	GND		
A40	DSI_1_D1_N	DSI0_TXN1		B40	I2C_3_DSI1_SDA	I2C0_SDA	
A41	DSI_1_D1_P	DSI0_TXP1		B41	I2C_3_DSI1_SCL	I2C0_SCL	
A42	GND			B42	GPIO_17_DSI_1	GPIO0_12	
A43	DSI_1_D0_N	DSI0_TXN0		B43	GPIO_18_DSI_1	MCASP0_AXR3	
A44	DSI_1_D0_P	DSI0_TXP0		B44	GPIO_19_DSI_1	PMIC_WAKE0	
A45	GND			B45	GPIO_20_DSI_1	MCASP0_AXR2	
A46	DP_1_AUX-	DP0_AUXN		B46	PWM_3_DSI	MCASP0_AXR5	
A47	DP_1_AUX+	DP0_AUXP		B47	GND		
A48	GND			B48	CAN_1_TX	MCASP1_AXR4	
A49	DP_1_LANE3-	SERDES4_TX3_N		B49	CAN_1_RX	MCASP1_ACLKX	
A50	DP_1_LANE3+	SERDES4_TX3_P		B50	CAN_2_TX	MCU_MCAN0_TX	
A51	GND			B51	CAN_2_RX	MCU_MCAN0_RX	
A52	DP_1_LANE2-	SERDES4_TX2_N		B52	GND		
A53	DP_1_LANE2+	SERDES4_TX2_P		B53	CAN_3_TX	MCAN13_TX	
A54	GND			B54	CAN_3_RX	MCAN13_RX	
A55	DP_1_LANE1-	SERDES4_TX1_N		B55	CAN_4_TX	WKUP_GPIO0_4	
A56	DP_1_LANE1+	SERDES4_TX1_P		B56	CAN_4_RX	WKUP_GPIO0_5	
A57	GND			B57	GPIO_21_DP	MCASP2_ACLKX	
A58	DP_1_LANE0-	SERDES4_TX0_N		B58	PWM_4_DP	MCASP0_AXR0	
A59	DP_1_LANE0+	SERDES4_TX0_P		B59	DP_1_HPD	MCAN14_TX	
A60	GND			B60	QSPI_1_IO3	MCU_OSPI0_D3	

Continued on next page

Table 3: Pin Map Column A and Column B (Continued)

Column A				Column B			
X1 Pin	Aquila Pin Name	Primary	Remarks	X1 Pin	Aquila Pin Name	Primary	Remarks
A61	USB_1_SSRX1_N	USB mux		B61	QSPI_1_IO2	MCU_OSPI0_D2	
A62	USB_1_SSRX1_P	USB mux		B62	QSPI_1_CS2#	MCU_OSPI0_CSn1	
A63	GND			B63	QSPI_1_DQS	MCU_OSPI0_DQS	
A64	USB_1_SSTX1_P	USB mux		B64	GND		
A65	USB_1_SSTX1_N	USB mux		B65	QSPI_1_SCK	MCU_OSPI0_CLK	
A66	GND			B66	QSPI_1_CS1#	MCU_OSPI0_CSn0	
A67	USB_1_SBU2	NC		B67	QSPI_1_IO1	MCU_OSPI0_D1	
A68	USB_1_SBU1	NC		B68	QSPI_1_IO0	MCU_OSPI0_D0	
A69	GND			B69	GND		
A70	USB_1_D_P	USB0_DP		B70	OSPI_1_IO4	MCU_OSPI0_D4	
A71	USB_1_D_N	USB0_DM		B71	OSPI_1_IO5	MCU_OSPI0_D5	
A72	GND			B72	OSPI_1_IO6	MCU_OSPI0_D6	
A73	USB_1_SSRX2_N	USB mux		B73	OSPI_1_IO7	MCU_OSPI0_D7	
A74	USB_1_SSRX2_P	USB mux		B74	USB_1_INT#	MCAN1_RX	
A75	GND			B75	USB_1_OC#	MCAN16_RX	
A76	USB_1_SSTX2_P	USB mux		B76	USB_1_VBUS	USB0_VBUS	
A77	USB_1_SSTX2_N	USB mux		B77	USB_1_EN	GPIO0_11	
A78	GND			B78	USB_2_OC#	USB Bridge	
A79	USB_2_SSTX1_N	USB Bridge		B79	USB_2_VBUS	NC	
A80	USB_2_SSTX1_P	USB Bridge		B80	USB_2_EN	USB Bridge	
A81	GND			B81	ETH_2_XGMII_INT#	MCASP1_AXR3	
A82	USB_2_SSRX1_N	USB Bridge		B82	GND		
A83	USB_2_SSRX1_P	USB Bridge		B83	ETH_2_XGMII_RX_N	SERDES2_RX3_N	SGMII_8_RX_N
A84	GND			B84	ETH_2_XGMII_RX_P	SERDES2_RX3_P	SGMII_8_RX_P
A85	USB_2_D_N	USB Bridge		B85	GND		
A86	USB_2_D_P	USB Bridge		B86	ETH_2_XGMII_TX_N	SERDES2_TX3_N	SGMII_8_TX_N
A87	GND			B87	ETH_2_XGMII_TX_P	SERDES2_TX3_P	SGMII_8_TX_P
A88	ETH_1_MDI0_P	Eth PHY		B88	GND		
A89	ETH_1_MDI0_N	Eth PHY		B89	ETH_2_XGMII_MDIO	MCASP2_AXR0	
A90	GND			B90	ETH_2_XGMII_MDC	MCASP2_AFSX	
A91	ETH_1_MDI1_P	Eth PHY		B91	CTRL_RECOVERY_MICO#	Recovery logic	
A92	ETH_1_MDI1_N	Eth PHY		B92	CTRL_RESET_MICO#	Reset logic	
A93	GND			B93	CTRL_PWR_BTN_MICO#	PMIC logic	
A94	ETH_1_MDI2_P	Eth PHY		B94	CTRL_FORCE_OFF_MOCI#	PMIC logic	
A95	ETH_1_MDI2_N	Eth PHY		B95	CTRL_PWR_EN_MOCI	PMIC logic	
A96	GND			B96	PWR_1V8_MOCI	+V1.8_VDD_IO	
A97	ETH_1_MDI3_P	Eth PHY		B97	VCC	VCC	

Continued on next page

Table 3: Pin Map Column A and Column B (Continued)

Column A				Column B			
X1 Pin	Aquila Pin Name	Primary	Remarks	X1 Pin	Aquila Pin Name	Primary	Remarks
A98	ETH_1_MDI3_N	Eth PHY		B98	VCC	VCC	
A99	ETH_1_LED1	Eth PHY		B99	VCC	VCC	
A100	ETH_1_LED2	Eth PHY		B100	VCC_BACKUP	VCC_BACKUP	

Table 4: Pin Map Column C

Column C				
X1 Pin	Aquila Pin Name	Primary	Secondary	Remarks
C1	GPIO_13_CSI_2	MCU_OSPI1_LBCLKO		
C2	GPIO_14_CSI_2	MCU_OSPI1_DQS		
C3	GPIO_15_CSI_2	MCU_OSPI1_D3		
C4	GGPIO_16_CSI_2	MCU_OSPI1_CSn1		
C5	I2C_5_CSI2_SDA	MCASP1_AXR2		
C6	I2C_5_CSI2_SCL	MCASP1_AXR1		
C7	JTAG_1_TRST#	TRSTn		
C8	JTAG_1_TDI	TDI		
C9	GND			
C10	JTAG_1_TDO	TDO		
C11	JTAG_1_TCK	TCK		
C12	JTAG_1_VREF	+V1.8_VDD_IO		
C13	JTAG_1_TMS	TMS		
C14	CTRL_TAMPER0	NC		
C15	CTRL_TAMPER1	NC		
C16	I2C_2_SDA	WKUP_GPIO0_9		
C17	I2C_2_SCL	WKUP_GPIO0_8		
C18	I2C_6_SDA	MCAN14_RX		
C19	I2C_6_SCL	MCAN15_TX		
C20	GPIO_04	MCU_OSPI0_LBCLKO		
C21	GPIO_05	MCU_OSPI0_CSn2		
C22	GPIO_06	MCU_OSPI0_CSn3		
C23	GPIO_07	MCU_OSPI1_CLK		
C24	GPIO_08	MCU_OSPI1_CSn0		
C25	PWM_1	MCAN0_TX		
C26	PWM_2	MCASP2_AXR1		
C27	GND			
C28	PCIE_2_L0_RX_P	SERDES0_RX0_P		
C29	PCIE_2_L0_RX_N	SERDES0_RX0_N		

Continued on next page

Table 4: Pin Map Column C (Continued)

Column C				
X1 Pin	**Aquila Pin Name**	**Primary**	**Secondary**	**Remarks**
C30	GND			
C31	PCIE_2_L1_RX_P	SERDES0_RX1_P		
C32	PCIE_2_L1_RX_N	SERDES0_RX1_N		
C33	GND			
C34	PCIE_2_CLKREQ#	GPIO Expander		
C35	PCIE_2_RESET#	MCASP0_AXR13		
C36	PCIE_WAKE#	MCU_ADC1_AIN1		
C37	PCIE_1_CLKREQ	GPIO Expander		
C38	PCIE_1_RESET#	MCASP0_AXR4		
C39	GND			
C40	PCIE_1_L0_RX_P	SERDES1_RX0_P		
C41	PCIE_1_L0_RX_N	SERDES1_RX0_N		
C42	GND			
C43	PCIE_1_L1_RX_P	SERDES1_RX1_P		
C44	PCIE_1_L1_RX_N	SERDES1_RX1_N		
C45	GND			
C46	MSP_1_RX_P	SERDES0_RX2_P		PCIE_4_L0_RX_P
C47	MSP_1_RX_N	SERDES0_RX2_N		PCIE_4_L0_RX_N
C48	GND			
C49	MSP_2_RX_P	GPIO Expander		PCIE_4_CLKREQ#
C50	MSP_2_RX_N	GPIO Expander		PCIE_4_RESET#
C51	GND			
C52	MSP_3_RX_P	PMIC-EN_DRV		
C53	MSP_3_RX_N	WKUP_GPIO0_3	+VDD_SD_DV	
C54	GND			
C55	MSP_4_RX_P	MCU_ADC0_AIN6		
C56	MSP_4_RX_N	MCU_ADC0_AIN7		
C57	GND			
C58	MSP_5_RX_P	wifi_led1	+V2.5_ETH	
C59	MSP_5_RX_N	wifi_led2	+V1.0_ETH	
C60	GND			
C61	MSP_6_RX_P	SERDES2_RX0_P		SGMII_5_RX_P
C62	MSP_6_RX_N	SERDES2_RX0_N		SGMII_5_RX_N
C63	GND			
C64	MSP_7_RX_P	SERDES2_RX1_P		SGMII_6_RX_P
C65	MSP_7_RX_N	SERDES2_RX1_N		SGMII_6_RX_N
C66	GND			
C67	MSP_8_RX_P	SERDES2_RX2_P		SGMII_7_RX_P

Continued on next page

Table 4: Pin Map Column C (Continued)

Column C				
X1 Pin	**Aquila Pin Name**	**Primary**	**Secondary**	**Remarks**
C68	MSP_8_RX_N	SERDES2_RX2_N		SGMII_7_RX_N
C69	GND			
C70	MSP_9_RX_P	SERDES1_RX3_P		SGMII_2_RX_P
C71	MSP_9_RX_N	SERDES1_RX3_N		SGMII_2_RX_N
C72	GND			
C73	MSP_10_RX_P	Wi-Fi Module	+V1.1_VDD_DDR	LTE_COEX_TXD
C74	MSP_10_RX_N	Wi-Fi Module	+V1.1_VIO	LTE_COEX_RXD
C75	GND			
C76	MSP_11_RX_P	USB Bridge SS_RX_P	SERDES1_RX2_P	PCIE_3_L0_RX_P
C77	MSP_11_RX_N	USB Bridge SS_RX_N	SERDES1_RX2_N	PCIE_3_L0_RX_N
C78	GND			
C79	MSP_12_RX_P	USB Bridge OC#	GPIO Expander	PCIE_3_CLKREQ#
C80	MSP_12_RX_N	USB Bridge EN	GPIO Expander	PCIE_3_RESET#
C81	GND			
C82	MSP_13_RX_P	CSI2_RXP3		CSI_3_D3_P
C83	MSP_13_RX_N	CSI2_RXN3		CSI_3_D3_N
C84	GND			
C85	MSP_14_RX_P	CSI2_RXP2		CSI_3_D2_P
C86	MSP_14_RX_N	CSI2_RXN2		CSI_3_D2_N
C87	GND			
C88	MSP_15_RX_P	CSI2_RXCLKP		CSI_3_CLK_P
C89	MSP_15_RX_N	CSI2_RXCLKN		CSI_3_CLK_N
C90	GND			
C91	MSP_16_RX_P	CSI2_RXP1		DSI_3_D1_P
C92	MSP_16_RX_N	CSI2_RXN1		CSI_3_D1_N
C93	GND			
C94	MSP_17_RX_P	CSI2_RXP0		CSI_2_D0_P
C95	MSP_17_RX_N	CSI2_RXN0		CSI_3_D0_N
C96	VCC	VCC		
C97	VCC	VCC		
C98	VCC	VCC		
C99	VCC	VCC		
C100	VCC	VCC		

Table 5: Pin Map Column D

Column D				
X1 Pin	**Aquila Pin Name**	**Primary**	**Secondary**	**Remarks**
D1	ADC_1	MCU_ADC0_AIN0		
D2	ADC_2	MCU_ADC0_AIN1		
D3	ADC_3	MCU_ADC0_AIN2		
D4	ADC_4	MCU_ADC0_AIN3		
D5	CTRL_RESET_MOCI#	Reset logic		
D6	CTRL_WAKE1_MICO#	WKUP_GPIO0_49		
D7	I2C_1_SDA	MCU_I2C0_SDA		
D8	I2C_1_SCL	MCU_I2C0_SCL		
D9	SPI_1_CS	MCASP0_AXR11		
D10	SPI_1_MISO	MCASP0_AXR14		
D11	SPI_1_MOSI	MCASP0_AXR15		
D12	SPI_1_CLK	MCASP0_AXR12		
D13	GND			
D14	SPI_2_CLK	SPI0_CLK		
D15	SPI_2_MISO	SPI0_D0		
D16	SPI_2_CS	SPI0_CS0		
D17	SPI_2_MOSI	SPI0_D1		
D18	GND			
D19	UART_3_RXD	MCASP0_ACLKX		
D20	UART_3_TXD	MCASP0_AFSX		
D21	UART_4_RXD	MCU_OSPI1_D1		
D22	UART_4_TXD	WKUP_GPIO0_10		
D23	GPIO_01	MCASP0_AXR6		
D24	GPIO_02	MCASP0_AXR1		
D25	GPIO_03	MCAN2_TX		
D26	GND			
D27	PCIE_2_CLK_P	PCIE_REFCLK1_P_OUT		
D28	PCIE_2_CLK_N	PCIE_REFCLK1_N_OUT		
D29	GND			
D30	PCIE_2_L0_TX_P	SERDES0_TX0_P		
D31	PCIE_2_L0_TX_N	SERDES0_TX0_N		
D32	GND			
D33	PCIE_2_L1_TX_P	SERDES0_TX1_P		
D34	PCIE_2_L1_TX_N	SERDES0_TX1_N		
D35	GND			
D36	PCIE_1_CLK_P	PCIE_REFCLK0_P_OUT		
D37	PCIE_1_CLK_N	PCIE_REFCLK0_N_OUT		
D38	GND			

Continued on next page

Table 5: Pin Map Column D (Continued)

Column D				
X1 Pin	**Aquila Pin Name**	**Primary**	**Secondary**	**Remarks**
D39	PCIE_1_L0_TX_P	SERDES1_TX0_P		
D40	PCIE_1_L0_TX_N	SERDES1_TX0_N		
D41	GND			
D42	PCIE_1_L1_TX_P	SERDES1_TX1_P		
D43	PCIE_1_L1_TX_N	SERDES1_TX1_N		
D44	GND			
D45	MSP_1_TX_P	SERDES0_TX2_P		PCIE_4_L0_TX_P
D46	MSP_1_TX_N	SERDES0_TX2_N		PCIE_4_L0_TX_N
D47	GND			
D48	MSP_2_TX_P	PCIE_REFCLK3_P_OUT		PCIE_4_CLK_P
D49	MSP_2_TX_N	PCIE_REFCLK3_N_OUT		PCIE_4_CLK_N
D50	GND			
D51	MSP_3_TX_P	clk32_out		
D52	MSP_3_TX_N	phy-eth-1588-sof	TIMER_IO1	
D53	GND			
D54	MSP_4_TX_P	MCU_ADC0_AIN4		
D55	MSP_4_TX_N	MCU_ADC0_AIN5		
D56	GND			
D57	MSP_5_TX_P	CTRL_MCU_RESET_MOCI#		
D58	MSP_5_TX_N	DSCRT_PWRGRP_IRQn		
D59	GND			
D60	MSP_6_TX_P	SERDES2_TX0_P		SGMII_5_TX_P
D61	MSP_6_TX_N	SERDES2_TX0_N		SGMII_5_TX_N
D62	GND			
D63	MSP_7_TX_P	SERDES2_TX1_P		SGMII_6_TX_P
D64	MSP_7_TX_N	SERDES2_TX1_N		SGMII_6_TX_N
D65	GND			
D66	MSP_8_TX_P	SERDES2_TX2_P		SGMII_7_TX_P
D67	MSP_8_TX_N	SERDES2_TX2_N		SGMII_7_TX_N
D68	GND			
D69	MSP_9_TX_P	SERDES1_TX3_P		SGMII_2_TX_P
D70	MSP_9_TX_N	SERDES1_TX3_N		SGMII_2_TX_N
D71	GND			
D72	MSP_10_TX_P	wifi_laa_tx_en	+V0.85_VDD_RAM	
D73	MSP_10_TX_N	wifi_wl_tx_en	+V0.8_VDA_DLL	
D74	GND			
D75	MSP_11_TX_P	USB Bridge SS_TX_P	SERDES1_TX2_P	PCIE_3_L0_TX_P
D76	MSP_11_TX_N	USB Bridge SS_TX_N	SERDES1_TX2_N	PCIE_3_L0_TX_N

Continued on next page

Table 5: Pin Map Column D (Continued)

Column D				
X1 Pin	**Aquila Pin Name**	**Primary**	**Secondary**	**Remarks**
D77	GND			
D78	MSP_12_TX_P	USB Bridge DP	PCIE_REFCLK2_P_OUT	
D79	MSP_12_TX_N	USB Bridge DN	PCIE_REFCLK2_N_OUT	
D80	GND			
D81	MSP_13_TX_P	DSI1_TXP0		DSI_2_D0_P
D82	MSP_13_TX_N	DSI1_TXN0		DSI_2_D0_N
D83	GND			
D84	MSP_14_TX_P	DSI1_TXP1		DSI_2_D1_P
D85	MSP_14_TX_N	DSI1_TXN1		DSI_2_D1_N
D86	GND			
D87	MSP_15_TX_P	DSI1_TXCLKP		DSI_2_CLK_P
D88	MSP_15_TX_N	DSI1_TXCLKN		DSI_2_CLK_N
D89	GND			
D90	MSP_16_TX_P	DSI1_TXP2		DSI_2_D2_P
D91	MSP_16_TX_N	DSI1_TXN2		DSI_2_D2_N
D92	GND			
D93	MSP_17_TX_P	DSI1_TXP3		DSI_2_D3_P
D94	MSP_17_TX_N	DSI1_TXN3		DSI_2_D3_N
D95	VCC	VCC		
D96	VCC	VCC		
D97	VCC	VCC		
D98	VCC	VCC		
D99	VCC	VCC		
D100	VCC	VCC		

4 I/O Pins

4.1 SoC Functions List

Tables 6 to 45 contain a list of all the SoC pins that are available on the X1 connector. It shows the alternate functions that are available for each pin. For most of the pins, the GPIO functionality is defined as the ALT7 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted in **bold**.

4.1.1 Alternate Functions

Table 6: Alternate functions from A1 to A10

Pin	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
Aquila Pin Name	SD_1_CD#	SD_1_D1	SD_1_D0	GND	SD_1_CLK	SD_1_PWR_EN	SD_1_CMD	SD_1_D3	GND	SD_1_D2
Main use	MMC1_SDCD	MMC1_DAT1	MMC1_DAT0		MMC1_CLK	GPIO0_52	MMC1_CMD	MMC1_DAT3		MMC1_DAT2
Primary	TIMER_IO0	MMC1_DAT1	MMC1_DAT0		MMC1_CLK	SPI0_CS1	MMC1_CMD	MMC1_DAT3		MMC1_DAT2
Mode 0	TIMER_IO0	MMC1_DAT1	MMC1_DAT0		MMC1_CLK	SPI0_CS1	MMC1_CMD	MMC1_DAT3		MMC1_DAT2
Mode 1	ECAP1_IN_APWM_OUT	UART7_CTSn	UART7_RTSn		UART8_RXD	CPTS0_TS_COMP	UART8_TXD	UART7_RXD		UART7_TXD
Mode 2	SYSCLKOUT0	ECAP0_IN_APWM_OUT	ECAP1_IN_APWM_OUT			UART0_RTSn		PCIE1_CLKREQn		
Mode 3	DDR0_IO_PLL_TESTOUT0P	TIMER_IO4	TIMER_IO5		TIMER_IO6	MCASP3_AFSX	TIMER_IO7	TIMER_IO2		TIMER_IO3
Mode 4	DDR0_IO_PLL_TESTOUT1P	EHRPWM1_B	EHRPWM1_A		EHRPWM2_B	MCASP3_AFSR	EHRPWM2_A	EHRPWM0_B		EHRPWM0_A
Mode 5	UART3_RXD	UART4_RXD	UART4_TXD		UART4_CTSn	EHRPWM1_A	UART4_RTSn			
Mode 6	PCIE1_CLKREQn	EHRPWM4_A			EHRPWM5_A			EHRPWM3_A		
Mode 7	GPIO0_58	GPIO0_62	GPIO0_63		GPIO0_64	GPIO0_52	GPIO0_65	GPIO0_60		GPIO0_61
Mode 8	MMC1_SDCD	SPI1_CS2	SPI1_D0		SPI1_CLK		SPI1_D1	SPI1_CS0		SPI1_CS1
Mode 9	MCAN13_TX	UART5_CTSn	UART5_RTSn		UART0_RTSn	MCAN14_RX		UART0_CTSn		CPTS0_TS_SYNC
Mode 10	DDR1_IO_PLL_TESTOUT0P	I2C4_SDA	I2C4_SCL		I2C6_SDA		I2C6_SCL	I2C3_SCL		I2C3_SDA
Mode 11	DDR1_IO_PLL_TESTOUT1P	UART2_RXD	UART2_TXD		MCAN15_TX	UART8_RXD	MCAN15_RX	UART5_RXD		UART5_TXD
Mode 12	DDR2_IO_PLL_TESTOUT0P	RSVD_ASYNC14	RSVD_ASYNC15		PCIE2_CLKREQn	RSVD_ASYNC9	PCIE3_CLKREQn	RSVD_ASYNC12		RSVD_ASYNC13
Mode 13	I2C6_SDA					PGD_VDD_CPU_MEM_FLAGH				
Mode 14	DDR2_IO_PLL_TESTOUT1P					VPU0_UART_RXD				
Mode 15										
Bootstrap										

Table 7: Alternate functions from A11 to A20

Pin	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
Aquila Pin Name	GPIO_11_CSI_1	I2C_4_CSI1_SDA	I2C_4_CSI1_SCL	CTRL_MCLK_MOCI	GND	CSI_1_D3_P	CSI_1_D3_N	GND	CSI_1_D2_P	CSI_1_D2_N
Main use	GPIO0_36	I2C1_SDA	I2C1_SCL			CSI0_RXP3	CSI0_RXN3		CSI0_RXP2	CSI0_RXN2
Primary	MCASP1_AFSX	MCAN16_TX	MCAN15_RX	WKUP_GPIO0_11		CSI0_RXP3	CSI0_RXN3		CSI0_RXP2	CSI0_RXN2
Mode 0	MCAN11_TX	MCAN16_TX	MCAN15_RX	MCU_OBSCLK0		CSI0_RXP3	CSI0_RXN3		CSI0_RXP2	CSI0_RXN2
Mode 1	MCASP1_AFSX			MCU_OBSCLK0						
Mode 2		VOUT0_DATA20	VOUT0_DATA21	MCU_UART0_RXD						
Mode 3				MCU_ADC_EXT_TRIGGER1						
Mode 4				MCU_TIMER_IO1						
Mode 5	GPMC0_A12			MCU_I3C0_SDAPULLEN						
Mode 6	MDIO0_MDIO	GPMC0_A16	GPMC0_A17	MCU_CLKOUT0						
Mode 7	GPIO0_47	GPIO0_9	GPIO0_8	WKUP_GPIO0_11						
Mode 8	SPI3_CS0	SPI1_CS3	SPI0_CS2							
Mode 9	EQEP0_I									
Mode 10		TRC_DATA23	TRC_DATA22							
Mode 11	UART0_RXD									
Mode 12		I2C1_SDA	I2C1_SCL							
Mode 13										
Mode 14										
Mode 15	LED_DIO7			LED_DI46						
Bootstrap										

Table 8: Alternate functions from A21 to A30

Pin	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30
Aquila Pin Name	GND	CSI_1_CLK_P	CSI_1_CLK_N	GND	CSI_1_D1_P	CSI_1_D1_N	GND	CSI_1_D0_P	CSI_1_D0_N	GND
Main use		CSI0_RXCLKP	CSI0_RXCLKN		CSI0_RXP1	CSI0_RXN1		CSI0_RXP0	CSI0_RXN0	
Primary		CSI0_RXCLKP	CSI0_RXCLKN		CSI0_RXP1	CSI0_RXN1		CSI0_RXP0	CSI0_RXN0	
Mode 0		CSI0_RXCLKP	CSI0_RXCLKN		CSI0_RXP1	CSI0_RXN1		CSI0_RXP0	CSI0_RXN0	
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 9: Alternate functions from A31 to A40

Pin	A31	A32	A33	A34	A35	A36	A37	A38	A39	A40
Aquila Pin Name	DSI_1_D3_N	DSI_1_D3_P	GND	DSI_1_D2_N	DSI_1_D2_P	GND	DSI_1_CLK_N	DSI_1_CLK_P	GND	DSI_1_D1_N
Main use	DSI0_TXN3	DSI0_TXP3		DSI0_TXN2	DSI0_TXP2		DSI0_TXCLKN	DSI0_TXCLKP		DSI0_TXN1
Primary	DSI0_TXN3	DSI0_TXP3		DSI0_TXN2	DSI0_TXP2		DSI0_TXCLKN	DSI0_TXCLKP		DSI0_TXN1
Mode 0	DSI0_TXN3	DSI0_TXP3		DSI0_TXN2	DSI0_TXP2		DSI0_TXCLKN	DSI0_TXCLKP		DSI0_TXN1
Mode 1	CSI0_TXN3	CSI0_TXP3		CSI0_TXN2	CSI0_TXP2		CSI0_TXCLKN	CSI0_TXCLKP		CSI0_TXN1
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 10: Alternate functions from A41 to A50

Pin	A41	A42	A43	A44	A45	A46	A47	A48	A49	A50
Aquila Pin Name	DSI_1_D1_P	GND	DSI_1_D0_N	DSI_1_D0_P	GND	DP_1_AUX-	DP_1_AUX+	GND	DP_1_LANE3-	DP_1_LANE3+
Main use	DSI0_TXP1		DSI0_TXN0	DSI0_TXP0		DP0_AUXN	DP0_AUXP		DP0_TXN3	DP0_TXP3
Primary	DSI0_TXP1		DSI0_TXN0	DSI0_TXP0		DP0_AUXN	DP0_AUXP		SERDES4_TX3_N	SERDES4_TX3_P
Mode 0	DSI0_TXP1		DSI0_TXN0	DSI0_TXP0		DP0_AUXN	DP0_AUXP		DP0_TXN3	DP0_TXP3
Mode 1	CSI0_TXP1		CSI0_TXN0	CSI0_TXP0					SGMII8_TXN0	SGMII8_TXP0
Mode 2									USB0_SSTX2N	USB0_SSTX2P
Mode 3										
Mode 4									HYP_TXN3	HYP_TXP3
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 11: Alternate functions from A51 to A60

Pin	A51	A52	A53	A54	A55	A56	A57	A58	A59	A60
Aquila Pin Name	GND	DP_1_LANE2-	DP_1_LANE2+	GND	DP_1_LANE1-	DP_1_LANE1+	GND	DP_1_LANE0-	DP_1_LANE0+	GND
Main use		DP0_TXN2	DP0_TXP2		DP0_TXN1	DP0_TXP1		DP0_TXN0	DP0_TXP0	
Primary		SERDES4_TX2_N	SERDES4_TX2_P		SERDES4_TX1_N	SERDES4_TX1_P		SERDES4_TX0_N	SERDES4_TX0_P	
Mode 0		DP0_TXN2	DP0_TXP2		DP0_TXN1	DP0_TXP1		DP0_TXN0	DP0_TXP0	
Mode 1		SGMII7_TXN0	SGMII7_TXP0		SGMII6_TXN0	SGMII6_TXP0		SGMII5_TXN0	SGMII5_TXP0	
Mode 2		USB0_SSTX1N	USB0_SSTX1P							
Mode 3										
Mode 4		HYP_TXN2	HYP_TXP2		HYP_TXN1	HYP_TXP1		HYP_TXN0	HYP_TXP0	
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 12: Alternate functions from A61 to A70

Pin	A61	A62	A63	A64	A65	A66	A67	A68	A69	A70
Aquila Pin Name	USB_1_SSRX1_N	USB_1_SSRX1_P	GND	USB_1_SSTX1_P	USB_1_SSTX1_N	GND	USB_1_SBU2	USB_1_SBU1	GND	USB_1_D_P
Main use										USB0_DP
Primary	USB mux	USB mux		USB mux	USB mux		NC	NC		USB0_DP
Mode 0										USB0_DP
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 13: Alternate functions from A71 to A80

Pin	A71	A72	A73	A74	A75	A76	A77	A78	A79	A80
Aquila Pin Name	USB_1_D_N	GND	USB_1_SSRX2_N	USB_1_SSRX2_P	GND	USB_1_SSTX2_P	USB_1_SSTX2_N	GND	USB_2_SSTX1_N	USB_2_SSTX1_P
Main use	USB0_DM									
Primary	USB0_DM		USB mux	USB mux		USB mux	USB mux		USB Bridge	USB Bridge
Mode 0	USB0_DM									
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 14: Alternate functions from A81 to A90

Pin	A81	A82	A83	A84	A85	A86	A87	A88	A89	A90
Aquila Pin Name	GND	USB_2_SSRX1_N	USB_2_SSRX1_P	GND	USB_2_D_N	USB_2_D_P	GND	ETH_1_MDI0_P	ETH_1_MDI0_N	GND
Main use										
Primary		USB Bridge	USB Bridge		USB Bridge	USB Bridge		Eth PHY	Eth PHY	
Mode 0										
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 15: Alternate functions from A91 to A100

Pin	A91	A92	A93	A94	A95	A96	A97	A98	A99	A100
Aquila Pin Name	ETH_1_MDI1_P	ETH_1_MDI1_N	GND	ETH_1_MDI2_P	ETH_1_MDI2_N	GND	ETH_1_MDI3_P	ETH_1_MDI3_N	ETH_1_LED1	ETH_1_LED2
Main use										
Primary	Eth PHY	Eth PHY		Eth PHY	Eth PHY		Eth PHY	Eth PHY	Eth PHY	Eth PHY
Mode 0										
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 16: Alternate functions from B1 to B10

Pin	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
Aquila Pin Name	GND	CSI_2_D3_P	CSI_2_D3_N	GND	CSI_2_D2_P	CSI_2_D2_N	GND	CSI_2_CLK_P	CSI_2_CLK_N	GND
Main use		CSI1_RXP0	CSI1_RXN0		CSI1_RXP1	CSI1_RXN1		CSI1_RXCLKP	CSI1_RXCLKN	
Primary		CSI1_RXP3	CSI1_RXN3		CSI1_RXP2	CSI1_RXN2		CSI1_RXCLKP	CSI1_RXCLKN	
Mode 0		CSI1_RXP3	CSI1_RXN3		CSI1_RXP2	CSI1_RXN2		CSI1_RXCLKP	CSI1_RXCLKN	
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 17: Alternate functions from B11 to B20

Pin	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20
Aquila Pin Name	CSI_2_D1_P	CSI_2_D1_N	GND	CSI_2_D0_P	CSI_2_D0_N	GND	GPIO_09_CSI_1	GPIO_10_CSI_1	GPIO_12_CSI_1	I2S_1_BCLK
Main use	CSI1_RXP2	CSI1_RXN2		CSI1_RXP3	CSI1_RXN3		GPIO0_1	GPIO0_2	GPIO0_38	MCASP4_ACLKX
Primary	CSI1_RXP1	CSI1_RXN1		CSI1_RXP0	CSI1_RXN0		MCAN12_TX	MCAN12_RX	MCASP1_AXR0	EXT_REFCLK1
Mode 0	CSI1_RXP1	CSI1_RXN1		CSI1_RXP0	CSI1_RXN0		MCAN12_TX	MCAN12_RX	MCAN11_RX	EXT_REFCLK1
Mode 1								UART0_DCDn	MCASP1_AXR0	MCASP4_ACLKX
Mode 2										VOUT0_DATA16
Mode 3							DSS_FSYNC0	DSS_FSYNC1		HYP1_TXFLDAT
Mode 4										MCAN1_RX
Mode 5									GPMC0_A13	
Mode 6							GPMC0_A24	GPMC0_A23	MDIO0_MDC	GPMC0_AD6
Mode 7							GPIO0_1	GPIO0_2	GPIO0_48	GPIO0_50
Mode 8									SPI3_CLK	
Mode 9									EQEP1_S	SYNC1_OUT
Mode 10							TRC_CLK	TRC_CTL		TRC_CLK
Mode 11							UART5_TXD	UART5_RXD	UART0_TXD	UART2_RTSn
Mode 12							GPMC0_CLK	GPMC0_CSn3	GPMC0_WAIT3	CPTS0_HW2TSPUSH
Mode 13										I2C1_SDA
Mode 14									SYNC2_OUT	UART3_TXD
Mode 15									LED_DIO6	
Bootstrap										

Table 18: Alternate functions from B21 to B30

Pin	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30
Aquila Pin Name	I2S_1_SYNC	I2S_1_D_OUT	I2S_1_D_IN	I2S_1_MCLK	GND	I2S_2_BCLK	I2S_2_SYNC	I2S_2_D_OUT	I2S_2_D_IN	GND
Main use	MCASP4_AFSX	MCASP4_AXR1	MCASP4_AXR2	AUDIO_EXT_REFCLK1						
Primary	MCAN1_TX	MCAN0_RX	ECAP0_IN_APWM_OUT	MCAN2_RX		GPIO Expander	GPIO Expander	GPIO Expander	GPIO Expander	
Mode 0	MCAN1_TX	MCAN0_RX	ECAP0_IN_APWM_OUT	MCAN2_RX						
Mode 1	MCASP4_AFSX	MCASP4_AXR1	MCASP4_AXR2	AUDIO_EXT_REFCLK1						
Mode 2	VOUT0_EXTPCLKIN	VOUT0_DATA3	CPTS0_RFT_CLK	VOUT0_PCLK						
Mode 3	HYP1_TXPMCLK		HYP1_TXFLCLK							
Mode 4	DSS_FSYNC0		MCAN12_TX							
Mode 5			VOUT0_DATA23							
Mode 6	GPMC0_AD7	GPMC0_AD15	GPMC0_AD5	GPMC0_CSn1						
Mode 7	GPIO0_27	GPIO0_26	GPIO0_49	GPIO0_30						
Mode 8		SPI5_CS0	SPI6_D0	SPI6_CS1						
Mode 9	EHRPWM_TZn_IN5	EHRPWM0_A	SYNC0_OUT	EHRPWM4_B						
Mode 10	TRC_CTL	TRC_DATA16	TRC_DATA1	TRC_DATA17						
Mode 11	UART6_TXD	UART2_TXD	UART2_CTSn	UART3_TXD						
Mode 12		UART6_RTSn	CPTS0_HW1TSPUSH	GPMC0_DIR						
Mode 13		SPI7_D0	I2C1_SCL	I2C5_SDA						
Mode 14			UART3_RXD							
Mode 15	LED_DIO10	LED_DIO9	LED_DIO20	LED_DIO13						
Bootstrap										

Table 19: Alternate functions from B31 to B40

Pin	B31	B32	B33	B34	B35	B36	B37	B38	B39	B40
Aquila Pin Name	UART_2_RXD	UART_2_CTS	UART_2_TXD	UART_2_RTS	UART_1_RXD	UART_1_CTS	UART_1_TXD	UART_1_RTS	GND	I2C_3_DSI1_SDA
Main use	WKUP_UART0_RXD	WKUP_UART0_CTSn	WKUP_UART0_TXD	WKUP_UART0_RTSn	UART1_RXD	UART1_CTSn	UART1_TXD	UART1_RTSn		I2C0_SDA
Primary	WKUP_UART0_RXD	WKUP_GPIO0_6	WKUP_UART0_TXD	WKUP_GPIO0_7	MCASP0_AXR7	MCASP0_AXR9	MCASP0_AXR8	MCASP0_AXR10		I2C0_SDA
Mode 0	WKUP_UART0_RXD	WKUP_UART0_CTSn	WKUP_UART0_TXD	WKUP_UART0_RTSn	MCAN5_TX	MCAN6_TX	MCAN5_RX	MCAN6_RX		I2C0_SDA
Mode 1		WKUP_UART0_CTSn		WKUP_UART0_RTSn	MCASP0_AXR7	MCASP0_AXR9	MCASP0_AXR8	MCASP0_AXR10		
Mode 2		MCU_CPTS0_HW1TSPUSH		MCU_CPTS0_HW2TSPUSH		MCASP4_AXR4				
Mode 3		MCU_I2C1_SCL		MCU_I2C1_SDA	MCASP4_ACLKR		MCASP4_AFSR			
Mode 4										
Mode 5					GPMC0_A0	GPMC0_A2	GPMC0_A1	GPMC0_A3		
Mode 6					RGMII1_TD0	RGMII1_TD2	RGMII1_TD1	RGMII1_TD3		
Mode 7	WKUP_GPIO0_58	WKUP_GPIO0_6	WKUP_GPIO0_59	WKUP_GPIO0_7	GPIO0_35	GPIO0_37	GPIO0_36	GPIO0_38		GPIO0_57
Mode 8					GPMC0_A14	RMII1_RXD1	RMII1_RXD0	RMII1_CRS_DV		
Mode 9					EHRPWM3_A	EHRPWM3_SYNCO	EHRPWM_TZn_IN3	EHRPWM3_SYNCI		
Mode 10										
Mode 11					UART4_RXD	UART4_CTSn	UART4_TXD	UART4_RTSn		
Mode 12					GPMC0_CSn2	RSVD_ASYNC4		RSVD_ASYNC5		
Mode 13					AC71_4_EXT_PLF_CPU_STALL_IPCFG	AC71_6_EXT_PLF_CPU_STALL_IPCFG	AC71_5_EXT_PLF_CPU_STALL_IPCFG	AC71_7_EXT_PLF_CPU_STALL_IPCFG		
Mode 14					USB0_DRVVBUS					
Mode 15		LED_DI39		LED_DI40	LED_DIO25	LED_DIO27	LED_DIO26	LED_DIO28		
Bootstrap										

Table 20: Alternate functions from B41 to B50

Pin	B41	B42	B43	B44	B45	B46	B47	B48	B49	B50
Aquila Pin Name	I2C_3_DSI1_SCL	GPIO_17_DSI_1	GPIO_18_DSI_1	GPIO_19_DSI_1	GPIO_20_DSI_1	PWM_3_DSI	GND	CAN_1_TX	CAN_1_RX	CAN_2_TX
Main use	I2C0_SCL	GPIO0_12	GPIO0_31	GPIO0_13	GPIO0_18	EHRPWM5_A		MCAN10_TX	MCAN10_RX	MCU_MCAN0_TX
Primary	I2C0_SCL	GPIO0_12	MCASP0_AXR3	PMIC_WAKE0	MCASP0_AXR2	MCASP0_AXR5		MCASP1_AXR4	MCASP1_ACLKX	MCU_MCAN0_TX
Mode 0	I2C0_SCL	MCAN12_RX	MCAN3_TX	PMIC_WAKE0	MCAN7_TX	MCAN4_TX		MCAN10_TX	MCAN10_RX	MCU_MCAN0_TX
Mode 1			MCASP0_AXR3	MCASP4_AXR0	MCASP0_AXR2	MCASP0_AXR5		MCASP1_AXR4	MCASP1_ACLKX	
Mode 2		VOUT0_DATA17	VOUT0_DATA2		VOUT0_DATA11	VOUT0_DE				
Mode 3		HYP1_RXFLDAT			HYP1_RXFLCLK				DP0_HPD	
Mode 4				DSS_FSYNC1		VOUT0_VP0_DE		PCIE3_CLKREQn	PCIE0_CLKREQn	
Mode 5		VOUT0_DATA22		MCAN17_RX		VOUT0_VP2_DE		GPMC0_A10	GPMC0_A11	
Mode 6		GPMC0_AD4	GPMC0_BE1n	GPMC0_WEn	GPMC0_ADVn_ALE	GPMC0_CSn0		RGMII1_TXC	RGMII1_RD0	
Mode 7	GPIO0_56	GPIO0_12	GPIO0_31	GPIO0_13	GPIO0_18	GPIO0_33		GPIO0_45	GPIO0_46	WKUP_GPIO0_60
Mode 8		SPI6_CLK	SPI5_CLK	SPI6_CS0		SPI6_CS3				
Mode 9		EQEP1_I	EHRPWM_TZn_IN0		EQEP2_A	EHRPWM5_A		EQEP1_B	EQEP0_S	
Mode 10		TRC_DATA2	TRC_DATA7	TRC_DATA0	TRC_DATA10	TRC_DATA19				
Mode 11		UART9_CTSn	UART3_CTSn	UART9_RTSn	UART4_CTSn			UART4_RXD	UART4_RTSn	
Mode 12		UART6_RXD	SPI3_CS1		GPMC0_WPn				SPI3_CS3	
Mode 13			SPI7_D1	UART7_TXD	UART9_CTSn	I2C4_SCL			UART9_RTSn	
Mode 14				AUDIO_EXT_REFCLK0					PGD_VDD_CPU1_CORE_FLAGL	
Mode 15		LED_CLK	LED_DIO21		LED_DIO5	LED_DIO23		LED_OPCODE2	LED_DIO4	
Bootstrap										

Table 21: Alternate functions from B51 to B60

Pin	B51	B52	B53	B54	B55	B56	B57	B58	B59	B60
Aquila Pin Name	CAN_2_RX	GND	CAN_3_TX	CAN_3_RX	CAN_4_TX	CAN_4_RX	GPIO_21_DP	PWM_4_DP	DP_1_HPD	QSPI_1_IO3
Main use	MCU_MCAN0_RX		MCAN13_TX	MCAN13_RX	MCU_MCAN1_TX	MCU_MCAN1_RX	GPIO0_5	EHRPWM5_B	DP0_HPD	MCU_OSPI0_D3
Primary	MCU_MCAN0_RX		MCAN13_TX	MCAN13_RX	WKUP_GPIO0_4	WKUP_GPIO0_5	MCASP2_ACLKX	MCASP0_AXR0	MCAN14_TX	MCU_OSPI0_D3
Mode 0	MCU_MCAN0_RX		MCAN13_TX	MCAN13_RX	MCU_MCAN1_TX	MCU_MCAN1_RX	MCAN8_RX	MCAN6_TX	MCAN14_TX	MCU_OSPI0_D3
Mode 1			UART0_DSRn	UART0_DTRn	MCU_MCAN1_TX	MCU_MCAN1_RX	MCASP2_ACLKX	MCASP0_AXR0	UART0_RIn	MCU_HYPERBUS0_DQ3
Mode 2					MCU_SPI0_CS3	MCU_SPI1_CS3	VOUT0_DATA8	VOUT0_DATA13		
Mode 3			DSS_FSYNC2	DSS_FSYNC3	MCU_ADC_EXT_TRIGGER0	MCU_ADC_EXT_TRIGGER1	HYP0_TXPMCLK	HYP0_TXFLCLK		
Mode 4										
Mode 5							VOUT0_DATA20			
Mode 6			GPMC0_A22	GPMC0_A21			GPMC0_AD10	GPMC0_AD2	GPMC0_A20	
Mode 7	WKUP_GPIO0_61		GPIO0_3	GPIO0_4	WKUP_GPIO0_4	WKUP_GPIO0_5	GPIO0_21	GPIO0_16	GPIO0_5	WKUP_GPIO0_22
Mode 8				I2C4_SDA			SPI5_CS2	SPI2_CS2	I2C4_SCL	
Mode 9							EQEP2_S	EHRPWM2_A		
Mode 10			TRC_DATA0	TRC_DATA1			TRC_DATA4	TRC_DATA14	TRC_DATA2	
Mode 11			UART4_TXD	UART6_TXD			UART1_RXD	UART4_RXD	UART6_RXD	
Mode 12			GPMC0_WAIT2							
Mode 13				RSVD_ASYNC0			SPI7_CS1	SPI7_CLK	DP0_HPD	
Mode 14							SYNC3_OUT	UART8_CTSn		
Mode 15	LED_DI56				LED_DI37	LED_DI38	LED_DIO16	LED_DIO3		LED_OPCODE3
Bootstrap										

Table 22: Alternate functions from B61 to B70

Pin	B61	B62	B63	B64	B65	B66	B67	B68	B69	B70
Aquila Pin Name	QSPI_1_IO2	QSPI_1_CS2#	QSPI_1_DQS	GND	QSPI_1_SCK	QSPI_1_CS1#	QSPI_1_IO1	QSPI_1_IO0	GND	OSPI_1_IO4
Main use	MCU_OSPI0_D2	MCU_OSPI0_CSn1	MCU_OSPI0_DQS		MCU_OSPI0_CLK	MCU_OSPI0_CSn0	MCU_OSPI0_D1	MCU_OSPI0_D0		MCU_OSPI0_D4
Primary	MCU_OSPI0_D2	MCU_OSPI0_CSn1	MCU_OSPI0_DQS		MCU_OSPI0_CLK	MCU_OSPI0_CSn0	MCU_OSPI0_D1	MCU_OSPI0_D0		MCU_OSPI0_D4
Mode 0	MCU_OSPI0_D2	MCU_OSPI0_CSn1	MCU_OSPI0_DQS		MCU_OSPI0_CLK	MCU_OSPI0_CSn0	MCU_OSPI0_D1	MCU_OSPI0_D0		MCU_OSPI0_D4
Mode 1	MCU_HYPERBUS0_DQ2	MCU_HYPERBUS0_RESETn	MCU_HYPERBUS0_RWDS		MCU_HYPERBUS0_CK	MCU_HYPERBUS0_CSn0	MCU_HYPERBUS0_DQ1	MCU_HYPERBUS0_DQ0		MCU_HYPERBUS0_DQ4
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7	WKUP_GPIO0_21	WKUP_GPIO0_28	WKUP_GPIO0_18		WKUP_GPIO0_16	WKUP_GPIO0_27	WKUP_GPIO0_20	WKUP_GPIO0_19		WKUP_GPIO0_23
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15	LED_DI63	LED_DI60	LED_DI57		LED_DI58	LED_DI59	LED_DI62	LED_DI61		LED_DOUT_SEL0
Bootstrap							BOOTMODE01	BOOTMODE00		BOOTMODE02

Table 23: Alternate functions from B71 to B80

Pin	B71	B72	B73	B74	B75	B76	B77	B78	B79	B80
Aquila Pin Name	OSPI_1_IO5	OSPI_1_IO6	OSPI_1_IO7	USB_1_INT#	USB_1_OC#	USB_1_VBUS	USB_1_EN	USB_2_OC#	USB_2_VBUS	USB_2_EN
Main use	MCU_OSPI0_D5	MCU_OSPI0_D6	MCU_OSPI0_D7	GPIO0_28	GPIO0_10	USB0_VBUS	GPIO0_11			
Primary	MCU_OSPI0_D5	MCU_OSPI0_D6	MCU_OSPI0_D7	MCAN1_RX	MCAN16_RX	USB0_VBUS	GPIO0_11	USB Bridge	NC	USB Bridge
Mode 0	MCU_OSPI0_D5	MCU_OSPI0_D6	MCU_OSPI0_D7	MCAN1_RX	MCAN16_RX	USB0_VBUS	MCAN17_TX			
Mode 1	MCU_HYPERBUS0_DQ5	MCU_HYPERBUS0_DQ6	MCU_HYPERBUS0_DQ7	MCASP4_AXR3						
Mode 2				VOUT0_DATA1	VOUT0_DATA19		VOUT0_DATA18			
Mode 3										
Mode 4										
Mode 5				VOUT0_DATA19						
Mode 6				GPMC0_BE0n_CLE	GPMC0_A15		GPMC0_A14			
Mode 7	WKUP_GPIO0_24	WKUP_GPIO0_25	WKUP_GPIO0_26	GPIO0_28	GPIO0_10		GPIO0_11			
Mode 8				SPI5_D0	SPI0_CS3		SPI7_CS3			
Mode 9				EHRPWM0_SYNCI						
Mode 10				TRC_DATA5	TRC_DATA24		TRC_DATA25			
Mode 11				UART3_RTSn						
Mode 12					GPMC0_WAIT1		GPMC0_CSn2			
Mode 13							UART7_RXD			
Mode 14							USB0_DRVVBUS			
Mode 15	LED_DOUT_SEL1	LED_DVALID	LED_ACK	LED_DIO11						
Bootstrap	BOOTMODE03									

Table 24: Alternate functions from B81 to B90

Pin	B81	B82	B83	B84	B85	B86	B87	B88	B89	B90
Aquila Pin Name	ETH_2_XGMII_INT#	GND	ETH_2_XGMII_RX_N	ETH_2_XGMII_RX_P	GND	ETH_2_XGMII_TX_N	ETH_2_XGMII_TX_P	GND	ETH_2_XGMII_MDIO	ETH_2_XGMII_MDC
Main use	GPIO0_44		SGMII8_RXN0	SGMII8_RXP0		SGMII8_TXN0	SGMII8_TXP0		MDIO0_MDIO	MDIO0_MDC
Primary	MCASP1_AXR3		SERDES2_RX3_N	SERDES2_RX3_P		SERDES2_TX3_N	SERDES2_TX3_P		MCASP2_AXR0	MCASP2_AFSX
Mode 0	MCAN9_RX		SGMII8_RXN0	SGMII8_RXP0		SGMII8_TXN0	SGMII8_TXP0		MCAN9_RX	MCAN9_TX
Mode 1	MCASP1_AXR3		SGMII2_RXN0	SGMII2_RXP0		SGMII2_TXN0	SGMII2_TXP0		MCASP2_AXR0	MCASP2_AFSX
Mode 2									VOUT0_DATA6	VOUT0_DATA7
Mode 3									HYP0_RXPMCLK	HYP0_TXPMDAT
Mode 4	PCIE2_CLKREQn								MDIO1_MDIO	MDIO1_MDC
Mode 5	GPMC0_A9									
Mode 6	RGMII1_RXC								GPMC0_AD12	GPMC0_AD11
Mode 7	GPIO0_44								GPIO0_23	GPIO0_22
Mode 8	RMII1_TXD1									SPI5_CS3
Mode 9	EQEP1_A								EQEP2_I	EHRPWM_SOCA
Mode 10									TRC_DATA15	TRC_DATA9
Mode 11	UART8_TXD								UART1_CTSn	UART1_TXD
Mode 12									UART6_RXD	
Mode 13	I2C1_SDA									SPI7_CS2
Mode 14	PGD_VDD_CPU1_CORE_FLAGH									
Mode 15	LED_OPCODE1								LED_DIO18	LED_DIO17
Bootstrap										

Table 25: Alternate functions from B91 to B100

Pin	B91	B92	B93	B94	B95	B96	B97	B98	B99	B100
Aquila Pin Name	CTRL_RECOVERY_MICO#	CTRL_RESET_MICO#	CTRL_PWR_BTN_MICO#	CTRL_FORCE_OFF_MOCI#	CTRL_PWR_EN_MOCI	PWR_1V8_MOCI	VCC	VCC	VCC	VCC_BACKUP
Main use										
Primary	Recovery logic	Reset logic	pmic logic	pmic logic	pmic logic	+V1.8_VDD_IO	VCC	VCC	VCC	VCC_BACKUP
Mode 0										
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 26: Alternate functions from C1 to C10

Pin	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
Aquila Pin Name	GPIO_13_CSI_2	GPIO_14_CSI_2	GPIO_15_CSI_2	GPIO_16_CSI_2	I2C_5_CSI2_SDA	I2C_5_CSI2_SCL	JTAG_1_TRST#	JTAG_1_TDI	GND	JTAG_1_TDO
Main use	WKUP_GPIO0_32	WKUP_GPIO0_33	WKUP_GPIO0_37	WKUP_GPIO0_39	I2C2_SDA	I2C2_SCL	TRSTn	TDI		TDO
Primary	MCU_OSPI1_LBCLKO	MCU_OSPI1_DQS	MCU_OSPI1_D3	MCU_OSPI1_CSn1	MCASP1_AXR2	MCASP1_AXR1	TRSTn	TDI		TDO
Mode 0	MCU_OSPI1_LBCLKO	MCU_OSPI1_DQS	MCU_OSPI1_D3	MCU_OSPI1_CSn1	MCAN8_TX	MCAN7_RX	TRSTn	TDI		TDO
Mode 1	MCU_OSPI0_CSn2	MCU_OSPI0_CSn3		MCU_HYPERBUS0_WPn	MCASP1_AXR2	MCASP1_AXR1				
Mode 2	MCU_HYPERBUS0_RESETOn	MCU_HYPERBUS0_INTn		MCU_TIMER_IO0	VOUT0_DATA9	VOUT0_DATA10				
Mode 3				MCU_HYPERBUS0_CSn1	HYP1_RXPMDAT	HYP1_RXPMCLK				
Mode 4			MCU_UART0_CTSn	MCU_UART0_RTSn						
Mode 5			MCU_SPI0_CS1	MCU_SPI0_CS2	VOUT0_DATA21					
Mode 6	MCU_OSPI0_RESET_OUT0	MCU_OSPI0_ECC_FAIL		MCU_OSPI0_RESET_OUT1	GPMC0_AD9	GPMC0_AD8				
Mode 7	WKUP_GPIO0_32	WKUP_GPIO0_33	WKUP_GPIO0_37	WKUP_GPIO0_39	GPIO0_20	GPIO0_19				
Mode 8					SPI3_D1	SPI3_D0				
Mode 9					EQEP2_B	EHRPWM_TZn_IN1				
Mode 10					TRC_DATA6	TRC_DATA8				
Mode 11					UART0_RTSn	UART0_CTSn				
Mode 12					UART9_TXD	UART9_RXD				
Mode 13					I2C2_SDA	I2C2_SCL				
Mode 14										
Mode 15					LED_DIO15	LED_DIO14				
Bootstrap										

Table 27: Alternate functions from C11 to C20

Pin	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20
Aquila Pin Name	JTAG_1_TCK	JTAG_1_VREF	JTAG_1_TMS	CTRL_TAMPER0	CTRL_TAMPER1	I2C_2_SDA	I2C_2_SCL	I2C_6_SDA	I2C_6_SCL	GPIO_04
Main use	TCK		TMS			MCU_I2C1_SDA	MCU_I2C1_SCL	I2C5_SDA	I2C5_SCL	WKUP_GPIO0_17
Primary	TCK	+V1.8_VDD_IO	TMS	NC	NC	WKUP_GPIO0_9	WKUP_GPIO0_8	MCAN14_RX	MCAN15_TX	MCU_OSPI0_LBCLKO
Mode 0	TCK		TMS			MCU_I2C1_SDA	MCU_I2C1_SCL	MCAN14_RX	MCAN15_TX	MCU_OSPI0_LBCLKO
Mode 1						MCU_I2C1_SDA	MCU_I2C1_SCL			MCU_HYPERBUS0_CKn
Mode 2						MCU_CPTS0_TS_COMP	MCU_CPTS0_TS_SYNC	VOUT0_DATA23	VOUT0_DATA22	
Mode 3						MCU_I3C0_SDA	MCU_I3C0_SCL			
Mode 4						MCU_TIMER_IO7	MCU_TIMER_IO6			
Mode 5										
Mode 6								GPMC0_A19	GPMC0_A18	
Mode 7						WKUP_GPIO0_9	WKUP_GPIO0_8	GPIO0_6	GPIO0_7	WKUP_GPIO0_17
Mode 8								I2C5_SDA	I2C5_SCL	
Mode 9										
Mode 10								TRC_DATA3	TRC_DATA21	
Mode 11								UART9_TXD	UART9_RXD	
Mode 12										
Mode 13								RSVD_ASYNC2	RSVD_ASYNC3	
Mode 14										
Mode 15						LED_DI42	LED_DI41			
Bootstrap										

Table 28: Alternate functions from C21 to C30

Pin	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30
Aquila Pin Name	GPIO_05	GPIO_06	GPIO_07	GPIO_08	PWM_1	PWM_2	GND	PCIE_2_L0_RX_P	PCIE_2_L0_RX_N	GND
Main use	WKUP_GPIO0_29	WKUP_GPIO0_30	WKUP_GPIO0_31	WKUP_GPIO0_38	EHRPWM0_B	EHRPWM3_A		PCIE1_RXP0	PCIE1_RXN0	
Primary	MCU_OSPI0_CSn2	MCU_OSPI0_CSn3	MCU_OSPI1_CLK	MCU_OSPI1_CSn0	MCAN0_TX	MCASP2_AXR1		SERDES0_RX0_P	SERDES0_RX0_N	
Mode 0	MCU_OSPI0_CSn2	MCU_OSPI0_CSn3	MCU_OSPI1_CLK	MCU_OSPI1_CSn0	MCAN0_TX	MCAN17_RX				
Mode 1	MCU_OSPI0_CSn2	MCU_OSPI0_CSn3			MCASP2_AXR2	MCASP2_AXR1		PCIE1_RXP0	PCIE1_RXN0	
Mode 2	MCU_HYPERBUS0_RESETOn	MCU_HYPERBUS0_INTn			VOUT0_DATA4	VOUT0_DATA5				
Mode 3	MCU_HYPERBUS0_WPn	MCU_HYPERBUS0_WPn				HYP0_RXPMDAT				
Mode 4	MCU_HYPERBUS0_CSn1							HYP_RXP0	HYP_RXN0	
Mode 5		MCU_OSPI0_RESET_OUT1								
Mode 6	MCU_OSPI0_RESET_OUT0	MCU_OSPI0_ECC_FAIL			GPMC0_AD14	GPMC0_AD13				
Mode 7	WKUP_GPIO0_29	WKUP_GPIO0_30	WKUP_GPIO0_31	WKUP_GPIO0_38	GPIO0_25	GPIO0_24				
Mode 8					SPI5_CS1					
Mode 9					EHRPWM0_B	EHRPWM1_A				
Mode 10					TRC_DATA11	TRC_DATA13				
Mode 11					UART2_RXD	UART1_RTSn				
Mode 12					UART6_CTSn	UART6_TXD				
Mode 13					I2C3_SCL	I2C3_SDA				
Mode 14										
Mode 15					LED_DIO8	LED_DIO19				
Bootstrap										

Table 29: Alternate functions from C31 to C40

Pin	C31	C32	C33	C34	C35	C36	C37	C38	C39	C40
Aquila Pin Name	PCIE_2_L1_RX_P	PCIE_2_L1_RX_N	GND	PCIE_2_CLKREQ#	PCIE_2_RESET#	PCIE_WAKE#	PCIE_1_CLKREQ	PCIE_1_RESET#	GND	PCIE_1_L0_RX_P
Main use	PCIE1_RXP1	PCIE1_RXN1			GPIO0_41	WKUP_GPIO0_80		GPIO0_32		SGMII3_RXP0
Primary	SERDES0_RX1_P	SERDES0_RX1_N		GPIO Expander	MCASP0_AXR13	MCU_ADC1_AIN1	GPIO Expander	MCASP0_AXR4		SERDES1_RX0_P
Mode 0					MCAN8_TX	MCU_ADC1_AIN1		MCAN3_RX		SGMII3_RXP0
Mode 1	PCIE1_RXP1	PCIE1_RXN1			MCASP0_AXR13			MCASP0_AXR4		PCIE0_RXP0
Mode 2								VOUT0_HSYNC		
Mode 3					MCASP2_AFSR			HYP1_TXPMDAT		
Mode 4	HYP_RXP1	HYP_RXN1						VOUT0_VP0_HSYNC		
Mode 5					GPMC0_A6			VOUT0_VP2_HSYNC		
Mode 6					RGMII1_RD2			GPMC0_OEn_REn		
Mode 7					GPIO0_41	WKUP_GPIO0_80		GPIO0_32		
Mode 8					RMII_REF_CLK			SPI6_CS2		
Mode 9					EHRPWM4_A			EHRPWM5_B		
Mode 10					SPI2_CS0			TRC_DATA18		
Mode 11					UART5_CTSn					
Mode 12					RSVD_ASYNC6					
Mode 13					UART7_RXD			I2C4_SDA		
Mode 14					PGD_VDD_MAIN_CORE_FLAGl					
Mode 15					LED_DIO31			LED_DIO22		
Bootstrap										

Table 30: Alternate functions from C41 to C50

Pin	C41	C42	C43	C44	C45	C46	C47	C48	C49	C50
Aquila Pin Name	PCIE_1_L0_RX_N	GND	PCIE_1_L1_RX_P	PCIE_1_L1_RX_N	GND	MSP_1_RX_P	MSP_1_RX_N	GND	MSP_2_RX_P	MSP_2_RX_N
Main use	SGMII3_RXN0		SGMII4_RXP0	SGMII4_RXN0		PCIE3_RXP0	PCIE3_RXN0			
Primary	SERDES1_RX0_N		SERDES1_RX1_P	SERDES1_RX1_N		SERDES0_RX2_P	SERDES0_RX2_N		GPIO Expander	GPIO Expander
Mode 0	SGMII3_RXN0		SGMII4_RXP0	SGMII4_RXN0						
Mode 1	PCIE0_RXN0		PCIE0_RXP1	PCIE0_RXN1		PCIE1_RXP2	PCIE1_RXN2			
Mode 2						USB0_SSRX1P	USB0_SSRX1N			
Mode 3						PCIE3_RXP0	PCIE3_RXN0			
Mode 4						HYP_RXP2	HYP_RXN2			
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 31: Alternate functions from C51 to C60

Pin	C51	C52	C53	C54	C55	C56	C57	C58	C59	C60
Aquila Pin Name	GND	MSP_3_RX_P	MSP_3_RX_N	GND	MSP_4_RX_P	MSP_4_RX_N	GND	MSP_5_RX_P	MSP_5_RX_N	GND
Main use			WKUP_GPIO0_3		MCU_ADC0_AIN6	MCU_ADC0_AIN7				
Primary		PMIC-EN_DRV	WKUP_GPIO0_3		MCU_ADC0_AIN6	MCU_ADC0_AIN7		wifi_led1	wifi_led2	
Mode 0			MCU_SPI1_CS0		MCU_ADC0_AIN6	MCU_ADC0_AIN7				
Mode 1			MCU_SPI1_CS0							
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7			WKUP_GPIO0_3		WKUP_GPIO0_77	WKUP_GPIO0_78				
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15			LED_DI36							
Bootstrap										

Table 32: Alternate functions from C61 to C70

Pin	C61	C62	C63	C64	C65	C66	C67	C68	C69	C70
Aquila Pin Name	MSP_6_RX_P	MSP_6_RX_N	GND	MSP_7_RX_P	MSP_7_RX_N	GND	MSP_8_RX_P	MSP_8_RX_N	GND	MSP_9_RX_P
Main use	SGMII5_RXP0	SGMII5_RXN0		SGMII6_RXP0	SGMII6_RXN0		SGMII7_RXP0	SGMII7_RXN0		SGMII2_RXP0
Primary	SERDES2_RX0_P	SERDES2_RX0_N		SERDES2_RX1_P	SERDES2_RX1_N		SERDES2_RX2_P	SERDES2_RX2_N		SERDES1_RX3_P
Mode 0	SGMII5_RXP0	SGMII5_RXN0		SGMII6_RXP0	SGMII6_RXN0		SGMII7_RXP0	SGMII7_RXN0		SGMII2_RXP0
Mode 1							SGMII1_RXP0	SGMII1_RXN0		PCIE0_RXP3
Mode 2										
Mode 3										PCIE2_RXP1
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 33: Alternate functions from C71 to C80

Pin	C71	C72	C73	C74	C75	C76	C77	C78	C79	C80
Aquila Pin Name	MSP_9_RX_N	GND	MSP_10_RX_P	MSP_10_RX_N	GND	MSP_11_RX_P	MSP_11_RX_N	GND	MSP_12_RX_P	MSP_12_RX_N
Main use	SGMII2_RXN0					PCIE0_RXP2	PCIE0_RXN2			
Primary	SERDES1_RX3_N		Wi-Fi Module	Wi-Fi Module		USB Bridge SS_RX_P	USB Bridge SS_RX_N		USB Bridge OC#	USB Bridge EN
Mode 0	SGMII2_RXN0					SGMII1_RXP0	SGMII1_RXN0			
Mode 1	PCIE0_RXN3					PCIE0_RXP2	PCIE0_RXN2			
Mode 2										
Mode 3	PCIE2_RXN1					PCIE2_RXP0	PCIE2_RXN0			
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 34: Alternate functions from C81 to C90

Pin	C81	C82	C83	C84	C85	C86	C87	C88	C89	C90
Aquila Pin Name	GND	MSP_13_RX_P	MSP_13_RX_N	GND	MSP_14_RX_P	MSP_14_RX_N	GND	MSP_15_RX_P	MSP_15_RX_N	GND
Main use		CSI2_RXP3	CSI2_RXN3		CSI2_RXP2	CSI2_RXN2		CSI2_RXCLKP	CSI2_RXCLKN	
Primary		CSI2_RXP3	CSI2_RXN3		CSI2_RXP2	CSI2_RXN2		CSI2_RXCLKP	CSI2_RXCLKN	
Mode 0		CSI2_RXP3	CSI2_RXN3		CSI2_RXP2	CSI2_RXN2		CSI2_RXCLKP	CSI2_RXCLKN	
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 35: Alternate functions from C91 to C100

Pin	C91	C92	C93	C94	C95	C96	C97	C98	C99	C100
Aquila Pin Name	MSP_16_RX_P	MSP_16_RX_N	GND	MSP_17_RX_P	MSP_17_RX_N	VCC	VCC	VCC	VCC	VCC
Main use	CSI2_RXP1	CSI2_RXN1		CSI2_RXP0	CSI2_RXN0					
Primary	CSI2_RXP1	CSI2_RXN1		CSI2_RXP0	CSI2_RXN0	VCC	VCC	VCC	VCC	VCC
Mode 0	CSI2_RXP1	CSI2_RXN1		CSI2_RXP0	CSI2_RXN0					
Mode 1										
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 36: Alternate functions from D1 to D10

Pin	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Aquila Pin Name	ADC_1	ADC_2	ADC_3	ADC_4	CTRL_RESET_MOCI#	CTRL_WAKE1_MICO#	I2C_1_SDA	I2C_1_SCL	SPI_1_CS	SPI_1_MISO
Main use	MCU_ADC0_AIN0	MCU_ADC0_AIN1	MCU_ADC0_AIN2	MCU_ADC0_AIN3			MCU_I2C0_SDA	MCU_I2C0_SCL	SPI2_CS1	SPI2_D0
Primary	MCU_ADC0_AIN0	MCU_ADC0_AIN1	MCU_ADC0_AIN2	MCU_ADC0_AIN3	Reset logic	WKUP_GPIO0_49	MCU_I2C0_SDA	MCU_I2C0_SCL	MCASP0_AXR11	MCASP0_AXR14
Mode 0	MCU_ADC0_AIN0	MCU_ADC0_AIN1	MCU_ADC0_AIN2	MCU_ADC0_AIN3		PMIC_WAKE1	MCU_I2C0_SDA	MCU_I2C0_SCL	MCAN7_TX	MCAN8_RX
Mode 1						MCU_EXT_REFCLK0			MCASP0_AXR11	MCASP0_AXR14
Mode 2						MCU_CPTS0_RFT_CLK				MCASP2_AXR4
Mode 3										MCASP0_ACLKR
Mode 4									DSS_FSYNC2	
Mode 5									GPMC0_A4	GPMC0_A7
Mode 6									RGMII1_TX_CTL	RGMII1_RD3
Mode 7	WKUP_GPIO0_71	WKUP_GPIO0_72	WKUP_GPIO0_73	WKUP_GPIO0_74		WKUP_GPIO0_49	WKUP_GPIO0_87	WKUP_GPIO0_65	GPIO0_39	GPIO0_42
Mode 8									RMII1_RX_ER	CLKOUT
Mode 9									EHRPWM3_B	EQEP0_A
Mode 10									SPI2_CS1	SPI2_D0
Mode 11									UART5_RXD	UART5_RTSn
Mode 12										RSVD_ASYNC7
Mode 13										UART7_TXD
Mode 14										PGD_VDD_MAIN_MEM_FLAGH
Mode 15									LED_DIO29	LED_CMD
Bootstrap										

Table 37: Alternate functions from D11 to D20

Pin	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
Aquila Pin Name	SPI_1_MOSI	SPI_1_CLK	GND	SPI_2_CLK	SPI_2_MISO	SPI_2_CS	SPI_2_MOSI	GND	UART_3_RXD	UART_3_TXD
Main use	SPI2_D1	SPI2_CLK		SPI0_CLK	SPI0_D0	SPI0_CS0	SPI0_D1		UART8_RXD	UART8_TXD
Primary	MCASP0_AXR15	MCASP0_AXR12		SPI0_CLK	SPI0_D0	SPI0_CS0	SPI0_D1		MCASP0_ACLKX	MCASP0_AFSX
Mode 0	MCAN9_TX	MCAN7_RX		SPI0_CLK	SPI0_D0	SPI0_CS0	SPI0_D1		MCAN5_TX	MCAN5_RX
Mode 1	MCASP0_AXR15	MCASP0_AXR12		UART1_CTSn	UART1_RTSn				MCASP0_ACLKX	MCASP0_AFSX
Mode 2				I2C2_SCL	I2C2_SDA				VOUT0_DATA15	VOUT0_DATA14
Mode 3	MCASP0_AFSR	MCASP2_ACLKR		MCASP3_AXR0	MCASP3_AXR1	MCASP3_ACLKX	MCASP3_AXR2		HYP0_RXFLCLK	HYP0_RXFLDAT
Mode 4		DSS_FSYNC3			DDR3_IO_PLL_TESTOUT0P	MCASP3_ACLKR	DDR3_IO_PLL_REFCLK_TEST0P			
Mode 5	GPMC0_A8	GPMC0_A5		EHRPWM2_A	EHRPWM3_A	EHRPWM0_A	EHRPWM4_A			
Mode 6	RGMII1_RX_CTL	RGMII1_RD1			DDR3_IO_PLL_TESTOUT1P		DDR3_IO_PLL_REFCLK_TEST1P		GPMC0_AD0	GPMC0_AD1
Mode 7	GPIO0_43	GPIO0_40		GPIO0_53	GPIO0_54	GPIO0_51	GPIO0_55		GPIO0_14	GPIO0_15
Mode 8	RMII1_TX_EN	RMII1_TXD0								
Mode 9	EQEP0_B	EHRPWM_SOCB				MCAN14_TX			EHRPWM_TZn_IN2	EHRPWM2_B
Mode 10	SPI2_D1	SPI2_CLK								
Mode 11	UART8_RXD	UART5_TXD		UART8_TXD	UART2_RXD		UART2_TXD		UART8_RXD	UART8_TXD
Mode 12					RSVD_ASYNC10	DP0_HPD	RSVD_ASYNC11			
Mode 13	I2C1_SCL			PGD_VDD_CPU_MEM_FLAGL	PGD_VDD_CPU_CORE_FLAGH		PGD_VDD_CPU_CORE_FLAGL			
Mode 14	PGD_VDD_MAIN_MEM_FLAGL	PGD_VDD_MAIN_CORE_FLAGH		VPU0_UART_TXD	VPU1_UART_RXD		VPU1_UART_TXD			
Mode 15	LED_OPCODE0	LED_DIO30				LED_OPCODE4			LED_DIO1	LED_DIO0
Bootstrap										

Table 38: Alternate functions from D21 to D30

Pin	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30
Aquila Pin Name	UART_4_RXD	UART_4_TXD	GPIO_01	GPIO_02	GPIO_03	GND	PCIE_2_CLK_P	PCIE_2_CLK_N	GND	PCIE_2_L0_TX_P
Main use	MCU_UART0_RXD	MCU_UART0_TXD	GPIO0_34	GPIO0_17	GPIO0_29					PCIE1_TXP0
Primary	MCU_OSPI1_D1	WKUP_GPIO0_10	MCASP0_AXR6	MCASP0_AXR1	MCAN2_TX		PCIE_REFCLK1_P_OUT	PCIE_REFCLK1_N_OUT		SERDES0_TX0_P
Mode 0	MCU_OSPI1_D1	MCU_EXT_REFCLK0	MCAN4_RX	MCAN6_RX	MCAN2_TX		PCIE_REFCLK1_P_OUT	PCIE_REFCLK1_N_OUT		
Mode 1		MCU_EXT_REFCLK0	MCASP0_AXR6	MCASP0_AXR1	MCASP2_AXR3					PCIE1_TXP0
Mode 2		MCU_UART0_TXD	VOUT0_VSYNC	VOUT0_DATA12	VOUT0_DATA0					
Mode 3		MCU_ADC_EXT_TRIGGER0	MCASP1_AFSR	HYP0_TXFLDAT						
Mode 4	MCU_UART0_RXD	MCU_CPTS0_RFT_CLK	VOUT0_VP0_VSYNC	OBSCLK1						HYP_TXP0
Mode 5	MCU_SPI1_CS1	MCU_SYSCLKOUT0	VOUT0_VP2_VSYNC		VOUT0_DATA18					
Mode 6			GPMC0_CLKOUT	GPMC0_AD3	GPMC0_WAIT0					
Mode 7	WKUP_GPIO0_35	WKUP_GPIO0_10	GPIO0_34	GPIO0_17	GPIO0_29					
Mode 8			SPI3_CS2	SPI2_CS3	SPI6_D1					
Mode 9			EHRPWM_TZn_IN4	EHRPWM0_SYNCO	EHRPWM1_B					
Mode 10			TRC_DATA20	TRC_DATA12	TRC_DATA3					
Mode 11			SPI5_D1	UART4_TXD	UART3_RXD					
Mode 12			GPMC0_FCLK_MUX		GPMC0_DIR					
Mode 13				SPI7_CS0	I2C5_SCL					
Mode 14				UART8_RTSn						
Mode 15		LED_DI34	LED_DIO24	LED_DIO2	LED_DIO12					
Bootstrap										

Table 39: Alternate functions from D31 to D40

Pin	D31	D32	D33	D34	D35	D36	D37	D38	D39	D40
Aquila Pin Name	PCIE_2_L0_TX_N	GND	PCIE_2_L1_TX_P	PCIE_2_L1_TX_N	GND	PCIE_1_CLK_P	PCIE_1_CLK_N	GND	PCIE_1_L0_TX_P	PCIE_1_L0_TX_N
Main use	PCIE1_TXN0		PCIE1_TXP1	PCIE1_TXN1					PCIE0_TXP0	PCIE0_TXN0
Primary	SERDES0_TX0_N		SERDES0_TX1_P	SERDES0_TX1_N		PCIE_REFCLK0_P_OUT	PCIE_REFCLK0_N_OUT		SERDES1_TX0_P	SERDES1_TX0_N
Mode 0						PCIE_REFCLK0_P_OUT	PCIE_REFCLK0_N_OUT		SGMII3_TXP0	SGMII3_TXN0
Mode 1	PCIE1_TXN0		PCIE1_TXP1	PCIE1_TXN1					PCIE0_TXP0	PCIE0_TXN0
Mode 2										
Mode 3										
Mode 4	HYP_TXN0		HYP_TXP1	HYP_TXN1						
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 40: Alternate functions from D41 to D50

Pin	D41	D42	D43	D44	D45	D46	D47	D48	D49	D50
Aquila Pin Name	GND	PCIE_1_L1_TX_P	PCIE_1_L1_TX_N	GND	MSP_1_TX_P	MSP_1_TX_N	GND	MSP_2_TX_P	MSP_2_TX_N	GND
Main use		PCIE0_TXP1	PCIE0_TXN1		PCIE3_TXP0	PCIE3_TXN0		PCIE_REFCLK3_P_OUT	PCIE_REFCLK3_N_OUT	
Primary		SERDES1_TX1_P	SERDES1_TX1_N		SERDES0_TX2_P	SERDES0_TX2_N		PCIE_REFCLK3_P_OUT	PCIE_REFCLK3_N_OUT	
Mode 0		SGMII4_TXP0	SGMII4_TXN0					PCIE_REFCLK3_P_OUT	PCIE_REFCLK3_N_OUT	
Mode 1		PCIE0_TXP1	PCIE0_TXN1		PCIE1_TXP2	PCIE1_TXN2				
Mode 2					USB0_SSTX1P	USB0_SSTX1N				
Mode 3					PCIE3_TXP0	PCIE3_TXN0				
Mode 4					HYP_TXP2	HYP_TXN2				
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 41: Alternate functions from D51 to D60

Pin	D51	D52	D53	D54	D55	D56	D57	D58	D59	D60
Aquila Pin Name	MSP_3_TX_P	MSP_3_TX_N	GND	MSP_4_TX_P	MSP_4_TX_N	GND	MSP_5_TX_P	MSP_5_TX_N	GND	MSP_6_TX_P
Main use				MCU_ADC0_AIN4	MCU_ADC0_AIN5					SGMII5_TXP0
Primary	clk32_out	phy-eth-1588-sof		MCU_ADC0_AIN4	MCU_ADC0_AIN5		CTRL_MCU_RESET_MOCI#	DSCRT_PWRGRP_IRQn		SERDES2_TX0_P
Mode 0		TIMER_IO1		MCU_ADC0_AIN4	MCU_ADC0_AIN5					SGMII5_TXP0
Mode 1		ECAP2_IN_APWM_OUT								
Mode 2		OBSCLK0								
Mode 3		DDR0_IO_PLL_REFCLK_TEST0F								
Mode 4		DDR0_IO_PLL_REFCLK_TEST1F								
Mode 5		UART3_TXD								
Mode 6		USB0_DRVVBUS								
Mode 7		GPIO0_59		WKUP_GPIO0_75	WKUP_GPIO0_76					
Mode 8		MMC1_SDWP								
Mode 9		MCAN13_RX								
Mode 10		DDR1_IO_PLL_REFCLK_TEST0F								
Mode 11		DDR1_IO_PLL_REFCLK_TEST1F								
Mode 12		DDR2_IO_PLL_REFCLK_TEST0F								
Mode 13		I2C6_SCL								
Mode 14		DDR2_IO_PLL_REFCLK_TEST1F								
Mode 15		OBSCLK0								
Bootstrap										

Table 42: Alternate functions from D61 to D70

Pin	D61	D62	D63	D64	D65	D66	D67	D68	D69	D70
Aquila Pin Name	MSP_6_TX_N	GND	MSP_7_TX_P	MSP_7_TX_N	GND	MSP_8_TX_P	MSP_8_TX_N	GND	MSP_9_TX_P	MSP_9_TX_N
Main use	SGMII5_TXN0		SGMII6_TXP0	SGMII6_TXN0		SGMII7_TXP0	SGMII7_TXN0		SGMII2_TXP0	SGMII2_TXN0
Primary	SERDES2_TX0_N		SERDES2_TX1_P	SERDES2_TX1_N		SERDES2_TX2_P	SERDES2_TX2_N		SERDES1_TX3_P	SERDES1_TX3_N
Mode 0	SGMII5_TXN0		SGMII6_TXP0	SGMII6_TXN0		SGMII7_TXP0	SGMII7_TXN0		SGMII2_TXP0	SGMII2_TXN0
Mode 1						SGMII1_TXP0	SGMII1_TXN0		PCIE0_TXP3	PCIE0_TXN3
Mode 2										
Mode 3									PCIE2_TXP1	PCIE2_TXN1
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 43: Alternate functions from D71 to D80

Pin	D71	D72	D73	D74	D75	D76	D77	D78	D79	D80
Aquila Pin Name	GND	MSP_10_TX_P	MSP_10_TX_N	GND	MSP_11_TX_P	MSP_11_TX_N	GND	MSP_12_TX_P	MSP_12_TX_N	GND
Main use					PCIE0_TXP2	PCIE0_TXN2		PCIE_REFCLK2_P_OUT	PCIE_REFCLK2_N_OUT	
Primary		wifi_laa_tx_en	wifi_wl_tx_en		USB Bridge SS_TX_P	USB Bridge SS_TX_N		USB Bridge DP	USB Bridge DN	
Mode 0					SGMII1_TXP0	SGMII1_TXN0		PCIE_REFCLK2_P_OUT	PCIE_REFCLK2_N_OUT	
Mode 1					PCIE0_TXP2	PCIE0_TXN2				
Mode 2										
Mode 3					PCIE2_TXP0	PCIE2_TXN0				
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 44: Alternate functions from D81 to D90

Pin	D81	D82	D83	D84	D85	D86	D87	D88	D89	D90
Aquila Pin Name	MSP_13_TX_P	MSP_13_TX_N	GND	MSP_14_TX_P	MSP_14_TX_N	GND	MSP_15_TX_P	MSP_15_TX_N	GND	MSP_16_TX_P
Main use	DSI1_TXP0	DSI1_TXN0		DSI1_TXP1	DSI1_TXN1		DSI1_TXCLKP	DSI1_TXCLKN		DSI1_TXP2
Primary	DSI1_TXP0	DSI1_TXN0		DSI1_TXP1	DSI1_TXN1		DSI1_TXCLKP	DSI1_TXCLKN		DSI1_TXP2
Mode 0	DSI1_TXP0	DSI1_TXN0		DSI1_TXP1	DSI1_TXN1		DSI1_TXCLKP	DSI1_TXCLKN		DSI1_TXP2
Mode 1	CSI1_TXP0	CSI1_TXN0		CSI1_TXP1	CSI1_TXN1		CSI1_TXCLKP	CSI1_TXCLKN		CSI1_TXP2
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

Table 45: Alternate functions from D91 to D100

Pin	D91	D92	D93	D94	D95	D96	D97	D98	D99	D100
Aquila Pin Name	MSP_16_TX_N	GND	MSP_17_TX_P	MSP_17_TX_N	VCC	VCC	VCC	VCC	VCC	VCC
Main use	DSI1_TXN2		DSI1_TXP3	DSI1_TXN3						
Primary	DSI1_TXN2		DSI1_TXP3	DSI1_TXN3	VCC	VCC	VCC	VCC	VCC	VCC
Mode 0	DSI1_TXN2		DSI1_TXP3	DSI1_TXN3						
Mode 1	CSI1_TXN2		CSI1_TXP3	CSI1_TXN3						
Mode 2										
Mode 3										
Mode 4										
Mode 5										
Mode 6										
Mode 7										
Mode 8										
Mode 9										
Mode 10										
Mode 11										
Mode 12										
Mode 13										
Mode 14										
Mode 15										
Bootstrap										

5 Interface Description

5.1 SDIO/SD/MMC

Table 46: SD Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A1	SD_1_CD#	TIMER_IO0	ALT8	MMC1_SDCD	I/O	Card detect input
A2	SD_1_D1	MMC1_DAT1	ALT0	MMC1_DAT1	I/O	Data line 1
A3	SD_1_D0	MMC1_DAT0	ALT0	MMC1_DAT0	I/O	Data line 0
A5	SD_1_CLK	MMC1_CLK	ALT0	MMC1_CLK	I/O	SD clock output
A6	SD_1_PWR_EN	SPI0_CS1	ALT7	MMC1_PWR_EN	I/O	SD power enable
A7	SD_1_CMD	MMC1_CMD	ALT0	MMC1_CMD	I/O	SD command line
A8	SD_1_D3	MMC1_DAT3	ALT0	MMC1_DAT3	I/O	Data line 3
A10	SD_1_D2	MMC1_DAT2	ALT0	MMC1_DAT2	I/O	Data line 2

5.2 OSPI/QSPI

Table 47: OSPI QSPI Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description	Mode
B60	QSPI_1_IO3	MCU_OSPI0_D3	ALT0	MCU_OSPI0_D3	I/O	Data bit 3 / IO3.	OSPI x8 & QSPI x4
B61	QSPI_1_IO2	MCU_OSPI0_D2	ALT0	MCU_OSPI0_D2	I/O	Data bit 2 / IO2.	OSPI x8 & QSPI x4
B62	QSPI_1_CS2#	MCU_OSPI0_CSn1	ALT0	MCU_OSPI0_CSn1	I/O	Chip select 1 (active low).	OSPI & QSPI
B63	QSPI_1_DQS	MCU_OSPI0_DQS	ALT0	MCU_OSPI0_DQS	I/O	Data strobe (DQS/RWDS).	OSPI DDR (not used in legacy QSPI)
B65	QSPI_1_SCK	MCU_OSPI0_CLK	ALT0	MCU_OSPI0_CLK	I/O	Serial clock.	OSPI & QSPI
B66	QSPI_1_CS1#	MCU_OSPI0_CSn0	ALT0	MCU_OSPI0_CSn0	I/O	Chip select 0 (active low).	OSPI & QSPI
B67	QSPI_1_IO1	MCU_OSPI0_D1	ALT0	MCU_OSPI0_D1	I/O	Data bit 1 / IO1.	OSPI x8 & QSPI x4
B68	QSPI_1_IO0	MCU_OSPI0_D0	ALT0	MCU_OSPI0_D0	I/O	Data bit 0 / IO0.	OSPI x8 & QSPI x4
B70	OSPI_1_IO4	MCU_OSPI0_D4	ALT0	MCU_OSPI0_D4	I/O	Data bit 4 / IO4.	OSPI x8 only
B71	OSPI_1_IO5	MCU_OSPI0_D5	ALT0	MCU_OSPI0_D5	I/O	Data bit 5 / IO5.	OSPI x8 only
B72	OSPI_1_IO6	MCU_OSPI0_D6	ALT0	MCU_OSPI0_D6	I/O	Data bit 6 / IO6.	OSPI x8 only
B73	OSPI_1_IO7	MCU_OSPI0_D7	ALT0	MCU_OSPI0_D7	I/O	Data bit 7 / IO7.	OSPI x8 only

5.3 PCIe

Table 48: PCIE1 Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C37	PCIE_1_CLKREQ#	-	-	-	I/O	PCIe 1 clock request (bidirectional, active-low). Connected to GPIO expander.[1]
D39	PCIE_1_L0_TX_P	SERDES1_TX0_P	ALT1	PCIE0_TXP0	O	PCIe transmit lane 0 positive (SoC → device).
D40	PCIE_1_L0_TX_N	SERDES1_TX0_N	ALT1	PCIE0_TXN0	O	PCIe transmit lane 0 negative (SoC → device).
D42	PCIE_1_L1_TX_P	SERDES1_TX1_P	ALT1	PCIE0_TXP1	O	PCIe transmit lane 1 positive (SoC → device).
D43	PCIE_1_L1_TX_N	SERDES1_TX1_N	ALT1	PCIE0_TXN1	O	PCIe transmit lane 1 negative (SoC → device).
C40	PCIE_1_L0_RX_P	SERDES1_RX0_P	ALT1	PCIE0_RXP0	I	PCIe receive lane 0 positive (device → SoC).
C41	PCIE_1_L0_RX_N	SERDES1_RX0_N	ALT1	PCIE0_RXN0	I	PCIe receive lane 0 negative (device → SoC).
C43	PCIE_1_L1_RX_P	SERDES1_RX1_P	ALT1	PCIE0_RXP1	I	PCIe receive lane 1 positive (device → SoC).
C44	PCIE_1_L1_RX_N	SERDES1_RX1_N	ALT1	PCIE0_RXN1	I	PCIe receive lane 1 negative (device → SoC).
D37	PCIE_1_CLK_N	PCIE_REFCLK0_N_OUT	ALT0	PCIE_REFCLK0_N_OUT	O	PCIe reference clock negative (100 MHz).
D36	PCIE_1_CLK_P	PCIE_REFCLK0_P_OUT	ALT0	PCIE_REFCLK0_P_OUT	O	PCIe reference clock positive (100 MHz).
C38	PCIE_1_RESET#	MCASP0_AXR4	ALT1	MCASP0_AXR4	I/O	PCIe reset (active-low) output from SoC.

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default

Table 49: PCIE2 Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C34	PCIE_2_CLKREQ#	-	-	-	I/O	PCIe2 clock request (bidirectional, active-low). Connected to GPIO expander[1]
D30	PCIE_2_L0_TX_P	SERDES0_TX0_P	ALT1	PCIE1_TXP0	O	PCIe transmit lane 0 positive (SoC → device).
D31	PCIE_2_L0_TX_N	SERDES0_TX0_N	ALT0	PCIE1_TXN0	O	PCIe transmit lane 0 negative (SoC → device).
D33	PCIE_2_L1_TX_P	SERDES0_TX1_P	ALT1	PCIE1_TXP1	O	PCIe transmit lane 1 positive (SoC → device).
D34	PCIE_2_L1_TX_N	SERDES0_TX1_N	ALT1	PCIE1_TXN1	O	PCIe transmit lane 1 negative (SoC → device).
C28	PCIE_2_L0_RX_P	SERDES0_RX0_P	ALT1	PCIE1_RXP0	I	PCIe receive lane 0 positive (device → SoC).
C29	PCIE_2_L0_RX_N	SERDES0_RX0_N	ALT1	PCIE1_RXN0	I	PCIe receive lane 0 negative (device → SoC).
C31	PCIE_2_L1_RX_P	SERDES0_RX1_P	ALT1	PCIE1_RXP1	I	PCIe receive lane 1 positive (device → SoC).

Continued on next page

Table 49: PCIE2 Signal Pins (Continued)

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C32	PCIE_2_L1_RX_N	SERDES0_RX1_N	ALT1	PCIE1_RXN1	I	PCIe receive lane 1 negative (device → SoC).
D28	PCIE_2_CLK_N	PCIE_REFCLK1_N_OUT	ALT0	PCIE_REFCLK1_N_OUT	O	PCIe reference clock negative.
D27	PCIE_2_CLK_P	PCIE_REFCLK1_P_OUT	ALT0	PCIE_REFCLK1_P_OUT	O	PCIe reference clock positive.
C35	PCIE_2_RESET#	MCASP0_AXR13	ALT1	MCASP0_AXR13	I/O	PCIe reset (active-low) output from SoC.

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default

Table 50: PCIE3 Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C76	MSP_11_RX_P	SERDES1_RX2_P	ALT1	PCIE0_RXP2	I	PCIe receive lane 2 positive
C77	MSP_11_RX_N	SERDES1_RX2_N	ALT1	PCIE0_RXN2	I	PCIe receive lane 2 negative
D75	MSP_11_TX_P	SERDES1_TX2_P	ALT1	PCIE0_TXP2	O	PCIe transmit lane 2 positive
D76	MSP_11_TX_N	SERDES1_TX2_N	ALT1	PCIE0_TXN2	O	PCIe transmit lane 2 negative
D78	MSP_12_TX_P	PCIE_REFCLK2_P_OUT	ALT0	PCIE_REFCLK2_P_OUT	O	PCIe reference clock positive
D79	MSP_12_TX_N	PCIE_REFCLK2_N_OUT	ALT0	PCIE_REFCLK2_N_OUT	O	PCIe reference clock negative
C79	MSP_12_RX_P	-	-	-	I	PCIe 3 clock request (bidirectional, active-low). Connected to GPIO expander.[1]
C80	MSP_12_RX_N	-	-	-	I	PCIe reset (active-low). Connected to a GPIO Expander[2]

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default
[2] Connected to the TI-TCA6408ARSVR GPIO Expander B

Table 51: PCIE4 Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C46	MSP_1_RX_P	SERDES0_RX2_P	ALT3	PCIE3_RXP0	I	PCIe receive lane 0 positive
C47	MSP_1_RX_N	SERDES0_RX2_N	ALT3	PCIE3_RXN0	I	PCIe receive lane 0 negative
D45	MSP_1_TX_P	SERDES0_TX2_P	ALT3	PCIE3_TXP0	O	PCIe transmit lane 0 positive
D46	MSP_1_TX_N	SERDES0_TX2_N	ALT3	PCIE3_TXN0	O	PCIe transmit lane 0 negative
D48	MSP_2_TX_P	PCIE_REFCLK3_P_OUT	ALT0	PCIE_REFCLK3_P_OUT	O	PCIe reference clock positive
D49	MSP_2_TX_N	PCIE_REFCLK3_N_OUT	ALT0	PCIE_REFCLK3_N_OUT	O	PCIe reference clock negative
C49	MSP_2_RX_P	-	-	-	I	PCIe 4 clock request (bidirectional, active-low). Connected to GPIO expander.[1]
C50	MSP_2_RX_N	-	-	-	I	PCIe reset (active-low). Connected to the GPIO Expander[2]

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default
[2] Connected to the TI-TCA6408ARSVR GPIO Expander B

5.4 Ethernet

5.4.1 ETH_1 (PHY)

The following signals are connected to a TI-DP83867IIRGZR Gigabit Ethernet Transceiver.

Table 52: Ethernet 1 - PHY

X1 pin	Aquila specification signal name	I/O	Description
A88	ETH_1_MDI0_P	I/O	Positive differential MDI signal
A89	ETH_1_MDI0_N	I/O	Negative differential MDI signal
A91	ETH_1_MDI1_P	I/O	Positive differential MDI signal
A92	ETH_1_MDI1_N	I/O	Negative differential MDI signal
A94	ETH_1_MDI2_P	I/O	Positive differential MDI signal
A95	ETH_1_MDI2_N	I/O	Negative differential MDI signal
A97	ETH_1_MDI3_P	I/O	Positive differential MDI signal
A98	ETH_1_MDI3_N	I/O	Negative differential MDI signal
A99	ETH_1_LED2	O	Link/activity LED output from on-module Ethernet PHY.
A100	ETH_1_LED1	O	Speed/activity LED output from on-module Ethernet PHY.

5.4.2 ETH_2 (SGMII)

Table 53: Ethernet 2 - SGMII

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C64	MSP_7_RX_P	SERDES2_RX1_P	ALT0	SGMII6_RXP0	I	SGMII ch.6 RX positive.
C65	MSP_7_RX_N	SERDES2_RX1_N	ALT0	SGMII6_RXN0	I	SGMII ch.6 RX negative.
D63	MSP_7_TX_P	SERDES2_TX1_P	ALT0	SGMII6_TXP0	O	SGMII ch.6 TX positive.
D64	MSP_7_TX_N	SERDES2_TX1_N	ALT0	SGMII6_TXN0	O	SGMII ch.6 TX negative.
C67	MSP_8_RX_P	SERDES2_RX2_P	ALT0	SGMII7_RXP0	I	SGMII ch.7 RX positive.
C68	MSP_8_RX_N	SERDES2_RX2_N	ALT0	SGMII7_RXN0	I	SGMII ch.7 RX negative.
D66	MSP_8_TX_P	SERDES2_TX2_P	ALT0	SGMII7_TXP0	O	SGMII ch.7 TX positive.
D67	MSP_8_TX_N	SERDES2_TX2_N	ALT0	SGMII7_TXN0	O	SGMII ch.7 TX negative.
C70	MSP_9_RX_P	SERDES1_RX3_P	ALT0	SGMII2_RXP0	I	SGMII ch.2 RX positive.
C71	MSP_9_RX_N	SERDES1_RX3_N	ALT0	SGMII2_RXN0	I	SGMII ch.2 RX negative.
D69	MSP_9_TX_P	SERDES1_TX3_P	ALT0	SGMII2_TXP0	O	SGMII ch.2 TX positive.
D70	MSP_9_TX_N	SERDES1_TX3_N	ALT0	SGMII2_TXN0	O	SGMII ch.2 TX negative.
B89	ETH_2_XGMII_MDIO	MCASP2_AXR0	ALT4	MDIO1_MDIO	I/O	MDIO data to ext. PHY.
B90	ETH_2_XGMII_MDC	MCASP2_AFSX	ALT4	MDIO1_MDC	I/O	MDIO management clock.

5.5 Wifi/Bluetooth

The Aquila AM69/TDA4 is available with optional on-module Wi-Fi and Bluetooth interfaces. The Aquila AM69/TDA4 WB versions have a SILEX-SX-PCEBE-SMT Wi-Fi/Bluetooth module, which supports 2.4Ghz/5Ghz/6Ghz and Blueteooth 5.4. It is connected via the PCIe4 interface for high-speed Wi-Fi data transfer, while the

Bluetooth signals are routed separately through a USB interface.

Table 54: Wi-fi and Bluetooth Signal Pins

Aquila specification signal name	SX-PCEBE-SMT Pin name	SoC ball name	Description
Wi-Fi interface			
PCIe_WIFI_TX_P	HMT_PCIE_RXP0	PCIE3_TXP0	
PCIe_WIFI_TX_N	HMT_PCIE_RXN0	PCIE3_TXN0	
PCIe_WIFI_RX_P	HMT_PCIE_TXP0	PCIE3_RXP0	
PCIe_WIFI_RX_N	HMT_PCIE_TXN0	PCIE3_RXN0	
PCIe_REFCLK_WIFI_P	HMT_PCIE_REFCLKP	PCIE_REFCLK3_P_OUT	
PCIe_REFCLK_WIFI_N	HMT_PCIE_REFCLKN	PCIE_REFCLK3_N_OUT	
PCIe_WAKE_WIFI#	PEWAKE0_L	WKUP_GPIO_80	10 kΩ pull-up resistor
PCIe_4_CLKREQ#	CLKREQ0_L	–[1]	
PCIe_4_RESET#	PERST0_L	–[2]	
Bluetooth interface			
USB_WIFI_D_P	BT_USB_DP	–[3]	
USB_WIFI_D_N	BT_USB_DM	–[3]	
Control signals			
WIFI_DISABLE#	WL_EN	–[2]	10 kΩ pull-up resistor
BT_DISABLE#	WL_DISABLE2_L	–[2]	10 kΩ pull-up resistor

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default
[2] Connected to the TI-TCA6408ARSVR GPIO Expander B
[3] Available through the on-module USB hub (TUSB7320IRKMR).

5.6 USB

Table 55: USB1 - DRP

X1 pin	Aquila specification signal name	SoC ball name	I/O	Description
A70	USB_1_D_P	USB0_DP	I/O	USB2.0 differential data positive (DP).
A71	USB_1_D_N	USB0_DM	I/O	USB2.0 differential data negative (DM).
A62	USB_1_SSRX1_P	-	I	USB3.x SuperSpeed RX0 positive (via on-module mux).[1]
A61	USB_1_SSRX1_N	-	I	USB3.x SuperSpeed RX0 negative (via on-module mux).[1]
A64	USB_1_SSTX1_P	-	O	USB3.x SuperSpeed TX0 positive (via on-module mux).[1]
A65	USB_1_SSTX1_N	-	O	USB3.x SuperSpeed TX0 negative (via on-module mux).[1]
A74	USB_1_SSRX2_P	-	I	USB3.x SuperSpeed RX1 positive (2nd lane, via mux).[1]
A73	USB_1_SSRX2_N	-	I	USB3.x SuperSpeed RX1 negative (2nd lane, via mux).[1]
A76	USB_1_SSTX2_P	-	O	USB3.x SuperSpeed TX1 positive (2nd lane, via mux).[1]

Continued on next page

Table 55: USB1 - DRP (Continued)

X1 pin	Aquila specification signal name	SoC ball name	I/O	Description
A77	USB_1_SSTX2_N	-	O	USB3.x SuperSpeed TX1 negative (2nd lane, via mux).[1]
A67	USB_1_SBU2	–	–	Sideband use (not connected).
A68	USB_1_SBU1	–	–	Sideband use (not connected).
B76	USB_1_VBUS	USB0_VBUS	-	Use this pin to detect if VBUS is present.

[1] Connected to the TI-TMUXHS4212IRKS USB Differential Multiplexer

The following signals are connected to a TI-TUSB7320IRKMR USB 3.0 Host Controller

Table 56: USB2 - Host Bridge

X1 Pin	Aquila specification signal name	I/O	Description
A86	USB_2_D_P	I/O	USB2.0 differential data positive (DP) via on-module USB bridge.
A85	USB_2_D_N	I/O	USB2.0 differential data negative (DM) via on-module USB bridge.
A82	USB_2_SSRX1_N	I	USB3.x SuperSpeed RX0 negative via on-module USB bridge.
A83	USB_2_SSRX1_P	I	USB3.x SuperSpeed RX0 positive via on-module USB bridge.
A79	USB_2_SSTX1_N	O	USB3.x SuperSpeed TX0 negative via on-module USB bridge.
A80	USB_2_SSTX1_P	O	USB3.x SuperSpeed TX0 positive via on-module USB bridge.
B78	USB_2_OC#	O	USB3.x Overcurrent protection
B80	USB_2_EN	O	USB3.x Power Enable

5.7 Display

5.7.1 DisplayPort

Table 57: Displayport - Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A46	DP_1_AUX-	DP0_AUXN	ALT0	DP0_AUXN	I/O	DisplayPort AUX differential negative.
A47	DP_1_AUX+	DP0_AUXP	ALT0	DP0_AUXP	I/O	DisplayPort AUX differential positive.
A49	DP_1_LANE3-	SERDES4_TX3_N	ALT0	DP0_TXN3	O	DisplayPort main link lane 3 negative.
A50	DP_1_LANE3+	SERDES4_TX3_P	ALT0	DP0_TXP3	O	DisplayPort main link lane 3 positive.
A52	DP_1_LANE2-	SERDES4_TX2_N	ALT0	DP0_TXN2	O	DisplayPort main link lane 2 negative.
A53	DP_1_LANE2+	SERDES4_TX2_P	ALT0	DP0_TXP2	O	DisplayPort main link lane 2 positive.
A55	DP_1_LANE1-	SERDES4_TX1_N	ALT0	DP0_TXN1	O	DisplayPort main link lane 1 negative.
A56	DP_1_LANE1+	SERDES4_TX1_P	ALT0	DP0_TXP1	O	DisplayPort main link lane 1 positive.
A58	DP_1_LANE0-	SERDES4_TX0_N	ALT0	DP0_TXN0	O	DisplayPort main link lane 0 negative.
A59	DP_1_LANE0+	SERDES4_TX0_P	ALT0	DP0_TXP0	O	DisplayPort main link lane 0 positive.
B59	DP_1_HPD	MCAN14_TX	ALT13	DP0_HPD	I/O	Hot-plug detect input from DisplayPort sink.

5.7.2 MIPI-DSI

Table 58: MIPI DSI 0 Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A43	DSI_1_D0_N	DSI0_TXN0	ALT0	DSI0_TXN0	I/O	MIPI-DSI0 data lane 0 negative.
A44	DSI_1_D0_P	DSI0_TXP0	ALT0	DSI0_TXP0	I/O	MIPI-DSI0 data lane 0 positive.
A40	DSI_1_D1_N	DSI0_TXN1	ALT0	DSI0_TXN1	O	MIPI-DSI0 data lane 1 negative.
A41	DSI_1_D1_P	DSI0_TXP1	ALT0	DSI0_TXP1	O	MIPI-DSI0 data lane 1 positive.
A37	DSI_1_CLK_N	DSI0_TXCLKN	ALT0	DSI0_TXCLKN	O	MIPI-DSI0 differential clock negative.
A38	DSI_1_CLK_P	DSI0_TXCLKP	ALT0	DSI0_TXCLKP	O	MIPI-DSI0 differential clock positive.
A34	DSI_1_D2_N	DSI0_TXN2	ALT0	DSI0_TXN2	O	MIPI-DSI0 data lane 2 negative.
A35	DSI_1_D2_P	DSI0_TXP2	ALT0	DSI0_TXP2	O	MIPI-DSI0 data lane 2 positive.
A31	DSI_1_D3_N	DSI0_TXN3	ALT0	DSI0_TXN3	O	MIPI-DSI0 data lane 3 negative.
A32	DSI_1_D3_P	DSI0_TXP3	ALT0	DSI0_TXP3	O	MIPI-DSI0 data lane 3 positive.

Table 59: MIPI DSI 1 Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D81	MSP_13_TX_P	DSI1_TXP0	ALT0	DSI1_TXP0	I/O	MIPI-DSI1 data lane 0 positive.
D82	MSP_13_TX_N	DSI1_TXN0	ALT0	DSI1_TXN0	I/O	MIPI-DSI1 data lane 0 negative.
D84	MSP_14_TX_P	DSI1_TXP1	ALT0	DSI1_TXP1	O	MIPI-DSI1 data lane 1 positive.
D85	MSP_14_TX_N	DSI1_TXN1	ALT0	DSI1_TXN1	O	MIPI-DSI1 data lane 1 negative.
D87	MSP_15_TX_P	DSI1_TXCLKP	ALT0	DSI1_TXCLKP	O	MIPI-DSI1 differential clock positive.
D88	MSP_15_TX_N	DSI1_TXCLKN	ALT0	DSI1_TXCLKN	O	MIPI-DSI1 differential clock negative.
D90	MSP_16_TX_P	DSI1_TXP2	ALT0	DSI1_TXP2	O	MIPI-DSI1 data lane 2 positive.
D91	MSP_16_TX_N	DSI1_TXN2	ALT0	DSI1_TXN2	O	MIPI-DSI1 data lane 2 negative.
D93	MSP_17_TX_P	DSI1_TXP3	ALT0	DSI1_TXP3	O	MIPI-DSI1 data lane 3 positive.
D94	MSP_17_TX_N	DSI1_TXN3	ALT0	DSI1_TXN3	O	MIPI-DSI1 data lane 3 negative.

5.8 MIPI-CSI

Table 60: MIPI CSI Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A16	CSI_1_D3_P	CSI0_RXP3	ALT0	CSI0_RXP3	I	CSI0 data lane 3 positive.
A17	CSI_1_D3_N	CSI0_RXN3	ALT0	CSI0_RXN3	I	CSI0 data lane 3 negative.
A19	CSI_1_D2_P	CSI0_RXP2	ALT0	CSI0_RXP2	I	CSI0 data lane 2 positive.
A20	CSI_1_D2_N	CSI0_RXN2	ALT0	CSI0_RXN2	I	CSI0 data lane 2 negative.
A25	CSI_1_D1_P	CSI0_RXP1	ALT0	CSI0_RXP1	I	CSI0 data lane 1 positive.
A26	CSI_1_D1_N	CSI0_RXN1	ALT0	CSI0_RXN1	I	CSI0 data lane 1 negative.
A28	CSI_1_D0_P	CSI0_RXP0	ALT0	CSI0_RXP0	I	CSI0 data lane 0 positive.

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Table 60: MIPI CSI Signal Pins (Continued)

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
A29	CSI_1_D0_N	CSI0_RXN0	ALT0	CSI0_RXN0	I	CSI0 data lane 0 negative.
A22	CSI_1_CLK_P	CSI0_RXCLKP	ALT0	CSI0_RXCLKP	I	CSI0 reference clock positive.
A23	CSI_1_CLK_N	CSI0_RXCLKN	ALT0	CSI0_RXCLKN	I	CSI0 reference clock negative.
B2	CSI_2_D3_P	CSI1_RXP3	ALT0	CSI1_RXP3	I	CSI1 data lane 3 positive.
B3	CSI_2_D3_N	CSI1_RXN3	ALT0	CSI1_RXN3	I	CSI1 data lane 3 negative.
B5	CSI_2_D2_P	CSI1_RXP2	ALT0	CSI1_RXP2	I	CSI1 data lane 2 positive.
B6	CSI_2_D2_N	CSI1_RXN2	ALT0	CSI1_RXN2	I	CSI1 data lane 2 negative.
B11	CSI_2_D1_P	CSI1_RXP1	ALT0	CSI1_RXP1	I	CSI1 data lane 1 positive.
B12	CSI_2_D1_N	CSI1_RXN1	ALT0	CSI1_RXN1	I	CSI1 data lane 1 negative.
B14	CSI_2_D0_P	CSI1_RXP0	ALT0	CSI1_RXP0	I	CSI1 data lane 0 positive.
B15	CSI_2_D0_N	CSI1_RXN0	ALT0	CSI1_RXN0	I	CSI1 data lane 0 negative.
B8	CSI_2_CLK_P	CSI1_RXCLKP	ALT0	CSI1_RXCLKP	I	CSI2 reference clock positive.
B9	CSI_2_CLK_N	CSI1_RXCLKN	ALT0	CSI1_RXCLKN	I	CSI2 reference clock negative.
C82	MSP_13_RX_P	CSI2_RXP3	ALT0	CSI2_RXP3	I	CSI2 data lane 3 positive.
C83	MSP_13_RX_N	CSI2_RXN3	ALT0	CSI2_RXN3	I	CSI2 data lane 3 negative.
C85	MSP_14_RX_P	CSI2_RXP2	ALT0	CSI2_RXP2	I	CSI2 data lane 2 positive.
C86	MSP_14_RX_N	CSI2_RXN2	ALT0	CSI2_RXN2	I	CSI2 data lane 2 negative.
C91	MSP_16_RX_P	CSI2_RXP1	ALT0	CSI2_RXP1	I	CSI2 data lane 1 positive.
C92	MSP_16_RX_N	CSI2_RXN1	ALT0	CSI2_RXN1	I	CSI2 data lane 1 negative.
C94	MSP_17_RX_P	CSI2_RXP0	ALT0	CSI2_RXP0	I	CSI2 data lane 0 positive.
C95	MSP_17_RX_N	CSI2_RXN0	ALT0	CSI2_RXN0	I	CSI2 data lane 0 negative.
C88	MSP_15_RX_P	CSI2_RXCLKP	ALT0	CSI2_RXCLKP	I	CSI2 reference clock positive.
C89	MSP_15_RX_N	CSI2_RXCLKN	ALT0	CSI2_RXCLKN	I	CSI2 reference clock negative.

5.9 CAN

Table 61: CAN Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B48	CAN_1_TX	MCASP1_AXR4	ALT0	MCAN10_TX	O	Transmit data for CAN1 (MCAN index per full pinmux).
B49	CAN_1_RX	MCASP1_ACLKX	ALT0	MCAN10_RX	I	Receive data for CAN1 (MCAN index per full pinmux).
B50	CAN_2_TX	MCU_MCAN0_TX	ALT0	MCU_MCAN0_TX	O	Transmit data for CAN2 (MCU domain).
B51	CAN_2_RX	MCU_MCAN0_RX	ALT0	MCU_MCAN0_RX	I	Receive data for CAN2 (MCU domain).
B53	CAN_3_TX	MCAN13_TX	ALT0	MCAN13_TX	O	Transmit data for CAN3.
B54	CAN_3_RX	MCAN13_RX	ALT0	MCAN13_RX	I	Receive data for CAN3.
B55	CAN_4_TX	WKUP_GPIO0_4	ALT0	MCU_MCAN1_TX	O	Transmit data for CAN4 (requires mux to MCAN, per full pinmux).

Continued on next page

Table 61: CAN Signal Pins (Continued)

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B56	CAN_4_RX	WKUP_GPIO0_5	ALT0	MCU_MCAN1_RX	I	Receive data for CAN4 (requires mux to MCAN, per full pinmux).

5.10 GPIO

5.10.1 Always Compatible

Table 62: GPIO Pins - Always Compatible

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D23	GPIO_01	MCASP0_AXR6	ALT7	GPIO0_34	I/O	General-purpose I/O.
D24	GPIO_02	MCASP0_AXR1	ALT7	GPIO0_17	I/O	General-purpose I/O.
D25	GPIO_03	MCAN2_TX	ALT7	GPIO0_29	I/O	General-purpose I/O.
C20	GPIO_04	MCU_OSPI0_LBCLKO	ALT7	WKUP_GPIO0_17	I/O	General-purpose I/O.
C21	GPIO_05	MCU_OSPI0_CSn2	ALT7	WKUP_GPIO0_29	I/O	General-purpose I/O.
C22	GPIO_06	MCU_OSPI0_CSn3	ALT7	WKUP_GPIO0_30	I/O	General-purpose I/O.
C23	GPIO_07	MCU_OSPI1_CLK	ALT7	WKUP_GPIO0_31	I/O	General-purpose I/O.
C24	GPIO_08	MCU_OSPI1_CSn0	ALT7	WKUP_GPIO0_38	I/O	General-purpose I/O.

5.10.2 Reserved

Table 63: GPIO Pins - Reserved

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B17	GPIO_09_CSI_1	MCAN12_TX	ALT7	GPIO0_1	I/O	General-purpose I/O. (CSI Reserved)
B18	GPIO_10_CSI_1	MCAN12_RX	ALT7	GPIO0_2	I/O	General-purpose I/O. (CSI Reserved)
A11	GPIO_11_CSI_1	MCASP1_AFSX	ALT7	GPIO0_47	I/O	General-purpose I/O. (CSI Reserved)
B19	GPIO_12_CSI_1	MCASP1_AXR0	ALT7	GPIO0_48	I/O	General-purpose I/O. (CSI Reserved)
C1	GPIO_13_CSI_2	MCU_OSPI1_LBCLKO	ALT7	WKUP_GPIO0_32	I/O	General-purpose I/O. (CSI Reserved)
C2	GPIO_14_CSI_2	MCU_OSPI1_DQS	ALT7	WKUP_GPIO0_33	I/O	General-purpose I/O. (CSI Reserved)
C3	GPIO_15_CSI_2	MCU_OSPI1_D3	ALT7	WKUP_GPIO0_37	I/O	General-purpose I/O. (CSI Reserved)
C4	GPIO_16_CSI_2	MCU_OSPI1_CSn1	ALT7	WKUP_GPIO0_39	I/O	General-purpose I/O. (CSI Reserved)
B42	GPIO_17_DSI_1	GPIO0_12	ALT7	GPIO0_12	I/O	General-purpose I/O. (DSI Reserved)
B43	GPIO_18_DSI_1	MCASP0_AXR3	ALT7	GPIO0_31	I/O	General-purpose I/O. (DSI Reserved)
B44	GPIO_19_DSI_1	PMIC_WAKE0	ALT7	GPIO0_13	I/O	General-purpose I/O. (DSI Reserved)
B45	GPIO_20_DSI_1	MCASP0_AXR2	ALT7	GPIO0_18	I/O	General-purpose I/O. (DSI Reserved)
B57	GPIO_21_DP	MCASP2_ACLKX	ALT7	GPIO0_21	I/O	General-purpose I/O. (DP Reserved)

5.11 UART

Table 64: UART Always Compatible Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B35	UART_1_RXD	MCASP0_AXR7	ALT11	UART4_RXD	I/O	Receive data for UART1.
B37	UART_1_TXD	MCASP0_AXR8	ALT11	UART4_TXD	I/O	Transmit data for UART1.
B36	UART_1_CTS	MCASP0_AXR9	ALT11	UART4_CTSN	I/O	Clear-to-send for UART1.
B38	UART_1_RTS	MCASP0_AXR10	ALT11	UART4_RTSN	I/O	Request-to-send for UART1.
B31	UART_2_RXD	WKUP_UART0_RXD	ALT0	WKUP_UART0_RXD	I/O	Receive data for UART2.
B33	UART_2_TXD	WKUP_UART0_RXD	ALT0	WKUP_UART0_RXD	I/O	Transmit data for UART2.
B32	UART_2_CTS	WKUP_UART0_CTSn	ALT0	WKUP_UART0_CTSn	I/O	Clear-to-send for UART2.
B34	UART_2_RTS	WKUP_UART0_RTSn	ALT0	WKUP_UART0_RTSn	I/O	Request-to-send for UART2.
D19	UART_3_RXD	MCASP0_ACLKX	ALT1	MCASP0_ACLKX	I/O	Receive data for UART3.
D20	UART_3_TXD	MCASP0_AFSX	ALT1	MCASP0_AFSX	I/O	Transmit data for UART3.
D21	UART_4_RXD	MCU_OSPI1_D1	ALT0	MCU_OSPI1_D1	I/O	Receive data for UART4.
D22	UART_4_TXD	WKUP_GPIO0_10	ALT7	WKUP_GPIO0_10	I/O	Transmit data for UART4.

5.12 I2C

5.12.1 I2C

Table 65: I2C Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D8	I2C_1_SCL	MCU_I2C0_SCL	ALT0	MCU_I2C0_SCL	I/O	I^2C0 clock (MCU domain).
D7	I2C_1_SDA	MCU_I2C0_SDA	ALT0	MCU_I2C0_SDA	I/O	I^2C0 data (MCU domain).
C17	I2C_2_SCL	WKUP_GPIO0_8	ALT0	MCU_I2C1_SCL	I/O	I^2C1 clock (MCU domain).
C16	I2C_2_SDA	WKUP_GPIO0_9	ALT0	MCU_I2C1_SDA	I/O	I^2C1 data (MCU domain).
B41	I2C_3_DSI1_SCL	I2C0_SCL	ALT0	I2C0_SCL	I/O	I^2C0 clock (DSI/disp aux usage).
B40	I2C_3_DSI1_SDA	I2C0_SDA	ALT0	I2C0_SDA	I/O	I^2C0 data (DSI/disp aux usage).
A13	I2C_4_CSI1_SCL	MCAN15_RX	ALT12	I2C1_SCL	I/O	I^2C1 clock (CSI1 aux option).
A12	I2C_4_CSI1_SDA	MCAN16_TX	ALT12	I2C1_SDA	I/O	I^2C1 data (CSI1 aux option).
C6	I2C_5_CSI2_SCL	MCASP1_AXR1	ALT13	I2C2_SCL	I/O	I^2C2 clock (CSI2 aux option).
C5	I2C_5_CSI2_SDA	MCASP1_AXR2	ALT13	I2C2_SDA	I/O	I^2C2 data (CSI2 aux option).
C19	I2C_6_SCL	MCAN15_TX	ALT8	I2C5_SCL	I/O	I^2C5 clock (SoC domain)
C18	I2C_6_SDA	MCAN14_RX	ALT8	I2C5_SDA	I/O	I^2C5 data (SoC domain)

Table 66 shows the addresses of the on-board I²C components.

Table 66: I²C addresses

Component	Part Number	I²C Address
Buck Converter	TPS62873Z0WRXSR	0x29
EEPROM	M24C02-FMC6TG	0x50
GPIO Expander A [1]	TCA6408ARSVR	0x20
GPIO Expander B	TCA6408ARSVR	0x21
Power Management IC (PMIC)	MPF0900AMBA1ES	0x48 to 0x4B plus 0x12 (watchdog) Depends on orderable part
Real-Time Clock (RTC)	RX8130CE:B3	0x32
Temperature Sensor	TMP1075DSGR	0x4F

[1] Not assembled by default

5.12.2 I2C/I3C

Table 67: I2C/I3C Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C16	I2C_2_SDA	WKUP_GPIO0_9	ALT3	MCU_I3C0_SCL	I/O	MCU domain I3C data line (shared with I2C_2_SDA on connector)
C17	I2C_2_SCL	WKUP_GPIO0_8	ALT3	MCU_I3C0_SDA	I/O	MCU domain I3C clock line (shared with I2C_2_SCL on connector)
A14	CTRL_MCLK_MOCI	WKUP_GPIO0_11	ALT5	MCU_I3C0_SDAPULLEN	I/O	MCU I3C0 SDA pull-up control / helper signal (multiplexed with CTRL_MCLK_MOCI)

5.13 SPI

Table 68: SPI Signal Pins

X1 pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D14	SPI_2_CLK	SPI0_CLK	ALT0	SPI0_CLK	O	SPI serial clock.
D16	SPI_2_CS	SPI0_CS0	ALT0	SPI0_CS0	O	Chip select (active low).
D15	SPI_2_MISO	SPI0_D0	ALT0	SPI0_D0	O	MOSI (SoC → device).
D17	SPI_2_MOSI	SPI0_D1	ALT0	SPI0_D1	I	MISO (device → SoC).
D12	SPI_1_CLK	MCASP0_AXR12	ALT0	MCASP0_AXR12	O	SPI serial clock.
D9	SPI_1_CS	MCASP0_AXR11	ALT0	MCASP0_AXR11	O	Chip select (active low).
D10	SPI_1_MISO	MCASP0_AXR14	ALT0	MCASP0_AXR14	O	MOSI (SoC → device).
D11	SPI_1_MOSI	MCASP0_AXR15	ALT0	MCASP0_AXR15	I	MISO (device → SoC).

5.14 ADC

Table 69: ADC Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
D1	ADC1	MCU_ADC0_AIN0	ALT0	MCU_ADC0_AIN0	I	Analog input channel 0 (MCU domain).
D2	ADC2	MCU_ADC0_AIN1	ALT0	MCU_ADC0_AIN1	I	Analog input channel 1 (MCU domain).
D3	ADC3	MCU_ADC0_AIN2	ALT0	MCU_ADC0_AIN2	I	Analog input channel 2 (MCU domain).
D4	ADC4	MCU_ADC0_AIN3	ALT0	MCU_ADC0_AIN3	I	Analog input channel 3 (MCU domain).
D54	MSP_4_TX_P	MCU_ADC0_AIN4	ALT0	MCU_ADC0_AIN4	I	Analog input channel 4 (MCU domain).
D55	MSP_4_TX_N	MCU_ADC0_AIN5	ALT0	MCU_ADC0_AIN5	I	Analog input channel 5 (MCU domain).
C55	MSP_4_RX_P	MCU_ADC0_AIN6	ALT0	MCU_ADC0_AIN6	I	Analog input channel 6 (MCU domain).
C56	MSP_4_RX_N	MCU_ADC0_AIN7	ALT0	MCU_ADC0_AIN7	I	Analog input channel 7 (MCU domain).

5.15 I2S

Table 70: I2S Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
B20	I2S_1_BCLK	MCASP4_ACLKX	ALT1	MCASP4_ACLKX	I/O	Bit clock for I^2S1.
B21	I2S_1_SYNC	MCASP4_AFSX	ALT1	MCASP4_AFSX	I/O	Sync for I^2S1.
B22	I2S_1_D_OUT	MCASP4_AXR1	ALT1	MCASP4_AXR1	I/O	Serial data output for I^2S1.
B23	I2S_1_D_IN	MCASP4_AXR2	ALT1	MCASP4_AXR2	I/O	Serial data input for I^2S1.
B24	I2S_1_MCLK	AUDIO_EXT_REFCLK1	ALT1	AUDIO_EXT_REFCLK1	I/O	Master clock for I^2S1.
B26	I2S_2_BCLK	-	-	I2S2_BCLK	I/O	Bit clock for I^2S2. Connected to GPIO expander.[1]
B27	I2S_2_SYNC	-	-	I2S2_D_SYNC	I/O	Serial data output for I^2S2. Connected to GPIO expander.[1]
B28	I2S_2_D_OUT	-	-	I2S2_D_OUT	I/O	Serial data input for I^2S2. Connected to GPIO expander.[1]
B29	I2S_2_D_IN	-	-	I2S2_D_IN	I/O	Serial data input for I^2S2. Connected to GPIO expander.[1]

[1] Connected to the TI-TCA6408ARSVR GPIO Expander A, which is not assembled by default

5.16 JTAG

Table 71: JTAG Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C12	JTAG_1_VREF	-	-	-	I	JTAG test reference voltage.
C11	JTAG_1_TCK	TCK	ALT0	TCK	I	JTAG test clock input. (Via 4.7k Ohm Pull-up resistor)
C13	JTAG_1_TMS	TMS	ALT0	TMS	I	JTAG test mode select input. (Via 4.7k Ohm Pull-up resistor)
C8	JTAG_1_TDI	TDI	ALT0	TDI	I	JTAG test data input. (Via 4.7k Ohm Pull-up resistor)

Continued on next page

Table 71: JTAG Signal Pins (Continued)

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C10	JTAG_1_TDO	TDO	ALT0	TDO	O	JTAG test data output. (Via 4.7k Ohm Pull-up resistor)
C7	JTAG_1_TRST#	TRSTN	ALT0	TRSTn	I	Active-low JTAG reset.

5.17 Power

Table 72: Power Supply pins

X1 Pin	Aquila Signal Name	I/O	Description	Remarks
B97, B98, B99, C96, C97, C98, C99, C100, D95, D96, D97, D98, D99, D100	VCC	I	(5V ±10%)	(Use decoupling capacitors on the carrier board)
A4, A9, A15, A18, A21, A24, A27, A30, A33, A36, A39, A42, A45, A48, A51, A54, A57, A60, A63, A66, A69, A72, A75, A78, A81, A84, A87, A90, A93, A96, B1, B4, B7, B10, B13, B16, B25, B30, B39, B47, B52, B64, B69, B82, B85, B88, C9, C27, C30, C33, C39, C42, C45, C48, C51, C54, C57, C60, C63, C66, C69, C72, C75, C78, C81, C84, C87, C90, C93, D13, D18, D26, D29, D32, D35, D38, D41, D44, D47, D50, D53, D56, D59, D62, D65, D68, D71, D74, D77, D80, D83, D86, D89, D92	GND	I	Digital Ground	
B96	PWR_1V8_MOCI	O	1.8V output	Max. 250mA
B100	VCC_BACKUP	I	RTC power supply backup battery	(May be left unconnected)

5.17.1 Power Management Signals

Table 73: Power Related Signal Pins

X1 pin	Aquila specification signal name	I/O	Description
B92	CTRL_RESET_MICO#	I	External reset input to the module (active-low).
D5	CTRL_RESET_MOCI#	O	System reset driven by module to carrier (active-low).
B93	CTRL_PWR_BTN_MICO#	I	Power-button input from carrier to module (active-low).
B94	CTRL_FORCE_OFF_MOCI#	O	Force-off output to PMIC/power logic (active-low).
B95	CTRL_PWR_EN_MOCI	O	Power-enable drive from module to PMIC/power tree.
D6	CTRL_WAKE1_MICO#	I/O	Wake/event input from carrier/PMIC (active-low).

5.18 PWM

Table 74: PWM Signal Pins

X1 Pin	Aquila specification signal name	SoC ball name	SoC alternate function	SoC alternate function name	I/O	Description
C25	PWM_1	MCAN0_TX	ALT9	EHRPWM0_B	I/O	PWM output channel 1 .
C26	PWM_2	MCASP2_AXR1	ALT9	EHRPWM1_A	I/O	PWM output channel 2 .
B46	PWM_3_DSI	MCASP0_AXR5	ALT9	EHRPWM5_A	I/O	PWM output channel 3 (Dedicated for DSI).
B58	PWM_4_DP	MCASP0_AXR0	ALT9	EHRPWM2_A	I/O	PWM output channel 4A (Dedicated for DisplayPort).

6 Test Points

The Aquila AM69/TDA4 system on module includes a comprehensive set of test points (TPs) that facilitate debugging, signal monitoring, and system validation during development and production. These test points provide direct access to critical signals such as power rails, communication interfaces, clock outputs, and control lines, enabling precise measurement and troubleshooting without disrupting normal module operation.

Each test point is identified by a unique label (e.g., TP01, TP02) and corresponds to specific signals, including PMIC control signals, eMMC interface lines, I^2C buses, and various power supply voltages. Some test points incorporate external pull-up or pull-down resistors, which are detailed in the specification, to ensure signal stability and proper logic levels during testing.

Figure 2: Aquila AM69/TDA4 test points - Top view

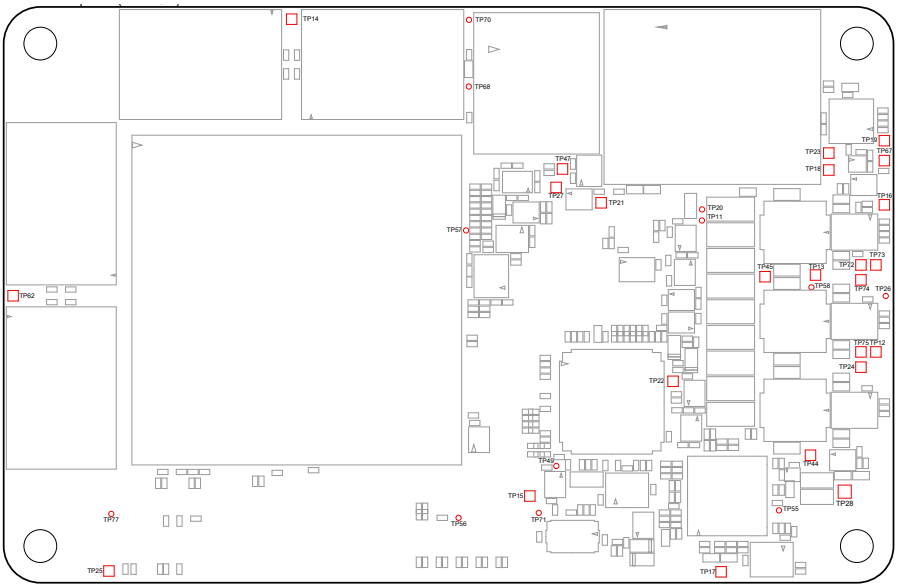


Figure 3: Aquila AM69/TDA4 test points - Bottom view

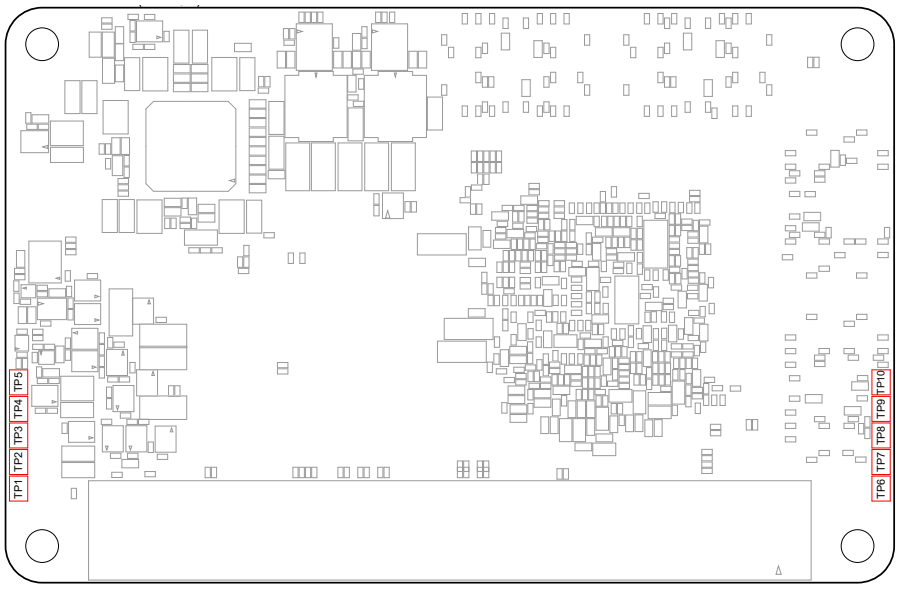


Table 75: Aquila AM69/TDA4 Test Points

Test Point	Net	Voltage
TP1	PMIC_SCL	1.8V
TP2	PMIC_SDA	1.8V
TP3	+V1.8_STBY	1.8V
TP4	IC1-AA31 (VPP_CORE)	1.8V
TP5	IC1-L29 (VPP_MCU)	0V (1.8V if R521 is populated)
TP6	JTAG_EMU0	1.8V
TP7	JTAG_EMU1	1.8V
TP8	+VDD_CPU_AVS	0.7-0.8V (0.8V on start-up)
TP9	+V0.8_VDD_CORE	0.8V
TP10	+V0.85_VDD_RAM	0.85V
TP11	MCU_PORZ	1.8V
TP12	+V1.8_STBY	1.8V
TP13	+V0.85_VDD_RAM	0.85V
TP14	+V1.8_VDD_IO	1.8V
TP15	+V3.3_VIO	3.3V
TP16	+V1.8_VDA_PHY	1.8V
TP17	+V2.5_ETH	2.5V
TP18	+V0.8_VDA_DLL	0.8V
TP19	+V1.8_VDA_PLL	1.8V
TP20	PORZ	1.8V
TP21	WKUP_3V3_I2C_SCL	3.3V
TP22	+V1.1_VIO	1.1V
TP23	+V3.3_WIFI	3.3V
TP24	DSCRT_PWRGRP_IRQn	1.8V
TP25	+VDD_SD_DV	1.8/3.3V
TP26	PMIC_EN_3V3_VIO	1.8V
TP27	WKUP_3V3_I2C_SDA	3.3V
TP28	+V1.8_ETH	1.8V
TP44	+V1.0_ETH	1.0V
TP45	+VDD_CPU_AVS	0.7-0.8V (0.8V on start-up)
TP47	+V0.8_VDD_CORE	0.8V
TP49	RESETSTATZ	1.8V
TP55	NetIC8-18 (CLK_OUT)	1.8V
TP56	EN_DRV	4.5-5.5V
TP57	WKUP_GPIO_88	1.8V
TP58	MCU_RESETSTATZ	1.8V
TP62	+V1.1_VDD_DDR	1.1V
TP67	NetIC25_6	1.8V
TP68	eMMC_CMD	1.8V

Continued on next page

Table 75: Aquila AM69/TDA4 Test Points (Continued)

Test Point	Net	Voltage
TP70	eMMC_DATA0	1.8V
TP71	MUX_SEL	1.8V
TP72	WKUP_I2C.SDA	1.8V
TP73	WKUP_I2C.SCL	1.8V
TP74	+VCC_BACKUP	1.25-5.5V
TP75	+V_IN	4.5-5.5V
TP77	IC1_AN17 (USB0_ID)	3.3V

7 Recovery Mode

Missing Content
More information about recovery mode will be available on the next release of the datasheet.

8 Known Issues

There are no known issues.

9 Technical Specifications

9.1 Absolute Maximum Ratings

Table 76: Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	2.1	V
USB_1_VBUS	Input Voltage at USB_1_VBUS	-0.3	5.5	V

9.2 Recommended Operation Conditions

Table 77: Recommended operation conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Main power supply	4.5	5.0	5.5	V
VCC_BACKUP	RTC power supply	1.25	3.0	5.5	V

9.2.1 Power Consumption

For designing and scaling the power supplies, it is advised to follow the recommendations provided in the specification of the Aquila product family. Following those recommendations ensures that the carrier board being designed will be compatible with all existing and future Aquila modules. For details, please refer to the Aquila Carrier Board Design Guide or the Aquila Family Specification.

9.3 Mechanical Characteristics

Missing Content
More information about mechanical characteristics will be available on the next release of the datasheet.

9.3.1 Sockets for the Aquila Modules

The Aquila modules use Samtec's Accelerate HP (High-Performance Array) Board-to-Board connector for state-of-the-art robustness and reliability. This connector has 400 pins in a 100×4 organization with a 0.635mm pitch. The board-to-board connector is available to Toradex customers for custom carrier board designs, both during development and production. Volume pricing is also available. For more information, see Aquila Carrier Board Connector[1].

[1] https://www.toradex.com/accessories/aquila-carrier-board-connector

Table 78: Board-to-Board connector models

PN (Module Side)	Solder Balls	Remarks
Samtec APF6-100-03.5-L-04-0-A-FR	No	
Samtec APF6-100-03.5-L-04-2-TR	Yes	No alignment pins

Mating parts for the Carrier side can have two stacking height options:

- 5 mm stacking height
- 10 mm stacking height

Table 79: Mating Board-to-Board connector models

PN (Module Side)	Solder Balls	Stacking Height	Remarks
Samtec APM6-100-01.5-L-04-0-A-FR	No	5mm	
Samtec APM6-100-01.5-L-04-2-TR	Yes	5mm	No alignment pins
Samtec APM6-100-06.5-L-04-0-A-FR	No	10mm	
Samtec APM6-100-06.5-L-04-2-TR	Yes	10mm	No alignment pins

The above PNs indicate 10 μm gold contacts. For 30 μm gold please change the -L- option to -S-.

The following table compares the different mating parts options. The connector height is the stacking height of the connector. The board-to-board distance is the nominal space between the carrier board and the module. The column “Component Height Carrier Board” indicates the recommended maximum height of components underneath the module.

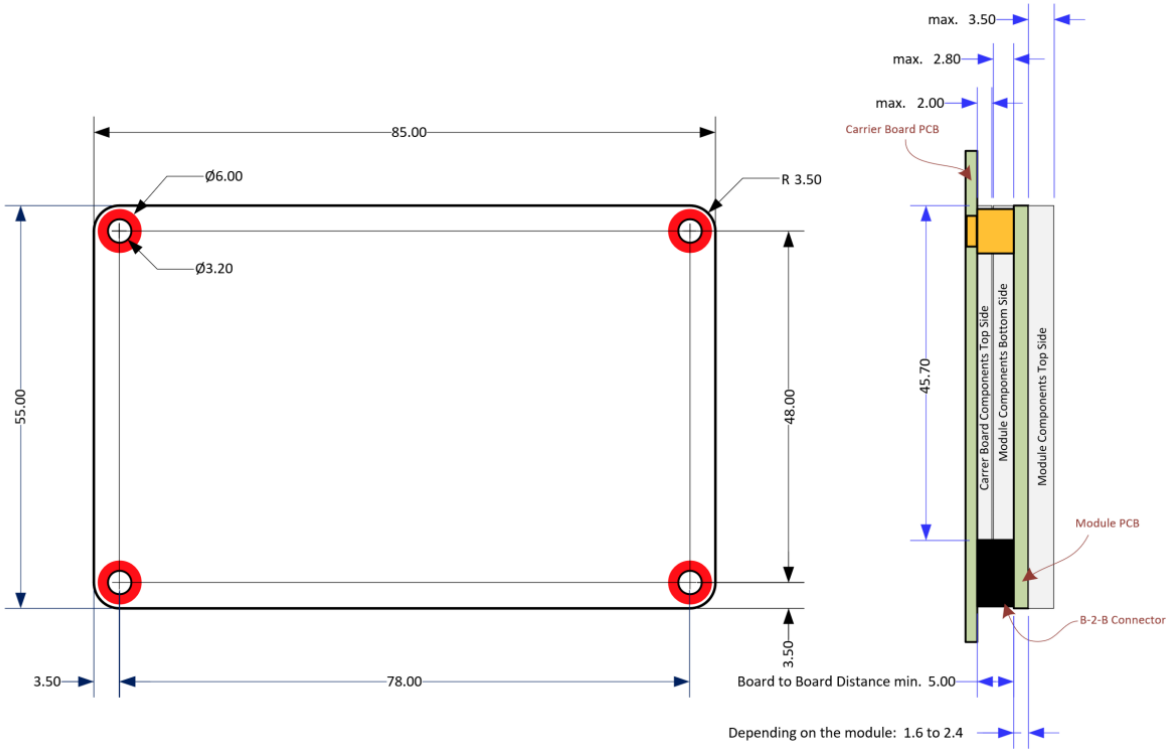
Table 80: Board-to-Board connector stacking height

Connector Height	Board-to-Board distance	Component Height Carrier Board	Remarks
5mm	5 mm	2 mm	Recommended stacking height for Aquila modules
10mm	10 mm	8 mm	Recommended for special cases where high components under the module are required

To ensure mechanical compatibility with current and future Aquila modules and module revisions, it is recommended to reserve the full component height allowance specified for the module on the carrier board. Even if the module does not fully utilize the allotted component height, additional components should not be placed between the module and the carrier board. Figure 4 shows the module dimensions including the specified stacking height to assist in carrier board design.

If system design requires components taller than 2 mm in this area, it is advisable to select a connector with an increased stacking height to maintain mechanical integrity and compatibility.

Figure 4: Module stacking dimensions



9.4 Thermal Specification

Table 81: Thermal specification

Description	Min.	Typ.	Max.	Unit
Operating temperature range	–40		+85	°C
Storage temperature	–40		+85	°C
SoC junction temperature	–40		+105	°C
$R\theta_{JA}$ – junction-to-ambient thermal resistance		8.3		°C/W
$R\theta_{JC}$ – junction-to-case thermal resistance		0.11		°C/W

10 Product Compliance

Up-to-date information about product compliance—such as RoHS, CE, UL 94, Conflict Minerals, REACH, and others—can be found on our website[2].

[2] https://www.toradex.com/support/product-compliance

11 Device and Documentation Support

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