iW-Rainbow-G64M

Speedster7T FPGA SOM

Hardware Datasheet

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1. INTRODUCTION

1.1. Purpose

This document is the Hardware datasheet for the Speedster7t FPGA System on Module (SOM) based on the Achronix Speedster7t FPGA. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This datasheet provides detailed information on the overall design and usage of the Speedster7t FPGA SOM from a hardware systems perspective.

1.2. SOM Overview

The Speedster7t FPGA SOM is an extension of Achronix Speedster7t 1500 FPGA. Speedster7t FPGA SOM has a form factor of 120mm x 90mm and provides the functional requirements for an embedded application. Two high-speed high-density connectors provide the carrier board interface to carry all the IO signals to and from the Speedster7t FPGA SOM.

1.3. List of Acronyms

The following acronyms will be used throughout this document.

Table 1 : Acronyms and Abbreviations

Acronyms	Abbreviations
ADM	Achronix Device Manager
BRAM	Block Random Access Memory
DDR4	Double Data Rate 4
ECC	Error Correcting Code
eMMC	embedded Multi Media Card
FPGA	Field Programmable Gate Array
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GDDR6	Graphics Double Data Rate 6
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LED	Light Emitting Diode
LGA	Land Grid Array
LPDDR4	Low Power DDR4
LRAM	Local Random Access Memory
LUT	Look up Table
MAC	Media Access Control
NRZ	Non-Return to Zero

OSM	Open Standard Module
PAM4	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PTP	Precision Time Protocol
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
SERDES	Serializer/Deserializer
SoC	System on Chip
SOM	System on Module
TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

1.4. Terminology Description

In this document, wherever signal type is mentioned, below terminology is used.

Table 2 : Terminology List

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
SE	Single Ended
DIFF	Differential IO Pair
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5. References

- Achronix Speedster7t FPGA Datasheet and User Guides
- iW-RainboW-G43M-Intel Agilex SoC FPGA (R31B, R31C)-SOM-HardwareUserGuide-R1.0-REL0.1
- iW-RainboW-G46M_i.MX_8XLite_OSM_LGA_Module-HardwareUserGuide-R2.0-REL0.1

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Speedster7t FPGA SOM features and hardware architecture with high level block diagram. Also, this section provides detailed information about board-to-board connectors pin assignment and usage.

2.1. Speedster7t FPGA SOM Block Diagram

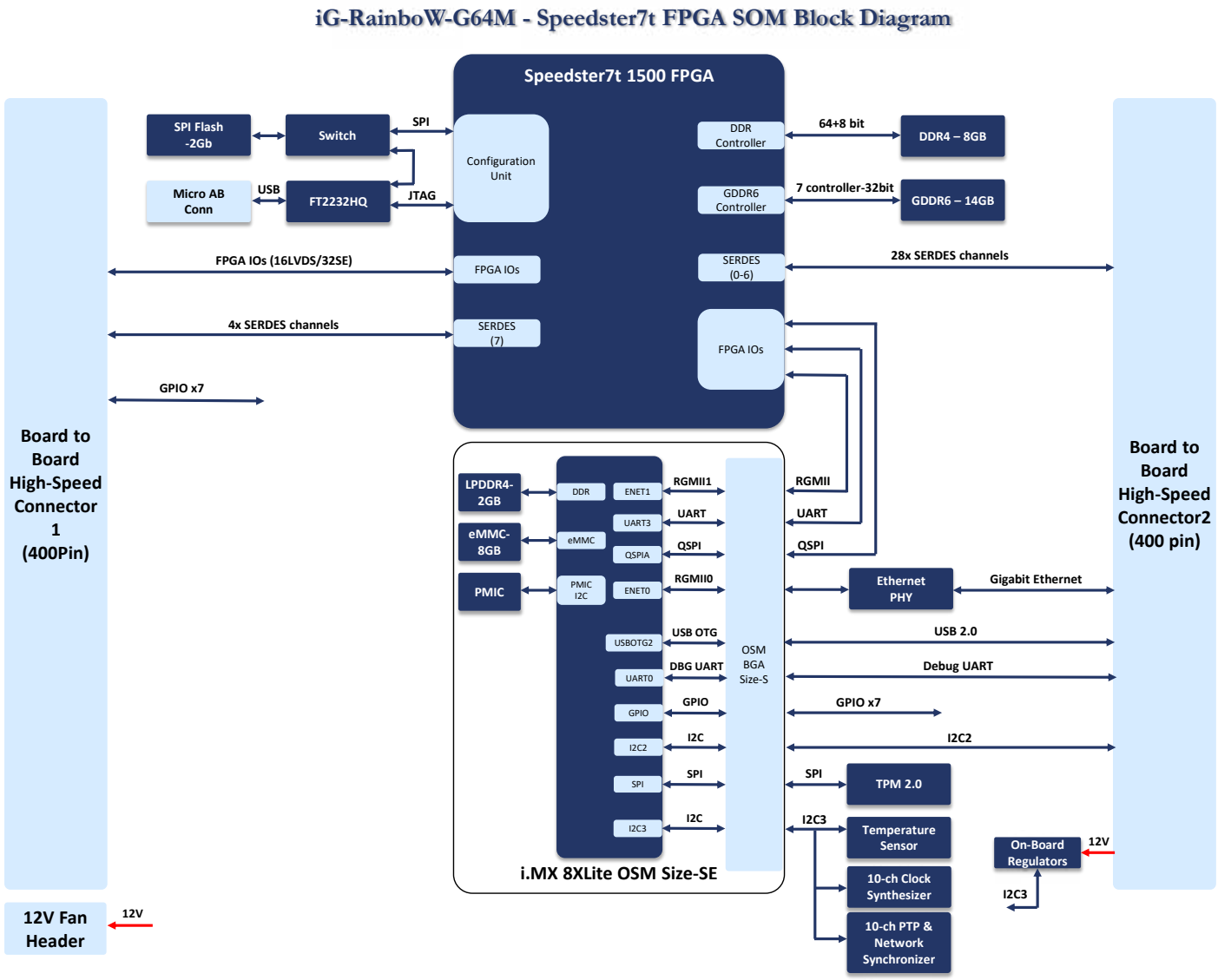


Figure 1: Speedster7t FPGA SOM Block Diagram

2.2. Speedster7t FPGA SOM Features

The Speedster7t FPGA SOM supports the following features.

Achronix FPGA

- Achronix Speedster7t 1500 FPGA with F53 package
  - 692K 6-input LUTs
  - 2560 LRAMs and 2560 BRAMs & 2560 MLPs
  - High speed SERDES transceivers supporting 53.125Gbps PAM4 and 28Gbps NRZ modulation

CPU

- iWave OSM – SE LGA Module with i.MX 8XLite Processor
  - On SOM LPDDR4 and eMMC

Power

- Discrete power regulators

Memory Interfaces

- 8GB DDR4 with ECC
- 14GB GDDR6
- 2Gb SPI Flash

FPGA to CPU Features

- RGMII x 1
- QSPI x 1
- UART x 1

On SOM Features

- Gigabit Ethernet PHY
- Clock Synthesizer for On-SOM Clocks
- PTP & SyncE Network Synchronizer
- Temperature Sensor & Voltage Monitoring
- TPM2.0 Module
- Fan Header

Board to Board Connector 1 Interfaces (400 pin)

From FPGA

- 4x SERDES Channels (with line rates of 53.125Gbps Raw SERDES)
- FPGA IOs – N0 Bank[1]
  - Up to 3 DIFF IOs/6 Single Ended (SE) IOs
- FPGA IOs – S0 Bank[2]
  - Up to 13 DIFF IOs/26 Single Ended (SE) IOs

From OSM

- GPIOs x 7

Board to Board Connector 2 Interfaces

From FPGA

- 28x SERDES Channels (with line rates of 53.125Gbps Raw SERDES)

From OSM

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB 2.0 Device x 1 Port
- Debug UART x 1 Port
- I2C x 1 Port

General Specification

- Power Supply: 12V through Board-to-Board Connector 2
- Operating Temperature: -40°C to +85°C
- Form factor: 120mm x 90 mm

[1] *In Speedster7t FPGA SOM, GPIO bank N0 supports fixed IO voltage level of 1.8V.*

[2] *In Speedster7t FPGA SOM, GPIO bank S0 supports a variable IO voltage setting which is configurable through software. The available voltage options include 1.1V, 1.2V, 1.35V, 1.5V and 1.8V (default).*

2.3. Achronix Speedster7t FPGA

The Achronix high-performance, 7nm Speedster7t FPGA family is specifically designed to support extremely high bandwidth requirements for demanding applications including data-centre workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence and machine learning (AI/ML) and high-speed networking.

The Achronix FPGA has two-dimensional network on chip (2D NoC) enabling high bandwidth data flow throughout and between the FPGA fabric and hard IO and memory controllers and interfaces, multiple PCIe Gen5 ports, high-speed Serdes transceivers supporting 112 Gbps PAM4 and 56 Gbps PAM4/NRZ modulation as well as lower data rates, GDDR6 and DDR4 controllers and interfaces. Block diagram of Achronix Speedster7t FPGA from Achronix website is shown below for reference.

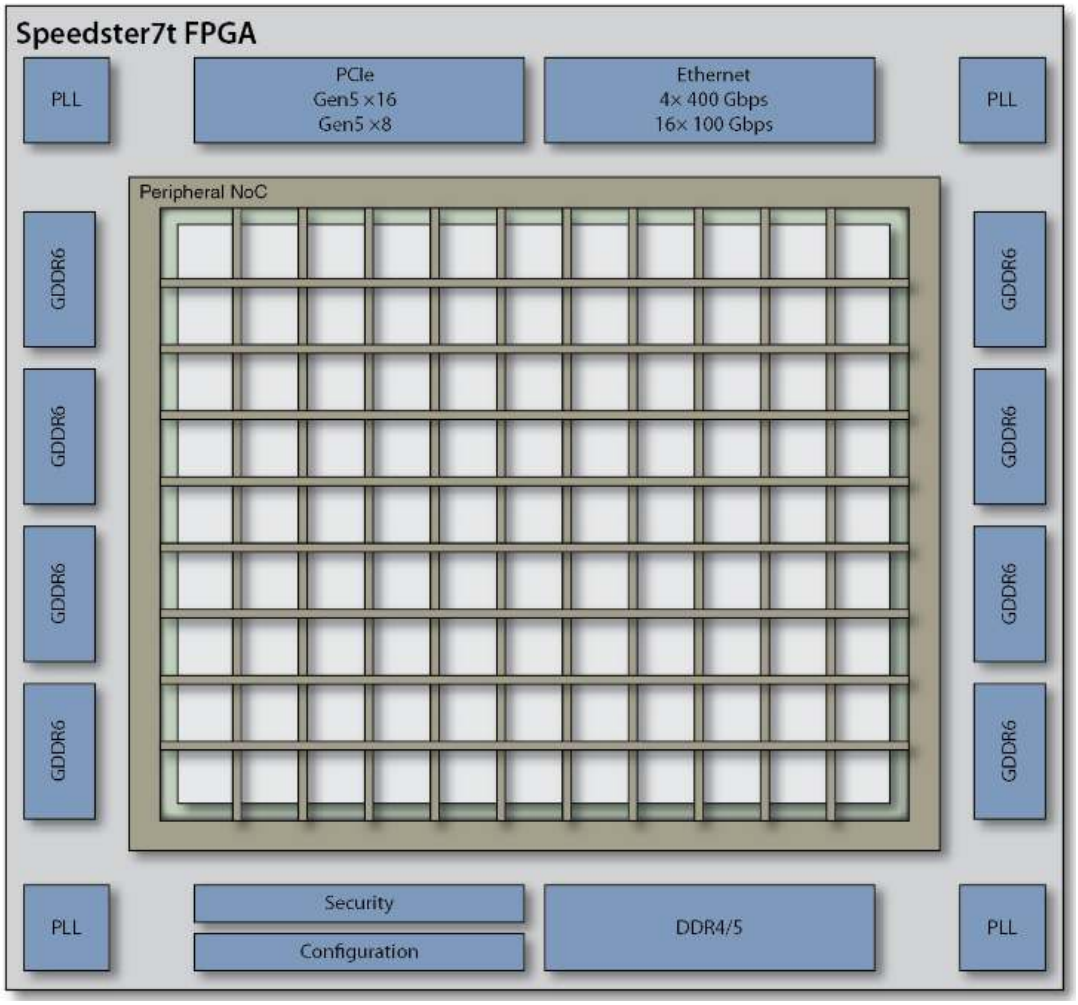


Figure 2: Achronix Speedster7t FPGA Simplified Block Diagram

Note: Please refer the latest Achronix Speedster7t FPGA datasheet & technical reference manual for more details which may be revised from time to time.

2.3.1. FPGA Power

The Speedster7t FPGA SOM uses discrete power regulators for power management. In SOM, FPGA core power supply (CORE_VDD) is fixed to 0.85V or 0.9V based on the speed grade of the FPGA. The GPIO bank N0 I/O voltage is fixed to 1.8V and GPIO bank S0 I/O voltage is variable with 1.1V being default. The I/O voltage details of each FPGA bank & high-speed transceiver will be mentioned in the corresponding sections.

2.3.2. FPGA Reset

The Speedster7t FPGA SOM supports warm reset from board-to-board connector J2 pin B14 which is connected to SYS_RST# (U17) pin of OSM, pull-up resistor is provide on SOM for this reset signal. Reset output signal of OSM is connected to FPGA reset pin CLKIO_NW_REFIO_P_0 (N16).

2.3.3. FPGA Reference Clock

The Speedster7t FPGA SOM supports on board clock synthesizer for reference clock to different blocks of Speedster7t FPGA. The reference clock from clock synthesizer to FPGA is mentioned in the below table.

Table 3 : List of on SOM Clock Source

Sl. No	On-SOM Clock Synthesizer Frequency	FPGA Pin Name	FPGA Pin No	Signal Type/ Termination	Description
1	100MHz	SRDS_N0_REFCLK_P	J15	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 0
		SRDS_N0_REFCLK_N	J16		
2	100MHz	SRDS_N1_REFCLK_P	G15	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 1
		SRDS_N1_REFCLK_N	G16		
3	156.25MHz	SRDS_N2_REFCLK_P	B26	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 2
		SRDS_N2_REFCLK_N	A26		
4	156.25MHz	SRDS_N3_REFCLK_P	E26	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 3
		SRDS_N3_REFCLK_N	D26		
5	156.25MHz	SRDS_N4_REFCLK_P	H26	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 4
		SRDS_N4_REFCLK_N	G26		
6	156.25MHz	SRDS_N5_REFCLK_P	L26	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 5
		SRDS_N5_REFCLK_N	K26		
7	156.25MHz	SRDS_N6_REFCLK_P	G37	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 6
		SRDS_N6_REFCLK_N	G36		
8	156.25MHz	SRDS_N7_REFCLK_P	J37	2.5V, LVPECL	LVPECL reference clock for SERDES Bank 7
		SRDS_N7_REFCLK_N	J36		
9	200MHz	CLKIO_NW_REFIO_P_1	R16	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_NW_REFIO_N_1	R17		
10	100MHz	CLKIO_SW_REFIO_P_0	AV17	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_SW_REFIO_N_0	AU17		
11	100MHz	CLKIO_NE_REFIO_P_0	N36	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_NE_REFIO_N_0	N35		
12	10MHz	CLKIO_NE_REFIO_P_1	R36	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_NE_REFIO_N_1	R35		
13	100MHz	CLKIO_SE_REFIO_P_0	AY34	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_SE_REFIO_N_0	AW34		
14	200MHz	CLKIO_SE_REFIO_P_1	AY36	1.8V, LVDS	LVDS reference clock for Achronix FPGA
		CLKIO_SE_REFIO_N_1	AW36		

2.3.4. FPGA Configuration and Status

The Speedster7t FPGA can be configured via flash mode or JTAG mode. A configuration bitstream is generated in ACE by selecting the appropriate configuration interface. The configuration mode of the FPGA is controlled via mode select pins of the FPGA. These pins can be driven via hardware on the board. The Speedster 7t FPGA SOM supports LED for the FPGA configuration status indication namely CONFIG_DONE. LED interfaced to CONFIG_DONE is asserted when the FPGA configuration is complete. It is used to indicate if the FPGA is configured or not.

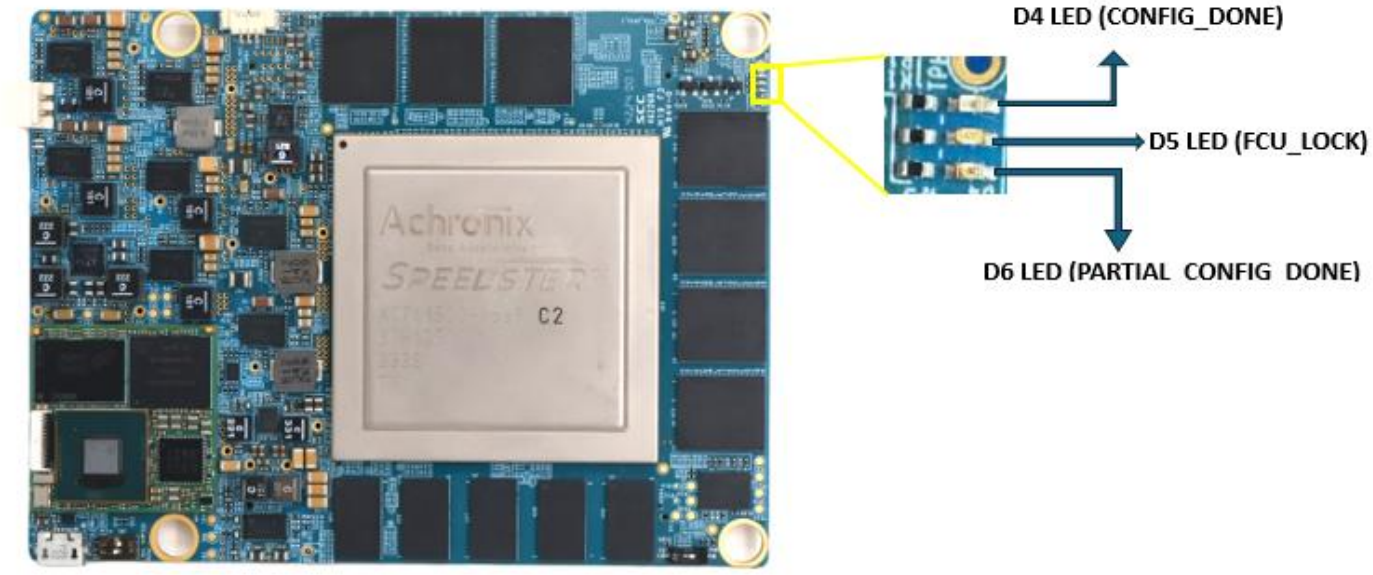


Figure 3: FPGA Configuration Status LEDs

The D5 LED (FCU_LOCK) indicates that the bitstream file has started to load to FPGA and the FPGA is being configured. D6 LED (PARTIAL_CONFIG_DONE) indicates that bitstream loading has been completed successfully for partial reconfiguration of the FPGA and that it is ready to enter user mode. The D4 LED (CONFIG_DONE) indicates the completion of the configuration.

2.3.5. FPGA Configuration Switch

The Speedster7t FPGA SOM supports FPGA configuration switch (SW3) to select the configuration path for the SPI flash memory. When the switch is in ON position, FPGA will be configured through SPI Flash and when it will be in OFF position, SPI Flash will be configured using USB connector through JTAG mode.

Table 4 : FPGA Switch Truth Table

Achronix SOM Switch	SW3	
	Switch Position	Switch Position Image
FPGA configuration through SPI	ON	
SPI flash configuration through JTAG	OFF	

2.4. FPGA Memory

2.4.1. DDR4 with ECC

The Speedster7t FPGA SOM supports 64bit, 8GB DDR4 RAM memory for Achronix FPGA. Four 16 bit, 2GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 8GB. Also, Speedster7t FPGA SOM supports 8-bit ECC for RAM memory. DDR4 devices operate at 2666Mbps data rate for Speedster7t FPGA having speed grade 2 and at 3200Mbps for FPGA having speed grade 1. DDR4 memory is connected to the hard memory controller of the Achronix FPGA.

2.4.2. GDDR6

The Speedster7t FPGA SOM supports 224-bit, 14GB GDDR6 RAM memory. Seven 32 bit, 2GB GDDR6 IC is used to support RAM memory of 14GB. GDDR6 devices operate at 14Gbps data rate for Speedster7t FPGA having speed grade 2 and at 16Gbps for FPGA having speed grade 1. GDDR6 memory is connected to the hard memory controller of the Achronix FPGA.

2.4.3. SPI Flash

The Speedster7t FPGA SOM supports 2Gb SPI flash memory for boot and storage of Speedster7t FPGA. This SPI flash memory is directly connected to the configuration bank of the Speedster7t FPGA and operates at 1.8V voltage level.

2.5. i.MX 8XLite OSM

The i.MX 8XLite OSM will serve as the control unit in the Speedster7t FPGA SOM. This module, having an OSM LGA package is based on NXP's i.MX 8XLite SoC and features the i.MX 8XLite dual processor.

OSM supports LPDDR4, SPI, eMMC, RGMII, QSPI, Debug UART, Gigabit Ethernet, USB2.0 Device along with I2C and GPIO interface for Speedster7t FPGA SOM.

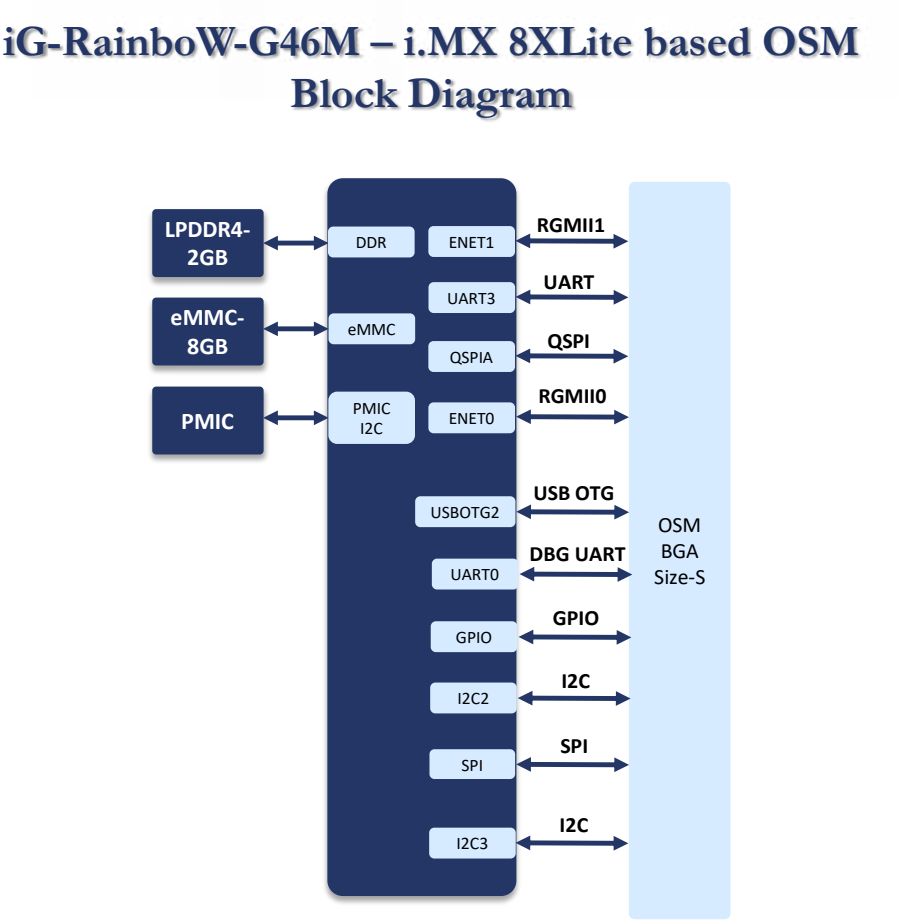


Figure 4 : i.MX 8XLite OSM Simplified Block Diagram

Note: Please refer the latest i.MX 8XLite OSM datasheet & technical reference manual for more details which may be revised from time to time.

2.5.1. OSM Booting and Configuration

The Speedster7t FPGA SOM supports OSM boot mode configuration switch (SW1) to select the boot device for OSM. If BOOT_MODE[0:1] is in '01' position, OSM will be configured through USB serial download mode and if it is in '10' position OSM will be configured through eMMC boot mode.

Table 5 : Boot Mode Switch Truth Table

OSM Boot Mode	SW1		
	(Position 1) BOOT_MODE[0]	(Position 2) BOOT_MODE[1]	Switch Position Image
USB	OFF	ON	
eMMC	ON	OFF	

2.5.2. OSM Memory

2.5.2.1. LPDDR4 RAM

OSM supports 2GB LPDDR4 RAM memory.

2.5.2.2. eMMC Flash

OSM supports 8GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 8XLite SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) voltage levels.

2.6. FPGA to OSM Interfaces

2.6.1. RGMII

The Speedster7t FPGA SOM supports one RGMII interface between Speedster7t FPGA and OSM through GPIO Bank N0 of FPGA and Ethernet 1 interface of OSM. IO voltage level of RGMII interface is 1.8V.

For more details on RGMII pinouts between FPGA and OSM, refer the below table.

Table 6 : RGMII Interface

Signal Name	FPGA Pin Name	FPGA Pin No	OSM Pin Name	OSM Pin No	Signal Type/ Termination*	Description
FPGA_ETH_TXD0	GPIO_N0_BYTE0_BIT_0	W17	ETH_B_(S)(R)(G)MII_TXD0	G1	I, 1.8V LVCMOS	Transmit Data
FPGA_ETH_TXD1	GPIO_N0_BYTE0_BIT_1	W16	ETH_B_(S)(R)(G)MII_TXD1	F1	I, 1.8V LVCMOS	Transmit Data
FPGA_ETH_TXD2	GPIO_N0_BYTE0_BIT_2	Y17	ETH_B_(S)(R)(G)MII_TXD2	G2	I, 1.8V LVCMOS	Transmit Data
FPGA_ETH_TXD3	GPIO_N0_BYTE0_BIT_3	Y16	ETH_B_(S)(R)(G)MII_TXD3	F2	I, 1.8V LVCMOS	Transmit Data
FPGA_ETH_RXD0	GPIO_N0_BYTE0_BIT_6	AB17	ETH_B_(S)(R)(G)MII_RXD0	J1	O, 1.8V LVCMOS	Receive Data
FPGA_ETH_RXD1	GPIO_N0_BYTE0_BIT_7	AC16	ETH_B_(S)(R)(G)MII_RXD1	K1	O, 1.8V LVCMOS	Receive Data
FPGA_ETH_RXD2	GPIO_N0_BYTE0_BIT_8	AD16	ETH_B_(R)(G)MII_RXD2	M1	O, 1.8V LVCMOS	Receive Data
FPGA_ETH_RXD3	GPIO_N0_BYTE0_BIT_9	AD17	ETH_B_(R)(G)MII_RXD3	N1	O, 1.8V LVCMOS	Receive Data
FPGA_ETH_TX_EN	GPIO_N0_BYTE1_BIT_0	AF16	ETH_B_(R)(G)MII_TX_EN(_ER)	J2	I, 1.8V LVCMOS	Transmit Enable
FPGA_ETH_TX_CLK	GPIO_N0_BYTE1_BIT_1	AG17	ETH_B_(R)(G)MII_TX_CLK	H1	I, 1.8V LVCMOS	Transmit Clock
FPGA_ETH_RX_DV	GPIO_N0_BYTE0_BIT_10	AE16	ETH_B_(R)(G)MII_RX_DV(_ER)	L1	O, 1.8V LVCMOS	Receive Data Valid
FPGA_ETH_RX_CLK	GPIO_N0_BYTE0_BIT_11	AE17	ETH_B_(R)(G)MII_RX_CLK	P1	O, 1.8V LVCMOS	Receive Clock

**Signal directions mentioned in table are based on FPGA*

2.6.2. QSPI

The Speedster7t FPGA SOM supports one QSPI interface between Speedster7t FPGA and OSM through GPIO bank N0 of FPGA and QSPI A interface of OSM. IO voltage level of QSPI interface is 1.8V.

For more details on QSPI pinouts between FPGA and OSM, refer the below table.

Table 7 : QSPI Interface

Signal Name	FPGA Pin Name	FPGA Pin No	OSM Pin Name	OSM Pin No	Signal Type/ Termination*	Description
OSM_QSPI_CS#	GPIO_N0_BYTE1_BIT_10	AN16	GPIO_B_0	D19	I,1.8V LVCMOS	QSPI chip select.
OSM_QSPI_CLK	GPIO_N0_BYTE1_BIT_11	AR16	GPIO_A_7 / SPI_B_CS1#	L17	I,1.8V LVCMOS	QSPI clock.
OSM_QSPI_DATA0	GPIO_N0_BYTE1_BIT_6	AJ16	GPIO_B_1	E19	IO,1.8V LVCMOS	QSPI Data0.
OSM_QSPI_DATA1	GPIO_N0_BYTE1_BIT_7	AK17	GPIO_B_2	F19	IO,1.8V LVCMOS	QSPI Data1.
OSM_QSPI_DATA2	GPIO_N0_BYTE1_BIT_8	AL16	GPIO_B_3	G19	IO,1.8V LVCMOS	QSPI Data2.
OSM_QSPI_DATA3	GPIO_N0_BYTE1_BIT_9	AM16	GPIO_B_4	H19	IO,1.8V LVCMOS	QSPI Data3.

**Signal directions mentioned in table are based on FPGA*

2.6.3. UART

The Speedster7t FPGA SOM supports one UART interface between Speedster7t FPGA and OSM through GPIO Bank N0 of FPGA and UART 3 interface of OSM. IO voltage level of UART interface is 1.8V.

For more details on UART pinouts between FPGA and OSM, refer the below table.

Table 8 : UART Interface

Signal Name	FPGA Pin Name	FPGA Pin No	OSM Pin Name	OSM Pin No	Signal Type/ Termination*	Description
OSM_UART_TX	GPIO_N0_BYTE1_BIT_3	AH17	UART_A_TX	B13	I,1.8V LVCMOS	UART Transmitter.
OSM_UART_RX	GPIO_N0_BYTE1_BIT_2	AG16	UART_A_RX	A14	O,1.8V LVCMOS	UART Receiver.

**Signal directions mentioned in table are based on FPGA*

2.7. Other On SOM Features

2.7.1. TPM 2.0 Module

The Speedster7t FPGA SOM supports Trusted Platform Module (TPM) 2.0 through OSM. The TPM technology is designed to provide hardware-based, security-related functions. A TPM chip is a secure crypto-processor that is designed to carry out cryptographic operations. This TPM module is connected to the SPI2 lane of OSM and operates at 1.8V voltage level.

2.7.2. Temperature Sensor

The Speedster7t FPGA SOM supports temperature sensor to measure the junction temperature on SOM. The temperature sensor is connected to I2C3 lane of OSM and operates at 1.8V voltage level.

2.7.3. USB Connector

The Speedster7t FPGA SOM supports one USB connector (J5) for JTAG interface. JTAG interface signals from Speedster7t FPGA is connected to FTDI IC “FT2232HQ-REEL” through which it is connected to USB connector. FTDI IC supports JTAG communication which enables debug and configuration interfaces for Achronix devices. These JTAG interface signals are at 1.8V voltage level.

The USB connector (J5) is physically located on top side of the SOM. USB Micro-B connector cable can be directly connected to this USB connector.

- Connector Part - 475890001 from Molex

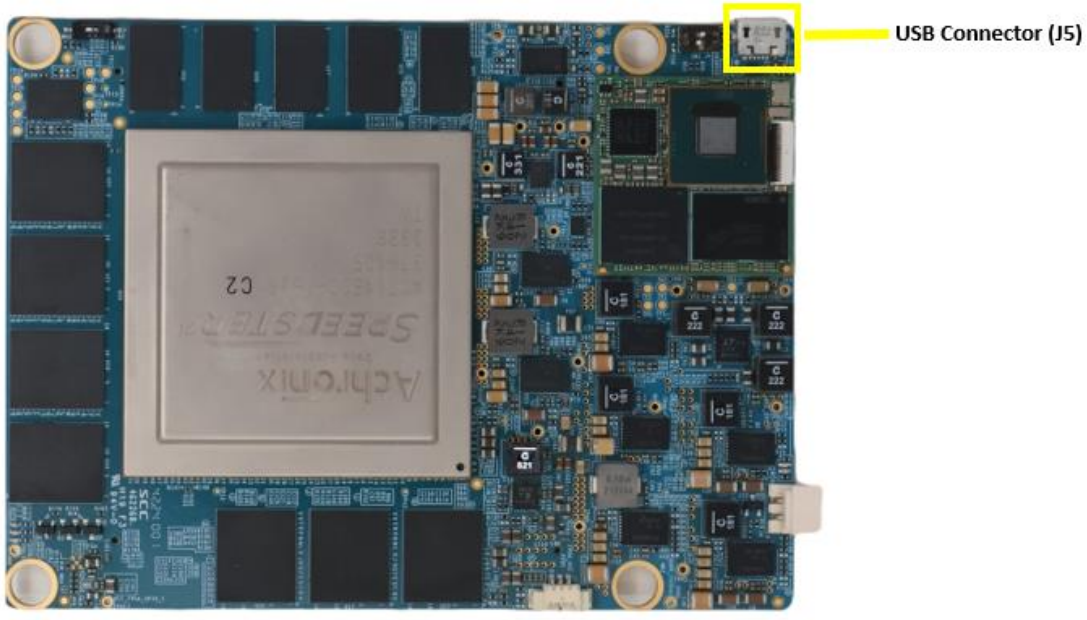


Figure 5 : USB Connector

2.7.4. Power Indication LEDs

The Speedster7t FPGA SOM supports two LEDs to indicate the status of SOM power. LED D2 functions as power indicator for VCC_5V which is the first voltage rail in the power sequence. LED D1 functions as power indicator for VCC_3V3 which is the last voltage rail in the power sequence.

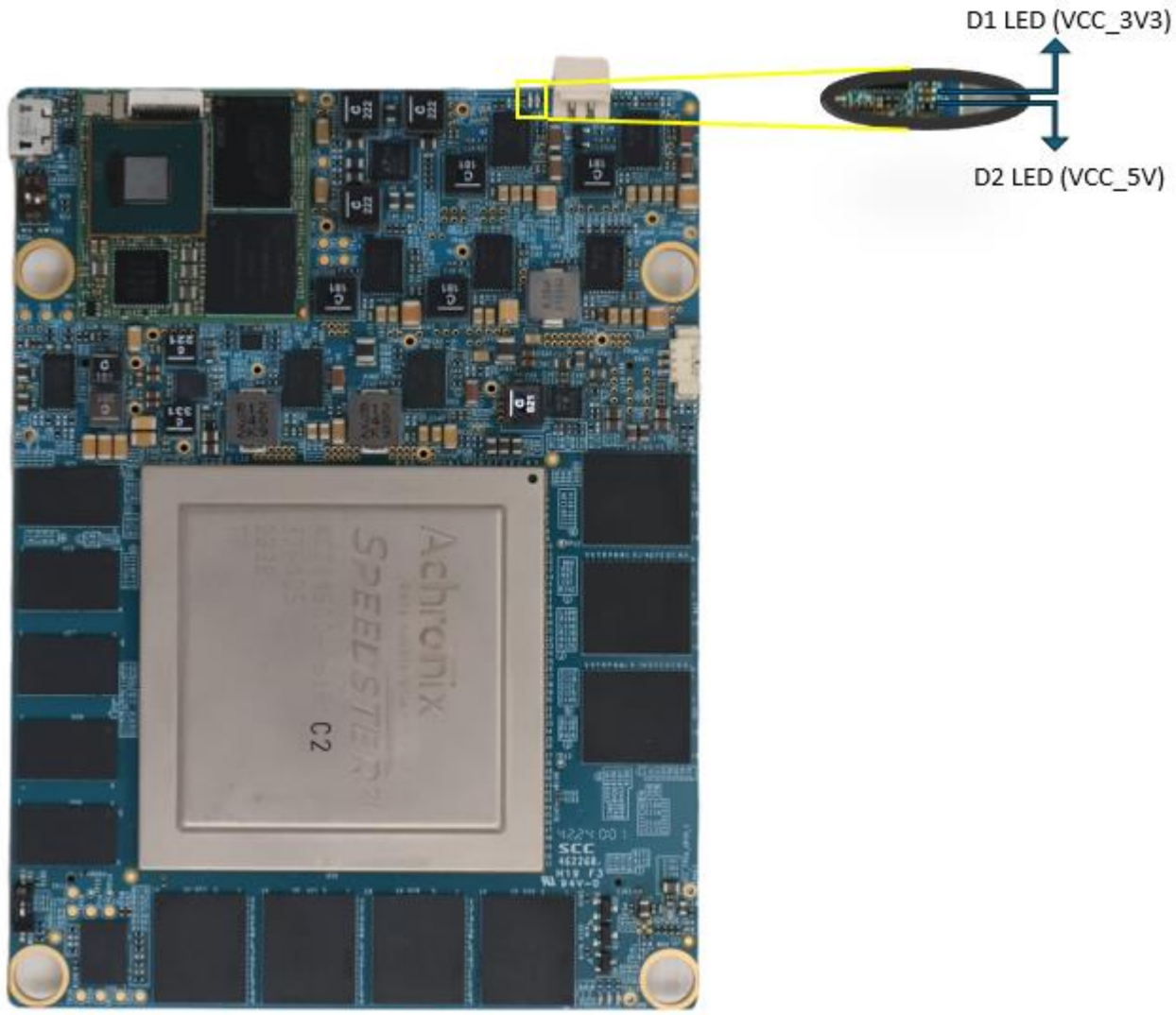


Figure 6 : Power Indication LEDs

2.7.5. Fan Header

The Speedster7t FPGA SOM supports a fan header (J4) to connect cooling Fan if required. The fan header (J4) is physically located on top side of the SOM as shown below.

- Number of Pins - 2
- Connector Part - 52125-02-0200-01 from CNC
- Mating Connector - 52225-02 from CNC

Table 9 : Fan Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_12V	I, 12V Power	Supply Voltage.
2	GND	Power	Ground.

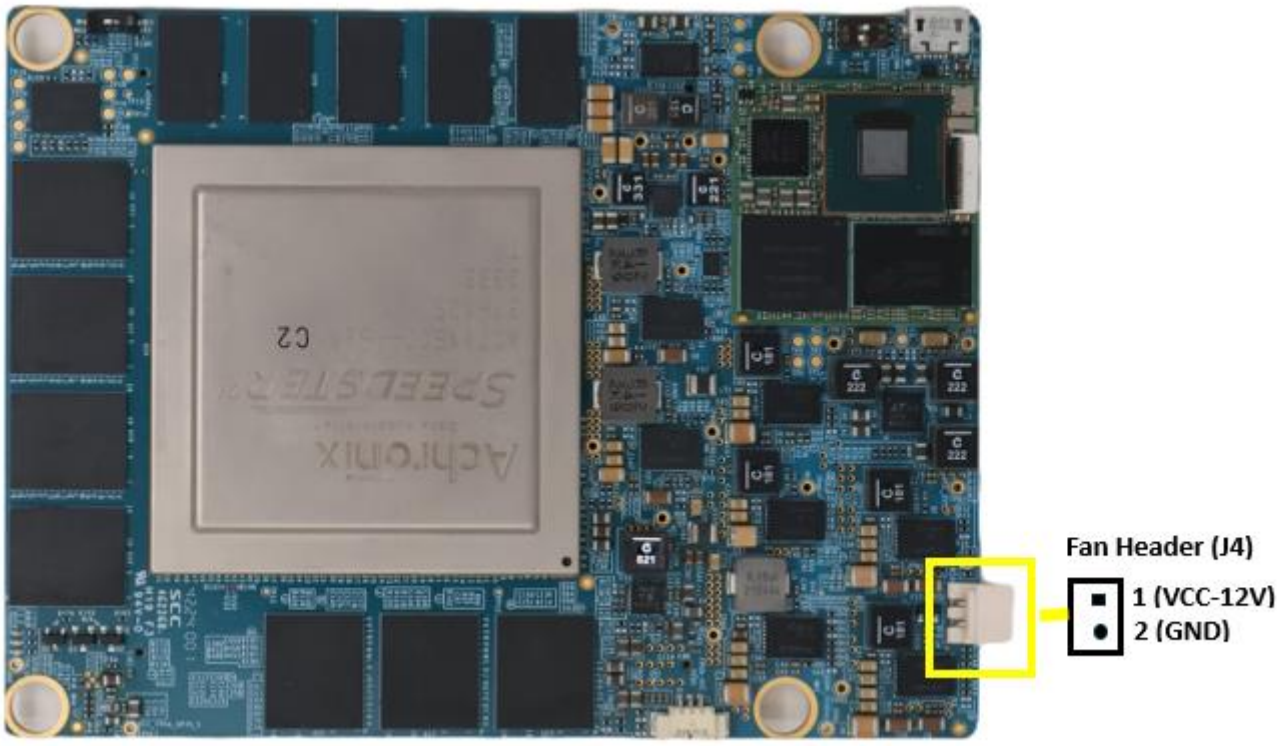


Figure 7 : Fan Header

2.8. Board to Board Connector-1

The Speedster7t FPGA SOM supports two 400 pin high speed ruggedized terminal strip connectors.

The Speedster7t FPGA SOM Board-to-Board Connector 1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector 1 are explained in the following sections. The Board-to-Board Connector 1 (J1) is physically located on bottom side of the SOM.

- Number of Pins - 400
- Connector Part Number - ASP-209946-01 from Samtec
- Mating Connector - ASP-214802-01 from Samtec
- Stacking Height - 5mm

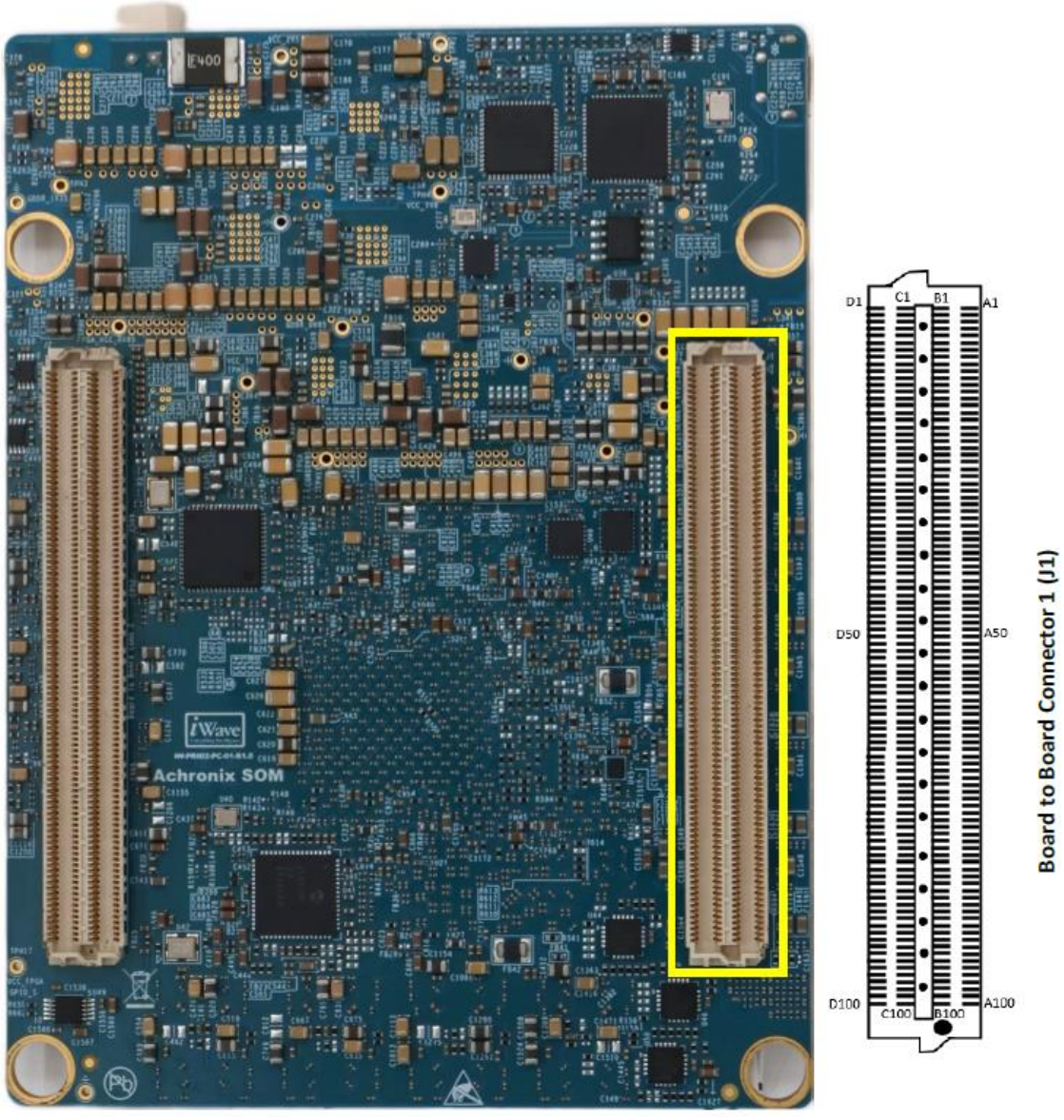


Figure 8 : Board to Board Connector 1

Table 10 : Board-to-Board Connector 1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
NA	A1	B1	NA
FPGA_GPIO19	A2	B2	FPGA_GPIO13
FPGA_GPIO20	A3	B3	FPGA_GPIO14
FPGA_GPIO21	A4	B4	FPGA_GPIO15
FPGA_GPIO22	A5	B5	FPGA_GPIO16
FPGA_GPIO23	A6	B6	FPGA_GPIO17
FPGA_GPIO24	A7	B7	FPGA_GPIO18
GND	A8	B8	GND
NA	A9	B9	NA
NA	A10	B10	NA
NA	A11	B11	NA
NA	A12	B12	NA
NA	A13	B13	NA
NA	A14	B14	NA
GND	A15	B15	GND
NA	A16	B16	OSM_GPIO7
NA	A17	B17	NA
NA	A18	B18	NA
NA	A19	B19	NA
NA	A20	B20	NA
NA	A21	B21	NA
GND	A22	B22	GND
NA	A23	B23	NA
NA	A24	B24	NA
NA	A25	B25	NA
NA	A26	B26	NA
NA	A27	B27	NA
NA	A28	B28	NA
GND	A29	B29	GND
NA	A30	B30	NA
NA	A31	B31	NA
NA	A32	B32	NA
NA	A33	B33	NA
NA	A34	B34	NA
NA	A35	B35	NA
GND	A36	B36	GND
NA	A37	B37	NA
NA	A38	B38	NA
NA	A39	B39	NA
NA	A40	B40	NA
NA	A41	B41	NA

NA	A42	B42	NA
GND	A43	B43	GND
NA	A44	B44	NA
NA	A45	B45	NA
NA	A46	B46	NA
NA	A47	B47	NA
NA	A48	B48	NA
NA	A49	B49	NA
GND	A50	B50	GND
NA	A51	B51	NA
NA	A52	B52	NA
NA	A53	B53	NA
NA	A54	B54	NA
NA	A55	B55	NA
NA	A56	B56	NA
GND	A57	B57	GND
GND	A58	B58	GND
NA	A59	B59	NA
NA	A60	B60	NA
GND	A61	B61	GND
GND	A62	B62	GND
NA	A63	B63	SRDS_N7_TX_P2
NA	A64	B64	SRDS_N7_TX_N2
GND	A65	B65	GND
GND	A66	B66	GND
NA	A67	B67	SRDS_N7_TX_P3
NA	A68	B68	SRDS_N7_TX_N3
GND	A69	B69	GND
GND	A70	B70	GND
NA	A71	B71	NA
NA	A72	B72	NA
GND	A73	B73	GND
GND	A74	B74	GND
NA	A75	B75	NA
NA	A76	B76	NA
GND	A77	B77	GND
GND	A78	B78	GND
SRDS_N7_RX_P2	A79	B79	NA
SRDS_N7_RX_N2	A80	B80	NA
GND	A81	B81	GND
GND	A82	B82	GND
SRDS_N7_RX_P3	A83	B83	SRDS_N7_RX_P1
SRDS_N7_RX_N3	A84	B84	SRDS_N7_RX_N1

GND	A85	B85	GND
GND	A86	B86	GND
NA	A87	B87	NA
NA	A88	B88	NA
GND	A89	B89	GND
GND	A90	B90	GND
NA	A91	B91	SRDS_N7_RX_P0
NA	A92	B92	SRDS_N7_RX_N0
GND	A93	B93	GND
GND	A94	B94	GND
NA	A95	B95	NA
NA	A96	B96	NA
GND	A97	B97	GND
GND	A98	B98	GND
NA	A99	B99	NA
NA	A100	B100	NA
FPGA_VDDIO_1V8	C1	D1	VCC_FPGA_GPIO_S
FPGA_GPIO7	C2	D2	FPGA_GPIO1
FPGA_GPIO8	C3	D3	FPGA_GPIO2
FPGA_GPIO9	C4	D4	FPGA_GPIO3
FPGA_GPIO10	C5	D5	FPGA_GPIO4
FPGA_GPIO11	C6	D6	FPGA_GPIO5
FPGA_GPIO12	C7	D7	FPGA_GPIO6
GND	C8	D8	GND
NA	C9	D9	FPGA_GPIO25
NA	C10	D10	FPGA_GPIO26
NA	C11	D11	NA
NA	C12	D12	NA
NA	C13	D13	NA
NA	C14	D14	NA
GND	C15	D15	GND
OSM_GPIO1	C16	D16	FPGA_GPIO1_1V8
OSM_GPIO2	C17	D17	FPGA_GPIO2_1V8
OSM_GPIO3	C18	D18	FPGA_GPIO3_1V8
OSM_GPIO4	C19	D19	FPGA_GPIO4_1V8
OSM_GPIO5	C20	D20	FPGA_GPIO5_1V8
OSM_GPIO6	C21	D21	FPGA_GPIO6_1V8
GND	C22	D22	GND
NA	C23	D23	NA
NA	C24	D24	NA
NA	C25	D25	NA
NA	C26	D26	NA
NA	C27	D27	NA

NA	C28	D28	NA
GND	C29	D29	GND
NA	C30	D30	NA
NA	C31	D31	NA
NA	C32	D32	NA
NA	C33	D33	NA
NA	C34	D34	NA
NA	C35	D35	NA
GND	C36	D36	GND
NA	C37	D37	NA
NA	C38	D38	NA
NA	C39	D39	NA
NA	C40	D40	NA
NA	C41	D41	NA
NA	C42	D42	NA
GND	C43	D43	GND
NA	C44	D44	NA
NA	C45	D45	NA
NA	C46	D46	NA
NA	C47	D47	NA
NA	C48	D48	NA
NA	C49	D49	NA
GND	C50	D50	GND
NA	C51	D51	NA
NA	C52	D52	NA
NA	C53	D53	NA
NA	C54	D54	NA
NA	C55	D55	NA
NA	C56	D56	NA
GND	C57	D57	GND
GND	C58	D58	GND
NA	C59	D59	NA
NA	C60	D60	NA
GND	C61	D61	GND
GND	C62	D62	GND
SRDS_N7_TX_P1	C63	D63	NA
SRDS_N7_TX_N1	C64	D64	NA
GND	C65	D65	GND
GND	C66	D66	GND
NA	C67	D67	NA
NA	C68	D68	NA
GND	C69	D69	GND
GND	C70	D70	GND

NA	C71	D71	NA
NA	C72	D72	NA
GND	C73	D73	GND
GND	C74	D74	GND
NA	C75	D75	SRDS_N7_TX_P0
NA	C76	D76	SRDS_N7_TX_N0
GND	C77	D77	GND
GND	C78	D78	GND
NA	C79	D79	NA
NA	C80	D80	NA
GND	C81	D81	GND
GND	C82	D82	GND
NA	C83	D83	NA
NA	C84	D84	NA
GND	C85	D85	GND
GND	C86	D86	GND
NA	C87	D87	NA
NA	C88	D88	NA
GND	C89	D89	GND
GND	C90	D90	GND
NA	C91	D91	NA
NA	C92	D92	NA
GND	C93	D93	GND
GND	C94	D94	GND
NA	C95	D95	NA
NA	C96	D96	NA
GND	C97	D97	GND
GND	C98	D98	GND
NA	C99	D99	NA
NA	C100	D100	NA

2.8.1. OSM Interface

The interfaces which are supported in Board-to-Board Connector 1 from OSM are explained in the following section.

2.8.1.1. OSM GPIOs

The Speedster7t FPGA SOM supports 7 SE IOs on Board-to-Board Connector 1 from OSM. By default, IO voltage of OSM GPIO is 1.8V.

For more details on OSM GPIO pinouts in Board-to-Board Connector 1, refer the below table.

Table 11 : OSM GPIO pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	OSM Pin Name	OSM Pin No	Signal Type/ Termination	Description
C16	OSM_GPIO1	GPIO_A_0	D17	IO, 1.8V CMOS	General Purpose IO
C17	OSM_GPIO2	GPIO_A_1	E17	IO, 1.8V CMOS	General Purpose IO
C18	OSM_GPIO3	GPIO_A_2	F17	IO, 1.8V CMOS	General Purpose IO
C19	OSM_GPIO4	GPIO_A_3	G17	IO, 1.8V CMOS	General Purpose IO
C20	OSM_GPIO5	GPIO_A_4	H17	IO, 1.8V CMOS	General Purpose IO
C21	OSM_GPIO6	GPIO_A_5	J17	IO, 1.8V CMOS	General Purpose IO
B16	OSM_GPIO7	GPIO_A_6 / SPI_A_CS1#	K17	IO, 1.8V CMOS	General Purpose IO

2.8.2. FPGA Interface

The interfaces which are supported in Board-to-Board Connector 1 from Speedster7t FPGA is explained in the following section.

2.8.2.1. SERDES Interface

The Speedster7t FPGA SOM supports 4 SERDES transceiver channels through one bank (Bank N7) from Speedster7t FPGA with line rate from 1Gbps to 53.125Gbps on Board-to-Board Connector 1. These transceivers can be used to interface to multiple high-speed interface protocols. Bank N7 is connected to Shared Ethernet and PCIe controller.

On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board.

For more details on SERDES transceiver pinouts in Board-to-Board Connector 1, refer the below table.

Table 12 : SERDES Transceiver Pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
SERDES Bank N7 Transceiver Pins						
D75	SRDS_N7_TX_P0	SRDS_N7_TX_P0	N7	B44	O, DIFF	SERDES Bank N7 channel 0 High speed differential transmitter positive.
D76	SRDS_N7_TX_N0	SRDS_N7_TX_N0	N7	A44	O, DIFF	SERDES Bank N7 channel 0 High speed differential transmitter negative.
B91	SRDS_N7_RX_P0	SRDS_N7_RX_P0	N7	E44	I, DIFF	SERDES Bank N7 channel 0 High speed differential receiver positive.
B92	SRDS_N7_RX_N0	SRDS_N7_RX_N0	N7	D44	I, DIFF	SERDES Bank N7 channel 0 High speed differential receiver negative.
C63	SRDS_N7_TX_P1	SRDS_N7_TX_P1	N7	B46	O, DIFF	SERDES Bank N7 channel 1 High speed differential transmitter positive.
C64	SRDS_N7_TX_N1	SRDS_N7_TX_N1	N7	A46	O, DIFF	SERDES Bank N7 channel 1 High speed differential transmitter negative.
B83	SRDS_N7_RX_P1	SRDS_N7_RX_P1	N7	E46	I, DIFF	SERDES Bank N7 channel 1 High speed differential receiver positive.
B84	SRDS_N7_RX_N1	SRDS_N7_RX_N1	N7	D46	I, DIFF	SERDES Bank N7 channel 1 High speed differential receiver negative.

B63	SRDS_N7_TX_P2	SRDS_N7_TX_P2	N7	B48	O, DIFF	SERDES Bank N7 channel 2 High speed differential transmitter positive.
B64	SRDS_N7_TX_N2	SRDS_N7_TX_N2	N7	A48	O, DIFF	SERDES Bank N7 channel 2 High speed differential transmitter negative.
A79	SRDS_N7_RX_P2	SRDS_N7_RX_P2	N7	E48	I, DIFF	SERDES Bank N7 channel 2 High speed differential receiver positive.
A80	SRDS_N7_RX_N2	SRDS_N7_RX_N2	N7	D48	I, DIFF	SERDES Bank N7 channel 2 High speed differential receiver negative.
B67	SRDS_N7_TX_P3	SRDS_N7_TX_P3	N7	B50	O, DIFF	SERDES Bank N7 channel 3 High speed differential transmitter positive.
B68	SRDS_N7_TX_N3	SRDS_N7_TX_N3	N7	A50	O, DIFF	SERDES Bank N7 channel 3 High speed differential transmitter negative.
A83	SRDS_N7_RX_P3	SRDS_N7_RX_P3	N7	E50	I, DIFF	SERDES Bank N7 channel 3 High speed differential receiver positive.
A84	SRDS_N7_RX_N3	SRDS_N7_RX_N3	N7	D50	I, DIFF	SERDES Bank N7 channel 3 High speed differential receiver negative.

2.8.2.2. FPGA GPIOs

The Speedster7t FPGA SOM supports 16 DIFF IO/32 SE IO on Board-to-Board Connector 1 from Speedster7t FPGA GPIO Bank S0 and N0.

The IO voltage of FPGA GPIO Bank N0 is by default set to 1.8V and does not support variable IO voltage setting.

The IO voltage of GPIO Bank S0 is connected from output of Buck Regulator (U24) and supports variable IO voltage setting. IO voltage is configurable from 1.1V to 1.8V through software. While using as DIFF IOs or SE IOs, make sure to set the buck regulator to output appropriate IO voltage for FPGA GPIO Bank S0. By default, IO voltage of FPGA GPIO Bank S0 is set as 1.8V. For more details about supported IO standard, refer the Speedster7t FPGA datasheet.

For more details on FPGA GPIO pinouts in Board-to-Board Connector 1, refer the below table

Table 13 : FPGA GPIO pinouts

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
D16	FPGA_GPIO1_1V8	GPIO_N0_BYTE2_BIT_0	N0	AP17	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D17	FPGA_GPIO2_1V8	GPIO_N0_BYTE2_BIT_1	N0	AR17	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D18	FPGA_GPIO3_1V8	GPIO_N0_BYTE2_BIT_2	N0	AT17	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D19	FPGA_GPIO4_1V8	GPIO_N0_BYTE2_BIT_3	N0	AV18	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D20	FPGA_GPIO5_1V8	GPIO_N0_BYTE2_BIT_6	N0	AR19	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D21	FPGA_GPIO6_1V8	GPIO_N0_BYTE2_BIT_7	N0	AT20	IO, 1.8V LVCMOS	GPIO Bank N0 General Purpose IO
D2	FPGA_GPIO1	GPIO_S0_BYTE0_BIT_0	S0	BL2	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D3	FPGA_GPIO2	GPIO_S0_BYTE0_BIT_1	S0	BL3	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D4	FPGA_GPIO3	GPIO_S0_BYTE0_BIT_2	S0	BL4	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D5	FPGA_GPIO4	GPIO_S0_BYTE0_BIT_3	S0	BL5	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D6	FPGA_GPIO5	GPIO_S0_BYTE0_BIT_6	S0	BL9	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D7	FPGA_GPIO6	GPIO_S0_BYTE0_BIT_7	S0	BL11	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO

C2	FPGA_GPIO7	GPIO_S0_BYTE0_BIT_8	S0	BL12	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
C3	FPGA_GPIO8	GPIO_S0_BYTE0_BIT_9	S0	BL13	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
C4	FPGA_GPIO9	GPIO_S0_BYTE0_BIT_10	S0	BL14	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
C5	FPGA_GPIO10	GPIO_S0_BYTE0_BIT_11	S0	BL15	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
C6	FPGA_GPIO11	GPIO_S0_BYTE1_BIT_0	S0	BL39	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
C7	FPGA_GPIO12	GPIO_S0_BYTE1_BIT_1	S0	BL40	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B2	FPGA_GPIO13	GPIO_S0_BYTE1_BIT_2	S0	BL41	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B3	FPGA_GPIO14	GPIO_S0_BYTE1_BIT_3	S0	BL42	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B4	FPGA_GPIO15	GPIO_S0_BYTE1_BIT_6	S0	BK44	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B5	FPGA_GPIO16	GPIO_S0_BYTE1_BIT_7	S0	BL45	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B6	FPGA_GPIO17	GPIO_S0_BYTE1_BIT_8	S0	BL46	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
B7	FPGA_GPIO18	GPIO_S0_BYTE1_BIT_9	S0	BL47	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A2	FPGA_GPIO19	GPIO_S0_BYTE1_BIT_10	S0	BL49	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A3	FPGA_GPIO20	GPIO_S0_BYTE1_BIT_11	S0	BL50	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A4	FPGA_GPIO21	GPIO_S0_BYTE2_BIT_0	S0	AU20	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A5	FPGA_GPIO22	GPIO_S0_BYTE2_BIT_1	S0	AW22	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A6	FPGA_GPIO23	GPIO_S0_BYTE2_BIT_2	S0	AV22	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
A7	FPGA_GPIO24	GPIO_S0_BYTE2_BIT_3	S0	AU22	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO
D9	FPGA_GPIO25	GPIO_S0_BYTE2_BIT_6	S0	AW23	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO

D10	FPGA_GPIO26	GPIO_S0_BYTE2_BIT_7	S0	AR23	IO, 1.8V LVCMOS, Programmable	GPIO Bank S0 General Purpose IO

2.8.3. Power Control Input

The Speedster7t FPGA SOM works with 12V power input (VCC_12V) from Board-to-Board Connector 2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector 1, ground pins are distributed throughout the connector for better performance.

For more details on ground pins in Board-to-Board Connector 1, refer the below table.

Table 14 : Ground pins

B2B-1 Pin No	B2B Connector1 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
A8, A15, A22, A29, A36, A43, A50, A57, A58, A61, A62, A65, A66, A69, A70, A73, A74, A77, A78, A81, A82, A85, A86, A89, A90, A93, A94, A97, A98, B8, B15, B22, B29, B36, B43, B50, B57, B58, B61, B62, B65, B66, B69, B70, B73, B74, B77, B78, B81, B82, B85, B86, B89, B90, B93, B94, B97, B98, C8, C15, C22, C29, C36, C43, C50, C57, C58, C61, C62, C65, C66, C69, C70, C73, C74, C77, C78, C81, C82, C85, C86, C89, C90, C93, C94, C97, C98, D8, D15, D22, D29, D36, D43, D50, D57, D58, D61, D62, D65, D66, D69, D70, D73, D74, D77, D78, D81, D82, D85, D86, D89, D90, D93, D94, D97, D98	GND	NA	NA	NA	Power	Ground.

2.9. Board to Board Connector-2

The Speedster7t FPGA SOM Board-to-Board Connector 2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector 2 are explained in the following sections. The Board-to-Board Connector 2 (J2) is physically located on bottom side of the SOM.

- Number of Pins - 400
- Connector Part Number - ASP-209946-01 from Samtec
- Mating Connector - ASP-214802-01 from Samtec
- Stacking Height - 5mm

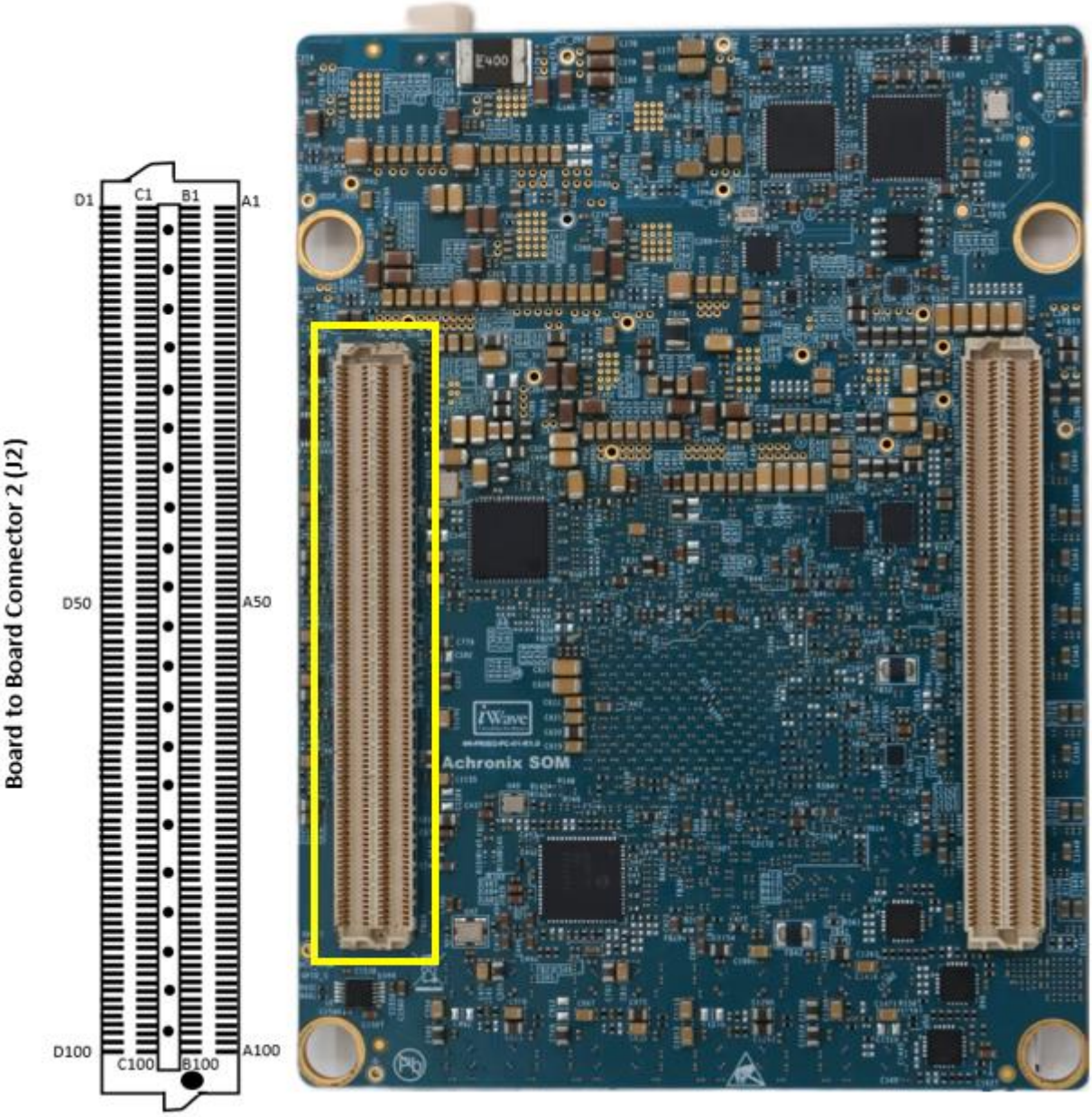


Figure 9 : Board to Board Connector 2

Table 15 : Board-to-Board Connector 2 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_12V	A1	B1	VCC_12V
VCC_12V	A2	B2	VCC_12V
VCC_12V	A3	B3	VCC_12V
VCC_12V	A4	B4	VCC_12V
VCC_12V	A5	B5	VCC_12V
VCC_12V	A6	B6	VCC_12V
VCC_12V	A7	B7	VCC_12V
VCC_12V	A8	B8	VCC_12V
GND	A9	B9	GND
GND	A10	B10	GND
NC	A11	B11	SOM_PWR_EN
NC	A12	B12	Voltage_MON_RST#
NC	A13	B13	NC
NC	A14	B14	RESET#_IN
NC	A15	B15	NC
GND	A16	B16	GND
NC	A17	B17	NC
NC	A18	B18	NC
NC	A19	B19	NC
NC	A20	B20	NC
NC	A21	B21	NC
NC	A22	B22	NC
GND	A23	B23	GND
NC	A24	B24	NC
NC	A25	B25	10MHz_EX_IN
OSM_I2C2_SCL	A26	B26	1PPS_EX_IN
OSM_I2C2_SDA	A27	B27	NC
NC	A28	B28	NC
NC	A29	B29	NC
DBG_UART_TX	A30	B30	NC
DBG_UART_RX	A31	B31	OSM_USB_VBUS
ETH_ACTIVITY_LED1	A32	B32	OSM_USB_B_EN
ETH_LINK_LED0	A33	B33	OSM_USB_B_ID
GND	A34	B34	GND
GPHY_DTXRXM	A35	B35	OSM_USB_B_DN
GPHY_DTXRXP	A36	B36	OSM_USB_B_DP
GND	A37	B37	GND
GPHY_CTXRXM	A38	B38	NC
GPHY_CTXRXP	A39	B39	NC
GND	A40	B40	GND

GPHY_BTXRXM	A41	B41	NC
GPHY_BTXRXP	A42	B42	NC
GND	A43	B43	GND
GPHY_ATXRXM	A44	B44	NC
GPHY_ATXRXP	A45	B45	NC
GND	A46	B46	GND
SRDS_N4_TX_P0	A47	B47	SRDS_N4_RX_P0
SRDS_N4_TX_N0	A48	B48	SRDS_N4_RX_N0
GND	A49	B49	GND
SRDS_N4_TX_P1	A50	B50	SRDS_N4_RX_P1
SRDS_N4_TX_N1	A51	B51	SRDS_N4_RX_N1
GND	A52	B52	GND
SRDS_N4_TX_P2	A53	B53	SRDS_N4_RX_P2
SRDS_N4_TX_N2	A54	B54	SRDS_N4_RX_N2
GND	A55	B55	GND
SRDS_N4_TX_P3	A56	B56	SRDS_N4_RX_P3
SRDS_N4_TX_N3	A57	B57	SRDS_N4_RX_N3
GND	A58	B58	GND
NC	A59	B59	NC
NC	A60	B60	NC
GND	A61	B61	GND
SRDS_N0_TX_P0	A62	B62	SRDS_N0_RX_P0
SRDS_N0_TX_N0	A63	B63	SRDS_N0_RX_N0
GND	A64	B64	GND
SRDS_N0_TX_P1	A65	B65	SRDS_N0_RX_P1
SRDS_N0_TX_N1	A66	B66	SRDS_N0_RX_N1
GND	A67	B67	GND
SRDS_N0_TX_P2	A68	B68	SRDS_N0_RX_P2
SRDS_N0_TX_N2	A69	B69	SRDS_N0_RX_N2
GND	A70	B70	GND
SRDS_N0_TX_P3	A71	B71	SRDS_N0_RX_P3
SRDS_N0_TX_N3	A72	B72	SRDS_N0_RX_N3
GND	A73	B73	GND
NC	A74	B74	NC
NC	A75	B75	NC
GND	A76	B76	GND
SRDS_N2_TX_P0	A77	B77	SRDS_N2_RX_P0
SRDS_N2_TX_N0	A78	B78	SRDS_N2_RX_N0
GND	A79	B79	GND
SRDS_N2_TX_P1	A80	B80	SRDS_N2_RX_P1
SRDS_N2_TX_N1	A81	B81	SRDS_N2_RX_N1
GND	A82	B82	GND
SRDS_N2_TX_P2	A83	B83	SRDS_N2_RX_P2

SRDS_N2_TX_N2	A84	B84	SRDS_N2_RX_N2
GND	A85	B85	GND
SRDS_N2_TX_P3	A86	B86	SRDS_N2_RX_P3
SRDS_N2_TX_N3	A87	B87	SRDS_N2_RX_N3
GND	A88	B88	GND
NC	A89	B89	NC
NC	A90	B90	NC
GND	A91	B91	GND
SRDS_N6_TX_P0	A92	B92	SRDS_N6_RX_P0
SRDS_N6_TX_N0	A93	B93	SRDS_N6_RX_N0
GND	A94	B94	GND
SRDS_N6_TX_P1	A95	B95	SRDS_N6_RX_P1
SRDS_N6_TX_N1	A96	B96	SRDS_N6_RX_N1
GND	A97	B97	GND
NC	A98	B98	NC
NC	A99	B99	NC
GND	A100	B100	GND
VCC_12V	C1	D1	VCC_12V
VCC_12V	C2	D2	VCC_12V
VCC_12V	C3	D3	VCC_12V
VCC_12V	C4	D4	VCC_12V
VCC_12V	C5	D5	VCC_12V
VCC_12V	C6	D6	VCC_12V
VCC_12V	C7	D7	VCC_12V
VCC_12V	C8	D8	VCC_12V
GND	C9	D9	GND
GND	C10	D10	GND
NC	C11	D11	10MHz_B2B_OUT
NC	C12	D12	1PPS_B2B_OUT
NC	C13	D13	NC
NC	C14	D14	DEDICATED_INT
NC	C15	D15	NC
GND	C16	D16	GND
NC	C17	D17	NC
NC	C18	D18	NC
NC	C19	D19	NC
NC	C20	D20	NC
NC	C21	D21	NC
NC	C22	D22	NC
GND	C23	D23	GND
NC	C24	D24	NC
NC	C25	D25	NC
FPGA_PCIE_PERST#	C26	D26	NC

NC	C27	D27	NC
GND	C28	D28	GND
NC	C29	D29	NC
NC	C30	D30	NC
GND	C31	D31	GND
NC	C32	D32	NC
NC	C33	D33	NC
GND	C34	D34	GND
NC	C35	D35	NC
NC	C36	D36	NC
GND	C37	D37	GND
NC	C38	D38	NC
NC	C39	D39	NC
GND	C40	D40	GND
NC	C41	D41	NC
NC	C42	D42	NC
GND	C43	D43	GND
NC	C44	D44	NC
NC	C45	D45	NC
GND	C46	D46	GND
SRDS_N5_TX_P0	C47	D47	SRDS_N5_RX_P0
SRDS_N5_TX_N0	C48	D48	SRDS_N5_RX_N0
GND	C49	D49	GND
SRDS_N5_TX_P1	C50	D50	SRDS_N5_RX_P1
SRDS_N5_TX_N1	C51	D51	SRDS_N5_RX_N1
GND	C52	D52	GND
SRDS_N5_TX_P2	C53	D53	SRDS_N5_RX_P2
SRDS_N5_TX_N2	C54	D54	SRDS_N5_RX_N2
GND	C55	D55	GND
SRDS_N5_TX_P3	C56	D56	SRDS_N5_RX_P3
SRDS_N5_TX_N3	C57	D57	SRDS_N5_RX_N3
GND	C58	D58	GND
NC	C59	D59	NC
NC	C60	D60	NC
GND	C61	D61	GND
SRDS_N1_TX_P0	C62	D62	SRDS_N1_RX_P0
SRDS_N1_TX_N0	C63	D63	SRDS_N1_RX_N0
GND	C64	D64	GND
SRDS_N1_TX_P1	C65	D65	SRDS_N1_RX_P1
SRDS_N1_TX_N1	C66	D66	SRDS_N1_RX_N1
GND	C67	D67	GND
SRDS_N1_TX_P2	C68	D68	SRDS_N1_RX_P2
SRDS_N1_TX_N2	C69	D69	SRDS_N1_RX_N2

GND	C70	D70	GND
SRDS_N1_TX_P3	C71	D71	SRDS_N1_RX_P3
SRDS_N1_TX_N3	C72	D72	SRDS_N1_RX_N3
GND	C73	D73	GND
NC	C74	D74	NC
NC	C75	D75	NC
GND	C76	D76	GND
SRDS_N3_TX_P0	C77	D77	SRDS_N3_RX_P0
SRDS_N3_TX_N0	C78	D78	SRDS_N3_RX_N0
GND	C79	D79	GND
SRDS_N3_TX_P1	C80	D80	SRDS_N3_RX_P1
SRDS_N3_TX_N1	C81	D81	SRDS_N3_RX_N1
GND	C82	D82	GND
SRDS_N3_TX_P2	C83	D83	SRDS_N3_RX_P2
SRDS_N3_TX_N2	C84	D84	SRDS_N3_RX_N2
GND	C85	D85	GND
SRDS_N3_TX_P3	C86	D86	SRDS_N3_RX_P3
SRDS_N3_TX_N3	C87	D87	SRDS_N3_RX_N3
GND	C88	D88	GND
NC	C89	D89	NC
NC	C90	D90	NC
GND	C91	D91	GND
SRDS_N6_TX_P2	C92	D92	SRDS_N6_RX_P2
SRDS_N6_TX_N2	C93	D93	SRDS_N6_RX_N2
GND	C94	D94	GND
SRDS_N6_TX_P3	C95	D95	SRDS_N6_RX_P3
SRDS_N6_TX_N3	C96	D96	SRDS_N6_RX_N3
GND	C97	D97	GND
NC	C98	D98	NC
NC	C99	D99	NC
GND	C100	D100	GND

2.9.1. OSM Interface

The interfaces which are supported in Board-to-Board Connector 2 from OSM are explained in the following section.

2.9.1.1. Gigabit Ethernet Interface

The Speedster7t FPGA SOM supports 1G Ethernet interface in Board-to-Board Connector 2. MAC is integrated in the OSM and connected to the external Gigabit ethernet PHY "88E1512-A0-NNP2I000" on SOM. This Gigabit ethernet PHY is interfaced with ENET0 controller of OSM and works at 1.8V IO voltage level. This PHY supports active high Link and activity LED indication signals and is available in Board-to-Board Connector 2. Since MAC and PHY are supported on SOM itself, only magnetics is required on the carrier board.

In Speedster7t FPGA SOM, ethernet PHY address is 000.

For more details on Gigabit ethernet interface pinouts in Board-to-Board Connector 2, refer the below table.

Table 16 : Gigabit Ethernet Interface pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	OSM Pin Name	OSM Bank	OSM Pin No	Signal Type/ Termination	Description
A35	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
A36	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
A38	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A39	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
A41	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A42	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A44	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A45	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A33	ETH_LINK_LED0	NA	NA	NA	O, 1.8V CMOS	Gigabit Ethernet 1000Mbps Link status LED (Active High).
A32	ETH_ACTIVITY_LED1	NA	NA	NA	O, 1.8V CMOS	Gigabit Ethernet Activity LED (Active High).

2.9.1.2. USB2.0 Device Interface

The Speedster7t FPGA SOM supports one USB2.0 device interface in Board-to-Board Connector 2. USB_OTG2 controller of OSM is used for USB2.0 device interface. This controller supports all high-speed, full-speed and low-speed transfers in device mode.

Speedster7t FPGA SOM supports USB VBUS inputs from Board-to-Board Connector 2 for VBUS monitoring purpose.

For more details on USB2.0 device interface pinouts in Board-to-Board Connector 2, refer the below table.

Table 17 : USB2.0 Device Interface pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	OSM Pin Name	OSM Bank	OSM Pin No	Signal Type/ Termination	Description
B35	OSM_USB_B_DN	USB_B_D_N	NA	AB23	IO, USB	USB Host data negative.
B36	OSM_USB_B_DP	USB_B_D_P	NA	AC22	IO, USB	USB Host data positive.
B32	OSM_USB_B_EN	USB_B_EN	NA	AC20	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.
B33	OSM_USB_B_ID	USB_B_ID	NA	AB22	I, 3.3V CMOS	USB Host ID input for USB host or device detection.
B31	OSM_USB_VBUS	USB_B_VBUS	NA	AB20	I, 5V Power	USB VBUS for VBUS monitoring.

2.9.1.3. Debug UART Interface

The Speedster7t FPGA SOM supports one Debug UART interface on Board-to-Board Connector 2. The UART0 controller of OSM is used for Debug UART interface. It works at 1.8V IO voltage level.

For more details on Debug UART interface pinouts in Board-to-Board Connector 2, refer the below table.

Table 18 : Debug UART interface pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	OSM Pin Name	OSM Bank	OSM Pin No	Signal Type/ Termination	Description
A30	DBG_UART_TX	UART_CON_TX	NA	D23	O, 1.8V CMOS	UART0 Transmit data line for Debug.
A31	DBG_UART_RX	UART_CON_RX	NA	D22	I, 1.8V CMOS	UART0 Receive data line for Debug.

2.9.1.4. I2C Interface

The Speedster7t FPGA SOM supports one I2C interface in Board-to-Board Connector 2. The I2C2 controller of OSM is used for I2C interface. It supports standard mode with data transfer rates of up to 100Kbps and fast mode with data transfer rates of up to 400Kbps.

For more details on I2C interface pinouts in Board-to-Board Connector 2, refer the below table.

Table 19 : I2C Interface pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	OSM Pin Name	OSM Bank	OSM Pin No	Signal Type/ Termination	Description
A27	OSM_I2C2_SDA	I2C_A_SDA	NA	AA16	IO, 1.8V OD/ 4.7K PU	I2C2 data.
A26	OSM_I2C2_SCL	I2C_A_SCL	NA	AA15	O, 1.8V OD/ 4.7K PU	I2C2 clock.

2.9.2. FPGA Interface

The interfaces which are supported in Board-to-Board Connector 2 from Speedster7t FPGA is explained in the following section.

2.9.2.1. SERDES Interface

The Speedster7t FPGA SOM supports 28 SERDES transceiver channels through seven banks (Bank N0, N1, N2, N3, N4, N5, N6) from Speedster7t FPGA with line rate from 1Gbps to 53.125Gbps on Board-to-Board Connector 2. These transceivers can be used to interface to multiple high-speed interface protocols. Bank N0, N1, N2, N3 are connected to hard PCIe controller of Speedster7t FPGA. Bank N4, N5 are connected to hard Ethernet controller of Speedster7t FPGA. Bank N6 is connected to shared Ethernet and PCIe controller.

On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board.

For more details on SERDES transceiver pinouts on Board-to-Board Connector 2, refer the below table.

Table 20 : SERDES transceiver pinouts

B2B-2 Pin No	B2B Connector2 Signal Name	FPGA Pin Name	FPGA Bank	FPGA Pin No	Signal Type/ Termination	Description
SERDES Bank N0 Transceiver Pins						
A62	SRDS_N0_TX_P0	SRDS_N0_TX_P0	N0	B2	O, DIFF	SERDES Bank N0 channel 0 High speed differential transmitter positive.
A63	SRDS_N0_TX_N0	SRDS_N0_TX_N0	N0	A2	O, DIFF	SERDES Bank N0 channel 0 High speed differential transmitter negative.
B62	SRDS_N0_RX_P0	SRDS_N0_RX_P0	N0	E2	I, DIFF	SERDES Bank N0 channel 0 High speed differential receiver positive.
B63	SRDS_N0_RX_N0	SRDS_N0_RX_N0	N0	D2	I, DIFF	SERDES Bank N0 channel 0 High speed differential receiver negative.
A65	SRDS_N0_TX_P1	SRDS_N0_TX_P1	N0	B4	O, DIFF	SERDES Bank N0 channel 1 High speed differential transmitter positive.
A66	SRDS_N0_TX_N1	SRDS_N0_TX_N1	N0	A4	O, DIFF	SERDES Bank N0 channel 1 High speed differential transmitter negative.
B65	SRDS_N0_RX_P1	SRDS_N0_RX_P1	N0	E4	I, DIFF	SERDES Bank N0 channel 1 High speed differential receiver positive.

B66	SRDS_N0_RX_N1	SRDS_N0_RX_N1	N0	D4	I, DIFF	SERDES Bank N0 channel 1 High speed differential receiver negative.
A68	SRDS_N0_TX_P2	SRDS_N0_TX_P2	N0	B6	O, DIFF	SERDES Bank N0 channel 2 High speed differential transmitter positive.
A69	SRDS_N0_TX_N2	SRDS_N0_TX_N2	N0	A6	O, DIFF	SERDES Bank N0 channel 2 High speed differential transmitter negative.
B68	SRDS_N0_RX_P2	SRDS_N0_RX_P2	N0	E6	I, DIFF	SERDES Bank N0 channel 2 High speed differential receiver positive.
B69	SRDS_N0_RX_N2	SRDS_N0_RX_N2	N0	D6	I, DIFF	SERDES Bank N0 channel 2 High speed differential receiver negative.
A71	SRDS_N0_TX_P3	SRDS_N0_TX_P3	N0	B8	O, DIFF	SERDES Bank N0 channel 3 High speed differential transmitter positive.
A72	SRDS_N0_TX_N3	SRDS_N0_TX_N3	N0	A8	O, DIFF	SERDES Bank N0 channel 3 High speed differential transmitter negative.
B71	SRDS_N0_RX_P3	SRDS_N0_RX_P3	N0	E8	I, DIFF	SERDES Bank N0 channel 3 High speed differential receiver positive.
B72	SRDS_N0_RX_N3	SRDS_N0_RX_N3	N0	D8	I, DIFF	SERDES Bank N0 channel 3 High speed differential receiver negative.
SERDES Bank N1 Transceiver Pins						
C62	SRDS_N1_TX_P0	SRDS_N1_TX_P0	N1	B10	O, DIFF	SERDES Bank N1 channel 0 High speed differential transmitter positive.
C63	SRDS_N1_TX_N0	SRDS_N1_TX_N0	N1	A10	O, DIFF	SERDES Bank N1 channel 0 High speed differential transmitter negative.
D62	SRDS_N1_RX_P0	SRDS_N1_RX_P0	N1	E10	I, DIFF	SERDES Bank N1 channel 0 High speed differential receiver positive.
D63	SRDS_N1_RX_N0	SRDS_N1_RX_N0	N1	D10	I, DIFF	SERDES Bank N1 channel 0 High speed differential receiver negative.
C65	SRDS_N1_TX_P1	SRDS_N1_TX_P1	N1	B12	O, DIFF	SERDES Bank N1 channel 1 High speed differential transmitter positive.
C66	SRDS_N1_TX_N1	SRDS_N1_TX_N1	N1	A12	O, DIFF	SERDES Bank N1 channel 1 High speed differential transmitter negative.

D65	SRDS_N1_RX_P1	SRDS_N1_RX_P1	N1	E12	I, DIFF	SERDES Bank N1 channel 1 High speed differential receiver positive.
D66	SRDS_N1_RX_N1	SRDS_N1_RX_N1	N1	D12	I, DIFF	SERDES Bank N1 channel 1 High speed differential receiver negative.
C68	SRDS_N1_TX_P2	SRDS_N1_TX_P2	N1	B14	O, DIFF	SERDES Bank N1 channel 2 High speed differential transmitter positive.
C69	SRDS_N1_TX_N2	SRDS_N1_TX_N2	N1	A14	O, DIFF	SERDES Bank N1 channel 2 High speed differential transmitter negative.
D68	SRDS_N1_RX_P2	SRDS_N1_RX_P2	N1	E14	I, DIFF	SERDES Bank N1 channel 2 High speed differential receiver positive.
D69	SRDS_N1_RX_N2	SRDS_N1_RX_N2	N1	D14	I, DIFF	SERDES Bank N1 channel 2 High speed differential receiver negative.
C71	SRDS_N1_TX_P3	SRDS_N1_TX_P3	N1	B16	O, DIFF	SERDES Bank N1 channel 3 High speed differential transmitter positive.
C72	SRDS_N1_TX_N3	SRDS_N1_TX_N3	N1	A16	O, DIFF	SERDES Bank N1 channel 3 High speed differential transmitter negative.
D71	SRDS_N1_RX_P3	SRDS_N1_RX_P3	N1	E16	I, DIFF	SERDES Bank N1 channel 3 High speed differential receiver positive.
D72	SRDS_N1_RX_N3	SRDS_N1_RX_N3	N1	D16	I, DIFF	SERDES Bank N1 channel 3 High speed differential receiver negative.
SERDES Bank N2 Transceiver Pins						
A77	SRDS_N2_TX_P0	SRDS_N2_TX_P0	N2	B18	O, DIFF	SERDES Bank N2 channel 0 High speed differential transmitter positive.
A78	SRDS_N2_TX_N0	SRDS_N2_TX_N0	N2	A18	O, DIFF	SERDES Bank N2 channel 0 High speed differential transmitter negative.
B77	SRDS_N2_RX_P0	SRDS_N2_RX_P0	N2	H18	I, DIFF	SERDES Bank N2 channel 0 High speed differential receiver positive.
B78	SRDS_N2_RX_N0	SRDS_N2_RX_N0	N2	G18	I, DIFF	SERDES Bank N2 channel 0 High speed differential receiver negative.
A80	SRDS_N2_TX_P1	SRDS_N2_TX_P1	N2	E18	O, DIFF	SERDES Bank N2 channel 1 High speed differential transmitter positive.

A81	SRDS_N2_TX_N1	SRDS_N2_TX_N1	N2	D18	O, DIFF	SERDES Bank N2 channel 1 High speed differential transmitter negative.
B80	SRDS_N2_RX_P1	SRDS_N2_RX_P1	N2	L18	I, DIFF	SERDES Bank N2 channel 1 High speed differential receiver positive.
B81	SRDS_N2_RX_N1	SRDS_N2_RX_N1	N2	K18	I, DIFF	SERDES Bank N2 channel 1 High speed differential receiver negative.
A83	SRDS_N2_TX_P2	SRDS_N2_TX_P2	N2	B20	O, DIFF	SERDES Bank N2 channel 2 High speed differential transmitter positive.
A84	SRDS_N2_TX_N2	SRDS_N2_TX_N2	N2	A20	O, DIFF	SERDES Bank N2 channel 2 High speed differential transmitter negative.
B83	SRDS_N2_RX_P2	SRDS_N2_RX_P2	N2	H20	I, DIFF	SERDES Bank N2 channel 2 High speed differential receiver positive.
B84	SRDS_N2_RX_N2	SRDS_N2_RX_N2	N2	G20	I, DIFF	SERDES Bank N2 channel 2 High speed differential receiver negative.
A86	SRDS_N2_TX_P3	SRDS_N2_TX_P3	N2	E20	O, DIFF	SERDES Bank N2 channel 3 High speed differential transmitter positive.
A87	SRDS_N2_TX_N3	SRDS_N2_TX_N3	N2	D20	O, DIFF	SERDES Bank N2 channel 3 High speed differential transmitter negative.
B86	SRDS_N2_RX_P3	SRDS_N2_RX_P3	N2	L20	I, DIFF	SERDES Bank N2 channel 3 High speed differential receiver positive.
B87	SRDS_N2_RX_N3	SRDS_N2_RX_N3	N2	K20	I, DIFF	SERDES Bank N2 channel 3 High speed differential receiver negative.
SERDES Bank N3 Transceiver Pins						
C77	SRDS_N3_TX_P0	SRDS_N3_TX_P0	N3	B22	O, DIFF	SERDES Bank N3 channel 0 High speed differential transmitter positive.
C78	SRDS_N3_TX_N0	SRDS_N3_TX_N0	N3	A22	O, DIFF	SERDES Bank N3 channel 0 High speed differential transmitter negative.
D77	SRDS_N3_RX_P0	SRDS_N3_RX_P0	N3	H22	I, DIFF	SERDES Bank N3 channel 0 High speed differential receiver positive.
D78	SRDS_N3_RX_N0	SRDS_N3_RX_N0	N3	G22	I, DIFF	SERDES Bank N3 channel 0 High speed differential receiver negative.

C80	SRDS_N3_TX_P1	SRDS_N3_TX_P1	N3	E22	O, DIFF	SERDES Bank N3 channel 1 High speed differential transmitter positive.
C81	SRDS_N3_TX_N1	SRDS_N3_TX_N1	N3	D22	O, DIFF	SERDES Bank N3 channel 1 High speed differential transmitter negative.
D80	SRDS_N3_RX_P1	SRDS_N3_RX_P1	N3	L22	I, DIFF	SERDES Bank N3 channel 1 High speed differential receiver positive.
D81	SRDS_N3_RX_N1	SRDS_N3_RX_N1	N3	K22	I, DIFF	SERDES Bank N3 channel 1 High speed differential receiver negative.
C83	SRDS_N3_TX_P2	SRDS_N3_TX_P2	N3	B24	O, DIFF	SERDES Bank N3 channel 2 High speed differential transmitter positive.
C84	SRDS_N3_TX_N2	SRDS_N3_TX_N2	N3	A24	O, DIFF	SERDES Bank N3 channel 2 High speed differential transmitter negative.
D83	SRDS_N3_RX_P2	SRDS_N3_RX_P2	N3	H24	I, DIFF	SERDES Bank N3 channel 2 High speed differential receiver positive.
D84	SRDS_N3_RX_N2	SRDS_N3_RX_N2	N3	G24	I, DIFF	SERDES Bank N3 channel 2 High speed differential receiver negative.
C86	SRDS_N3_TX_P3	SRDS_N3_TX_P3	N3	E24	O, DIFF	SERDES Bank N3 channel 3 High speed differential transmitter positive.
C87	SRDS_N3_TX_N3	SRDS_N3_TX_N3	N3	D24	O, DIFF	SERDES Bank N3 channel 3 High speed differential transmitter negative.
D86	SRDS_N3_RX_P3	SRDS_N3_RX_P3	N3	L24	I, DIFF	SERDES Bank N3 channel 3 High speed differential receiver positive.
D87	SRDS_N3_RX_N3	SRDS_N3_RX_N3	N3	K24	I, DIFF	SERDES Bank N3 channel 3 High speed differential receiver negative.
SERDES Bank N4 Transceiver Pins						
A47	SRDS_N4_TX_P0	SRDS_N4_TX_P0	N4	B28	O, DIFF	SERDES Bank N4 channel 0 High speed differential transmitter positive.
A48	SRDS_N4_TX_N0	SRDS_N4_TX_N0	N4	A28	O, DIFF	SERDES Bank N4 channel 0 High speed differential transmitter negative.
B47	SRDS_N4_RX_P0	SRDS_N4_RX_P0	N4	H28	I, DIFF	SERDES Bank N4 channel 0 High speed differential receiver positive.

B48	SRDS_N4_RX_N0	SRDS_N4_RX_N0	N4	G28	I, DIFF	SERDES Bank N4 channel 0 High speed differential receiver negative.
A50	SRDS_N4_TX_P1	SRDS_N4_TX_P1	N4	E28	O, DIFF	SERDES Bank N4 channel 1 High speed differential transmitter positive.
A51	SRDS_N4_TX_N1	SRDS_N4_TX_N1	N4	D28	O, DIFF	SERDES Bank N4 channel 1 High speed differential transmitter negative.
B50	SRDS_N4_RX_P1	SRDS_N4_RX_P1	N4	L28	I, DIFF	SERDES Bank N4 channel 1 High speed differential receiver positive.
B51	SRDS_N4_RX_N1	SRDS_N4_RX_N1	N4	K28	I, DIFF	SERDES Bank N4 channel 1 High speed differential receiver negative.
A53	SRDS_N4_TX_P2	SRDS_N4_TX_P2	N4	B30	O, DIFF	SERDES Bank N4 channel 2 High speed differential transmitter positive.
A54	SRDS_N4_TX_N2	SRDS_N4_TX_N2	N4	A30	O, DIFF	SERDES Bank N4 channel 2 High speed differential transmitter negative.
B53	SRDS_N4_RX_P2	SRDS_N4_RX_P2	N4	H30	I, DIFF	SERDES Bank N4 channel 2 High speed differential receiver positive.
B54	SRDS_N4_RX_N2	SRDS_N4_RX_N2	N4	G30	I, DIFF	SERDES Bank N4 channel 2 High speed differential receiver negative.
A56	SRDS_N4_TX_P3	SRDS_N4_TX_P3	N4	E30	O, DIFF	SERDES Bank N4 channel 3 High speed differential transmitter positive.
A57	SRDS_N4_TX_N3	SRDS_N4_TX_N3	N4	D30	O, DIFF	SERDES Bank N4 channel 3 High speed differential transmitter negative.
B56	SRDS_N4_RX_P3	SRDS_N4_RX_P3	N4	L30	I, DIFF	SERDES Bank N4 channel 3 High speed differential receiver positive.
B57	SRDS_N4_RX_N3	SRDS_N4_RX_N3	N4	K30	I, DIFF	SERDES Bank N4 channel 3 High speed differential receiver negative.
SERDES Bank N5 Transceiver Pins						
C47	SRDS_N5_TX_P0	SRDS_N5_TX_P0	N5	B32	O, DIFF	SERDES Bank N5 channel 0 High speed differential transmitter positive.
C48	SRDS_N5_TX_N0	SRDS_N5_TX_N0	N5	A32	O, DIFF	SERDES Bank N5 channel 0 High speed differential transmitter negative.

D47	SRDS_N5_RX_P0	SRDS_N5_RX_P0	N5	H32	I, DIFF	SERDES Bank N5 channel 0 High speed differential receiver positive.
D48	SRDS_N5_RX_N0	SRDS_N5_RX_N0	N5	G32	I, DIFF	SERDES Bank N5 channel 0 High speed differential receiver negative.
C50	SRDS_N5_TX_P1	SRDS_N5_TX_P1	N5	E32	O, DIFF	SERDES Bank N5 channel 1 High speed differential transmitter positive.
C51	SRDS_N5_TX_N1	SRDS_N5_TX_N1	N5	D32	O, DIFF	SERDES Bank N5 channel 1 High speed differential transmitter negative.
D50	SRDS_N5_RX_P1	SRDS_N5_RX_P1	N5	L32	I, DIFF	SERDES Bank N5 channel 1 High speed differential receiver positive.
D51	SRDS_N5_RX_N1	SRDS_N5_RX_N1	N5	K32	I, DIFF	SERDES Bank N5 channel 1 High speed differential receiver negative.
C53	SRDS_N5_TX_P2	SRDS_N5_TX_P2	N5	B34	O, DIFF	SERDES Bank N5 channel 2 High speed differential transmitter positive.
C54	SRDS_N5_TX_N2	SRDS_N5_TX_N2	N5	A34	O, DIFF	SERDES Bank N5 channel 2 High speed differential transmitter negative.
D53	SRDS_N5_RX_P2	SRDS_N5_RX_P2	N5	H34	I, DIFF	SERDES Bank N5 channel 2 High speed differential receiver positive.
D54	SRDS_N5_RX_N2	SRDS_N5_RX_N2	N5	G34	I, DIFF	SERDES Bank N5 channel 2 High speed differential receiver negative.
C56	SRDS_N5_TX_P3	SRDS_N5_TX_P3	N5	E34	O, DIFF	SERDES Bank N5 channel 3 High speed differential transmitter positive.
C57	SRDS_N5_TX_N3	SRDS_N5_TX_N3	N5	D34	O, DIFF	SERDES Bank N5 channel 3 High speed differential transmitter negative.
D56	SRDS_N5_RX_P3	SRDS_N5_RX_P3	N5	L34	I, DIFF	SERDES Bank N5 channel 3 High speed differential receiver positive.
D57	SRDS_N5_RX_N3	SRDS_N5_RX_N3	N5	K34	I, DIFF	SERDES Bank N5 channel 3 High speed differential receiver negative.
SERDES Bank N6 Transceiver Pins						
A92	SRDS_N6_TX_P0	SRDS_N6_TX_P0	N6	B36	O, DIFF	SERDES Bank N6 channel 0 High speed differential transmitter positive.

A93	SRDS_N6_TX_N0	SRDS_N6_TX_N0	N6	A36	O, DIFF	SERDES Bank N6 channel 0 High speed differential transmitter negative.
B92	SRDS_N6_RX_P0	SRDS_N6_RX_P0	N6	E36	I, DIFF	SERDES Bank N6 channel 0 High speed differential receiver positive.
B93	SRDS_N6_RX_N0	SRDS_N6_RX_N0	N6	D36	I, DIFF	SERDES Bank N6 channel 0 High speed differential receiver negative.
A95	SRDS_N6_TX_P1	SRDS_N6_TX_P1	N6	B38	O, DIFF	SERDES Bank N6 channel 1 High speed differential transmitter positive.
A96	SRDS_N6_TX_N1	SRDS_N6_TX_N1	N6	A38	O, DIFF	SERDES Bank N6 channel 1 High speed differential transmitter negative.
B95	SRDS_N6_RX_P1	SRDS_N6_RX_P1	N6	E38	I, DIFF	SERDES Bank N6 channel 1 High speed differential receiver positive.
B96	SRDS_N6_RX_N1	SRDS_N6_RX_N1	N6	D38	I, DIFF	SERDES Bank N6 channel 1 High speed differential receiver negative.
C92	SRDS_N6_TX_P2	SRDS_N6_TX_P2	N6	B40	O, DIFF	SERDES Bank N6 channel 2 High speed differential transmitter positive.
C93	SRDS_N6_TX_N2	SRDS_N6_TX_N2	N6	A40	O, DIFF	SERDES Bank N6 channel 2 High speed differential transmitter negative.
D92	SRDS_N6_RX_P2	SRDS_N6_RX_P2	N6	E40	I, DIFF	SERDES Bank N6 channel 2 High speed differential receiver positive.
D93	SRDS_N6_RX_N2	SRDS_N6_RX_N2	N6	D40	I, DIFF	SERDES Bank N6 channel 2 High speed differential receiver negative.
C95	SRDS_N6_TX_P3	SRDS_N6_TX_P3	N6	B42	O, DIFF	SERDES Bank N6 channel 3 High speed differential transmitter positive.
C96	SRDS_N6_TX_N3	SRDS_N6_TX_N3	N6	A42	O, DIFF	SERDES Bank N6 channel 3 High speed differential transmitter negative.
D95	SRDS_N6_RX_P3	SRDS_N6_RX_P3	N6	E42	I, DIFF	SERDES Bank N6 channel 3 High speed differential receiver positive.
D96	SRDS_N6_RX_N3	SRDS_N6_RX_N3	N6	D42	I, DIFF	SERDES Bank N6 channel 3 High speed differential receiver negative.

2.9.3. Power and Reset Input

The Speedster7t FPGA SOM works with 12V power input (VCC_12V) from Board-to-Board Connector 2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM power enable pin (pin B11) in Board-to-Board Connector 2. SOM supports reset input from Board-to-Board Connector 2 and it is connected to SYS_RST# pin (pin U17) of OSM. In Board-to-Board Connector 2, ground pins are distributed throughout the connector for better performance.

For more details on Power pins in Board-to-Board Connector 2, refer the below table.

Table 21 : Power pins

B2B-2 Pin No	B2B Connector2 Signal Name	Pin Name	Signal Type/ Termination	Description
A1, A2, A3, A4, A5, A6, A7, A8, B1, B2, B3, B4, B5, B6, B7, B8, C1, C2, C3, C4, C5, C6, C7, C8, D1, D2, D3, D4, D5, D6, D7, D8	VCC_12V	NA	Power	12V SOM Input Power
A9, A10, A16, A23, A34, A37, A40, A43, A46, A49, A52, A55, A58, A61, A64, A67, A70, A73, A76, A79, A82, A85, A88, A91, A94, A97, A100, B9, B10, B16, B23, B34, B37, B40, B43, B46, B49, B52, B55, B58, B61, B64, B67, B70, B73, B76, B79, B82, B85, B88, B91, B94, B97, B100, C9, C10, C16, C23,C28, C31 C34, C37, C40, C43, C46, C49, C52, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, C100, D9, D10, D16, D23,D28, D31, D34, D37, D40, D43, D46, D49, D52, D55, D58, D61, D64, D67, D70, D73, D76, D79, D82, D85, D88, D91, D94, D97, D100	GND	NA	Power	Ground
B11	SOM_PWR_EN	NA	OD/ Input	Control signal for controlling SOM Power.
B14	RESET#_IN	SYS_RST#	1.8V Input/ 10K PU	Control Signal to reset the CPU.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Speedster7t FPGA SOM technical specification with electrical, environmental and mechanical characteristics.

3.1. Electrical Characteristics

3.1.1. Power Input Requirement

The below table provides the power input requirement of Speedster7t FPGA SOM.

Table 22 : Power Input

Sl. No.	Power Rail	Min (V)	Typical (V)	Max (V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.2V	±50mV

[1] Speedster7t FPGA SOM is designed to work with VCC_12V input power rail from Board-to-Board Connector 2.

3.1.2. Power Input Sequencing

There is only a single power sequencing requirement applicable for the Speedster7t family of devices. The VCC core power supply (0.85V) should be brought up before the EFUSE_VDD2 (1.8V) and pulled down after EFUSE2_VDD2 is pulled down. This sequencing is to ensure that there is no unwanted leakage when powering up the device.

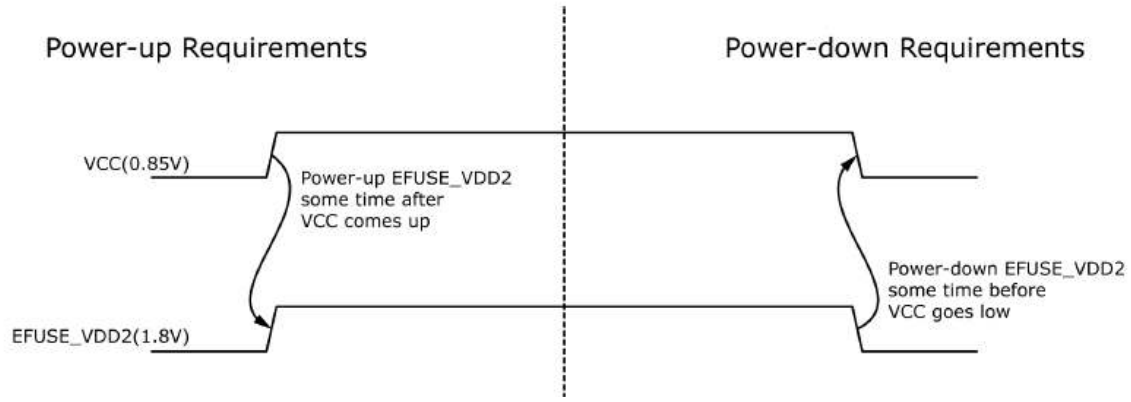


Figure 10 : Speedster7t FPGA Power Input Sequence

3.1.3. Power Consumption

The Speedster7t FPGA SOM power consumption is considered by calculating power required for both Speedster7t FPGA device and OSM.

The CPU power consumption is calculated based on OSM datasheet power requirement. The Speedster7t FPGA power is calculated using the Achronix Power Estimation (XPE) tool.

For more accurate power estimation, iWave recommends to use Achronix Power Estimator (XPE) tool and calculate the Speedster7t FPGA power as per the design requirement.

Table 23 : Power Consumption

Task/Status	Power Rail	Current Drawn/Power Consumption
Initial SOM Power ON	VCC_12V	1.86A/22.32W
Programming FPGA with ADM Disabled		7.58A/90.96W
Programming FPGA with ADM Enabled		11.5A/138W
DDR4 Read/Write GDDR6 Read/Write		12.8A/153.6W
DDR4 Read/Write GDDR6 Read/Write 32 SERDES (53.125 Gbps) Loopback Test		14.9A/178.8W
DDR4 Read/Write GDDR6 Read/Write 32 SERDES (112 Gbps) Loopback Test		17.2A/206.4W

NOTE: This measurement is done in Achronix Speedster7t -2 speed grade FPGA with iWave's FPGA design at an ambient temperature of 25℃

3.2. Environmental Characteristics

3.2.1. Temperature Specification

The below table provides the environmental specification of Speedster7t FPGA SOM.

Table 24 : Temperature Range

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Commercial[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2. RoHS2 Compliance

iWave's Speedster7t FPGA SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

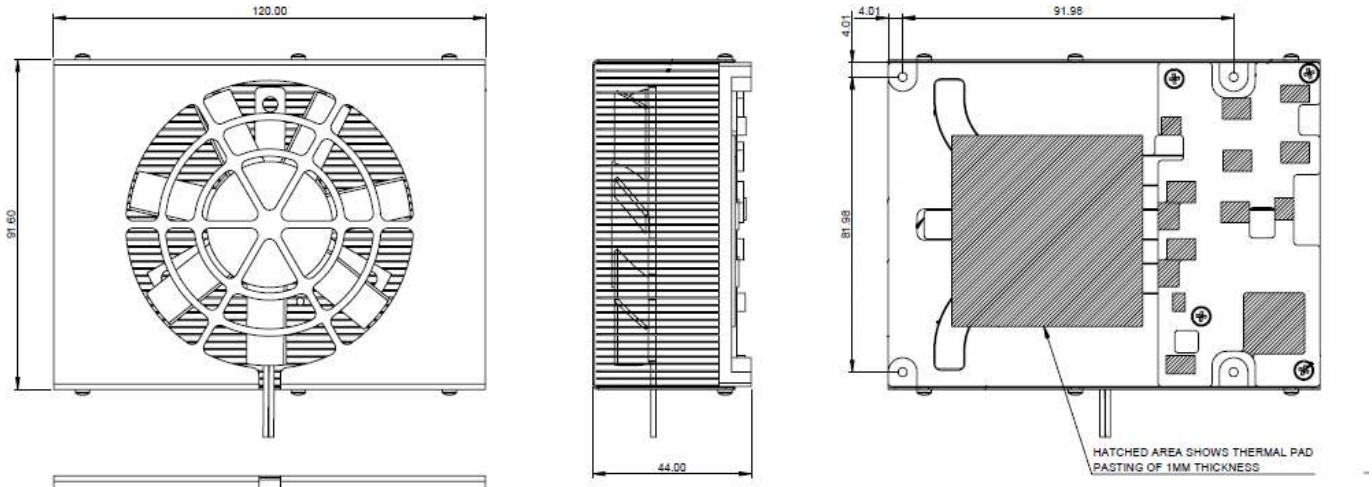
3.2.3. Electrostatic Discharge

iWave's Speedster7t FPGA SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4. Heat Sink

For any highly integrated SOM, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.



Fan Specifications	
Part No	T128015XU
Dimensions	80x80x15mm
Air Flow	48.14CFM 1.36m3/min
Static Pressure	4.02mmH2O
Rated Voltage	12V

TIM Specifications	
Material	Silicone Rubber (SIR)
Thermal Conductivity	6.2W/mk
Flame Rating	UL 94 V-0
Hardness	50 Shore OO
Working Temp	-50~+180 °C
RoHS	Yes

Figure 11 : Heat Sink

3.3. Mechanical Characteristics

The Speedster7t FPGA SOM PCB size is 120mm x 90mm x 2.50mm. SOM mechanical dimension is shown below.

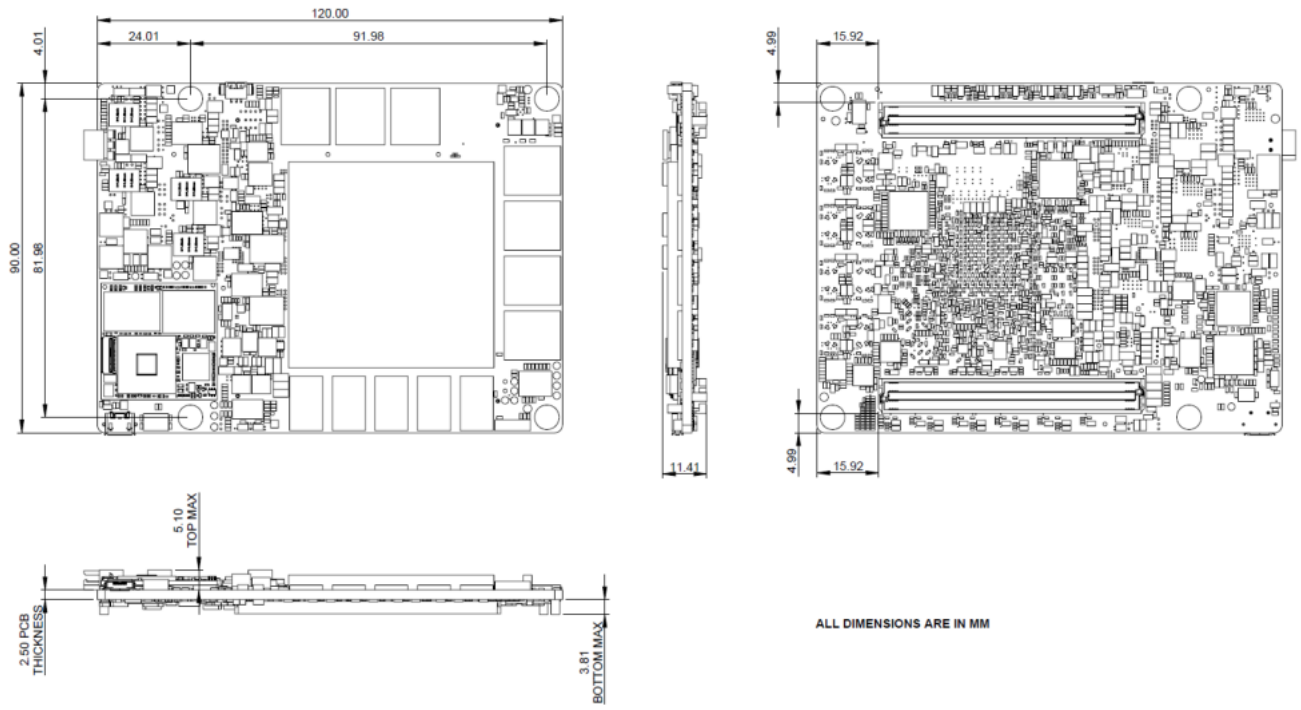


Figure 12 : SOM Mechanical dimensions

The Speedster7t FPGA SOM PCB thickness is 2.50mm±0.1mm, top side component with maximum height is inductor L5 (5.10mm) and bottom side component with maximum height is Board-to-Board connector 1 & 2 (3.81mm).

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Speedster7t FPGA SOM variations. If desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 25 : Orderable Product Part Numbers

Product Part Number	Description
iG-64M-7t1501-6G014G-4E08G-IAA	Speedster7t 1500 (-1) Speed FPGA with 14GB GDDR6, 8GB DDR4, Industrial grade SOM
iG-64M-7t1502-6G014G-4E08G-IAA	Speedster7t 1500 (-2) Speed FPGA with 14GB GDDR6, 8GB DDR4, Industrial grade SOM
iG-64M-7t1501-6G014G-4E08G-CAA	Speedster7t 1500 (-1) Speed FPGA with 14GB GDDR6, 8GB DDR4, Commercial grade SOM
iG-64M-7t1502-6G014G-4E08G-CAA	Speedster7t 1500 (-2) Speed FPGA with 14GB GDDR6, 8GB DDR4, Commercial grade SOM

5. APPENDIX

5.1. Speedster7t FPGA SOM Development Platform

iWave supports iW-RainboW-G64D-Speedster7t FPGA SOM development platform which is targeted for quick validation of Speedster7t FPGA based SOM. iWave's Speedster7t FPGA development board incorporates Speedster7t FPGA SOM and high-performance carrier board with complete BSP support.

Contact us for more details on Speedster7t FPGA SOM development platform.

Figure 13 : iW-RainboW-G64D-Speedster7t FPGA SOM Development Platform

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Since 1999, we have pioneered leadership in embedded systems technology, establishing ourselves as a strategic embedded technology partner for advanced solutions. Our comprehensive portfolio encompasses ARM and FPGA System on Modules, COTS FPGA solutions, and ODM solutions which include Telematics, Gateways & HMI Solutions.

Beyond our robust product ecosystem, we provide comprehensive ODM support with specialized custom design and manufacturing capabilities, enabling customers to accelerate and optimize their product development roadmaps. With a strategic focus on industrial, automotive, medical, and avionics markets, we deliver innovative technology solutions to global clients.

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