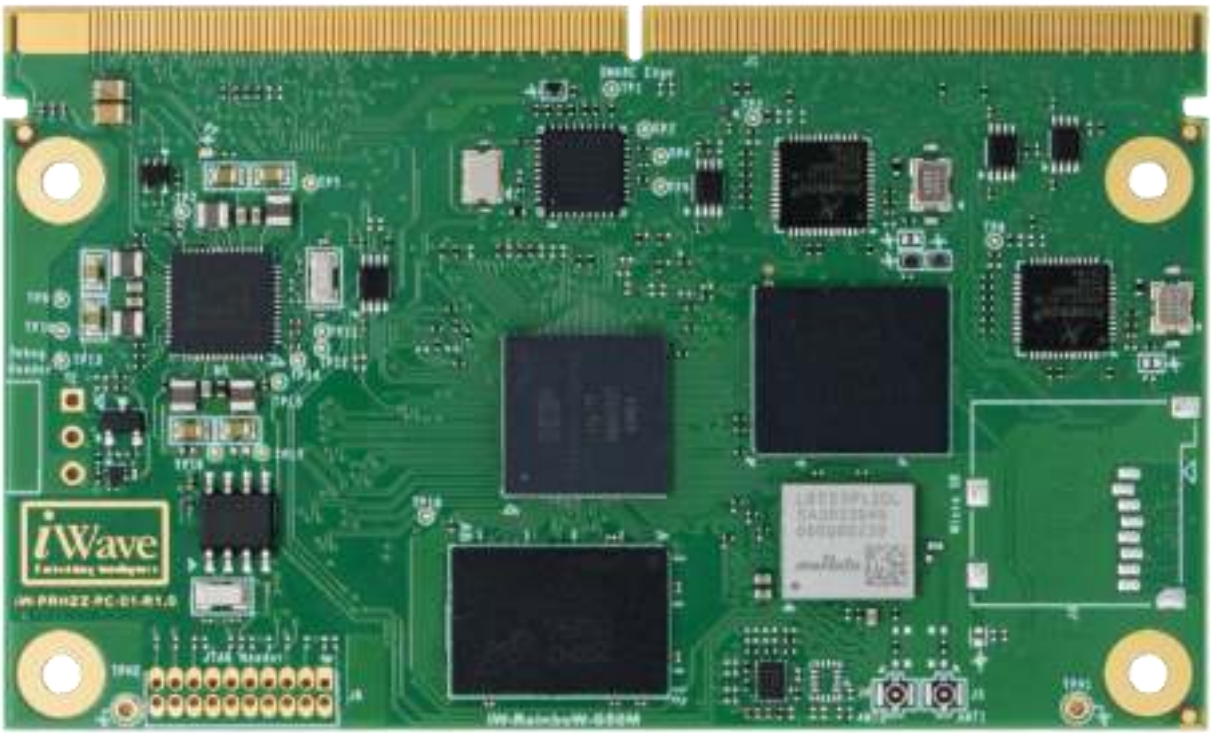
iW-RainboW-G50M

i.MX 93 or i.MX 91

SMARC System On Module Datasheet



Document Revision History

Document Number		iW-PRHZZ-UM-01-R1.0-REL1.0-Hardware
Revision	**Date**	**Description**
0.1	24th Nov 2023	Draft Release Version
0.2	20th June 2025	Updated format

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1. INTRODUCTION

1.1 Purpose

This datasheet provides comprehensive technical details for the **NXP's i.MX 93 or i.MX 91 Application processor based SMARC V2.1.1 SOM**, a robust and versatile solution designed and supported by iWave Global. It encompasses information on hardware specifications, software capabilities, and mechanical dimensions, enabling seamless integration into diverse embedded and industrial applications.

1.2 SMARC SOM Overview

The SMARC V2.1.1 ("Smart Mobility Architecture version 2.1.1") is a versatile small form factor Computer Module definition targeting application that require low power, low costs, and high performance.

The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies, GbE, GNSS module (optional) and dual channel LVDS/ MIPI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 93 or i.MX 91 SoC based SMARC System on Module is rich with i.MX 93 or i.MX 91 features along with on SOM LPDDR4/4X, eMMC, Wi-Fi/BT module, Dual Ethernet PHY, USB2.0 Hub and comes in compact 82mm x 50mm form factor. The Module PCB has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
EMS	Electronics manufacturing services
FLEXCAN	Flexible Control Area Network

Acronyms	Abbreviations
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface differential pair signals
OTG	On-The-Go
PCB	Printed Circuit Board
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
USB	Universal Serial Bus
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- IMX93IEC_Rev_x.pdf
- IMX91PEC_Revx
- i.MX93RM Rev_x.pdf
- SMARC Specification v2.1.1

1.6 Important Note

In this document, wherever i.MX 93 or i.MX 91 SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "F*unctionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.
- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

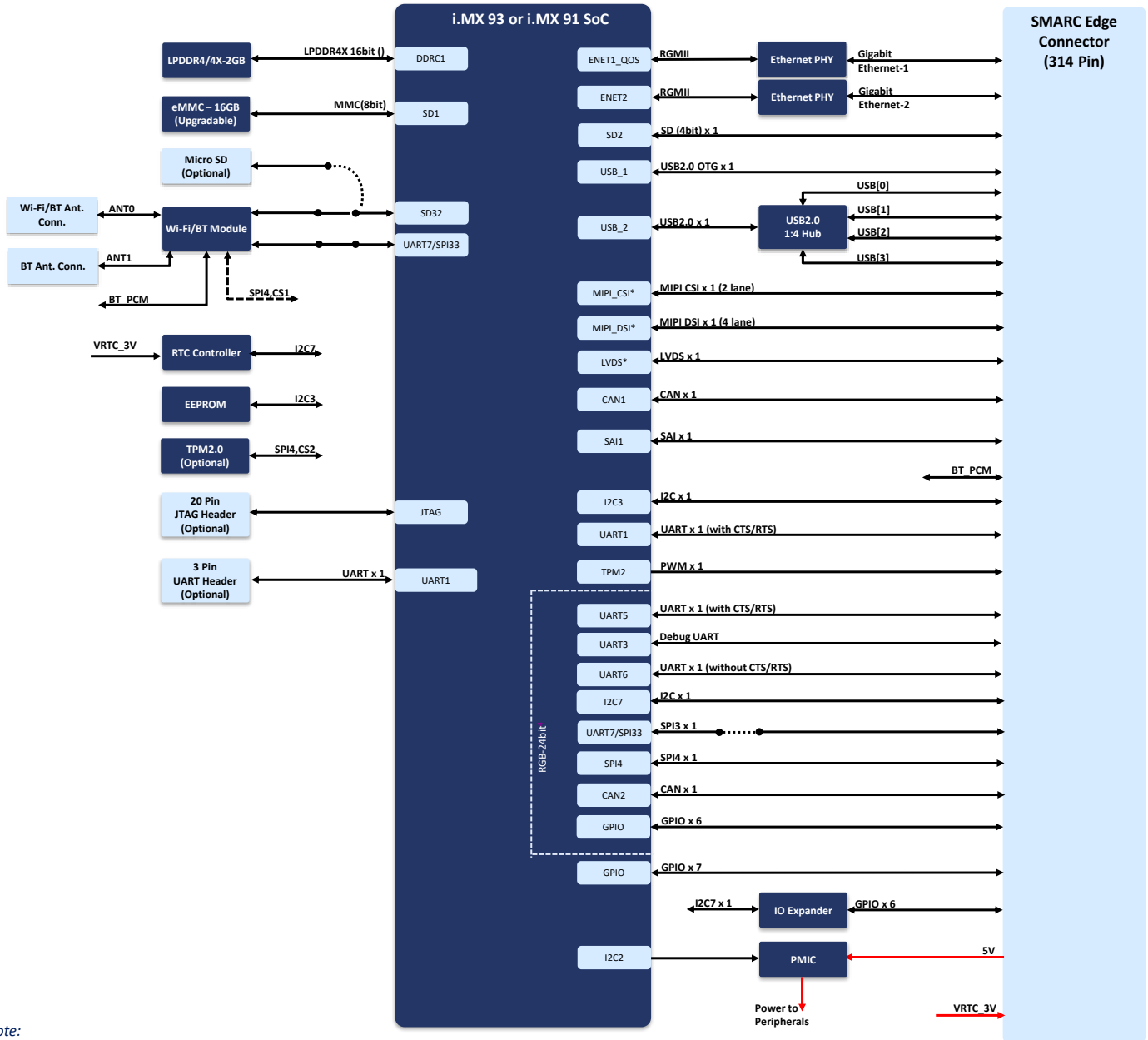
  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 93 or i.MX 91 SMARC SOM features and Hardware architecture with high level block diagram.

2.1 i.MX 93 or i.MX 91 SMARC SOM Block Diagram



Note:
1. By default, LPDDR4X is supported in i.MX 93. Also note, LPDDR4X is not supported in i.MX 91 SoC.
2. SD3 is default connected to Wi-Fi module and Optionally connected to microSD Connector.
3. In default configuration UART7 interface of i.MX 93 is connected to on SOM Bluetooth module and optionally connected to SMARC SPI1.
4. 24-bit RGB is optionally available.
** Not supported in i.MX 91 SoC*

Figure 1: i.MX 93 or i.MX 91 SMARC SOM Block Diagram

2.2 i.MX 93 or i.MX 91 SOM Features

i.MX 93 or i.MX 91 SMARC SOM supports the following features.

SoC

- i.MX 93 Processor[1]
  - i.MX 9352: 2x Cortex®-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9351: 1 x Cortex-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9332: 2x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9331: 1x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 91 Processor
  - i.MX 91: 1x Cortex®-A55, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0

Power

- PCA9451 PMIC

Memory

- LPDDR4/4X - 2GB[2,3]
- eMMC Flash - 16GB (Expandable)[2]
- EEPROM
- Micro SD Connector (Optional)[4]

Other On-SOM Features

- IEEE 802.11a/b/g/n/ac/ax+ Bluetooth 5.3+ IEEE802.15.4[4,5]
- Gigabit Ethernet PHY Transceiver x 2
- USB2.0 1:4 Hub
- RTC Controller
- TPM2.0 (Optional)
- UART Header (Optional)
- JTAG Header (Optional)

SMARC PCB Edge Interfaces

- Gigabit Ethernet x 2 Ports (through On-SOM Gigabit Ethernet PHY transceivers)
- SD (4bit) x 1 Port
- USB2.0 OTG x 1

- USB2.0 Host x 4 (through On-SOM USB Hub)
- SAI/I2S (Audio Interface) x 2
- SPI x 2 (1 is optional) [6]
- Data UART with flow control x 2
- Data UART without flow control x 1
- Debug UART x 1
- GPIOs x 15
- MIPI_DSI(4lane) x 1*
- MIPI_CSI(2lane) x 1*
- LVDS x 1*
- I2C x 2
- PWM x 1
- ADC x 4 (Optional through CAM0 pins)
- Tamper x 2 (Optional through RSVD pins)

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 82mm X 50mm (SMARC V2.1.1 Specification)

1. *There are four configurations of i.MX 93 Processor, hence this document is used to represent either of one based on SOM Part Number.*
2. *Memory Size will differ based on iWave's SOM Product Part Number.*
3. *i.MX 93 SMARC SOM supports LPDDR4X by default and i.MX 91 SoC supports LPDDR4.*
4. *SD3 is by default connected to Wi-Fi module and optionally connected to microSD Connector.*
5. *IEEE802.15.4 is supported optionally.*
6. *In default configuration UART7 interface of i.MX 93 is connected to on SOM Bluetooth module and optionally connected to SMARC SPI1.*

**** Not supported in i.MX 91 SoC.***

2.3 CPU

iW-RainboW-G50M i.MX 93 and i.MX 91 SMARC SOM can support different i.MX 93 or i.MX 91 SoCs from NXP.

2.3.1 i.MX 93 CPU

The i.MX 93 (11 x 11 mm) Family consists of four processors.

- i.MX 9352: 2x Cortex®-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9351: 1 x Cortex-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9332: 2x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9331: 1x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Memory interfaces supporting 16-bit LPDDR4 and LPDDR4X, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

Figure 2: i.MX 93 SoC Block Diagram

2.3.2 i.MX 91 CPU

The i.MX 91 (11 x 11 mm) Family consists of two processors.

- i.MX 91P1C: Industrial Grade
- i.MX 91P1D: Consumer Grade

The i.MX 91 includes powerful single Arm® Cortex®-A55 processor with speeds up to 1.4 GHz. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, drive gateway applications with low latency. Memory interfaces supporting 16-bit LPDDR4, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

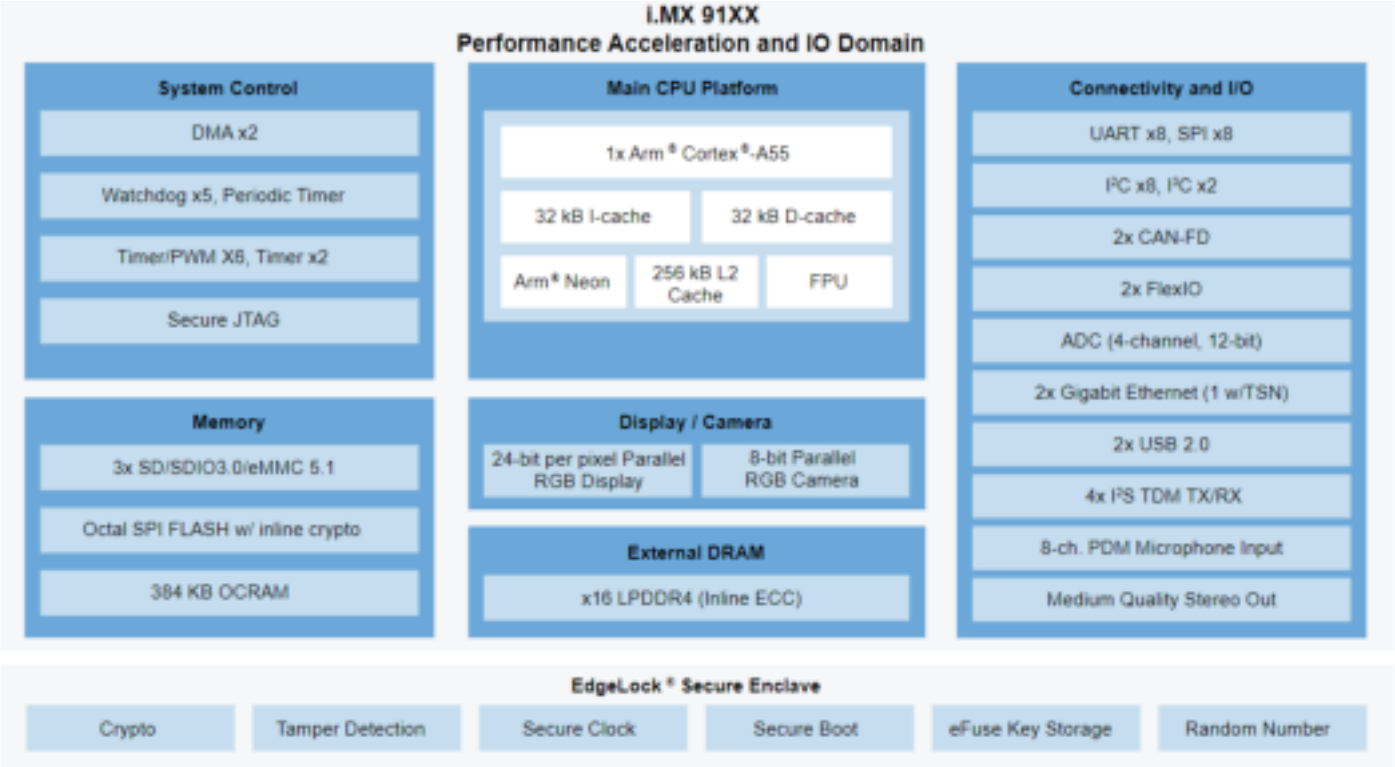


Figure 3: i.MX 91 SoC Block Diagram

Note: The i.MX 93 and i.MX 91 processor offers numerous advanced features, please refer the latest i.MX 93 or i.MX 91 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PCA9451 PMIC

The i.MX 93 or i.MX 91 SMARC SOM uses one PCA9451 PMIC (U9) for module power management. The PCA9451 features six high efficiency step-down regulators and three linear regulators. The PCA9451 is a single chip Power Management IC (PMIC) specifically designed to support i.MX 93x family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5V adapter non-portable applications. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9451 PMIC comes in 56-pin HVQFN package and is placed on the top side of the SOM.

2.5 Memory

2.5.1 LPDDR4X/LPDDR4

The i.MX 93 or i.MX 91 SMARC SOM supports 2GB LPDDR4X/LPDDR4 memory by using 16bit DDR_CH0 channel of the SoC. By default, LPDDR4X is supported in i.MX 93 SMARC SOM. The i.MX 91 SoC supports only LPDDR4. To customize the LPDDR4X/LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 93 or i.MX 91 SMARC SOM supports 16GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 93 or i.MX 91 SoC and operates at 1.8V (IO supply) and 3.3V (NAND core supply) Voltage levels. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 EEPROM

The i.MX 93 or i.MX 91 SMARC SOM supports s 32 Kbits of EEPROM. This EEPROM is connected to i.MX 93 SoC through I2C3 Interface and operates at 1.8V voltage level.

2.5.4 Micro SD Connector (Optional)

The i.MX 93 or i.MX 91 SMARC SOM optionally supports Micro SD connector which can be used to connect Micro SD card as optional Mass storage device. Micro SD card connector (J3) is connected to the uSDHC3 controller of the i.MX 93 or i.MX 91 SoC.

The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 93 or i.MX 91 SMARC SOM supports configurable I/O voltage levels for USDHC3 lines through GPIO port4 of the IO Expander. If the GPIO is set to low, then 3.3V IO level is selected for uSDHC3 lines. If GPIO is set to high, then 1.8V IO level is selected for uSDHC3 lines. Micro SD Connector is physically located on top side of the i.MX 93 or i.MX 91 SMARC SOM.

Figure 4: Micro SD Connector

2.6 Network & Communications features

2.6.1 Wi-Fi and Bluetooth Interface

The i.MX 93 or i.MX 91 SMARC SOM is integrated with Murata's "LBEE5PL2DL-921" based Wi-Fi + Bluetooth module. LBEE5PL2DL-921 module is complaint with IEEE 802.11a/b/g/n/ac/ax, SISO and Bluetooth specification v5. It supports standard SDIO 3.0 interface for WLAN, UART interfaces support for Bluetooth is Host Controller Interface (HCI) and SPI interface to optionally support IEEE 802.15.4. Connection to a host processor is through SDIO, High-Speed UART interfaces and SPI. The i.MX 93 SMARC SOM uses processor's UART7 interface for Bluetooth and SD3 interface for Wi-Fi in a default configuration. In the SMARC SOM, antenna pins of LBES5PL2EL-SMP Wi-Fi and Bluetooth is connected to J4 & J5 connectors.

Note: In default configuration, IEEE 802.15.4 is not supported and can be supported by changing the module from LBEE5PL2DL-921 to LBES5PL2EL-SMP and other hardware changes. Contact iWave Support Team for further information.

Figure 5: Wi-Fi & Bluetooth Antenna Connectors

Connector Part Number - : RECE-20449-001E-01 from Taoglas

Antenna Part Number - : 2042811100 from Molex

2.6.2 RTC Controller

The i.MX 93 and i.MX 91 SMARC SOM by supports external RTC Controller "PCF85263" On-SOM for Real time clock support. This external RTC Controller IC (U13) is connected to i.MX 93 SoC through I2C7 Interface and operates at 1.8V voltage level. In SOM power off condition, this device will take power SMARC PCB Edge (VDD_RTC) coin cell power input (Pin S147) and continues to update the current time. GPIO3_26 is connected to the interrupt pin of the RTC controller, which can be utilized for supporting wakeup and other features.

2.7 SMARC PCB Edge Connector

SMARC PCB edge connector (J1) has standard pinout as per SMARC Specification V2.1.1. The interfaces which are available at 314pin SMARC Edge connector are explained in the following sections.

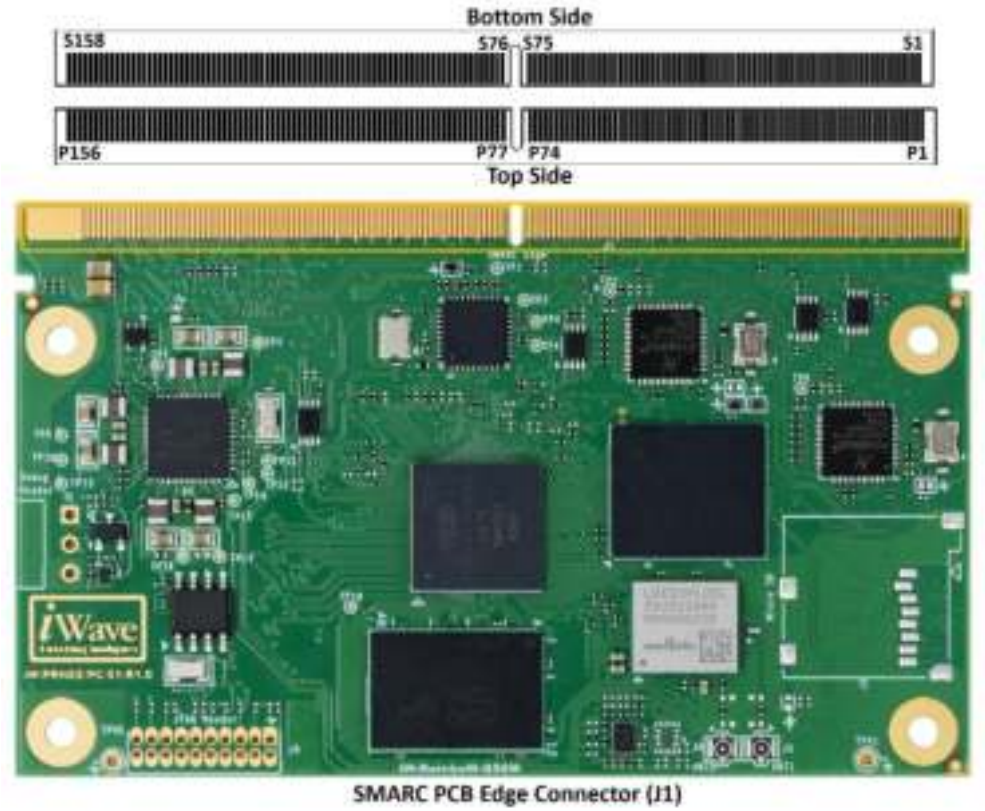


Figure 6: SMARC Edge Connector

Number of Pins - : 314

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 91782-3140M-001 from Aces

Table 3: SMARC Edge Connector Pinouts

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
NC	**P1**	**S1**	I2C7_SCL(GPIO_IO07)
GND	**P2**	**S2**	I2C7_SDA(GPIO_IO06)
MIPI_CSI1_CLK_P**	**P3**	**S3**	GND
MIPI_CSI1_CLK_N**	**P4**	**S4**	ADC_IN0*
GBE2_PPS_SDP	**P5**	**S5**	ADC_IN1*
GBE1_PPS_SDP	**P6**	**S6**	ADC_IN2*
MIPI_CSI1_D0_P**	**P7**	**S7**	ADC_IN3*
MIPI_CSI1_D0_N**	**P8**	**S8**	NC
GND	**P9**	**S9**	NC
MIPI_CSI1_D1_P**	**P10**	**S10**	GND
MIPI_CSI1_D1_N**	**P11**	**S11**	NC
GND	**P12**	**S12**	NC
NC	**P13**	**S13**	GND
NC	**P14**	**S14**	NC
GND	**P15**	**S15**	NC
NC	**P16**	**S16**	GND
NC	**P17**	**S17**	GBE1_MDI0+
GND	**P18**	**S18**	GBE1_MDI0-
GBE0_MDI3-	**P19**	**S19**	GBE1_LINK100#_3V3
GBE0_MDI3+	**P20**	**S20**	GBE1_MDI1+
GBE0_LINK100#_3V3	**P21**	**S21**	GBE1_MDI1-
GBE0_LINK1000#_3V3	**P22**	**S22**	GBE1_LINK1000#_3V3
GBE0_MDI2-	**P23**	**S23**	GBE1_MDI2+
GBE0_MDI2+	**P24**	**S24**	GBE1_MDI2-
GBE0_LINK_ACT#_3V3	**P25**	**S25**	GND
GBE0_MDI1-	**P26**	**S26**	GBE1_MDI3+
GBE0_MDI1+	**P27**	**S27**	GBE1_MDI3-
CTREF0	**P28**	**S28**	CTREF1
GBE0_MDI0-	**P29**	**S29**	NC
GBE0_MDI0+	**P30**	**S30**	NC
SPI4_SS1(GPIO_IO17)	**P31**	**S31**	GBE1_LINK_ACT#_3V3
GND	**P32**	**S32**	NC
NC	**P33**	**S33**	NC
SD2_CMD	**P34**	**S34**	GND
SD2_CD_B	**P35**	**S35**	USB_HUB4OUT_DP
SD2_CLK	**P36**	**S36**	USB_HUB4OUT_DM
SDIO_PWR_EN	**P37**	**S37**	VBUS_OTG2*
GND	**P38**	**S38**	SAI1_MCLK
SD2_DATA0	**P39**	**S39**	SAI1_TXFS(BOOT_MODE2)
SD2_DATA1	**P40**	**S40**	SAI1_TXD0(BOOT_MODE3)

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
SD2_DATA2	**P41**	**S41**	SAI1_RX_DATA0
SD2_DATA3	**P42**	**S42**	SAI1_TXCLK
SPI4_SSO(GPIO_IO18)	**P43**	**S43**	NC
SPI4_CLK	**P44**	**S44**	NC
SPI4_MISO(GPIO_IO19)	**P45**	**S45**	SMARC_MDIO_CLK
SPI4_MOSI(GPIO_IO20)	**P46**	**S46**	SMARC_MDIO_DATA
GND	**P47**	**S47**	GND
NC	**P48**	**S48**	I2C3_SCL(GPIO_IO29)
NC	**P49**	**S49**	I2C3_SDA(GPIO_IO28)
GND	**P50**	**S50**	BT_PCM_SYNC
NC	**P51**	**S51**	BT_PCM_DOUT
NC	**P52**	**S52**	BT_PCM_DIN
GND	**P53**	**S53**	BT_PCM_CLK
SPI3_CS0*	**P54**	**S54**	NC
SPI4_SS2*	**P55**	**S55**	NC
SPI3_CLK*	**P56**	**S56**	NC
SPI3_MISO*	**P57**	**S57**	NC
SPI3_MOSI*	**P58**	**S58**	NC
GND	**P59**	**S59**	NC
USB_OTG1_DP	**P60**	**S60**	NC
USB_OTG1_DM	**P61**	**S61**	GND
USB0_EN_OC#	**P62**	**S62**	NC
VBUS_OTG1	**P63**	**S63**	NC
USB0_OTG_ID	**P64**	**S64**	GND
USB_HUB1OUT_DP	**P65**	**S65**	NC
USB_HUB1OUT_DM	**P66**	**S66**	NC
USB_HUB1_OC	**P67**	**S67**	GND
GND	**P68**	**S68**	USB_HUB3OUT_DP
USB_HUB2OUT_DP	**P69**	**S69**	USB_HUB3OUT_DM
USB_HUB2OUT_DM	**P70**	**S70**	GND
USB_HUB2_OC	**P71**	**S71**	NC
TAMPER0*	**P72**	**S72**	NC
TAMPER1*	**P73**	**S73**	GND
USB_HUB3_OC	**P74**	**S74**	NC
		S75	NC
Key			
NC	**P75**	**S76**	NC
USB_HUB4_OC	**P76**	**S77**	NC
NC	**P77**	**S78**	NC
NC	**P78**	**S79**	NC
GND	**P79**	**S80**	GND

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
NC	**P80**	**S81**	NC
NC	**P81**	**S82**	NC
GND	**P82**	**S83**	GND
NC	**P83**	**S84**	NC
NC	**P84**	**S85**	NC
GND	**P85**	**S86**	GND
NC	**P86**	**S87**	NC
NC	**P87**	**S88**	NC
GND	**P88**	**S89**	GND
NC	**P89**	**S90**	NC
NC	**P90**	**S91**	NC
GND	**P91**	**S92**	GND
NC	**P92**	**S93**	NC
NC	**P93**	**S94**	NC
GND	**P94**	**S95**	NC
NC	**P95**	**S96**	NC
NC	**P96**	**S97**	NC
GND	**P97**	**S98**	NC
NC	**P98**	**S99**	NC
NC	**P99**	**S100**	NC
GND	**P100**	**S101**	GND
NC	**P101**	**S102**	NC
NC	**P102**	**S103**	NC
GND	**P103**	**S104**	USB3_OTG_ID*
NC	**P104**	**S105**	NC
NC	**P105**	**S106**	NC
NC	**P106**	**S107**	LCD1_BKLT_EN(IO1_02)
NC	**P107**	**S108**	MIPI_DSI1_CLK_P**
SMARC_GPIO0_GPIO2_IO12(GPIO_IO09)	**P108**	**S109**	MIPI_DSI1_CLK_N**
SMARC_GPIO1_GPIO2_IO13(GPIO_IO13)	**P109**	**S110**	GND
SMARC_GPIO2(IO3_00)	**P110**	**S111**	MIPI_DSI1_D0_P**
SMARC_GPIO3(IO3_05)	**P111**	**S112**	MIPI_DSI1_D0_N**
SMARC_GPIO4_GPIO2_IO22(GPIO_IO22)	**P112**	**S113**	NC
SMARC_GPIO5_GPIO2_IO23(GPIO_IO23)	**P113**	**S114**	MIPI_DSI1_D1_P**
SMARC_GPIO6_GPIO2_IO24(GPIO_IO24)	**P114**	**S115**	MIPI_DSI1_D1_N**

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
SMARC_GPIO7_GPIO2_IO26(GPIO_IO26)	**P115**	**S116**	LCD1_VDD_EN(IO1_01)
SMARC_GPIO8(IO3_01)	**P116**	**S117**	MIPI_DSI1_D2_P**
SMARC_GPIO9_GPIO1_IO1(I2C1_SDA)	**P117**	**S118**	MIPI_DSI1_D2_N**
SMARC_GPIO10_GPIO3_IO30(JTAG_TCK)	**P118**	**S119**	GND
SMARC_GPIO11_GPIO3_IO31(JTAG_TDO)	**P119**	**S120**	MIPI_DSI1_D3_P**
GND	**P120**	**S121**	MIPI_DSI1_D3_N**
PMIC_I2C2_SCL*	**P121**	**S122**	NC
PMIC_I2C2_SDA*	**P122**	**S123**	SMARC_GPIO13(JTAG_TDI)
BOOT_SEL0#	**P123**	**S124**	GND
BOOT_SEL1#	**P124**	**S125**	LVDS0_D0_P**
BOOT_SEL2#	**P125**	**S126**	LVDS0_D0_N**
RESETOUT#_GPIO3_IO27(CCM_CLKO2)	**P126**	**S127**	LCD0_BKLT_EN(IO1_00)
PMIC_RST_B	**P127**	**S128**	LVDS0_D1_P**
CPU_ON_OFF	**P128**	**S129**	LVDS0_D1_N**
UART1_TXD(BOOT_MODE0)	**P129**	**S130**	GND
UART1_RXD	**P130**	**S131**	LVDS0_D2_P**
UART1_RTS(UART2_TXD)	**P131**	**S132**	LVDS0_D2_N**
UART1_CTS	**P132**	**S133**	LCD0_VDD_EN_GPIO4_IO28(CCM_CLKO3)
GND	**P133**	**S134**	LVDS0_CLK_P**
UART6_TXD(GPIO_IO04)	**P134**	**S135**	LVDS0_CLK_N**
UART6_RXD(GPIO_IO05)	**P135**	**S136**	GND
UART5_TXD(GPIO_IO00)	**P136**	**S137**	LVDS0_D3_P**
UART5_RXD(GPIO_IO01)	**P137**	**S138**	LVDS0_D3_N**
UART5_RTS(GPIO_IO03)	**P138**	**S139**	I2C7_SCL(GPIO_IO07)
UART5_CTS(GPIO_IO02)	**P139**	**S140**	I2C7_SDA(GPIO_IO06)
UART3_TXD(GPIO_IO14)	**P140**	**S141**	TPM2(I2C1_SCL)
UART3_RXD(GPIO_IO15)	**P141**	**S142**	SMARC_GPIO12(JTAG_TMS)
GND	**P142**	**S143**	GND
CAN1_TX(PDM_CLK)	**P143**	**S144**	NC
CAN1_RX(PDM_BIT0)	**P144**	**S145**	GPIO_WDT_OUT
CAN2_TX(GPIO_IO25)	**P145**	**S146**	NC
CAN2_RX(GPIO_IO27)	**P146**	**S147**	VRTC_3V0
VDD_IN	**P147**	**S148**	NC
VDD_IN	**P148**	**S149**	NC
VDD_IN	**P149**	**S150**	VIN_PWR_BAD#
VDD_IN	**P150**	**S151**	NC

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
VDD_IN	**P151**	**S152**	NC
VDD_IN	**P152**	**S153**	CARRIER_STBY#
VDD_IN	**P153**	**S154**	CARRIER_PWR_ON
VDD_IN	**P154**	**S155**	FORCE_RECOV#
VDD_IN	**P155**	**S156**	NC
VDD_IN	**P156**	**S157**	TEST#
		S158	GND

**** Not supported in i.MX 91 SoC.***

2.7.1 RGMII Interface

The i.MX 93 or i.MX 91 SMARC SOM supports two Gigabit Ethernet using the two on SOM Ethernet PHY "AR8031" from Atheros, Qualcomm. ENET0 and ENET1 of i.MX 93 or i.MX 91 SoC are connected to GBE0 and GBE1 ports of SMARC edge connector respectively. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system.

For more details on GBE0 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P6	GBE0_SDP	GBE1_PPS_SDP	NA	IO, 3.3V CMOS	NC. Note: Optionally connected to GBE1_PPS_SDP.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#_3V3	NA	O, 3.3V CMOS 10K PU	100Mbps Ethernet link status LED. *Note: Connect to Cathode of LED.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P22	GBE0_LINK1000#	GBE0_LINK1000#_3V3	NA	O, 3.3V CMOS 10K PU	Gigabit Ethernet link status LED. *Note: Connect to Cathode of LED.*
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#_3V3	NA	O, 3.3V CMOS 10K PU	Gigabit Ethernet activity status *Note: Connect to Cathode of LED.*
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of the magnetics.
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.

For more details on GBE1 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P5	GBE1_SDP	GBE2_PPS_SDP	NA	IO, 3.3V CMOS	NC. *Note: Optionally connected to GBE2_PPS_SDP.*
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	GBE1_LINK100#_3V3	NA	O, 3.3V CMOS 10K PU	100Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	GBE1_LINK1000#_3V3	NA	O, 3.3V CMOS 10K PU	1000Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair2 negative.
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	GBE1_CTREF	VPHY1_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#_3V3	NA	O, 3.3V CMOS 10K PU	Ethernet Activity status LED.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Connect to Cathode of LED.

2.7.2 MDIO Interface (Optional)

The i.MX 93 or i.MX 91 SMARC SOM optionally supports MDIO support from the ENET MDIO of the i.MX 93 or i.MX 91 processor on the SMARC Edge connector.

For more details on MDIO pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S45	MDIO_CLK	SMARC_MDIO_CLK	ENET2_MDC/ Y7	O, 1.8V CMOS	NC. *Note: Optionally connected to ENET2_MDC*
S46	MDIO_DAT	SMARC_MDIO_DATA	ENET2_MDIO /AA6	IO, 1.8V CMOS	NC. *Note: Optionally connected to ENET2_MDIO*

2.7.3 SD Interface

The i.MX 93 or i.MX 91 SMARC SOM supports 4bit SD interface over SMARC PCB Edge connector which can be used to connect SD card as Mass storage or boot device. uSDHC2 controller of the i.MX 93 or i.MX 91 SoC is used to support SMARC SD interface. uSDHC2 operates both in 3.3V and 1.8V IO level and supports maximum card bus frequency of 208 MHz. The i.MX 93 or i.MX 91 SMARC SOM supports configurable I/O voltage levels for USDHC2 lines through SD2_VSELECT.If SD2_VSELECT is set to low, then 3.3V IO level is selected for uSDHC2 lines. If SD2_VSELECT is set to high, then 1.8V IO level is selected for uSDHC2 lines. Control GPIO like Card detect signal also operate at both 1.8V and 3.3V IO level.

For more details on SD pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P34	SDIO_CMD	SD2_CMD	SD2_CMD/ Y19	IO, 1.8/3.3V CMOS	SD command.
P35	SDIO_CD#	SD2_CD_B	SD2_CD_B/ Y17	I, 1.8V/3.3V CMOS 10K PU	SD Card Detect.
P36	SDIO_CK	SD2_CLK	SD2_CLK/ AA19	O, 1.8/3.3V	SD Clock

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				CMOS, 33E Series	
P37	SDIO_PWR_EN	GPIO3_07(SD2_RESET_B)	SD2_RESET_B / AA17	O, 3.3V CMOS 10K PU	SD Power enable.
P39	SDIO_D0	SD2_DATA0	SD2_DATA0/ Y18	IO, 1.8/3.3V CMOS	SD data 0
P40	SDIO_D1	SD2_DATA1	SD2_DATA1/ AA18	IO, 1.8/3.3V CMOS	SD data 1.
P41	SDIO_D2	SD2_DATA2	SD2_DATA2/ Y20	IO, 1.8/3.3V CMOS	SD data 2.
P42	SDIO_D3	SD2_DATA3	SD2_DATA3/ AA20	IO, 1.8/3.3V CMOS	SD data 3.

2.7.4 USB 2.0 OTG Interface

The i.MX 93 or i.MX 91 SMARC SOM can support USB2.0 OTG through the USB0 port of SMARC PCB Edge connector. The USB2.0 lines of the USB OTG1 controller (with integrated PHY) supports USB2.0 High-Speed, Full-Speed and Low-Speed transfer.

To support 2nd USB2.0 OTG interface, i.MX 93 or i.MX 91 SoC's USB OTG2 controller is used. The USB2.0 lines of the USB OTG2 controller (with integrated PHY) is optionally connected to USB3 port of SMARC PCB Edge connector.

For more details on USB 2.0 OTG pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P60	USB0+	USB_OTG1_DP	USB1_D_P/B14	IO, USB	USB2.0 Port0 Data Positive.
P61	USB0-	USB_OTG1_DM	USB1_D_N/A14	IO, USB	USB2.0 Port0 Data Negative.
P62	USB0_EN_OC#	USB0_EN_OC	-	IO, 3.3V CMOS 10K PU	USB Port0 Power Enable/ Over Current Indicator.
P63	USB0_VBUS_DET	VBUS_OTG1	USB1_VBUS/ F12	5V, Power	USB host power detection, when this port is used as a device.
P64	USB0_OTG_ID	USB0_OTG_ID	USB1_ID/C11	I, 3.3V CMOS	USB0 OTG ID. *Note: 1.8V to 3.3V level translator is used to match SMARC specification.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S68	USB3+	USB_HUB3OUT_DP	USB2_D_P/B15	IO, USB	USB2.0 Port3 Data Positive. *Note: This pin is optionally connected from i.MX 93 or i.MX 91 SoC's USB2 Data Positive for 2nd USB 2.0 OTG through resistor and default not populated.* *Note: SoC's USB2 Data Positive is by default connected to the USB HUB through resistor and default populated.*
S69	USB3-	USB_HUB3OUT_DM	USB2_D_N/A15	IO, USB	USB2.0 Port3 Data Negative. *Note: This pin is optionally connected from i.MX 93 or i.MX 91 SoC's USB2 Data Negative for 2nd USB 2.0 OTG through resistor and default not populated.* *Note: SoC's USB2 Data Negative is by default connected to the USB HUB through resistor and default populated.*
S37	USB3_VBUS_DET	VBUS_OTG2	USB2_VBUS/E14	5V, Power	Default NC. *Note: This pin is optionally connected to i.MX 93 or i.MX 91 SoC's USB2_VBUS for VBUS detection through resistor and default not populated.*
S104	USB3_OTG_ID	USB3_OTG_ID	USB2_ID/E12	I, 3.3V CMOS	Default NC. *Note: This pin is optionally connected to i.MX 93 or i.MX 91 SoC's USB2_ID pin through resistor and default not populated.*

2.7.5 USB 2.0 Host Interface

The i.MX 93 or i.MX 91 SMARC SOM supports four USB2.0 Host interface on SMARC PCB Edge connector. To support four USB2.0 Host interfaces, SOM includes a four-port USB hub "USB2514" from Microchip. This Hub is interfaced with

USB OTG2 controller of i.MX 93 or i.MX 91 SoC (with integrated PHY) which supports USB2.0 High-Speed, Full-Speed and Low-Speed transfer. This Hub output is directly connected to USB1, USB2, USB3 & USB4 ports of SMARC PCB Edge connector.

For more details on USB 2.0 Host pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P65	USB1+	USB_HUB1OUT_DP	NA	IO, USB	USB 2.0 Port1 Data Positive. *Note: This pin is connected from 4port USB Hub Out1.*
P66	USB1-	USB_HUB1OUT_DM	NA	IO, USB	USB 2.0 Port1 Data Negative. *Note: This pin is connected from 4port USB Hub Out1.*
P67	USB1_EN_OC#	USB_HUB1_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port1 Over Current Indicator. *Note: This pin is connected to USB Hub OCS1 pin.*
P69	USB2+	USB_HUB2OUT_DP	NA	IO, USB	USB 2.0 Port2 Data Positive. *Note: This pin is connected from 4port USB Hub Out2.*
P70	USB2-	USB_HUB2OUT_DM	NA	IO, USB	USB 2.0 Port2 Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
P71	USB2_EN_OC#	USB_HUB2_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port2 Over Current Indicator. *Note: This pin is connected to USB Hub OCS2 pin.*
S68	USB3+	USB_HUB3OUT_DP	NA	IO, USB	USB 2.0 Port3 Data Positive. *Note: This pin is connected from 4port USB Hub Out3.*
S69	USB3-	USB_HUB3OUT_DM	NA	IO, USB	USB 2.0 Port3 Data Negative. *Note: This pin is connected from 4port USB Hub Out3.*
P74	USB3_EN_OC#	USB_HUB3_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port3 Over Current Indicator. *Note: This pin is connected to USB Hub OCS3 pin.*
S35	USB4+	USB_HUB4OUT_DP	NA	IO, USB	USB 2.0 Port4 Data Positive. *Note: This pin is connected from 4port USB Hub Out4.*
S36	USB4-	USB_HUB4OUT_DM	NA	IO, USB	USB 2.0 Port4 Data Negative.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: This pin is connected from 4port USB Hub Ou4.
P76	USB4_EN_OC#	USB_HUB4_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port4 Over Current Indicator. *Note: This pin is connected to USB Hub OCS4 pin.*

2.7.6 MIPI CSI Interface (Not supported in i.MX 91 SoC)

The i.MX 93 supports one 2-lane MIPI CSI-2 camera input complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2. It supports up to 2 Rx data lanes (plus 1 Rx clock lane) and 80 Mbps -1.5 Gbps per lane data rate in high-speed operation. It also supports 10 Mbps data rate in low power operation.

For more details on MIPI CSI SMARC pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	CSI1_TX+ / I2C_CAM1_CK	I2C7_SCL(GPIO_IO07)	GPIO_IO07/ L21	O, 1.8V CMOS/ 4.7K PU	MIPI CSI I2C Clock. *Note: This I2C7_SCL line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S139 (I2C_LCD_CK).*
S2	CSI1_TX- / I2C_CAM1_DAT	I2C7_SDA(GPIO_IO06)	GPIO_IO06/ AD18	IO, 1.8V CMOS/ 4.7K PU	MIPI CSI I2C Data. *Note: This I2C7_SDA line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S140 (I2C_LCD_DAT).*
P3	CSI1_CK+	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ E10	I, MIPI	MIPI CSI differential clock positive.
P4	CSI1_CK-	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ D10	I, MIPI	MIPI CSI differential clock negative.
P7	CSI1_RX0+	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P/ B11	I, MIPI	MIPI CSI differential data lane 0 positive.
P8	CSI1_RX0-	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N/ A11	I, MIPI	MIPI CSI differential data lane 0 negative.
P10	CSI1_RX1+	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P/ B10	I, MIPI	MIPI CSI differential data lane 1 positive.
P11	CSI1_RX1-	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N/ A10	I, MIPI	MIPI CSI differential data lane 1 negative.

2.7.7 MIPI DSI Display Interface (Not supported in i.MX 91 SoC)

The i.MX 93 SMARC SOM supports one 4-lane MIPI DSI display with data supplied by the LCDIF Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2. Supports 80 Mbps—1.5 Gbps data rate per lane in high-speed operation.

For more details on DSI pinouts on SMARC Edge Connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S107	LCD1_BKLT_EN	LCD1_BKLT_EN(IO1_02)	-	O, 1.8V CMOS	LCD Backlight Enable. Output from on SOM IO expander.
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P/ E6	O, MIPI	MIPI differential Clock positive.
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N/ D6	O, MIPI	MIPI differential Clock negative.
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P/ B6	O, MIPI	MIPI differential data lane 0 positive.
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N/ A6	O, MIPI	MIPI differential data Lane 0 negative.
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P/ B7	O, MIPI	MIPI differential data lane 1 positive.
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N A7	O, MIPI	MIPI differential data lane 1 negative.
S116	LCD1_VDD_EN	LCD1_VDD_EN(IO1_01)	-	O, 1.8V CMOS	LCD Power Enable. Output from on SOM IO expander.
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P/ D8	O, MIPI	MIPI differential data lane 2 positive.
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N/ A8	O, MIPI	MIPI differential data lane 2 negative.
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P/ B9	O, MIPI	MIPI differential data lane 3 positive.
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N/ A9	O, MIPI	MIPI differential data lane 3 negative.

2.7.8 LVDS Display Interface (Not supported in i.MX 91 SoC)

The i.MX 93 SoC has LVDS Display Bridge which provides connectivity to relevant devices-Displays with LVDS receivers, arranging the data as required by the external display receiver and by LVDS display standards.

For more details on LVDS0 pinouts on Display Controller0 of SMARC PCB Edge Connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_D0_P	LVDS_D0_P/B5	O, LVDS	LVDS differential data lane 0 positive.
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_D0_N	LVDS_D0_N/A5	O, LVDS	LVDS differential data Lane 0 negative.
S127	LCD0_BKLT_EN	LCD0_BKLT_EN(IO1_00)	-	O, 1.8V CMOS	LCD0 Backlight Enable. Output from on SOM IO expander.
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_D1_P	LVDS_D1_P/B4	O, LVDS	LVDS differential data lane 1 positive.
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_D1_N	LVDS_D1_N/A4	O, LVDS	LVDS differential data Lane 1 negative.
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_D2_P	LVDS_D2_PP/B2	O, LVDS	LVDS differential data lane 2 positive.
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_D2_N	LVDS_D2_N/A2	O, LVDS	LVDS differential data Lane 2 negative.
S133	LCD0_VDD_EN	LCD0_VDD_EN_GPIO4_IO28(CCM_CLKO3)	CCM_CLKO3/ U4	O, 1.8V CMOS	LCD0 Power Enable.
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CLK_P	LVDS_CLK_P/B3	O, LVDS	LVDS differential Clock positive.
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CLK_N	LVDS_CLK_N/A3	O, LVDS	LVDS differential Clock negative.
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_D3_P	LVDS_D3_P/C1	O, LVDS	LVDS differential data lane 3 positive.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_D3_N	LVDS_D3_N/B1	O, LVDS	LVDS differential data Lane 3 negative.
S139	I2C_LCD_CK	I2C7_SCL(GPIO_IO07)	GPIO_IO07/L21	O, 1.8V CMOS/ 4.7K PU	I2C CLK for Display and Touch. *Note: This I2C7_SCL line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S139 (I2C_LCD_CK).*
S140	I2C_LCD_DAT	I2C7_SDA(GPIO_IO06)	GPIO_IO06/L20	IO, 1.8V CMOS/ 4.7K PU	I2C DATA for Display and Touch. *Note: This I2C7_SDA line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S140 (I2C_LCD_DAT).*
S141	LCD0_BKLT_PWM	TPM2(I2C1_SCL)	I2C1_SCL/C20	O, 1.8V CMOS	LCD Back Light Brightness control PWM

2.7.9 Audio Interface

The i.MX 93 or i.MX 91 SMARC SOM supports I2S0 and I2S2 channels of SMARC Edge connector from SoC's SAI1 channel and PCM from on SOM BT module. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97, TDM and other audio codec/DSP interfaces. The SAI general feature includes Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits.

In i.MX 93 or i.MX 91 SMARC SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on SMARC Edge I2S pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S38	AUDIO_MCK	SAI1_MCLK	UART2_RXD / F20	O, 1.8V CMOS	NC. *Master Clock for Audio codec is optionally available. By default, it is connected to SER0_CTS#.*
S39	I2S0_LRCK	SAI1_TXFS(BOOT_ MODE2)	SAI1_TXFS/ G21	O, 1.8V CMOS	Serial Audio Interface Channel0 Frame Sync /Left Right Clock.
S40	I2S0_SDOUT	SAI1_TXD0(BOOT_ MODE3)	SAI1_TXD0/ H21	O, 1.8V CMOS	Serial Audio Interface Channel0 Data Output
S41	I2S0_SDIN	SAI1_RX_DATA0	SAI1_RXD0/ H20	I, 1.8V CMOS	Serial Audio Interface Channel0 Data Input
S42	I2S0_CK	SAI1_TXCLK	SAI1_TXC/ G20	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel0 Clock.
S50	HDA_SYNC / I2S2_LRCK	BT_PCM_SYNC	-	O, 1.8V CMOS	Serial Audio Interface Channel2 Left Right Clock.
S51	HDA_SDO / I2S2_SDOUT	BT_PCM_DOUT	-	O, 1.8V CMOS	Serial Audio Interface Channel2 Data Output.
S52	HDA_SDI / I2S2_SDIN	BT_PCM_DIN	-	I, 1.8V CMOS	Serial Audio Interface Channel2 Data Input.
S53	HDA_CK / I2S2_CK	BT_PCM_CLK	-	O, 1.8V CMOS	Serial Audio Interface Channel2 Clock.

2.7.10 SPI Interface

The i.MX 93 or i.MX 91 SoC supports Low Power Serial Peripheral Interface (LPSPI) module which provides an efficient interface to a SPI bus, either as a master or slave. The i.MX 93 or i.MX 91 SoC's SPI4 supports SPI0 channel and SPI3 optionally supports SPI1 channel of the SMARC Edge connector.

For more details on SPI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P31	SPI0_CS1#	SPI4_SS1(GPIO_IO17)	GPIO_IO17/R20	O, 1.8V CMOS	SPI4 Chip Select 1 *Optionally connected to on SOM IEEE802.15.4 chip select.*
P43	SPI0_CS0#	SPI4_SSO(GPIO_IO18)	GPIO_IO18/ R18	O, 1.8V CMOS	SPI4 Chip Select 0

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P44	SPI0_CK	SPI4_CLK	GPIO_IO21/ T21	O, 1.8V CMOS/ 33E Series	SPI4 Clock. *Optionally connected to on SOM IEEE802.15.4 & TPM2.0.*
P45	SPI0_DIN	SPI4_MISO(GPIO_IO19)	GPIO_IO19/ R17	I, 1.8V CMOS	SPI4 Master IN Slave Out. *Optionally connected to on SOM IEEE802.15.4 & TPM2.0.*
P46	SPI0_DO	SPI4_MOSI(GPIO_IO20)	GPIO_IO20/ T20	O, 1.8V CMOS	SPI4 Master Out Slave In. *Optionally connected to on SOM IEEE802.15.4 & TPM2.0.*
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	SPI3_CS0	GPIO_IO08 / M20	O, 1.8V CMOS	NC. *Note: Optionally connect to SPI1_CS0#. By default, connected to on SOM Bluetooth module.*
P56	SPI1_CK / ESPI_CK / QSPI_CK	SPI3_CLK	GPIO_IO11 / N18	O, 1.8V CMOS/ 33E Series	NC. *Note: Optionally connect to SPI1_CK. By default, connected to on SOM Bluetooth module.*
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	SPI3_MISO	GPIO_IO09 / M21	I, 1.8V CMOS	NC. *Note: Optionally connect to SPI1_DIN. By default, connected to on SOM Bluetooth module.*
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	SPI3_MOSI	GPIO_IO10 / N17	O, 1.8V CMOS	NC. *Note: Optionally connect to SPI1_DO. By default, connected to on SOM Bluetooth module.*
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	SPI4_SS2	GPIO_IO16/R21	IO, 1.8V CMOS	NC. Optionally connected to P55 and TPM2.0 chip select.

2.7.11 Data UART

SMARC V2.1.1 supports four UART channels where two channels SER0 & SER2 are with CTS and RTS and two channels SER1 & SER3 are without. The i.MX 93 or i.MX 91 SoC's UART1, UART6 and UART5 are connected SER0, SER1 and SER2

channels of SMARC Edge connector respectively. SER0, SER1 & SER2 can be used for any data communication. UART3 of the SoC is connected to SER3 channel of SMARC Edge connector and used as Debug UART.

For more details on UART pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P129	SER0_TX	UART1_TXD(BOOT_MODE0)	UART1_TXD/ E21	O, 1.8V CMOS	UART1 Transmitter. *Also connected to BOOT_SEL0# (P123). Optionally connected to on SOM Debug Header.*
P130	SER0_RX	UART1_RXD	UART1_RXD/ E20	I, 1.8V CMOS	UART1 Receiver. *Optionally connected to on SOM Debug Header.*
P131	SER0_RTS#	UART1_RTS(UART2_TXD)	UART2_TXD/ F21	O, 1.8V CMOS	UART1 Request to Send.
P132	SER0_CTS#	UART1_CTS	UART2_RXD/ F20	I, 1.8V CMOS	UART1 Clear to Send.
P134	SER1_TX	UART6_TXD(GPIO_IO04)	GPIO_IO04/ L17	O, 1.8V CMOS	UART6 Transmitter.
P135	SER1_RX	UART6_RXD(GPIO_IO05)	GPIO_IO05/ L18	I, 1.8V CMOS	UART6 Receiver.
P136	SER2_TX	UART5_TXD(GPIO_IO00)	GPIO_IO00/ J21	O, 1.8V CMOS	UART5 Transmitter.
P137	SER2_RX	UART5_RXD(GPIO_IO01)	GPIO_IO01/ J20	I, 1.8V CMOS	UART5 Receiver.
P138	SER2_RTS#	UART5_RTS(GPIO_IO03)	GPIO_IO03/ K21	O, 1.8V CMOS	UART5 Request to Send.
P139	SER2_CTS#	UART5_CTS(GPIO_IO02)	GPIO_IO02/ K20	I, 1.8V CMOS	UART5 Clear to Send.
P140	SER3_TX	UART3_TXD(GPIO_IO14)	GPIO_IO14/ P20	O, 1.8V CMOS	Debug UART Transmitter.
P141	SER3_RX	UART3_RXD(GPIO_IO15)	GPIO_IO15/ P21	I, 1.8V CMOS	Debug UART Receiver.

2.7.12 CAN Interface

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according ISO 11898-1:2015 standard and CAN 2.0 B protocol specifications. The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads. The i.MX 93 or i.MX 91 SoC Supports two CAN interface and are connected to SMARC Edge Connector.

For more details of CAN pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P143	CAN0_TX	CAN1_TX(PDM_CLK)	PDM_CLK/G17	O, 1.8V CMOS	CAN 1 Transmitter.
P144	CAN0_RX	CAN1_RX(PDM_BIT0)	PDM_BIT_STREAM0/J17	I, 1.8V CMOS	CAN 1 Receiver.
P145	CAN1_TX	CAN2_TX(GPIO_IO25)	GPIO_IO25/V21	O, 1.8V CMOS	CAN 2 Transmitter.
P146	CAN1_RX	CAN2_RX(GPIO_IO27)	GPIO_IO27/W21	I, 1.8V CMOS	CAN 2 Receiver.

2.7.13 I2C Interface

SMARC Specification V2.1.1 supports Five I2C but i.MX 93 or i.MX 91 SMARC SOM supports only two I2C in default configuration and third I2C as optional which are listed down:

For more details of I2C pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	CSI1_TX+ / I2C_CAM1_CK	I2C7_SCL(GPIO_IO07)	GPIO_IO07/ L21	O, 1.8V CMOS/ 4.7K PU	MIPI CSI I2C Clock. *Note: This I2C7_SCL line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S139 (I2C_LCD_CK).*
S2	CSI1_TX- / I2C_CAM1_DAT	I2C7_SDA(GPIO_IO06)	GPIO_IO06/ AD18	IO, 1.8V CMOS/ 4.7K PU	MIPI CSI I2C Data. *Note: This I2C7_SDA line is also connected to the on-SOM I/O expanders (x20, x21), the on-SOM RTC controller(x51), and pin S140 (I2C_LCD_DAT).*
S48	I2C_GP_CK	I2C3_SCL(GPIO_IO29)	GPIO_IO29/ Y21	O, 1.8V CMOS 4.7K PU	General Purpose I2C Clock. *Note: This I2C3_SCL is also connected to on-SOM EEPROM.*
S49	I2C_GP_DAT	I2C3_SDA(GPIO_IO28)	GPIO_IO28/ W20	IO, 1.8V CMOS 4.7K PU	General Purpose I2C Data. *Note: This I2C3_SDA is also connected to on-SOM EEPROM.*
S139	I2C_LCD_CK	I2C7_SCL(GPIO_IO07)	GPIO_IO07/ L21	O, 1.8V CMOS/	Display Purpose I2C Clock.

				4.7K PU	*Note: This I2C7_SCL is also connected to on-SOM IO expanders and pin S1 (I2C_CAM1_CK).*
S140	I2C_LCD_DAT	I2C7_SDA(GPIO_IO06)	GPIO_IO06/ AD18	IO, 1.8V CMOS/ 4.7K PU	Display Purpose I2C Clock. *Note: This I2C7_SDA is also connected to on-SOM IO expanders and pin S2 (I2C_CAM1_DAT).*
P121	I2C_PM_CK	PMIC_I2C2_SCL	I2C2_SCL/ D20	O, 1.8V CMOS 4.7K PU	NC. *Note: By default, connected to PMIC_I2C*
P122	I2C_PM_DAT	PMIC_I2C2_SDA	I2C2_SDA/ D21	IO, 1.8V CMOS 4.7K PU	NC. *Note: By default, connected to PMIC_I2C*

2.7.14 SMARC GPIOs

SMARC V2.1.1 supports 14 GPIOs, which can be used for any general-purpose application and are listed below. But, if extra GPIO are required then refer **"i.MX 93 or i.MX 91 Pin Multiplexing on SMARC Edge"** table, which gives all optional GPIO supported via Edge connector.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P108	GPIO0 / CAM0_PWR#	SMARC_GPIO0_GPIO2_IO12(GPIO_IO09)	GPIO_IO12/ N20	IO, 1.8V CMOS	SMARC General Purpose Input/output 0.
P109	GPIO1 / CAM1_PWR#	SMARC_GPIO1_GPIO2_IO13(GPIO_IO13)	GPIO_IO13/ N21	IO, 1.8V CMOS	SMARC General Purpose Input/output 1.
P110	GPIO2 / CAM0_RST#	SMARC_GPIO2(IO3_00)	-	IO, 1.8V CMOS	SMARC General Purpose Input/output 2. *Note: Connected to on-SOM IO Expander.*
P111	GPIO3 / CAM1_RST#	SMARC_GPIO3(IO3_05)	-	IO, 1.8V CMOS	SMARC General Purpose Input/output 3. *Note: Connected to on-SOM IO Expander.*
P112	GPIO4 / HDA_RST#	SMARC_GPIO4_GPIO2_IO22(GPIO_IO22)	GPIO_IO22/ U18	IO, 1.8V CMOS	SMARC General Purpose Input/output 4.
P113	GPIO5 / PWM_OUT	SMARC_GPIO5_GPIO2_IO23(GPIO_IO23)	GPIO_IO23/ U20	IO, 1.8V CMOS	SMARC General Purpose Input/output 5.
P114	GPIO6 / TACHIN	SMARC_GPIO6_GPIO2_IO24(GPIO_IO24)	GPIO_IO24/ U21	IO, 1.8V CMOS	SMARC General Purpose Input/output 6.

P115	GPIO7	SMARC_GPIO7_GPIO2_IO26(GPIO_IO26)	GPIO_IO26/V20	IO, 1.8V CMOS	SMARC General Purpose Input/output 7.
P116	GPIO8	SMARC_GPIO8(IO3_01)	-	IO, 1.8V CMOS	SMARC General Purpose Input/output 8. *Note: Connected to on-SOM IO Expander.*
P117	GPIO9	SMARC_GPIO9_GPIO1_IO1(I2C1_SDA)	I2C1_SDA/C21	IO, 1.8V CMOS	SMARC General Purpose Input/output 9.
P118	GPIO10	SMARC_GPIO10_GPIO3_IO30(JTAG_TCK)	DAP_TCLK_SWCLK/Y1	IO, 1.8V CMOS	SMARC General Purpose Input/output 10. *Note: Muxed with JTAG_TCK which is not supported by default.*
P119	GPIO11	SMARC_GPIO11_GPIO3_IO31(JTAG_TDO)	DAP_TDO_TRACESWO/Y2	IO, 1.8V CMOS	SMARC General Purpose Input/output 11. *Note: Muxed with JTAG_TDO which is not supported by default.*
S142	GPIO12	SMARC_GPIO12(JTAG_TMS)	DAP_TMS_SWDIO/W2	IO, 1.8V CMOS	NC (Optionally SMARC General Purpose Input/output 12). *Note: Muxed with JTAG_TMS which is not supported by default.*
S123	GPIO13	SMARC_GPIO13(JTAG_TDI)	DAP_TDI/W1	IO, 1.8V CMOS	NC (Optionally SMARC General Purpose Input/output 13). *Note: Muxed with JTAG_TDI which is not supported by default.*

2.7.15 Control Signals

SMARC V2.1.1 specification supports control Signals, for more details on SMARC Control Signals pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P126	RESET_OUT#	RESETOUT#_GPIO3_IO27(CCM_CLKO2)	CCM_CLKO2/Y3	I, 1.8V CMOS	RESET OUT from SoC to all other peripherals.
P127	RESET_IN#	PMIC_RST_B	NA	I, 1.8V CMOS 100K PU	Hard RESET Input to SOM.
P128	POWER_BTN#	CPU_ON_OFF	ONOFF/A19	I, 1.8V CMOS 100K PU	Power ON /OFF Input to SOM.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	I, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier Board power supplies shall not be enabled while this signal is held low by the Carrier.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	O, 1.8V CMOS	Carrier Board power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	O, 1.8V CMOS 10K PU	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.
S157	TEST#	TEST#	NA	I, 1.8V CMOS	Not supported. *Note: This pin is connected to GND in SOM.*

2.7.16 Boot Select

The i.MX 93 or i.MX 91 SMARC SOM supports three Boot Select pins as per SMARC V2.1.1 specification. i.MX 93 or i.MX 91 SMARC SOM supports booting from On-SOM eMMC and SMARC SD (from carrier board). Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

Boot Select Pins			Description
BOOT_SEL2#	**BOOT_SEL1#**	**BOOT_SEL0#**	
HIGH	HIGH	GND	eMMC Flash (uSDHC1)
GND	GND	HIGH	SMARC SD (uSDHC2)

Also, i.MX 93 or i.MX 91 SMARC SOM supports active low FORCE_RECOV# functionality as per SMARC V2.1.1 specification. Pulling low this pin forces the i.MX 93 or i.MX 91 SoC to serial download mode where the SoC boot media can be programmed through i.MX 93 or i.MX 91 SoC's USB1 controller USB 2.0 interface which is connected to USB0 port of SMARC PCB Edge connector.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P123	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 0
P124	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 1
P125	BOOT_SEL2#	BOOT_SEL2#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 2
S155	FORCE_RECOV#	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Active low Force Recovery Input.

2.7.17 Other Signals

The i.MX 93 or i.MX 91 SMARC SOM optionally supports ADC and TAMPER signals.

For more details on ADC and TAMPER signals pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S4	RSVD1	ADC_IN0	ADC_IN0/B19	Analog, 0V -1.8V	Analog Digital Converter 0
S5	CSI0_TX-/ I2C_CAM0_CK	ADC_IN1	ADC_IN1/A20	Analog, 0V -1.8V	Analog Digital Converter 1
S6	CAM_MCK	ADC_IN2	ADC_IN2/B20	Analog, 0V -1.8V	Analog Digital Converter 2
S7	CSI0_TX+/ I2C_CAM0_DAT	ADC_IN3	ADC_IN3/B21	Analog, 0V -1.8V	Analog Digital Converter 3
P72	RSVD4	TAMPER0	TAMPER0/B16	-	Tamper Pin 0
P73	RSVD5	TAMPER1	TAMPER1/F14	-	Tamper Pin 1

2.7.18 Power and GND

The i.MX 93 or i.MX 91 SMARC SOM works with 5V power input (VCC) from SMARC PCB Edge Connector and generates all other required powers internally On-SOM itself. i.MX 93 or i.MX 91 SMARC SOM also supports coin cell power input (VDD_RTC) from SMARC PCB Edge Connector to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage.
P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S13, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	GND	GND	NA	Power	Ground.
S147	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.8 Other Features

2.8.1 UART Header (Optional)

The i.MX 93 or i.MX 91 SMARC SOM optionally supports 3pin UART header. The i.MX 93 or i.MX 91 SoC's UART1 can be connected to this header. This UART header (J2) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Number of Pins - 3

Connector Part - M20-9960345 from Harwin Inc.

Table 4: Debug UART Header Pin Assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	UART1_TXD(BOOT_MODE0)	UART1_TXD/E21	O, 1.8V CMOS	UART Transmitter
2	UART1_RXD	UART1_RXD/E20	I, 1.8V CMOS	UART Receiver
3	GND	NA	Power	Ground

2.8.2 JTAG Header (Optional)

The i.MX i.MX 93 or i.MX 91 SMARC SOM optionally supports JTAG interface for SoC debug purpose. A customized 20-pin ARM JTAG connector (J6) is available in SOM for JTAG interface. The i.MX i.MX 93 or i.MX 91 SoC's JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector (J6) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Number of Pins - 20

Connector Part - GRPB102MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

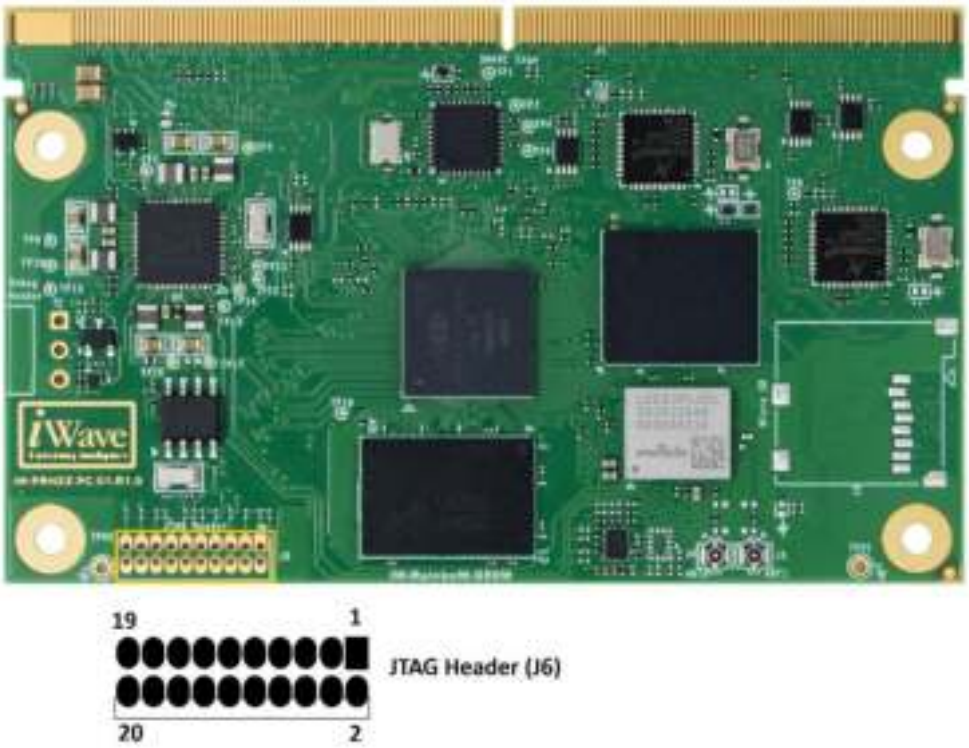


Table 5: JTAG Header Pin Assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VDD_1V8	NA	O, 1.8V Power	VTREF Voltage Reference.
2	VFRE_JTAG1	NA	O, 1.8V Power	Supply Voltage.
3	-	NA	10K PU	Only pull up is provided.
4	GND	NA	Power	Ground.
5	JTAG_CONN_TDI	DAP_TDI/ W1	I, 1.8V CMOS/ 10K PU	JTAG test data input. *By default, connected to SMARC GPIO13.*
6	GND	NA	Power	Ground.
7	JTAG_CONN_TMS	DAP_TMS_SWDIO/ W2	I, 1.8V CMOS/ 10K PU	JTAG test mode select. *By default, connected to SMARC GPIO12.*
8	GND	NA	Power	Ground.
9	JTAG_CONN_TCK	DAP_TCLK_SWCLK/ Y1	I, 1.8V CMOS/ 10K PD	JTAG test Clock. *By default, connected to SMARC GPIO10.*
10	GND	NA	Power	Ground.
11	-	NA	10K PD	Only pull down is provided.
12	GND	NA	Power	Ground.
13	JTAG_CONN_TDO	DAP_TDO_TRACESWO/ Y2	O, 1.8V CMOS	JTAG test data output.
14	GND	NA	Power	Ground.

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
15	-	NA	10K PU	Only pull up is provided.
16	GND	NA	Power	Ground.
17	-	NA	10K PU	Only pull up is provided.
18	GND	NA	Power	Ground.
19	-	NA	10K PD	Only pull down is provided.
20	GND	NA	Power	Ground.

2.8.3 TPM2.0 (Optional)

The i.MX 93 or i.MX 91 SMARC SOM optionally TPM2.0. The i.MX 93 or i.MX 91 SoC's SPI4 is optionally connected to this Trusted Platform Module. It implements version 2.0 of the Trusted Computing Group® (TCG) specification for Trusted Platform Modules (TPM).

2.9 i.MX 93 or i.MX 91 Pin Multiplexing on SMARC LGA

The i.MX 93 or i.MX 91 SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 93 or i.MX 91 SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 93 or i.MX 91 SoC pin connections to the SMARC edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 93 or i.MX 91 Hardware Reference Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SMARC SOM Edge connector for iWave's BSP reusability and to have compatible SMARC modules in future for upgradability.

Table 6: i.MX 93 or i.MX 91 SoC IOMUX for SMARC Edge Connector interfaces

Interface/ Function	SMARC Edge Pin Number	i.MX 93 or i.MX 91 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
SD Interface	P36	AA19	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]		
	P34	Y19	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]		
	P39	Y18	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]		
	P40	AA18	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		
	P41	Y20	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
	P42	AA20	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]		
	P37	AA17	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]		
	P35	Y17	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
SPI0	P43	R18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]
	P44	T21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK
	P45	R17	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
	P46	T20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]
	P31	R20	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
SPI1 (Optional)	P54	M20	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
	P56	N18	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
	P57	M21	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]
	P58	N17	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
UART1	P130	E20	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]		
	P129	E21	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]		
	P132	F20	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
	P131	F21	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]		
UART5	P136	J21	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
	P137	J20	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
	P138	K21	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
	P139	K20	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
UART6	P134	L17	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]
	P135	L18	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
UART3	P140	P20	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]

Interface/ Function	SMARC Edge Pin Number	i.MX 93 or i.MX 91 SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
	P141	P21	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
Audio SAI1	S41	H20	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
	S42	G20	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		
	S40	H21	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]		
	S39	G21	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]		
CAN1	P143	G17	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX	
	P144	J17	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX	
CAN2	P145	V21	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
	P146	W21	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
I2C3	S48	Y21	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]
	S49	W20	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]
I2C7	S1, S139	L21	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]
	S2, S140	L20	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
I2C2 (Optionl)	P121	D20	i2c2.SCL	i3c1.PUR	uart2.DCB_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
	P122	D21	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
Control Signal	P126	Y3	ccmsrcgpcmix.CLKO2				flexio1.FLEXIO[27]	gpio3.IO[27]		
	S145	J18	wdog1.WDOG_ANY					gpio1.IO[15]		
GPIO	P108	N20	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
	P109	N21	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
	P112	U18	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
	P113	U20	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
	P114	U21	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
	P115	V20	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
	P117	C21	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]		
	P118	Y1	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B	
	P119	Y2	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX	
	S142	W2	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B	
	S123	W1	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX	

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 93 or i.MX 91 SMARC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VDD_IN that may vary over the 4.5V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.5V to 5.25V. Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX 93 or i.MX 91 SMARC SOM.

Table 7: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V [1]	4.75	5V	5.25	-
2	VDD_RTC [2]	-	3V	-	-

[1] i.MX 93 or i.MX 91 SMARC SOM is designed to work with VDD_IN input power rail from SMARC PCB Edge connector only. VDD_IN can be as low as 3.3V with sufficient current if fan is not used.

[2] i.MX 93 or i.MX 91 SMARC SOM use this voltage as backup power source to RTC controller when VDD_IN is off.

3.1.2 Power Input Sequencing

The i.MX 93 or i.MX 91 SMARC SOM Power Input sequence requirement is explained below.

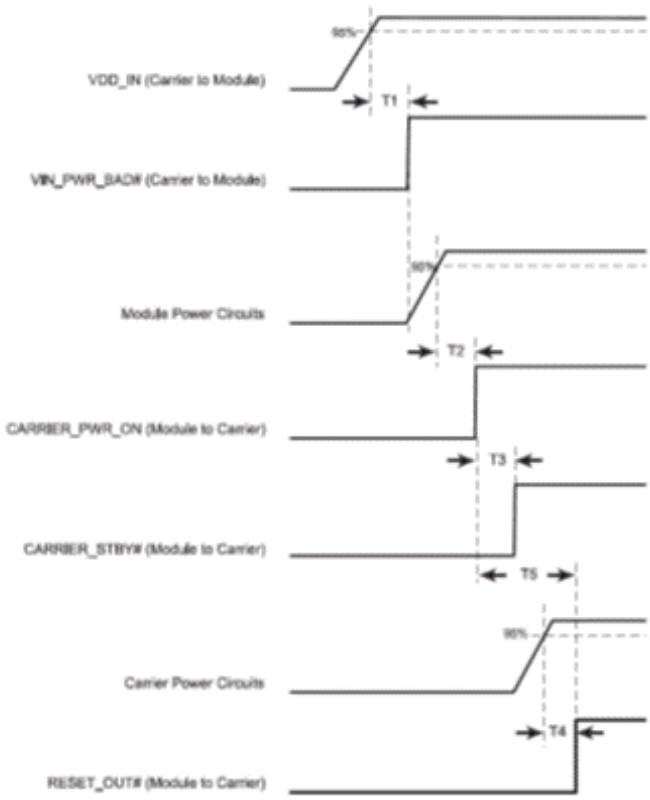


Figure 7: Power Input Sequencing

Table 8: Power Sequence Timing

Item	Description	Value
T1	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T2	VIN_PWR_BAD# rise time to SOM Power rise time	≥ 0 ms
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	≥ 0 ms
T4	Carrier power circuits are up to RESET_OUT# rise	≥ 0 ms
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 to 500ms

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/bootup issues due to reverse current flows. NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.1.3 Power Consumption

Table 9: i.MX 93 SMARC SOM Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Boot time Power consumption		
While booting	VDD_IN	0.34A/1.7W
Run Mode Power Consumption		
Play Audio	VDD_IN	0.19A/0.95W
Camera Streaming in MIPI Display	VDD_IN	0.22A/1.1W
Camera Streaming in LVDS Display	VDD_IN	0.21A/1.05W
Play Video run in LVDS Display (Gplay)	VDD_IN	0.29A/1.45W
Play Video run in MIPI Display (Gplay)	VDD_IN	0.25A/1.25W
Ping Bluetooth	VDD_IN	0.23A/1.15W
Ping Wifi	VDD_IN	0.23A/1.15W
Ping Ethernet (Eth0) at 1000Mbps	VDD_IN	0.3A/1.5W
Ping Ethernet (Eth1) at 1000Mbps	VDD_IN	0.27A/1.35W
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VDD_IN	0.38A/1.9W
eMMC to USB2.0 x 2 Host file transfer	VDD_IN	0.25A/1.25W
eMMC to USB2.0 x1 OTG as Host file transfer	VDD_IN	0.22A/1.1W
eMMC to USB 2.0 x 1 Type C Host file transfer	VDD_IN	0.3A/1.5W
eMMC to Standard SD file transfer	VDD_IN	0.26A/1.3W
File Transfer - Transfer the 1MB files between storage devices	VDD_IN	0.34A/1.7W
Dhrystone	VDD_IN	0.29A/1.45
Bluetooth file transfer	VDD_IN	0.26A/1.3W
Wi-Fi file transfer	VDD_IN	0.43A/2.15W
Ethernet Streaming (Video Play)	VDD_IN	0.27A/1.35W
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1MB files in storage devices • Run the dry2 application on background • Ping Wifi • Camera Streaming • Play Video in LVDS	VDD_IN	0.63A/3.15W
Low Power Mode Power Consumption		
System Idle Mode	VDD_IN	0.14A/0.7W
Deep Sleep Mode	VDD_IN	0.03A/0.15W
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	0.4uA/2uW

Power consumption measurements have been done in iWave's i.MX 93 SMARC SOM with iWave's iW-PRHZZ-SC-01-R1.0-REL0.1-Linux6.1.22 BSP.

Table 10: i.MX 91 SMARC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Boot time Power consumption		
While booting	VCC_IN_5V	TBD
Run Mode Power Consumption		
Play Audio	VCC_IN_5V	TBD
Ping Bluetooth	VCC_IN_5V	TBD
Ping Wi-Fi	VCC_IN_5V	TBD
Ping Ethernet (Eth0) at 1000Mbps	VCC_IN_5V	TBD
Ping Ethernet (Eth1) at 1000Mbps	VCC_IN_5V	TBD
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_IN_5V	TBD
eMMC to USB2.0 Host file transfer	VCC_IN_5V	TBD
eMMC to USB2.0 OTG as host file transfer	VCC_IN_5V	TBD
eMMC to USB 2.0 x 1 Type C Host file transfer	VCC_IN_5V	TBD
eMMC to Micro SD file transfer	VCC_IN_5V	TBD
File Transfer - Transfer the 1GB files in storage devices	VCC_IN_5V	TBD
Dhrystone	VCC_IN_5V	TBD
Bluetooth file transfer	VCC_IN_5V	TBD
Wi-fi File transfer	VCC_IN_5V	TBD
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • Ping Wi-fi	VCC_IN_5V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_IN_5V	TBD
Deep Sleep Mode.	VCC_IN_5V	TBD
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	TBD

Power consumption measurements have been done in iWave's i.MX 93 SMARC SOM with iWave's iW-PRHZZ-SC-01-R1.0-REL0.1-Linux6.1.22 BSP.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 93 or i.MX 91 SMARC SOM.

Table 11: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution & Heat sink, refer the following section.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink Solution for i.MX 93 or i.MX 91 SMARC SOM. For more information on Heat Sink contact iWave support team. Do not Power ON the SOM without a proper thermal solution.

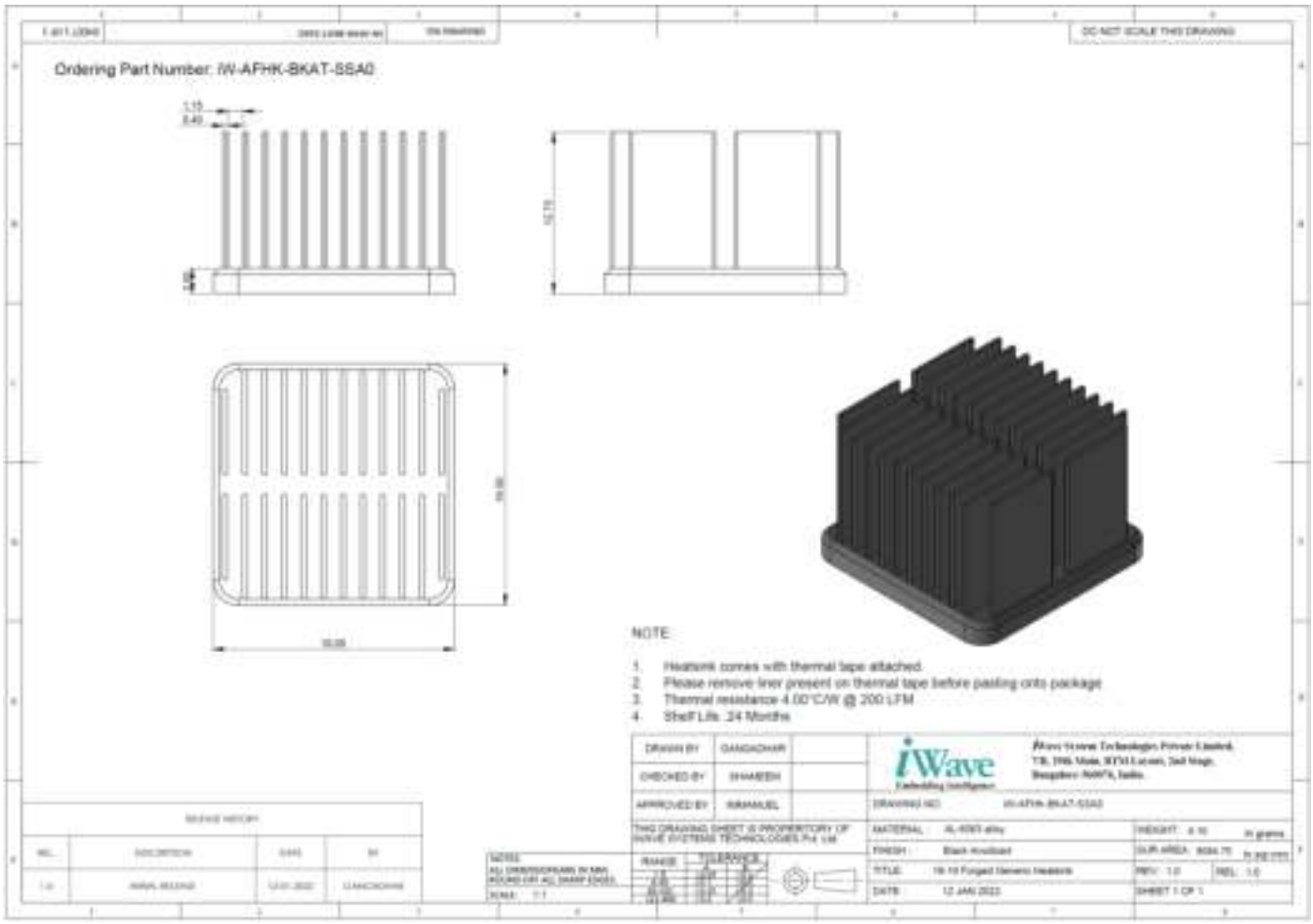


Figure 8: Mechanical dimension of Heat Sink

3.2.3 RoHS Compliance

iWave's i.MX 93 or i.MX 91 SMARC SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 93 or i.MX 91 SMARC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 93 or i.MX 91 SMARC SOM Mechanical Dimensions

i.MX 93 or i.MX 91 SMARC SOM PCB size is 50 mm x 82mm x 1.2mm. The i.MX 93 or i.MX 91 SMARC SOM PCB thickness is 1.2mm±0.15mm, top side maximum height component is JTAG header (3.4mm) followed by UART Header (2.54mm), followed by uSD Connector GTFP08431BEU (1.85mm) which are optional in default configuration hence RTC Controller (1.75mm) will be the maximum height on Top side in default configuration. In bottom side maximum height component is EEPROM (1.2mm).

component is EEPROM (1.2mm).

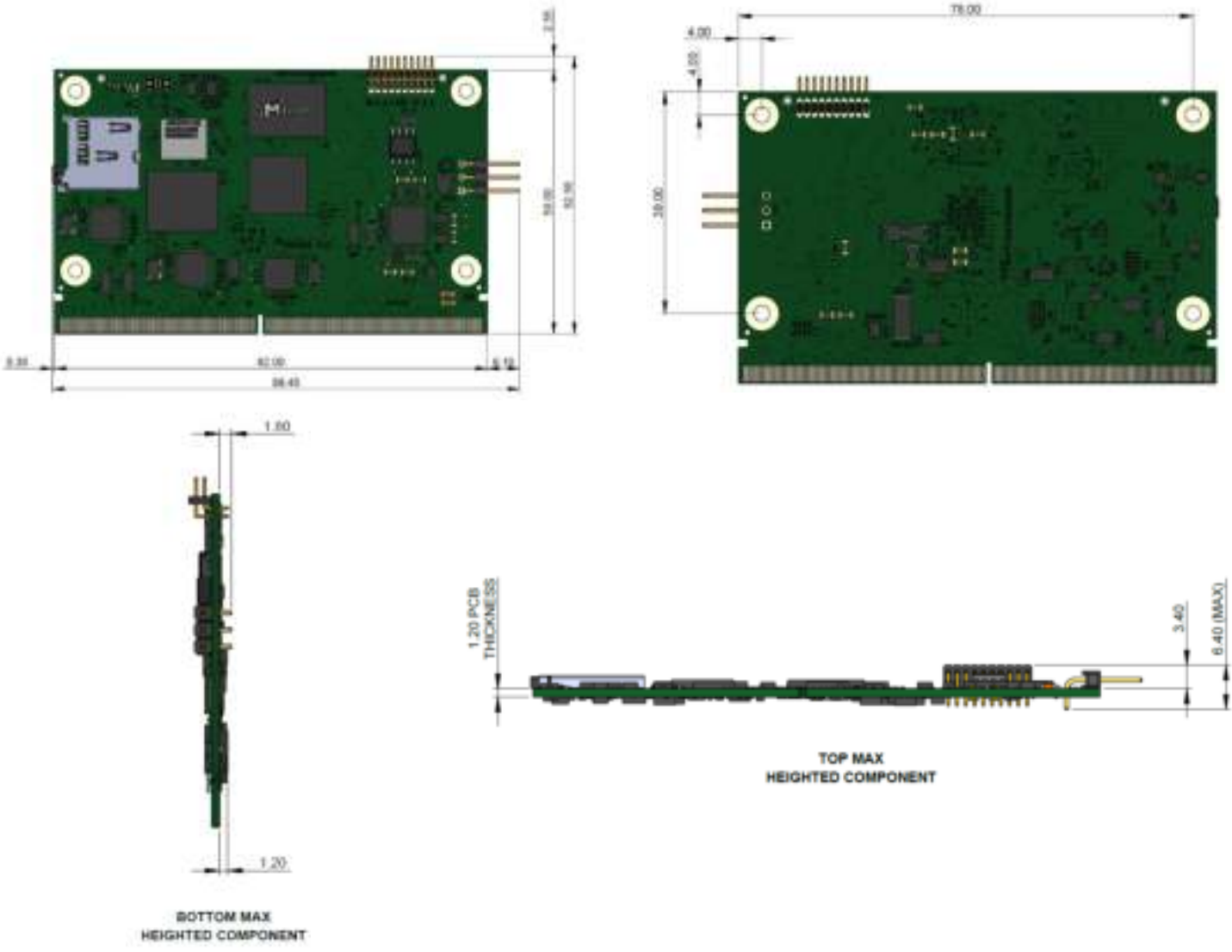


Figure 9: i.MX 93 or i.MX 91 SMARC SOM Mechanical Dimensions

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 93 or i.MX 91 SMARC SOM variants. Please contact iWave for orderable part number of different RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 12: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G50M - i.MX 9352 R1.0 SMARC SOM (Industrial grade)- With Wi-Fi, BT		
iW-G50M-SC93-4L002G-E016G-BID	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 9352 R1.0 SMARC SOM (Industrial grade)- Without Wi-Fi, BT		
iW-G50M-SC93-4L002G-E016G-BIE	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-Without Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 9131 R1.0 SMARC SOM (Industrial grade)- With Wi-Fi, BT		
iW-G50M- SC91-4L001G-E008G-BIA	i.MX 9131 Single, 1GB LPDDR4, 8GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 9131 R1.0 SMARC SOM (Industrial grade)- Without Wi-Fi, BT		
iW-G50M- SC91-4L001G-E008G-BIB	i.MX 9131 Single, 1GB LPDDR4, 8GB eMMC-Without Wi-Fi, BT	-40°C to 85°C

Note:

- *Custom configuration Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*
- *For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.*

5. APPENDIX

5.1 i.MX 93 or i.MX 91 SMARC SOM Development Platform

iWave Global supports iW-RainboW-G50D-i.MX 93 or i.MX 91 SMARC SOM Development Platform which is targeted for quick validation of i.MX 93 or i.MX 91 SoC based SMARC SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete SMARC supported features.

For more details on i.MX 93 or i.MX 91 SMARC SOM and Development Platform, visit the below web link.

https://www.iwavesystems.com/product/i-mx-93-i-mx-91-smarc-som/

Figure 10: i.MX 93 or i.MX 91 SMARC SOM Development Platform

A Global Leader in Embedded Systems Engineering and Solutions

Since 1999, we have pioneered leadership in embedded systems technology, establishing ourselves as a strategic embedded technology partner for advanced solutions. Our comprehensive portfolio encompasses ARM and FPGA System on Modules, COTS FPGA solutions, and ODM solutions which include Telematics, Gateways & HMI Solutions.

Beyond our robust product ecosystem, we provide comprehensive ODM support with specialized custom design and manufacturing capabilities, enabling customers to accelerate and optimize their product development roadmaps. With a strategic focus on industrial, automotive, medical, and avionics markets, we deliver innovative technology solutions to global clients.

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