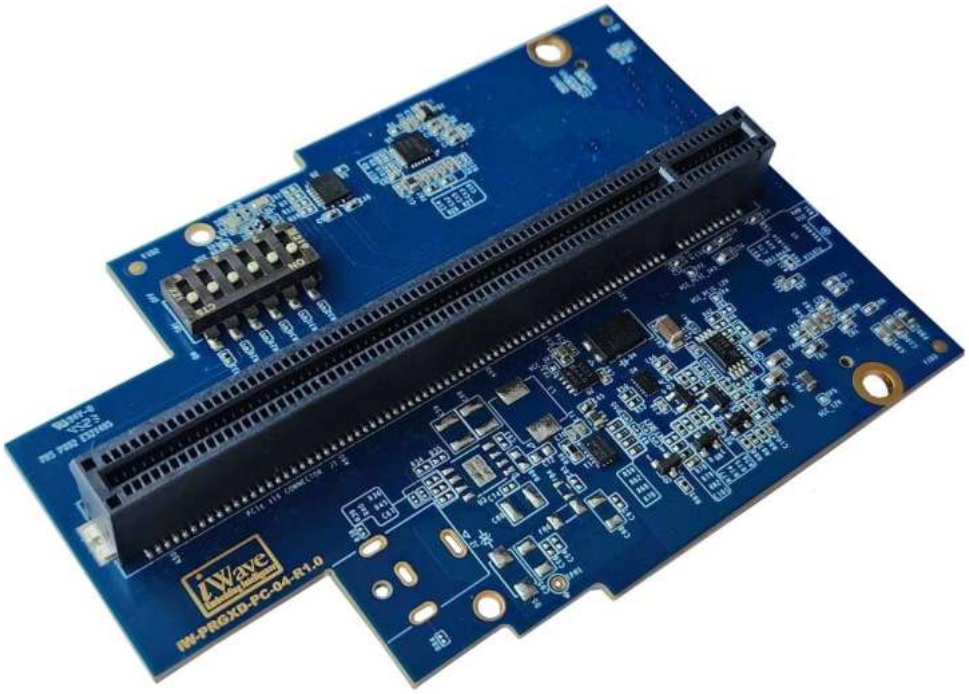
FMC+ PCIe x16 Gen4/Gen3/Gen2/Gen1

Module Datasheet



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1. INTRODUCTION

1.1 Purpose

This document is the Datasheet for the FMC+ PCIe x16 Gen4/Gen3/Gen2/Gen1 (Vita57.4) Module Board and provides detailed information on the overall design & usage of the Carrier Board from a Hardware Systems perspective.

1.2 Overview

The FMC+ PCIe x16 Module can be used for quick validation for PCIe Gen4/Gen3/Gen2/Gen1 x16 Root port and End point mode of operation.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
B2B	Board to Board
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor Signal
FMC+	FPGA Mezzanine Card Plus
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RX	Receiver
SOM	System On Module
TX	Transmitter
TXVR	Transceiver

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Vita57.4 FMC+ Specification
- Vita57.1 FMC Specification

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the FMC+ PCIe x16 Module features with high level block diagram and detailed information about each block.

2.1 FMC+ PCIe x16 Module Block Diagram

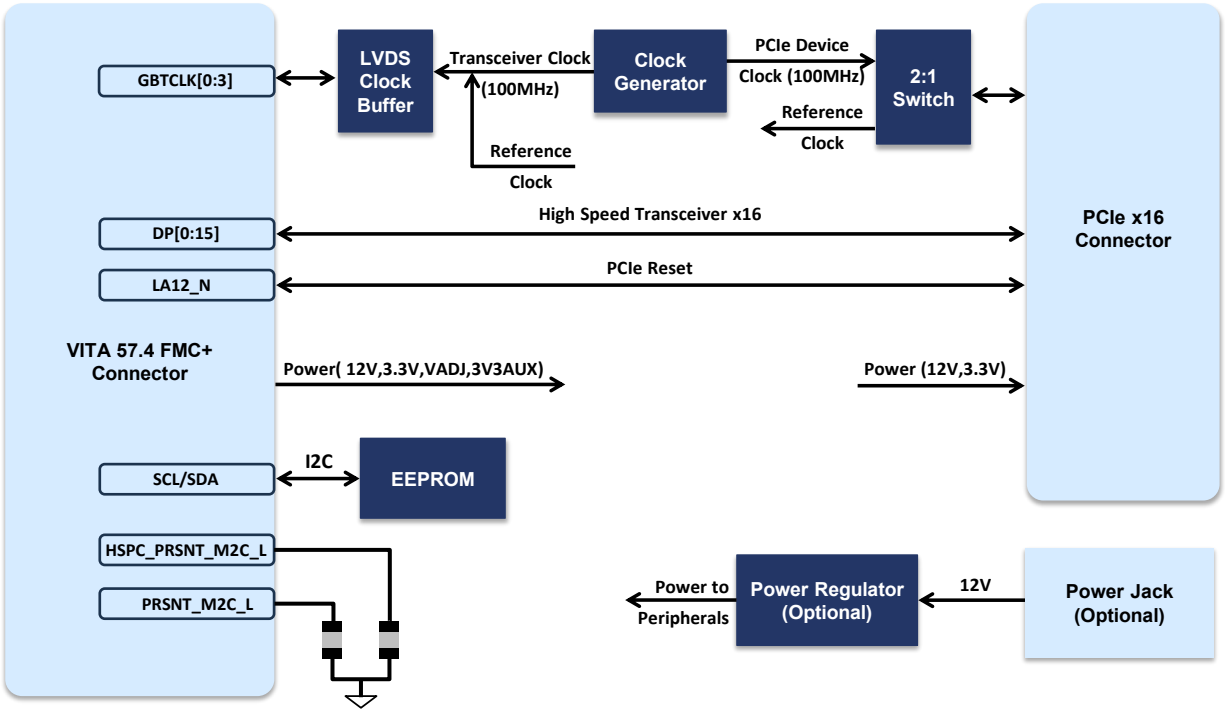

Figure 1: FMC+ PCIe x16 Module Block Diagram

2.2 PCIe x16 FMC+ Module Features

The FMC+ PCIe x16 Module supports the following features through ANSI/VITA 57.4 FMC+ Connector.

- PCIe Gen4/Gen3/Gen2/Gen1 x16 Connector
- 32Kb EEPROM

Additional Features

- 100MHz Clock from Clock Oscillator
- 4 Output Clock Buffer

General Specification

- Power: From FMC+ connector
- Form Factor: 98.5mm X 69mm

2.2.1 FMC+ Connector

The FMC+ PCIe x16 Module support one 560 Pin standard FMC+ VITA 57.4 connector. This FMC+ Connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications.

This FMC+ PCIe x16 Module supports 16 High speed transceivers, 4 transceiver Clock for reference and 6 SE IOs for reset, wake and PRSNT pins of PCIe connector.

This 560 Pin FMC+ Connector (J3) is physically located at the bottom of the module as shown below.

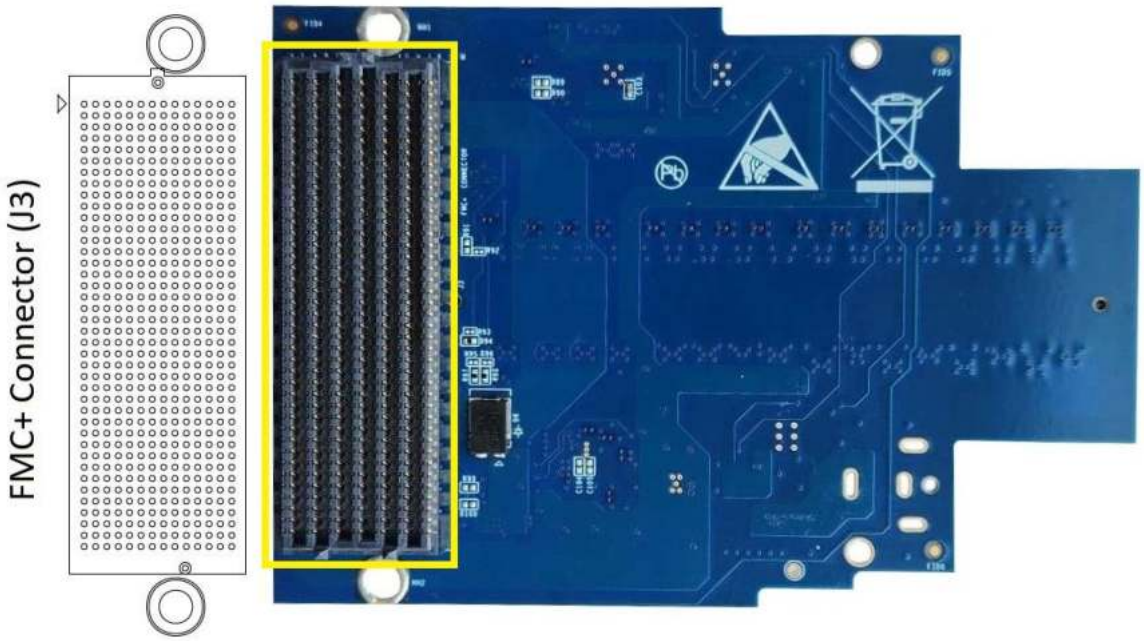

Figure 2: FMC+ Connector

FMC+ connector (J3) pin mapping is shown below.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	NC	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	NC	GND	GND	NC	PRSNT_M2C_L	NC	GND	NC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	NC
3	NC	GND	GND	NC	GND	NC	GND	NC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	NC
4	GND	NC	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	NC	GND
5	GND	NC	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	NC	GND
6	NC	GND	GND	NC	GND	NC	GND	NC	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	NC
7	NC	GND	NC	NC	NC	NC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	NC
8	GND	GBTCLK3_M2C_P	NC	GND	NC	GND	NC	GND	NC	GND	DP8_M2C_P	GND	NC	GND
9	GND	GBTCLK3_M2C_N	GND	NC	GND	NC	GND	NC	NC	GND	DP8_M2C_N	GND	NC	GND
10	NC	GND	NC	NC	NC	NC	NC	NC	GND	NC	GND	DP3_M2C_P	GND	DP10_M2C_P
11	NC	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	NC	GND	LA08_P	GND	NC	NC	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	NC	NC	NC	LA08_N	NC	NC	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	NC	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP4_M2C_P	GND	DP12_M2C_P
15	NC	GND	GND	NC	GND	LA12_P	GND	NC	NC	NC	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	NC	NC	NC	NC	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	NC	NC	GND	NC	GND	NC	GND	NC	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	NC	GND	LA16_P	GND	NC	NC	NC	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	NC	NC	NC	LA16_N	NC	NC	GND	NC	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	NC	NC	GND	NC	GND	NC	GND	NC	GND	GBTCLK1_M2C_P	GND	NC	GND
21	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	GBTCLK1_M2C_N	GND	NC	GND
22	DP15_C2M_P	GND	NC	NC	NC	NC	NC	NC	GND	NC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	NC	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP2_C2M_P	GND	DP11_C2M_P
27	NC	GND	GND	NC	GND	NC	GND	NC	NC	NC	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	NC	NC	NC	NC	NC	NC	NC	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	NC	NC	GND	NC	GND	NC	GND	NC	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	NC	GND	GND	NC	GND	NC	GND	NC	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	NC	GND	NC	NC	NC	NC	NC	NC	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	NC	NC	GND	NC	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND	NC	GND
33	GND	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP7_C2M_N	GND	NC	GND
34	NC	GND	NC	NC	NC	NC	NC	NC	NC	GA0	GND	DP4_C2M_P	GND	NC
35	NC	GND	NC	GND	NC	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N	GND	NC
36	GND	12P0V	GND	NC	GND	NC	GND	NC	3P3V	GND	DP6_C2M_P	GND	NC	GND
37	GND	12P0V	NC	NC	NC	NC	NC	NC	GND	12P0V	DP6_C2M_N	GND	NC	GND
38	NC	GND	NC	GND	NC	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P	GND	NC
39	NC	GND	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	NC
40	GND	12P0V	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC	GND	3P3V	GND

Figure 3: FMC+ Connector Pin Out

Table 3: FMC+ Connector Pin Assignment

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	HS_TXVR0_RX_CH1p	O, DIFF	PCIe Lane1 Receive pair positive.
A3	DP1_M2C_N	HS_TXVR0_RX_CH1n	O, DIFF	PCIe Lane1 Receive pair negative.
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	HS_TXVR0_RX_CH2p	O, DIFF	PCIe Lane2 Receive pair positive.
A7	DP2_M2C_N	HS_TXVR0_RX_CH2n	O, DIFF	PCIe Lane2 Receive pair negative.
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	HS_TXVR0_RX_CH3p	O, DIFF	PCIe Lane3 Receive pair positive.
A11	DP3_M2C_N	HS_TXVR0_RX_CH3n	O, DIFF	PCIe Lane3 Receive pair negative.
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	HS_TXVR1_RX_CH0p	O, DIFF	PCIe Lane4 Receive pair positive.
A15	DP4_M2C_N	HS_TXVR1_RX_CH0n	O, DIFF	PCIe Lane4 Receive pair negative.
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	HS_TXVR1_RX_CH1p	O, DIFF	PCIe Lane5 Receive pair positive.
A19	DP5_M2C_N	HS_TXVR1_RX_CH1n	O, DIFF	PCIe Lane5 Receive pair negative.
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	HS_TXVR0_TX_CH1p	I, DIFF	PCIe Lane1 Transmit pair positive.
A23	DP1_C2M_N	HS_TXVR0_TX_CH1n	I, DIFF	PCIe Lane1 Transmit pair negative.
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	HS_TXVR0_TX_CH2p	I, DIFF	PCIe Lane2 Transmit pair positive.
A27	DP2_C2M_N	HS_TXVR0_TX_CH2n	I, DIFF	PCIe Lane2 Transmit pair negative.
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	HS_TXVR0_TX_CH3p	I, DIFF	PCIe Lane3 Transmit pair positive.
A31	DP3_C2M_N	HS_TXVR0_TX_CH3n	I, DIFF	PCIe Lane3 Transmit pair negative.
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	HS_TXVR1_TX_CH0p	I, DIFF	PCIe Lane4 Transmit pair positive.
A35	DP4_C2M_N	HS_TXVR1_TX_CH0n	I, DIFF	PCIe Lane4 Transmit pair negative.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	HS_TXVR1_TX_CH1p	I, DIFF	PCIe Lane5 Transmit pair positive.
A39	DP5_C2M_N	HS_TXVR1_TX_CH1n	I, DIFF	PCIe Lane5 Transmit pair negative.
A40	GND	GND	Power	Ground.
B1	CLK_DIR	NA	NA	NC.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	HS_TXVR2_RX_CH1p	O, DIFF	PCIe Lane9 Receive pair positive.
B5	DP9_M2C_N	HS_TXVR2_RX_CH1n	O, DIFF	PCIe Lane9 Receive pair negative.
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	HS_TXVR2_RX_CH0p	O, DIFF	PCIe Lane8 Receive pair positive.
B9	DP8_M2C_N	HS_TXVR2_RX_CH0n	O, DIFF	PCIe Lane8 Receive pair negative.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	HS_TXVR1_RX_CH3p	O, DIFF	PCIe Lane7 Receive pair positive.
B13	DP7_M2C_N	HS_TXVR1_RX_CH3n	O, DIFF	PCIe Lane7 Receive pair negative.
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	HS_TXVR1_RX_CH2p	O, DIFF	PCIe Lane6 Receive pair positive.
B17	DP6_M2C_N	HS_TXVR1_RX_CH2n	O, DIFF	PCIe Lane6 Receive pair negative.
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	HS_TXVR1_REFCLK_CH0p	O, DIFF	PCIe Transceiver reference clock 1 positive.
B21	GBTCLK1_M2C_N	HS_TXVR1_REFCLK_CH0n	O, DIFF	PCIe Transceiver reference clock 1 negative.
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	HS_TXVR2_TX_CH1p	I, DIFF	PCIe Lane9 Transmit pair positive.
B25	DP9_C2M_N	HS_TXVR2_TX_CH1n	I, DIFF	PCIe Lane9 Transmit pair negative.
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	HS_TXVR2_TX_CH0p	I, DIFF	PCIe Lane8 Transmit pair positive.
B29	DP8_C2M_N	HS_TXVR2_TX_CH0n	I, DIFF	PCIe Lane8 Transmit pair negative.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	HS_TXVR1_TX_CH3p	I, DIFF	PCIe Lane7 Transmit pair positive.
B33	DP7_C2M_N	HS_TXVR1_TX_CH3n	I, DIFF	PCIe Lane7 Transmit pair negative.
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	HS_TXVR1_TX_CH2p	I, DIFF	PCIe Lane6 Transmit pair positive.
B37	DP6_C2M_N	HS_TXVR1_TX_CH2n	I, DIFF	PCIe Lane6 Transmit pair negative.
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NC	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	HS_TXVR0_TX_CH0p	I, DIFF	PCIe Lane0 Transmit pair positive.
C3	DP0_C2M_N	HS_TXVR0_TX_CH0n	I, DIFF	PCIe Lane0 Transmit pair negative.
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DP0_M2C_P	HS_TXVR0_RX_CH0p	O, DIFF	PCIe Lane0 Receive pair positive.
C7	DP0_M2C_N	HS_TXVR0_RX_CH0n	O, DIFF	PCIe Lane0 Receive pair negative.
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	NA	NA	NC
C11	LA06_N	NA	NA	NC
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	NA	NA	NC
C15	LA10_N	NA	NA	NC
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	NA	NA	NC
C19	LA14_N	NA	NA	NC
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	NA	NA	NC.
C23	LA18_N_CC	NA	NA	NC.
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
C26	LA27_P	NA	NA	NC
C27	LA27_N	NA	NA	NC
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	NA	NA	NC
C31	SDA	NA	NA	NC
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0_FMC+	I, 3.3V CMOS	Geographical address 0
C35	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.
D1	PG_C2M	FMC_PG_C2M	I, 3.3V CMOS	Power good from carrier to module
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	HS_TXVR0_REFCLK_CH0p	O, DIFF	PCIe Transceiver reference clock 0 positive.
D5	GBTCLK0_M2C_N	HS_TXVR0_REFCLK_CH0n	O, DIFF	PCIe Transceiver reference clock 0 negative.
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	NA	NA	NC
D9	LA01_N_CC	NA	NA	NC
D10	GND	GND	Power	Ground.
D11	LA05_P	NA	NA	NC
D12	LA05_N	NA	NA	NC
D13	GND	GND	Power	Ground.
D14	LA09_P	NA	NA	NC
D15	LA09_N	NA	NA	NC
D16	GND	GND	Power	Ground.
D17	LA13_P	NA	NA	NC
D18	LA13_N	NA	NA	NC
D19	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
D20	LA17_P_CC	NA	NA	NC
D21	LA17_N_CC	NA	NA	NC
D22	GND	GND	Power	Ground.
D23	LA23_P	NA	NA	NC
D24	LA23_N	NA	NA	NC
D25	GND	GND	Power	Ground.
D26	LA26_P	NA	NA	NC
D27	LA26_N	NA	NA	NC
D28	GND	GND	Power	Ground.
D29	TCK	NA	NA	NC.
D30	TDI	TDI	I, 3.3V CMOS	Connected to TDO
D31	TDO	TDO	O, 3.3V CMOS	Connected to TDI
D32	3P3VAUX	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D33	TMS	NA	NA	NC.
D34	TRST_L	NA	NA	NC.
D35	GA1	GA1_FMC+	I, 3.3V CMOS	Geographical address1
D36	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	NA	NA	NC.
E3	HA01_N_CC	NA	NA	NC.
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.
E6	HA05_P	NA	NA	NC.
E7	HA05_N	NA	NA	NC.
E8	GND	GND	Power	Ground.
E9	HA09_P	NA	NA	NC.
E10	HA09_N	NA	NA	NC.
E11	GND	GND	Power	Ground.
E12	HA13_P	NA	NA	NC.
E13	HA13_N	NA	NA	NC.
E14	GND	GND	Power	Ground.
E15	HA16_P	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
E16	HA16_N	NA	NA	NC.
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC.
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.
E39	VADJ	VCC_FMC+_ADJ	I, ADJ Power	Supply Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	FMC_PG_M2C	NA	NC.
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	NA	NA	NC.
F5	HA00_N_CC	NA	NA	NC.
F6	GND	GND	Power	Ground.
F7	HA04_P	NA	NA	NC.
F8	HA04_N	NA	NA	NC.
F9	GND	GND	Power	Ground.
F10	HA08_P	NA	NA	NC.
F11	HA08_N	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
F12	GND	GND	Power	Ground.
F13	HA12_P	NA	NA	NC.
F14	HA12_N	NA	NA	NC.
F15	GND	GND	Power	Ground.
F16	HA15_P	NA	NA	NC.
F17	HA15_N	NA	NA	NC.
F18	GND	GND	Power	Ground.
F19	HA19_P	NA	NA	NC.
F20	HA19_N	NA	NA	NC.
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC+_ADJ	I, ADJ Power	Supply Voltage.
G1	GND	GND	Power	Ground.
G2	CLK1_M2C_P	NA	NA	NC.
G3	CLK1_M2C_N	NA	NA	NC.
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	NA	NA	NC.
G7	LA00_N_CC	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
G8	GND	GND	Power	Ground.
G9	LA03_P	NA	NA	NC.
G10	LA03_N	NA	NA	NC.
G11	GND	GND	Power	Ground.
G12	LA08_P	NA	NA	NC.
G13	LA08_N	NA	NA	NC.
G14	GND	GND	Power	Ground.
G15	LA12_P	FPGA_BANK1_LVDS_CLKIN_01P	IO, VADJ LVCMOS	PCIe wake. *Note: This wake signal is input to the FMC+ module for Root Port application and output from the FMC+ module for Endpoint application.*
G16	LA12_N	FPGA_BANK1_LVDS_CLKIN_01N	IO, VADJ LVCMOS	PCIe Reset. *Note: This reset signal is input to the FMC+ module for Root Port application and output from the FMC+ module for Endpoint application.*
G17	GND	GND	Power	Ground.
G18	LA16_P	NA	NA	NC.
G19	LA16_N	NA	NA	NC.
G20	GND	GND	Power	Ground.
G21	LA20_P	NA	NA	NC.
G22	LA20_N	NA	NA	NC.
G23	GND	GND	Power	Ground.
G24	LA22_P	NA	NA	NC.
G25	LA22_N	NA	NA	NC.
G26	GND	GND	Power	Ground.
G27	LA25_P	NA	NA	NC.
G28	LA25_N	NA	NA	NC.
G29	GND	GND	Power	Ground.
G30	LA29_P	NA	NA	NC.
G31	LA29_N	NA	NA	NC.
G32	GND	GND	Power	Ground.
G33	LA31_P	NA	NA	NC.
G34	LA31_N	NA	NA	NC.
G35	GND	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
G36	LA33_P	NA	NA	NC.
G37	LA33_N	NA	NA	NC.
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC+_ADJ	I, ADJ Power	Supply Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC
H2	PRSNT_M2C_L	NA	O, 1K PD	Module Present Signal.
H3	GND	GND	Power	Ground.
H4	CLK0_M2C_P	NA	NA	NC.
H5	CLK0_M2C_N	NA	NA	NC.
H6	GND	GND	Power	Ground.
H7	LA02_P	NA	NA	NC.
H8	LA02_N	NA	NA	NC.
H9	GND	GND	Power	Ground.
H10	LA04_P	NA	NA	NC.
H11	LA04_N	NA	NA	NC.
H12	GND	GND	Power	Ground.
H13	LA07_P	NA	NA	NC.
H14	LA07_N	NA	NA	NC.
H15	GND	GND	Power	Ground.
H16	LA11_P	NA	NA	NC.
H17	LA11_N	NA	NA	NC.
H18	GND	GND	Power	Ground.
H19	LA15_P	NA	NA	NC.
H20	LA15_N	NA	NA	NC.
H21	GND	GND	Power	Ground.
H22	LA19_P	NA	NA	NC.
H23	LA19_N	NA	NA	NC.
H24	GND	GND	Power	Ground.
H25	LA21_P	NA	NA	NC.
H26	LA21_N	NA	NA	NC.
H27	GND	GND	Power	Ground.
H28	LA24_P	NA	NA	NC.
H29	LA24_N	NA	NA	NC.
H30	GND	GND	Power	Ground.
H31	LA28_P	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
H32	LA28_N	NA	NA	NC.
H33	GND	GND	Power	Ground.
H34	LA30_P	NA	NA	NC.
H35	LA30_N	NA	NA	NC.
H36	GND	GND	Power	Ground.
H37	LA32_P	NA	NA	NC.
H38	LA32_N	NA	NA	NC.
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_FMC+_ADJ	I, ADJ Power	Supply Voltage.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	NA	NA	NC.
J3	CLK3_BIDIR_N	NA	NA	NC.
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	NA	NA	NC.
J7	HA03_N	NA	NA	NC.
J8	GND	GND	Power	Ground.
J9	HA07_P	NA	NA	NC.
J10	HA07_N	NA	NA	NC.
J11	GND	GND	Power	Ground.
J12	HA11_P	NA	NA	NC.
J13	HA11_N	NA	NA	NC.
J14	GND	GND	Power	Ground.
J15	HA14_P	NA	NA	NC.
J16	HA14_N	NA	NA	NC.
J17	GND	GND	Power	Ground.
J18	HA18_P	NA	NA	NC.
J19	HA18_N	NA	NA	NC.
J20	GND	GND	Power	Ground.
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.
J27	HB07_P	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	NA	NA	NC.
J34	HB15_N	NA	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	NA	NA	NC.
K5	CLK2_BIDIR_N	NA	NA	NC.
K6	GND	GND	Power	Ground.
K7	HA02_P	NA	NA	NC.
K8	HA02_N	NA	NA	NC.
K9	GND	GND	Power	Ground.
K10	HA06_P	NA	NA	NC.
K11	HA06_N	NA	NA	NC.
K12	GND	GND	Power	Ground.
K13	HA10_P	NA	NA	NC.
K14	HA10_N	NA	NA	NC.
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	NA	NA	NC.
K17	HA17_N_CC	NA	NA	NC.
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC.
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.
L1	RES1	NA	NA	NC.
L2	GND2	GND	Power	Ground.
L3	GND3	GND	Power	Ground.
L4	GBTCLK4_M2C_P	NA	NA	NC.
L5	GBTCLK4_M2C_N	NA	NA	NC.
L6	GND4	GND	Power	Ground.
L7	GND5	GND	Power	Ground.
L8	GBTCLK3_M2C_P	HS_TXVR3_REFCLK_CH0p	O, DIFF	PCIe reference clock 3 positive.
L9	GBTCLK3_M2C_N	HS_TXVR3_REFCLK_CH0n	O, DIFF	PCIe reference clock 3 negative.
L10	GND6	GND	Power	Ground.
L11	GND7	GND	Power	Ground.
L12	GBTCLK2_M2C_P	HS_TXVR2_REFCLK_CH0p	O, DIFF	PCIe reference clock 2 positive.
L13	GBTCLK2_M2C_N	HS_TXVR2_REFCLK_CH0n	O, DIFF	PCIe reference clock 2 negative.
L14	GND8	GND	Power	Ground.
L15	GND9	GND	Power	Ground.
L16	SYNC_C2M_P	NA	NA	NC.
L17	SYNC_C2M_N	NA	NA	NC.
L18	GND10	GND	Power	Ground.
L19	GND11	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
L20	REFCLK_C2M_P	NA	NA	NC.
L21	REFCLK_C2M_N	NA	NA	NC.
L22	GND12	GND	Power	Ground.
L23	GND13	GND	Power	Ground.
L24	REFCLK_M2C_P	NA	NA	NC.
L25	REFCLK_M2C_N	NA	NA	NC.
L26	GND14	GND	Power	Ground.
L27	GND15	GND	Power	Ground.
L28	SYNC_M2C_P	NA	NA	NC.
L29	SYNC_M2C_N	NA	NA	NC.
L30	GND16	GND	Power	Ground.
L31	GND17	GND	Power	Ground.
L32	RES2	NA	NA	NC.
L33	RES3	NA	NA	NC.
L34	GND18	GND	Power	Ground.
L35	GND19	GND	Power	Ground.
L36	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
L37	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
L38	GND20	GND	Power	Ground.
L39	GND37	GND	Power	Ground.
L40	12P0V	VCC_12V_FMC+	I, 12V Power	Supply Voltage.
M1	GND1	GND	Power	Ground.
M2	DP23_M2C_P	NA	NA	NC
M3	DP23_M2C_N	NA	NA	NC
M4	GND2	GND	Power	Ground.
M5	GND3	GND	Power	Ground.
M6	DP22_M2C_P	NA	NA	NC
M7	DP22_M2C_N	NA	NA	NC
M8	GND4	GND	Power	Ground.
M9	GND5	GND	Power	Ground.
M10	DP21_M2C_P	NA	NA	NC
M11	DP21_M2C_N	NA	NA	NC
M12	GND6	GND	Power	Ground.
M13	GND7	GND	Power	Ground.
M14	DP20_M2C_P	NA	NA	NC
M15	DP20_M2C_N	NA	NA	NC

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
M16	GND8	GND	Power	Ground.
M17	GND9	GND	Power	Ground.
M18	DP14_C2M_P	HS_TXVR3_TX_CH2p	I, DIFF	PCIe Lane14 Transmit pair positive.
M19	DP14_C2M_N	HS_TXVR3_TX_CH2n	I, DIFF	PCIe Lane14 Transmit pair negative.
M20	GND10	GND	Power	Ground.
M21	GND11	GND	Power	Ground.
M22	DP15_C2M_P	HS_TXVR3_TX_CH3p	I, DIFF	PCIe Lane15 Transmit pair positive.
M23	DP15_C2M_N	HS_TXVR3_TX_CH3n	I, DIFF	PCIe Lane15 Transmit pair negative.
M24	GND12	GND	Power	Ground.
M25	GND13	GND	Power	Ground.
M26	DP16_C2M_P	NA	NA	NC
M27	DP16_C2M_N	NA	NA	NC
M28	GND14	GND	Power	Ground.
M29	GND15	GND	Power	Ground.
M30	DP17_C2M_P	NA	NA	NC
M31	DP17_C2M_N	NA	NA	NC
M32	GND16	GND	Power	Ground.
M33	GND17	GND	Power	Ground.
M34	DP18_C2M_P	NA	NA	NC
M35	DP18_C2M_N	NA	NA	NC
M36	GND18	GND	Power	Ground.
M37	GND19	GND	Power	Ground.
M38	DP19_C2M_P	NA	NA	NC
M39	DP19_C2M_N	NA	NA	NC
M40	GND20	GND	Power	Ground.
Y1	GND1	GND	Power	Ground.
Y2	DP23_C2M_P	NA	NA	NC
Y3	DP23_C2M_N	NA	NA	NC
Y4	GND2	GND	Power	Ground.
Y5	GND3	GND	Power	Ground.
Y6	DP21_C2M_P	NA	NA	NC
Y7	DP21_C2M_N	NA	NA	NC
Y8	GND4	GND	Power	Ground.
Y9	GND5	GND	Power	Ground.
Y10	DP10_M2C_P	HS_TXVR2_RX_CH2p	O, DIFF	PCIe Lane10 Receive pair positive.
Y11	DP10_M2C_N	HS_TXVR2_RX_CH2n	O, DIFF	PCIe Lane10 Receive pair negative.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
Y12	GND6	GND	Power	Ground.
Y13	GND7	GND	Power	Ground.
Y14	DP12_M2C_P	HS_TXVR3_RX_CH0p	O, DIFF	PCIe Lane12 Receive pair positive.
Y15	DP12_M2C_N	HS_TXVR3_RX_CH0n	O, DIFF	PCIe Lane12 Receive pair negative.
Y16	GND8	GND	Power	Ground.
Y17	GND9	GND	Power	Ground.
Y18	DP14_M2C_P	HS_TXVR3_RX_CH2p	O, DIFF	PCIe Lane14 Receive pair positive.
Y19	DP14_M2C_N	HS_TXVR3_RX_CH2n	O, DIFF	PCIe Lane14 Receive pair negative.
Y20	GND10	GND	Power	Ground.
Y21	GND11	GND	Power	Ground.
Y22	DP15_M2C_P	HS_TXVR3_RX_CH3p	O, DIFF	PCIe Lane15 Receive pair positive.
Y23	DP15_M2C_N	HS_TXVR3_RX_CH3n	O, DIFF	PCIe Lane15 Receive pair negative.
Y24	GND12	GND	Power	Ground.
Y25	GND13	GND	Power	Ground.
Y26	DP11_C2M_P	HS_TXVR2_TX_CH3p	I, DIFF	PCIe Lane11 Transmit pair positive.
Y27	DP11_C2M_N	HS_TXVR2_TX_CH3n	I, DIFF	PCIe Lane11 Transmit pair negative.
Y28	GND14	GND	Power	Ground.
Y29	GND15	GND	Power	Ground.
Y30	DP13_C2M_P	HS_TXVR3_TX_CH1p	I, DIFF	PCIe Lane13 Transmit pair positive.
Y31	DP13_C2M_N	HS_TXVR3_TX_CH1n	I, DIFF	PCIe Lane13 Transmit pair negative.
Y32	GND16	GND	Power	Ground.
Y33	GND17	GND	Power	Ground.
Y34	DP17_M2C_P	NA	NA	NC
Y35	DP17_M2C_N	NA	NA	NC
Y36	GND18	GND	Power	Ground.
Y37	GND19	GND	Power	Ground.
Y38	DP19_M2C_P	NA	NA	NC
Y39	DP19_M2C_N	NA	NA	NC
Y40	GND20	GND	Power	Ground.
Z1	HSPC_PRSNT_M2C_L	NA	O, 1K PD	Module Present Signal.
Z2	GND2	GND	Power	Ground.
Z3	GND3	GND	Power	Ground.
Z4	DP22_C2M_P	NA	NA	NC
Z5	DP22_C2M_N	NA	NA	NC
Z6	GND6	GND	Power	Ground.
Z7	GND7	GND	Power	Ground.

Pin No	FMC+ Connector Pin Name	Signal Name	Signal Type/ Termination	Description
Z8	DP20_C2M_P	NA	NA	NC
Z9	DP20_C2M_N	NA	NA	NC
Z10	GND8	GND	Power	Ground.
Z11	GND9	GND	Power	Ground.
Z12	DP11_M2C_P	HS_TXVR2_RX_CH3p	O, DIFF	PCIe Lane11 Receive pair positive.
Z13	DP11_M2C_N	HS_TXVR2_RX_CH3n	O, DIFF	PCIe Lane11 Receive pair negative.
Z14	GND10	GND	Power	Ground.
Z15	GND11	GND	Power	Ground.
Z16	DP13_M2C_P	HS_TXVR3_RX_CH1p	O, DIFF	PCIe Lane13 Receive pair positive.
Z17	DP13_M2C_N	HS_TXVR3_RX_CH1n	O, DIFF	PCIe Lane13 Receive pair negative.
Z18	GND12	GND	Power	Ground.
Z19	GND13	GND	Power	Ground.
Z20	GBTCLK5_M2C_P	NA	NA	NC
Z21	GBTCLK5_M2C_N	NA	NA	NC
Z22	GND14	GND	Power	Ground.
Z23	GND15	GND	Power	Ground.
Z24	DP10_C2M_P	HS_TXVR2_TX_CH2p	I, DIFF	PCIe Lane10 Transmit pair positive.
Z25	DP10_C2M_N	HS_TXVR2_TX_CH2n	I, DIFF	PCIe Lane10 Transmit pair negative.
Z26	GND16	GND	Power	Ground.
Z27	GND17	GND	Power	Ground.
Z28	DP12_C2M_P	HS_TXVR3_TX_CH0p	I, DIFF	PCIe Lane12 Transmit pair positive.
Z29	DP12_C2M_N	HS_TXVR3_TX_CH0n	I, DIFF	PCIe Lane12 Transmit pair negative.
Z30	GND18	GND	Power	Ground.
Z31	GND19	GND	Power	Ground.
Z32	DP16_M2C_P	NA	NA	NC
Z33	DP16_M2C_N	NA	NA	NC
Z34	GND20	GND	Power	Ground.
Z35	GND21	GND	Power	Ground.
Z36	DP18_M2C_P	NA	NA	NC
Z37	DP18_M2C_N	NA	NA	NC
Z38	GND22	GND	Power	Ground.
Z39	GND23	GND	Power	Ground.
Z40	3P3V	VCC_3V3_FMC+	I, 3.3V Power	Supply Voltage.

2.2.2 PCIe x16 Connector

The FMC+ PCIe x16 module support one PCIe x16 interface through PCIe Connector. Sixteen high speed transceiver pairs from FMC+ connector is directly connected to PCIe x16 Connector (J1) for PCIe interface. This PCIe connector physically located at the top of the board as shown below.

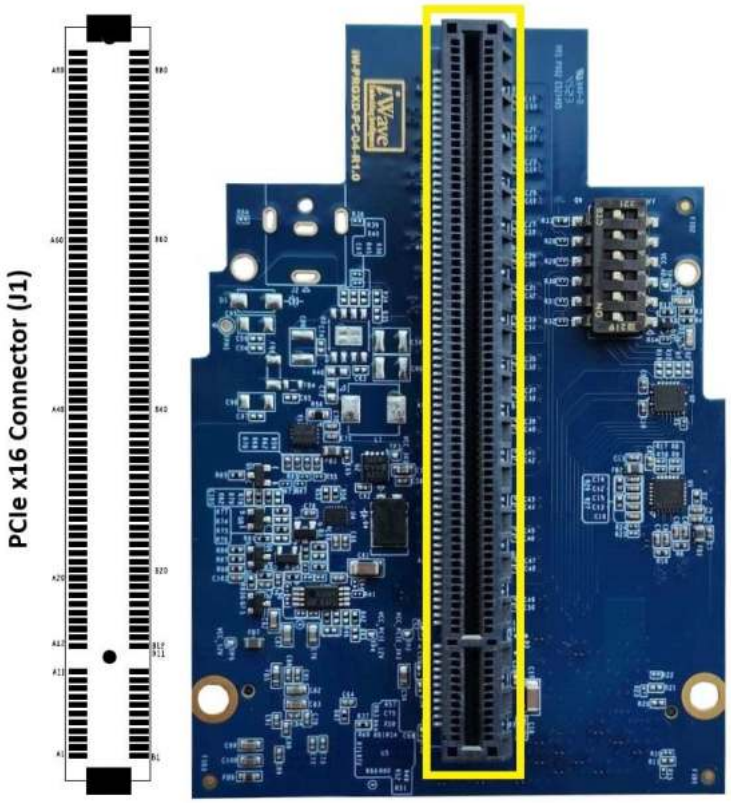

Figure 4: PCIe x 16 Connector

This FMC+ module supports both PCIe Root Port and PCIe Endpoint Synchronous Mode of operation. To select between PCIe Root port mode and Endpoint mode, the PCIe Mode Select Switch (SW1.1) is utilized. PCIe Root port mode is selected by keeping SW1.1 in the OFF state. In this condition, the on-module clock oscillator will be the source of the clock for the PCIe X16 connector and the GBTCLK[0:3] pins of FMC+ Connector through Clock Buffer.

Endpoint mode of operation is selected by keeping SW1.1 in the ON state. In this condition, the PCIe reference clock will be sourced from the Host PC via the PCIe X16 connector to the GBTCLK[0:3] pins of FMC+ Connector through Clock Buffer. For Endpoint, connect cable to host PC as shown in Figure 16.

To support Root Port and End point configuration, make the switch (SW1) positions as follows:

Table 4: Root Port and End point switch position

PCIe SELECT SWITCH							
SW1.1	SW1.2	SW1.3	SW1.4	SW1.5	SW1.6	Mode	Switch Position Image
0	0	0	0	0	1	Root Port	
1	1	1	1	1	0	End Point	

Figure 5: End Point through cable

Warning: Before Powering ON the board, make sure that VCC_12V and VCC_3V3 voltages should be disabled for Endpoint configuration.

Table 5: PCIe x16 Connector Pin Assignment

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
A1	PRSNT1#	NA	NA	NA	NA	Hot-Plug presence detect Default grounded.
A2	+12V	VCC_PCIE_12V[1]	NA	NA	12V Power	12V Supply Voltage.
A3	+12V	VCC_PCIE_12V[1]	NA	NA	12V Power	12V Supply Voltage.
A4	GND	GND	NA	NA	Power	Ground.
A5	JTAG_TCK	NA	NA	NA	NA	NC.
A6	JTAG_TDI	NA	NA	NA	NA	NC.
A7	JTAG_TDO	NA	NA	NA	NA	NC.
A8	JTAG_TMS	NA	NA	NA	NA	NC.
A9	+3_3V	VCC_PCIE_3V3[1]	NA	NA	3.3V Power	3.3V Supply Voltage.
A10	+3_3V	VCC_PCIE_3V3[1]	NA	NA	3.3V Power	3.3V Supply Voltage.
A11	PERST#	PCIE_RESET	G16	LA12_N	IO, 3.3V CMOS	PCIe Reset. *Note: This reset signal is input to the module for Root Port application and output from the module for Endpoint application.*
A12	GND	GND	NA	NA	Power	Ground.
A13	REFCLK+	PCIe_REFCLKP	NA	NA	IO, DIFF	100MHz PCIe Reference Clock positive. *Note: This 100MHz clock is Input to PCIe connector for Root Port application from On-Module clock generator and output from PCIe connector for Endpoint application.*
A14	REFCLK-	PCIe_REFCLKN	NA	NA	IO, DIFF	100MHz PCIe Reference Clock negative. *Note: This 100MHz clock is Input to PCIe connector for Root Port application from On-Module clock generator and output from PCIe connector for Endpoint application.*
A15	GND	GND	NA	NA	Power	Ground.
A16	PER0P	HS_TXVR0_RX_CH0P	C6	DP0_M2C_P	O, DIFF	PCIe Lane0 Receive pair positive.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
A17	PER0N	HS_TXVR0_RX_CH0N	C7	DP0_M2C_N	O, DIFF	PCIe Lane0 Receive pair negative.
A18	GND	GND	NA	NA	Power	Ground.
A19	RSVD4	NA	NA	NA	NA	NC.
A20	GND	GND	NA	NA	Power	Ground.
A21	PER1P	HS_TXVR0_RX_CH1P	A2	DP1_M2C_P	O, DIFF	PCIe Lane1 Receive pair positive.
A22	PER1N	HS_TXVR0_RX_CH1N	A3	DP1_M2C_N	O, DIFF	PCIe Lane1 Receive pair negative
A23	GND	GND	NA	NA	Power	Ground.
A24	GND	GND	NA	NA	Power	Ground.
A25	PER2P	HS_TXVR0_RX_CH2P	A6	DP2_M2C_P	O, DIFF	PCIe Lane2 Receive pair positive.
A26	PER2N	HS_TXVR0_RX_CH2N	A7	DP2_M2C_N	O, DIFF	PCIe Lane2 Receive pair negative.
A27	GND	GND	NA	NA	Power	Ground.
A28	GND	GND	NA	NA	Power	Ground.
A29	PER3P	HS_TXVR0_RX_CH3P	A10	DP3_M2C_P	O, DIFF	PCIe Lane3 Receive pair positive.
A30	PER3N	HS_TXVR0_RX_CH3N	A11	DP3_M2C_N	O, DIFF	PCIe Lane3 Receive pair negative.
A31	GND	GND	NA	NA	Power	Ground.
A32	RSVD5	NA	NA	NA	NA	NC.
A33	RSVD6	NA	NA	NA	NA	NC.
A34	GND	GND	NA	NA	Power	Ground.
A35	PER4P	HS_TXVR1_RX_CH0P	A14	DP4_M2C_P	O, DIFF	PCIe Lane4 Receive pair positive.
A36	PER4N	HS_TXVR1_RX_CH0N	A15	DP4_M2C_N	O, DIFF	PCIe Lane4 Receive pair negative.
A37	GND	GND	NA	NA	Power	Ground.
A38	GND	GND	NA	NA	Power	Ground.
A39	PER5P	HS_TXVR1_RX_CH1P	A18	DP5_M2C_P	O, DIFF	PCIe Lane5 Receive pair positive.
A40	PER5P	HS_TXVR1_RX_CH1N	A19	DP5_M2C_N	O, DIFF	PCIe Lane5 Receive pair negative.
A41	GND	GND	NA	NA	Power	Ground.
A42	GND	GND	NA	NA	Power	Ground.
A43	PER6P	HS_TXVR1_RX_CH2P	B16	DP6_M2C_P	O, DIFF	PCIe Lane6 Receive pair positive.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
A44	PER6N	HS_TXVR1_RX_CH2N	B17	DP6_M2C_N	O, DIFF	PCIe Lane6 Receive pair negative.
A45	GND	GND	NA	NA	Power	Ground.
A46	GND	GND	NA	NA	Power	Ground.
A47	PER7P	HS_TXVR1_RX_CH3P	B12	DP7_M2C_P	O, DIFF	PCIe Lane7 Receive pair positive.
A48	PER7N	HS_TXVR1_RX_CH3N	B13	DP7_M2C_N	O, DIFF	PCIe Lane7 Receive pair negative.
A49	GND	GND	NA	NA	Power	Ground.
A50	RSVD7	NA	NA	NA	NA	NC
A51	GND	GND	NA	NA	Power	Ground.
A52	PER8P	HS_TXVR2_RX_CH0P	B8	DP8_M2C_P	O, DIFF	PCIe Lane8 Receive pair positive.
A53	PER8N	HS_TXVR2_RX_CH0N	B9	DP8_M2C_N	O, DIFF	PCIe Lane8 Receive pair negative.
A54	GND	GND	NA	NA	Power	Ground.
A55	GND	GND	NA	NA	Power	Ground.
A56	PER9P	HS_TXVR2_RX_CH1P	B4	DP9_M2C_P	O, DIFF	PCIe Lane9 Receive pair positive.
A57	PER9N	HS_TXVR2_RX_CH1N	B5	DP9_M2C_N	O, DIFF	PCIe Lane9 Receive pair negative.
A58	GND	GND	NA	NA	Power	Ground.
A59	GND	GND	NA	NA	Power	Ground.
A60	PER10P	HS_TXVR2_RX_CH2P	Y10	DP10_M2C_P	O, DIFF	PCIe Lane10 Receive pair positive.
A61	PER10N	HS_TXVR2_RX_CH2N	Y11	DP10_M2C_N	O, DIFF	PCIe Lane10 Receive pair negative.
A62	GND	GND	NA	NA	Power	Ground.
A63	GND	GND	NA	NA	Power	Ground.
A64	PER11P	HS_TXVR2_RX_CH3P	Z12	DP11_M2C_P	O, DIFF	PCIe Lane11 Receive pair positive.
A65	PER11N	HS_TXVR2_RX_CH3N	Z13	DP11_M2C_N	O, DIFF	PCIe Lane11 Receive pair negative.
A66	GND	GND	NA	NA	Power	Ground.
A67	GND	GND	NA	NA	Power	Ground.
A68	PER12P	HS_TXVR3_RX_CH0P	Y14	DP12_M2C_P	O, DIFF	PCIe Lane12 Receive pair positive.
A69	PER12N	HS_TXVR3_RX_CH0N	Y15	DP12_M2C_N	O, DIFF	PCIe Lane12 Receive pair negative.
A70	GND	GND	NA	NA	Power	Ground.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
A71	GND	GND	NA	NA	Power	Ground.
A72	PER13P	HS_TXVR3_RX_CH1P	Z16	DP13_M2C_P	O, DIFF	PCIe Lane13 Receive pair positive.
A73	PER13N	HS_TXVR3_RX_CH1N	Z17	DP13_M2C_N	O, DIFF	PCIe Lane13 Receive pair negative.
A74	GND	GND	NA	NA	Power	Ground.
A75	GND	GND	NA	NA	Power	Ground.
A76	PER14P	HS_TXVR3_RX_CH2P	Y18	DP14_M2C_P	O, DIFF	PCIe Lane14 Receive pair positive.
A77	PER14N	HS_TXVR3_RX_CH2N	Y19	DP14_M2C_N	O, DIFF	PCIe Lane14 Receive pair negative.
A78	GND	GND	NA	NA	Power	Ground.
A79	GND	GND	NA	NA	Power	Ground.
A80	PER15P	HS_TXVR3_RX_CH3P	Y22	DP15_M2C_P	O, DIFF	PCIe Lane15 Receive pair positive.
A81	PER15N	HS_TXVR3_RX_CH3N	Y23	DP15_M2C_N	O, DIFF	PCIe Lane15 Receive pair negative.
A82	GND	GND	NA	NA	Power	Ground.
B1	+12V	VCC_PCIE_12V[1]	NA	NA	12V Power	12V Supply Voltage.
B2	+12V	VCC_PCIE_12V[1]	NA	NA	12V Power	12V Supply Voltage.
B3	+12V	VCC_PCIE_12V[1]	NA	NA	12V Power	12V Supply Voltage.
B4	GND	GND	NA	NA	Power	Ground.
B5	SMCLK	NA	NA	NA	NA	NC.
B6	SMDAT	NA	NA	NA	NA	NC.
B7	GND	GND	NA	NA	Power	Ground.
B8	+3_3V	VCC_PCIE_3V3[1]	NA	NA	3.3V Power	3.3V Supply Voltage.
B9	JTAG1	NA	NA	NA	NA	NC.
B10	+3_3VAUX	NA	NA	NA	NA	NC
B11	WAKE_N	NA	NA	NA	NA	NC
B12	RSVD1	NA	NA	NA	NA	NC.
B13	GND	GND	NA	NA	Power	Ground.
B14	PET0P	HS_TXVR0_TX_CH0P	C2	DP0_C2M_P	I, DIFF	PCIe Lane0 Transmit pair positive.
B15	PET0N	HS_TXVR0_TX_CH0N	C3	DP0_C2M_N	I, DIFF	PCIe Lane0 Transmit pair negative.
B16	GND	GND	NA	NA	Power	Ground.
B17	PRSNT2#_1	NA	NA	NA	NA	NC
B18	GND	GND	NA	NA	Power	Ground.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
B19	PET1P	HS_TXVR0_TX_CH1P	A22	DP1_C2M_P	I, DIFF	PCIe Lane1 Transmit pair positive.
B20	PET1N	HS_TXVR0_TX_CH1N	A23	DP1_C2M_N	I, DIFF	PCIe Lane1 Transmit pair negative
B21	GND	GND	NA	NA	Power	Ground.
B22	GND	GND	NA	NA	Power	Ground.
B23	PET2P	HS_TXVR0_TX_CH2P	A26	DP2_C2M_P	I, DIFF	PCIe Lane2 Transmit pair positive.
B24	PET2N	HS_TXVR0_TX_CH2N	A27	DP2_C2M_N	I, DIFF	PCIe Lane2 Transmit pair negative
B25	GND	GND	NA	NA	Power	Ground.
B26	GND	GND	NA	NA	Power	Ground.
B27	PET3P	HS_TXVR0_TX_CH3P	A30	DP3_C2M_P	I, DIFF	PCIe Lane3 Transmit pair positive.
B28	PET3N	HS_TXVR0_TX_CH3N	A31	DP3_C2M_N	I, DIFF	PCIe Lane3 Transmit pair negative
B29	GND	GND	NA	NA	Power	Ground.
B30	RSVD2	NA	NA	NA	NA	NC.
B31	PRSNT2#_2	NA	NA	NA	NA	NC
B32	GND	GND	NA	NA	Power	Ground.
B33	PET4P	HS_TXVR1_TX_CH0P	A34	DP4_C2M_P	I, DIFF	PCIe Lane4 Transmit pair positive.
B34	PET4N	HS_TXVR1_TX_CH0N	A35	DP4_C2M_N	I, DIFF	PCIe Lane4 Transmit pair negative
B35	GND	GND	NA	NA	Power	Ground.
B36	GND	GND	NA	NA	Power	Ground.
B37	PET5P	HS_TXVR1_TX_CH1P	A38	DP5_C2M_P	I, DIFF	PCIe Lane5 Transmit pair positive.
B38	PET5N	HS_TXVR1_TX_CH1N	A39	DP5_C2M_N	I, DIFF	PCIe Lane5 Transmit pair negative
B39	GND	GND	NA	NA	Power	Ground.
B40	GND	GND	NA	NA	Power	Ground.
B41	PET6P	HS_TXVR1_TX_CH2P	B36	DP6_C2M_P	I, DIFF	PCIe Lane6 Transmit pair positive.
B42	PET6N	HS_TXVR1_TX_CH2N	B37	DP6_C2M_N	I, DIFF	PCIe Lane6 Transmit pair negative
B43	GND	GND	NA	NA	Power	Ground.
B44	GND	GND	NA	NA	Power	Ground.
B45	PET7P	HS_TXVR1_TX_CH3P	B32	DP7_C2M_P	I, DIFF	PCIe Lane7 Transmit pair positive.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
B46	PET7N	HS_TXVR1_TX_CH3N	B33	DP7_C2M_N	I, DIFF	PCIe Lane7 Transmit pair negative
B47	GND	GND	NA	NA	Power	Ground.
B48	PRSNT2#_3	NA	NA	NA	NA	NC
B49	GND	GND	NA	NA	Power	Ground.
B50	PET8P	HS_TXVR2_TX_CH0P	B28	DP8_C2M_P	I, DIFF	PCIe Lane8 Transmit pair positive.
B51	PET8N	HS_TXVR2_TX_CH0N	B29	DP8_C2M_N	I, DIFF	PCIe Lane8 Transmit pair negative
B52	GND	GND	NA	NA	Power	Ground.
B53	GND	GND	NA	NA	Power	Ground.
B54	PET9P	HS_TXVR2_TX_CH1P	B24	DP9_C2M_P	I, DIFF	PCIe Lane9 Transmit pair positive.
B55	PET9N	HS_TXVR2_TX_CH1N	B25	DP9_C2M_N	I, DIFF	PCIe Lane9 Transmit pair negative
B56	GND	GND	NA	NA	Power	Ground.
B57	GND	GND	NA	NA	Power	Ground.
B58	PET10P	HS_TXVR2_TX_CH2P	Z24	DP10_C2M_P	I, DIFF	PCIe Lane10 Transmit pair positive.
B59	PET10N	HS_TXVR2_TX_CH2N	Z25	DP10_C2M_N	I, DIFF	PCIe Lane10 Transmit pair negative
B60	GND	GND	NA	NA	Power	Ground.
B61	GND	GND	NA	NA	Power	Ground.
B62	PET11P	HS_TXVR2_TX_CH3P	Y26	DP11_C2M_P	I, DIFF	PCIe Lane11 Transmit pair positive.
B63	PET11N	HS_TXVR2_TX_CH3N	Y27	DP11_C2M_N	I, DIFF	PCIe Lane11 Transmit pair negative
B64	GND	GND	NA	NA	Power	Ground.
B65	GND	GND	NA	NA	Power	Ground.
B66	PET12P	HS_TXVR3_TX_CH0P	Z28	DP12_C2M_P	I, DIFF	PCIe Lane12 Transmit pair positive.
B67	PET12N	HS_TXVR3_TX_CH0N	Z29	DP12_C2M_N	I, DIFF	PCIe Lane12 Transmit pair negative
B68	GND	GND	NA	NA	Power	Ground.
B69	GND	GND	NA	NA	Power	Ground.
B70	PET13P	HS_TXVR3_TX_CH1P	Y30	DP13_C2M_P	I, DIFF	PCIe Lane13 Transmit pair positive.
B71	PET13N	HS_TXVR3_TX_CH1N	Y31	DP13_C2M_N	I, DIFF	PCIe Lane13 Transmit pair negative
B72	GND	GND	NA	NA	Power	Ground.

PCIe Connector Pin No	PCIe Connector Pin Name	Signal Name	FMC+ Connector Pin No	FMC+ Connector Pin Name	Signal Type/ Termination	Description
B73	GND	GND	NA	NA	Power	Ground.
B74	PET14P	HS_TXVR3_TX_CH2P	M18	DP14_C2M_P	I, DIFF	PCIe Lane14 Transmit pair positive.
B75	PET14N	HS_TXVR3_TX_CH2N	M19	DP14_C2M_N	I, DIFF	PCIe Lane14 Transmit pair negative
B76	GND	GND	NA	NA	Power	Ground.
B77	GND	GND	NA	NA	Power	Ground.
B78	PET15P	HS_TXVR3_TX_CH3P	M22	DP15_C2M_P	I, DIFF	PCIe Lane15 Transmit pair positive.
B79	PET15N	HS_TXVR3_TX_CH3N	M23	DP15_C2M_N	I, DIFF	PCIe Lane15 Transmit pair negative
B80	GND	GND	NA	NA	Power	Ground.
B81	PRSNT2#_4	NA	NA	NA	NA	NC
B82	RSVD3	NA	NA	NA	NA	NC.

[1] *VCC_PCIE_12V and VCC_PCIE_3V3 voltages are the input to PCIe x16 connector for Root port application and output from PCIe x16 connector for Endpoint application*

2.2.3 Clock Oscillator

This FMC+ module supports both PCIe Root port and PCIe Endpoint Mode of operation. For Root port application 100MHz clock is generated on FMC+ module itself through dual output Clock Oscillator “DSC557-0344FL1T”. This Clock Oscillator outputs are connected to PCIe x16 Connector (pins A13 & A14) and FMC+ Connector through Clock buffer “SI53342-B-GM”. The output of Clock buffer consists of AC Caps of value 0.01uF. The FMC+ PCIex16 module supports below mentioned clock flow in Root port configuration.

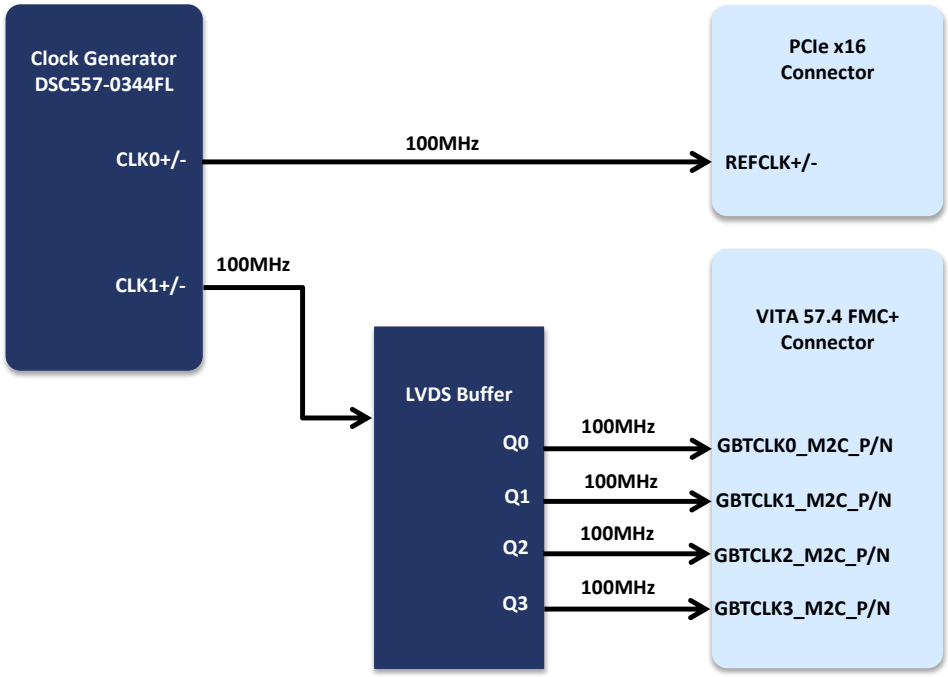

Figure 6: Clock for Root Port Application

For Endpoint application, 100MHz clock is from PCIe Host through PCIe x16 connector to FMC+ PCIex16 module. This input clock from host is connected to FMC+ reference clocks using buffer. The FMC+ module supports below mentioned clock flow in Endpoint configuration.

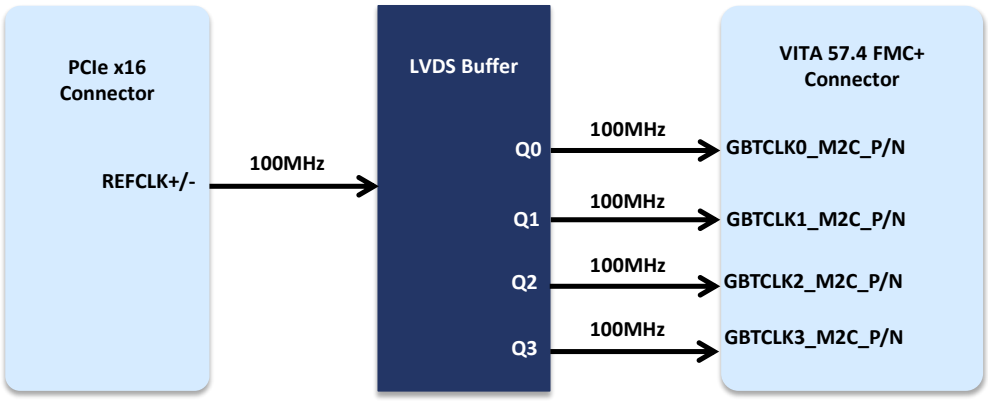

Figure 7: Clock for Endpoint Application

2.2.4 EEPROM

The FMC+ PCIe x16 Module supports 32Kb EEPROM “M24C32-RDW6TP” to store FMC+ FRU details. This EEPROM is programmed through SCL & SDA pins of the FMC+ connector. Also, its I2C address setting pins A0 & A1 is connected to FMC+ connectors pin GA0 & GA1 respectively and A2 is fixed to ‘1’ in FMC+ Module.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the FMC+ PCIe x16 Module technical specification with Electrical and Environmental characteristics.

3.1 Power Input Requirement

By default, The FMC+ PCIe x16 Module is designed to work with power from FMC+ Connector. The below table provides the Power Input Requirement of FMC+ PCIe x16 Module.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)
1	VCC_FMC_ADJ	0	VADJ[1]	3.3
2	VCC_3V3	3.15	3.3	3.45
3	3P3VAUX	3.15	3.3	3.45
4	VCC_12V	11.75	12	12.25

[1] *VADJ voltage will vary based on the supported IO power*

Important Note: While using PCIe as Endpoint and connected to external PCIe Host (PC), don't provide VCC_12V & VCC_3V3 to PCIe Connector.

The PCIe x 16 Module also has option to connect external power supply through Power Jack (J2) and by default not populated. This connector is physically placed at top of the board as shown below.

Figure 8: Power IN Jack (optional)

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of FMC+ PCIe x16 Module.

Table 7: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.2.2 RoHS Compliance

The FMC+ PCIe x16 Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

The FMC+ PCIe x16 Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 FMC+ PCIe x16 Module Mechanical Dimensions

The FMC+ PCIe x16 Module PCB form factor is 98.5mm X 69mm and Board mechanical dimension is shown below.

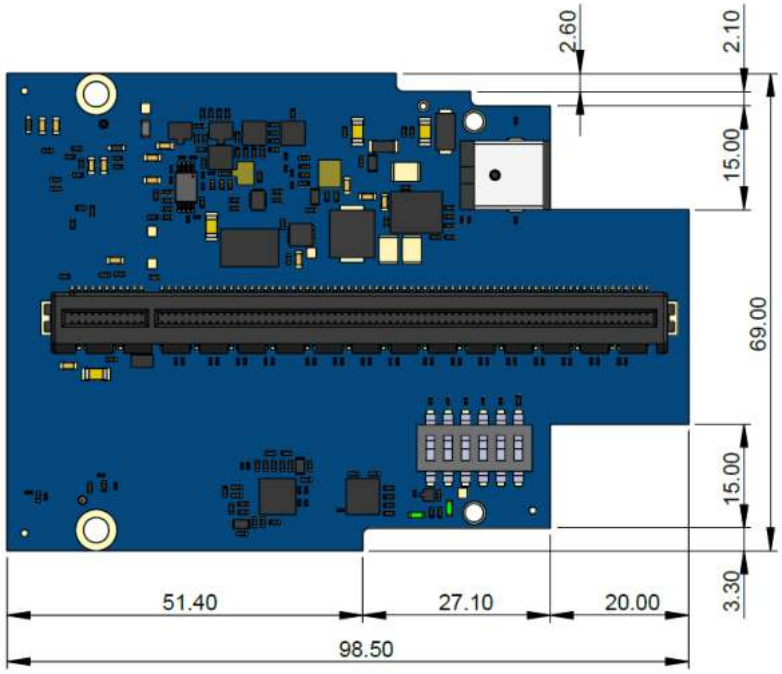

Figure 9: FMC+ PCIe x16 Module Mechanical dimension – Top View

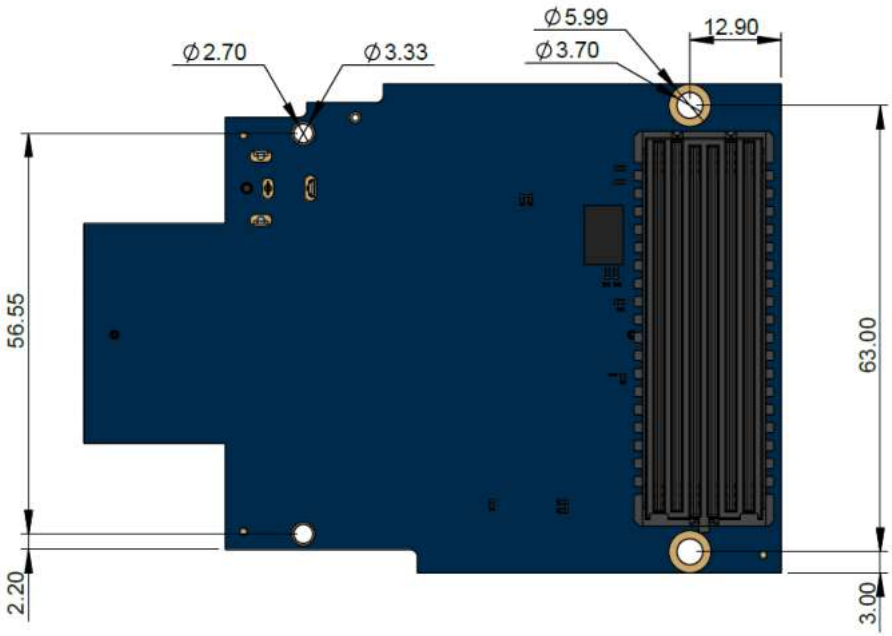

Figure 10:FMC+ PCIe x16 Module Mechanical dimension – Bottom View

The FMC+ PCIe x16 Module PCB thickness is 1.6mm±0.1mm, top side maximum height component is PCIex16 Connector (11.25mm) and bottom side maximum height component is FMC+ Connector (6.223mm). Please refer the below figure for height details of the FMC+ PCIe x16 Module.

Figure 11: FMC+ PCIe x16 Module Mechanical dimension – Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for FMC+ PCIe x16 Module.

Table 8: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-FMC-PCIe16-I1	PCIe Gen4x16 FMC+ Module	Industrial
iW-C40-PCIe16-C1	PCIe x16 Gen3 Goldfinger to Goldfinger Cross cable (40cm length) for PCIe Endpoint testing.	Commercial
iW-C40-PCIe16-C2	PCIe x16 Gen4 Goldfinger to Goldfinger Cross cable (40cm length) for PCIe Endpoint testing.	Commercial

5. APPENDIX

5.1 Root Port Connection

Refer Table 4 in the PCIe x16 Connector section and change the Config Switch (SW1) settings to Rootport mode and FMC+ Module in the development kit, insert the PCIe NVMe module as shown below.

Figure 12: PCIe Root Port Connection

5.2 Endpoint Connection to Host PC

Refer Table 4 in the PCIe x16 Connector section and change the Config Switch (SW1) settings to End Point mode

1. Insert the FMC+ PCIe Gen4/Gen3/Gen2/Gen1 x16 Module in iWave's Development kit as shown below.

Figure 13: Inserting FMC+ Module in Development Kit

2. Insert the PCIe x16 Cable to the PCIe x16 connector in the FMC+ Module as shown below.

Figure 14: PCIe x16 Cable insertion in FMC+ Module

3. Insert the other end (TX-RX Swapped end) of the x16 cable to the Host PC's PCIe Slot as shown below.

Figure 15: TX-RX Swapped End

Figure 16: Endpoint Setup

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