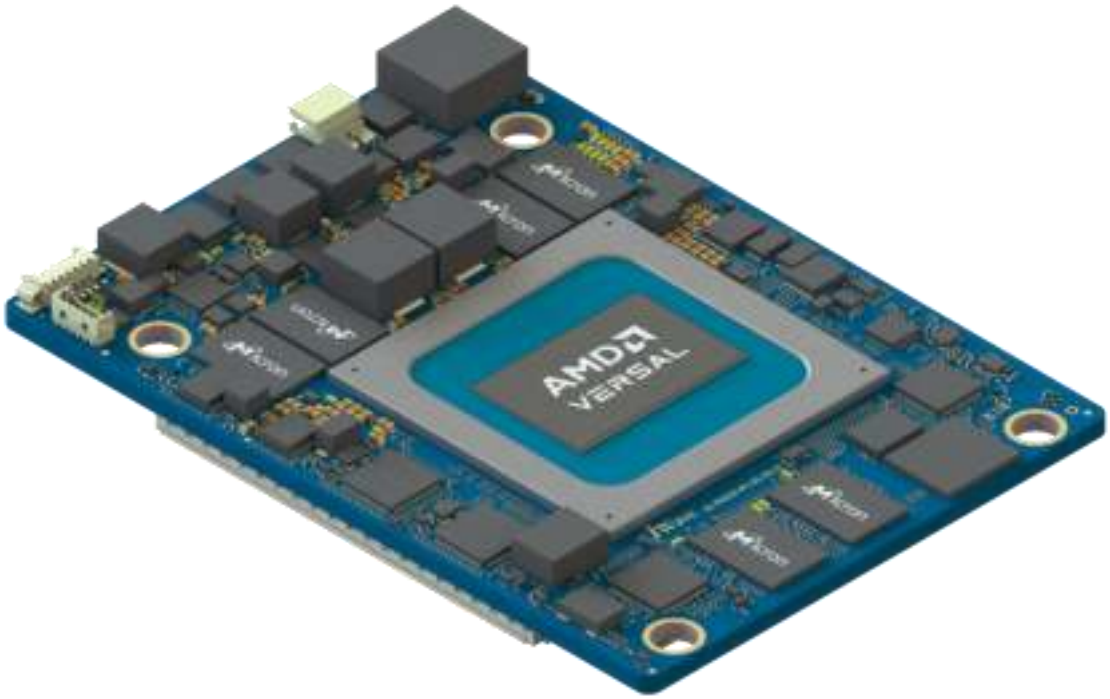
iG-RainboW-G63M

Versal Premium SOM

Datasheet



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Document Revision History:

Document Number		iG-PRIDZ-UM-01-R1.0-REL0.1-Datasheet
Release	**Date**	**Description**
0.1	06th MAR 2025	Initial Draft Version

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1. INTRODUCTION

1.1 Purpose

This document is the datasheet for the Versal Premium System on Module based on the AMD Versa premium series SoC (VP1552/VP1502/VP1402/VP1202/VP1102). This Guide provides detailed information on the overall design and usage of the Versal premium on Module from a Hardware Systems perspective.

1.2 SOM Overview

Versal Premium SOM has a form factor of 82mm x 115 mm and provides the functional requirements for an embedded application. Three High-Speed, Receptacle, Center Strip Contact Connector provides the carrier board interface to carry all the I/O signals to and from the Versal premium SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
B2B	Board To Board
CAN	Controller Area Network
CPU	Central Processing Unit
LPDDR4	Low Power Double Data Rate fourth-generation
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock

Acronyms	Abbreviations
SD	Secure Digital
SDIO	Secure Digital Input Output
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On the Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminology description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/Output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

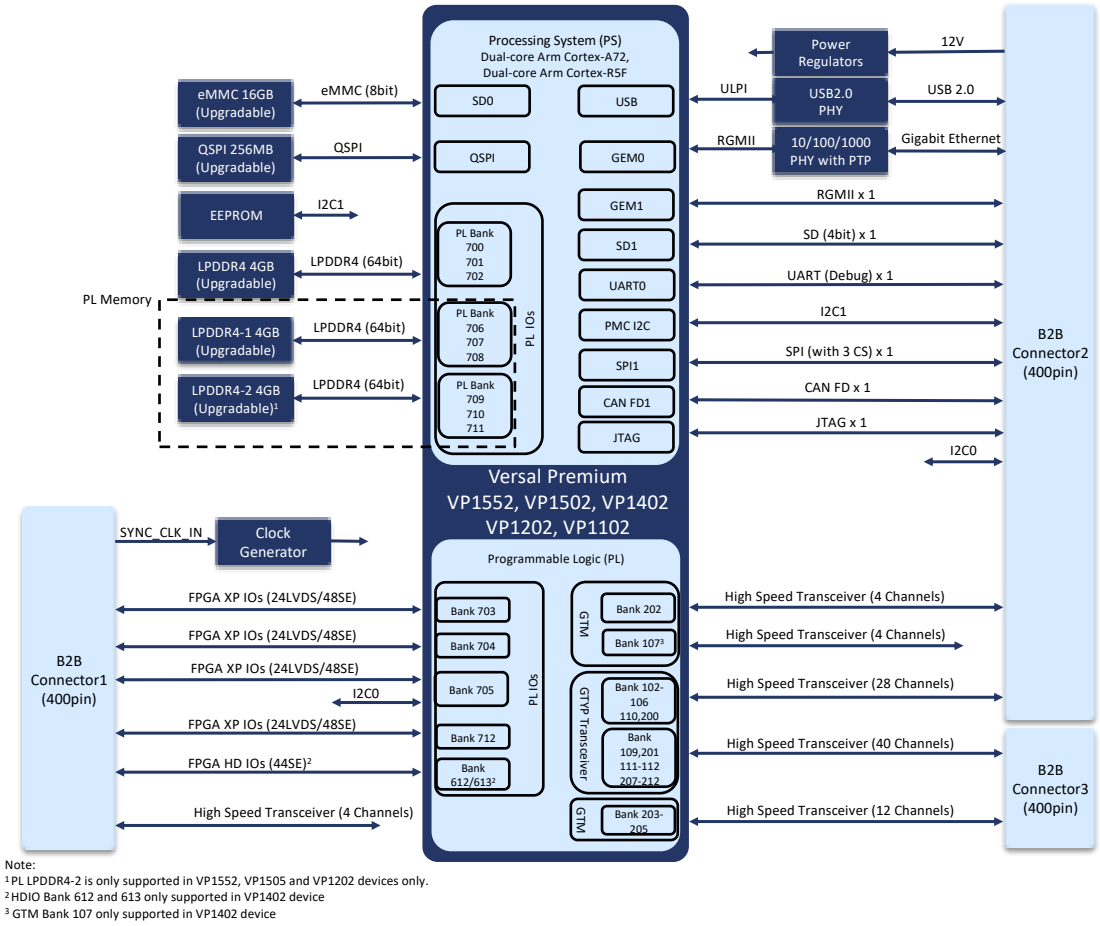
1.5 References

- Versal Adaptive SoC Technical reference manual
- Versal Premium Device data sheet

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Versal Premium SOM features and Hardware architecture with high level block diagram.

2.1 Block Diagram



Note:
[1] PL LPDDR4-2 is only supported in VP1552, VP1505 and VP1202 devices only.
[2] HDIO Bank 612 and 613 only supported in VP1402 device
[3] GTM Bank 107 only supported in VP1402 device

Figure 1: Block Diagram of Versal premium SOM

2.2 Versal Premium SOM features.

The Versal Premium SOM supports the following features.

SoC

- Versal Premium SOC with VSVA2785 package.
- Compatible with VP1552, VP1502, VP1402 VP1202, VP1102 devices.
- Processing System with integrated Dual-core Arm Cortex-A72 Application processor (up to 1.7GHz), Dual-core Arm Cortex-R5 Real Time Processor (up to 800MHz) and programming logic with up to 3.8M Logic cells.

Memory Interfaces

- 64bit 4GB LPDDR4 for PS (Expandable)
- Dual 64bit 4GB LPDDR4 for PL (Expandable)[1]
- 16GB eMMC Flash (Expandable)
- 256MB QSPI Flash

PMIC

- Renesas/Dialog's DA9062 PMIC with RTC

Board-to-Board Interfaces

From PS Block

- USB2.0 through on-SOM USB2.0 PHY Transceiver
- GEM0 through on-SOM Gigabit Ethernet PHY
- RGMII x1(GEM1)
- SD x1(4-bit)
- UART(Debug) x1
- I2C x2
- SPI x1
- CAN FD x1
- JTAG x1

From PL Block

- 24 LVDS/48 SE signals from XPIO Bank 703
- 24 LVDS/48 SE signals from XPIO Bank 704
- 24 LVDS/48 SE signals from XPIO Bank 705
- 24 LVDS/48 SE signals from XPIO Bank 712
- 44 SE IO from HDIO Bank 612 and Bank 613[2]

- GTM Transceiver channels (up to 112 Gbps PAM4) x16[3]
- GTYP Transceiver Channels (up to 32.75Gbps) x68[3]

Power Supply

- 12V input through Board-to-Board connector 2

Component's Temperature Support

- -40°C to +85°C

Environment Specification

- RoHS and REACH Compliance

Form Factor

- 82mm x 115mm (BRYN Form Factor)

[1] VP1402 and VP1102 Supports only one 4GB LPDDR4 for PL.

[2] HDIO Bank 612 and 613 is only supported in VP1402 Devices.

[3] Number of GTM and GTYP transceiver channels varies in compatible devices, refer Bank Migration Info in Appendix.

Important Note: Bank name and bank number mentioned in this document is with respect to VP1552 Devices.

2.3 Versal Adaptive SoC

AMD Versal™ adaptive SoCs combine Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application The Versal portfolio is the first to combine software programmability and domain-specific hardware acceleration with the adaptability necessary to meet today's rapid pace of innovation. The portfolio includes six series of devices uniquely architected to deliver scalability and AI inference capabilities for a host of applications across different markets—from cloud—to networking—to wireless communications—to edge computing and endpoints. The Versal architecture combines different engine types with a wealth of connectivity and communication capability and a programmable network on chip (NoC) to enable seamless memory-mapped access to the full height and width of the device.

The Versal Premium series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data center, test & measurement, and other applications. The Versal Premium series include 112G PAM4 transceivers and integrated blocks for 600G Ethernet, 600G Interlaken, PCI Express® Gen5, and high-speed cryptography.

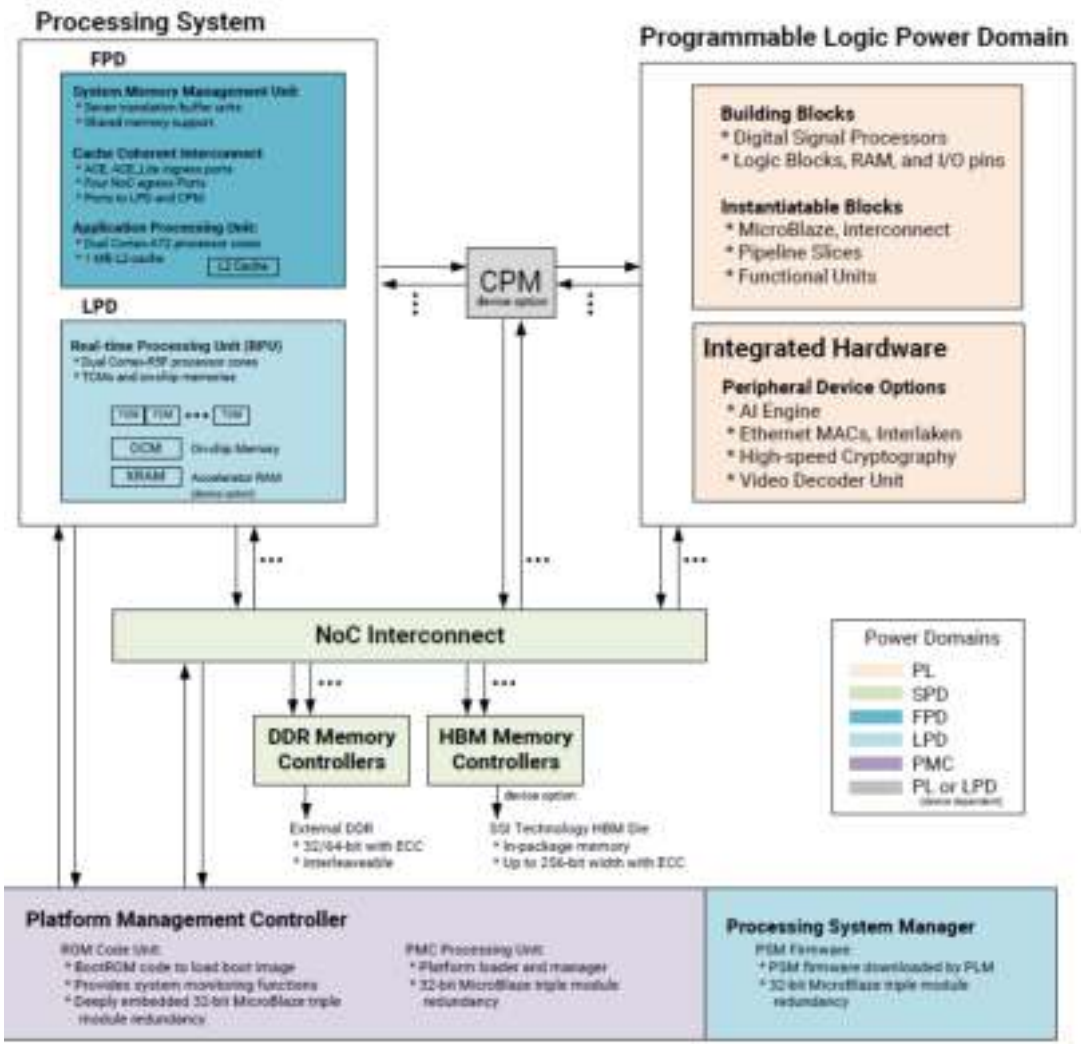


Figure 2: Versal Premium Simplified Block Diagram

The Versal Premium SOM is compatible to VP1102, VP1202, VP1402, VP1502, VP1552, VP1702, VP1802 SoC of VSVA2785 package devices and feature comparison between these devices are shown below.

	VP1102	VP1202	VP1402	VP1502	VP1552
APU	Dual-core Arm Cortex-A72; 48KB/32KB L1 Cache w/ parity and ECC; 1MB L2 Cache w/ ECC				
RPU	Dual-core Arm Cortex-R5F; 32KB/32KB L1 Cache, and TCM w/ECC				
Connectivity	Ethernet (x2); UART (x1); CAN-FD (x1); USB 2.0 (x1); SPI (x1); I2C (x2)				
System Logic Cells	15,74,720	19,69,240	22,33,280	37,63,480	38,36,840
CLB Flip-Flops	14,39,744	18,00,448	20,41,856	34,40,896	35,07,968
LUTs	7,19,872	9,00,224	10,20,928	17,20,448	17,53,984
Distributed RAM (Mb)	22	27	31	53	54
Block RAM Blocks	1,405	1,341	1,981	2,541	2,541
Block RAM (Mb)	49	47	70	89	89
UltraRAM Blocks	453	677	645	1,301	1,301
UltraRAM (Mb)	127	190	181	366	366
DSP Engines	1,904	3,984	2,672	7,440	7,392
NoC Master / Slave Ports	30	28	42	52	52
PCIe w/DMA & CCIX (CPM5)	–	Supported	–	Supported	Supported
PCIe (PLPCIE5)	Supported	Supported	Supported	Supported	Supported
Multirate Ethernet MAC	6	2	6	4	4
600G Ethernet MAC	7	1	11	3	1
600G Interlaken	–	–	–	1	–
400G HSC Engine	3	1	4	2	2
XPIO	144	192	144	192	192
HDIO	–	–	44	–	–
GTYP Transceivers (32.75Gb/s)	8	28	8	28	68
GTM Transceivers(2) 58Gb/s (112Gb/s)	64(32)	20(10)	80(40)	56(38)	16(8)

Figure 3: Versal Premium SoC Devices Comparison

The Versal Premium, Processing System (PS) supports a total 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for peripheral interfaces. These 78 MIO pins are divided as Platform Management Controller (PMC) and Low Power Domain (LPD). The PMC supports total 52 MIO with BANK 500 & 501 and each bank includes 26 device pins. The LPD supports a 26 MIO with Bank 502 and this bank also includes a 26 MIO pins. 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in Versal to route IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Versal premium PS peripheral pin mapping options between MIO & EMIO is shown below.

Table 3: MIO and EMIO Pin Mapping Table

Peripheral Interface	Controller Location	PMC MIO	LPD MIO	EMIO	Notes
CAN_FD 0,1	LPD	Yes	Yes	Yes	-
GEM 0,1	LPD	Yes	Yes	-	RGMII
		-	-	Yes	GMII/MII, TSU, and external FIFO
		Yes	Yes	Yes	MDIO
LPD DMA	LPD	-	-	YES	Flow control
PMC_GPIO	PMC	Yes	-	-	Bank 0,1 (no Bank 2)
		-	-	Yes	BANK 3,4
LPD_GPIO	LPD	-	Yes	-	LPD GPIO BANK 0 (no Bank 1,2)

Peripheral Interface	Controller Location	PMC MIO	LPD MIO	EMIO	Notes
		-	-	Yes	LPD GPIO Bank 3
LPD_I2C 0,1	LPD	Yes	Yes	Yes	-
PMC_I2C	PMC	Yes	-	Yes	-
Octal SPI	PMC	Yes	-		-
SD/eMMC 0, 1	PMC	Yes	-	Yes	-
Select MAP	PMC	Yes	-		-
SPI 0, 1	LPD	Yes	Yes	Yes	-
Quad SPI	PMC	Yes			-
UART 0, 1	LPD	Yes	Yes	Yes	MIO only includes RX, TX, CTS, and RTS
USB_2.0	LPD	Yes			ULPI
LPD_SWDT	LPD	Yes	Yes	Yes	-

The Versal Premium PL Banks are classified as Xtreme Performance (XP) banks or high-density (HD) banks. The XP Bank IO's are optimized for highest performance operation organized in a bank of 703, 704, 705 & 712. Each XPIO bank contains a 48 SE / 24 LVDS pins. The HD Bank I/O's are reduced-feature I/O's organized in a bank of 612 and 613 with 44 SE pins.

In Versal Premium, each XPIO bank supports four Global Clock (GC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and DPLLs of the same Bank. The HD bank supports a two High Density Global Clock (HDGC) input pin pair and have direct access only to the DPLL.

Versal Premium supports 68 high-speed transceiver GTYP from Programmable Logic (PL), these banks support up to 32.75Gbps speed. Also, Versal Premium supports 4 high-speed transceiver GTM from Programmable Logic (PL) which supports up to 112Gbps speed in PAM4 or 29Gbps in NRZ format.

2.3.1 Power

The versal premium SOM uses discrete power regulators and the DA9062 PMIC from Dialog Semiconductor (Renesas) to manage SOM power. In the SOM, the PS low-power domain, PS full-power domain, and PL power domain supply voltage (VCC_PSLP, VCC_PSFP, VCC_SOC, VCC_CPM5 and VCCINT) are up to 0.88V. AMD Versal Premium devices are available in -3 (highest performance), -2, -1 speed grades, depending on the speed grade of the device. Additionally, all PS Bank I/O voltages (VCCO_PSIO) are fixed at 1.8V.

The I/O voltage of FPGA IOs are generated from PMIC. PL XPIO Bank 703 supply is generated from Buck3, PL XPIO Bank 704 is generated from buck4, PL XPIO Bank 705 and 712 supply voltages are generated from PMIC LDOs LDO2 and LDO3, respectively. PL HD Bank 612 and 613 supply voltages are combined and generated from PMIC LDO3. By default, XPIO Banks voltages are set to 1.0V, and HD Banks voltages are set to 1.2V, but they can be configured through software during boot-up.

2.3.2 Reset

The Versal Premium SOM uses Output of the reset IC TPS3808G01DBVR (nRESET) for PS Power On Reset and connected to POR_B_503 pin of SoC. The reset is de asserted after the last of power of SOM is stable.

The SOM also supports hard reset from board-to-board connector2 pin B14.

2.3.3 Versal System Monitor

The System Monitor (SYSMON) resides in the PMC and monitors operating conditions on the device. The SYSMON can access internal sensors for monitoring internal power supplies and temperature. The results captured by the SYSMON are stored in a register map that is accessible through platform management controller resources.

2.3.4 Reference Clocks

The Versal premium SOM supports an on-board clock synthesizer for PS reference clock and reference clock to different blocks of versal premium SOC. These reference clock details are mentioned in the below table.

The Versal premium SOM supports on board clock synthesizer for PS reference clock and reference clock to different blocks of versal premium SOC. The reference clock from Clock Synthesizer to SoC is mentioned in the below table. The SOM supports three clock synthesizer IC to provide clock to on SOM interfaces and transceiver reference clock1. Versal premium SOM clock synthesizer1, “ZL30733LDG1“is pre-programmed to support on board interfaces during power ON, this IC is also connected to I2C-B port of OSM to change the OUT0 to OUT2 frequency after board boots up. The address of Clock syntehsizer1 is 70h.

Versal premium SOM support two clock synthesizer, “SI5341B-D-GM” to support FPGA transceiver secondary reference clocks. The output of these clock synthesizer is configured using I2C-1. The 7-bit address of Clock synthesizer2 and clock synthesizer 3 is 74h and 75h respectively. Refer the below table for clock output frequency details.

Table 4: Clock Synthesizer 1 reference Clocks

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
1	33.3333 MHz	REF_CLK_503	503	AC15	1.8V, LVCMOS	33.33MHz single ended reference clock for PS from OUT0 of Clock Synthesizer 1.
2	200MHz	IO_L24P_GC_XCC_N8P0_M0P48_700	700	AT11	LVDS	LVDS reference clock for PS LPDDR4. This is connected to XPIO_BANK 700 Global clock pins from OUT4 of Clock Synthesizer 1.
		IO_L24N_GC_XCC_N8P1_M0P49_700		AU12		
3	200MHz	IO_L24P_GC_XCC_N8P0_M2P156_708	708	AK43	LVDS	LVDS reference clock for PL LPDDR4-I. This is connected to XPIO_BANK 708 Global clock pins from OUT5 of Clock Synthesizer 1.
		IO_L24N_GC_XCC_N8P1_M2P157_708		AL42		

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
4	200MHz	IO_L24P_GC_XCC_N8P0_M3P48_709	709	M24	LVDS	LVDS reference clock for PL LPDDR4-II. This is connected to XPIO_BANK 709 Global clock pins from OUT6 of Clock Synthesizer 1.
		IO_L24N_GC_XCC_N8P1_M3P49_709		L24		
5	100MHz	IO_L24P_GC_XCC_N8P0_M1P156_705	705	BD30	LVDS	LVDS reference clock This is connected to XPIO BANK 705 Global clock pins from OUT7 of Clock Synthesizer 1.
		IO_L24N_GC_XCC_N8P1_M1P157_705		BE30		
6	100MHz	IO_L24P_GC_XCC_N8P0_M1P48_703	703	BC20	LVDS	LVDS reference clock This is connected to XPIO BANK 705 Global clock pins from OUT9 of Clock Synthesizer 1.
		IO_L24N_GC_XCC_N8P1_M1P49_703		BD20		

Table 5: Clock Synthesizer 2 reference Clocks

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
1	156.25MHz	GTYP_REFCLKP1_200	200	AU47	LVDS	LVDS reference clock This is connected to GTYP_BANK 200 Global clock pins from OUT1 of Clock Synthesizer 2.
		GTYP_REFCLKN1_200		AU48		
2	156.25MHz	GTYP_REFCLKP1_201	201	AN47	LVDS	LVDS reference clock This is connected to GTYP_BANK 201 Global clock pins from OUT2 of Clock Synthesizer 2.
		GTYP_REFCLKN1_201		AN48		
3	156.25MHz	GTM_REFCLKP1_202	202	AG47	LVDS	LVDS reference clock This is connected to GTYP_BANK 202 Global clock pins from OUT3 of Clock Synthesizer 2
		GTM_REFCLKN1_202		AG48		
4	156.25MHz	GTM_REFCLKP1_203	203	AD45	LVDS	LVDS reference clock This is connected to GTYP_BANK 203 Global clock pins from OUT4 of Clock Synthesizer 2
		GTM_REFCLKN1_203		AD46		
5	156.25MHz	GTM_REFCLKP1_204	204	AA43	LVDS	LVDS reference clock This is connected to GTYP_BANK 204 Global clock pins from OUT5 of Clock Synthesizer 2
		GTM_REFCLKN1_204		AA44		
6	156.25MHz	GTM_REFCLKP1_205	205	W43	LVDS	LVDS reference clock This is connected to GTYP_BANK 205 Global clock pins from OUT6 of Clock Synthesizer 2
		GTM_REFCLKN1_205		W44		

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
7	156.25MHz	GTYP_REFCLKP1_207	207	U47	LVDS	LVDS reference clock This is connected to GTYP_BANK 207 Global clock pins from OUT7 of Clock Synthesizer 2
		GTYP_REFCLKN1_207		U48		
8	156.25MHz	GTYP_LPD_REFCLKP1_102	102	AP9	LVDS	LVDS reference clock This is connected to GTYP_BANK 102 Global clock pins from OUT8 of Clock Synthesizer 2.
		GTYP_LPD_REFCLKN1_102		AP8		
9	156.25MHz	GTYP_LPD_REFCLKP1_103	103	AH9	LVDS	LVDS reference clock This is connected to GTYP_BANK 103 Global clock pins from OUT9 of Clock Synthesizer 2
		GTYP_LPD_REFCLKN1_103		AH8		

Table 6: Clock Synthesizer 3 reference Clocks

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
1	110	GTYP_REFCLKP1_110	156.25MHz	N11	LVDS	LVDS reference clock This is connected to GTYP_BANK 110 Global clock pins from OUT0 of Clock Synthesizer 3
		GTYP_REFCLKN1_110		N10		
2	104	GTYP_LPD_REFCLKP1_104	156.25MHz	AE11	LVDS	LVDS reference clock This is connected to GTYP_BANK 104 Global clock pins from OUT1 of Clock Synthesizer 3
		GTYP_LPD_REFCLKN1_104		AE10		
3	105	GTYP_LPD_REFCLKP1_105	156.25MHz	AC11	LVDS	LVDS reference clock This is connected to GTYP_BANK 105 Global clock pins from OUT2 of Clock Synthesizer 3
		GTYP_LPD_REFCLKN1_105		AC10		
4	106	GTYP_REFCLKP1_106	156.25MHz	W11	LVDS	LVDS reference clock This is connected to GTYP_BANK 106 Global clock pins from OUT3 of Clock Synthesizer 3
		GTYP_REFCLKN1_106		W10		
5	208	GTYP_REFCLKP1_208	156.25MHz	R47	LVDS	LVDS reference clock This is connected to GTYP_BANK 208 Global clock pins from OUT4 of Clock Synthesizer 3
		GTYP_REFCLKN1_208		R48		
6	209	GTYP_REFCLKP1_209	156.25MHz	P45	LVDS	LVDS reference clock This is connected to GTYP_BANK 209 Global clock pins from OUT5 of Clock Synthesizer 3
		GTYP_REFCLKN1_209		P46		

Sl. No	On-SOM Synthesizer	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
7	210	GTYP_REFCLKP1_210	156.25MHz	N43	LVDS	LVDS reference clock This is connected to GTYP_BANK 210 Global clock pins from OUT6 of Clock Synthesizer 3
		GTYP_REFCLKN1_210		N44		
8	211	GTYP_REFCLKP1_211	156.25MHz	L47	LVDS	LVDS reference clock This is connected to GTYP_BANK 211 Global clock pins from OUT7 of Clock Synthesizer 3
		GTYP_REFCLKN1_211		L48		
9	212	GTYP_REFCLKN1_212	156.25MHz	J48	LVDS	LVDS reference clock This is connected to GTYP_BANK 212 Global clock pins from OUT8 of Clock Synthesizer 3
		GTYP_REFCLKP1_212		J47		
10	109	GTYP_REFCLKP1_109	156.25MHz	R11	LVDS	LVDS reference clock This is connected to GTYP_BANK 109 Global clock pins from OUT9 of Clock Synthesizer 3.
		GTYP_REFCLKN1_109		R10		

2.4 Memory

2.4.1 LPDDR4 SDRAM for PS

The Versal Premium SOM supports 64bit, 4GB LPDDR4 RAM memory for PS. Two 32 bit, 2GB LPDDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. These LPDDR4 devices operates up to 4266MT/s data rate. Versal Premium SOM, PL XPIO bank of 700, 701 and 702 are used for LPDDR4 interface. Also, the integrated DDR memory controller (DDRMC) is attached to the NoC interconnect.

The Versal Premium SOM supports 200MHz clock from Clock synthesizer to PL XPIO bank of 700 for LPDDR4 bank reference clock and it is connected to AT11 & AU12 clock input pins through AC Coupling capacitors.

2.4.2 LPDDR4 SDRAM1 for PL

The Versal Premium SOM supports 64bit, 4GB LPDDR4 RAM memory for PL. Two 32 bit, 2GB LPDDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. These LPDDR4 devices operates up to 4266MT/s data rate. Versal Premium SOM, PL XPIO bank of 706, 707 and 708 are used for LPDDR4 interface.

The Versal Premium SOM supports 200MHz clock from Clock synthesizer to PL XPIO bank of 708 for LPDDR4 bank reference clock and it is connected to AK43 & AL42 clock input pins through AC Coupling capacitors.

2.4.3 LPDDR4 SDRAM2 for PL

The Versal Premium SOM supports 64bit, 4GB LPDDR4 RAM memory for PL. Two 32 bit, 2GB LPDDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. These LPDDR4 devices are supported from low performance PL XPIO bank of 709, 710 and 711, hence operates up to 3200MT/s data rate. Versal Premium SOM.

The SOM supports 200MHz clock from Clock synthesizer to PL XPIO bank of 709 for LPDDR4 bank reference clock and it is connected to M24 & L24 clock input pins through AC Coupling capacitors.

2.4.4 QSPI Flash

The Versal Premium SOM supports 256MB of Quad SPI through QSPI interface. The QSPI controller use an interface through MIO pins of Versal SOM with 1.8V voltage level. The Flash can be used as boot device or storage device. By default, mode bit is configured for QSPI Flash as configuration device.

2.4.5 eMMC Flash

The Versal Premium SOM supports 16GB eMMC Flash memory and Storage of Versal Adaptive SoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the SOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable up to 128GB for storage

2.4.6 EEPROM

The Versal Premium SOM supports 2Kb EEPROM for storing SOM configuration. The I2C1 module of Versal Adaptive SoC PS is used for EEPROM interface through MIO pins with I2C address 0x52h, 0x5Ah and 0x32h. This device operates at 1.8 voltage level.

2.5 Board-to-Board Connector 1

The Versal Premium SOM supports three 400-pin high-speed, Receptacle, Center Strip Connectors for interface expansion. The SOM design makes every effort to maximize the interfaces of the Versal Adaptive SoC to the carrier board by adding these Three board-to-board connectors.

The pinout for Board-to-Board Connector1 (J5) on the Versal premium SOM is provided in the table below, and the available interfaces are explained in the following sections. Board-to-Board Connector-1 is located on the bottom side of the SOM, as shown in the diagram below.

Number of Pins	- 400
Connector Part Number	- ASP-209946-01 from Samtec
Mating Connector	- ASP-214802-01 from Samtec
Staking Height	- 5mm

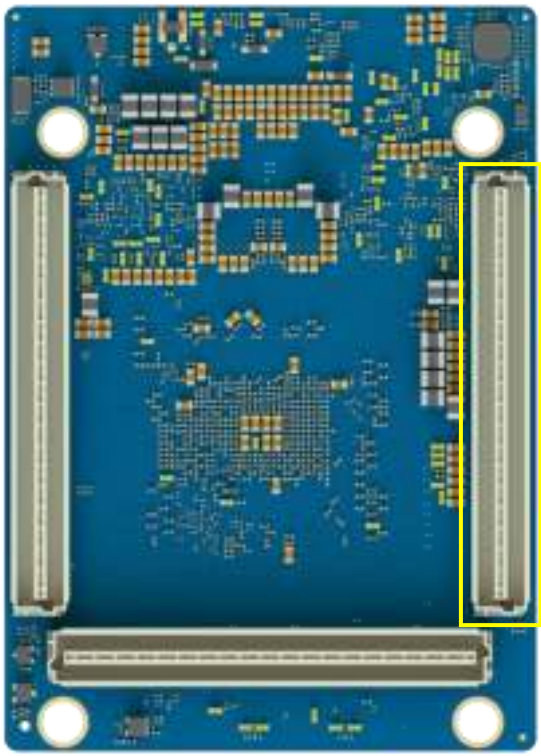


Figure 4: Board-to-Board Connector 1

Table 7: Board-to-Board Connector 1 Pinout

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	VCCO_XPIO_712	B1	VCCO_XPIO_705	C1	VCCO_XPIO_704	D1	VCCO_XPIO_703
A2	XP_BG21_LVDS703_L8P	B2	XP_BH20_LVDS703_L9P_GC	C2	XP_BN19_LVDS703_L3P	D2	XP_BL19_LVDS703_L2P
A3	XP_BH22_LVDS703_L8N	B3	XP_BJ19_LVDS703_L9N_GC	C3	XP_BN20_LVDS703_L3N	D3	XP_BM19_LVDS703_L2N
A4	XP_BG20_LVDS703_L7P	B4	XP_BJ20_LVDS703_L11P	C4	XP_BM21_LVDS703_L5P	D4	XP_BK21_LVDS703_L1P
A5	XP_BH19_LVDS703_L7N	B5	XP_BK20_LVDS703_L11N	C5	XP_BN21_LVDS703_L5N	D5	XP_BL20_LVDS703_L1N
A6	XP_BF22_LVDS703_L6P_GC	B6	XP_BH21_LVDS703_L10P	C6	XP_BM22_LVDS703_L4P	D6	XP_BK22_LVDS703_L0P
A7	XP_BG22_LVDS703_L6N_GC	B7	XP_BJ22_LVDS703_L10N	C7	XP_BN22_LVDS703_L4N	D7	XP_BL21_LVDS703_L0N
A8	GND	B8	GND	C8	GND	D8	GND
A9	XP_AT20_LVDS703_L18P	B9	XP_AV18_LVDS703_L21P	C9	XP_BA19_LVDS703_L15P	D9	XP_AY21_LVDS703_L12P_GC
A10	XP_AU21_LVDS703_L18N	B10	XP_AW19_LVDS703_L21N	C10	XP_BB18_LVDS703_L15N	D10	XP_BA22_LVDS703_L12N_GC
A11	XP_AU20_LVDS703_L20P	B11	XP_AV19_LVDS703_L23P	C11	XP_BB22_LVDS703_L16P	D11	XP_AY20_LVDS703_L14P
A12	XP_AV21_LVDS703_L20N	B12	XP_AW20_LVDS703_L23N	C12	XP_BC21_LVDS703_L16N	D12	XP_BA21_LVDS703_L14N
A13	XP_AT19_LVDS703_L19P	B13	XP_AV22_LVDS703_L22P	C13	XP_BB19_LVDS703_L17P	D13	XP_AY18_LVDS703_L13P
A14	XP_AU18_LVDS703_L19N	B14	XP_AW22_LVDS703_L22N	C14	XP_BB20_LVDS703_L17N	D14	XP_BA18_LVDS703_L13N
A15	GND	B15	GND	C15	GND	D15	GND
A16	XP_BM27_LVDS704_L10P	B16	XP_BG26_LVDS704_L6P_GC	C16	XP_BL23_LVDS704_L3P	D16	XP_BG24_LVDS704_L0P
A17	XP_BN27_LVDS704_L10N	B17	XP_BH26_LVDS704_L6N_GC	C17	XP_BM23_LVDS704_L3N	D17	XP_BH24_LVDS704_L0N
A18	XP_BM26_LVDS704_L11P	B18	XP_BH25_LVDS704_L7P	C18	XP_BN24_LVDS704_L5P	D18	XP_BJ23_LVDS704_L1P
A19	XP_BN26_LVDS704_L11N	B19	XP_BJ25_LVDS704_L7N	C19	XP_BN25_LVDS704_L5N	D19	XP_BK23_LVDS704_L1N
A20	XP_BK26_LVDS704_L9P_GC	B20	XP_BK27_LVDS704_L8P	C20	XP_BL24_LVDS704_L4P	D20	XP_BJ24_LVDS704_L2P
A21	XP_BL25_LVDS704_L9N_GC	B21	XP_BL26_LVDS704_L8N	C21	XP_BM24_LVDS704_L4N	D21	XP_BK25_LVDS704_L2N
A22	GND	B22	GND	C22	GND	D22	GND
A23	XP_AY24_LVDS704_L21P	B23	XP_AY26_LVDS704_L20P	C23	XP_AW23_LVDS704_L15P	D23	XP_AT22_LVDS704_L12P_GC
A24	XP_AW25_LVDS704_L21N	B24	XP_BA25_LVDS704_L20N	C24	XP_AY23_LVDS704_L15N	D24	XP_AT23_LVDS704_L12N_GC
A25	XP_BB26_LVDS704_L22P	B25	XP_AV25_LVDS704_L19P	C25	XP_BB24_LVDS704_L17P	D25	XP_AU23_LVDS704_L13P
A26	XP_BC25_LVDS704_L22N	B26	XP_AW26_LVDS704_L19N	C26	XP_BC24_LVDS704_L17N	D26	XP_AV24_LVDS704_L13N
A27	XP_BD24_LVDS704_L23P	B27	XP_AT26_LVDS704_L18P	C27	XP_BA24_LVDS704_L16P	D27	XP_AT25_LVDS704_L14P
A28	XP_BE25_LVDS704_L23N	B28	XP_AU26_LVDS704_L18N	C28	XP_BB23_LVDS704_L16N	D28	XP_AU24_LVDS704_L14N
A29	GND	B29	GND	C29	GND	D29	GND
A30	XP_BJ28_LVDS705_L11P	B30	XP_BG30_LVDS705_L6P_GC	C30	XP_BN29_LVDS705_L5P	D30	XP_BL28_LVDS705_L1P
A31	XP_BK28_LVDS705_L11N	B31	XP_BH31_LVDS705_L6N_GC	C31	XP_BN30_LVDS705_L5N	D31	XP_BM28_LVDS705_L1N
A32	XP_BH29_LVDS705_L10P	B32	XP_BH30_LVDS705_L8P	C32	XP_BL30_LVDS705_L3P	D32	XP_BK30_LVDS705_L2P
A33	XP_BJ29_LVDS705_L10N	B33	XP_BJ30_LVDS705_L8N	C33	XP_BM29_LVDS705_L3N	D33	XP_BL29_LVDS705_L2N
A34	XP_BH27_LVDS705_L9P_GC	B34	XP_BF27_LVDS705_L7P	C34	XP_BM31_LVDS705_L4P	D34	XP_BK31_LVDS705_L0P
A35	XP_BJ27_LVDS705_L9N_GC	B35	XP_BG28_LVDS705_L7N	C35	XP_BN31_LVDS705_L4N	D35	XP_BL31_LVDS705_L0N
A36	GND	B36	GND	C36	GND	D36	GND
A37	XP_AV27_LVDS705_L21P	B37	XP_AT29_LVDS705_L18P	C37	XP_BB28_LVDS705_L16P	D37	XP_AY30_LVDS705_L12P_GC
A38	XP_AW28_LVDS705_L21N	B38	XP_AU30_LVDS705_L18N	C38	XP_BC29_LVDS705_L16N	D38	XP_BA30_LVDS705_L12N_GC
A39	XP_AV30_LVDS705_L22P	B39	XP_AT28_LVDS705_L19P	C39	XP_BD28_LVDS705_L17P	D39	XP_AY29_LVDS705_L13P

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A40	XP_AW29_LVDS705_L22N	B40	XP_AU27_LVDS705_L19N	C40	XP_BE28_LVDS705_L17N	D40	XP_BA28_LVDS705_L13N
A41	XP_AV36_LVDS705_L23P	B41	XP_AU29_LVDS705_L20P	C41	XP_BB27_LVDS705_L15P	D41	XP_BB30_LVDS705_L14P
A42	XP_AW37_LVDS705_L23N	B42	XP_AV28_LVDS705_L20N	C42	XP_BC28_LVDS705_L15N	D42	XP_BC30_LVDS705_L14N
A43	GND	B43	GND	C43	GND	D43	GND
A44	XP_M33_LVDS712_L11P	B44	XP_N36_LVDS712_L6P_GC	C44	XP_L36_LVDS712_L1P	D44	XP_J38_LVDS712_L4P
A45	XP_L33_LVDS712_L11N	B45	XP_M37_LVDS712_L6N_GC	C45	XP_K37_LVDS712_L1N	D45	XP_J37_LVDS712_L4N
A46	XP_N37_LVDS712_L10P	B46	XP_M36_LVDS712_L8P	C46	XP_L38_LVDS712_L2P	D46	XP_J35_LVDS712_L3P
A47	XP_M38_LVDS712_L10N	B47	XP_L35_LVDS712_L8N	C47	XP_K38_LVDS712_L2N	D47	XP_J34_LVDS712_L3N
A48	XP_M34_LVDS712_L9P_GC	B48	XP_N32_LVDS712_L7P	C48	XP_K36_LVDS712_L0P	D48	XP_K33_LVDS712_L5P
A49	XP_L34_LVDS712_L9N_GC	B49	XP_M32_LVDS712_L7N	C49	XP_K35_LVDS712_L0N	D49	XP_J33_LVDS712_L5N
A50	GND	B50	GND	C50	GND	D50	GND
A51	XP_V31_LVDS712_L21P	B51	XP_V32_LVDS712_L19P	C51	XP_R33_LVDS712_L15P	D51	XP_T35_LVDS712_L12P_GC
A52	XP_U31_LVDS712_L21N	B52	XP_U32_LVDS712_L19N	C52	XP_P33_LVDS712_L15N	D52	XP_R35_LVDS712_L12N_GC
A53	XP_U33_LVDS712_L23P	B53	XP_V35_LVDS712_L18P	C53	XP_T31_LVDS712_L17P	D53	XP_T36_LVDS712_L14P
A54	XP_T33_LVDS712_L23N	B54	XP_V34_LVDS712_L18N	C54	XP_R31_LVDS712_L17N	D54	XP_R36_LVDS712_L14N
A55	XP_V37_LVDS712_L22P	B55	XP_V36_LVDS712_L20P	C55	XP_R37_LVDS712_L16P	D55	XP_U34_LVDS712_L13P
A56	XP_U37_LVDS712_L22N	B56	XP_U36_LVDS712_L20N	C56	XP_P37_LVDS712_L16N	D56	XP_T34_LVDS712_L13N
A57	GND	B57	GND	C57	GND	D57	GND
A58	GND	B58	GND	C58	GND	D58	GND
A59	HDIO_V41_LVDS612_L6P_HDGC	B59	HDIO_W39_LVDS612_L5P_HDGC	C59	NC	D59	GTM_REFCLK1P_107
A60	HDIO_V40_LVDS612_L6N_HDGC	B60	HDIO_V39_LVDS612_L5N_HDGC	C60	NC	D60	GTM_REFCLK1N_107
A61	GND	B61	GND	C61	GND	D61	GND
A62	GND	B62	GND	C62	GND	D62	GND
A63	HDIO_U38_LVDS612_L9P	B63	HDIO_AC40_LVDS612_L0P	C63	HDIO_AB41_LVDS612_L2P	D63	HDIO_AB39_LVDS612_L1P
A64	HDIO_T39_LVDS612_L9N	B64	HDIO_AC39_LVDS612_L0N	C64	HDIO_AA40_LVDS612_L2N	D64	HDIO_AA39_LVDS612_L1N
A65	GND	B65	GND	C65	GND	D65	GND
A66	GND	B66	GND	C66	GND	D66	GND
A67	HDIO_AA41_LVDS612_L3P	B67	HDIO_J43_LVDS613_L9P	C67	HDIO_U39_LVDS612_L8P	D67	HDIO_Y41_LVDS612_L4P
A68	HDIO_Y40_LVDS612_L3N	B68	HDIO_J42_LVDS613_L9N	C68	HDIO_T40_LVDS612_L8N	D68	HDIO_W40_LVDS612_L4N
A69	GND	B69	GND	C69	GND	D69	GND
A70	GND	B70	GND	C70	GND	D70	GND
A71	NC	B71	NC	C71	HDIO_N40_LVDS613_L3P	D71	HDIO_R40_LVDS613_L1P
A72	NC	B72	NC	C72	HDIO_M39_LVDS613_L3N	D72	HDIO_P39_LVDS613_L1N
A73	GND	B73	GND	C73	GND	D73	GND
A74	GND	B74	GND	C74	GND	D74	GND
A75	GTM_TXP3_107	B75	GTM_TXP2_107	C75	GTM_TXP1_107	D75	GTM_TXP0_107
A76	GTM_TXN3_107	B76	GTM_TXN2_107	C76	GTM_TXN1_107	D76	GTM_TXN0_107
A77	GND	B77	GND	C77	GND	D77	GND
A78	GND	B78	GND	C78	GND	D78	GND
A79	HDIO_J40_LVDS613_L10P	B79	HDIO_L41_LVDS613_L7P	C79	HDIO_T38_LVDS612_L10P	D79	HDIO_U41_LVDS612_L7P

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A80	HDIO_J39_LVDS613_L10N	B80	HDIO_K42_LVDS613_L7N	C80	HDIO_R38_LVDS612_L10N	D80	HDIO_T41_LVDS612_L7N
A81	GND	B81	GND	C81	GND	D81	GND
A82	GND	B82	GND	C82	GND	D82	GND
A83	HDIO_P38_LVDS613_L2P	B83	HDIO_L43_LVDS613_L8P	C83	HDIO_N41_LVDS613_L4P	D83	HDIO_R41_LVDS613_L0P
A84	HDIO_N39_LVDS613_L2N	B84	HDIO_K43_LVDS613_L8N	C84	HDIO_M41_LVDS613_L4N	D84	HDIO_P40_LVDS613_L0N
A85	GND	B85	GND	C85	GND	D85	GND
A86	GND	B86	GND	C86	GND	D86	GND
A87	NC	B87	NC	C87	NC	D87	NC
A88	NC	B88	NC	C88	NC	D88	NC
A89	GND	B89	GND	C89	GND	D89	GND
A90	GND	B90	GND	C90	GND	D90	GND
A91	GTM_RXP3_107	B91	GTM_RXP2_107	C91	GTM_RXP1_107	D91	GTM_RXP0_107
A92	GTM_RXN3_107	B92	GTM_RXN2_107	C92	GTM_RXN1_107	D92	GTM_RXN0_107
A93	GND	B93	GND	C93	GND	D93	GND
A94	GND	B94	GND	C94	GND	D94	GND
A95	HDIO_L40_LVDS613_L6P_HDGC	B95	HDIO_L39_LVDS613_L5P_HDGC	C95	NC	D95	GTM_REFCLK0P_107
A96	HDIO_K41_LVDS613_L6N_HDGC	B96	HDIO_K40_LVDS613_L5N_HDGC	C96	NC	D96	GTM_REFCLK0N_107
A97	GND	B97	GND	C97	GND	D97	GND
A98	GND	B98	GND	C98	GND	D98	GND
A99	NC	B99	VCCO_HDIO	C99	NC	D99	VCM0
A100	NC	B100	VCCO_HDIO	C100	NC	D100	VCM1

Important Note: Bank name and bank number mentioned in this document is with respect to VP1552 Devices.

2.5.1 PL Interfaces

The interfaces which are supported in Board-to-Board Connector 1 from Versal Adaptive SoC's PL is explained in the following section.

2.5.1.1 PL IOs – XPIO BANK 703

The Versal Premium SOM supports 24 LVDS IOs/ 48 Single Ended (SE) IOs on Board-to-Board Connector-1 from SoC's PL XPIO BANK 703. Upon these 24 LVDS IOs/ 48 SE IOs, up to 3 GC Global Clock Inputs.

The IO voltage of XPIO BANK 703 is connected from BUCK3 of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.5V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC BUCK3 to appropriate IO voltage for XPIO BANK 703. By default, IO voltage of XPIO BANK 703 is set as 1V and after U-boot boot-up configurable up to 1.5V. For more details about supported IO standard, refer the Versal Premium Series Data Sheet.

In the Versal Premium SOM, XPIO BANK 703 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though XPIO BANK 703 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A6, A7, B2, B3, D9 and D10 are GC Global Clock Input capable pins of XPIO BANK 703.

For more details on XPIO BANK 703 pinouts on Board-to-Board Connector 1, refer the below table.

Table 8: PL IOs - XPIO BANK 703

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A2	XP_BG21_LVDS703_L8P	IO_L8P_N2P4_M1P16_703	XPIO BANK 703	BG21	IO,1.2V LVDS	XPIO BANK 703 IO 08 Differential Positive
A3	XP_BH22_LVDS703_L8N	IO_L8N_N2P5_M1P17_703	XPIO BANK 703	BH22	IO,1.2V LVDS	XPIO BANK 703 IO 08 Differential Negative
A4	XP_BG20_LVDS703_L7P	IO_L7P_N2P2_M1P14_703	XPIO BANK 703	BG20	IO,1.2V LVDS	XPIO BANK 703 IO 07 Differential Positive
A5	XP_BH19_LVDS703_L7N	IO_L7N_N2P3_M1P15_703	XPIO BANK 703	BH19	IO,1.2V LVDS	XPIO BANK 703 IO 07 Differential Negative
A6	XP_BF22_LVDS703_L6P_GC	IO_L6P_GC_XCC_N2P0_M1P12_703	XPIO BANK 703	BF22	IO,1.2V LVDS	XPIO BANK 703 IO 06 Differential Positive
A7	XP_BG22_LVDS703_L6N_GC	IO_L6N_GC_XCC_N2P1_M1P13_703	XPIO BANK 703	BG22	IO,1.2V LVDS	XPIO BANK 703 IO 06 Differential Negative
A9	XP_AT20_LVDS703_L18P	IO_L18P_XCC_N6P0_M1P36_703	XPIO BANK 703	AT20	IO,1.2V LVDS	XPIO BANK 703 IO 18 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A10	XP_AU21_LVDS703_L18N	IO_L18N_XCC_N6P1_M1P37_703	XPIO BANK 703	AU21	IO,1.2V LVDS	XPIO BANK 703 IO 18 Differential Negative
A11	XP_AU20_LVDS703_L20P	IO_L20P_N6P4_M1P40_703	XPIO BANK 703	AU20	IO,1.2V LVDS	XPIO BANK 703 IO 20 Differential Positive
A12	XP_AV21_LVDS703_L20N	IO_L20N_N6P5_M1P41_703	XPIO BANK 703	AV21	IO,1.2V LVDS	XPIO BANK 703 IO 20 Differential Negative
A13	XP_AT19_LVDS703_L19P	IO_L19P_N6P2_M1P38_703	XPIO BANK 703	AT19	IO,1.2V LVDS	XPIO BANK 703 IO 19 Differential Positive
A14	XP_AU18_LVDS703_L19N	IO_L19N_N6P3_M1P39_703	XPIO BANK 703	AU18	IO,1.2V LVDS	XPIO BANK 703 IO 19 Differential Negative
B2	XP_BH20_LVDS703_L9P_GC	IO_L9P_GC_XCC_N3P0_M1P18_703	XPIO BANK 703	BH20	IO,1.2V LVDS	XPIO BANK 703 IO 09 Differential Positive
B3	XP_BJ19_LVDS703_L9N_GC	IO_L9N_GC_XCC_N3P1_M1P19_703	XPIO BANK 703	BJ19	IO,1.2V LVDS	XPIO BANK 703 IO 09 Differential Negative
B4	XP_BJ20_LVDS703_L11P	IO_L11P_N3P4_M1P22_703	XPIO BANK 703	BJ20	IO,1.2V LVDS	XPIO BANK 703 IO 11 Differential Positive
B5	XP_BK20_LVDS703_L11N	IO_L11N_N3P5_M1P23_703	XPIO BANK 703	BK20	IO,1.2V LVDS	XPIO BANK 703 IO 11 Differential Negative
B6	XP_BH21_LVDS703_L10P	IO_L10P_N3P2_M1P20_703	XPIO BANK 703	BH21	IO,1.2V LVDS	XPIO BANK 703 IO 10 Differential Positive
B7	XP_BJ22_LVDS703_L10N	IO_L10N_N3P3_M1P21_703	XPIO BANK 703	BJ22	IO,1.2V LVDS	XPIO BANK 703 IO 10 Differential Negative
B9	XP_AV18_LVDS703_L21P	IO_L21P_XCC_N7P0_M1P42_703	XPIO BANK 703	AV18	IO,1.2V LVDS	XPIO BANK 703 IO 21 Differential Positive
B10	XP_AW19_LVDS703_L21N	IO_L21N_XCC_N7P1_M1P43_703	XPIO BANK 703	AW19	IO,1.2V LVDS	XPIO BANK 703 IO 21 Differential Negative
B11	XP_AV19_LVDS703_L23P	IO_L23P_N7P4_M1P46_703	XPIO BANK 703	AV19	IO,1.2V LVDS	XPIO BANK 703 IO 23 Differential Positive
B12	XP_AW20_LVDS703_L23N	IO_L23N_N7P5_M1P47_703	XPIO BANK 703	AW20	IO,1.2V LVDS	XPIO BANK 703 IO 23 Differential Negative
B13	XP_AV22_LVDS703_L22P	IO_L22P_N7P2_M1P44_703	XPIO BANK 703	AV22	IO,1.2V LVDS	XPIO BANK 703 IO 22 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B14	XP_AW22_LVDS703_L22N	IO_L22N_N7P3_M1P45_703	XPIO BANK 703	AW22	IO,1.2V LVDS	XPIO BANK 703 IO 22 Differential Negative
C2	XP_BN19_LVDS703_L3P	IO_L3P_XCC_N1P0_M1P6_703	XPIO BANK 703	BN19	IO,1.2V LVDS	XPIO BANK 703 IO 03 Differential Positive
C3	XP_BN20_LVDS703_L3N	IO_L3N_XCC_N1P1_M1P7_703	XPIO BANK 703	BN20	IO,1.2V LVDS	XPIO BANK 703 IO 03 Differential Negative
C4	XP_BM21_LVDS703_L5P	IO_L5P_N1P4_M1P10_703	XPIO BANK 703	BM21	IO,1.2V LVDS	XPIO BANK 703 IO 05 Differential Positive
C5	XP_BN21_LVDS703_L5N	IO_L5N_N1P5_M1P11_703	XPIO BANK 703	BN21	IO,1.2V LVDS	XPIO BANK 703 IO 05 Differential Negative
C6	XP_BM22_LVDS703_L4P	IO_L4P_N1P2_M1P8_703	XPIO BANK 703	BM22	IO,1.2V LVDS	XPIO BANK 703 IO 04 Differential Positive
C7	XP_BN22_LVDS703_L4N	IO_L4N_N1P3_M1P9_703	XPIO BANK 703	BN22	IO,1.2V LVDS	XPIO BANK 703 IO 04 Differential Negative
C9	XP_BA19_LVDS703_L15P	IO_L15P_XCC_N5P0_M1P30_703	XPIO BANK 703	BA19	IO,1.2V LVDS	XPIO BANK 703 IO 15 Differential Positive
C10	XP_BB18_LVDS703_L15N	IO_L15N_XCC_N5P1_M1P31_703	XPIO BANK 703	BB18	IO,1.2V LVDS	XPIO BANK 703 IO 15 Differential Negative
C11	XP_BB22_LVDS703_L16P	IO_L16P_N5P2_M1P32_703	XPIO BANK 703	BB22	IO,1.2V LVDS	XPIO BANK 703 IO 16 Differential Positive
C12	XP_BC21_LVDS703_L16N	IO_L16N_N5P3_M1P33_703	XPIO BANK 703	BC21	IO,1.2V LVDS	XPIO BANK 703 IO 16 Differential Negative
C13	XP_BB19_LVDS703_L17P	IO_L17P_N5P4_M1P34_703	XPIO BANK 703	BB19	IO,1.2V LVDS	XPIO BANK 703 IO 17 Differential Positive
C14	XP_BB20_LVDS703_L17N	IO_L17N_N5P5_M1P35_703	XPIO BANK 703	BB20	IO,1.2V LVDS	XPIO BANK 703 IO 17 Differential Negative
D2	XP_BL19_LVDS703_L2P	IO_L2P_N0P4_M1P4_703	XPIO BANK 703	BL19	IO,1.2V LVDS	XPIO BANK 703 IO 02 Differential Positive
D3	XP_BM19_LVDS703_L2N	IO_L2N_N0P5_M1P5_703	XPIO BANK 703	BM19	IO,1.2V LVDS	XPIO BANK 703 IO 02 Differential Negative
D4	XP_BK21_LVDS703_L1P	IO_L1P_N0P2_M1P2_703	XPIO BANK 703	BK21	IO,1.2V LVDS	XPIO BANK 703 IO 01 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D5	XP_BL20_LVDS703_L1N	IO_L1N_N0P3_M1P3_703	XPIO BANK 703	BL20	IO,1.2V LVDS	XPIO BANK 703 IO 01 Differential Negative
D6	XP_BK22_LVDS703_L0P	IO_L0P_XCC_N0P0_M1P0_703	XPIO BANK 703	BK22	IO,1.2V LVDS	XPIO BANK 703 IO 0 Differential Positive
D7	XP_BL21_LVDS703_L0N	IO_L0N_XCC_N0P1_M1P1_703	XPIO BANK 703	BL21	IO,1.2V LVDS	XPIO BANK 703 IO 0 Differential Negative
D9	XP_AY21_LVDS703_L12P_GC	IO_L12P_GC_XCC_N4P0_M1P24_703	XPIO BANK 703	AY21	IO,1.2V LVDS	XPIO BANK 703 IO 12 Differential Positive
D10	XP_BA22_LVDS703_L12N_GC	IO_L12N_GC_XCC_N4P1_M1P25_703	XPIO BANK 703	BA22	IO,1.2V LVDS	XPIO BANK 703 IO 12 Differential Negative
D11	XP_AY20_LVDS703_L14P	IO_L14P_N4P4_M1P28_703	XPIO BANK 703	AY20	IO,1.2V LVDS	XPIO BANK 703 IO 14 Differential Positive
D12	XP_BA21_LVDS703_L14N	IO_L14N_N4P5_M1P29_703	XPIO BANK 703	BA21	IO,1.2V LVDS	XPIO BANK 703 IO 14 Differential Negative
D13	XP_AY18_LVDS703_L13P	IO_L13P_N4P2_M1P26_703	XPIO BANK 703	AY18	IO,1.2V LVDS	XPIO BANK 703 IO 13 Differential Positive
D14	XP_BA18_LVDS703_L13N	IO_L13N_N4P3_M1P27_703	XPIO BANK 703	BA18	IO,1.2V LVDS	XPIO BANK 703 IO 13 Differential Negative

2.5.1.2 PL IOs - XPIO BANK 704

The Versal Premium SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector-1 from SoC's PL XPIO BANK 704. Upon these 24 LVDS IOs/48 SE IOs, Upto 3 GC Global Clock Inputs.

The IO voltage of XPIO BANK 704 is connected from BUCK4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.5V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC BUCK4 to output appropriate IO voltage for XPIO BANK 704. By default, IO voltage of XPIO BANK 704 is set as 1V and after U-boot bootup configurable up to 1.5V. For more details about supported IO standard, refer the Versal Premium Series Data Sheet.

In the Versal Premium SOM, XPIO BANK 704 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though XPIO BANK 704 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A20, A21, B16, B17, D23 and D24 are GC Global Clock Input capable pins of XPIO BANK 704.

For more details on XPIO BANK 704 pinouts on Board-to-Board Connector 1, refer the below table.

Table 9: PL IOs - XPIO BANK 704

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A16	XP_BM27_LVDS704_L10P	IO_L10P_N3P2_M1P74_704	XPIO BANK 704	BM27	IO,1.2V LVDS	XPIO BANK 704 IO 10 Differential Positive
A17	XP_BN27_LVDS704_L10N	IO_L10N_N3P3_M1P75_704	XPIO BANK 704	BN27	IO,1.2V LVDS	XPIO BANK 704 IO 10 Differential Negative
A18	XP_BM26_LVDS704_L11P	IO_L11P_N3P4_M1P76_704	XPIO BANK 704	BM26	IO,1.2V LVDS	XPIO BANK 704 IO 11 Differential Positive
A19	XP_BN26_LVDS704_L11N	IO_L11N_N3P5_M1P77_704	XPIO BANK 704	BN26	IO,1.2V LVDS	XPIO BANK 704 IO 11 Differential Negative
A20	XP_BK26_LVDS704_L9P_GC	IO_L9P_GC_XCC_N3P0_M1P72_704	XPIO BANK 704	BK26	IO,1.2V LVDS	XPIO BANK 704 IO 09 Differential Positive
A21	XP_BL25_LVDS704_L9N_GC	IO_L9N_GC_XCC_N3P1_M1P73_704	XPIO BANK 704	BL25	IO,1.2V LVDS	XPIO BANK 704 IO 09 Differential Negative
A23	XP_AY24_LVDS704_L21P	IO_L21P_XCC_N7P0_M1P96_704	XPIO BANK 704	AY24	IO,1.2V LVDS	XPIO BANK 704 IO 21 Differential Positive
A24	XP_AW25_LVDS704_L21N	IO_L21N_XCC_N7P1_M1P97_704	XPIO BANK 704	AW25	IO,1.2V LVDS	XPIO BANK 704 IO 21 Differential Negative
A25	XP_BB26_LVDS704_L22P	IO_L22P_N7P2_M1P98_704	XPIO BANK 704	BB26	IO,1.2V LVDS	XPIO BANK 704 IO 22 Differential Positive
A26	XP_BC25_LVDS704_L22N	IO_L22N_N7P3_M1P99_704	XPIO BANK 704	BC25	IO,1.2V LVDS	XPIO BANK 704 IO 22 Differential Negative
A27	XP_BD24_LVDS704_L23P	IO_L23P_N7P4_M1P100_704	XPIO BANK 704	BD24	IO,1.2V LVDS	XPIO BANK 704 IO 23 Differential Positive
A28	XP_BE25_LVDS704_L23N	IO_L23N_N7P5_M1P101_704	XPIO BANK 704	BE25	IO,1.2V LVDS	XPIO BANK 704 IO 23 Differential Negative
B16	XP_BG26_LVDS704_L6P_GC	IO_L6P_GC_XCC_N2P0_M1P66_704	XPIO BANK 704	BG26	IO,1.2V LVDS	XPIO BANK 704 IO 06 Differential Positive
B17	XP_BH26_LVDS704_L6N_GC	IO_L6N_GC_XCC_N2P1_M1P67_704	XPIO BANK 704	BH26	IO,1.2V LVDS	XPIO BANK 704 IO 06 Differential Negative
B18	XP_BH25_LVDS704_L7P	IO_L7P_N2P2_M1P68_704	XPIO BANK 704	BH25	IO,1.2V LVDS	XPIO BANK 704 IO 07 Differential Positive
B19	XP_BJ25_LVDS704_L7N	IO_L7N_N2P3_M1P69_704	XPIO BANK 704	BJ25	IO,1.2V LVDS	XPIO BANK 704 IO 07 Differential Negative
B20	XP_BK27_LVDS704_L8P	IO_L8P_N2P4_M1P70_704	XPIO BANK 704	BK27	IO,1.2V LVDS	XPIO BANK 704 IO 08 Differential Positive
B21	XP_BL26_LVDS704_L8N	IO_L8N_N2P5_M1P71_704	XPIO BANK 704	BL26	IO,1.2V LVDS	XPIO BANK 704 IO 08 Differential Negative
B23	XP_AY26_LVDS704_L20P	IO_L20P_N6P4_M1P94_704	XPIO BANK 704	AY26	IO,1.2V LVDS	XPIO BANK 704 IO 20 Differential Positive
B24	XP_BA25_LVDS704_L20N	IO_L20N_N6P5_M1P95_704	XPIO BANK 704	BA25	IO,1.2V LVDS	XPIO BANK 704 IO 20 Differential Negative
B25	XP_AV25_LVDS704_L19P	IO_L19P_N6P2_M1P92_704	XPIO BANK 704	AV25	IO,1.2V LVDS	XPIO BANK 704 IO 19 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B26	XP_AW26_LVDS704_L19N	IO_L19N_N6P3_M1P93_704	XPIO BANK 704	AW26	IO,1.2V LVDS	XPIO BANK 704 IO 19 Differential Negative
B27	XP_AT26_LVDS704_L18P	IO_L18P_XCC_N6P0_M1P90_704	XPIO BANK 704	AT26	IO,1.2V LVDS	XPIO BANK 704 IO 18 Differential Positive
B28	XP_AU26_LVDS704_L18N	IO_L18N_XCC_N6P1_M1P91_704	XPIO BANK 704	AU26	IO,1.2V LVDS	XPIO BANK 704 IO 18 Differential Negative
C16	XP_BL23_LVDS704_L3P	IO_L3P_XCC_N1P0_M1P60_704	XPIO BANK 704	BL23	IO,1.2V LVDS	XPIO BANK 704 IO 03 Differential Positive
C17	XP_BM23_LVDS704_L3N	IO_L3N_XCC_N1P1_M1P61_704	XPIO BANK 704	BM23	IO,1.2V LVDS	XPIO BANK 704 IO 03 Differential Negative
C18	XP_BN24_LVDS704_L5P	IO_L5P_N1P4_M1P64_704	XPIO BANK 704	BN24	IO,1.2V LVDS	XPIO BANK 704 IO 05 Differential Positive
C19	XP_BN25_LVDS704_L5N	IO_L5N_N1P5_M1P65_704	XPIO BANK 704	BN25	IO,1.2V LVDS	XPIO BANK 704 IO 05 Differential Negative
C20	XP_BL24_LVDS704_L4P	IO_L4P_N1P2_M1P62_704	XPIO BANK 704	BL24	IO,1.2V LVDS	XPIO BANK 704 IO 04 Differential Positive
C21	XP_BM24_LVDS704_L4N	IO_L4N_N1P3_M1P63_704	XPIO BANK 704	BM24	IO,1.2V LVDS	XPIO BANK 704 IO 04 Differential Negative
C23	XP_AW23_LVDS704_L15P	IO_L15P_XCC_N5P0_M1P84_704	XPIO BANK 704	AW23	IO,1.2V LVDS	XPIO BANK 704 IO 15 Differential Positive
C24	XP_AY23_LVDS704_L15N	IO_L15N_XCC_N5P1_M1P85_704	XPIO BANK 704	AY23	IO,1.2V LVDS	XPIO BANK 704 IO 15 Differential Negative
C25	XP_BB24_LVDS704_L17P	IO_L17P_N5P4_M1P88_704	XPIO BANK 704	BB24	IO,1.2V LVDS	XPIO BANK 704 IO 17 Differential Positive
C26	XP_BC24_LVDS704_L17N	IO_L17N_N5P5_M1P89_704	XPIO BANK 704	BC24	IO,1.2V LVDS	XPIO BANK 704 IO 17 Differential Negative
C27	XP_BA24_LVDS704_L16P	IO_L16P_N5P2_M1P86_704	XPIO BANK 704	BA24	IO,1.2V LVDS	XPIO BANK 704 IO 16 Differential Positive
C28	XP_BB23_LVDS704_L16N	IO_L16N_N5P3_M1P87_704	XPIO BANK 704	BB23	IO,1.2V LVDS	XPIO BANK 704 IO 16 Differential Negative
D16	XP_BG24_LVDS704_L0P	IO_L0P_XCC_N0P0_M1P54_704	XPIO BANK 704	BG24	IO,1.2V LVDS	XPIO BANK 704 IO 0 Differential Positive
D17	XP_BH24_LVDS704_L0N	IO_L0N_XCC_N0P1_M1P55_704	XPIO BANK 704	BH24	IO,1.2V LVDS	XPIO BANK 704 IO 0 Differential Negative
D18	XP_BJ23_LVDS704_L1P	IO_L1P_N0P2_M1P56_704	XPIO BANK 704	BJ23	IO,1.2V LVDS	XPIO BANK 704 IO 01 Differential Positive
D19	XP_BK23_LVDS704_L1N	IO_L1N_N0P3_M1P57_704	XPIO BANK 704	BK23	IO,1.2V LVDS	XPIO BANK 704 IO 01 Differential Negative
D20	XP_BJ24_LVDS704_L2P	IO_L2P_N0P4_M1P58_704	XPIO BANK 704	BJ24	IO,1.2V LVDS	XPIO BANK 704 IO 02 Differential Positive
D21	XP_BK25_LVDS704_L2N	IO_L2N_N0P5_M1P59_704	XPIO BANK 704	BK25	IO,1.2V LVDS	XPIO BANK 704 IO 02 Differential Negative
D23	XP_AT22_LVDS704_L12P_GC	IO_L12P_GC_XCC_N4P0_M1P78_704	XPIO BANK 704	AT22	IO,1.2V LVDS	XPIO BANK 704 IO 12 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D24	XP_AT23_LVDS704_L12N_GC	IO_L12N_GC_XCC_N4P1_M1P79_704	XPIO BANK 704	AT23	IO,1.2V LVDS	XPIO BANK 704 IO 12 Differential Negative
D25	XP_AU23_LVDS704_L13P	IO_L13P_N4P2_M1P80_704	XPIO BANK 704	AU23	IO,1.2V LVDS	XPIO BANK 704 IO 13 Differential Positive
D26	XP_AV24_LVDS704_L13N	IO_L13N_N4P3_M1P81_704	XPIO BANK 704	AV24	IO,1.2V LVDS	XPIO BANK 704 IO 13 Differential Negative
D27	XP_AT25_LVDS704_L14P	IO_L14P_N4P4_M1P82_704	XPIO BANK 704	AT25	IO,1.2V LVDS	XPIO BANK 704 IO 14 Differential Positive
D28	XP_AU24_LVDS704_L14N	IO_L14N_N4P5_M1P83_704	XPIO BANK 704	AU24	IO,1.2V LVDS	XPIO BANK 704 IO 14 Differential Negative

2.5.1.3 PL IOs - XPIO BANK 705

The Versal Premium SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector-1 from SoC's PL XPIO BANK 705. Upon these 24 LVDS IOs/48 SE IOs, Upto 3 GC Global Clock Inputs.

The IO voltage of XPIO BANK 705 is connected from LDO2 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.5V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO2 to output appropriate IO voltage for XPIO BANK 705. By default, IO voltage of XPIO BANK 705 is set as 1V and after U-boot bootup configurable up to 1.5V. For more details about supported IO standard, refer the Versal Premium Series Data Sheet.

In the Versal Premium SOM, XPIO BANK 705 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though XPIO BANK 705 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A34, A35, B30, B31, D37 and D38 are GC Global Clock Input capable pins of XPIO BANK 705.

For more details on XPIO BANK 705 pinouts on Board-to-Board Connector 1, refer the below table.

Table 10: PL IOs - XPIO BANK 705

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A30	XP_BJ28_LVDS705_L11P	IO_L11P_N3P4_M1P130_705	XPIO BANK 705	BJ28	IO,1.2V LVDS	XPIO BANK 705 IO 11 Differential Positive
A31	XP_BK28_LVDS705_L11N	IO_L11N_N3P5_M1P131_705	XPIO BANK 705	BK28	IO,1.2V LVDS	XPIO BANK 705 IO 11 Differential Negative
A32	XP_BH29_LVDS705_L10P	IO_L10P_N3P2_M1P128_705	XPIO BANK 705	BH29	IO,1.2V LVDS	XPIO BANK 705 IO 10 Differential Positive
A33	XP_BJ29_LVDS705_L10N	IO_L10N_N3P3_M1P129_705	XPIO BANK 705	BJ29	IO,1.2V LVDS	XPIO BANK 705 IO 10 Differential Negative
A34	XP_BH27_LVDS705_L9P_GC	IO_L9P_GC_XCC_N3P0_M1P126_705	XPIO BANK 705	BH27	IO,1.2V LVDS	XPIO BANK 705 IO 09 Differential Positive
A35	XP_BJ27_LVDS705_L9N_GC	IO_L9N_GC_XCC_N3P1_M1P127_705	XPIO BANK 705	BJ27	IO,1.2V LVDS	XPIO BANK 705 IO 09 Differential Negative

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A37	XP_AV27_LVDS705_L21P	IO_L21P_XCC_N7P0_M1P150_705	XPIO BANK 705	AV27	IO,1.2V LVDS	XPIO BANK 705 IO 21 Differential Positive
A38	XP_AW28_LVDS705_L21N	IO_L21N_XCC_N7P1_M1P151_705	XPIO BANK 705	AW28	IO,1.2V LVDS	XPIO BANK 705 IO 21 Differential Negative
A39	XP_AV30_LVDS705_L22P	IO_L22P_N7P2_M1P152_705	XPIO BANK 705	AV30	IO,1.2V LVDS	XPIO BANK 705 IO 22 Differential Positive
A40	XP_AW29_LVDS705_L22N	IO_L22N_N7P3_M1P153_705	XPIO BANK 705	AW29	IO,1.2V LVDS	XPIO BANK 705 IO 22 Differential Negative
A41	XP_AV36_LVDS705_L23P	IO_L23P_N7P4_M1P154_705	XPIO BANK 705	AY27	IO,1.2V LVDS	XPIO BANK 705 IO 23 Differential Positive
A42	XP_AW37_LVDS705_L23N	IO_L23N_N7P5_M1P155_705	XPIO BANK 705	BA27	IO,1.2V LVDS	XPIO BANK 705 IO 23 Differential Negative
B30	XP_BG30_LVDS705_L6P_GC	IO_L6P_GC_XCC_N2P0_M1P120_705	XPIO BANK 705	BG30	IO,1.2V LVDS	XPIO BANK 705 IO 06 Differential Positive
B31	XP_BH31_LVDS705_L6N_GC	IO_L6N_GC_XCC_N2P1_M1P121_705	XPIO BANK 705	BH31	IO,1.2V LVDS	XPIO BANK 705 IO 06 Differential Negative
B32	XP_BH30_LVDS705_L8P	IO_L8P_N2P4_M1P124_705	XPIO BANK 705	BH30	IO,1.2V LVDS	XPIO BANK 705 IO 08 Differential Positive
B33	XP_BJ30_LVDS705_L8N	IO_L8N_N2P5_M1P125_705	XPIO BANK 705	BJ30	IO,1.2V LVDS	XPIO BANK 705 IO 08 Differential Negative
B34	XP_BF27_LVDS705_L7P	IO_L7P_N2P2_M1P122_705	XPIO BANK 705	BF27	IO,1.2V LVDS	XPIO BANK 705 IO 07 Differential Positive
B35	XP_BG28_LVDS705_L7N	IO_L7N_N2P3_M1P123_705	XPIO BANK 705	BG28	IO,1.2V LVDS	XPIO BANK 705 IO 07 Differential Negative
B37	XP_AT29_LVDS705_L18P	IO_L18P_XCC_N6P0_M1P144_705	XPIO BANK 705	AT29	IO,1.2V LVDS	XPIO BANK 705 IO 18 Differential Positive
B38	XP_AU30_LVDS705_L18N	IO_L18N_XCC_N6P1_M1P145_705	XPIO BANK 705	AU30	IO,1.2V LVDS	XPIO BANK 705 IO 18 Differential Negative
B39	XP_AT28_LVDS705_L19P	IO_L19P_N6P2_M1P146_705	XPIO BANK 705	AT28	IO,1.2V LVDS	XPIO BANK 705 IO 19 Differential Positive
B40	XP_AU27_LVDS705_L19N	IO_L19N_N6P3_M1P147_705	XPIO BANK 705	AU27	IO,1.2V LVDS	XPIO BANK 705 IO 19 Differential Negative
B41	XP_AU29_LVDS705_L20P	IO_L20P_N6P4_M1P148_705	XPIO BANK 705	AU29	IO,1.2V LVDS	XPIO BANK 705 IO 20 Differential Positive
B42	XP_AV28_LVDS705_L20N	IO_L20N_N6P5_M1P149_705	XPIO BANK 705	AV28	IO,1.2V LVDS	XPIO BANK 705 IO 20 Differential Negative
C30	XP_BN29_LVDS705_L5P	IO_L5P_N1P4_M1P118_705	XPIO BANK 705	BN29	IO,1.2V LVDS	XPIO BANK 705 IO 05 Differential Positive
C31	XP_BN30_LVDS705_L5N	IO_L5N_N1P5_M1P119_705	XPIO BANK 705	BN30	IO,1.2V LVDS	XPIO BANK 705 IO 05 Differential Negative
C32	XP_BL30_LVDS705_L3P	IO_L3P_XCC_N1P0_M1P114_705	XPIO BANK 705	BL30	IO,1.2V LVDS	XPIO BANK 705 IO 03 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C33	XP_BM29_LVDS705_L3N	IO_L3N_XCC_N1P1_M1P115_705	XPIO BANK 705	BM29	IO,1.2V LVDS	XPIO BANK 705 IO 03 Differential Negative
C34	XP_BM31_LVDS705_L4P	IO_L4P_N1P2_M1P116_705	XPIO BANK 705	BM31	IO,1.2V LVDS	XPIO BANK 705 IO 04 Differential Positive
C35	XP_BN31_LVDS705_L4N	IO_L4N_N1P3_M1P117_705	XPIO BANK 705	BN31	IO,1.2V LVDS	XPIO BANK 705 IO 04 Differential Negative
C37	XP_BB28_LVDS705_L16P	IO_L16P_N5P2_M1P140_705	XPIO BANK 705	BB28	IO,1.2V LVDS	XPIO BANK 705 IO 16 Differential Positive
C38	XP_BC29_LVDS705_L16N	IO_L16N_N5P3_M1P141_705	XPIO BANK 705	BC29	IO,1.2V LVDS	XPIO BANK 705 IO 16 Differential Negative
C39	XP_BD28_LVDS705_L17P	IO_L17P_N5P4_M1P142_705	XPIO BANK 705	BD28	IO,1.2V LVDS	XPIO BANK 705 IO 17 Differential Positive
C40	XP_BE28_LVDS705_L17N	IO_L17N_N5P5_M1P143_705	XPIO BANK 705	BE28	IO,1.2V LVDS	XPIO BANK 705 IO 17 Differential Negative
C41	XP_BB27_LVDS705_L15P	IO_L15P_XCC_N5P0_M1P138_705	XPIO BANK 705	BB27	IO,1.2V LVDS	XPIO BANK 705 IO 15 Differential Positive
C42	XP_BC28_LVDS705_L15N	IO_L15N_XCC_N5P1_M1P139_705	XPIO BANK 705	BC28	IO,1.2V LVDS	XPIO BANK 705 IO 15 Differential Negative
D30	XP_BL28_LVDS705_L1P	IO_L1P_N0P2_M1P110_705	XPIO BANK 705	BL28	IO,1.2V LVDS	XPIO BANK 705 IO 01 Differential Positive
D31	XP_BM28_LVDS705_L1N	IO_L1N_N0P3_M1P111_705	XPIO BANK 705	BM28	IO,1.2V LVDS	XPIO BANK 705 IO 01 Differential Negative
D32	XP_BK30_LVDS705_L2P	IO_L2P_N0P4_M1P112_705	XPIO BANK 705	BK30	IO,1.2V LVDS	XPIO BANK 705 IO 02 Differential Positive
D33	XP_BL29_LVDS705_L2N	IO_L2N_N0P5_M1P113_705	XPIO BANK 705	BL29	IO,1.2V LVDS	XPIO BANK 705 IO 02 Differential Negative
D34	XP_BK31_LVDS705_L0P	IO_L0P_XCC_N0P0_M1P108_705	XPIO BANK 705	BK31	IO,1.2V LVDS	XPIO BANK 705 IO 00 Differential Positive
D35	XP_BL31_LVDS705_L0N	IO_L0N_XCC_N0P1_M1P109_705	XPIO BANK 705	BL31	IO,1.2V LVDS	XPIO BANK 705 IO 00 Differential Negative
D37	XP_AY30_LVDS705_L12P_GC	IO_L12P_GC_XCC_N4P0_M1P132_705	XPIO BANK 705	AY30	IO,1.2V LVDS	XPIO BANK 705 IO 12 Differential Positive
D38	XP_BA30_LVDS705_L12N_GC	IO_L12N_GC_XCC_N4P1_M1P133_705	XPIO BANK 705	BA30	IO,1.2V LVDS	XPIO BANK 705 IO 12 Differential Negative
D39	XP_AY29_LVDS705_L13P	IO_L13P_N4P2_M1P134_705	XPIO BANK 705	AY29	IO,1.2V LVDS	XPIO BANK 705 IO 13 Differential Positive
D40	XP_BA28_LVDS705_L13N	IO_L13N_N4P3_M1P135_705	XPIO BANK 705	BA28	IO,1.2V LVDS	XPIO BANK 705 IO 13 Differential Negative
D41	XP_BB30_LVDS705_L14P	IO_L14P_N4P4_M1P136_705	XPIO BANK 705	BB30	IO,1.2V LVDS	XPIO BANK 705 IO 14 Differential Positive
D42	XP_BC30_LVDS705_L14N	IO_L14N_N4P5_M1P137_705	XPIO BANK 705	BC30	IO,1.2V LVDS	XPIO BANK 705 IO 14 Differential Negative

2.5.1.4 PL IOs – XPIO BANK 712

The Versal Premium SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board-to-Board Connector-1 from SoC's PL XPIO BANK 712. Upon these 24 LVDS IOs/48 SE IOs, Upto 3 GC Global Clock Inputs.

The IO voltage of XPIO BANK 712 is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.5V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for XPIO BANK 712. By default, IO voltage of XPIO BANK 712 is set as 1V and after U-boot bootup configurable up to 1.5V. For more details about supported IO standard, refer the Versal Premium Series Data Sheet.

In the Versal Premium SOM, XPIO BANK 712 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though XPIO BANK 712 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A48, A49, B44, B45, D51 and D52 are GC Global Clock Input capable pins of XPIO BANK 712

For more details on XPIO BANK 712 pinouts on Board-to-Board Connector 1, refer the below table.

Table 11: PL IOs - XPIO BANK 712

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A44	XP_M33_LVDS712_L11P	IO_L11P_N3P4_712	XPIO BANK 712	M33	IO,1.2V LVDS	XPIO BANK 712 IO 11 Differential Positive
A45	XP_L33_LVDS712_L11N	IO_L11N_N3P5_712	XPIO BANK 712	L33	IO,1.2V LVDS	XPIO BANK 712 IO 11 Differential Negative
A46	XP_N37_LVDS712_L10P	IO_L10P_N3P2_712	XPIO BANK 712	N37	IO,1.2V LVDS	XPIO BANK 712 IO 10 Differential Positive
A47	XP_M38_LVDS712_L10N	IO_L10N_N3P3_712	XPIO BANK 712	M38	IO,1.2V LVDS	XPIO BANK 712 IO 10 Differential Negative
A48	XP_M34_LVDS712_L9P_GC	IO_L9P_GC_XCC_N3P0_712	XPIO BANK 712	M34	IO,1.2V LVDS	XPIO BANK 712 IO 09 Differential Positive
A49	XP_L34_LVDS712_L9N_GC	IO_L9N_GC_XCC_N3P1_712	XPIO BANK 712	L34	IO,1.2V LVDS	XPIO BANK 712 IO 09 Differential Negative
A51	XP_V31_LVDS712_L21P	IO_L21P_XCC_N7P0_712	XPIO BANK 712	V31	IO,1.2V LVDS	XPIO BANK 712 IO 21 Differential Positive
A52	XP_U31_LVDS712_L21N	IO_L21N_XCC_N7P1_712	XPIO BANK 712	U31	IO,1.2V LVDS	XPIO BANK 712 IO 21 Differential Negative
A53	XP_U33_LVDS712_L23P	IO_L23P_N7P4_712	XPIO BANK 712	U33	IO,1.2V LVDS	XPIO BANK 712 IO 23 Differential Positive

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A54	XP_T33_LVDS712_L23N	IO_L23N_N7P5_712	XPIO BANK 712	T33	IO,1.2V LVDS	XPIO BANK 712 IO 23 Differential Negative
A55	XP_V37_LVDS712_L22P	IO_L22P_N7P2_712	XPIO BANK 712	V37	IO,1.2V LVDS	XPIO BANK 712 IO 22 Differential Positive
A56	XP_U37_LVDS712_L22N	IO_L22N_N7P3_712	XPIO BANK 712	U37	IO,1.2V LVDS	XPIO BANK 712 IO 22 Differential Negative
B44	XP_N36_LVDS712_L6P_GC	IO_L6P_GC_XCC_N2P0_712	XPIO BANK 712	N36	IO,1.2V LVDS	XPIO BANK 712 IO 06 Differential Positive
B45	XP_M37_LVDS712_L6N_GC	IO_L6N_GC_XCC_N2P1_712	XPIO BANK 712	M37	IO,1.2V LVDS	XPIO BANK 712 IO 06 Differential Negative
B46	XP_M36_LVDS712_L8P	IO_L8P_N2P4_712	XPIO BANK 712	M36	IO,1.2V LVDS	XPIO BANK 712 IO 08 Differential Positive
B47	XP_L35_LVDS712_L8N	IO_L8N_N2P5_712	XPIO BANK 712	L35	IO,1.2V LVDS	XPIO BANK 712 IO 08 Differential Negative
B48	XP_N32_LVDS712_L7P	IO_L7P_N2P2_712	XPIO BANK 712	N32	IO,1.2V LVDS	XPIO BANK 712 IO 07 Differential Positive
B49	XP_M32_LVDS712_L7N	IO_L7N_N2P3_712	XPIO BANK 712	M32	IO,1.2V LVDS	XPIO BANK 712 IO 07 Differential Negative
B51	XP_V32_LVDS712_L19P	IO_L19P_N6P2_712	XPIO BANK 712	V32	IO,1.2V LVDS	XPIO BANK 712 IO 19 Differential Positive
B52	XP_U32_LVDS712_L19N	IO_L19N_N6P3_712	XPIO BANK 712	U32	IO,1.2V LVDS	XPIO BANK 712 IO 19 Differential Negative
B53	XP_V35_LVDS712_L18P	IO_L18P_XCC_N6P0_712	XPIO BANK 712	V35	IO,1.2V LVDS	XPIO BANK 712 IO 18 Differential Positive
B54	XP_V34_LVDS712_L18N	IO_L18N_XCC_N6P1_712	XPIO BANK 712	V34	IO,1.2V LVDS	XPIO BANK 712 IO 18 Differential Negative
B55	XP_V36_LVDS712_L20P	IO_L20P_N6P4_712	XPIO BANK 712	V36	IO,1.2V LVDS	XPIO BANK 712 IO 20 Differential Positive
B56	XP_U36_LVDS712_L20N	IO_L20N_N6P5_712	XPIO BANK 712	U36	IO,1.2V LVDS	XPIO BANK 712 IO 20 Differential Negative

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C44	XP_L36_LVDS712_L1P	IO_L1P_N0P2_712	XPIO BANK 712	L36	IO,1.2V LVDS	XPIO BANK 712 IO 01 Differential Positive
C45	XP_K37_LVDS712_L1N	IO_L1N_N0P3_712	XPIO BANK 712	K37	IO,1.2V LVDS	XPIO BANK 712 IO 01 Differential Negative
C46	XP_L38_LVDS712_L2P	IO_L2P_N0P4_712	XPIO BANK 712	L38	IO,1.2V LVDS	XPIO BANK 712 IO 02 Differential Positive
C47	XP_K38_LVDS712_L2N	IO_L2N_N0P5_712	XPIO BANK 712	K38	IO,1.2V LVDS	XPIO BANK 712 IO 02 Differential Negative
C48	XP_K36_LVDS712_L0P	IO_L0P_XCC_N0P0_712	XPIO BANK 712	K36	IO,1.2V LVDS	XPIO BANK 712 IO 00 Differential Positive
C49	XP_K35_LVDS712_L0N	IO_L0N_XCC_N0P1_712	XPIO BANK 712	K35	IO,1.2V LVDS	XPIO BANK 712 IO 00 Differential Negative
C51	XP_R33_LVDS712_L15P	IO_L15P_XCC_N5P0_712	XPIO BANK 712	R33	IO,1.2V LVDS	XPIO BANK 712 IO 15 Differential Positive
C52	XP_P33_LVDS712_L15N	IO_L15N_XCC_N5P1_712	XPIO BANK 712	P33	IO,1.2V LVDS	XPIO BANK 712 IO 15 Differential Negative
C53	XP_T31_LVDS712_L17P	IO_L17P_N5P4_712	XPIO BANK 712	T31	IO,1.2V LVDS	XPIO BANK 712 IO 17 Differential Positive
C54	XP_R31_LVDS712_L17N	IO_L17N_N5P5_712	XPIO BANK 712	R31	IO,1.2V LVDS	XPIO BANK 712 IO 17 Differential Negative
C55	XP_R37_LVDS712_L16P	IO_L16P_N5P2_712	XPIO BANK 712	R37	IO,1.2V LVDS	XPIO BANK 712 IO 16 Differential Positive
C56	XP_P37_LVDS712_L16N	IO_L16N_N5P3_712	XPIO BANK 712	P37	IO,1.2V LVDS	XPIO BANK 712 IO 16 Differential Negative
D44	XP_J38_LVDS712_L4P	IO_L4P_N1P2_712	XPIO BANK 712	J38	IO,1.2V LVDS	XPIO BANK 712 IO 04 Differential Positive
D45	XP_J37_LVDS712_L4N	IO_L4N_N1P3_712	XPIO BANK 712	J37	IO,1.2V LVDS	XPIO BANK 712 IO 04 Differential Negative
D46	XP_J35_LVDS712_L3P	IO_L3P_XCC_N1P0_712	XPIO BANK 712	J35	IO,1.2V LVDS	XPIO BANK 712 IO 03 Differential Positive
D47	XP_J34_LVDS712_L3N	IO_L3N_XCC_N1P1_712	XPIO BANK 712	J34	IO,1.2V LVDS	XPIO BANK 712 IO 03 Differential Negative

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D48	XP_K33_LVDS712_L5P	IO_L5P_N1P4_712	XPIO BANK 712	K33	IO,1.2V LVDS	XPIO BANK 712 IO 05 Differential Positive
D49	XP_J33_LVDS712_L5N	IO_L5N_N1P5_712	XPIO BANK 712	J33	IO,1.2V LVDS	XPIO BANK 712 IO 05 Differential Negative
D51	XP_T35_LVDS712_L12P_GC	IO_L12P_GC_XCC_N4P0_712	XPIO BANK 712	T35	IO,1.2V LVDS	XPIO BANK 712 IO 12 Differential Positive
D52	XP_R35_LVDS712_L12N_GC	IO_L12N_GC_XCC_N4P1_712	XPIO BANK 712	R35	IO,1.2V LVDS	XPIO BANK 712 IO 12 Differential Negative
D53	XP_T36_LVDS712_L14P	IO_L14P_N4P4_712	XPIO BANK 712	T36	IO,1.2V LVDS	XPIO BANK 712 IO 14 Differential Positive
D54	XP_R36_LVDS712_L14N	IO_L14N_N4P5_712	XPIO BANK 712	R36	IO,1.2V LVDS	XPIO BANK 712 IO 14 Differential Negative
D55	XP_U34_LVDS712_L13P	IO_L13P_N4P2_712	XPIO BANK 712	U34	IO,1.2V LVDS	XPIO BANK 712 IO 13 Differential Positive
D56	XP_T34_LVDS712_L13N	IO_L13N_N4P3_712	XPIO BANK 712	T34	IO,1.2V LVDS	XPIO BANK 712 IO 13 Differential Negative

2.5.1.5 PL IOs - HDIO BANK

The Versal Premium SOM supports 44 Single Ended (SE) IOs on Board-to-Board Connector-1 from SoC's PL HDIO BANK 612/613. Upon these 24 SE IOs, up to 4 GC Global input pairs.

The IO voltage of HDIO BANK 612/613 is connected from LDO4 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1V to 1.8V through software. While using as LVDS IOs or Single Ended IOs, make sure to set the PMIC LDO4 to output appropriate IO voltage for HDIO BANK 612/613. By default, IO voltage of HDIO BANK 612/613 is set as 1V and after U-boot bootup configurable up to 1.8V. For more details about supported IO standard, refer the Versal Premium Series Data Sheet.

In the Versal Premium SOM, HDIO BANK 612/613 signals are routed as LVDS IOs to Board-to-Board Connector-1. Even though XPIO BANK 712 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board-to-Board Connector-1 pins A59, A60, B59, B60, B95, B96, A96 and A96 are GC Global Clock Input capable pins of HDIO BANK 612/613.

Important Note: HDIO Bank is only available in VP1402 devices, these pins are NC in other devices.

For more details on HDIO BANK 612/613 pinouts on Board-to-Board Connector 1, refer the below table.

Table 12: PL IOs - HDIO BANK 612/613

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A59	HDIO_V41_LVDS612_L6P_HDGC	NC/IO_L6P_HDGC_612	HDIO BANK 612	V41	IO,1.8V	PL HDIO BANK 612 IO 06 signal.
A60	HDIO_V40_LVDS612_L6N_HDGC	NC/IO_L6N_HDGC_612	HDIO BANK 612	V40	IO,1.8V	PL HDIO BANK 612 IO 06 signal.
A63	HDIO_U38_LVDS612_L9P	NC/IO_L9P_612	HDIO BANK 612	U38	IO,1.8V	PL HDIO BANK 612 IO 09 signal.
A64	HDIO_T39_LVDS612_L9N	NC/IO_L9N_612	HDIO BANK 612	T39	IO,1.8V	PL HDIO BANK 612 IO 03 signal.
A67	HDIO_AA41_LVDS612_L3P	NC/IO_L3P_612	HDIO BANK 612	AA41	IO,1.8V	PL HDIO BANK 612 IO 03 signal.
A68	HDIO_Y40_LVDS612_L3N	NC/IO_L3N_612	HDIO BANK 612	Y40	IO,1.8V	PL HDIO BANK 612 IO 03 signal.
B59	HDIO_W39_LVDS612_L5P_HDGC	NC/IO_L5P_HDGC_612	HDIO BANK 612	W39	IO,1.8V	HDIO BANK 612 IO 05 signal.
B60	HDIO_V39_LVDS612_L5N_HDGC	NC/IO_L5N_HDGC_612	HDIO BANK 612	V39	IO,1.8V	HDIO BANK 612 IO 05 signal.
B63	HDIO_AC40_LVDS612_L0P	NC/IO_L0P_612	HDIO BANK 612	AC40	IO,1.8V	HDIO BANK 612 IO 00 signal.
B64	HDIO_AC39_LVDS612_L0N	NC/IO_L0N_612	HDIO BANK 612	AC39	IO,1.8V	HDIO BANK 612 IO 00 signal.
C63	HDIO_AB41_LVDS612_L2P	NC/IO_L2P_612	HDIO BANK 612	AB41	IO,1.8V	HDIO BANK 612 IO 02 signal.
C64	HDIO_AA40_LVDS612_L2N	NC/IO_L2N_612	HDIO BANK 612	AA40	IO,1.8V	HDIO BANK 612 IO 02 signal.
C67	HDIO_U39_LVDS612_L8P	NC/IO_L8P_612	HDIO BANK 612	U39	IO,1.8V	HDIO BANK 612 IO 08 signal.
C68	HDIO_T40_LVDS612_L8N	NC/IO_L8N_612	HDIO BANK 612	T40	IO,1.8V	HDIO BANK 612 IO 08 signal.
C79	HDIO_T38_LVDS612_L10P	NC/IO_L10P_612	HDIO BANK 612	T38	IO,1.8V	HDIO BANK 612 IO 10 signal.
C80	HDIO_R38_LVDS612_L10N	NC/IO_L10N_612	HDIO BANK 612	R38	IO,1.8V	HDIO BANK 612 IO 10 signal.
D63	HDIO_AB39_LVDS612_L1P	NC/IO_L1P_612	HDIO BANK 612	AB39	IO,1.8V	HDIO BANK 612 IO 01 signal.
D64	HDIO_AA39_LVDS612_L1N	NC/IO_L1N_612	HDIO BANK 612	AA39	IO,1.8V	HDIO BANK 612 IO 01 signal.
D67	HDIO_Y41_LVDS612_L4P	NC/IO_L4P_612	HDIO BANK 612	Y41	IO,1.8V	HDIO BANK 612 IO 04 signal.
D68	HDIO_W40_LVDS612_L4N	NC/IO_L4N_612	HDIO BANK 612	W40	IO,1.8V	HDIO BANK 612 IO 04 signal.

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D79	HDIO_U41_LVDS612_L7P	NC/IO_L7P_612	HDIO BANK 612	U41	IO,1.8V	HDIO BANK 612 IO 07 signal.
D80	HDIO_T41_LVDS612_L7N	NC/IO_L7N_612	HDIO BANK 612	T41	IO,1.8V	HDIO BANK 612 IO 07 signal.
A79	HDIO_J40_LVDS613_L10P	NC/IO_L10P_613	HDIO BANK 613	J40	IO,1.8V	HDIO BANK 613 IO 10 signal.
A80	HDIO_J39_LVDS613_L10N	NC/IO_L10N_613	HDIO BANK 613	J39	IO,1.8V	HDIO BANK 613 IO 10 signal.
A83	HDIO_P38_LVDS613_L2P	NC/IO_L2P_613	HDIO BANK 613	P38	IO,1.8V	HDIO BANK 613 IO 02 signal.
A84	HDIO_N39_LVDS613_L2N	NC/IO_L2N_613	HDIO BANK 613	N39	IO,1.8V	HDIO BANK 613 IO 02 signal.
A95	HDIO_L40_LVDS613_L6P_HDGC	NC/IO_L6P_HDGC_613	HDIO BANK 613	L40	IO,1.8V	HDIO BANK 613 IO 06 signal.
A96	HDIO_K41_LVDS613_L6N_HDGC	NC/IO_L6N_HDGC_613	HDIO BANK 613	K41	IO,1.8V	HDIO BANK 613 IO 06 signal.
B67	HDIO_J43_LVDS613_L9P	NC/IO_L9P_613	HDIO BANK 613	J43	IO,1.8V	HDIO BANK 613 IO 09 signal.
B68	HDIO_J42_LVDS613_L9N	NC/IO_L9N_613	HDIO BANK 613	J42	IO,1.8V	HDIO BANK 613 IO 09 signal.
B79	HDIO_L41_LVDS613_L7P	NC/IO_L7P_613	HDIO BANK 613	L41	IO,1.8V	HDIO BANK 613 IO 07 signal.
B80	HDIO_K42_LVDS613_L7N	NC/IO_L7N_613	HDIO BANK 613	K42	IO,1.8V	HDIO BANK 613 IO 07 signal.
B83	HDIO_L43_LVDS613_L8P	NC/IO_L8P_613	HDIO BANK 613	L43	IO,1.8V	HDIO BANK 613 IO 08 signal.
B84	HDIO_K43_LVDS613_L8N	NC/IO_L8N_613	HDIO BANK 613	K43	IO,1.8V	HDIO BANK 613 IO 08 signal.
B95	HDIO_L39_LVDS613_L5P_HDGC	NC/IO_L5P_HDGC_613	HDIO BANK 613	L39	IO,1.8V	HDIO BANK 613 IO 05 signal.
B96	HDIO_K40_LVDS613_L5N_HDGC	NC/IO_L5N_HDGC_613	HDIO BANK 613	K40	IO,1.8V	HDIO BANK 613 IO 05 signal.
C71	HDIO_N40_LVDS613_L3P	NC/IO_L3P_613	HDIO BANK 613	N40	IO,1.8V	HDIO BANK 613 IO 03 signal.
C72	HDIO_M39_LVDS613_L3N	NC/IO_L3N_613	HDIO BANK 613	M39	IO,1.8V	HDIO BANK 613 IO 03 signal.
C83	HDIO_N41_LVDS613_L4P	NC/IO_L4P_613	HDIO BANK 613	N41	IO,1.8V	HDIO BANK 613 IO 04 signal.
C84	HDIO_M41_LVDS613_L4N	NC/IO_L4N_613	HDIO BANK 613	M41	IO,1.8V	HDIO BANK 613 IO 04 signal.

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D71	HDIO_R40_LVDS613_L1P	NC/IO_L1P_613	HDIO BANK 613	R40	IO,1.8V	HDIO BANK 613 IO 01 signal.
D72	HDIO_P39_LVDS613_L1N	NC/IO_L1N_613	HDIO BANK 613	P39	IO,1.8V	HDIO BANK 613 IO 01 signal.
D83	HDIO_R41_LVDS613_L0P	NC/IO_L0P_613	HDIO BANK 613	R41	IO,1.8V	HDIO BANK 613 IO 00 signal.
D84	HDIO_P40_LVDS613_L0N	NC/IO_L0N_613	HDIO BANK 613	P40	IO,1.8V	HDIO BANK 613 IO 00 signal.

2.5.1.6 GTM Bank 107 High Speed Transceiver

The Versal Premium SOM supports 4 GTM transceiver Lanes through one transceiver Bank 107 These transceivers can be used to interface to multiple high-speed interface protocols. Each GTM transceiver quad supports two dedicated reference clock input pairs.

For more details on GTM transceiver pinouts on Board-to-Board Connector 1, refer the below table.

Important Note: Bank 107 is only supported in VP1402 and VP1102 devices, these pins are NC in other devices.

Table 13: GTM Bank 107 Transceiver Board to board Connector 1 Pin outs

B2B-1 Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A75	GTM_TXP3_107	NC/GTM_TXP3_107	GTM_BANK 107	Y5	O, DIFF	GTM Bank107 channel3 High speed differential Transmitter positive.
A76	GTM_TXN3_107	NC/GTM_TXN3_107	GTM_BANK 107	Y4	O, DIFF	GTM Bank107 channel3 High speed differential Transmitter negative.
A91	GTM_RXP3_107	NC/GTM_RXP3_107	GTM_BANK 107	N2	I, DIFF	GTM Bank107 channel3 High speed differential receiver Positive.
A92	GTM_RXN3_107	NC/GTM_RXN3_107	GTM_BANK 107	N1	I, DIFF	GTM Bank107 channel3 High speed differential receiver negative.
B75	GTM_TXP2_107	NC/GTM_TXP2_107	GTM_BANK 107	AA7	O, DIFF	GTM Bank107 channel2 High speed differential Transmitter positive.
B76	GTM_TXN2_107	NC/GTM_TXN2_107	GTM_BANK 107	AA6	O, DIFF	GTM Bank107 channel2 High speed differential Transmitter negative.
B91	GTM_RXP2_107	NC/GTM_RXP2_107	GTM_BANK 107	R2	I, DIFF	GTM Bank107 channel2 High speed differential receiver Positive.
B92	GTM_RXN2_107	NC/GTM_RXN2_107	GTM_BANK 107	R1	I, DIFF	GTM Bank107 channel2 High speed differential receiver negative.
C75	GTM_TXP1_107	NC/GTM_TXP1_107	GTM_BANK 107	AB9	O, DIFF	GTM Bank107 channel1 High speed differential Transmitter positive.
C76	GTM_TXN1_107	NC/GTM_TXN1_107	GTM_BANK 107	AB8	O, DIFF	GTM Bank107 channel1 High speed differential Transmitter negative.
C91	GTM_RXP1_107	NC/GTM_RXP1_107	GTM_BANK 107	T4	I, DIFF	GTM Bank107 channel1 High speed differential receiver Positive.
C92	GTM_RXN1_107	NC/GTM_RXN1_107	GTM_BANK 107	T3	I, DIFF	GTM Bank107 channel1 High speed differential receiver negative.

D75	GTM_TXP0_107	NC/GTM_TXP0_107	GTM_BANK 107	AC7	O, DIFF	GTM Bank107 channel0 High speed differential Transmitter Positive.
D76	GTM_TXN0_107	NC/GTM_TXN0_107	GTM_BANK 107	AC6	O, DIFF	GTM Bank107 channel0 High speed differential Transmitter negative.
D91	GTM_RXP0_107	NC/GTM_RXP0_107	GTM_BANK 107	U2	I, DIFF	GTM Bank107 channel0 High speed differential receiver positive.
D92	GTM_RXN0_107	NC/GTM_RXN0_107	GTM_BANK 107	U1	I, DIFF	GTM Bank107 channel0 High speed differential receiver negative.
D95	GTM_REFCLK0P_107	NC/GTM_REFCLKN0_107	GTM_BANK 107	V8	I, DIFF	GTM Bank107 channel0 High speed differential Reference Clock Positive.
D96	GTM_REFCLK0N_107	NC/GTM_REFCLKP0_107	GTM_BANK 107	V9	I, DIFF	GTM Bank107 channel0 High speed differential Reference Clock negative.
D59	GTM_REFCLK1P_107	NC/GTM_REFCLKN1_107	GTM_BANK 107	U10	I, DIFF	GTM Bank107 channel1 High speed differential Reference Clock positive.
D60	GTM_REFCLK1N_107	NC/GTM_REFCLKP1_107	GTM_BANK 107	U11	I, DIFF	GTM Bank107 channel1 High speed differential Reference Clock negative.

2.5.2 Power and Control Pins

The I/O supply voltages of XPIO BANK 703, XPIO BANK 704, XPIO BANK 705, XPIO BANK 712, HDIO BANK 613/612 is connected to dedicated I/O voltage power pins located in Board-to-Board Connector 1. This connection enables expanded usage options and flexibility for both the carrier board and the end user. XP and HD Bank I/O supply voltages are configurable.

To ensure proper electrical grounding, reduce EMI, and provide mechanical stability between the two boards, ground pins are distributed throughout the Board-to-Board Connectors.

For more details on these ground pins on Board-to-Board Connector 1, refer the below table

Table 14: Power and Control Pinouts of Board to board Connector 1

B2B-1Pin No	B2B Connector 1 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A1	VCCO_XPIO_712	VCCO_712	XPIO BANK 712	H32, J32, K32	Power	PL XPIO BANK 712 Power Supply
B1	VCCO_XPIO_705	VCCO_705	XPIO BANK 705	BC26, BD26, BD27	Power	PL XPIO BANK 705 Power Supply
C1	VCCO_XPIO_704	VCCO_704	XPIO BANK 704	BC22, BD22, BE22	Power	PL XPIO BANK 704 Power Supply
D1	VCCO_XPIO_703	VCCO_703	XPIO BANK 703	BC18, BD18, BD19	Power	PL XPIO BANK 703 Power Supply
B99, B100	VCCO_HDIO	VCCO_613, VCCO_612	HDIO BANK 613, HDIO BANK 612	J41, M40, Y39, U40	Power	PL HDIO BANK 613, HDIO BANK 612 Power Supply
A8, A15, A22, A29, A36, A43, A50, A57, A58, A61, A62, A65, A66, A69, A70, A73, A74, A77, A78, A89, A90, A81, A82, A85, A86, A93, A94, A97, A98, B8, B15 B22, B29, B36, B43, B50, B57, B58, B61, B62, B65, B66, B69, B70, B73, B74, B77, B78, B81, B82, B85, B86, B89, B90, B93, B94, B97, B98, C8, C15, C22, C29, C36, C43, C50 C57, C58, C61, C62 C65, C66, C69, C70, C73, C74, C77, C78, C81 C82, C85, C86, C89, C90, C93, C94, C97, C98, D8, D15, D22, D29, D36, D43, D50, D57, D58, D61, D62, D65, D66, D69, D70, D73, D74, D77, D78 ,D81, D82, D85, D86, D89, D90, D93, D94, D97, D98.	GND	NA	NA	NA	Power	Ground.

2.6 Board-to-Board Connector 2

The Versal Premium SOM supports interfaces of PS such USB, Ethernet, RGMII, UART and I2C through 400 pin board to board connector2(J4). Also, this connector supports PL interfaces such as High-speed transceiver channels and their reference clocks.

The pinout for Board-to-Board Connector-2 on the Versal premium SOM is provided in the table below, and the available interfaces are explained in the following sections. Board-to-Board Connector-2 is located on the bottom side of the SOM, as shown in the diagram below.

Number of Pins	- 400
Connector Part Number	- ASP-209946-01 from Samtec
Mating Connector	- ASP-214802-01 from Samtec
Staking Height	- 5mm

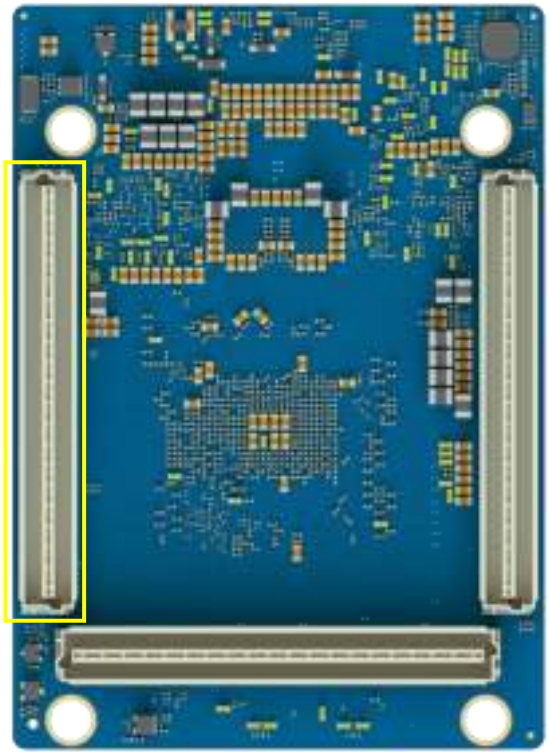


Figure 5: Board-to-Board Connector 2

Table 15: Board-to-Board Connector 2 Pinout

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	VCC_12V	B1	VCC_12V	C1	VCC_12V	D1	VCC_12V
A2	VCC_12V	B2	VCC_12V	C2	VCC_12V	D2	VCC_12V
A3	VCC_12V	B3	VCC_12V	C3	VCC_12V	D3	VCC_12V
A4	VCC_12V	B4	VCC_12V	C4	VCC_12V	D4	VCC_12V
A5	VCC_12V	B5	VCC_12V	C5	VCC_12V	D5	VCC_12V
A6	VCC_12V	B6	VCC_12V	C6	VCC_12V	D6	VCC_12V
A7	VCC_12V	B7	VCC_12V	C7	VCC_12V	D7	VCC_12V
A8	VCC_12V	B8	VCC_12V	C8	VCC_12V	D8	VCC_12V
A9	GND	B9	GND	C9	GND	D9	GND
A10	GND	B10	GND	C10	GND	D10	GND
A11	NC	B11	SOM_PWR_EN	C11	VSTBY (5V)	D11	10M_CLK_OUT
A12	JTAG_TCK	B12	SOM_PWR_OK	C12	VRTC_3V	D12	1PPS_CLK_OUT
A13	JTAG_TMS	B13	B_RST_OUT(XP_BE20_LVDS703_L25P)	C13	PS_MODE0	D13	NC
A14	JTAG_TDO	B14	RESET_SW_IN	C14	PS_MODE1	D14	B_D_INT(XP_BE21_LVDS703_L26P)
A15	JTAG_TDI	B15	CONFIG_DONE	C15	PS_MODE2	D15	PWRBTN#
A16	GND	B16	GND	C16	GND	D16	GND
A17	SD1_CLK(PMC_MIO26_501)	B17	SPI1_CLK(PMC_MIO6_500)	C17	GEM1_TX_CLK(LPD_MIO12_502)	D17	GEM1_RX_CLK(LPD_MIO18_502)
A18	SD1_CMD(PMC_MIO29_501)	B18	SPI1_SI(PMC_MIO11_500)	C18	GEM1_TXD0(LPD_MIO13_502)	D18	GEM1_RXD0(LPD_MIO19_502)
A19	SD1_DATA0(PMC_MIO30_501)	B19	SPI1_SO(PMC_MIO10_500)	C19	GEM1_TXD1(LPD_MIO14_502)	D19	GEM1_RXD1(LPD_MIO20_502)
A20	SD1_DATA1(PMC_MIO31_501)	B20	SPI1_CS2(PMC_MIO7_500)	C20	GEM1_TXD2(LPD_MIO15_502)	D20	GEM1_RXD2(LPD_MIO21_502)
A21	SD1_DATA2(PMC_MIO32_501)	B21	SPI1_CS1(PMC_MIO8_500)	C21	GEM1_TXD3(LPD_MIO16_502)	D21	GEM1_RXD3(LPD_MIO22_502)
A22	SD1_DATA3(PMC_MIO33_501)	B22	SPI1_CS0(PMC_MIO9_500)	C22	GEM1_TX_CTL(LPD_MIO17_502)	D22	GEM1_RX_CTL(LPD_MIO23_502)
A23	GND	B23	GND	C23	GND	D23	GND
A24	SD1_CD(PMC_MIO28_501)	B24	ETH2_INT(PMC_MIO12_500)	C24	GEM1_MDC(LPD_MIO24_502)	D24	CANFD1_RX(PMC_MIO37_501)
A25	GPIO(PMC_MIO27_501)	B25	10MHZ_B2B_IN	C25	GEM1_MDIO(LPD_MIO25_502)	D25	CANFD1_TX(PMC_MIO36_501)
A26	B_I2C0_SCL(XP_BE29_LVDS705_L25P)	B26	1PPS_B2B_IN	C26	HS_PCIE_RSTN	D26	NC
A27	B_I2C0_SDA(XP_BF28_LVDS705_L25N)	B27	NC	C27	B_LS_RST(XP_BD23_LVDS704_L25P)	D27	NC
A28	I2C_SCL(PMC_MIO50_501)	B28	NC	C28	GND	D28	GND
A29	I2C_SDA(PMC_MIO51_501)	B29	NC	C29	GTYP_TXP0_106	D29	GTYP_RXP0_106
A30	UART_TXD(PMC_MIO35_501)	B30	NC	C30	GTYP_TXN0_106	D30	GTYP_RXN0_106
A31	UART_RXD(PMC_MIO34_501)	B31	VBUS_USB	C31	GND	D31	GND
A32	GPHY_ACTIVITY_LED2	B32	USB_PWR_EN	C32	GTYP_TXP1_106	D32	GTYP_RXP1_106
A33	GPHY_LINK_LED1	B33	USB_OTG_ID	C33	GTYP_TXN1_106	D33	GTYP_RXN1_106
A34	GND	B34	GND	C34	GND	D34	GND
A35	GPHY_DTXRXM	B35	USB_OTG_DM	C35	GTYP_TXP2_106	D35	GTYP_RXP2_106
A36	GPHY_DTXRXP	B36	USB_OTG_DP	C36	GTYP_TXN2_106	D36	GTYP_RXN2_106

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A37	GND	B37	GND	C37	GND	D37	GND
A38	GPHY_CTXRXM	B38	NC	C38	GTYP_TXP3_106	D38	GTYP_RXP3_106
A39	GPHY_CTXRXP	B39	NC	C39	GTYP_TXN3_106	D39	GTYP_RXN3_106
A40	GND	B40	GND	C40	GND	D40	GND
A41	GPHY_BTXRXM	B41	SYS_SYNC_XP_BE32_LVDS706_L24P	C41	GTYP_REFCLK0P_106	D41	B2B_GTYP_REFCLK1P_106
A42	GPHY_BTXRXP	B42	SYS_SYNC_XP_BE33_LVDS706_L24N	C42	GTYP_REFCLK0N_106	D42	B2B_GTYP_REFCLK1N_106
A43	GND	B43	GND	C43	GND	D43	GND
A44	GPHY_ATXRXM	B44	SYS_SYNC_CLK_INP	C44	NC	D44	NC
A45	GPHY_ATXRXP	B45	SYS_SYNC_CLK_INN	C45	NC	D45	NC
A46	GND	B46	GND	C46	GND	D46	GND
A47	GTM_TXP0_202	B47	GTM_RXP0_202	C47	GTYP_TXP0_110	D47	GTYP_RXP0_110
A48	GTM_TXN0_202	B48	GTM_RXN0_202	C48	GTYP_TXN0_110	D48	GTYP_RXN0_110
A49	GND	B49	GND	C49	GND	D49	GND
A50	GTM_TXP1_202	B50	GTM_RXP1_202	C50	GTYP_TXP1_110	D50	GTYP_RXP1_110
A51	GTM_TXN1_202	B51	GTM_RXN1_202	C51	GTYP_TXN1_110	D51	GTYP_RXN1_110
A52	GND	B52	GND	C52	GND	D52	GND
A53	GTM_TXP2_202	B53	GTM_RXP2_202	C53	GTYP_TXP2_110	D53	GTYP_RXP2_110
A54	GTM_TXN2_202	B54	GTM_RXN2_202	C54	GTYP_TXN2_110	D54	GTYP_RXN2_110
A55	GND	B55	GND	C55	GND	D55	GND
A56	GTM_TXP3_202	B56	GTM_RXP3_202	C56	GTYP_TXP3_110	D56	GTYP_RXP3_110
A57	GTM_TXN3_202	B57	GTM_RXN3_202	C57	GTYP_TXN3_110	D57	GTYP_RXN3_110
A58	GND	B58	GND	C58	GND	D58	GND
A59	GTM_REFCLK0P_202	B59	B2B_GTM_REFCLK1P_202	C59	GTYP_REFCLK0P_110	D59	B2B_GTYP_REFCLK1P_110
A60	GTM_REFCLK0N_202	B60	B2B_GTM_REFCLK1N_202	C60	GTYP_REFCLK0N_110	D60	B2B_GTYP_REFCLK1N_110
A61	GND	B61	GND	C61	GND	D61	GND
A62	GTYP_LPD_TXP0_102	B62	GTYP_LPD_RXP0_102	C62	GTYP_LPD_TXP0_103	D62	GTYP_LPD_RXP0_103
A63	GTYP_LPD_TXN0_102	B63	GTYP_LPD_RXN0_102	C63	GTYP_LPD_TXN0_103	D63	GTYP_LPD_RXN0_103
A64	GND	B64	GND	C64	GND	D64	GND
A65	GTYP_LPD_TXP1_102	B65	GTYP_LPD_RXP1_102	C65	GTYP_LPD_TXP1_103	D65	GTYP_LPD_RXP1_103
A66	GTYP_LPD_TXN1_102	B66	GTYP_LPD_RXN1_102	C66	GTYP_LPD_TXN1_103	D66	GTYP_LPD_RXN1_103
A67	GND	B67	GND	C67	GND	D67	GND
A68	GTYP_LPD_TXP2_102	B68	GTYP_LPD_RXP2_102	C68	GTYP_LPD_TXP2_103	D68	GTYP_LPD_RXP2_103
A69	GTYP_LPD_TXN2_102	B69	GTYP_LPD_RXN2_102	C69	GTYP_LPD_TXN2_103	D69	GTYP_LPD_RXN2_103
A70	GND	B70	GND	C70	GND	D70	GND
A71	GTYP_LPD_TXP3_102	B71	GTYP_LPD_RXP3_102	C71	GTYP_LPD_TXP3_103	D71	GTYP_LPD_RXP3_103
A72	GTYP_LPD_TXN3_102	B72	GTYP_LPD_RXN3_102	C72	GTYP_LPD_TXN3_103	D72	GTYP_LPD_RXN3_103
A73	GND	B73	GND	C73	GND	D73	GND
A74	CPM5_REFCLK_P	B74	B2B_GTYP_LPD_REFCLK1P_102	C74	GTYP_LPD_REFCLK0P_103	D74	B2B_GTYP_LPD_REFCLK1P_103
A75	CPM5_REFCLK_N	B75	B2B_GTYP_LPD_REFCLK1N_102	C75	GTYP_LPD_REFCLK0N_103	D75	B2B_GTYP_LPD_REFCLK1N_103
A76	GND	B76	GND	C76	GND	D76	GND

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A77	GTYP_LPD_TXP0_104	B77	GTYP_LPD_RXP0_104	C77	GTYP_LPD_TXP0_105	D77	GTYP_LPD_RXP0_105
A78	GTYP_LPD_TXN0_104	B78	GTYP_LPD_RXN0_104	C78	GTYP_LPD_TXN0_105	D78	GTYP_LPD_RXN0_105
A79	GND	B79	GND	C79	GND	D79	GND
A80	GTYP_LPD_TXP1_104	B80	GTYP_LPD_RXP1_104	C80	GTYP_LPD_TXP1_105	D80	GTYP_LPD_RXP1_105
A81	GTYP_LPD_TXN1_104	B81	GTYP_LPD_RXN1_104	C81	GTYP_LPD_TXN1_105	D81	GTYP_LPD_RXN1_105
A82	GND	B82	GND	C82	GND	D82	GND
A83	GTYP_LPD_TXP2_104	B83	GTYP_LPD_RXP2_104	C83	GTYP_LPD_TXP2_105	D83	GTYP_LPD_RXP2_105
A84	GTYP_LPD_TXN2_104	B84	GTYP_LPD_RXN2_104	C84	GTYP_LPD_TXN2_105	D84	GTYP_LPD_RXN2_105
A85	GND	B85	GND	C85	GND	D85	GND
A86	GTYP_LPD_TXP3_104	B86	GTYP_LPD_RXP3_104	C86	GTYP_LPD_TXP3_105	D86	GTYP_LPD_RXP3_105
A87	GTYP_LPD_TXN3_104	B87	GTYP_LPD_RXN3_104	C87	GTYP_LPD_TXN3_105	D87	GTYP_LPD_RXN3_105
A88	GND	B88	GND	C88	GND	D88	GND
A89	TXVR_REFCLK_P	B89	B2B_GTYP_LPD_REFCLK1P_104	C89	GTYP_LPD_REFCLK0P_105	D89	B2B_GTYP_LPD_REFCLK1P_105
A90	TXVR_REFCLK_N	B90	B2B_GTYP_LPD_REFCLK1N_104	C90	GTYP_LPD_REFCLK0N_105	D90	B2B_GTYP_LPD_REFCLK1N_105
A91	GND	B91	GND	C91	GND	D91	GND
A92	GTYP_TXP0_200	B92	GTYP_RXP0_200	C92	GTYP_TXP2_200	D92	GTYP_RXP2_200
A93	GTYP_TXN0_200	B93	GTYP_RXN0_200	C93	GTYP_TXN2_200	D93	GTYP_RXN2_200
A94	GND	B94	GND	C94	GND	D94	GND
A95	GTYP_TXP1_200	B95	GTYP_RXP1_200	C95	GTYP_TXP3_200	D95	GTYP_RXP3_200
A96	GTYP_TXN1_200	B96	GTYP_RXN1_200	C96	GTYP_TXN3_200	D96	GTYP_RXN3_200
A97	GND	B97	GND	C97	GND	D97	GND
A98	GTYP_REFCLK0P_200	B98	B2B_GTYP_REFCLK1P_200	C98	NC	D98	SYSMON_D_VP
A99	GTYP_REFCLK0N_200	B99	B2B_GTYP_REFCLK1N_200	C99	NC	D99	SYSMON_D_VN
A100	GND	B100	GND	C100	GND	D100	GND

Important Note: Bank name and bank number mentioned in this document is with respect to VP1552 Devices.

2.6.1 PS Interfaces

The interfaces which are supported in Board-to-Board Conenector2 from Versal Premium's PS is explained in the following section.

2.6.1.1 USB2.0 OTG Interface

The Versal Premium SOM supports one USB2.0 OTG interface on Board-to-Board Connector 2. USB0 OTG controller of Versal Premium SoC PS is used for USB2.0 OTG interface.

The ULPI interface from PMC MIO is connected to on SOM USB PHY to support the USB2.0 interface. The Versal Premium SOM supports "USB3320" ULPI transceiver and works at 1.8V IO voltage level. In Versal Premium SOM, PMC MIO13 is used for USB ULPI PHY reset. SOM supports active high power enable signal on Board-to-Board Connector 2 from USB PHY for external VBUS power control.

The reference clock for the on-board USB PHY is provided by the on-board clock synthesizer1's OUT1 output, generating a single-ended 24 MHz clock.

Also, Versal Premium SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector 2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 16: USB2.0 OTG Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B36	USB_OTG_DP	-	-	-	IO, USB	USB OTG data negative.
B35	USB_OTG_DM	-	-	-	IO, USB	USB OTG data positive.
B33	USB_OTG_ID	-	-	-	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
B31	VBUS_USB	-	-	-	I, 5V Power	USB active high power enable output to control external USB VBUS.
B32	USB_PWR_EN	-	-	-	O, 3.3V CMOS	USB active high power enable output to control external USB VBUS.

2.6.1.2 Gigabit Ethernet Interface

The Versal Premium SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector 2. The MAC is integrated in the Versal Premium PS and connected to the external Gigabit Ethernet PHY "88E1512" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of SOC through LPD MIO pins and works at 1.8V IO voltage level. The reference clock for the on-board Ethernet PHY is provided by the on-board clock synthesize1's OUT2 output, generating a single-ended 25 MHz clock.

In Versal premium SOM, IO of XPIO Bank 703 "IO_L25N_N8P3_M1P51_703" is used for Ethernet PHY reset. Also, SOM supports Ethernet PHY interrupt through IO of XPIO Bank 703 "IO_L26N_N8P5_M1P53_703". This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector 2.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 17: Gigabit Ethernet Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A44	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 0 negative.
A45	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 0 positive.
A41	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
A42	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
A38	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
A39	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
A35	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
A36	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
A32	GPHY_ACTIVITY_LED2	NA	NA	NA	O, 1.8V CMOS	Gigabit Ethernet Activity LED.
A33	GPHY_LINK_LED1	NA	NA	NA	O, 1.8V CMOS	Gigabit Ethernet 1000Mbps Link status LED.

2.6.1.3 SD/SDIO Interface

The Versal premium SOM supports SD/SDIO interface on Board-to-Board Connector2. The SD1 controller of Versal's is used for SD/SDIO interface through PMC MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (25MHz), High Speed mode (50MHz), SDR12 (25MHz), SDR25 (50MHz), SDR50 (100MHz), SDR104 (200MHz) & DDR50 mode (50MHz). Also in SD mode, data transfers in 1-bit and 4-bit modes. The Versal premium SOM supports Card Detect & Power Enable/Voltage Select pins through PMC MIO pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 18: SD/SDIO Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A17	SD1_CLK(PMC_MIO26_501)	PMC_MIO 26_501	PMC MIO BANK 501	T16	O, 1.8V LVCMOS/ 4.7K PU	SD1 Clock.
A18	SD1_CMD(PMC_MIO29_501)	PMC_MIO 29_501	PMC MIO BANK 501	M16	IO, 1.8V LVCMOS/ 10K PU	SD1 Command.
A19	SD1_DATA0(PMC_MIO30_501)	PMC_MIO 30_501	PMC MIO BANK 501	L16	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA0.
A20	SD1_DATA1(PMC_MIO31_501)	PMC_MIO 31_501	PMC MIO BANK 501	K16	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA1.
A21	SD1_DATA2(PMC_MIO32_501)	PMC_MIO 32_501	PMC MIO BANK 501	M17	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA2.
A22	SD1_DATA3(PMC_MIO33_501)	PMC_MIO 33_501	PMC MIO BANK 501	N17	IO, 1.8V LVCMOS/ 10K PU	SD1 DATA3.
A24	SD1_CD(PMC_MIO28_501)	PMC_MIO 28_501	PMC MIO BANK 501	N16	I, 1.8V LVCMOS/ 10K PU	SD1 Card Detect.
A25	GPIO(PMC_MIO 27_501)	PMC_MIO 27_501	PMC MIO BANK 501	R16	O, 1.8V LVCMOS/ 4.7K PU	SD1 Power Enable/Voltage select through PS GPIO.

2.6.1.4 RGMII Interface

The Versal Premium SOM supports RGMII interface on Board-to-Board Connector 2. This RGMII is from GEM1 interface of Versal's LPD through MIO pins and works at 1.8V IO voltage level. Those LPD MIO pins are directly connected from Versal SoC to Board-to-Board conenctor2. Please refer PS Min Multiplexing section for available alternate functions.

The Versal Premium gigabit Ethernet controller (GEM) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through LPD Bank IOs through MIO interface in SOM.

For more details on RGMII Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 19: RGMII Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C17	GEM1_TX_CLK(LPD_MIO12_502)	LPD_MIO12_502	LPD MIO BANK 502	J18	O, 1.8V LVCMOS	GEM1 RGMII Transmit Clock. Or USB1 ULPI Clock.
C18	GEM1_TXD0(LPD_MIO13_502)	LPD_MIO13_502	LPD MIO BANK 502	K18	O, 1.8V LVCMOS	GEM1 RGMII Transmit DATA0. Or USB1 ULPI Direction Control.
C19	GEM1_TXD1(LPD_MIO14_502)	LPD_MIO14_502	LPD MIO BANK 502	L18	O, 1.8V LVCMOS	GEM1 RGMII Transmit DATA1. Or USB1 ULPI Bi-Directional Data2.
C20	GEM1_TXD2(LPD_MIO15_502)	LPD_MIO15_502	LPD MIO BANK 502	L19	O, 1.8V LVCMOS	GEM1 RGMII Transmit DATA2. Or USB1 ULPI NXT.
C21	GEM1_TXD3(LPD_MIO16_502)	LPD_MIO16_502	LPD MIO BANK 502	J19	O, 1.8V LVCMOS	GEM1 RGMII Transmit DATA3. Or USB1 ULPI Bi-Directional Data0.
C22	GEM1_TX_CTL(LPD_MIO17_502)	LPD_MIO17_502	LPD MIO BANK 502	H19	O, 1.8V LVCMOS	GEM1 RGMII Transmit Control. Or USB1 ULPI Bi-Directional Data1.
D17	GEM1_RX_CLK(LPD_MIO18_502)	LPD_MIO18_502	LPD MIO BANK 502	G19	I, 1.8V LVCMOS	GEM1 RGMII Receive Clock. Or USB1 ULPI STP.
D18	GEM1_RXD0(LPD_MIO19_502)	LPD_MIO19_502	LPD MIO BANK 502	F19	I, 1.8V LVCMOS	GEM1 RGMII Receive DATA0. Or USB1 ULPI Bi-Directional Data3.
D19	GEM1_RXD1(LPD_MIO20_502)	LPD_MIO20_502	LPD MIO BANK 502	E20	I, 1.8V LVCMOS	GEM1 RGMII Receive DATA1. Or USB1 ULPI Bi-Directional Data4.
D20	GEM1_RXD2(LPD_MIO21_502)	LPD_MIO21_502	LPD MIO BANK 502	F20	I, 1.8V LVCMOS	GEM1 RGMII Receive DATA2. Or USB1 ULPI Bi-Directional Data5.
D21	GEM1_RXD3(LPD_MIO22_502)	LPD_MIO22_502	LPD MIO BANK 502	H20	I, 1.8V LVCMOS	GEM1 RGMII Receive DATA3. Or USB1 ULPI Bi-Directional Data6.
D22	GEM1_RX_CTL(LPD_MIO23_502)	LPD_MIO23_502	LPD MIO BANK 502	J20	I, 1.8V LVCMOS	GEM1 RGMII Receive control. Or USB1 ULPI Bi-Directional Data7.
C24	GEM1_MDC(LPD_MIO24_502)	LPD_MIO24_502	LPD MIO BANK 502	K20	O, 1.8V LVCMOS	MDC Clock Output
C25	GEM1_MDIO(LPD_MIO25_502)	LPD_MIO25_502	LPD MIO BANK 502	L20	IO, 1.8V LVCMOS	MDIO Data In/Out

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B24	ETH2_INT(PMC_MIO12_500)	PMC_MIO12_500	PMC MIO BANK 500	N14	I, 1.8V LVCMOS	GEM1 Interrupt Input. This pin is multiplexed with SD1 Write protect.

2.6.1.5 SPI Interface

The Versal Premium SOM supports one SPI interface with three chip select pins on Board-to-Board Connector 2. The SPI1 controller of Versal's PS is used for SPI interface through PMC MIO pins. It can function in master mode with multi-master feature, slave mode, or loop-back test mode. .

For more details on SPI Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 20: SPI Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/Termination	Description
B17	SPI1_CLK(PMC_MIO6_500)	PMC_MIO6_500	PMC MIO BANK 500	T13	O, 1.8V LVCMOS	SPI Clock output pin. In slave mode, this pin is input to SOM.
B18	SPI1_SI(PMC_MIO11_500)	PMC_MIO11_500	PMC MIO BANK 500	P14	O, 1.8V LVCMOS	SPI Master Output Slave Input pin. In slave mode, this pin is input to SOM.
B19	SPI1_SO(PMC_MIO10_500)	PMC_MIO10_500	PMC MIO BANK 500	T14	I, 1.8V LVCMOS	SPI Master input slave output pin. In slave mode, this pin is input to SOM.
B20	SPI1_CS2(PMC_MIO7_500)	PMC_MIO7_500	PMC MIO BANK 500	U13	O, 1.8V LVCMOS	SPI Chip select2.
B21	SPI1_CS1(PMC_MIO8_500)	PMC_MIO8_500	PMC MIO BANK 500	V14	O, 1.8V LVCMOS	SPI Chip select1.
B22	SPI1_CS0(PMC_MIO9_500)	PMC_MIO9_500	PMC MIO BANK 500	U14	IO, 1.8V LVCMOS	SPI Chip select0. This chip select can be used for both master or slave mode.

2.6.1.6 Debug UART Interface

The Versal Premium SOM supports one Debug UART interface on Board-to-Board Connector 2. The UART0 controller of SoC's PS is used for Debug UART interface through PMC MIO pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector 2, refer the below table.

Table 21: Debug UART pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A30	UART_TXD(PMC_MIO35_501)	PMC_MIO35_501	PMC MIO BANK 501	R17	O, 1.8V LVCMOS	UART Transmit data line for Debug.
A31	UART_RXD(PMC_MIO34_501)	PMC_MIO34_501	PMC MIO BANK 501	P17	I, 1.8V LVCMOS	UART Receive data line for Debug.

2.6.1.7 I2C Interface

The Versal Premium SOM supports two I2C interface on Board-to-Board Connector 2 I2C0 & I2C1. The I2C1 is from Versal's PS is used for I2C interface through PMC MIO pins. The controller supports multi-master mode for 7-bit and extended 10-bit addressing and also supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C1 interface is also connected to On-SOM PMIC with I2C address 0x58h, 0x59h, On-SOM Clock Synthesizer 1 with 0x70h, Clock Synthesizer 2 with 0x74h, Clock Synthesizer 3 with 0x75h, MPS Controller with 0x60h and EEPROM with 0x52h, 0x5Ah, 0x32h addresses in the Versal Premium SOM. This PMC I2C is connected to I2C1 port of board-to-board connector. I2C0 is from versal's LPD controller and it is supported via EMIO.

For more details on I2C Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 22: I2C Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A26	B_I2C0_SCL(XP_BE29_LVDS705_L25P)	IO_L25P_N8P2_M1P158_705	XPIO Bank 705	BE29	O, 1.8V	I2C0 data.
A27	B_I2C0_SDA(XP_BF28_LVDS705_L25N)	IO_L25N_N8P3_M1P159_705	XPIO Bank 705	BF28	IO, 1.8V	I2C0 clock.
A28	I2C_SCL(PMC_MIO50_501)	PMC_MIO50_501	PMC MIO BANK 501	V19	O, 1.8V LVCMOS/ 4.7K PU	I2C1 Clock
A29	I2C_SDA(PMC_MIO51_501)	PMC_MIO51_501	PMC MIO BANK 501	N20	IO, 1.8V LVCOMS/ 4.7K PU	I2C1 Data

2.6.1.8 CAN Interface

The Versal Premium SOM supports one CAN interfaces on Board-to-Board Connector 2. one CAN FD (CAN Flexible Data-Rate) interfaces on Board-to-Board Connector2. The CAN FD1 controller of Versal's PS is used for CAN FD interface through PMC MIO pins. This CAN FD controller is compatible with CAN 2.0 frames specified in ISO specification 11898-1:2015 standards. And it supports flexible data rates up to 8Mb/s and normal data rates up to 1Mb/s.

If CAN interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section for available alternate functions.

For more details on CAN Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 23: CAN Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D24	CANFD1_RX(PMC_MIO37_501)	PMC_MIO37_501	PMC MIO BANK 501	V17	I, 1.8V LVCMOS	CAN0 Receive Data,
D25	CANFD1_TX(PMC_MIO36_501)	PMC_MIO36_501	PMC MIO BANK 501	U17	O, 1.8V LVCMOS	CAN0 Transmit Data.

2.6.1.9 JTAG Interface

The Versal Premium SOM supports JTAG interface on Board-to-Board Connector 2. The Versal Premium's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Versal Premium.

For more details on JTAG Interface pinouts on Board-to-Board Connector 2, refer the below table.

Table 24: JTAG Interface pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A12	JTAG_TCK	TCK_503	PMC DIO BANK 503	B19	I, 1.8V LVCMOS/ 4.7K PU	JTAG Test Clock.
A13	JTAG_TMS	TMS_503	PMC DIO BANK 503	B16	I, 1.8V LVCMOS/ 4.7K PU	JTAG Test Mode Select.
A14	JTAG_TDO	TDO_503	PMC DIO BANK 503	B17	O, 1.8V LVCMOS	JTAG Test Data Output.
A15	JTAG_TDI	TDI_503	PMC DIO BANK 503	B18	I, 1.8V LVCMOS PU	JTAG Test Data Input.

2.6.2 PL Interfaces

The interfaces which are supported in Board-to-Board Connector 2 from Versal Premium's PL is explained in the following section.

2.6.2.1 GTM High speed Transceivers

The Versal Premium supports GTM transceiver Lanes through transceiver Bank 202 in board to board connector 2. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTM transceiver quad supports two dedicated reference clock input pairs.

For more details on GTM transceiver pinouts on Board-to-Board Connector 2, refer the below table.

Table 25: GTM transceiver pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A47	GTM_TXP0_202	GTM_TXP0_202	GTM_BANK 202	BG45	O, DIFF	GTM Bank202 channel0 High speed differential Transmitter positive.
A48	GTM_TXN0_202	GTM_TXN0_202	GTM_BANK 202	BH45	O, DIFF	GTM Bank202 channel0 High speed differential Transmitter negative.
A50	GTM_TXP1_202	GTM_TXP1_202	GTM_BANK 202	BG47	O, DIFF	GTM Bank202 channel1 High speed differential Transmitter Positive.
A51	GTM_TXN1_202	GTM_TXN1_202	GTM_BANK 202	BH47	O, DIFF	GTM Bank202 channel1 High speed differential Transmitter negative.
A53	GTM_TXP2_202	GTM_TXP2_202	GTM_BANK 202	BJ48	O, DIFF	GTM Bank202 channel2 High speed differential Transmitter positive.
A54	GTM_TXN2_202	GTM_TXN2_202	GTM_BANK 202	BK48	O, DIFF	GTM Bank202 channel2 High speed differential Transmitter negative.
A56	GTM_TXP3_202	GTM_TXP3_202	GTM_BANK 202	BF49	O, DIFF	GTM Bank202 channel3 High speed differential Transmitter Positive.

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A57	GTM_TXN3_202	GTM_TXN3_202	GTM_BANK 202	BF50	O, DIFF	GTM Bank202 channel3 High speed differential Transmitter negative.
A59	GTM_REFCLK0P_202	GTM_REFCLKP0_202	GTM_BANK 202	AJ47	I, DIFF	GTM Bank202 channel0 High speed differential Reference Clock Positive.
A60	GTM_REFCLK0N_202	GTM_REFCLKN0_202	GTM_BANK 202	AJ48	I, DIFF	GTM Bank202 channel0 High speed differential Reference Clock negative.
B47	GTM_RXP0_202	GTM_RXP0_202	GTM_BANK 202	BM49	I, DIFF	GTM Bank202 channel0 High speed differential Receiver positive.
B48	GTM_RXN0_202	GTM_RXN0_202	GTM_BANK 202	BN49	I, DIFF	GTM Bank202 channel0 High speed differential Receiver negative.
B50	GTM_RXP1_202	GTM_RXP1_202	GTM_BANK 202	BK50	I, DIFF	GTM Bank202 channel1 High speed differential Receiver positive.
B51	GTM_RXN1_202	GTM_RXN1_202	GTM_BANK 202	BK51	I, DIFF	GTM Bank202 channel1 High speed differential Receiver negative.
B53	GTM_RXP2_202	GTM_RXP2_202	GTM_BANK 202	BJ52	I, DIFF	GTM Bank202 channel2 High speed differential Receiver positive.
B54	GTM_RXN2_202	GTM_RXN2_202	GTM_BANK 202	BJ53	I, DIFF	GTM Bank202 channel2 High speed differential Receiver negative.
B56	GTM_RXP3_202	GTM_RXP3_202	GTM_BANK 202	BH50	I, DIFF	GTM Bank202 channel3 High speed differential Receiver positive.
B57	GTM_RXN3_202	GTM_RXN3_202	GTM_BANK 202	BH51	I, DIFF	GTM Bank202 channel3 High speed differential Receiver negative.

2.6.2.2 GTYP LPD Bank High Speed Transceiver

The Versal Premium supports 16 GTYP LPD transceiver Lanes through four transceiver Banks. These GTYP LPD transceivers bank used to supports only PCIe Gen5 through CPM5 controller. Each GTYP LPD transceiver quad supports two dedicated reference clock input pairs.

For more details on GTYP transceiver pinouts on Board-to-Board Connector 2, refer the below table.

Table 26: GTYP LPD transceiver bank pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank102 Transceiver Quad Pins						
A62	GTYP_LPD_TXP0_102	GTYP_LPD_TXP0_102	GTYP_BANK102	BG7	O, DIFF	Low power domain GTYP Bank 102 channel 0 High speed differential Transmitter positive
A63	GTYP_LPD_TXN0_102	GTYP_LPD_TXN0_102	GTYP_BANK102	BG6	O, DIFF	Low power domain GTYP Bank 102 channel 0 High speed differential Transmitter Negative
A65	GTYP_LPD_TXP1_102	GTYP_LPD_TXP1_102	GTYP_BANK102	BF5	O, DIFF	Low power domain GTYP Bank 102 channel 1 High speed differential Transmitter positive
A66	GTYP_LPD_TXN1_102	GTYP_LPD_TXN1_102	GTYP_BANK102	BF4	O, DIFF	Low power domain GTYP Bank 102 channel 1 High speed differential Transmitter Negative
A68	GTYP_LPD_TXP2_102	GTYP_LPD_TXP2_102	GTYP_BANK102	BE7	O, DIFF	Low power domain GTYP Bank 102 channel 2 High speed differential Transmitter positive
A69	GTYP_LPD_TXN2_102	GTYP_LPD_TXN2_102	GTYP_BANK102	BE6	O, DIFF	Low power domain GTYP Bank 102 channel 2 High speed differential Transmitter Negative
A71	GTYP_LPD_TXP3_102	GTYP_LPD_TXP3_102	GTYP_BANK102	BD5	O, DIFF	Low power domain GTYP Bank 102 channel 3 High speed differential Transmitter positive
A72	GTYP_LPD_TXN3_102	GTYP_LPD_TXN3_102	GTYP_BANK102	BD4	O, DIFF	Low power domain GTYP Bank 102 channel 3 High speed differential Transmitter Negative
B62	GTYP_LPD_RXP0_102	GTYP_LPD_RXP0_102	GTYP_BANK102	BG2	I, DIFF	Low power domain GTYP Bank 102 channel 0 High speed differential Receiver positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B63	GTYP_LPD_RXN0_102	GTYP_LPD_RXN0_102	GTYP_BANK 102	BG1	I, DIFF	Low power domain GTYP Bank 102 channel 0 High speed differential Receiver Negative
B65	GTYP_LPD_RXP1_102	GTYP_LPD_RXP1_102	GTYP_BANK 102	BE2	I, DIFF	Low power domain GTYP Bank 102 channel 1 High speed differential Receiver positive
B66	GTYP_LPD_RXN1_102	GTYP_LPD_RXN1_102	GTYP_BANK 102	BE1	I, DIFF	Low power domain GTYP Bank 102 channel 1 High speed differential Receiver Negative
B68	GTYP_LPD_RXP2_102	GTYP_LPD_RXP2_102	GTYP_BANK 102	BC2	I, DIFF	Low power domain GTYP Bank 102 channel 2 High speed differential Receiver positive
B69	GTYP_LPD_RXN2_102	GTYP_LPD_RXN2_102	GTYP_BANK 102	BC1	I, DIFF	Low power domain GTYP Bank 102 channel 2 High speed differential Receiver Negative
B71	GTYP_LPD_RXP3_102	GTYP_LPD_RXP3_102	GTYP_BANK 102	BB4	I, DIFF	Low power domain GTYP Bank 102 channel 3 High speed differential Receiver positive
B72	GTYP_LPD_RXN3_102	GTYP_LPD_RXN3_102	GTYP_BANK 102	BB3	I, DIFF	Low power domain GTYP Bank 102 channel 3 High speed differential Receiver Negative
Bank103 Transceiver Quad Pins						
C62	GTYP_LPD_TXP0_103	GTYP_LPD_TXP0_103	GTYP_BANK 103	BC7	O, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Transmitter positive
C63	GTYP_LPD_TXN0_103	GTYP_LPD_TXN0_103	GTYP_BANK 103	BC6	O, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Transmitter Negative
C65	GTYP_LPD_TXP1_103	GTYP_LPD_TXP1_103	GTYP_BANK 103	BA7	O, DIFF	Low power domain GTYP Bank 103 channel 1 High speed differential Transmitter positive
C66	GTYP_LPD_TXN1_103	GTYP_LPD_TXN1_103	GTYP_BANK 103	BA6	O, DIFF	Low power domain GTYP Bank 103 channel 1 High speed differential Transmitter Negative
C68	GTYP_LPD_TXP2_103	GTYP_LPD_TXP2_103	GTYP_BANK 103	AW7	O, DIFF	Low power domain GTYP Bank 103 channel 2 High speed differential Transmitter positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C69	GTYP_LPD_TXN2_103	GTYP_LPD_TXN2_103	GTYP_BANK 103	AW6	O, DIFF	Low power domain GTYP Bank 103 channel 2 High speed differential Transmitter Negative
C71	GTYP_LPD_TXP3_103	GTYP_LPD_TXP3_103	GTYP_BANK 103	AV5	O, DIFF	Low power domain GTYP Bank 103 channel 3 High speed differential Transmitter positive
C72	GTYP_LPD_TXN3_103	GTYP_LPD_TXN3_103	GTYP_BANK 103	AV4	O, DIFF	Low power domain GTYP Bank 103 channel 3 High speed differential Transmitter Negative
C74	GTYP_LPD_REFCLK0P_103	GTYP_LPD_REFCLKP0_103	GTYP_BANK 103	AK9	I, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Reference Clock positive
C75	GTYP_LPD_REFCLK0N_103	GTYP_LPD_REFCLKN0_103	GTYP_BANK 103	AK8	I, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Reference Clock Negative
D62	GTYP_LPD_RXP0_103	GTYP_LPD_RXP0_103	GTYP_BANK 103	BA2	I, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Receiver positive
D63	GTYP_LPD_RXN0_103	GTYP_LPD_RXN0_103	GTYP_BANK 103	BA1	I, DIFF	Low power domain GTYP Bank 103 channel 0 High speed differential Receiver Negative
D65	GTYP_LPD_RXP1_103	GTYP_LPD_RXP1_103	GTYP_BANK 103	AY4	I, DIFF	Low power domain GTYP Bank 103 channel 1 High speed differential Receiver positive
D66	GTYP_LPD_RXN1_103	GTYP_LPD_RXN1_103	GTYP_BANK 103	AY3	I, DIFF	Low power domain GTYP Bank 103 channel 1 High speed differential Receiver Negative
D68	GTYP_LPD_RXP2_103	GTYP_LPD_RXP2_103	GTYP_BANK 103	AW2	I, DIFF	Low power domain GTYP Bank 103 channel 2 High speed differential Receiver positive
D69	GTYP_LPD_RXN2_103	GTYP_LPD_RXN2_103	GTYP_BANK 103	AW1	I, DIFF	Low power domain GTYP Bank 103 channel 2 High speed differential Receiver Negative
D71	GTYP_LPD_RXP3_103	GTYP_LPD_RXP3_103	GTYP_BANK 103	AU2	I, DIFF	Low power domain GTYP Bank 103 channel 3 High speed differential Receiver positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D72	GTYP_LPD_RXN3_103	GTYP_LPD_RXN3_103	GTYP_BANK 103	AU1	I, DIFF	Low power domain GTYP Bank 103 channel 3 High speed differential Receiver Negative
Bank104 Transceiver Quad Pins						
A77	GTYP_LPD_TXP0_104	GTYP_LPD_TXP0_104	GTYP_BANK 104	AT5	O, DIFF	Low power domain GTYP Bank 104 channel 0 High speed differential Transmitter positive
A78	GTYP_LPD_TXN0_104	GTYP_LPD_TXN0_104	GTYP_BANK 104	AT4	O, DIFF	Low power domain GTYP Bank 104 channel 0 High speed differential Transmitter Negative
A80	GTYP_LPD_TXP1_104	GTYP_LPD_TXP1_104	GTYP_BANK 104	AR7	O, DIFF	Low power domain GTYP Bank 104 channel 1 High speed differential Transmitter positive
A81	GTYP_LPD_TXN1_104	GTYP_LPD_TXN1_104	GTYP_BANK 104	AR6	O, DIFF	Low power domain GTYP Bank 104 channel 1 High speed differential Transmitter Negative
A83	GTYP_LPD_TXP2_104	GTYP_LPD_TXP2_104	GTYP_BANK 104	AP5	O, DIFF	Low power domain GTYP Bank 104 channel 2 High speed differential Transmitter positive
A84	GTYP_LPD_TXN2_104	GTYP_LPD_TXN2_104	GTYP_BANK 104	AP4	O, DIFF	Low power domain GTYP Bank 104 channel 2 High speed differential Transmitter Negative
A86	GTYP_LPD_TXP3_104	GTYP_LPD_TXP3_104	GTYP_BANK 104	AN7	O, DIFF	Low power domain GTYP Bank 104 channel 3 High speed differential Transmitter positive
A87	GTYP_LPD_TXN3_104	GTYP_LPD_TXN3_104	GTYP_BANK 104	AN6	O, DIFF	Low power domain GTYP Bank 104 channel 3 High speed differential Transmitter Negative
B77	GTYP_LPD_RXP0_104	GTYP_LPD_RXP0_104	GTYP_BANK 104	AR2	I, DIFF	Low power domain GTYP Bank 104 channel 0 High speed differential Receiver positive
B78	GTYP_LPD_RXN0_104	GTYP_LPD_RXN0_104	GTYP_BANK 104	AR1	I, DIFF	Low power domain GTYP Bank 104 channel 0 High speed differential Receiver Negative
B80	GTYP_LPD_RXP1_104	GTYP_LPD_RXP1_104	GTYP_BANK 104	AN2	I, DIFF	Low power domain GTYP Bank 104 channel 1 High speed differential Receiver positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B81	GTYP_LPD_RXN1_104	GTYP_LPD_RXN1_104	GTYP_BANK 104	AN1	I, DIFF	Low power domain GTYP Bank 104 channel 1 High speed differential Receiver Negative
B83	GTYP_LPD_RXP2_104	GTYP_LPD_RXP2_104	GTYP_BANK 104	AL2	I, DIFF	Low power domain GTYP Bank 104 channel 2 High speed differential Receiver positive
B84	GTYP_LPD_RXN2_104	GTYP_LPD_RXN2_104	GTYP_BANK 104	AL1	I, DIFF	Low power domain GTYP Bank 104 channel 2 High speed differential Receiver Negative
B86	GTYP_LPD_RXP3_104	GTYP_LPD_RXP3_104	GTYP_BANK 104	AJ2	I, DIFF	Low power domain GTYP Bank 104 channel 3 High speed differential Receiver positive
B87	GTYP_LPD_RXN3_104	GTYP_LPD_RXN3_104	GTYP_BANK 104	AJ1	I, DIFF	Low power domain GTYP Bank 104 channel 3 High speed differential Receiver Negative
Bank105 Transceiver Quad Pins						
C77	GTYP_LPD_TXP0_105	GTYP_LPD_TXP0_105	GTYP_BANK 105	AM5	O, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Transmitter positive
C78	GTYP_LPD_TXN0_105	GTYP_LPD_TXN0_105	GTYP_BANK 105	AM4	O, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Transmitter Negative
C80	GTYP_LPD_TXP1_105	GTYP_LPD_TXP1_105	GTYP_BANK 105	AL7	O, DIFF	Low power domain GTYP Bank 105 channel 1 High speed differential Transmitter positive
C81	GTYP_LPD_TXN1_105	GTYP_LPD_TXN1_105	GTYP_BANK 105	AL6	O, DIFF	Low power domain GTYP Bank 105 channel 1 High speed differential Transmitter Negative
C83	GTYP_LPD_TXP2_105	GTYP_LPD_TXP2_105	GTYP_BANK 105	AK5	O, DIFF	Low power domain GTYP Bank 105 channel 2 High speed differential Transmitter positive
C84	GTYP_LPD_TXN2_105	GTYP_LPD_TXN2_105	GTYP_BANK 105	AK4	O, DIFF	Low power domain GTYP Bank 105 channel 2 High speed differential Transmitter Negative
C86	GTYP_LPD_TXP3_105	GTYP_LPD_TXP3_105	GTYP_BANK 105	AJ7	O, DIFF	Low power domain GTYP Bank 105 channel 3 High speed differential Transmitter positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C87	GTYP_LPD_TXN3_105	GTYP_LPD_TXN3_105	GTYP_BANK 105	AJ6	O, DIFF	Low power domain GTYP Bank 105 channel 3 High speed differential Transmitter Negative
C89	GTYP_LPD_REFCLK0P_105	GTYP_LPD_REFCLKP0_105	GTYP_BANK 105	AD9	I, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Reference Clock positive
C90	GTYP_LPD_REFCLK0N_105	GTYP_LPD_REFCLKN0_105	GTYP_BANK 105	AD8	I, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Reference Clock Negative
D77	GTYP_LPD_RXP0_105	GTYP_LPD_RXP0_105	GTYP_BANK 105	AG2	I, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Receiver positive
D78	GTYP_LPD_RXN0_105	GTYP_LPD_RXN0_105	GTYP_BANK 105	AG1	I, DIFF	Low power domain GTYP Bank 105 channel 0 High speed differential Receiver Negative
D80	GTYP_LPD_RXP1_105	GTYP_LPD_RXP1_105	GTYP_BANK 105	AE2	I, DIFF	Low power domain GTYP Bank 105 channel 1 High speed differential Receiver positive
D81	GTYP_LPD_RXN1_105	GTYP_LPD_RXN1_105	GTYP_BANK 105	AE1	I, DIFF	Low power domain GTYP Bank 105 channel 1 High speed differential Receiver Negative
D83	GTYP_LPD_RXP2_105	GTYP_LPD_RXP2_105	GTYP_BANK 105	AD4	I, DIFF	Low power domain GTYP Bank 105 channel 2 High speed differential Receiver positive
D84	GTYP_LPD_RXN2_105	GTYP_LPD_RXN2_105	GTYP_BANK 105	AD3	I, DIFF	Low power domain GTYP Bank 105 channel 2 High speed differential Receiver Negative
D86	GTYP_LPD_RXP3_105	GTYP_LPD_RXP3_105	GTYP_BANK 105	AC2	I, DIFF	Low power domain GTYP Bank 105 channel 3 High speed differential Receiver positive
D87	GTYP_LPD_RXN3_105	GTYP_LPD_RXN3_105	GTYP_BANK 105	AC1	I, DIFF	Low power domain GTYP Bank 105 channel 3 High speed differential Receiver Negative

2.6.2.3 GTYP Bank High Speed Transceiver

The Versal Premium supports 12 GTYP transceiver Lanes through three transceiver Banks. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTYP transceiver quad supports two dedicated reference clock input pairs.

For more details on GTYP transceiver pinouts on Board-to-Board Connector 2, refer the below table.

Table 27: GTYP transceiver Bank pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank106 Transceiver Quad Pins						
C29	GTYP_TXP0_106	GTYP_TXP0_106	GTYP_BANK 106	AH5	O, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Transmitter positive
C30	GTYP_TXN0_106	GTYP_TXN0_106	GTYP_BANK 106	AH4	O, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Transmitter Negative
C32	GTYP_TXP1_106	GTYP_TXP1_106	GTYP_BANK 106	AG7	O, DIFF	Low power domain GTYP Bank 106 channel 1 High speed differential Transmitter positive
C33	GTYP_TXN1_106	GTYP_TXN1_106	GTYP_BANK 106	AG6	O, DIFF	Low power domain GTYP Bank 106 channel 1 High speed differential Transmitter Negative
C35	GTYP_TXP2_106	GTYP_TXP2_106	GTYP_BANK 106	AF5	O, DIFF	Low power domain GTYP Bank 106 channel 2 High speed differential Transmitter positive
C36	GTYP_TXN2_106	GTYP_TXN2_106	GTYP_BANK 106	AF4	O, DIFF	Low power domain GTYP Bank 106 channel 2 High speed differential Transmitter Negative
C38	GTYP_TXP3_106	GTYP_TXP3_106	GTYP_BANK 106	AE7	O, DIFF	Low power domain GTYP Bank 106 channel 3 High speed differential Transmitter positive
C39	GTYP_TXN3_106	GTYP_TXN3_106	GTYP_BANK 106	AE6	O, DIFF	Low power domain GTYP Bank 106 channel 3 High speed differential Transmitter Negative
C41	GTYP_REFCLK0P_106	GTYP_REFCLKP0_106	GTYP_BANK 106	Y9	I, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Reference Clock positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C42	GTYP_REFCLK0N_106	GTYP_REFCLKN0_106	GTYP_BANK 106	Y8	I, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Reference Clock Negative
D29	GTYP_RXP0_106	GTYP_RXP0_106	GTYP_BANK 106	AB4	I, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Receiver positive
D30	GTYP_RXN0_106	GTYP_RXN0_106	GTYP_BANK 106	AB3	I, DIFF	Low power domain GTYP Bank 106 channel 0 High speed differential Receiver Negative
D32	GTYP_RXP1_106	GTYP_RXP1_106	GTYP_BANK 106	AA2	I, DIFF	Low power domain GTYP Bank 106 channel 1 High speed differential Receiver positive
D33	GTYP_RXN1_106	GTYP_RXN1_106	GTYP_BANK 106	AA1	I, DIFF	Low power domain GTYP Bank 106 channel 1 High speed differential Receiver Negative
D35	GTYP_RXP2_106	GTYP_RXP2_106	GTYP_BANK 106	W2	I, DIFF	Low power domain GTYP Bank 106 channel 2 High speed differential Receiver positive
D36	GTYP_RXN2_106	GTYP_RXN2_106	GTYP_BANK 106	W1	I, DIFF	Low power domain GTYP Bank 106 channel 2 High speed differential Receiver Negative
D38	GTYP_RXP3_106	GTYP_RXP3_106	GTYP_BANK 106	V4	I, DIFF	Low power domain GTYP Bank 106 channel 3 High speed differential Receiver positive
D39	GTYP_RXN3_106	GTYP_RXN3_106	GTYP_BANK 106	V3	I, DIFF	Low power domain GTYP Bank 106 channel 3 High speed differential Receiver Negative
Bank110 Transceiver Quad Pins						
C47	GTYP_TXP0_110	GTYP_TXP0_110	GTYP_BANK 110	N7	O, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Transmitter positive
C48	GTYP_TXN0_110	GTYP_TXN0_110	GTYP_BANK 110	N6	O, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Transmitter Negative
C50	GTYP_TXP1_110	GTYP_TXP1_110	GTYP_BANK 110	L7	O, DIFF	Low power domain GTYP Bank 110 channel 1 High speed differential Transmitter positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C51	GTYP_TXN1_110	GTYP_TXN1_110	GTYP_BANK 110	L6	O, DIFF	Low power domain GTYP Bank 110 channel 1 High speed differential Transmitter Negative
C53	GTYP_TXP2_110	GTYP_TXP2_110	GTYP_BANK 110	K5	O, DIFF	Low power domain GTYP Bank 110 channel 2 High speed differential Transmitter positive
C54	GTYP_TXN2_110	GTYP_TXN2_110	GTYP_BANK 110	K4	O, DIFF	Low power domain GTYP Bank 110 channel 2 High speed differential Transmitter Negative
C56	GTYP_TXP3_110	GTYP_TXP3_110	GTYP_BANK 110	J7	O, DIFF	Low power domain GTYP Bank 110 channel 3 High speed differential Transmitter positive
C57	GTYP_TXN3_110	GTYP_TXN3_110	GTYP_BANK 110	J6	O, DIFF	Low power domain GTYP Bank 110 channel 3 High speed differential Transmitter Negative
C59	GTYP_REFCLK0P_110	GTYP_REFCLKN0_110	GTYP_BANK 110	P8	I, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Reference Clock positive
C60	GTYP_REFCLK0N_110	GTYP_REFCLKP0_110	GTYP_BANK 110	P9	I, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Reference Clock Negative
D47	GTYP_RXP0_110	GTYP_RXP0_110	GTYP_BANK 110	G2	I, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Receiver positive
D48	GTYP_RXN0_110	GTYP_RXN0_110	GTYP_BANK 110	G1	I, DIFF	Low power domain GTYP Bank 110 channel 0 High speed differential Receiver Negative
D50	GTYP_RXP1_110	GTYP_RXP1_110	GTYP_BANK 110	F4	I, DIFF	Low power domain GTYP Bank 110 channel 1 High speed differential Receiver positive
D51	GTYP_RXN1_110	GTYP_RXN1_110	GTYP_BANK 110	F3	I, DIFF	Low power domain GTYP Bank 110 channel 1 High speed differential Receiver Negative
D53	GTYP_RXP2_110	GTYP_RXP2_110	GTYP_BANK 110	E2	I, DIFF	Low power domain GTYP Bank 110 channel 2 High speed differential Receiver positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D54	GTYP_RXN2_110	GTYP_RXN2_110	GTYP_BANK 110	E1	I, DIFF	Low power domain GTYP Bank 110 channel 2 High speed differential Receiver Negative
D56	GTYP_RXP3_110	GTYP_RXP3_110	GTYP_BANK 110	D3	I, DIFF	Low power domain GTYP Bank 110 channel 3 High speed differential Receiver positive
D57	GTYP_RXN3_110	GTYP_RXN3_110	GTYP_BANK 110	C3	I, DIFF	Low power domain GTYP Bank 110 channel 3 High speed differential Receiver Negative
Bank200 Transceiver Quad Pins						
A92	GTYP_TXP0_200	GTYP_TXP0_200	GTYP_BANK 200	BJ36	O, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Transmitter positive
A93	GTYP_TXN0_200	GTYP_TXN0_200	GTYP_BANK 200	BK36	O, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Transmitter Negative
A95	GTYP_TXP1_200	GTYP_TXP1_200	GTYP_BANK 200	BG37	O, DIFF	Low power domain GTYP Bank 200 channel 1 High speed differential Transmitter positive
A96	GTYP_TXN1_200	GTYP_TXN1_200	GTYP_BANK 200	BH37	O, DIFF	Low power domain GTYP Bank 200 channel 1 High speed differential Transmitter Negative
C92	GTYP_TXP2_200	GTYP_TXP2_200	GTYP_BANK 200	BJ38	O, DIFF	Low power domain GTYP Bank 200 channel 2 High speed differential Transmitter positive
C93	GTYP_TXN2_200	GTYP_TXN2_200	GTYP_BANK 200	BK38	O, DIFF	Low power domain GTYP Bank 200 channel 2 High speed differential Transmitter Negative
C95	GTYP_TXP3_200	GTYP_TXP3_200	GTYP_BANK 200	BG39	O, DIFF	Low power domain GTYP Bank 200 channel 3 High speed differential Transmitter positive
C96	GTYP_TXN3_200	GTYP_TXN3_200	GTYP_BANK 200	BH39	O, DIFF	Low power domain GTYP Bank 200 channel 3 High speed differential Transmitter Negative
A98	GTYP_REFCLK0P_200	GTYP_REFCLKP0_200	GTYP_BANK 200	AW47	I, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Reference Clock positive

B2B-2 Pin No	B2B Connector 2 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A99	GTYP_REFCLK0N_200	GTYP_REFCLKN0_200	GTYP_BANK 200	AW48	I, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Reference Clock Negative
B92	GTYP_RXP0_200	GTYP_RXP0_200	GTYP_BANK 200	BM37	I, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Receiver positive
B93	GTYP_RXN0_200	GTYP_RXN0_200	GTYP_BANK 200	BN37	I, DIFF	Low power domain GTYP Bank 200 channel 0 High speed differential Receiver Negative
B95	GTYP_RXP1_200	GTYP_RXP1_200	GTYP_BANK 200	BM39	I, DIFF	Low power domain GTYP Bank 200 channel 1 High speed differential Receiver positive
B96	GTYP_RXN1_200	GTYP_RXN1_200	GTYP_BANK 200	BN39	I, DIFF	Low power domain GTYP Bank 200 channel 1 High speed differential Receiver Negative
D92	GTYP_RXP2_200	GTYP_RXP2_200	GTYP_BANK 200	BM41	I, DIFF	Low power domain GTYP Bank 200 channel 2 High speed differential Receiver positive
D93	GTYP_RXN2_200	GTYP_RXN2_200	GTYP_BANK 200	BN41	I, DIFF	Low power domain GTYP Bank 200 channel 2 High speed differential Receiver Negative
D95	GTYP_RXP3_200	GTYP_RXP3_200	GTYP_BANK 200	BM43	I, DIFF	Low power domain GTYP Bank 200 channel 3 High speed differential Receiver positive
D96	GTYP_RXN3_200	GTYP_RXN3_200	GTYP_BANK 200	BN43	I, DIFF	Low power domain GTYP Bank 200 channel 3 High speed differential Receiver Negative

2.6.3 Power and Control Pins

The Versal Premium SOM uses a 12V power input (VCC) from Board-to-Board Connector 2 and generates all other necessary powers internally on the SOM itself. The SOM power can be turned on or off from the carrier board using the SOM Power enable pin (B11) in Board-to-Board Connector 2. Carrier Board will send the SOM Power Enable signal to enable on-SOM power regulators, eventually the Versal Premium SOM sends a SOM Power OK signal to the carrier board after the final power rail in the SOM becomes stable.

The Versal Premium SOM supports VRTC_3V coin cell power input from Board-to-Board Connector 2, which is connected to the PMIC's VBBAT pin for real-time clock backup voltage. It also supports a warm reset input from Board-to-Board Connector 2, dedicated RSTBTN# Pin from board-to-board connector 2.

A dedicated interrupt pin is provided as input from the Board-to-board connector. This interrupt pin is connected to the XPIO BANK 703.

An extended option for selecting the boot media to the board-to-board connectors is available in the Versal Premium SOM. This feature allows the end user to choose the boot media in the carrier board itself without any hardware changes in the SOM. PS MODE Pins configuration is provided at the SoC Boot Mode Section.

Additionally, Ground pins are distributed throughout the Board-to-Board Connectors for better performance.

For more details on these pins on Board-to-Board Connector 2, refer the below table.

Table 28: Power and controls pinouts on Board-to-Board Connector 2

B2B-2 Pin No	B2B Connector 2	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C12	VRTC_3V	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.
B11	SOM_PWR_EN	NA	NA	NA	OD, Input	SOM Power Enable from carrier board
B12	SOM_PWR_OK	NA	NA	NA	O, 1.8V Power	Active High SOM Power Good
B13	B_RST_OUT(XP_BE20_LVDS703_L25P)	IO_L25P_N8P2_M1P50_703	XPIO BANK 703	BE20	O, 1.8V, LVCMOS	Reset Out for carrier board interface reset.
B14	RESET_SW_IN	IO_L26N_N8P5_M1P161_705	XPIO BANK 705	BG29	I, 1.8V, LVCMOS	Warm reset input for SOC.
B15	CONFIG_DONE	DONE_503	PMC DIO BANK 503	A16	O, 1.8V, LVCMOS/ 4.7K PU	FPGA Configuration done status pin.
C13	PS_MODE0	MODE0_503	PMC DIO BANK 503	D20	I, 1.8V LVCMOS	Boot Mode0 Select pin

B2B-2 Pin No	B2B Connector 2	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C14	PS_MODE1	MODE1_503	PMC DIO BANK 503	D19	I, 1.8V LVCMOS	Boot Mode1 Select pin
C15	PS_MODE2	MODE2_503	PMC DIO BANK 503	C19	I, 1.8V LVCMOS	Boot Mode2 Select pin
C26	HS_PCIE_RSTN	PMC_MIO39_501	PMC MIO BANK 501	W18	IO, 1.8V LVCMOS	PCIe reset for CPM5 banks available in GTYP LPD TXVRs
C27	B_LS_RST(XP_BD23_LVDS704_L25P)	IO_L25P_N8P2_M1P104_704	XPIO BANK 704	BD23	IO, 1.8V LVCMOS	LS PCIe Reset for PCIe supported in LS TCVR banks.
D14	B_D_INT(XP_BE21_LVDS703_L26P)	IO_L26P_N8P4_M1P52_703		BE21	I, 1.8V LVCMOS	Dedicated interrupt input for SoC Device.
D98	SYSMON_D_VP	VP_500		AA20	Input	System Monitor dedicated differential analog positive input
D99	SYSMON_D_VN	VN_500		AB21	Input	System Monitor dedicated differential analog negative input
B25	10MHz_B2B_IN	NA	NA	NA	I, 1.8V, LVCMOS	10MHz clock input
B26	1PPS_B2B_IN	NA	NA	NA	I, 1.8V, LVCMOS	1Hz clock input
D11	10M_CLK_OUT	NA	NA	NA	O, 1.8V, LVCMOS	10MHz clock output
D12	1PPS_CLK_OUT	NA	NA	NA	O, 1.8V, LVCMOS	1Hz clock output
B41	SYS_SYNC_XP_BE32_LVDS706_L24P	IO_L24P_GC_XCC_N8P0_M2P48_706	XPIO BANK 706	BE32	O, LVDS	SYNC clock out positive from XPIO bank
B42	SYS_SYNC_XP_BE33_LVDS706_L24N	IO_L24N_GC_XCC_N8P1_M2P49_706	XPIO BANK 706	BE33	O, LVDS	SYNC clock out negative from XPIO bank
B44	SYS_SYNC_CLK_INp	NA	NA	NA	I, LVDS	SYNC clock in positive from XPIO bank
B45	SYS_SYNC_CLK_INn	NA	NA	NA	I, LVDS	SYNC clock in negative from XPIO bank

B2B-2 Pin No	B2B Connector 2	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A1, A2, A3, A4, A5, A6, A7, A8, B1, B2, B3, B4, B5, B6, B7, B8, C1, C2, C3, C4, C5, C6, C7, C8, D1, D2, D3, D4, D5, D6, D7, D8.	VCC_12V	NA		NA	I, 12V Power	Supply Voltage.
A9, A10, A16 ,A23, A34, A37, A40, A43, A46, A49, A52, A55, A58 A61, A64, A67, A70, A73, A76, A79, A82, A85, A88, A91, A94, A97, A100, B9, B10, B16, B23, B34, B37, B40, B43, B46, B49, B52, B55, B58, B61, B64, B67, B70, B73, B76, B79, B82, B85, B88, B91, B94, B97, B100, C9, C10, C16, C23, C28, C31, C34, C37, C40, C43, C46, C49, C52, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, C100, D9, D10, D16, D23, D28, D31, D34, D37, D40, D43, D46, D49, D52, D55, D58, D61, D64, D67, D70, D73, D76, D79, D82, D85, D88, D91, D94, D97, D100	GND	NA		NA	Power	Ground.

2.7 Board-to-Board Connector 3

The Versal Premium SOM supports three 400-pin high-speed, Receptacle, Center Strip Connectors for interface expansion. The SOM design makes every effort to maximize the interfaces of the Versal Adaptive SoC to the carrier board by adding these Three board-to-board connectors.

The pinout for Board-to-Board Connector-3(J6) on the Versal premium SOM is provided in the table below, and the available interfaces are explained in the following sections. Board-to-Board Connector-3 is located on the bottom side of the SOM, as shown in the diagram below.

Number of Pins	- 400
Connector Part Number	- ASP-209946-01 from Samtec
Mating Connector	- ASP-214802-01 from Samtec
Staking Height	- 5mm

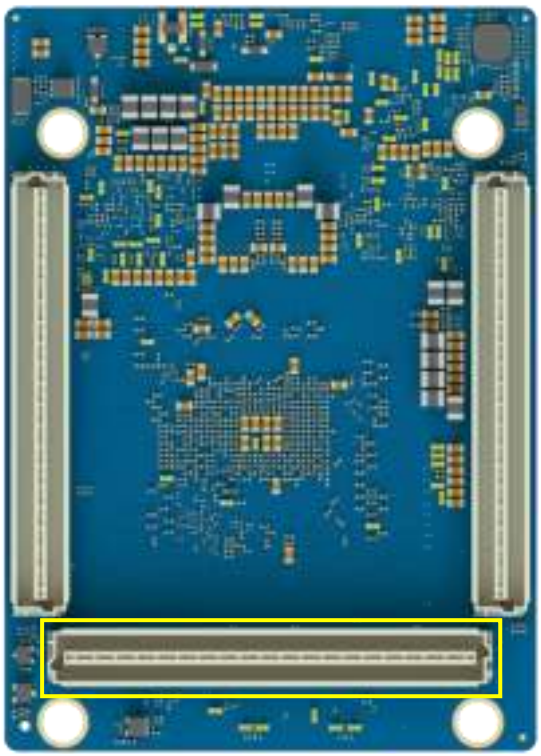


Figure 6: Board-to-Board Connector 3

Table 29: Board-to-Board Connector 3 Pinout

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	GND	B1	GND	C1	GND	D1	GND
A2	GTYP_TXP0_201	B2	GTYP_RXP0_201	C2	GTYP_TXP0_208	D2	GTYP_RXP0_208
A3	GTYP_TXN0_201	B3	GTYP_RXN0_201	C3	GTYP_TXN0_208	D3	GTYP_RXN0_208
A4	GND	B4	GND	C4	GND	D4	GND
A5	GTYP_TXP1_201	B5	GTYP_RXP1_201	C5	GTYP_TXP1_208	D5	GTYP_RXP1_208
A6	GTYP_TXN1_201	B6	GTYP_RXN1_201	C6	GTYP_TXN1_208	D6	GTYP_RXN1_208
A7	GND	B7	GND	C7	GND	D7	GND
A8	GTYP_TXP2_201	B8	GTYP_RXP2_201	C8	GTYP_TXP2_208	D8	GTYP_RXP2_208
A9	GTYP_TXN2_201	B9	GTYP_RXN2_201	C9	GTYP_TXN2_208	D9	GTYP_RXN2_208
A10	GND	B10	GND	C10	GND	D10	GND
A11	GTYP_TXP3_201	B11	GTYP_RXP3_201	C11	GTYP_TXP3_208	D11	GTYP_RXP3_208
A12	GTYP_TXN3_201	B12	GTYP_RXN3_201	C12	GTYP_TXN3_208	D12	GTYP_RXN3_208
A13	GND	B13	GND	C13	GND	D13	GND
A14	GTYP_REFCLK0P_201	B14	B2B_GTYP_REFCLK1P_201	C14	GTYP_REFCLK0P_208	D14	B2B_GTYP_REFCLK1P_208
A15	GTYP_REFCLK0N_201	B15	B2B_GTYP_REFCLK1N_201	C15	GTYP_REFCLK0N_208	D15	B2B_GTYP_REFCLK1N_208
A16	GND	B16	GND	C16	GND	D16	GND
A17	GTYP_TXP0_209	B17	GTYP_RXP0_209	C17	GTYP_TXP0_210	D17	GTYP_RXP0_210
A18	GTYP_TXN0_209	B18	GTYP_RXN0_209	C18	GTYP_TXN0_210	D18	GTYP_RXN0_210
A19	GND	B19	GND	C19	GND	D19	GND
A20	GTYP_TXP1_209	B20	GTYP_RXP1_209	C20	GTYP_TXP1_210	D20	GTYP_RXP1_210
A21	GTYP_TXN1_209	B21	GTYP_RXN1_209	C21	GTYP_TXN1_210	D21	GTYP_RXN1_210
A22	GND	B22	GND	C22	GND	D22	GND
A23	GTYP_TXP2_209	B23	GTYP_RXP2_209	C23	GTYP_TXP2_210	D23	GTYP_RXP2_210
A24	GTYP_TXN2_209	B24	GTYP_RXN2_209	C24	GTYP_TXN2_210	D24	GTYP_RXN2_210
A25	GND	B25	GND	C25	GND	D25	GND
A26	GTYP_TXP3_209	B26	GTYP_RXP3_209	C26	GTYP_TXP3_210	D26	GTYP_RXP3_210
A27	GTYP_TXN3_209	B27	GTYP_RXN3_209	C27	GTYP_TXN3_210	D27	GTYP_RXN3_210
A28	GND	B28	GND	C28	GND	D28	GND
A29	GTYP_REFCLK0P_209	B29	B2B_GTYP_REFCLK1P_209	C29	GTYP_REFCLK0P_210	D29	B2B_GTYP_REFCLK1P_210
A30	GTYP_REFCLK0N_209	B30	B2B_GTYP_REFCLK1N_209	C30	GTYP_REFCLK0N_210	D30	B2B_GTYP_REFCLK1N_210
A31	GND	B31	GND	C31	GND	D31	GND
A32	GTYP_TXP0_211	B32	GTYP_RXP0_211	C32	GTM_TXP0_205	D32	GTM_RXP0_205
A33	GTYP_TXN0_211	B33	GTYP_RXN0_211	C33	GTM_TXN0_205	D33	GTM_RXN0_205
A34	GND	B34	GND	C34	GND	D34	GND
A35	GTYP_TXP1_211	B35	GTYP_RXP1_211	C35	GTM_TXP1_205	D35	GTM_RXP1_205
A36	GTYP_TXN1_211	B36	GTYP_RXN1_211	C36	GTM_TXN1_205	D36	GTM_RXN1_205
A37	GND	B37	GND	C37	GND	D37	GND
A38	GTYP_TXP2_211	B38	GTYP_RXP2_211	C38	GTM_TXP2_205	D38	GTM_RXP2_205
A39	GTYP_TXN2_211	B39	GTYP_RXN2_211	C39	GTM_TXN2_205	D39	GTM_RXN2_205

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A40	GND	B40	GND	C40	GND	D40	GND
A41	GTYP_TXP3_211	B41	GTYP_RXP3_211	C41	GTM_TXP3_205	D41	GTM_RXP3_205
A42	GTYP_TXN3_211	B42	GTYP_RXN3_211	C42	GTM_TXN3_205	D42	GTM_RXN3_205
A43	GND	B43	GND	C43	GND	D43	GND
A44	GTYP_REFCLK0P_211	B44	B2B_GTYP_REFCLK1P_211	C44	GTM_REFCLK0P_205	D44	B2B_GTM_REFCLK1P_205
A45	GTYP_REFCLK0N_211	B45	B2B_GTYP_REFCLK1N_211	C45	GTM_REFCLK0N_205	D45	B2B_GTM_REFCLK1N_205
A46	GND	B46	GND	C46	GND	D46	GND
A47	GTM_TXP0_204	B47	GTM_RXP0_204	C47	GTYP_TXP0_207	D47	GTYP_RXP0_207
A48	GTM_TXN0_204	B48	GTM_RXN0_204	C48	GTYP_TXN0_207	D48	GTYP_RXN0_207
A49	GND	B49	GND	C49	GND	D49	GND
A50	GTM_TXP1_204	B50	GTM_RXP1_204	C50	GTYP_TXP1_207	D50	GTYP_RXP1_207
A51	GTM_TXN1_204	B51	GTM_RXN1_204	C51	GTYP_TXN1_207	D51	GTYP_RXN1_207
A52	GND	B52	GND	C52	GND	D52	GND
A53	GTM_TXP2_204	B53	GTM_RXP2_204	C53	GTYP_TXP2_207	D53	GTYP_RXP2_207
A54	GTM_TXN2_204	B54	GTM_RXN2_204	C54	GTYP_TXN2_207	D54	GTYP_RXN2_207
A55	GND	B55	GND	C55	GND	D55	GND
A56	GTM_TXP3_204	B56	GTM_RXP3_204	C56	GTYP_TXP3_207	D56	GTYP_RXP3_207
A57	GTM_TXN3_204	B57	GTM_RXN3_204	C57	GTYP_TXN3_207	D57	GTYP_RXN3_207
A58	GND	B58	GND	C58	GND	D58	GND
A59	GTM_REFCLK0P_204	B59	B2B_GTM_REFCLK1P_204	C59	GTYP_REFCLK0P_207	D59	B2B_GTYP_REFCLK1P_207
A60	GTM_REFCLK0N_204	B60	B2B_GTM_REFCLK1N_204	C60	GTYP_REFCLK0N_207	D60	B2B_GTYP_REFCLK1N_207
A61	GND	B61	GND	C61	GND	D61	GND
A62	GTYP_TXP0_109	B62	GTYP_RXP0_109	C62	GTM_TXP0_203	D62	GTM_RXP0_203
A63	GTYP_TXN0_109	B63	GTYP_RXN0_109	C63	GTM_TXN0_203	D63	GTM_RXN0_203
A64	GND	B64	GND	C64	GND	D64	GND
A65	GTYP_TXP1_109	B65	GTYP_RXP1_109	C65	GTM_TXP1_203	D65	GTM_RXP1_203
A66	GTYP_TXN1_109	B66	GTYP_RXN1_109	C66	GTM_TXN1_203	D66	GTM_RXN1_203
A67	GND	B67	GND	C67	GND	D67	GND
A68	GTYP_TXP2_109	B68	GTYP_RXP2_109	C68	GTM_TXP2_203	D68	GTM_RXP2_203
A69	GTYP_TXN2_109	B69	GTYP_RXN2_109	C69	GTM_TXN2_203	D69	GTM_RXN2_203
A70	GND	B70	GND	C70	GND	D70	GND
A71	GTYP_TXP3_109	B71	GTYP_RXP3_109	C71	GTM_TXP3_203	D71	GTM_RXP3_203
A72	GTYP_TXN3_109	B72	GTYP_RXN3_109	C72	GTM_TXN3_203	D72	GTM_RXN3_203
A73	GND	B73	GND	C73	GND	D73	GND
A74	GTYP_REFCLK0P_109	B74	B2B_GTYP_REFCLK1P_109	C74	GTM_REFCLK0P_203	D74	B2B_GTM_REFCLK1P_203
A75	GTYP_REFCLK0N_109	B75	B2B_GTYP_REFCLK1N_109	C75	GTM_REFCLK0N_203	D75	B2B_GTM_REFCLK1N_203
A76	GND	B76	GND	C76	GND	D76	GND
A77	GTYP_TXP0_111	B77	GTYP_RXP0_111	C77	GTYP_TXP0_112	D77	GTYP_RXP0_112
A78	GTYP_TXN0_111	B78	GTYP_RXN0_111	C78	GTYP_TXN0_112	D78	GTYP_RXN0_112
A79	GND	B79	GND	C79	GND	D79	GND
A80	GTYP_TXP1_111	B80	GTYP_RXP1_111	C80	GTYP_TXP1_112	D80	GTYP_RXP1_112

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A81	GTYP_TXN1_111	B81	GTYP_RXN1_111	C81	GTYP_TXN1_112	D81	GTYP_RXN1_112
A82	GND	B82	GND	C82	GND	D82	GND
A83	GTYP_TXP2_111	B83	GTYP_RXP2_111	C83	GTYP_TXP2_112	D83	GTYP_RXP2_112
A84	GTYP_TXN2_111	B84	GTYP_RXN2_111	C84	GTYP_TXN2_112	D84	GTYP_RXN2_112
A85	GND	B85	GND	C85	GND	D85	GND
A86	GTYP_TXP3_111	B86	GTYP_RXP3_111	C86	GTYP_TXP3_112	D86	GTYP_RXP3_112
A87	GTYP_TXN3_111	B87	GTYP_RXN3_111	C87	GTYP_TXN3_112	D87	GTYP_RXN3_112
A88	GND	B88	GND	C88	GND	D88	GND
A89	GTYP_REFCLK0P_111	B89	B2B_GTYP_REFCLK1P_111	C89	GTYP_REFCLK0P_112	D89	B2B_GTYP_REFCLK1P_112
A90	GTYP_REFCLK0N_111	B90	B2B_GTYP_REFCLK1N_111	C90	GTYP_REFCLK0N_112	D90	B2B_GTYP_REFCLK1N_112
A91	GND	B91	GND	C91	GND	D91	GND
A92	GTYP_TXP0_212	B92	GTYP_RXP0_212	C92	GTYP_TXP2_212	D92	GTYP_RXP2_212
A93	GTYP_TXN0_212	B93	GTYP_RXN0_212	C93	GTYP_TXN2_212	D93	GTYP_RXN2_212
A94	GND	B94	GND	C94	GND	D94	GND
A95	GTYP_TXP1_212	B95	GTYP_RXP1_212	C95	GTYP_TXP3_212	D95	GTYP_RXP3_212
A96	GTYP_TXN1_212	B96	GTYP_RXN1_212	C96	GTYP_TXN3_212	D96	GTYP_RXN3_212
A97	GND	B97	GND	C97	GND	D97	GND
A98	GTYP_REFCLK0P_212	B98	B2B_GTYP_REFCLK1P_212	C98	NC	D98	NC
A99	GTYP_REFCLK0N_212	B99	B2B_GTYP_REFCLK1N_212	C99	NC	D99	NC
A100	GND	B100	GND	C100	GND	D100	GND

Important Note: Bank name and bank number mentioned in this document is with respect to VP1552 Devices.

2.7.1 PL Interfaces

The interfaces which are supported in Board-to-Board Connector 3 from Versal Premium SoC's PL is explained in the following section.

2.7.1.1 GTM Bank High speed Transceiver

The Versal Premium supports 12 GTM transceiver Lanes through three transceiver Banks. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTM transceiver quad supports two dedicated reference clock input pairs.

For more details on GTM transceiver pinouts on Board-to-Board Connector 3, refer the below table.

Table 30:GTM Transceiver Bank pinouts on Board-to-Board Connector 3

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank203 Transceiver Quad Pins						
C62	GTM_TXP0_203	GTM_TXP0_203	GTM_BANK 203	BE47	O, DIFF	GTM Bank203 channel0 High speed differential Transmitter positive.
C63	GTM_TXN0_203	GTM_TXN0_203	GTM_BANK 203	BE48	O, DIFF	GTM Bank203 channel0 High speed differential Transmitter negative.
C65	GTM_TXP1_203	GTM_TXP1_203	GTM_BANK 203	BD49	O, DIFF	GTM Bank203 channel1 High speed differential Transmitter Positive.
C66	GTM_TXN1_203	GTM_TXN1_203	GTM_BANK 203	BD50	O, DIFF	GTM Bank203 channel1 High speed differential Transmitter negative.
C68	GTM_TXP2_203	GTM_TXP2_203	GTM_BANK 203	BC47	O, DIFF	GTM Bank203 channel2 High speed differential Transmitter positive.
C69	GTM_TXN2_203	GTM_TXN2_203	GTM_BANK 203	BC48	O, DIFF	GTM Bank203 channel2 High speed differential Transmitter negative.
C71	GTM_TXP3_203	GTM_TXP3_203	GTM_BANK 203	BB49	O, DIFF	GTM Bank203 channel3 High speed differential Transmitter Positive.
C72	GTM_TXN3_203	GTM_TXN3_203	GTM_BANK 203	BB50	O, DIFF	GTM Bank203 channel3 High speed differential Transmitter negative.
C74	GTM_REFCLK0P_203	GTM_REFCLKP0_203	GTM_BANK 203	AF45	I, DIFF	GTM Bank203 channel0 High speed differential Reference Clock Positive.
C75	GTM_REFCLK0N_203	GTM_REFCLKN0_203	GTM_BANK 203	AF46	I, DIFF	GTM Bank203 channel0 High speed differential Reference Clock negative.

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D62	GTM_RXP0_203	GTM_RXP0_203	GTM_BANK 203	BG52	I, DIFF	GTM Bank203 channel0 High speed differential Receiver positive.
D63	GTM_RXN0_203	GTM_RXN0_203	GTM_BANK 203	BG53	I, DIFF	GTM Bank203 channel0 High speed differential Receiver negative.
D65	GTM_RXP1_203	GTM_RXP1_203	GTM_BANK 203	BE52	I, DIFF	GTM Bank203 channel1 High speed differential Receiver positive.
D66	GTM_RXN1_203	GTM_RXN1_203	GTM_BANK 203	BE53	I, DIFF	GTM Bank203 channel1 High speed differential Receiver negative.
D68	GTM_RXP2_203	GTM_RXP2_203	GTM_BANK 203	BC52	I, DIFF	GTM Bank203 channel2 High speed differential Receiver positive.
D69	GTM_RXN2_203	GTM_RXN2_203	GTM_BANK 203	BC53	I, DIFF	GTM Bank203 channel2 High speed differential Receiver negative.
D71	GTM_RXP3_203	GTM_RXP3_203	GTM_BANK 203	BA52	I, DIFF	GTM Bank203 channel3 High speed differential Receiver positive.
D72	GTM_RXN3_203	GTM_RXN3_203	GTM_BANK 203	BA53	I, DIFF	GTM Bank203 channel3 High speed differential Receiver negative.
Bank204 Transceiver Quad Pins						
A47	GTM_TXP0_204	GTM_TXP0_204	GTM_BANK 204	BA47	O, DIFF	GTM Bank204 channel0 High speed differential Transmitter positive.
A48	GTM_TXN0_204	GTM_TXN0_204	GTM_BANK 204	BA48	O, DIFF	GTM Bank204 channel0 High speed differential Transmitter negative.
A50	GTM_TXP1_204	GTM_TXP1_204	GTM_BANK 204	AY49	O, DIFF	GTM Bank204 channel1 High speed differential Transmitter Positive.
A51	GTM_TXN1_204	GTM_TXN1_204	GTM_BANK 204	AY50	O, DIFF	GTM Bank204 channel1 High speed differential Transmitter negative.
A53	GTM_TXP2_204	GTM_TXP2_204	GTM_BANK 204	AV49	O, DIFF	GTM Bank204 channel2 High speed differential Transmitter positive.
A54	GTM_TXN2_204	GTM_TXN2_204	GTM_BANK 204	AV50	O, DIFF	GTM Bank204 channel2 High speed differential Transmitter negative.
A56	GTM_TXP3_204	GTM_TXP3_204	GTM_BANK 204	AT49	O, DIFF	GTM Bank204 channel3 High speed differential Transmitter Positive.

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A57	GTM_TXN3_204	GTM_TXN3_204	GTM_BANK 204	AT50	O, DIFF	GTM Bank204 channel3 High speed differential Transmitter negative.
A59	GTM_REFCLK0P_204	GTM_REFCLKP0_204	GTM_BANK 204	AB45	I, DIFF	GTM Bank204 channel0 High speed differential Reference Clock Positive.
A60	GTM_REFCLK0N_204	GTM_REFCLKN0_204	GTM_BANK 204	AB46	I, DIFF	GTM Bank204 channel0 High speed differential Reference Clock negative.
B47	GTM_RXP0_204	GTM_RXP0_204	GTM_BANK 204	AW52	I, DIFF	GTM Bank204 channel0 High speed differential Receiver positive.
B48	GTM_RXN0_204	GTM_RXN0_204	GTM_BANK 204	AW53	I, DIFF	GTM Bank204 channel0 High speed differential Receiver negative.
B50	GTM_RXP1_204	GTM_RXP1_204	GTM_BANK 204	AU52	I, DIFF	GTM Bank204 channel1 High speed differential Receiver positive.
B51	GTM_RXN1_204	GTM_RXN1_204	GTM_BANK 204	AU53	I, DIFF	GTM Bank204 channel1 High speed differential Receiver negative.
B53	GTM_RXP2_204	GTM_RXP2_204	GTM_BANK 204	AR52	I, DIFF	GTM Bank204 channel2 High speed differential Receiver positive.
B54	GTM_RXN2_204	GTM_RXN2_204	GTM_BANK 204	AR53	I, DIFF	GTM Bank204 channel2 High speed differential Receiver negative.
B56	GTM_RXP3_204	GTM_RXP3_204	GTM_BANK 204	AN52	I, DIFF	GTM Bank204 channel3 High speed differential Receiver positive.
B57	GTM_RXN3_204	GTM_RXN3_204	GTM_BANK 204	AN53	I, DIFF	GTM Bank204 channel3 High speed differential Receiver negative.
Bank205 Transceiver Quad Pins						
C32	GTM_TXP0_205	GTM_TXP0_205	GTM_BANK 205	AP49	O, DIFF	GTM Bank205 channel0 High speed differential Transmitter positive.
C33	GTM_TXN0_205	GTM_TXN0_205	GTM_BANK 205	AP50	O, DIFF	GTM Bank205 channel0 High speed differential Transmitter negative.
C35	GTM_TXP1_205	GTM_TXP1_205	GTM_BANK 205	AM49	O, DIFF	GTM Bank205 channel1 High speed differential Transmitter Positive.
C36	GTM_TXN1_205	GTM_TXN1_205	GTM_BANK 205	AM50	O, DIFF	GTM Bank205 channel1 High speed differential Transmitter negative.

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C38	GTM_TXP2_205	GTM_TXP2_205	GTM_BANK 205	AK49	O, DIFF	GTM Bank205 channel2 High speed differential Transmitter positive.
C39	GTM_TXN2_205	GTM_TXN2_205	GTM_BANK 205	AK50	O, DIFF	GTM Bank205 channel2 High speed differential Transmitter negative.
C41	GTM_TXP3_205	GTM_TXP3_205	GTM_BANK 205	AH49	O, DIFF	GTM Bank205 channel3 High speed differential Transmitter Positive.
C42	GTM_TXN3_205	GTM_TXN3_205	GTM_BANK 205	AH50	O, DIFF	GTM Bank205 channel3 High speed differential Transmitter negative.
C44	GTM_REFCLK0P_205	GTM_REFCLKP0_205	GTM_BANK 205	Y45	I, DIFF	GTM Bank205 channel0 High speed differential Reference Clock Positive.
C45	GTM_REFCLK0N_205	GTM_REFCLKN0_205	GTM_BANK 205	Y46	I, DIFF	GTM Bank205 channel0 High speed differential Reference Clock negative.
D32	GTM_RXP0_205	GTM_RXP0_205	GTM_BANK 205	AL52	I, DIFF	GTM Bank205 channel0 High speed differential Receiver positive.
D33	GTM_RXN0_205	GTM_RXN0_205	GTM_BANK 205	AL53	I, DIFF	GTM Bank205 channel0 High speed differential Receiver negative.
D35	GTM_RXP1_205	GTM_RXP1_205	GTM_BANK 205	AJ52	I, DIFF	GTM Bank205 channel1 High speed differential Receiver positive.
D36	GTM_RXN1_205	GTM_RXN1_205	GTM_BANK 205	AJ53	I, DIFF	GTM Bank205 channel1 High speed differential Receiver negative.
D38	GTM_RXP2_205	GTM_RXP2_205	GTM_BANK 205	AG52	I, DIFF	GTM Bank205 channel2 High speed differential Receiver positive.
D39	GTM_RXN2_205	GTM_RXN2_205	GTM_BANK 205	AG53	I, DIFF	GTM Bank205 channel2 High speed differential Receiver negative.
D41	GTM_RXP3_205	GTM_RXP3_205	GTM_BANK 205	AE52	I, DIFF	GTM Bank205 channel3 High speed differential Receiver positive.
D42	GTM_RXN3_205	GTM_RXN3_205	GTM_BANK 205	AE53	I, DIFF	GTM Bank205 channel3 High speed differential Receiver negative.

2.7.1.2 GTYP Bank High Speed Transceiver

The Versal Premium supports 40 GTYP transceiver Lanes through ten transceiver Banks. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTYP transceiver quad supports two dedicated reference clock input pairs.

For more details on GTYP transceiver pinouts on Board-to-Board Connector 3, refer the below table.

Table 31: GTYP transceiver Bank pinouts on Board-to-Board Connector 3

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank109 Transceiver Quad Pins						
A62	GTYP_TXP0_109	GTYP_TXP0_109	GTYP_BANK 109	W7	O, DIFF	GTYP Bank 109 channel 0 High speed differential Transmitter positive
A63	GTYP_TXN0_109	GTYP_TXN0_109	GTYP_BANK 109	W6	O, DIFF	GTYP Bank 109 channel 0 High speed differential Transmitter Negative
A65	GTYP_TXP1_109	GTYP_TXP1_109	GTYP_BANK 109	U7	O, DIFF	GTYP Bank 109 channel 1 High speed differential Transmitter positive
A66	GTYP_TXN1_109	GTYP_TXN1_109	GTYP_BANK 109	U6	O, DIFF	GTYP Bank 109 channel 1 High speed differential Transmitter Negative
A68	GTYP_TXP2_109	GTYP_TXP2_109	GTYP_BANK 109	R7	O, DIFF	GTYP Bank 109 channel 2 High speed differential Transmitter positive
A69	GTYP_TXN2_109	GTYP_TXN2_109	GTYP_BANK 109	R6	O, DIFF	GTYP Bank 109 channel 2 High speed differential Transmitter Negative
A71	GTYP_TXP3_109	GTYP_TXP3_109	GTYP_BANK 109	P5	O, DIFF	GTYP Bank 109 channel 3 High speed differential Transmitter positive
A72	GTYP_TXN3_109	GTYP_TXN3_109	GTYP_BANK 109	P4	O, DIFF	GTYP Bank 109 channel 3 High speed differential Transmitter Negative
A74	GTYP_REFCLK0P_109	GTYP_REFCLKP0_109	GTYP_BANK 109	T9	I, DIFF	GTYP Bank 109 channel 0 High speed differential Reference Clock positive
A75	GTYP_REFCLK0N_109	GTYP_REFCLKN0_109	GTYP_BANK 109	T8	I, DIFF	GTYP Bank 109 channel 0 High speed differential Reference Clock Negative
B62	GTYP_RXP0_109	GTYP_RXP0_109	GTYP_BANK 109	M4	I, DIFF	GTYP Bank 109 channel 0 High speed differential Receiver positive
B63	GTYP_RXN0_109	GTYP_RXN0_109	GTYP_BANK 109	M3	I, DIFF	GTYP Bank 109 channel 0 High speed differential Receiver Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
B65	GTYP_RXP1_109	GTYP_RXP1_109	GTYP_BANK 109	L2	I, DIFF	GTYP Bank 109 channel 1 High speed differential Receiver positive
B66	GTYP_RXN1_109	GTYP_RXN1_109	GTYP_BANK 109	L1	I, DIFF	GTYP Bank 109 channel 1 High speed differential Receiver Negative
B68	GTYP_RXP2_109	GTYP_RXP2_109	GTYP_BANK 109	J2	I, DIFF	GTYP Bank 109 channel 2 High speed differential Receiver positive
B69	GTYP_RXN2_109	GTYP_RXN2_109	GTYP_BANK 109	J1	I, DIFF	GTYP Bank 109 channel 2 High speed differential Receiver Negative
B71	GTYP_RXP3_109	GTYP_RXP3_109	GTYP_BANK 109	H4	I, DIFF	GTYP Bank 109 channel 3 High speed differential Receiver positive
B72	GTYP_RXN3_109	GTYP_RXN3_109	GTYP_BANK 109	H3	I, DIFF	GTYP Bank 109 channel 3 High speed differential Receiver Negative
Bank111 Transceiver Quad Pins						
A77	GTYP_TXP0_111	GTYP_TXP0_111	GTYP_BANK 111	G6	O, DIFF	GTYP Bank 111 channel 0 High speed differential Transmitter positive
A78	GTYP_TXN0_111	GTYP_TXN0_111	GTYP_BANK 111	F6	O, DIFF	GTYP Bank 111 channel 0 High speed differential Transmitter Negative
A80	GTYP_TXP1_111	GTYP_TXP1_111	GTYP_BANK 111	G8	O, DIFF	GTYP Bank 111 channel 1 High speed differential Transmitter positive
A81	GTYP_TXN1_111	GTYP_TXN1_111	GTYP_BANK 111	F8	O, DIFF	GTYP Bank 111 channel 1 High speed differential Transmitter Negative
A83	GTYP_TXP2_111	GTYP_TXP2_111	GTYP_BANK 111	E9	O, DIFF	GTYP Bank 111 channel 2 High speed differential Transmitter positive
A84	GTYP_TXN2_111	GTYP_TXN2_111	GTYP_BANK 111	D9	O, DIFF	GTYP Bank 111 channel 2 High speed differential Transmitter Negative
A86	GTYP_TXP3_111	GTYP_TXP3_111	GTYP_BANK 111	G10	O, DIFF	GTYP Bank 111 channel 3 High speed differential Transmitter positive
A87	GTYP_TXN3_111	GTYP_TXN3_111	GTYP_BANK 111	F10	O, DIFF	GTYP Bank 111 channel 3 High speed differential Transmitter Negative
A89	GTYP_REFCLK0P_111	GTYP_REFCLKP0_111	GTYP_BANK 111	M9	I, DIFF	GTYP Bank 111 channel 0 High speed differential Reference Clock positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A90	GTYP_REFCLK0N_111	GTYP_REFCLKN0_111	GTYP_BANK 111	M8	I, DIFF	GTYP Bank 111 channel 0 High speed differential Reference Clock Negative
B77	GTYP_RXP0_111	GTYP_RXP0_111	GTYP_BANK 111	D5	I, DIFF	GTYP Bank 111 channel 0 High speed differential Receiver positive
B78	GTYP_RXN0_111	GTYP_RXN0_111	GTYP_BANK 111	C5	I, DIFF	GTYP Bank 111 channel 0 High speed differential Receiver Negative
B80	GTYP_RXP1_111	GTYP_RXP1_111	GTYP_BANK 111	B6	I, DIFF	GTYP Bank 111 channel 1 High speed differential Receiver positive
B81	GTYP_RXN1_111	GTYP_RXN1_111	GTYP_BANK 111	A6	I, DIFF	GTYP Bank 111 channel 1 High speed differential Receiver Negative
B83	GTYP_RXP2_111	GTYP_RXP2_111	GTYP_BANK 111	D7	I, DIFF	GTYP Bank 111 channel 2 High speed differential Receiver positive
B84	GTYP_RXN2_111	GTYP_RXN2_111	GTYP_BANK 111	C7	I, DIFF	GTYP Bank 111 channel 2 High speed differential Receiver Negative
B86	GTYP_RXP3_111	GTYP_RXP3_111	GTYP_BANK 111	B8	I, DIFF	GTYP Bank 111 channel 3 High speed differential Receiver positive
B87	GTYP_RXN3_111	GTYP_RXN3_111	GTYP_BANK 111	A8	I, DIFF	GTYP Bank 111 channel 3 High speed differential Receiver Negative
Bank112 Transceiver Quad Pins						
C77	GTYP_TXP0_112	GTYP_TXP0_112	GTYP_BANK 112	G12	O, DIFF	GTYP Bank 112 channel 0 High speed differential Transmitter positive
C78	GTYP_TXN0_112	GTYP_TXN0_112	GTYP_BANK 112	F12	O, DIFF	GTYP Bank 112 channel 0 High speed differential Transmitter Negative
C80	GTYP_TXP1_112	GTYP_TXP1_112	GTYP_BANK 112	E13	O, DIFF	GTYP Bank 112 channel 1 High speed differential Transmitter positive
C81	GTYP_TXN1_112	GTYP_TXN1_112	GTYP_BANK 112	D13	O, DIFF	GTYP Bank 112 channel 1 High speed differential Transmitter Negative
C83	GTYP_TXP2_112	GTYP_TXP2_112	GTYP_BANK 112	G14	O, DIFF	GTYP Bank 112 channel 2 High speed differential Transmitter positive
C84	GTYP_TXN2_112	GTYP_TXN2_112	GTYP_BANK 112	F14	O, DIFF	GTYP Bank 112 channel 2 High speed differential Transmitter Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C86	GTYP_TXP3_112	GTYP_TXP3_112	GTYP_BANK 112	E15	O, DIFF	GTYP Bank 112 channel 3 High speed differential Transmitter positive
C87	GTYP_TXN3_112	GTYP_TXN3_112	GTYP_BANK 112	D15	O, DIFF	GTYP Bank 112 channel 3 High speed differential Transmitter Negative
C89	GTYP_REFCLK0P_112	GTYP_REFCLKP0_112	GTYP_BANK 112	K9	I, DIFF	GTYP Bank 112 channel 0 High speed differential Reference Clock positive
C90	GTYP_REFCLK0N_112	GTYP_REFCLKN0_112	GTYP_BANK 112	K8	I, DIFF	GTYP Bank 112 channel 0 High speed differential Reference Clock Negative
D77	GTYP_RXP0_112	GTYP_RXP0_112	GTYP_BANK 112	B10	I, DIFF	GTYP Bank 112 channel 0 High speed differential Receiver positive
D78	GTYP_RXN0_112	GTYP_RXN0_112	GTYP_BANK 112	A10	I, DIFF	GTYP Bank 112 channel 0 High speed differential Receiver Negative
D80	GTYP_RXP1_112	GTYP_RXP1_112	GTYP_BANK 112	D11	I, DIFF	GTYP Bank 112 channel 1 High speed differential Receiver positive
D81	GTYP_RXN1_112	GTYP_RXN1_112	GTYP_BANK 112	C11	I, DIFF	GTYP Bank 112 channel 1 High speed differential Receiver Negative
D83	GTYP_RXP2_112	GTYP_RXP2_112	GTYP_BANK 112	B12	I, DIFF	GTYP Bank 112 channel 2 High speed differential Receiver positive
D84	GTYP_RXN2_112	GTYP_RXN2_112	GTYP_BANK 112	A12	I, DIFF	GTYP Bank 112 channel 2 High speed differential Receiver Negative
D86	GTYP_RXP3_112	GTYP_RXP3_112	GTYP_BANK 112	B14	I, DIFF	GTYP Bank 112 channel 3 High speed differential Receiver positive
D87	GTYP_RXN3_112	GTYP_RXN3_112	GTYP_BANK 112	A14	I, DIFF	GTYP Bank 112 channel 3 High speed differential Receiver Negative
Bank201 Transceiver Quad Pins						
A2	GTYP_TXP0_201	GTYP_TXP0_201	GTYP_BANK 201	BJ40	O, DIFF	GTYP Bank 201 channel 0 High speed differential Transmitter positive
A3	GTYP_TXN0_201	GTYP_TXN0_201	GTYP_BANK 201	BK40	O, DIFF	GTYP Bank 201 channel 0 High speed differential Transmitter Negative
A5	GTYP_TXP1_201	GTYP_TXP1_201	GTYP_BANK 201	BG41	O, DIFF	GTYP Bank 201 channel 1 High speed differential Transmitter positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A6	GTYP_TXN1_201	GTYP_TXN1_201	GTYP_BANK 201	BH41	O, DIFF	GTYP Bank 201 channel 1 High speed differential Transmitter Negative
A8	GTYP_TXP2_201	GTYP_TXP2_201	GTYP_BANK 201	BJ42	O, DIFF	GTYP Bank 201 channel 2 High speed differential Transmitter positive
A9	GTYP_TXN2_201	GTYP_TXN2_201	GTYP_BANK 201	BK42	O, DIFF	GTYP Bank 201 channel 2 High speed differential Transmitter Negative
A11	GTYP_TXP3_201	GTYP_TXP3_201	GTYP_BANK 201	BG43	O, DIFF	GTYP Bank 201 channel 3 High speed differential Transmitter positive
A12	GTYP_TXN3_201	GTYP_TXN3_201	GTYP_BANK 201	BH43	O, DIFF	GTYP Bank 201 channel 3 High speed differential Transmitter Negative
A14	GTYP_REFCLK0P_201	GTYP_REFCLKP0_201	GTYP_BANK 201	AR47	I, DIFF	GTYP Bank 201 channel 0 High speed differential Reference Clock positive
A15	GTYP_REFCLK0N_201	GTYP_REFCLKN0_201	GTYP_BANK 201	AR48	I, DIFF	GTYP Bank 201 channel 0 High speed differential Reference Clock Negative
B2	GTYP_RXP0_201	GTYP_RXP0_201	GTYP_BANK 201	BK44	I, DIFF	GTYP Bank 201 channel 0 High speed differential Receiver positive
B3	GTYP_RXN0_201	GTYP_RXN0_201	GTYP_BANK 201	BL44	I, DIFF	GTYP Bank 201 channel 0 High speed differential Receiver Negative
B5	GTYP_RXP1_201	GTYP_RXP1_201	GTYP_BANK 201	BM45	I, DIFF	GTYP Bank 201 channel 1 High speed differential Receiver positive
B6	GTYP_RXN1_201	GTYP_RXN1_201	GTYP_BANK 201	BN45	I, DIFF	GTYP Bank 201 channel 1 High speed differential Receiver Negative
B8	GTYP_RXP2_201	GTYP_RXP2_201	GTYP_BANK 201	BK46	I, DIFF	GTYP Bank 201 channel 2 High speed differential Receiver positive
B9	GTYP_RXN2_201	GTYP_RXN2_201	GTYP_BANK 201	BL46	I, DIFF	GTYP Bank 201 channel 2 High speed differential Receiver Negative
B11	GTYP_RXP3_201	GTYP_RXP3_201	GTYP_BANK 201	BM47	I, DIFF	GTYP Bank 201 channel 3 High speed differential Receiver positive
B12	GTYP_RXN3_201	GTYP_RXN3_201	GTYP_BANK 201	BN47	I, DIFF	GTYP Bank 201 channel 3 High speed differential Receiver Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank207 Transceiver Quad Pins						
C47	GTYP_TXP0_207	GTYP_TXP0_207	GTYP_BANK 207	AF49	O, DIFF	GTYP Bank 207 channel 0 High speed differential Transmitter positive
C48	GTYP_TXN0_207	GTYP_TXN0_207	GTYP_BANK 207	AF50	O, DIFF	GTYP Bank 207 channel 0 High speed differential Transmitter Negative
C50	GTYP_TXP1_207	GTYP_TXP1_207	GTYP_BANK 207	AE47	O, DIFF	GTYP Bank 207 channel 1 High speed differential Transmitter positive
C51	GTYP_TXN1_207	GTYP_TXN1_207	GTYP_BANK 207	AE48	O, DIFF	GTYP Bank 207 channel 1 High speed differential Transmitter Negative
C53	GTYP_TXP2_207	GTYP_TXP2_207	GTYP_BANK 207	AD49	O, DIFF	GTYP Bank 207 channel 2 High speed differential Transmitter positive
C54	GTYP_TXN2_207	GTYP_TXN2_207	GTYP_BANK 207	AD50	O, DIFF	GTYP Bank 207 channel 2 High speed differential Transmitter Negative
C56	GTYP_TXP3_207	GTYP_TXP3_207	GTYP_BANK 207	AC47	O, DIFF	GTYP Bank 207 channel 3 High speed differential Transmitter positive
C57	GTYP_TXN3_207	GTYP_TXN3_207	GTYP_BANK 207	AC48	O, DIFF	GTYP Bank 207 channel 3 High speed differential Transmitter Negative
C59	GTYP_REFCLK0P_207	GTYP_REFCLKP0_207	GTYP_BANK 207	V45	I, DIFF	GTYP Bank 207 channel 0 High speed differential Reference Clock positive
C60	GTYP_REFCLK0N_207	GTYP_REFCLKN0_207	GTYP_BANK 207	V46	I, DIFF	GTYP Bank 207 channel 0 High speed differential Reference Clock Negative
D47	GTYP_RXP0_207	GTYP_RXP0_207	GTYP_BANK 207	AC52	I, DIFF	GTYP Bank 207 channel 0 High speed differential Receiver positive
D48	GTYP_RXN0_207	GTYP_RXN0_207	GTYP_BANK 207	AC53	I, DIFF	GTYP Bank 207 channel 0 High speed differential Receiver Negative
D50	GTYP_RXP1_207	GTYP_RXP1_207	GTYP_BANK 207	AA52	I, DIFF	GTYP Bank 207 channel 1 High speed differential Receiver positive
D51	GTYP_RXN1_207	GTYP_RXN1_207	GTYP_BANK 207	AA53	I, DIFF	GTYP Bank 207 channel 1 High speed differential Receiver Negative
D53	GTYP_RXP2_207	GTYP_RXP2_207	GTYP_BANK 207	Y50	I, DIFF	GTYP Bank 207 channel 2 High speed differential Receiver positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D54	GTYP_RXN2_207	GTYP_RXN2_207	GTYP_BANK 207	Y51	I, DIFF	GTYP Bank 207 channel 2 High speed differential Receiver Negative
D56	GTYP_RXP3_207	GTYP_RXP3_207	GTYP_BANK 207	W52	I, DIFF	GTYP Bank 207 channel 3 High speed differential Receiver positive
D57	GTYP_RXN3_207	GTYP_RXN3_207	GTYP_BANK 207	W53	I, DIFF	GTYP Bank 207 channel 3 High speed differential Receiver Negative
Bank208 Transceiver Quad Pins						
C2	GTYP_TXP0_208	GTYP_TXP0_208	GTYP_BANK 208	AB49	O, DIFF	GTYP Bank 208 channel 0 High speed differential Transmitter positive
C3	GTYP_TXN0_208	GTYP_TXN0_208	GTYP_BANK 208	AB50	O, DIFF	GTYP Bank 208 channel 0 High speed differential Transmitter Negative
C5	GTYP_TXP1_208	GTYP_TXP1_208	GTYP_BANK 208	AA47	O, DIFF	GTYP Bank 208 channel 1 High speed differential Transmitter positive
C6	GTYP_TXN1_208	GTYP_TXN1_208	GTYP_BANK 208	AA48	O, DIFF	GTYP Bank 208 channel 1 High speed differential Transmitter Negative
C8	GTYP_TXP2_208	GTYP_TXP2_208	GTYP_BANK 208	W47	O, DIFF	GTYP Bank 208 channel 2 High speed differential Transmitter positive
C9	GTYP_TXN2_208	GTYP_TXN2_208	GTYP_BANK 208	W48	O, DIFF	GTYP Bank 208 channel 2 High speed differential Transmitter Negative
C11	GTYP_TXP3_208	GTYP_TXP3_208	GTYP_BANK 208	V49	O, DIFF	GTYP Bank 208 channel 3 High speed differential Transmitter positive
C12	GTYP_TXN3_208	GTYP_TXN3_208	GTYP_BANK 208	V50	O, DIFF	GTYP Bank 208 channel 3 High speed differential Transmitter Negative
C14	GTYP_REFCLK0P_208	GTYP_REFCLKP0_208	GTYP_BANK 208	U43	I, DIFF	GTYP Bank 208 channel 0 High speed differential Reference Clock positive
C15	GTYP_REFCLK0N_208	GTYP_REFCLKN0_208	GTYP_BANK 208	U44	I, DIFF	GTYP Bank 208 channel 0 High speed differential Reference Clock Negative
D2	GTYP_RXP0_208	GTYP_RXP0_208	GTYP_BANK 208	U52	I, DIFF	GTYP Bank 208 channel 0 High speed differential Receiver positive
D3	GTYP_RXN0_208	GTYP_RXN0_208	GTYP_BANK 208	U53	I, DIFF	GTYP Bank 208 channel 0 High speed differential Receiver Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D5	GTYP_RXP1_208	GTYP_RXP1_208	GTYP_BANK 208	R52	I, DIFF	GTYP Bank 208 channel 1 High speed differential Receiver positive
D6	GTYP_RXN1_208	GTYP_RXN1_208	GTYP_BANK 208	R53	I, DIFF	GTYP Bank 208 channel 1 High speed differential Receiver Negative
D8	GTYP_RXP2_208	GTYP_RXP2_208	GTYP_BANK 208	P50	I, DIFF	GTYP Bank 208 channel 2 High speed differential Receiver positive
D9	GTYP_RXN2_208	GTYP_RXN2_208	GTYP_BANK 208	P51	I, DIFF	GTYP Bank 208 channel 2 High speed differential Receiver Negative
D11	GTYP_RXP3_208	GTYP_RXP3_208	GTYP_BANK 208	N52	I, DIFF	GTYP Bank 208 channel 3 High speed differential Receiver positive
D12	GTYP_RXN3_208	GTYP_RXN3_208	GTYP_BANK 208	N53	I, DIFF	GTYP Bank 208 channel 3 High speed differential Receiver Negative
Bank209 Transceiver Quad Pins						
A17	GTYP_TXP0_209	GTYP_TXP0_209	GTYP_BANK 209	T49	O, DIFF	GTYP Bank 209 channel 0 High speed differential Transmitter positive
A18	GTYP_TXN0_209	GTYP_TXN0_209	GTYP_BANK 209	T50	O, DIFF	GTYP Bank 209 channel 0 High speed differential Transmitter Negative
A20	GTYP_TXP1_209	GTYP_TXP1_209	GTYP_BANK 209	M49	O, DIFF	GTYP Bank 209 channel 1 High speed differential Transmitter positive
A21	GTYP_TXN1_209	GTYP_TXN1_209	GTYP_BANK 209	M50	O, DIFF	GTYP Bank 209 channel 1 High speed differential Transmitter Negative
A23	GTYP_TXP2_209	GTYP_TXP2_209	GTYP_BANK 209	K49	O, DIFF	GTYP Bank 209 channel 2 High speed differential Transmitter positive
A24	GTYP_TXN2_209	GTYP_TXN2_209	GTYP_BANK 209	K50	O, DIFF	GTYP Bank 209 channel 2 High speed differential Transmitter Negative
A26	GTYP_TXP3_209	GTYP_TXP3_209	GTYP_BANK 209	H49	O, DIFF	GTYP Bank 209 channel 3 High speed differential Transmitter positive
A27	GTYP_TXN3_209	GTYP_TXN3_209	GTYP_BANK 209	H50	O, DIFF	GTYP Bank 209 channel 3 High speed differential Transmitter Negative
A29	GTYP_REFCLK0P_209	GTYP_REFCLKP0_209	GTYP_BANK 209	R43	I, DIFF	GTYP Bank 209 channel 0 High speed differential Reference Clock positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A30	GTYP_REFCLK0N_209	GTYP_REFCLKN0_209	GTYP_BANK 209	R44	I, DIFF	GTYP Bank 209 channel 0 High speed differential Reference Clock Negative
B17	GTYP_RXP0_209	GTYP_RXP0_209	GTYP_BANK 209	L52	I, DIFF	GTYP Bank 209 channel 0 High speed differential Receiver positive
B18	GTYP_RXN0_209	GTYP_RXN0_209	GTYP_BANK 209	L53	I, DIFF	GTYP Bank 209 channel 0 High speed differential Receiver Negative
B20	GTYP_RXP1_209	GTYP_RXP1_209	GTYP_BANK 209	J52	I, DIFF	GTYP Bank 209 channel 1 High speed differential Receiver positive
B21	GTYP_RXN1_209	GTYP_RXN1_209	GTYP_BANK 209	J53	I, DIFF	GTYP Bank 209 channel 1 High speed differential Receiver Negative
B23	GTYP_RXP2_209	GTYP_RXP2_209	GTYP_BANK 209	G52	I, DIFF	GTYP Bank 209 channel 2 High speed differential Receiver positive
B24	GTYP_RXN2_209	GTYP_RXN2_209	GTYP_BANK 209	G53	I, DIFF	GTYP Bank 209 channel 2 High speed differential Receiver Negative
B26	GTYP_RXP3_209	GTYP_RXP3_209	GTYP_BANK 209	E52	I, DIFF	GTYP Bank 209 channel 3 High speed differential Receiver positive
B27	GTYP_RXN3_209	GTYP_RXN3_209	GTYP_BANK 209	E53	I, DIFF	GTYP Bank 209 channel 3 High speed differential Receiver Negative
Bank210 Transceiver Quad Pins						
C17	GTYP_TXP0_210	GTYP_TXP0_210	GTYP_BANK 210	F49	O, DIFF	GTYP Bank 210 channel 0 High speed differential Transmitter positive
C18	GTYP_TXN0_210	GTYP_TXN0_210	GTYP_BANK 210	F50	O, DIFF	GTYP Bank 210 channel 0 High speed differential Transmitter Negative
C20	GTYP_TXP1_210	GTYP_TXP1_210	GTYP_BANK 210	G47	O, DIFF	GTYP Bank 210 channel 1 High speed differential Transmitter positive
C21	GTYP_TXN1_210	GTYP_TXN1_210	GTYP_BANK 210	F47	O, DIFF	GTYP Bank 210 channel 1 High speed differential Transmitter Negative
C23	GTYP_TXP2_210	GTYP_TXP2_210	GTYP_BANK 210	E46	O, DIFF	GTYP Bank 210 channel 2 High speed differential Transmitter positive
C24	GTYP_TXN2_210	GTYP_TXN2_210	GTYP_BANK 210	D46	O, DIFF	GTYP Bank 210 channel 2 High speed differential Transmitter Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
C26	GTYP_TXP3_210	GTYP_TXP3_210	GTYP_BANK 210	G45	O, DIFF	GTYP Bank 210 channel 3 High speed differential Transmitter positive
C27	GTYP_TXN3_210	GTYP_TXN3_210	GTYP_BANK 210	F45	O, DIFF	GTYP Bank 210 channel 3 High speed differential Transmitter Negative
C29	GTYP_REFCLK0P_210	GTYP_REFCLKP0_210	GTYP_BANK 210	N47	I, DIFF	GTYP Bank 210 channel 0 High speed differential Reference Clock positive
C30	GTYP_REFCLK0N_210	GTYP_REFCLKN0_210	GTYP_BANK 210	N48	I, DIFF	GTYP Bank 210 channel 0 High speed differential Reference Clock Negative
D17	GTYP_RXP0_210	GTYP_RXP0_210	GTYP_BANK 210	D50	I, DIFF	GTYP Bank 210 channel 0 High speed differential Receiver positive
D18	GTYP_RXN0_210	GTYP_RXN0_210	GTYP_BANK 210	C50	I, DIFF	GTYP Bank 210 channel 0 High speed differential Receiver Negative
D20	GTYP_RXP1_210	GTYP_RXP1_210	GTYP_BANK 210	B49	I, DIFF	GTYP Bank 210 channel 1 High speed differential Receiver positive
D21	GTYP_RXN1_210	GTYP_RXN1_210	GTYP_BANK 210	A49	I, DIFF	GTYP Bank 210 channel 1 High speed differential Receiver Negative
D23	GTYP_RXP2_210	GTYP_RXP2_210	GTYP_BANK 210	D48	I, DIFF	GTYP Bank 210 channel 2 High speed differential Receiver positive
D24	GTYP_RXN2_210	GTYP_RXN2_210	GTYP_BANK 210	C48	I, DIFF	GTYP Bank 210 channel 2 High speed differential Receiver Negative
D26	GTYP_RXP3_210	GTYP_RXP3_210	GTYP_BANK 210	B47	I, DIFF	GTYP Bank 210 channel 3 High speed differential Receiver positive
D27	GTYP_RXN3_210	GTYP_RXN3_210	GTYP_BANK 210	A47	I, DIFF	GTYP Bank 210 channel 3 High speed differential Receiver Negative
Bank211 Transceiver Quad Pins						
A32	GTYP_TXP0_211	GTYP_TXP0_211	GTYP_BANK 211	E44	O, DIFF	GTYP Bank 211 channel 0 High speed differential Transmitter positive
A33	GTYP_TXN0_211	GTYP_TXN0_211	GTYP_BANK 211	D44	O, DIFF	GTYP Bank 211 channel 0 High speed differential Transmitter Negative
A35	GTYP_TXP1_211	GTYP_TXP1_211	GTYP_BANK 211	G43	O, DIFF	GTYP Bank 211 channel 1 High speed differential Transmitter positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A36	GTYP_TXN1_211	GTYP_TXN1_211	GTYP_BANK 211	F43	O, DIFF	GTYP Bank 211 channel 1 High speed differential Transmitter Negative
A38	GTYP_TXP2_211	GTYP_TXP2_211	GTYP_BANK 211	G41	O, DIFF	GTYP Bank 211 channel 2 High speed differential Transmitter positive
A39	GTYP_TXN2_211	GTYP_TXN2_211	GTYP_BANK 211	F41	O, DIFF	GTYP Bank 211 channel 2 High speed differential Transmitter Negative
A41	GTYP_TXP3_211	GTYP_TXP3_211	GTYP_BANK 211	E40	O, DIFF	GTYP Bank 211 channel 3 High speed differential Transmitter positive
A42	GTYP_TXN3_211	GTYP_TXN3_211	GTYP_BANK 211	D40	O, DIFF	GTYP Bank 211 channel 3 High speed differential Transmitter Negative
A44	GTYP_REFCLK0P_211	GTYP_REFCLKP0_211	GTYP_BANK 211	M45	I, DIFF	GTYP Bank 211 channel 0 High speed differential Reference Clock positive
A45	GTYP_REFCLK0N_211	GTYP_REFCLKN0_211	GTYP_BANK 211	M46	I, DIFF	GTYP Bank 211 channel 0 High speed differential Reference Clock Negative
B32	GTYP_RXP0_211	GTYP_RXP0_211	GTYP_BANK 211	B45	I, DIFF	GTYP Bank 211 channel 0 High speed differential Receiver positive
B33	GTYP_RXN0_211	GTYP_RXN0_211	GTYP_BANK 211	A45	I, DIFF	GTYP Bank 211 channel 0 High speed differential Receiver Negative
B35	GTYP_RXP1_211	GTYP_RXP1_211	GTYP_BANK 211	B43	I, DIFF	GTYP Bank 211 channel 1 High speed differential Receiver positive
B36	GTYP_RXN1_211	GTYP_RXN1_211	GTYP_BANK 211	A43	I, DIFF	GTYP Bank 211 channel 1 High speed differential Receiver Negative
B38	GTYP_RXP2_211	GTYP_RXP2_211	GTYP_BANK 211	D42	I, DIFF	GTYP Bank 211 channel 2 High speed differential Receiver positive
B39	GTYP_RXN2_211	GTYP_RXN2_211	GTYP_BANK 211	C42	I, DIFF	GTYP Bank 211 channel 2 High speed differential Receiver Negative
B41	GTYP_RXP3_211	GTYP_RXP3_211	GTYP_BANK 211	B41	I, DIFF	GTYP Bank 211 channel 3 High speed differential Receiver positive
B42	GTYP_RXN3_211	GTYP_RXN3_211	GTYP_BANK 211	A41	I, DIFF	GTYP Bank 211 channel 3 High speed differential Receiver Negative

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
Bank212 Transceiver Quad Pins						
A92	GTYP_TXP0_212	GTYP_TXP0_212	GTYP_BANK 212	G39	O, DIFF	GTYP Bank 212 channel 0 High speed differential Transmitter positive
A93	GTYP_TXN0_212	GTYP_TXN0_212	GTYP_BANK 212	F39	O, DIFF	GTYP Bank 212 channel 0 High speed differential Transmitter Negative
A95	GTYP_TXP1_212	GTYP_TXP1_212	GTYP_BANK 212	E38	O, DIFF	GTYP Bank 212 channel 1 High speed differential Transmitter positive
A96	GTYP_TXN1_212	GTYP_TXN1_212	GTYP_BANK 212	D38	O, DIFF	GTYP Bank 212 channel 1 High speed differential Transmitter Negative
C92	GTYP_TXP2_212	GTYP_TXP2_212	GTYP_BANK 212	G37	O, DIFF	GTYP Bank 212 channel 0 High speed differential Receiver positive
C93	GTYP_TXN2_212	GTYP_TXN2_212	GTYP_BANK 212	F37	O, DIFF	GTYP Bank 212 channel 0 High speed differential Receiver Negative
C95	GTYP_TXP3_212	GTYP_TXP3_212	GTYP_BANK 212	G35	O, DIFF	GTYP Bank 212 channel 1 High speed differential Receiver positive
C96	GTYP_TXN3_212	GTYP_TXN3_212	GTYP_BANK 212	F35	O, DIFF	GTYP Bank 212 channel 1 High speed differential Receiver Negative
A98	GTYP_REFCLK0P_212	GTYP_REFCLKP0_212	GTYP_BANK 212	K45	I, DIFF	GTYP Bank 212 channel 2 High speed differential Transmitter positive
A99	GTYP_REFCLK0N_212	GTYP_REFCLKN0_212	GTYP_BANK 212	K46	I, DIFF	GTYP Bank 212 channel 2 High speed differential Transmitter Negative
B92	GTYP_RXP0_212	GTYP_RXP0_212	GTYP_BANK 212	B39	I, DIFF	GTYP Bank 212 channel 3 High speed differential Transmitter positive
B93	GTYP_RXN0_212	GTYP_RXN0_212	GTYP_BANK 212	A39	I, DIFF	GTYP Bank 212 channel 3 High speed differential Transmitter Negative
B95	GTYP_RXP1_212	GTYP_RXP1_212	GTYP_BANK 212	B37	I, DIFF	GTYP Bank 212 channel 0 High speed differential Reference Clock positive
B96	GTYP_RXN1_212	GTYP_RXN1_212	GTYP_BANK 212	A37	I, DIFF	GTYP Bank 212 channel 0 High speed differential Reference Clock Negative
D92	GTYP_RXP2_212	GTYP_RXP2_212	GTYP_BANK 212	D36	I, DIFF	GTYP Bank 212 channel 2 High speed differential Receiver positive

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
D93	GTYP_RXN2_212	GTYP_RXN2_212	GTYP_BANK 212	C36	I, DIFF	GTYP Bank 212 channel 2 High speed differential Receiver Negative
D95	GTYP_RXP3_212	GTYP_RXP3_212	GTYP_BANK 212	B35	I, DIFF	GTYP Bank 212 channel 3 High speed differential Receiver positive
D96	GTYP_RXN3_212	GTYP_RXN3_212	GTYP_BANK 212	A35	I, DIFF	GTYP Bank 212 channel 3 High speed differential Receiver Negative

2.7.2 Power and Control Pins

To ensure proper electrical grounding, reduce EMI, and provide mechanical stability between the two boards, ground pins are distributed throughout the Board-to-Board Connectors.

For more details on these ground pins on Board-to-Board Connector 1, refer the below table

Table 32: Power and controls pinouts of Board-to-Board Connector 3

B2B-3 Pin No	B2B Connector 3 Signal Name	SoC Pin Name	SoC Bank	SoC Pin No	Signal Type/ Termination	Description
A1, A4, A7, A10, A13, A16, A19, A22, A25, A28, A31, A34, A37, A40, A43, A46, A49, A52, A55, A58, A61, A64, A67, A70, A73, A76, A79, A82, A85, A88, A91 ,A94, A97, A100, B1, B4, B7, B10, B13, B16, B19, B22, B25, B28, B31, B34, B37, B40, B43, B46, B49, B52, B55, B58, B61 B64, B67, B70, B73, B76, B79, B82, B85, B88, B91, B94, B97, B100, C1, C4, C7, C10, C13, C16, C19, C22, C25, C28, C31, C34, C37, C40, C43, C46, C49, C52, C55, C58, C61, C64, C67, C70, C73, C76, C79, C82, C85, C88, C91, C94, C97, C100, D1, D4, D7, D10, D13, D16, D19, D22, D25, D28, D31, D34, D37, D40, D43, D46, D49, D52, D55, D58, D61, D64, D67, D70, D73, D76, D79, D82, D85, D88, D91, D94, D97, D100.	GND	NA	NA	NA	Power	Ground.

2.8 Versal Premium PS Pin Multiplexing on Board-to-Board Connectors

The Versal Premium PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Versal Premium PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Versal Premium SoC with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 33: PS Pin Multiplexing on Board to Board Connectors of Versal Premium SOM

Interface/ Function	B2B PIN No.	SoC pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19	Function 20	Function 21	Function 22
On SOM Features from PS MIO																									
eMMC	NA	PMC_MIO 38_501	PMC_G PIO38	SD0/EMMC 0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0: CLK	-	-	-	-	-	-	SMAP_IO[18]	-	GEM1: RGMII_TX _CLK	PMC_I2C _SCL	CANFD0_ RX	UART 1_TXD	SPI0_SCLK	LPD_I2C0 _SCL	SWDT0_C LK	TTC 1_CLK
	NA	PMC_MIO 39_501	PMC_G PIO39	SD0_DETEC T	SD0: DETECT	SD0: DETECT	-	-	-	-	-	-	-	-	-	SMAP_IO[19]	-	GEM1: RGMII_TX D[0]	PMC_I2C _SDA	CANFD0_ TX	UART 1_RXD	SPI0_SS2_ B	LPD_I2C0 _SDA	SWDT0_R ST	TTC 1_WAVE
	NA	PMC_MIO 40_501	PMC_G PIO40	SD0/EMMC 0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0: CMD	-	-	-	-	-	-	SMAP_IO[20]	-	GEM1: RGMII_TX D[1]	-	CANFD1_ TX	UART 1_RTS_B	SPI0_SS1_ B	LPD_I2C1 _SCL	SWDT0_R ST_PEND	TTC 0_CLK
	NA	PMC_MIO 41_501	PMC_G PIO41	SD0/EMMC 0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0: DATA[0]	-	-	-	-	-	-	SMAP_IO[21]	-	GEM1: RGMII_TX D[2]	-	CANFD1_ RX	UART 1_CTS_B	SPI0_SS0_ B	LPD_I2C1 _SDA	SWDT0_I NT	TTC 0_WAVE
	NA	PMC_MIO 42_501	PMC_G PIO42	SD0/EMMC _DATA[1]	SD0/EMM C_DATA[1]	SD0/EMM C_DATA[1]	-	SD0/EMM C_DATA[1]	SD0/EMM C0: DATA[1]	-	-	-	-	-	-	SMAP_IO[22]	-	GEM1: RGMII_TX D[3]	PMC_I2C _SCL	CANFD0_ RX	UART 0_RXD	SPI0_MSI O	LPD_I2C0 _SCL	SWDT0_ WS0	TTC 3_CLK
	NA	PMC_MIO 43_501	PMC_G PIO43	SD0/EMMC 0_DATA[2]	SD0/EMM C0_DATA[2]	SD0/EMM C0_DATA[2]	-	SD0/EMM C0_DATA[2]	SD0/EMM C0: DATA[2]	-	-	-	-	-	-	SMAP_IO[23]	-	GEM1: RGMII_TX _CTL	PMC_I2C _SDA	CANFD0_ TX	UART 0_TXD	SPI0_MO SI	LPD_I2C0 _SDA	SWDT0_ WS1	TTC 3_WAVE
	NA	PMC_MIO 44_501	PMC_G PIO44	SD0/EMMC 0_DATA[3]	SD0/EMM C0_DATA[3]	SD0/EMM C0_DATA[3]	-	SD0/EMM C0_DATA[3]	SD0/EMM C0: DATA[3]	-	-	-	-	-	-	SMAP_IO[24]	-	GEM1: RGMII_RX _CLK	-	CANFD1_ TX	UART 0_CTS_B	SPI1_SCLK	LPD_I2C1 _SCL	SWDT1_C LK	TTC 2_CLK
	NA	PMC_MIO 45_501	PMC_G PIO45	-	SD0/EMM C0_SEL/D ATA[4]	SD0/EMM C0_SEL/D ATA[4]	-	-	SD0/EMM C0: SEL/DATA[4]	-	-	-	-	-	-	SMAP_IO[25]	-	GEM1: RGMII_RX D[0]	-	CANFD1_ RX	UART 0_RTS_B	SPI1_SS2_ B	LPD_I2C1 _SDA	SWDT1_R ST	TTC 2_WAVE
	NA	PMC_MIO 46_501	PMC_G PIO46	-	SD0/EMM C0_DIR_C MD/DATA [5]	-	-	-	SD0/EMM C0: DIR_CMD /DATA[5]	-	-	-	-	-	-	SMAP_IO[26]	-	GEM1: RGMII_RX D[1]	PMC_I2C _SCL	CANFD0_ RX	UART 1_TXD	SPI1_SS1_ B	LPD_I2C0 _SCL	SWDT1_R ST_PEND	TTC 1_CLK
	NA	PMC_MIO 47_501	PMC_G PIO47	-	SD0/EMM C0_DIR0/ DATA[6]	-	-	-	SD0/EMM C0: DIR0/DAT A[6]	-	-	-	-	-	-	SMAP_IO[27]	-	GEM1: RGMII_RX D[2]	PMC_I2C _SDA	CANFD0_ TX	UART 1_RXD	SPI1_SS0_ B	LPD_I2C0 _SDA	SWDT1_I NT	TTC 1_WAVE
	NA	PMC_MIO 48_501	PMC_G PIO48	-	SD0/EMM C0_DIR1/ DATA[7]	-	-	-	SD0/EMM C0: DIR1/DAT A[7]	-	-	-	-	-	-	SMAP_IO[28]	-	GEM1: RGMII_RX D[3]	-	CANFD1_ TX	UART 1_RTS_B	SPI1_MSI O	LPD_I2C1 _SCL	SWDT1_ WS0	TTC 0_CLK
	NA	PMC_MIO 49_501	PMC_G PIO49	SD0/EMMC 0_BUSPWR /RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0: BUSPWR/ RST	-	-	-	-	-	-	SMAP_IO[29]	-	GEM1: RGMII_RX _CTL	-	CANFD1_ RX	UART 1_CTS_B	SPI1_MO SI	LPD_I2C1 _SDA	SWDT1_ WS1	TTC 0_WAVE
QSPI	NA	PMC_MIO 0_500	PMC_G PIO0	QSPI0_CLK	QSPI0_CL K	QSPI0_CL K	QSPI0_CL K	QSPI0_CL K	QSPI0_CL K	QSPI0_CL K	QSPI0_CL K	OSPI_CLK	OSPI_CLK	SD1/EMM C1: CLK	SD1/EMM C1_CLK	SD1/EMM C1_CLK	SD1/EMM C1: CLK	SD1/EMM C1_CLK	SD1/EMM C1_CLK	-	CANFD0_ RX	UART 0_RXD	SPI0_SCLK	LPD_I2C1 _SCL	SWDT0_C LK	TTC3_CLK
	NA	PMC_MIO 1_500	PMC_G PIO1	QSPI0_IO[1]	QSPI0_IO[1]	QSPI0_IO[1]	QSPI: QSPI0_IO[1]	QSPI0_IO[1]	QSPI0_IO[1]	QSPI0_IO[1]	QSPI0_IO[1]	OSPI_IO[0]	OSPI_IO[0]	SD1_WP	SD1_WP	SD1: WP	-	-	-	-	CANFD0_ TX	UART 0_TXD	SPI0_SS2_ B	LPD_I2C1 _SDA	SWDT0_R ST	TTC3_WA VE
	NA	PMC_MIO 2_500	PMC_G PIO2	-	-	QSPI0_IO[2]		QSPI0_IO[2]	QSPI0_IO[2]	QSPI0_IO[2]	QSPI0_IO[2]	OSPI_IO[1]	OSPI_IO[1]	SD1: DETECT	SD1_DETE CT	SD1: DETECT	-	-	-	PMC_I2C _SCL	CANFD1_ TX	UART 0_CTS_B	SPI0_SS1_ B	LPD_I2C0 _SCL	SWDT0_R ST_PEND	TTC 2_CLK
	NA	PMC_MIO 3_500	PMC_G PIO3	-	-	QSPI0_IO[3]		QSPI0_IO[3]	QSPI0_IO[3]	QSPI0_IO[3]	QSPI0_IO[3]	OSPI_IO[2]	OSPI_IO[2]	SD1/EMM C1: CMD	SD1/EMM C1_CMD	SD1/EMM C1_CMD	SD1/EMM C1: CMD	SD1/EMM C1_CMD	SD1/EMM C1_CMD	PMC_I2C _SDA	CANFD1_ RX	UART 0_RTS_B	SPI0_SS0_ B	LPD_I2C0 _SDA	SWDT0_I NT	TTC 2_WAVE
	NA	PMC_MIO 4_500	PMC_G PIO4	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	QSPI0_IO[0]	OSPI_IO[3]	OSPI_IO[3]	SD1/EMM C1: DATA[0]	SD1/EMM C1_DATA[0]	SD1/EMM C1_DATA[0]	SD1/EMM C1: DATA[0]	SD1/EMM C1_DATA[0]	SD1/EMM C1_DATA[0]	-	CANFD0_ RX	UART 1_TXD	SPI0_MSI O	LPD_I2C1 _SCL	SWDT0_ WS0	TTC 1_CLK

Interface/ Function	B2B PIN No.	SoC pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19	Function 20	Function 21	Function 22
	NA	PMC_MIO 5_500	PMC_G PIO5	QSPI0_CS_B	QSPI0_CS _B	QSPI0_CS _B	QSPI0_CS _B	QSPI0_CS _B	QSPI0_CS _B	QSPI0_CS _B	OSPI_IO[4]	OSPI_IO[4]	SD1/EMM C1: DATA[1]	SD1/EMM C1_DATA[1]	SD1/EMM C1_DATA[1]	-	SD1/EMM C1_DATA[1]	SD1/EMM C1_DATA[1]	-	CANFD0_ TX	UART 1_RXD	SPI0_MO SI	LPD_I2C1 _SDA	SWDT0_ WS1	TTC 1_WAVE
USB 2.0	NA	PMC_MIO 13_500	PMC_G PIO13	SD0/EMMC 0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	SD0/EMM C0_DATA[0]	USB_ULPI _RST	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 1_RXD	SPI0_SS2_ B	LPD_I2C1 _SDA	SWDT0_R ST	TTC 1_WAVE
	NA	PMC_MIO 14_500	PMC_G PIO14	SD0/EMMC 0_DATA[1]	SD0/EMM C0_DATA[1]	SD0/EMM C0_DATA[1]	-	SD0/EMM C0_DATA[1]	SD0/EMM C0_DATA[1]	USB_ULPI _DATA[0]	-	-	-	-	-	SMAP_IO[0]	-	-	PMC_I2C _SCL	CANFD1_ TX	UART 1_RTS_B	SPI0_SS1_ B	LPD_I2C0 _SCL	SWDT0_R ST_PEND	TTC 0_CLK
	NA	PMC_MIO 15_500	PMC_G PIO15	SD0/EMMC 0_DATA[2]	SD0/EMM C0_DATA[2]	SD0/EMM C0_DATA[2]	-	SD0/EMM C0_DATA[2]	SD0/EMM C0_DATA[2]	USB_ULPI _DATA[1]	-	-	-	-	-	SMAP_IO[1]	-	-	PMC_I2C _SDA	CANFD1_ RX	UART 1_CTS_B	SPI0_SS0_ B	LPD_I2C0 _SDA	SWDT0_I NT	TTC 0_WAVE
	NA	PMC_MIO 16_500	PMC_G PIO16	SD0/EMMC 0_DATA[3]	SD0/EMM C0_DATA[3]	SD0/EMM C0_DATA[3]	-	SD0/EMM C0: DATA[3]	SD0/EMM C0_DATA[3]	USB_ULPI _DATA[2]	-	-	-	-	-	SMAP_IO[2]	-	-	-	CANFD0_ RX	UART 0_RXD	SPI0_MSI O	LPD_I2C1 _SCL	SWDT0_ WS0	TTC 3_CLK
	NA	PMC_MIO 17_500	PMC_G PIO17	SD0/EMMC 0_BUSPWR /RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	SD0/EMM C0_BUSP WR/RST	USB_ULPI _DATA[3]	-	-	-	-	-	SMAP_IO[3]	-	-	-	CANFD0_ TX	UART 0_TXD	SPI0_MO SI	LPD_I2C1 _SDA	SWDT0_ WS1	TTC 3_WAVE
	NA	PMC_MIO 18_500	PMC_G PIO18	SD0/EMMC 0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	SD0/EMM C0_CLK	USB_ULPI _CLK	-	-	-	-	-	SMAP_CL K	-	-	PMC_I2C _SCL	CANFD1_ TX	UART 0_CTS_B	SPI1_SCLK	LPD_I2C0 _SCL	SWDT1_C LK	TTC 2_CLK
	NA	PMC_MIO 19_500	PMC_G PIO19	-	SD0/EMM C0_SEL/D ATA[4]	SD0/EMM C0_SEL/D ATA[4]	-	-	SD0/EMM C0_SEL/D ATA[4]	USB_ULPI _DATA[4]	-	-	-	-	-	SMAP_CS _B	-	-	PMC_I2C _SDA	CANFD1_ RX	UART 0_RTS_B	SPI1_SS2_ B	LPD_I2C0 _SDA	SWDT1_R ST	TTC 2_WAVE
	NA	PMC_MIO 20_500	PMC_G PIO20	-	SD0/EMM C0_DIR_C MD/DATA [5]	-	-	-	SD0/EMM C0_DIR_C MD/DATA [5]	USB_ULPI _DATA[5]	-	-	-	-	-	SMAP_RD WR_B	-	-	-	CANFD0_ RX	UART 1_TXD	SPI1_SS1_ B	LPD_I2C1 _SCL	SWDT1_R ST_PEND	TTC 1_CLK
	NA	PMC_MIO 21_500	PMC_G PIO21	-	SD0/EMM C0_DIR0/ DATA[6]	-	-	-	SD0/EMM C0_DIR0/ DATA[6]	USB_ULPI _DATA[6]	-	-	-	-	-	SMAP_BU SY	-	-	-	CANFD0_ TX	UART 1_RXD	SPI1_SS0_ B	LPD_I2C1 _SDA	SWDT1_I NT	TTC 1_WAVE
	NA	PMC_MIO 22_500	PMC_G PIO22	-	SD0/EMM C0_DIR1/ DATA[7]	-	-	-	SD0/EMM C0_DIR1/ DATA[7]	USB_ULPI _DATA[7]	-	-	-	-	-	SMAP_IO[4]	-	-	PMC_I2C _SCL	CANFD1_ TX	UART 1_RTS_B	SPI1_MSI O	LPD_I2C0 _SCL	SWDT1_ WS0	TTC 0_CLK
	NA	PMC_MIO 23_500	PMC_G PIO23	SD0/EMMC 0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	SD0/EMM C0_CMD	USB_ULPI _DIR	-	-	-	-	-	SMAP_IO[5]	-	-	PMC_I2C _SDA	CANFD1_ RX	UART 1_CTS_B	SPI1_MO SI	LPD_I2C0 _SDA	SWDT1_ WS1	TTC 0_WAVE
	NA	PMC_MIO 24_500	PMC_G PIO24	SD0_DETEC T	SD0_DETE CT	SD0_DETE CT	-	-	-	USB_ULPI _STP	-	-	-	-	-	SMAP_IO[6]	-	-	-	-	-	-	-	-	-
	NA	PMC_MIO 25_500	PMC_G PIO25	SD0_WP	SD0_WP	SD0_WP	-	-	-	USB_ULPI _NXT	-	-	-	-	-	SMAP_IO[7]	-	-	-	-	-	-	-	-	-
GEM0	NA	LPD_MIO0 _502	LPD_GP IO0	GEM0_TX_ CLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 0_RXD	SPI0_SCLK	LPD_I2C1 _SCL	SWDT0_C LK	TTC 3_CLK
	NA	LPD_MIO1 _502	LPD_GP IO1	GEM0_TXD[0]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ RX	UART 0_TXD	SPI0_SS2_ B	LPD_I2C1 _SDA	SWDT0_R ST	TTC 3_WAVE
	NA	LPD_MIO2 _502	LPD_GP IO2	GEM0_TXD[1]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ RX	UART 0_CTS_B	SPI0_SS1_ B	LPD_I2C0 _SCL	SWDT0_R ST_PEND	TTC 2_CLK
	NA	LPD_MIO3 _502	LPD_GP IO3	GEM0_TXD[2]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 0_RTS_B	SPI0_SS0_ B	LPD_I2C0 _SDA	SWDT0_I NT	TTC 2_WAVE
	NA	LPD_MIO4 _502	LPD_GP IO4	GEM0_TXD[3]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 1_TXD	SPI0_MSI O	LPD_I2C1 _SCL	SWDT0_ WS0	TTC 1_CLK
	NA	LPD_MIO5 _502	LPD_GP IO5	GEM0_TX_ CTRL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ RX	UART 1_RXD	SPI0_MO SI	LPD_I2C1 _SDA	SWDT0_ WS1	TTC 1_WAVE
	NA	LPD_MIO6 _502	LPD_GP IO6	GEM0_RX_ CLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ RX	UART 1_RTS_B	SPI1_SCLK	LPD_I2C0 _SCL	SWDT1_C LK	TTC 0_CLK
	NA	LPD_MIO7 _502	LPD_GP IO7	GEM0_RXD [0]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 1_CTS_B	SPI1_SS2_ B	LPD_I2C0 _SDA	SWDT1_R ST	TTC 0_WAVE
	NA	LPD_MIO8 _502	LPD_GP IO8	GEM0_RXD [1]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 0_RXD	SPI1_SS1_ B	LPD_I2C1 _SCL	SWDT1_R ST_PEND	TTC 3_CLK

Interface/ Function	B2B PIN No.	SoC pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19	Function 20	Function 21	Function 22
	NA	LPD_MIO9_502	LPD_GPIO9	GEM0_RXD[2]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_RX	UART0_TXD	SPI1_SS0_B	LPD_I2C1_SDA	SWDT1_INT	TTC 3_WAVE
	NA	LPD_MIO10_502	LPD_GPIO10	GEM0_RXD[3]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_RX	UART0_CTS_B	SPI1_MSIO	LPD_I2C0_SCL	SWDT1_WS0	TTC 2_CLK
	NA	LPD_MIO11_502	LPD_GPIO11	GEM0_RX_CTRL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_TX	UART0_RTS_B	SPI1_MOSI	LPD_I2C0_SDA	SWDT1_WS1	TTC 2_WAVE
Board to Board Connector Interfaces from PS MIO																									
SPI	B17	PMC_MIO6_500	PMC_GPIO6	QSPI_LPBK	LOOPBACK CLK: QSPI_LPBK	LOOPBACK CLK: QSPI_LPBK	QSPI_LPBK	QSPI_LPBK	QSPI_LPBK	QSPI_LPBK	OSPI_DS	OSPI_DS	SD1/EMMC1: DATA[2]	SD1/EMMC1_DATA[2]	SD1/EMMC1_DATA[2]	-	SD1/EMMC1_DATA[2]	SD1/EMMC1_DATA[2]	PMC_I2C_SCL	CANFD1_TX	UART1_RTS_B	SPI1_SCLK	LPD_I2C0_SCL	SWDT1_CLK	TTC 0_CLK
	B20	PMC_MIO7_500	PMC_GPIO7	-	-	-	QSPI1_CS_B	QSPI1_CS_B	QSPI: QSPI1_CS_B	QSPI1_CS_B	OSPI_IO[5]	OSPI_IO[5]	SD1/EMMC1: DATA[3]	SD1/EMMC1_DATA[3]	SD1/EMMC1_DATA[3]	-	-	SD1/EMMC1_DATA[3]	PMC_I2C_SDA	CANFD1_RX	UART1_CTS_B	SPI1_SS2_B	LPD_I2C0_SDA	SWDT1_RST	TTC 0_WAVE
	B21	PMC_MIO8_500	PMC_GPIO8	-	-	-	-	-	-	QSPI1_IO[0]	OSPI_IO[6]	OSPI_IO[6]	-	SD1/EMMC1_SEL/DATA[4]	SD1/EMMC1_SEL/DATA[4]	-	-	SD1/EMMC1_SEL/DATA[4]	-	CANFD0_RX	UART0_RXD	SPI1_SS1_B	LPD_I2C1_SCL	SWDT1_RST_PEND	TTC 3_CLK
	B22	PMC_MIO9_500	PMC_GPIO9	-	-	-	-	-	-	QSPI1_IO[1]	OSPI_IO[7]	OSPI_IO[7]	-	SD1/EMMC1_DIR_CMD/DATA[5]	-	-	-	SD1/EMMC1_DIR_CMD/DATA[5]	-	CANFD0_TX	UART0_TXD	SPI1_SS0_B	LPD_I2C1_SDA	SWDT1_INT	TTC 3_WAVE
	B19	PMC_MIO10_500	PMC_GPIO10	-	-	-	-	-	-	QSPI1_IO[2]	OSPI0_CS_B	OSPI0_CS_B	-	SD1/EMMC1_DIR0/DATA[6]	-	-	-	SD1/EMMC1_DIR0/DATA[6]	PMC_I2C_SCL	CANFD1_TX	UART0_CTS_B	SPI1_MSIO	LPD_I2C0_SCL	SWDT1_WS0	TTC 2_CLK
	B18	PMC_MIO11_500	PMC_GPIO11	-	-	-	-	-	-	QSPI1_IO[3]	-	OSPI1_CS_B	-	SD1/EMMC1_DIR1/DATA[7]	-	-	-	SD1/EMMC1_DIR1/DATA[7]	PMC_I2C_SDA	CANFD1_RX	UART0_RTS_B	SPI1_MOSI	LPD_I2C0_SDA	SWDT1_WS1	TTC 2_WAVE
GPIO	NA	PMC_MIO12_500	PMC_GPIO12	-	-	-	-	-	-	QSPI1_CLK	-	-	SD1/EMMC1_BUSPWR/RST	SD1/EMMC1_BUSPWR/RST	SD1/EMMC1_BUSPWR/RST	SD1/EMMC1_BUSPWR/RST	SD1/EMMC1_BUSPWR/RST	SD1/EMMC1_BUSPWR/RST	-	CANFD0_RX	UART1_TXD	SPI0_SCLK	LPD_I2C1_SCL	SWDT0_CLK	TTC 1_CLK
SD1	A17	PMC_MIO26_501	PMC_GPIO26	-	-	-	-	-	-	SD1/EMMC1_CLK	SD1/EMMC1_CLK	SD1/EMMC1_CLK	SD1/EMMC1_CLK	SD1/EMMC1_CLK	SD1/EMMC1_CLK	-	GEM0_TX_CLK	-	PMC_I2C_SCL	CANFD0_RX	UART0_RXD	SPI0_SCLK	LPD_I2C0_SCL	SWDT0_CLK	TTC 3_CLK
	A25	PMC_MIO27_501	PMC_GPIO27	-	-	-	-	-	-		SD1/EMMC1_DIR1/DATA[7]	-	-	-	SD1/EMMC1_DIR1/DATA[7]	-	GEM0_TXD[0]	-	PMC_I2C_SDA	CANFD0_TX	UART0_TXD	SPI0_SS2_B	LPD_I2C0_SDA	SWDT0_RST	TTC 3_WAVE
	A24	PMC_MIO28_501	PMC_GPIO28	-	-	-	-	-	-	SD1: DETECT	SD1_DETECT	SD1_DETECT	-	-	-	SMAP_IO[8]	GEM0_TXD[1]	-	-	CANFD1_TX	UART0_CTS_B	SPI0_SS1_B	LPD_I2C1_SCL	SWDT0_RST_PEND	TTC 2_CLK
	A18	PMC_MIO29_501	PMC_GPIO29	-	-	-	-	-	-	SD1/EMMC1_CMD	SD1/EMMC1_CMD	SD1/EMMC1_CMD	SD1/EMMC1_CMD	SD1/EMMC1_CMD	SD1/EMMC1_CMD	SMAP_IO[9]	GEM0_TXD[2]	-	-	CANFD1_RX	UART0_RTS_B	SPI0_SS0_B	LPD_I2C1_SDA	SWDT0_INT	TTC 2_WAVE
	A19	PMC_MIO30_501	PMC_GPIO30	-	-	-	-	-	-	SD1/EMMC1_DATA[0]	SD1/EMMC1_DATA[0]	SD1/EMMC1_DATA[0]	SD1/EMMC1_DATA[0]	SD1/EMMC1_DATA[0]	SD1/EMMC1_DATA[0]	SMAP_IO[10]	GEM0_TXD[3]	-	PMC_I2C_SCL	CANFD0_RX	UART1_TXD	SPI0_MSIO	LPD_I2C0_SCL	SWDT0_WS0	TTC 1_CLK
	A20	PMC_MIO31_501	PMC_GPIO31	-	-	-	-	-	-	SD1/EMMC1_DATA[1]	SD1/EMMC1_DATA[1]	SD1/EMMC1_DATA[1]	-	SD1/EMMC1_DATA[1]	SD1/EMMC1_DATA[1]	SMAP_IO[11]	GEM0_TX_CTRL	-	PMC_I2C_SDA	CANFD0_TX	UART1_RXD	SPI0_MOSI	LPD_I2C0_SDA	SWDT0_WS1	TTC 1_WAVE
	A21	PMC_MIO32_501	PMC_GPIO32	-	-	-	-	-	-	SD1/EMMC1_DATA[2]	SD1/EMMC1_DATA[2]	SD1/EMMC1_DATA[2]	-	SD1/EMMC1_DATA[2]	SD1/EMMC1_DATA[2]	SMAP_IO[12]	GEM0_RX_CLK	-	-	CANFD1_TX	UART1_RTS_B	SPI1_SCLK	LPD_I2C1_SCL	SWDT1_CLK	TTC 0_CLK
	A22	PMC_MIO33_501	PMC_GPIO33	-	-	-	-	-	-	SD1/EMMC1_DATA[3]	SD1/EMMC1_DATA[3]	SD1/EMMC1_DATA[3]	-	SD1/EMMC1_DATA[3]	SD1/EMMC1_DATA[3]	SMAP_IO[13]	GEM0_RXD[0]	-	-	CANFD1_RX	UART1_CTS_B	SPI1_SS2_B	LPD_I2C1_SDA	SWDT1_RST	TTC 0_WAVE
UART0	A31	PMC_MIO34_501	PMC_GPIO34	-	-	-	-	-	-	-	SD1/EMMC1_SEL/DATA[4]	SD1/EMMC1_SEL/DATA[4]	-	-	SD1/EMMC1_SEL/DATA[4]	SMAP_IO[14]	GEM0_RXD[1]	-	PMC_I2C_SCL	CANFD0_RX	UART0_RXD	SPI1_SS1_B	LPD_I2C0_SCL	SWDT1_RST_PEND	TTC 3_CLK
	A30	PMC_MIO35_501	PMC_GPIO35	-	-	-	-	-	-	-	SD1/EMMC1_DIR_CMD/DATA[5]	-	-	-	SD1/EMMC1_DIR_CMD/DATA[5]	SMAP_IO[15]	GEM0_RXD[2]	-	PMC_I2C_SDA	CANFD0_TX	UART0_TXD	SPI1_SS0_B	LPD_I2C0_SDA	SWDT1_INT	TTC 3_WAVE

Interface/ Function	B2B PIN No.	SoC pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13	Function 14	Function 15	Function 16	Function 17	Function 18	Function 19	Function 20	Function 21	Function 22
CANFD1	D25	PMC_MIO 36_501	PMC_G PIO36	-	-	-	-	-	-	-	SD1/EMM C1_DIR0/ DATA[6]	-	-	-	SD1/EMM C1_DIR0/ DATA[6]	SMAP_I O[16]	GEM0_RX D[3]	-	-	CANFD1_ TX	UART 0_CTS_B	SPI1_MSI O	LPD_I2C1 _SCL	SWDT1_ WS0	TTC 2_CLK
	D24	PMC_MIO 37_501	PMC_G PIO37	SD0: WP	SD0: WP	SD0: WP	-	-	-	-	-	-	-	-	-	SMAP_IO[17]	GEM0_RX _CTRL	-	-	CANFD1_ RX	UART 0_RTS_B	SPI1_MO SI	LPD_I2C1 _SDA	SWDT1_ WS1	TTC 2_WAVE
I2C	A28	PMC_MIO 50_501	PMC_G PIO50	GEM0_MDI O_CLK	GEM1_M DIO_CLK	GEM_TSU _CLK	-	-	-	SD1_WP	SD1_WP	SD1_WP	-	-	-	SMAP_IO[30]	GEM0_M DIO_CLK	GEM1_M DIO_CLK	PMC_I2C _SCL	-	-	-	-	-	-
	A29	PMC_MIO 51_501	PMC_G PIO51	GEM0_MDI O_DATA	GEM1_M DIO_DATA	GEM_TSU _CLK	-	-	-	SD1/EMM C1_BUSP WR/RST	SD1/EMM C1_BUSP WR/RST	SD1/EMM C1_BUSP WR/RST	SD1/EMM C1_BUSP WR/RST	SD1/EMM C1_BUSP WR/RST	SD1/EMM C1_BUSP WR/RST	SMAP_IO[31]	GEM0_M DIO_DATA	GEM1_M DIO_DATA	PMC_I2C _SDA	-	-	-	-	-	-
GEM1	C17	LPD_MIO1 2_502	LPD_GP IO12	-	GEM1_TX _CLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 1_TXD	SPI0_SCLK	LPD_I2C1 _SCL	SWDT0_C LK	TTC 1_CLK
	C18	LPD_MIO1 3_502	LPD_GP IO13	-	GEM1_TX D[0]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ RX	UART 1_RXD	SPI0_SS2_ B	LPD_I2C1 _SDA	SWDT0_R ST	TTC 1_WAVE
	C19	LPD_MIO1 4_502	LPD_GP IO14	-	GEM1_TX D[1]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ RX	UART 1_RTS_B	SPI0_SS1_ B	LPD_I2C0 _SCL	SWDT0_R ST_PEND	TTC 0_CLK
	C20	LPD_MIO1 5_502	LPD_GP IO15	-	GEM1_TX D[2]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 1_CTS_B	SPI0_SS0_ B	LPD_I2C0 _SDA	SWDT0_I NT	TTC 0_WAVE
	C21	LPD_MIO1 6_502	LPD_GP IO16	-	GEM1_TX D[3]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 0_RXD	SPI0_MSI O	LPD_I2C1 _SCL	SWDT0_ WS0	TTC 3_CLK
	C22	LPD_MIO1 7_502	LPD_GP IO17	-	GEM1_TX _CTRL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ RX	UART 0_TXD	SPI0_MO SI	LPD_I2C1 _SDA	SWDT0_ WS1	TTC 3_WAVE
	D17	LPD_MIO1 8_502	LPD_GP IO18	-	GEM1_RX _CLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ RX	UART 0_CTS_B	SPI1_SCLK	LPD_I2C0 _SCL	SWDT1_C LK	TTC 2_CLK
	D18	LPD_MIO1 9_502	LPD_GP IO19	-	GEM1_RX D[0]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 0_RTS_B	SPI1_SS2_ B	LPD_I2C0 _SDA	SWDT1_R ST	TTC 2_WAVE
	D19	LPD_MIO2 0_502	LPD_GP IO20	-	GEM1_RX D[1]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ TX	UART 1_TXD	SPI1_SS1_ B	LPD_I2C1 _SCL	SWDT1_R ST_PEND	TTC 1_CLK
	D20	LPD_MIO2 1_502	LPD_GP IO21	-	GEM1_RX D[2]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD1_ RX	UART 1_RXD	SPI1_SS0_ B	LPD_I2C1 _SDA	SWDT1_I NT	TTC 1_WAVE
	D21	LPD_MIO2 2_502	LPD_GP IO22	-	GEM1_RX D[3]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ RX	UART 1_RTS_B	SPI1_MSI O	LPD_I2C0 _SCL	SWDT1_ WS0	TTC 0_CLK
	D22	LPD_MIO2 3_502	LPD_GP IO23	-	GEM1_RX _CTRL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CANFD0_ TX	UART 1_CTS_B	SPI1_MO SI	LPD_I2C0 _SDA	SWDT1_ WS1	TTC 0_WAVE
	C24	LPD_MIO2 4_502	LPD_GP IO24	GEM0_MDI O_CLK	GEM0_M DIO_CLK	GEM_TSU _CLK	-	-	-	-	-	-	-	-	-	-	GEM0_M DIO_CLK	GEM1_M DIO_CLK		CANFD1_ TX			LPD_I2C1 _SCL		
	C25	LPD_MIO2 5_502	LPD_GP IO25	GEM0_MDI O_DATA	GEM0_M DIO_DATA	GEM_TSU _CLK	-	-	-	-	-	-	-	-	-	-	GEM0_M DIO_DATA	GEM1_M DIO_DATA		CANFD1_ RX			LPD_I2C1 _SDA		
JTAG	A9	TCK_503	-	JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	A12	TDI_503	-	JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	A11	TDO_503	-	JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	A10	TMS_503	-	JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

3.Technical Specification

This section provides detailed information about the Versal premium SOM technical specification with Electrical, Environmental and Mechanical characteristics

3.1 Electrical Specification

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Versal Premium SOM.

Table 34: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V [2]	0V	3V	3.15V	±20mV

[1] Versal premium SOM is designed to work with VCC_12V input power rail from Board-to-Board Connector 2.

[2] Versal premium SOM uses this voltage as backup power source to PMIC RTC when VCC_12V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Output Specification

The Versal Premium SOM provides and extension of XPIO Bank and HDIO Bank Supply voltage to the Board-to-Board Connectors for various uses like IO Level shifting etc.

Table 35: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
1	VCCO_XPIO_703	1.0V	1.2V	1.5V	50mA
2	VCCO_XPIO_704	1.0V	1.2V	1.5V	50mA
3	VCCO_XPIO_705	1.0V	1.2V	1.5V	50mA
4	VCCO_XPIO_712	1.0V	1.2V	1.5V	50mA
5	VCCO_HDIO	1.2V	1.8V	3.2V	50mA

3.2 Environmental Characteristics.

3.2.1 Temperature Specification

The below table provides the Environment specification of Versal Premium SOM.

Table 36: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Versal Premium SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Versal Premium SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 Versal Premium SOM Mechanical Dimensions

Versal Premium SOM PCB size is T115mm x 82mm. SOM mechanical dimension is shown below.

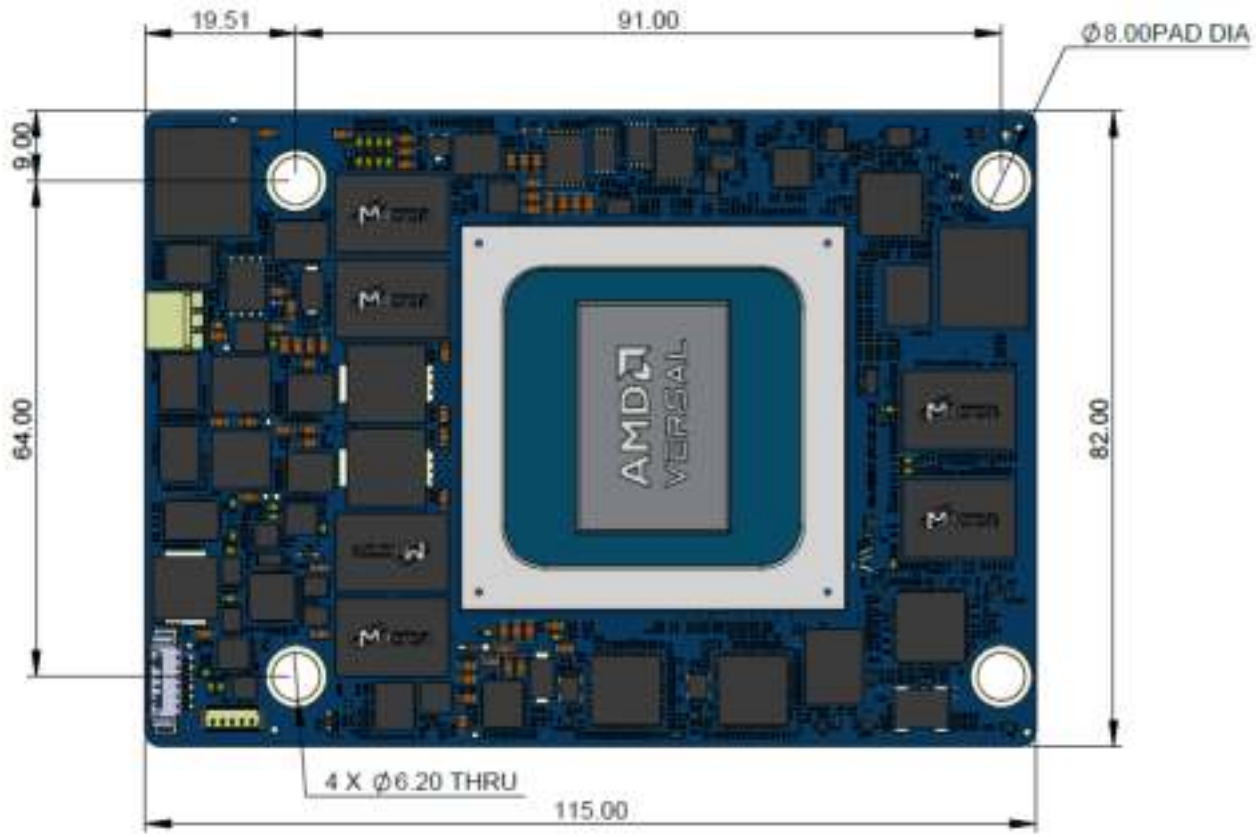


Figure 7: Mechanical dimension of Versal Premium SOM - Top View

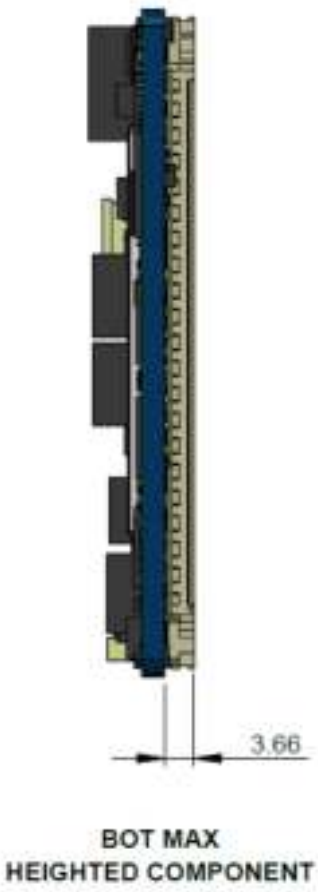


Figure 8: Mechanical dimension of Versal Premium SOM - Side View

4.Ordering Information

The below table provides the standard orderable part numbers for different Versal premium SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave

Table 37: Orderable Product Part Numbers

Product Part Number	Description	Temperature
TBD	TBD	TBD

5.APPENDIX

5.1 Bank Migration in Board-to-Board Connectors

The Versal premium SOM contains Three board-to-board connectors supporting high-speed transceiver banks, high-performance IOs, and interfaces to the carrier board. The Versal premium SOM supports several compatible FPGA devices with the VSVA2785 package and accommodates all speed grades FPGA chips.

Supported Transceiver banks by the following SoC is given in the table below.

Device / Connector	VP1102	VP1202	VP1402	VP1502	VP1552
Board To Board Connector- 1	GTM 107	NA	GTM 107	NA	NA
Board To Board Connector-- 2	GTM 106	GTYP 106	GTM 106	GTYP 106	GTYP 106
	GTM 109	NA	GTM 109	GTYP 110	GTYP 110
	GTM 202	GTM 202	GTM 202	GTM 202	GTM 202
	GTYP LPD 102	GTYP LPD 102	GTYP LPD 102	GTYP LPD 102	GTYP LPD 102
	GTYP LPD 103	GTYP LPD 103	GTYP LPD 103	GTYP LPD 103	GTYP LPD 103
	GTM 104	GTYP LPD 104	GTM 104	GTYP LPD 104	GTYP LPD 104
	GTM 105	GTYP LPD 105	GTM 105	GTYP LPD 105	GTYP LPD 105
	GTM 200	GTYP 200	GTM 200	GTYP 200	GTYP 200
Board To Board Connector- 3	GTM 201	GTYP 201	GTM 201	GTYP 201	GTYP 201
	GTM 207	NA	GTM 207	GTM 208	GTYP 208
	GTM 208	NA	GTM 208	GTM 209	GTYP 209
	GTM 209	NA	GTM 209	GTM 210	GTYP 210
	NA	NA	GTM 210	GTM 211	GTYP 211
	GTM 205	GTM 205	GTM 205	GTM 205	GTM 205
	GTM 204	GTM 204	GTM 204	GTM 204	GTM 204
	GTM 206	GTM 206	GTM 206	GTM 207	GTYP 207
	GTM 108	NA	GTM 108	GTYP 109	GTYP 109
	GTM 203	GTM 203	GTM 203	GTM 203	GTM 203
	NA	NA	GTM 110	GTYP 111	GTYP 111
	NA	NA	GTM 111	GTYP 112	GTYP 112
	NA	NA	GTM 211	GTM 212	GTYP 212

Supported XPIO banks by the following SoC is given in the table below.

Device / Connector	VP1102	VP1202	VP1402	VP1502	VP1552
Board To Board Connector- 1	XPIO 703	XPIO 703	XPIO 703	XPIO 703	XPIO 703
	XPIO 704	XPIO 704	XPIO 704	XPIO 704	XPIO 704
	XPIO 705	XPIO 705	XPIO 705	XPIO 705	XPIO 705
	NA	XPIO 712	NA	XPIO 712	XPIO 712
	NA	NA	HDIO 612 & 613	NA	NA

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