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Altera Agilex 7 SoC FPGA (R24C) SOM Hardware Datasheet

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware Datasheet for the **Altera Agilex 7 SoC FPGA(R24C) System on Module**. This board is fully supported by iWave Global. This Guide provides detailed information on the overall design and usage of the Altera Agilex 7 SoC FPGA System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The **Altera Agilex 7 SoC FPGA (R24C) SOM** is an extension of **Altera Agilex 7 SoC FPGA(R24C) SoC FPGA**. Altera Agilex 7 SoC FPGA (R24C) SOM has a form factor of 110mm x 75mm and provides the functional requirements for an embedded application. Two High-Speed High-Density ruggedized terminal strip connectors and One High-Speed High-Density connectors that facilitates the carrier board interfaces to carry all the I/O signals to and from the Altera Agilex 7 SoC FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NPTH	Non-Plated Through hole

Acronyms	Abbreviations
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On the Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Altera Agilex 7 Hard Processor Systems Technical Reference Manual.
- Altera Agilex 7 Device Data Sheet.
- Altera Agilex 7 Device Design Guidelines.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Altera Agilex 7 SoC FPGA (R24C) SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about Board-to-Board connectors pin assignment and usage.

2.1 Altera Agilex 7 SoC FPGA (R24C) SOM Block Diagram

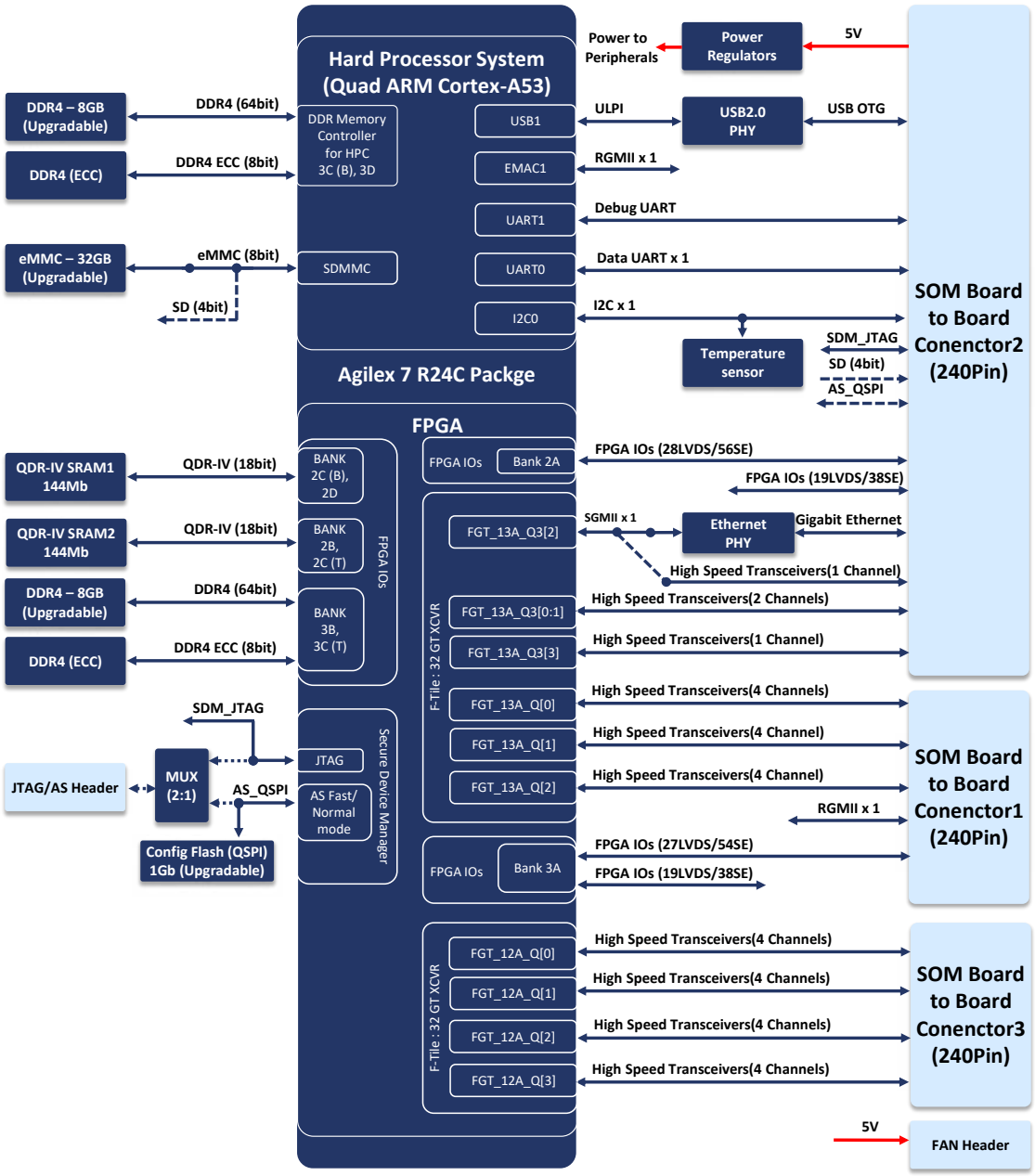

Figure 1: Altera Agilex 7 SoC FPGA SOM Block Diagram

2.2 Altera Agilex 7 SoC FPGA SOM Features

The Altera Agilex 7 SoC FPGA (R24C) SOM supports the following features.

SoC

- The Altera Agilex 7 SoC FPGA
  - Compatible Agilex 7 F-Series – Agilex 7 AGF 006, AGF 008, AGF 012, AGF 014, AGF 019, AGF 022, AGF 023, AGF 027
    - Hard Processing System (HPS)
      - Quad-core 64-bit Arm Cortex-A53 up to 1.50 GHz
    - Field Programmable Gate Array (FPGA)
      - Up to 2,692,760 Logic elements
      - 32 x FGT transceivers up to 32Gbps in NRZ or 58Gbps in PAM4 Format

Power

- Discrete Power Regulators

Memory

- 8GB DDR4 SDRAM (64bit + 8bit) with ECC for HPS (Expandable)[1]
- 8GB DDR4 SDRAM (64bit + 8bit) with ECC for FPGA (Expandable)[1]
- 2 x 144Mb QDR-IV (18bit) for FPGA
- 1Gb QSPI Flash (Expandable)[1]
- 32GB eMMC Flash (Expandable)[1]
- 4Kb EEPROM

Other On-SOM Features

- Gigabit Ethernet PHY Transceiver[2]
- USB2.0 Transceiver
- Clock Synchronizer
- Temperature sensor
- JTAG/Active Serial Header
- Fan Header

Board to Board Connector1 Interfaces (240pin)

From FPGA Block

- 12 x FGT transceivers up to 17Gbps (NRZ)[3]
- 27 LVDS/54SE FPGA IOs from Bank 3A

From HPS Block

- 1 x RGMII Interface

Board to Board Connector2 Interfaces (240pin)

From HPS Block

- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port (Optional)
- Debug UART x 1 Port
- Data UART x 1 Port (With CTS and RTS)
- I2C x 1 Ports

From SDM Block

- JTAG x 1
- AS x 1 (Active Serial x4)

From HPS to FPGA Block

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver) [2]

From FPGA Block

- 4 x FGT transceivers up to 17Gbps (NRZ) [3]
- 20 LVDS/40SE FPGA IOs from Bank 3A
- 28 LVDS/56SE FPGA IOs from Bank 2A

Board to Board Connector3 Interfaces (240pin)

From FPGA Block

- 16 x FGT transceivers up to 32Gbps (NRZ) or up to 56Gbps (PAM4)[3]

General Specification

- Power Supply **:** 5V (from Board-to-Board Connector2)
- Form Factor **:** 110mm x 75mm (OREN+).

[1] The Expansion of DDR4, QSPI Flash and eMMC size/capacity are subject to availability of chips in market.

[2] These interfaces are routed from HPS to FPGA.

[3] F-Tile: Quad0 transceivers from all FGT banks do not support PAM4 speed; they only support NRZ 32Gbps.

2.3 Altera Agilex 7 SoC FPGA (R24C)

Altera Agilex 7 FPGAs and SoCs are built using an innovative chiplet architecture, which provides agile and flexible integration of heterogeneous technology elements in a System-in-Package (SiP). The chiplet architecture enables Altera to address a broad array of acceleration and high-bandwidth applications with tailored and flexible solutions. Leveraging advanced 3D packaging technology such as Altera Embedded Multi-Die Interconnect Bridge (EMIB), the chiplet approach allows the combination of traditional FPGA die with purpose-built semiconductor die to create devices that are uniquely optimized for target applications.

The Altera® Agilex 7™ F-Series 10-nm SuperFin technology FPGAs and SoCs deliver on average 50% higher core performance or up to 40% lower power over previous generation high-performance FPGAs. These Altera® Agilex 7™ FPGAs and SoCs accelerate system engineers' delivery of todays and tomorrow's most advanced high-bandwidth applications through ground-breaking features.

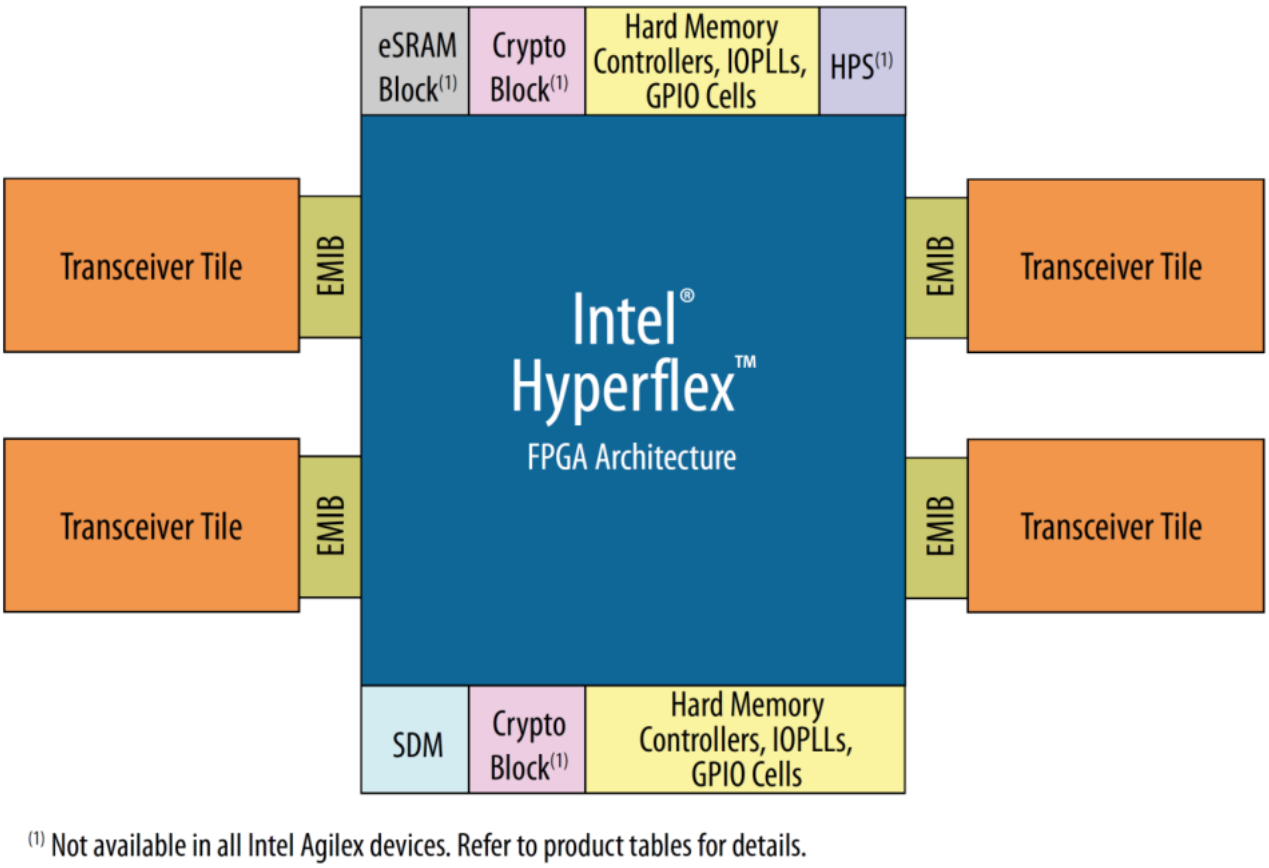

Figure 2: Altera Agilex 7 SoC FPGA CPU Simplified Block Diagram

Note: Please refer the latest Altera Agilex 7 SoC FPGA Datasheet from Altera website for more details which may be revised from time to time.

The Altera Agilex 7 SoC FPGA SOM is compatible to R24C Package AGF 006, AGF 008, AGF 012, AGF 014, AGF 019, AGF 022, AGF 023, AGF 027.

Product Line		AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 023	AGF 022	AGF 027
Resources	Logic elements (LEs)	573,480	764,640	1,178,525	1,437,240	1,918,975	2,308,080	2,208,075	2,692,760
	Adaptive logic modules (ALMs)	194,400	259,200	399,500	487,200	650,500	782,400	748,500	912,800
	ALM registers	777,600	1,036,800	1,598,000	1,948,800	2,602,000	3,129,600	2,994,000	3,651,200
	High-performance crypto blocks	0	0	0	0	2	2	0	0
	eSRAM memory blocks	0	0	2	2	1	1	0	0
	eSRAM memory size (Mb)	0	0	36	36	18	18	0	0
	M20K memory blocks	2,844	3,792	5,900	7,110	8,500	10,464	10,900	13,272
	M20K memory size (Mb)	56	74	115	139	166	204	212	259
	MLAB memory count	9,720	12,960	19,975	24,360	32,525	39,120	37,425	45,640
	MLAB memory size (Mb)	6	8	12	15	20	24	23	28
	Fabric PLL	6	6	8	8	5	5	12	12
	I/O PLL	12	12	16	16	10	10	16	16
	Variable-precision digital signal processing (DSP) blocks	1,640	2,296	3,743	4,510	1,354	1,640	6,250	8,528
	18 x 19 multipliers	3,280	4,592	7,486	9,020	2,708	3,280	12,500	17,056
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.5 / 5.0	3.5 / 6.9	6.0 / 12.0	6.8 / 13.6	2.0 / 4.0	2.5 / 5.0	9.4 / 18.8	12.8 / 25.6
	Maximum EMIF x72[2]	4	4	4	4	3	3	4	4
Maximum Available Device Resources	Maximum differential (RX or TX) pairs	192	288	384	384	240	240	384	384
	Maximum AIB interfaces	2	2	2	2	4	4	4	4
	Memory devices supported	DDR4 and QDR IV							
	Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support							
	Hard processor system	Quad-core 64 bit Arm Cortex*-A53 up to 1.50 GHz with 32 KB I/D cache, Neon* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4							
Tile Resources	F-Tile	PCI Express* (PCIe*) hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) Transceiver channel count : 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 GbE hard IP block (10/25/50/100/200 Gbps FEC/PCS) IEEE 1588 v2 support PMA direct							
	E-Tile	Transceiver channel count : Up to 24 channels at 28.9 Gbps (NRZ) / 12 channels at 57.8 Gbps (PAM4) - RS & KP FEC[1] Networking support : - 400GbE (4 x 100GbE hard IP blocks (10/25 GbE FEC/PCS/MAC)) IEEE 1588 v2 support PMA direct							
	P-Tile	PCIe hard IP block (Gen4 x16) or Bifurcateable 2x PCIe Gen4 x8 (EP) or 4x Gen4 x4 (RP) SR-IOV 8PF / 2kVF VirtIO support Scalable IOV							

Figure 3: Altera Agilex 7 SoC FPGA F-Series Devices Comparison

2.3.1 Altera Agilex 7 Power

The Altera Agilex 7 SoC FPGA SOM uses discrete power regulators Power Management. In Altera Agilex 7 SoC FPGA SOM, Core power, Periphery circuitry power (VCC and VCCP) is connected to a SmartVID regulator, where the voltage can be varied between 0.70V – 0.90V based on Temperature & Performance. The HPS I/O voltage (VCCIO_HPS) is fixed to 1.8V. The I/O voltage details of each FPGA Bank & High-speed transceiver will be mentioned in the corresponding sections.

2.3.2 Altera Agilex 7 Reset

The Altera Agilex 7 SOM POR is taken care internally by SDM Block in device. Also, it supports warm reset input from Board-to-Board Connector2 pin 35 and connected to pin CA43, HPS_COLD_nRESET pin of the SDM Bank of the device.

2.3.3 Altera Agilex 7 Reference Clock

The Altera Agilex 7 SoC FPGA SOM supports on board clock generator for reference clock to different blocks of Altera Agilex 7 SoC and FPGA and to other On SOM peripherals. These reference clock details are mentioned in the below table.

Table 3: Altera Agilex 7 SoC and FPGA SOM Reference Clocks.

Part Number		Clock Type	Frequency		Drive Level		Termination
Source	Destination		Source	Destination	Source	Destination	
Si5341B-D-GM OUT-0	FPGA DDR2 REFCLK	LVDS	100Hz-250MHz	300MHz	-	-	100Ω*
Si5341B-D-GM OUT-1	FPGA REFCLK	LVDS	100Hz-1028MHz	100MHz	-	-	-
Si5341B-D-GM OUT-2	FPGA DDR1 REFCLK	LVDS	100Hz-1028MHz	300MHz	-	-	100Ω*
Si5341B-D-GM OUT-3p	HPS OSC Clock	LVCMOS	100Hz-1028MHz	25MHz	-	-	33Ω
Si5341B-D-GM OUT-3n	Ethernet PHY Clock	LVCMOS	100Hz-1028MHz	25MHz			33Ω
Si5341B-D-GM OUT-4p	SDM OSC Clock	LVCMOS	100Hz-250MHz	125MHz	-	-	33Ω
Si5341B-D-GM OUT-5	FGT_13A_Q2 REFCLK	LVDS	100Hz-250MHz	156.25MHz	-	-	-
Si5341B-D-GM OUT-6p	USB TR REFCLK	LVCMOS	100Hz-250MHz	24MHz	-	-	33Ω

Part Number		Clock Type	Frequency		Drive Level		Termination
Source	Destination		Source	Destination	Source	Destination	
Si5341B-D-GM OUT-7	FGT_12A_Q2 REFCLK	LVDS	100Hz-250MHz	156.25MHz	-	-	-
Si5341B-D-GM OUT-8	FPGA QDR1 REFCLK	LVDS	100Hz-1028MHz	233.25MHz	-	-	100Ω*
Si5341B-D-GM OUT-9	FPGA QDR2 REFCLK	LVDS	100Hz-1028MHz	233.25MHz	-	-	100Ω*
B2B1-Pin 171	Si_CLKGEN_REFIN_N*	LVDS	NA	100Hz-750MHz	-	-	-
B2B1-Pin 169	Si_CLKGEN_REFIN_P*	LVDS	NA	100Hz-750MHz	-	-	-

Note:
[1] Si5341B-GM: Drive strength is register programmable setting and stored in NVM.
** Optional*

2.3.4 Altera Agilex 7 SoC and FPGA Configuration & Status

The Altera Agilex 7 SoC and FPGA uses multi-stage boot process that supports both a non-secure and a secure boot. It supports different configuration schemes -JTAG-based configuration, AS Fast or Standard POR configuration. These configuration schemes are selected using the MSEL pin setting.

The SDM is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the First stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the HPS first and then configure the FPGA or it can be set to configure the FPGA first, then boot the HPS.

The Altera Agilex 7 SoC and FPGA SOM supports LED for the FPGA Configuration status indication namely CONFIG_DONE. LED interfaced to CONFIG_DONE and it is asserted when the FPGA configuration is complete. It is used to indicate if the FPGA is configured or not.

2.3.5 Altera Agilex 7 Boot Mode Switch

The Altera Agilex 7 SoC and FPGA always boots from SDM first and then boots the HPS or FPGA. Altera Agilex 7 SoC and FPGA supports the SDM QSPI or JTAG as the First Stage Bootloader in Standard or Fast Mode. Upon device reset, Altera Agilex 7 SoC and FPGA MSEL pins are read to determine the primary boot device. The ON SOM Switch also supports to switch between Active serial or JTAG connectivity on the On SOM Header. Also Direct to Factory Image option is made available on the switch.

The Altera Agilex 7 SoC and FPGA SOM supports Switching between Active Serial & JTAG Connectivity on the On SOM Header using the POS3 of the switch. Refer the below table to select between JTAG & Active Serial.

Table 4: JTAG & Active Serial Switch Truth Table

Altera Agilex 7 -AS/JTAG Header selection	SW 1 (4 Position Switch-POS3)	
	POS 3	Switch Position Image
SDM JTAG on AS/JTAG Header	OFF	
SDM Active Serial on AS/JTAG Header	ON	

The Altera Agilex 7 SoC and FPGA SOM supports selection between the different configuration schemes making use of POS1 and POS2 the switch. Refer the below table to select between the different configuration schemes.

Table 5: Configuration Selection Truth Table

Altera Agilex 7 Configuration Scheme Selection	SW (4 Position Switch-POS1 &POS2)		
	POS 1	POS 2	Switch Position Image
	MSEL2	MSEL1	
Active Serial - Fast Mode	OFF	OFF	
Active Serial - Standard Mode	OFF	ON	
JTAG Only Mode	ON	ON	

2.3.6 Agilex 7 SoC/FPGA High Speed Transceivers

The Agilex 7 SoC/FPGA SOM supports 24 high speed transceivers on Board-to-Board connectors from Agilex 7 FPGA fabric. The Agilex 7 SoC/FPGA has two high speed transceiver banks (12A & 13A) and each transceiver bank has four quad and each quad supports four high speed transmit and receive channels. So, total 16 high speed transmit and receive channels for each bank. Also, each high-speed transceiver quad supports two reference clock input pairs and last two quad supports each one reference clock output pairs. Transceiver data rate performance is based on the transceiver speed grade of the Agilex 7 SoC/FPGA as mentioned in the below table.

Table 6: Agilex 7 R24C SoC/FPGA Transceiver data rate performance

Description	Condition	Transceiver Speed Grade			Unit
		-1	-2	-3	
Supported data rate	NRZ	1–32.45	1–32	1–17.4	Gbps
	PAM4	20–58.125	20–58.125	20–32	Gbps

Note: FGT Quad0 can only support 20-32 Gbps PAM4. FGT Quad1, Quad2, and Quad3 can ***support 20-58 Gbps PAM4.***

The Agilex 7 SoC/FPGA SOM supports 12 high speed transceiver channels from Bank 13A Quad0, Quad1 & Quad2 along with two reference clock input pairs of each quad on Board to Board connector1 and 16 high speed transceiver channels from Bank 12A Quad0, Quad1, Quad2, Quad3 along with two reference clock input pairs of each quad on Board-to-Board conenctor3 and 4 high speed transceiver channels from Bank 13A Quad3 along with two reference clock input pairs of quad on Board-to-Board conenctor1. In Agilex 7 SoC/FPGA SOM, on board termination and AC coupling capacitors are not supported on transceiver lines. So it has to be taken care in the carrier board if required.

2.4 Memory

2.4.1 DDR4 SDRAM with ECC for HPS

The Altera Agilex 7 SoC and FPGA SOM supports 64bit, 8GB DDR4 RAM memory for Altera Agilex 7 HPS. Four 16 bit, 2GB DDR4 SDRAM ICs are used to support total on board HPS RAM memory of 8GB. Also, Altera Agilex 7 SoC and FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1600MHz in -1 Speed Grade devices and 1334Mhz and 1200MHz speed respectively in -2 and -3 Speed Grade Devices. DDR4 memory is connected to the hard memory controller supported Banks- 3C and 3D. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The HPS DDR4 reference clock is connected to Bank 3D -G5 & F6 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.2 DDR4 SDRAM1 for FPGA

The Altera Agilex 7 SoC and FPGA SOM supports 2 x 64bit, 8GB DDR4 RAM memory for Altera Agilex 7 FPGA. For the first FPGA DDR4 SDRAM, four 16 bit, 2GB DDR4 SDRAM ICs are used to support a total on board FPGA RAM memory of 8GB. Also, Altera Agilex 7 SoC and FPGA SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1600MHz in -1 Speed Grade devices and 1334Mhz and 1200MHz speed respectively in -2 and -3 Speed Grade Devices. DDR4 memory is connected to the FPGA Banks- 2C and 2D. The RAM size can be expandable based on the availability of higher density 16bit DDR4 device.

The FPGA1 DDR4 reference clock is connected to Bank 2C -DE36 & DD35 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.3 Dual QDR-IV for FPGA

The Altera Agilex 7 SoC and FPGA SOM supports dual 18bit, 144Mb QDR-IV RAM memory for Altera Agilex 7 FPGA. These QDR-IV devices operate at 933MHz Speed. 1st QDR-IV memory is connected to the FPGA Banks- 2C and 2D and 2nd QDR-IV connected to the FPGA Banks- 2B and 2C Bank.

The 1st QDR-IV reference clock is connected to Bank 2D -DD12 & DC13 pins through on SOM clock synthesizer.

The 2nd QDR-IV reference clock is connected to Bank 2B -DD36 & DC37 pins through on SOM clock synthesizer.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.4.4 eMMC Flash

The Altera Agilex 7 SoC and FPGA SOM supports 32GB eMMC Flash memory for Second Stage Boot & Storage of Altera Agilex 7 SoC and FPGA. This eMMC Flash memory is directly connected to the SDMMC controller in HPS Block of the Altera Agilex 7 SoC and FPGA and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC5.0 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SOM based on the Product Part Number.*

2.4.5 QSPI Flash

The Altera Agilex 7 SoC and FPGA SOM supports 1Gb QSPI Flash memory for First Stage Boot & Storage of Altera Agilex 7 SoC and FPGA. This QSPI Flash memory is directly connected to the SDM controller of the Altera Agilex 7 SoC and FPGA SDM and operates at 1.8V Voltage level. The QSPI Flash size can be expandable based on the availability of higher density chips.

2.5 On SOM Features

2.5.1 JTAG/ Active Serial Header (Optional)

The Altera Agilex 7 SoC and FPGA SOM supports 10Pin JTAG/Active Serial Header for JTAG or Active Serial interface. JTAG Interface Signals and Active Serial Signals from the SDM of Altera Agilex 7 SoC and FPGA is connected to the 10pin Header through a MUX switch. JTAG and Active Serial can be selected by toggling the POS 3 of the DIP Switch. The Altera Agilex 7 SoC and FPGA 's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Altera Agilex 7 SoC and FPGA. These JTAG interface signals are at 1.8V Voltage level.

The JTAG/Active Serial Header is physically located on topside of the SOM as shown below. JTAG interface signals are also connected to Board-to-Board Connector2 for access from Carrier board. The JTAG/AS Header (J4) is physically located on topside of the SOM as shown below. By default, not supported.

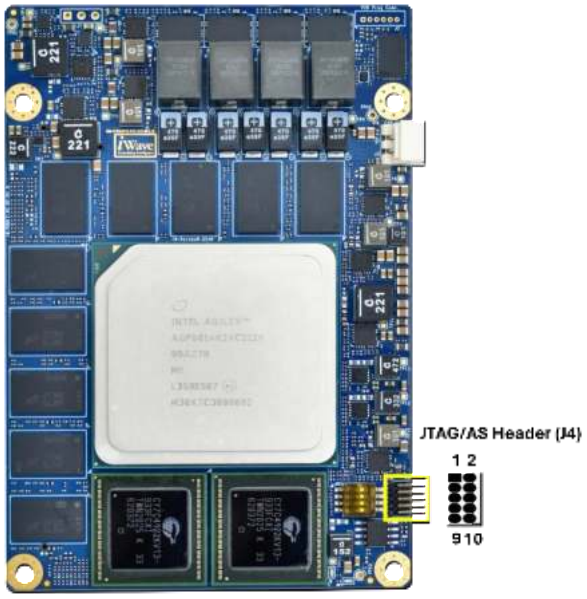

Figure 4: JTAG/AS Header

Number of Pins - 10

Connector Part - GRPB052MWCN-RC from Sullins

Mating Connector - LPPB052NFSS-RC from Sullins

Table 7: JTAG/Active Serial Header Pinout- JTAG is selected.

Pin No	Signal Name	Signal Type/ Termination	Description
1	JTAG_TCK	I, 1.8V CMOS/ 1K PD	JTAG test Clock.
2	GND	Power	Ground.
3	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
4	VCC(TRGT)	Power	Target Power Supply

Pin No	Signal Name	Signal Type/ Termination	Description
5	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
6	JTAG_RESET	I, 1.8V CMOS / 10K PU	JTAG RESET. Not connected to SoC or FPGA
7	NC	-	NC.
8	NC	-	NC.
9	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
10	GND	Power	Ground.

Table 8: JTAG/Active Serial Header Pinout- Active Serial is selected.

Pin No	Signal Name	Signal Type/ Termination	Description
1	AS_CLK	I, 1.8V CMOS/ 100K PD	Dedicated Serial clock to configure flash.
2	GND	Power	Ground.
3	AS_CONF_DONE	IO, 1.8V OD	Configuration status IO to Altera Agilex 7 SoC and FPGA.
4	VCC(TRGT)	Power	Target Power Supply
5	AS_nCONFIG	I, 1.8V CMOS/ 10K PU	Configuration input to Altera Agilex 7 SoC and FPGA
6	nCE	I, 1.8V CMOS/ 10K PU	Chip Enable input to Altera Agilex 7 SoC and FPGA
7	AS_DO	I, 1.8V CMOS	Serial Data input to Configuration flash
8	AS_CS0	I, 1.8V CMOS/ 10K PU	Chip select input to configuration flash.
9	AS_DI	O, 1.8V CMOS	Serial Data output from configuration flash.
10	GND	Power	Ground.

2.5.2 Fan Header

The Altera Agilex 7 SoC and FPGA SOM supports a Fan Header (J3) to connect cooling Fan if required. The Fan Header (J3) is physically located on topside of the SOM as shown below.

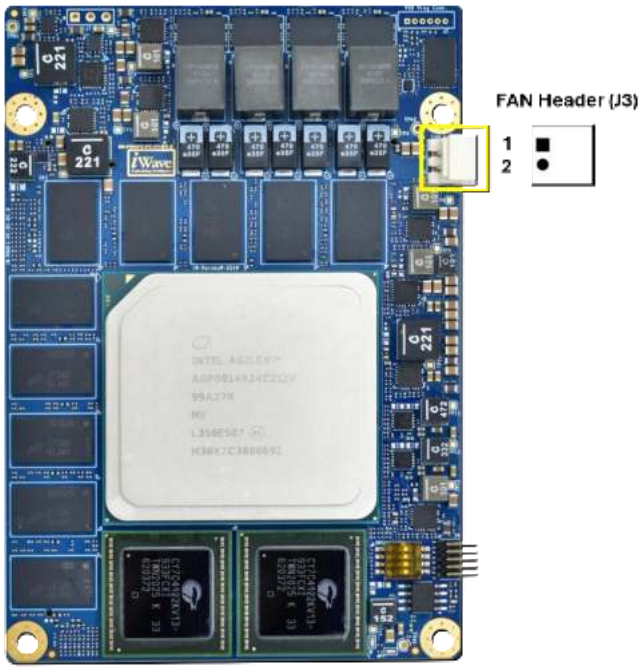

Figure 5: Fan Header

Number of Pins - 2

Connector Part - 52125-02-0200-01 from CNC

Mating Connector - 52225-02 from CNC

Table 9: Fan Header Pinout

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, 5V Power	Supply Voltage.
2	GND	Power	Ground.

The Altera Agilex 7 SoC and FPGA SOM supports three 240 pin high speed ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Altera Agilex 7 SoC FPGA SOM design to provide the maximum interfaces of Altera Agilex 7 SoC and FPGA to the carrier board through these three Board to Board Connectors.

2.6 Board to Board Connector1

The Altera Agilex 7 SoC and FPGA SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector1 are explained in the following sections. The Board-to-Board Connector1 (J7) is physically located on bottom side of the SOM as shown below.

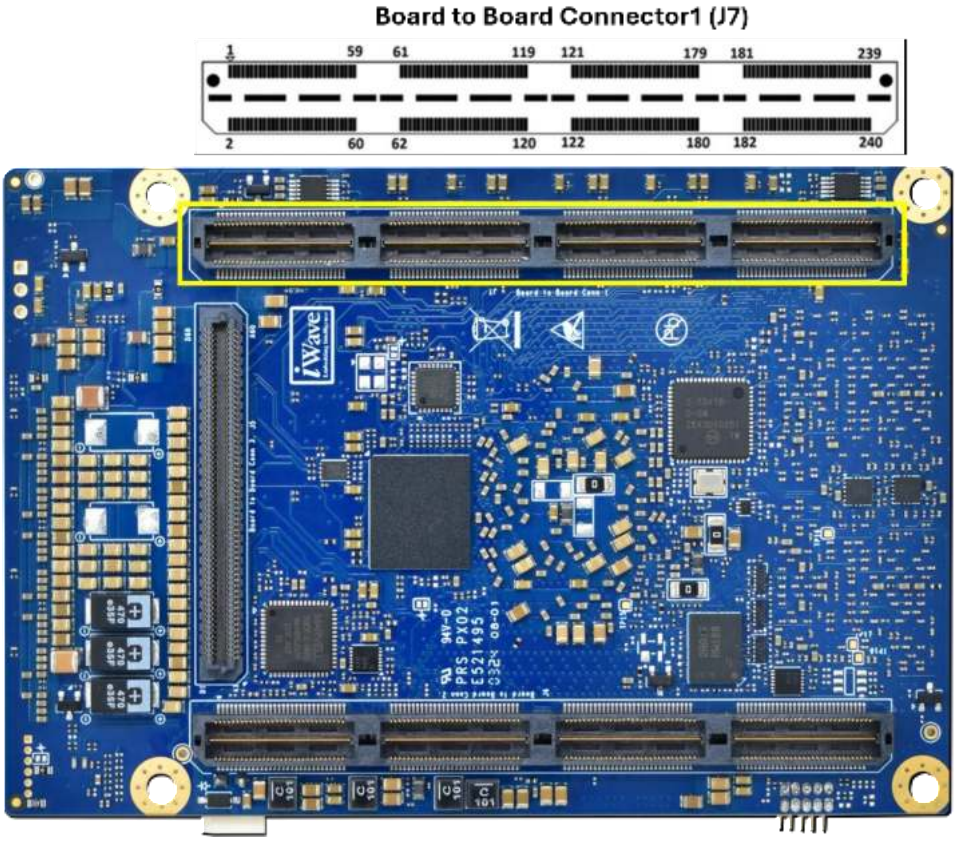

Figure 6: Board-to-Board Connector1

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtech

Mating Connector - QSH-120-01-L-D-Afrom Samtech

Staking Height - 5mm

Table 10: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
FGTR13A_TX_Q0_CH0P	3	4	REFCLK_FGTR13A_Q0_RX_CH0P
FGTR13A_TX_Q0_CH0N	5	6	REFCLK_FGTR13A_Q0_RX_CH0N
GND	7	8	GND
FGTR13A_TX_Q0_CH1P	9	10	FPGA_B36_LVDS3A_12N_TX_IO49
FGTR13A_TX_Q0_CH1N	11	12	FPGA_E47_LVDS3A_3P_RX_IO86
GND	13	14	FPGA_D48_LVDS3A_3N_RX_IO87
FGTR13A_RX_Q0_CH1N	15	16	FPGA_A47_LVDS3A_3P_TX_IO84
FGTR13A_RX_Q0_CH1P	17	18	FPGA_B48_LVDS3A_3N_TX_IO85
GND	19	20	GND
FGTR13A_RX_Q0_CH0N	21	22	FPGA_F46_LVDS3A_5N_TX_IO77/CLKOUT_1N
FGTR13A_RX_Q0_CH0P	23	24	FPGA_G45_LVDS3A_5P_TX_IO76/CLKOUT_1P
GND	25	26	GND
FPGA_E53_LVDS3A_1P_RX_IO94	27	28	FPGA_F50_LVDS3A_4N_RX_IO83
FPGA_D54_LVDS3A_1N_RX_IO95	29	30	FPGA_G49_LVDS3A_4P_RX_IO82
FPGA_E51_LVDS3A_1P_TX_IO92	31	32	FPGA_G47_LVDS3A_4P_TX_IO80
FPGA_D52_LVDS3A_1N_TX_IO93	33	34	FPGA_F48_LVDS3A_4N_TX_IO81
GND	35	36	GND
FGTR13A_TX_Q0_CH2P	37	38	FPGA_J45_LVDS3A_5P_RX_IO78
FGTR13A_TX_Q0_CH2N	39	40	FPGA_K46_LVDS3A_5N_RX_IO79
GND	41	42	FPGA_K44_LVDS3A_6N_RX_IO75
FGTR13A_TX_Q0_CH3P	43	44	FPGA_J43_LVDS3A_6P_RX_IO74
FGTR13A_TX_Q0_CH3N	45	46	FPGA_A45_LVDS3A_7P_TX_IO68
GND	47	48	FPGA_B46_LVDS3A_7N_TX_IO69
FGTR13A_RX_Q0_CH3N	49	50	FPGA_A43_LVDS3A_8P_TX_IO64
FGTR13A_RX_Q0_CH3P	51	52	FPGA_B44_LVDS3A_8N_TX_IO65
GND	53	54	GND
FGTR13A_RX_Q0_CH2N	55	56	FPGA_D46_LVDS3A_7N_RX_IO71/CLKIN_0N
FGTR13A_RX_Q0_CH2P	57	58	FPGA_E45_LVDS3A_7P_RX_IO70/CLKIN_0P
GND	59	60	GND
GND	61	62	GND
NC	63	64	REFCLK_FGTR13A_Q0_RX_CH1P
NC	65	66	REFCLK_FGTR13A_Q0_RX_CH1N
GND	67	68	GND
SDM_ADC_VSIGN_0	69	70	FPGA_E41_LVDS3A_9P_RX_IO62
SDM_ADC_VSIGP_0	71	72	FPGA_D42_LVDS3A_9N_RX_IO63
GND	73	74	FPGA_A41_LVDS3A_9P_TX_IO60
NC	75	76	FPGA_B42_LVDS3A_9N_TX_IO61
NC	77	78	NC
GND	79	80	GND
NC	81	82	FPGA_F44_LVDS3A_6N_TX_IO73/CLKIN_1N
NC	83	84	FPGA_G43_LVDS3A_6P_TX_IO72/CLKIN_1P
GND	85	86	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
FPGA_E49_LVDS3A_2P_RX_IO90	87	88	FPGA_D40_LVDS3A_10N_RX_IO59
FPGA_D50_LVDS3A_2N_RX_IO91	89	90	PCIE_PERST_N_13A
FPGA_A49_LVDS3A_2P_TX_IO88	91	92	HPS_GPIO0_10_ETH_RST_N
FPGA_B50_LVDS3A_2N_TX_IO89	93	94	HPS_GPIO0_11_ETH_INT
GND	95	96	GND
FGTR13A_TX_Q1_CH0P	97	98	REFCLK_FGTR13A_Q1_RX_CH2P
FGTR13A_TX_Q1_CH0N	99	100	REFCLK_FGTR13A_Q1_RX_CH2N
GND	101	102	GND
FGTR13A_TX_Q1_CH1P	103	104	NC
FGTR13A_TX_Q1_CH1N	105	106	NC
GND	107	108	NC
FGTR13A_RX_Q1_CH1N	109	110	NC
FGTR13A_RX_Q1_CH1P	111	112	NC
GND	113	114	GND
FGTR13A_RX_Q1_CH0N	115	116	FPGA_D44_LVDS3A_8N_RX_IO67/CLKOUT_0N
FGTR13A_RX_Q1_CH0P	117	118	FPGA_E43_LVDS3A_8P_RX_IO66/CLKOUT_0P
GND	119	120	GND
GND	121	122	GND
FGTR13A_TX_Q1_CH2P	123	124	HPS_MDIO1_MDC
FGTR13A_TX_Q1_CH2N	125	126	HPS_MDIO1_MDIO
GND	127	128	NC
FGTR13A_TX_Q1_CH3P	129	130	FPGA_R41_LVDS3A_19P_RX_IO22/CLKIN_0P
FGTR13A_TX_Q1_CH3N	131	132	FPGA_P42_LVDS3A_19N_RX_IO23/CLKIN_0N
GND	133	134	NC
FGTR13A_RX_Q1_CH3N	135	136	NC
FGTR13A_RX_Q1_CH3P	137	138	NC
GND	139	140	GND
FGTR13A_RX_Q1_CH2N	141	142	FPGA_M46_LVDS3A_17N_TX_IO29/CLKOUT_1N
FGTR13A_RX_Q1_CH2P	143	144	FPGA_L45_LVDS3A_17P_TX_IO28/CLKOUT_1P
GND	145	146	GND
FPGA_W41_LVDS3A_13P_RX_IO46	147	148	NC
FPGA_Y42_LVDS3A_13N_RX_IO47	149	150	NC
FPGA_T42_LVDS3A_13N_TX_IO45	151	152	NC
FPGA_U41_LVDS3A_13P_TX_IO44	153	154	NC
GND	155	156	GND
NC	157	158	REFCLK_FGTR13A_Q1_RX_CH3P
NC	159	160	REFCLK_FGTR13A_Q1_RX_CH3N
GND	161	162	GND
SDM_ADC_VSIGN_1	163	164	TEMPDIODE_12A_GXF_DP*
SDM_ADC_VSIGP_1	165	166	TEMPDIODE_12A_GXF_DN*
GND	167	168	TEMPDIODE_13A_GXF_DN*
Si_CLKGEN_REFIN_N*	169	170	PCIE_PERST_N_12A/TEMPDIODE_13A_GXF_DP*
Si_CLKGEN_REFIN_P*	171	172	FPGA_L41_LVDS3A_19P_TX_IO20
GND	173	174	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
NC	175	176	FPGA_M40_LVDS3A_20N_TX_IO17
NC	177	178	FPGA_L39_LVDS3A_20P_TX_IO16
GND	179	180	GND
GND	181	182	GND
FGTR13A_TX_Q2_CH0P	183	184	REFCLK_FGTR13A_Q2_RX_CH4P
FGTR13A_TX_Q2_CH0N	185	186	REFCLK_FGTR13A_Q2_RX_CH4N
GND	187	188	GND
FGTR13A_TX_Q2_CH1P	189	190	HPS_EMAC1_TX_CLK
FGTR13A_TX_Q2_CH1N	191	192	HPS_EMAC1_TXD0
GND	193	194	HPS_EMAC1_TXD1
FGTR13A_RX_Q2_CH1N	195	196	HPS_EMAC1_TXD2
FGTR13A_RX_Q2_CH1P	197	198	HPS_EMAC1_TXD3
GND	199	200	GND
FGTR13A_RX_Q2_CH0N	201	202	NC
FGTR13A_RX_Q2_CH0P	203	204	NC
GND	205	206	GND
FPGA_Y40_LVDS3A_14N_RX_IO43	207	208	SOM_PWR_OK
FPGA_W39_LVDS3A_14P_RX_IO42	209	210	HPS_EMAC1_TX_CTL
FPGA_U39_LVDS3A_14P_TX_IO40	211	212	HPS_EMAC1_RX_CLK
FPGA_T40_LVDS3A_14N_TX_IO41	213	214	HPS_EMAC1_RX_CTL
GND	215	216	GND
FGTR13A_TX_Q2_CH2P	217	218	REFCLK_FGTR13A_Q2_CH8P
FGTR13A_TX_Q2_CH2N	219	220	REFCLK_FGTR13A_Q2_CH8N
GND	221	222	GND
FGTR13A_TX_Q2_CH3P	223	224	HPS_EMAC1_RXD0
FGTR13A_TX_Q2_CH3N	225	226	HPS_EMAC1_RXD1
GND	227	228	HPS_EMAC1_RXD2
FGTR13A_RX_Q2_CH3N	229	230	HPS_EMAC1_RXD3
FGTR13A_RX_Q2_CH3P	231	232	SOMPWR_EN
GND	233	234	GND
FGTR13A_RX_Q2_CH2N	235	236	NC
FGTR13A_RX_Q2_CH2P	237	238	NC
GND	239	240	GND

**Optional*

2.6.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector1 from Altera Agilex 7 SoC and FPGA is explained in the following section.

2.6.2 FPGA High Speed Transceivers

The Altera Agilex 7 SoC and FPGA SOM supports 12 high speed transceiver channels (12 Channels from FGT 13A Bank Quad [2:0] and Each quad supports 4 Transceiver channels) on Board-to-Board connector1. In Altera Agilex 7 SoC and FPGA SOM, the Transceivers connected to Board-to-Board Connector1 is capable of running up to a maximum speed of 17.4Gbps in NRZ Format or 32Gbps in PAM4 Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two reference clock input pairs.

Note2: Based on Device bank names will change. In this datasheet AGF 014 Device considered.

For more details on FGTL 13A transceiver pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_13A Quad0 Channels				
3	FGTR13A_TX_Q0_CH0P	FGTR13A_TX_Q0_CH0P/ AK4	O, DIFF	Bank FGT13A-Q0 channel0 High speed differential transmitter positive.
5	FGTR13A_TX_Q0_CH0N	FGTR13A_TX_Q0_CH0N / AL5	O, DIFF	Bank FGT13A-Q0 channel0 High speed differential transmitter negative.
9	FGTR13A_TX_Q0_CH1P	FGTR13A_TX_Q0_CH1P/ AN7	O, DIFF	Bank FGT13A-Q0 channel1 High speed differential transmitter positive.
11	FGTR13A_TX_Q0_CH1N	FGTR13A_TX_Q0_CH1N / AM8	O, DIFF	Bank FGT13A-Q0 channel1 High speed differential transmitter negative.
37	FGTR13A_TX_Q0_CH2P	FGTR13A_TX_Q0_CH2P/ AP4	O, DIFF	Bank FGT13A-Q0 channel2 High speed differential transmitter positive.
39	FGTR13A_TX_Q0_CH2N	FGTR13A_TX_Q0_CH2N / AR5	O, DIFF	Bank FGT13A-Q0 channel2 High speed differential transmitter negative.
43	FGTR13A_TX_Q0_CH3P	FGTR13A_TX_Q0_CH3P/ AU7	O, DIFF	Bank FGT13A-Q0 channel3 High speed differential transmitter positive.
45	FGTR13A_TX_Q0_CH3N	FGTR13A_TX_Q0_CH3N / AT8	O, DIFF	Bank FGT13A-Q0 channel3 High speed differential transmitter negative.
21	FGTR13A_RX_Q0_CH0N	FGTR13A_RX_Q0_CH0N / AG5	I, DIFF	Bank FGT12A-Q0 channel0 High speed differential receiver negative.
23	FGTR13A_RX_Q0_CH0P	FGTR13A_RX_Q0_CH0P / AF4	I, DIFF	Bank FGT12A-Q0 channel0 High speed differential receiver positive.
15	FGTR13A_RX_Q0_CH1N	FGTR13A_RX_Q0_CH1N / AH2	I, DIFF	Bank FGT13A-Q0 channel1 High speed receiver negative.
17	FGTR13A_RX_Q0_CH1P	FGTR13A_RX_Q0_CH1P / AJ1	I, DIFF	Bank FGT13A-Q0 channel1 High speed differential receiver positive.
55	FGTR13A_RX_Q0_CH2N	FGTR13A_RX_Q0_CH2N / AM2	I, DIFF	Bank FGT13A-Q0 channel2 High speed differential receiver negative.

B2B-1 Pin No	B2B Connector1 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
57	FGTR13A_RX_Q0_CH2P	FGTR13A_RX_Q0_CH2P / AN1	I, DIFF	Bank FGT13A-Q0 channel2 High speed differential receiver positive.
49	FGTR13A_RX_Q0_CH3N	FGTR13A_RX_Q0_CH3N / AT2	I, DIFF	Bank FGT13A-Q0 channel3 High speed differential receiver negative.
51	FGTR13A_RX_Q0_CH3P	FGTR13A_RX_Q0_CH3P / AU1	I, DIFF	Bank FGT13A-Q0 channel3 High speed differential receiver positive.
4	REFCLK_FGTR13A_Q0_RX_CH0P	REFCLK_FGTR13A_Q0_RX_CH0P/ BH8	I, DIFF	Bank FGT13A-Q0 High speed differential Clock0 positive. Regional reference clock, this clock can be used for 13A Bank Q0 and Q1 Transceivers.
6	REFCLK_FGTR13A_Q0_RX_CH0N	REFCLK_FGTR13A_Q0_RX_CH0N/ BJ7	I, DIFF	Bank FGT13A-Q0 High speed differential Clock0 negative. Regional reference clock, this clock can be used for 13A Bank Q0 and Q1 Transceivers.
64	REFCLK_FGTR13A_Q0_RX_CH1P	REFCLK_FGTR13A_Q0_RX_CH1P/ BG7	I, DIFF	Bank FGT13A-Q0 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 13A Bank Q0 and Q1 Transceivers.
66	REFCLK_FGTR13A_Q0_RX_CH1N	REFCLK_FGTR13A_Q0_RX_CH1N/ BE7	I, DIFF	Bank FGT13A-Q0 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 13A Bank Q0 and Q1 Transceivers.
BANK-FGT_13A Quad1 Channels				
97	FGTR13A_TX_Q1_CH0P	FGTR13A_TX_Q1_CH0p/ AV4	O, DIFF	Bank FGT13A-Q1 channel0 High speed differential transmitter positive.
99	FGTR13A_TX_Q1_CH0N	FGTR13A_TX_Q1_CH0n/ AW5	O, DIFF	Bank FGT13A-Q1 channel0 High speed differential transmitter negative.
103	FGTR13A_TX_Q1_CH1P	FGTR13A_TX_Q1_CH1p/ BA7	O, DIFF	Bank FGT13A-Q1 channel1 High speed differential transmitter positive.
105	FGTR13A_TX_Q1_CH1N	FGTR13A_TX_Q1_CH1n/ AY8	O, DIFF	Bank FGT13A-Q1 channel1 High speed differential transmitter negative.
123	FGTR13A_TX_Q1_CH2P	FGTR13A_TX_Q1_CH2p/ BB4	O, DIFF	Bank FGT13A-Q1 channel2 High speed differential transmitter positive.
125	FGTR13A_TX_Q1_CH2N	FGTR13A_TX_Q1_CH2n/ BC5	O, DIFF	Bank FGT13A-Q1 channel2 High speed differential transmitter negative.
129	FGTR13A_TX_Q1_CH3P	FGTR13A_TX_Q1_CH3p/ BF4	O, DIFF	Bank FGT13A-Q1 channel3 High speed differential transmitter positive.
131	FGTR13A_TX_Q1_CH3N	FGTR13A_TX_Q1_CH3n/ BG5	O, DIFF	Bank FGT13A-Q1 channel3 High speed differential transmitter negative.

B2B-1 Pin No	B2B Connector1 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
115	FGTR13A_RX_Q1_CH0N	FGTR13A_RX_Q1_CH0n /AY2	I, DIFF	Bank FGT12A-Q1 channel0 High speed differential receiver negative.
117	FGTR13A_RX_Q1_CH0P	FGTR13A_RX_Q1_CH0p /BA1	I, DIFF	Bank FGT12A-Q1 channel0 High speed differential receiver positive.
109	FGTR13A_RX_Q1_CH1N	FGTR13A_RX_Q1_CH1n /BD2	I, DIFF	Bank FGT13A-Q1 channel1 High speed receiver negative.
111	FGTR13A_RX_Q1_CH1P	FGTR13A_RX_Q1_CH1p /BE1	I, DIFF	Bank FGT13A-Q1 channel1 High speed differential receiver positive.
141	FGTR13A_RX_Q1_CH2N	FGTR13A_RX_Q1_CH2n /BH2	I, DIFF	Bank FGT13A-Q1 channel2 High speed differential receiver negative.
143	FGTR13A_RX_Q1_CH2P	FGTR13A_RX_Q1_CH2p /BJ1	I, DIFF	Bank FGT13A-Q1 channel2 High speed differential receiver positive.
135	FGTR13A_RX_Q1_CH3N	FGTR13A_RX_Q1_CH3n /BM2	I, DIFF	Bank FGT13A-Q1 channel3 High speed differential receiver negative.
137	FGTR13A_RX_Q1_CH3P	FGTR13A_RX_Q1_CH3p /BN1	I, DIFF	Bank FGT13A-Q1 channel3 High speed differential receiver positive.
98	REFCLK_FGTR13A_Q1_RX_CH2P	REFCLK_FGTR13A_Q1_RX_CH2p/BR7	I, DIFF	Bank FGT13A-Q1 High speed differential Clock2 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
100	REFCLK_FGTR13A_Q1_RX_CH2N	REFCLK_FGTR13A_Q1_RX_CH2n/BU7	I, DIFF	Bank FGT13A-Q1 High speed differential Clock2 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
158	REFCLK_FGTR13A_Q1_RX_CH3P	REFCLK_FGTR13A_Q1_RX_CH3p/BP8	I, DIFF	Bank FGT13A-Q1 High speed differential Clock3 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
160	REFCLK_FGTR13A_Q1_RX_CH3N	REFCLK_FGTR13A_Q1_RX_CH2n/BU7	I, DIFF	Bank FGT13A-Q1 High speed differential Clock3 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
BANK-FGT_13A Quad2 Channels				
183	FGTR13A_TX_Q2_CH0P	FGTR13A_TX_Q2_CH0p/ BK4	O, DIFF	Bank FGT13A-Q2 channel0 High speed differential transmitter positive.
185	FGTR13A_TX_Q2_CH0N	FGTR13A_TX_Q2_CH0n/ BL5	O, DIFF	Bank FGT13A-Q2 channel0 High speed differential transmitter negative.
189	FGTR13A_TX_Q2_CH1P	FGTR13A_TX_Q2_CH1p/ BP4	O, DIFF	Bank FGT13A-Q2 channel1 High speed differential transmitter positive.

B2B-1 Pin No	B2B Connector1 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
191	FGTR13A_TX_Q2_CH1N	FGTR13A_TX_Q2_CH1n/ BR5	O, DIFF	Bank FGT13A-Q2 channel1 High speed differential transmitter negative.
217	FGTR13A_TX_Q2_CH2P	FGTR13A_TX_Q2_CH2p/ BV4	O, DIFF	Bank FGT13A-Q2 channel2 High speed differential transmitter positive.
219	FGTR13A_TX_Q2_CH2N	FGTR13A_TX_Q2_CH2n/ BW5	O, DIFF	Bank FGT13A-Q2 channel2 High speed differential transmitter negative.
223	FGTR13A_TX_Q2_CH3P	FGTR13A_TX_Q2_CH3p/ CB4	O, DIFF	Bank FGT13A-Q2 channel3 High speed differential transmitter positive.
225	FGTR13A_TX_Q2_CH3N	FGTR13A_TX_Q2_CH3n/ CC5	O, DIFF	Bank FGT13A-Q2 channel3 High speed differential transmitter negative.
201	FGTR13A_RX_Q2_CH0N	FGTR13A_RX_Q2_CH0n /BT2	I, DIFF	Bank FGT12A-Q2 channel0 High speed differential receiver negative.
203	FGTR13A_RX_Q2_CH0P	FGTR13A_RX_Q2_CH0p /BU1	I, DIFF	Bank FGT12A-Q2 channel0 High speed differential receiver positive.
195	FGTR13A_RX_Q2_CH1N	FGTR13A_RX_Q2_CH1n /BY2	I, DIFF	Bank FGT13A-Q2 channel1 High speed receiver negative.
197	FGTR13A_RX_Q2_CH1P	FGTR13A_RX_Q2_CH1p /CA1	I, DIFF	Bank FGT13A-Q2 channel1 High speed differential receiver positive.
235	FGTR13A_RX_Q2_CH2N	FGTR13A_RX_Q2_CH2n /CD2	I, DIFF	Bank FGT13A-Q2 channel2 High speed differential receiver negative.
237	FGTR13A_RX_Q2_CH2P	FGTR13A_RX_Q2_CH2p /CE1	I, DIFF	Bank FGT13A-Q2 channel2 High speed differential receiver positive.
229	FGTR13A_RX_Q2_CH3N	FGTR13A_RX_Q2_CH3n /CH2	I, DIFF	Bank FGT13A-Q2 channel3 High speed differential receiver negative.
231	FGTR13A_RX_Q2_CH3P	FGTR13A_RX_Q2_CH3p /CJ1	I, DIFF	Bank FGT13A-Q2 channel3 High speed differential receiver positive.
184	REFCLK_FGTR13A_Q2_RX_CH4P	REFCLK_FGTR13A_Q2_RX_CH4p/BW7	I, DIFF	Bank FGT13A-Q2 High speed differential Clock2 positive. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
186	REFCLK_FGTR13A_Q2_RX_CH4N	REFCLK_FGTR13A_Q2_RX_CH4n/BV8	I, DIFF	Bank FGT13A-Q2 High speed differential Clock4 negative. Global reference clock, this clock can be used for 13A Bank Q0, Q1, Q2 and Q3 Transceivers.
218	REFCLK_FGTR13A_Q2_CH8P	REFCLK_FGTR13A_Q2_CH8p/CE7	IO, DIFF	Bank FGT13A-Q2 High speed differential Clock4 positive. Local In/out reference clock, this clock can be used for 13A Bank Q2 Transceivers.

B2B-1 Pin No	B2B Connector1 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
220	REFCLK_FGTR13A_Q2_CH8N	REFCLK_FGTR13A_Q2_CH8n/CG7	IO, DIFF	Bank FGT13A-Q8 High speed differential Clock3 negative. Local In/out reference clock, this clock can be used for 13A Bank Q2 Transceivers.

2.6.3 FPGA IOs & General-Purpose Clocks – Bank3A

The Altera Agilex 7 SoC and FPGA SOM supports up to 27 LVDS or 54 Single Ended IOs and from Altera Agilex 7 FPGA Bank3A on Board-to-Board connector1. In Altera Agilex 7 SoC and FPGA SOM, Bank3A signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3A signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Altera Agilex 7 SoC and FPGA SOM, upon these 27 LVDS or 54 Single Ended IOs from Altera Agilex 7 FPGA Bank3A, Three General Purpose Clock input LVDS pair and Three General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Altera Agilex 7 SoC and FPGA SOM, Bank3A I/O voltage is set to **1.2V.** Contact iWave if **1.5V** voltage support is required. For Bank3A IO Voltage refer B2B-2 Pin 226.

For more details on Altera Agilex 7 SoC and FPGA Bank3A pinouts on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
10	FPGA_B36_LVDS3A_12N_TX_IO49	DIFF_TX_3A12n/ B36	IO, 1.2V LVCMOS	Bank3A IO49 Single Ended I/O
12	FPGA_E47_LVDS3A_3P_RX_IO86	DIFF_RX_3A3p/ E47	IO, 1.2V LVDS	Bank3A 3p Rx differential Positive. Same pin can be configured as Single ended I/O.
14	FPGA_D48_LVDS3A_3N_RX_IO87	DIFF_RX_3A3n/ D48	IO, 1.2V LVDS	Bank3A 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
16	FPGA_A47_LVDS3A_3P_TX_IO84	DIFF_TX_3A3p/ A47	IO, 1.2V LVDS	Bank3A 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
18	FPGA_B48_LVDS3A_3N_TX_IO85	DIFF_TX_3A3n/ B48	IO, 1.2V LVDS	Bank3A 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
22	FPGA_F46_LVDS3A_5N_TX_IO77/CLKOUT_1N	DIFF_TX_3A5n/ F46	IO, 1.2V LVDS	Bank3A 5n Tx differential Negative. Same pin can be configured as Clock1 output differential Negative or Single ended I/O.
24	FPGA_G45_LVDS3A_5P_TX_IO76/CLKOUT_1P	DIFF_TX_3A5p/ G45	IO, 1.2V LVDS	Bank3A 5p Tx differential Positive. Same pin can be configured as Clock1 output differential Positive or Single ended I/O.
27	FPGA_E53_LVDS3A_1P_RX_IO94	DIFF_RX_3A1p/ E53	IO, 1.2V LVDS	Bank3A 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
28	FPGA_F50_LVDS3A_4N_RX_IO83	DIFF_RX_3A4n/ F50	IO, 1.2V LVDS	Bank3A 4n Rx differential Negative. Same pin can be configured as Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
29	FPGA_D54_LVDS3A_1N_RX_IO95	DIFF_RX_3A1n/ D54	IO, 1.2V LVDS	Bank3A 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
30	FPGA_G49_LVDS3A_4P_RX_IO82	DIFF_RX_3A4p/ D54	IO, 1.2V LVDS	Bank3A 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
31	FPGA_E51_LVDS3A_1P_TX_IO92	DIFF_TX_3A1p/ E51	IO, 1.2V LVDS	Bank3A 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
32	FPGA_G47_LVDS3A_4P_TX_IO80	DIFF_TX_3A4p/ G47	IO, 1.2V LVDS	Bank3A 4p Tx differential Positive. Same pin can be configured as Single ended I/O.
33	FPGA_D52_LVDS3A_1N_TX_IO93	DIFF_TX_3A1n/ D52	IO, 1.2V LVDS	Bank3A 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
34	FPGA_F48_LVDS3A_4N_TX_IO81	DIFF_TX_3A4n/ F48	IO, 1.2V LVDS	Bank3A 4n Tx differential Negative. Same pin can be configured as Single ended I/O.
38	FPGA_J45_LVDS3A_5P_RX_IO78	DIFF_RX_3A5p/ J45	IO, 1.2V LVDS	Bank3A 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
40	FPGA_K46_LVDS3A_5N_RX_IO79	DIFF_RX_3A5n/ K46	IO, 1.2V LVDS	Bank3A 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
42	FPGA_K44_LVDS3A_6N_RX_IO75	DIFF_RX_3A6n/ K44	IO, 1.2V LVDS	Bank3A 6n Rx differential Negative. Same pin can be configured as Single ended I/O.
44	FPGA_J43_LVDS3A_6P_RX_IO74	DIFF_RX_3A6p/ J43	IO, 1.2V LVDS	Bank3A 6p Rx differential Positive. Same pin can be configured as Single ended I/O.
46	FPGA_A45_LVDS3A_7P_TX_IO68	DIFF_TX_3A7p/ A45	IO, 1.2V LVDS	Bank3A 7p Tx differential Positive. Same pin can be configured as Single ended I/O.
48	FPGA_B46_LVDS3A_7N_TX_IO69	DIFF_TX_3A7n/ B46	IO, 1.2V LVDS	Bank3A 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
50	FPGA_A43_LVDS3A_8P_TX_IO64	DIFF_TX_3A8p/ A43	IO, 1.2V LVDS	Bank3A 8p Tx differential Positive. Same pin can be configured as Single ended I/O.
52	FPGA_B44_LVDS3A_8N_TX_IO65	DIFF_TX_3A8n/ B44	IO, 1.2V LVDS	Bank3A 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
56	FPGA_D46_LVDS3A_7N_RX_IO71/CLKIN_0N	DIFF_RX_3A7n/ D46	IO, 1.2V LVDS	Bank3A 7n Tx differential Negative. Same pin can be configured as Clock1 input differential Negative or Single ended I/O.
58	FPGA_E45_LVDS3A_7P_RX_IO70/CLKIN_0P	DIFF_RX_3A7p/ E45	IO, 1.2V LVDS	Bank3A 7p Rx differential Positive. Same pin can be configured as Clock1 input differential Positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
70	FPGA_E41_LVDS3A_9P_RX_IO62	DIFF_RX_3A9p/ E41	IO, 1.2V LVDS	Bank3A 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
72	FPGA_D42_LVDS3A_9N_RX_IO63	DIFF_RX_3A9n/ D42	IO, 1.2V LVDS	Bank3A 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
74	FPGA_A41_LVDS3A_9P_TX_IO60	DIFF_TX_3A9p/ A41	IO, 1.2V LVDS	Bank3A 9p Tx differential Positive. Same pin can be configured as Single ended I/O.
76	FPGA_B42_LVDS3A_9N_TX_IO61	DIFF_TX_3A9n/ B42	IO, 1.2V LVDS	Bank3A 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
82	FPGA_F44_LVDS3A_6N_TX_IO73/CLKIN_1N	DIFF_TX_3A6n/ F44	IO, 1.2V LVDS	Bank3A 6n Tx differential Negative. Same pin can be configured as Clock1 input differential Negative or Single ended I/O.
84	FPGA_G43_LVDS3A_6P_TX_IO72/CLKIN_1P	DIFF_TX_3A6p/ G43	IO, 1.2V LVDS	Bank3A 6p Tx differential Positive. Same pin can be configured as Clock1 input differential Positive or Single ended I/O.
87	FPGA_E49_LVDS3A_2P_RX_IOx	DIFF_RX_3A2p/ E49	IO, 1.2V LVDS	Bank3A 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
88	FPGA_D40_LVDS3A_10N_RX_IO59	DIFF_RX_3A10n/ D40	IO, 1.2V LVDS	Bank3A 10n Rx differential Negative. Same pin can be configured as Single ended I/O.
89	FPGA_D50_LVDS3A_2N_RX_IO91	DIFF_RX_3A2n/ D50	IO, 1.2V LVDS	Bank3A 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
91	FPGA_A49_LVDS3A_2P_TX_IO88	DIFF_TX_3A2p/ A49	IO, 1.2V LVDS	Bank3A 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
93	FPGA_B50_LVDS3A_2N_TX_IO89	DIFF_TX_3A2n/ B50	IO, 1.2V LVDS	Bank3A 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
116	FPGA_D44_LVDS3A_8N_RX_IO67/CLKOUT_0N	DIFF_RX_3A8n/ D44	IO, 1.2V LVDS	Bank3A 8n Rx differential Negative. Same pin can be configured as Clock0 output differential Negative or Single ended I/O.
118	FPGA_E43_LVDS3A_8P_RX_IO66/CLKOUT_0P	DIFF_RX_3A8p/ E43	IO, 1.2V LVDS	Bank3A 8p Rx differential Positive. Same pin can be configured as Clock0 output differential Positive or Clock1 output differential Positive or Single ended I/O.
130	FPGA_R41_LVDS3A_19P_RX_IO22/CLKIN_0P	DIFF_RX_3A19p/ R41	IO, 1.2V LVDS	Bank3A 19p Rx differential Positive. Same pin can be configured as Clock0 input differential Positive or Single ended I/O.

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
132	FPGA_P42_LVDS3A_19 N_RX_IO23/CLKIN_0N	DIFF_RX_3A19n/ P42	IO, 1.2V LVDS	Bank3A 3n Rx differential Negative. Same pin can be configured as Clock0 input differential Negative or Single ended I/O.
142	FPGA_M46_LVDS3A_17 N_TX_IO29/CLKOUT_1N	DIFF_RX_3A24p/ M46	IO, 1.2V LVDS	Bank3A 3n Tx differential Negative. Same pin can be configured as Clock1 output differential Negative or Single ended I/O.
144	FPGA_L45_LVDS3A_17P _TX_IO28/CLKOUT_1P	DIFF_TX_3A17p/ L45	IO, 1.2V LVDS	Bank3A 3p Tx differential Positive. Same pin can be configured as Clock1 output differential Positive or Single ended I/O.
147	FPGA_W41_LVDS3A_13 P_RX_IO46	DIFF_RX_3A13p/ W41	IO, 1.2V LVDS	Bank3A 13p Rx differential Positive. Same pin can be configured as Single ended I/O.
149	FPGA_Y42_LVDS3A_13 N_RX_IO47	DIFF_RX_3A13n/ Y42	IO, 1.2V LVDS	Bank3A 13n Rx differential Negative. Same pin can be configured as Single ended I/O.
151	FPGA_T42_LVDS3A_13 N_TX_IO45	DIFF_TX_3A13n/ T42	IO, 1.2V LVDS	Bank3A 13n Tx differential Negative. Same pin can be configured as Single ended I/O.
153	FPGA_U41_LVDS3A_13 P_TX_IO44	DIFF_TX_3A13p/ 13P	IO, 1.2V LVDS	Bank3A 13p Tx differential Positive. Same pin can be configured as Single ended I/O.
172	FPGA_L41_LVDS3A_19P _TX_IO20	DIFF_TX_3A19p/ 19P	IO, 1.2V LVDS	Bank3A 19p Tx differential Positive. Same pin can be configured as Single ended I/O.
176	FPGA_M40_LVDS3A_20 N_TX_IO17	DIFF_TX_3A24n/ 20N	IO, 1.2V LVDS	Bank3A 20n Tx differential Negative. Same pin can be configured as Single ended I/O.
178	FPGA_L39_LVDS3A_20P _TX_IO16	DIFF_TX_3A20p/ L39	IO, 1.2V LVDS	Bank3A 20p Tx differential Positive. Same pin can be configured as Single ended I/O.
207	FPGA_Y40_LVDS3A_14 N_RX_IO43	DIFF_RX_3A14n/ Y40	IO, 1.2V LVDS	Bank3A 14n Tx differential Negative. Same pin can be configured as Single ended I/O.
208	FPGA_M42_LVDS3A_19 N_TX_IO21	DIFF_RX_3A24p/ M42	IO, 1.2V LVCMOS	By default, SOM Power ok supported. *Optionally: Bank3A IO2 Single Ended I/O*
209	FPGA_W39_LVDS3A_14 P_RX_IO42	DIFF_RX_3A14p/ W39	IO, 1.2V LVDS	Bank3A 14p Rx differential Positive. Same pin can be configured as Single ended I/O.
211	FPGA_U39_LVDS3A_14 P_TX_IO40	DIFF_TX_3A14p/ U39	IO, 1.2V LVDS	Bank3A 14p Tx differential Positive. Same pin can be configured as Single ended I/O.
213	FPGA_T40_LVDS3A_14 N_TX_IO41	DIFF_TX_3A14n/ T40	IO, 1.2V LVDS	Bank3A 14n Tx differential Negative. Same pin can be configured as Single ended I/O.

2.6.4 HPS RGMII Interface

The Altera Agilex 7 SoC and FPGA SOM supports RGMII interface on Board-to-Board connector1. Connection of the Agilex 7 SoC and FPGA to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on RGMII pinouts on Board-to-Board connector1, refer the below table:

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
190	HPS_EMAC1_TX_CLK	HPS_IOB_1/ AF10	O, 1.8V LVCMOS/ 33E	Transmit clock.
192	HPS_EMAC1_TXD0	HPS_IOB_5/ AG7	O, 1.8V LVCMOS/ 33E	Transmit data bit0.
194	HPS_EMAC1_TXD1	HPS_IOB_6/ AP12	O, 1.8V LVCMOS/ 33E	Transmit data bit1.
196	HPS_EMAC1_TXD2	HPS_IOB_9/ AD12	O, 1.8V LVCMOS/ 33E	Transmit data bit2.
198	HPS_EMAC1_TXD3	HPS_IOB_10/ AM12	O, 1.8V LVCMOS/ 33E	Transmit data bit3.
210	HPS_EMAC1_TX_CTL	HPS_IOB_2/ AU11	O, 1.8V LVCMOS/ 33E	Transmit data control.
212	HPS_EMAC1_RX_CLK	HPS_IOB_3/ AF8	I, 1.8V LVCMOS	Receive clock.
214	HPS_EMAC1_RX_CTL	HPS_IOB_4/ AT12	I, 1.8V LVCMOS	Receive control.
224	HPS_EMAC1_RXD0	HPS_IOB_7/ AC13	I, 1.8V LVCMOS	Receive data bit0.
226	HPS_EMAC1_RXD1	HPS_IOB_8/ AN11	I, 1.8V LVCMOS	Receive data bit1.
228	HPS_EMAC1_RXD2	HPS_IOB_11/ AD10	I, 1.8V LVCMOS	Receive data bit2.
230	HPS_EMAC1_RXD3	HPS_IOB_12/ AL11	I, 1.8V LVCMOS	Receive data bit3.
124	HPS_MDIO1_MDC	HPS_IOA_10/ AT16	O, 1.8V LVCMOS	Management Clock.
126	HPS_MDIO1_MDIO	HPS_IOA_9/ AF14	IO, 1.8V LVCMOS	Management data IO.
92	HPS_GPIO0_10_ETH_RST_N	HPS_IOA_11/ AH10	O, 1.8V LVCMOS	NC. *Optionally: Reset Out GPIO.*

B2B-1 Pin No	B2B Connector1 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
94	HPS_GPIO0_11_ETH_INT	HPS_IOA_12/ AU15	I, 1.8V LVCMOS	Interrupt GPIO.

2.6.5 Power, Control & Miscellaneous Signals

The Altera Agilex 7 SoC and FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector1, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board-to-Board Connector1, refer the below table.

B2B-1 Pin No	B2B Connector1 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
208	SOM_PWR_OK	NA	O, 1.8V	Active High SOM power Good.
232	SOMPWR_EN	NA	I, 5V	Active High SOM power enable. *Important Note:* *High – SOM power ON* *Low – SOM Power OFF*
69	SDM_ADC_VSIGN_0	VSIGN_0/ CH52	I, DIFF	*NC.* *Analog differential input0 negative pin used with the voltage sensor inside the FPGA to monitor external analog voltages.*
71	SDM_ADC_VSIGP_0	VSIGP_0/ CG53	I, DIFF	*NC.* *Analog differential input0 positive pin used with the voltage sensor inside the FPGA to monitor external analog voltages.*
163	SDM_ADC_VSIGN_1	VSIGN_1/ CJ55	I, DIFF	*NC.* *Analog differential input1 negative pin used with the voltage sensor inside the FPGA to monitor external analog voltages.*
165	SDM_ADC_VSIGP_1	VSIGP_1/ CL55	I, DIFF	*NC.* *Analog differential input1 positive pin used with the voltage sensor inside the FPGA to monitor external analog voltages.*
90	PCIE_PERST_N_13A	I_PIN_PERST_N_13A_GXF/CG13 or FPGA_CK48_LVDS2A_21P_RX_IO14/CK48	IO, 1.8V LVCMOS	13A Bank PCIe reset. *Note: For PCIe end point this pin act as input, connected to CG13 of FPGA 13A Bank and for Root port act as output, connected from CK48 of LVDS 2A Bank* *Select between End point and root port reset is done by CP48 pin of LVDS 2A Bank.* *By default, CP48 pin is high, and PCIe root port reset is selected.*
164	TEMPDIODE_12A_GXF_DP	TEMPDIODE3P/ AG45	O, DIFF	*NC.* *Optionally temperature diode of 12A Bank differential Positive pin is connected.*
166	TEMPDIODE_12A_GXF_DN	TEMPDIODE3N/ AJ45	O, DIFF	*NC.* *Optionally temperature diode of 12A Bank differential Negative pin is connected.*

B2B-1 Pin No	B2B Connector1 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
168	TEMPDIODE_13A_GXF_DN	TEMPDIODE4N/ CA11	O, DIFF	*NC.* *Optionally temperature diode of 13A Bank differential Negative pin is connected.*
170	PCIE_PERST_N_12A/TEMPDIODE_13A_GXF_DP	I_PIN_PERST_N_12A_GXF/BR43 or FPGA_CL49_LVDS2A_21N_RX_IO15/CL49 or TEMPDIODE4P/ CB12	IO, 1.8V LVCMOS Or O, DIFF	12A Bank PCIe reset. *Note: For PCIe end point this pin act as input, connected to BR43 of FPGA 12A Bank and for Root port act as output, connected from CL49 of LVDS 2A Bank* *Select between End point and root port reset is done by CN49 pin of LVDS 2A Bank.* *By default, CN49 pin is high, and PCIe root port reset is selected.* *Optionally temperature diode of 13A Bank differential Positive pin is connected.*

B2B-1 Pin No	B2B Connector1 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	Power	Ground.

2.7 Board to Board Connector2

The Altera Agilex 7 SoC and FPGA SOM Board to Board Connector2 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector2 are explained in the following sections. The Board-to-Board Connector2 (J6) is physically located on bottom side of the SOM as shown below.

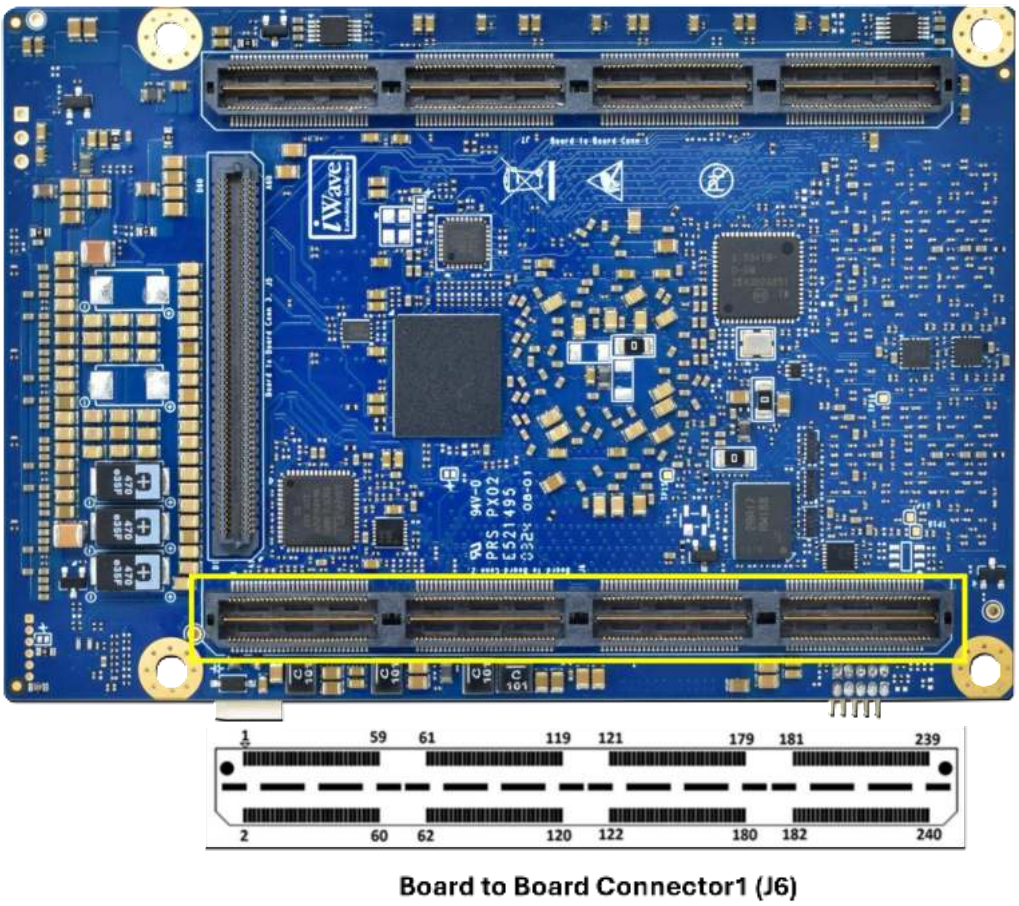

Figure 7: Board-to-Board Connector2

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A from Samtech

Mating Connector - QSH-120-01-L-D-Afrom Samtech

Staking Height - 5mm

Table 11: Board to Board Connector2 Pinout

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
NC	25	26	HPS_USB_OTG_DM
SDM_TDI_B2B	27	28	HPS_USB_OTG_DP
SDM_TMS_B2B	29	30	GND
SDM_TCK_B2B	31	32	HPS_USB_PWR_EN
SDM_TDO_B2B	33	34	HPS_USB_OTG_ID
SDM_HPS_NRESET_1V8	35	36	HPS_VBUS_USB
GND	37	38	HPS_I2C0_SDA_1V8*
GPHY_DTXRXM	39	40	SD_WP(GPIO1_19) *
GPHY_DTXRXP	41	42	SD_CD(GPIO1_18) *
GND	43	44	SD_PWR_EN(GPIO1_20) *
GPHY_CTXRXM	45	46	HPS_I2C0_SDA_1V8
GPHY_CTXRXP	47	48	HPS_I2C0_SCL_1V8
GND	49	50	QSPI_IO2*
GPHY_BTXRXM	51	52	QSPI_IO3*
GPHY_BTXRXP	53	54	HPS_UART1_TX
GND	55	56	HPS_UART1_RX
GPHY_ATXRXM	57	58	B_GPHY_LINK_LED2
GPHY_ATXRXP	59	60	B_GPHY_ACTIVITY_LED1
HPS_UART0_CTS	61	62	SD_DATA3/QSPI_CLK*
HPS_UART0_TX	63	64	SD_DATA2*
HPS_UART0_RTS	65	66	SD_DATA1*/SDM_nCONFIG_B2B
HPS_UART0_RX	67	68	VRTC_1V8/SDM_nSTATUS*
SD_DATA0/QSPI_CS*	69	70	HPS_I2C0_SCL_1V8/nCATTRIP_1V8*
SD_CMD/QSPI_IO0*	71	72	SD_CLK/QSPI_IO1*
GND	73	74	GND
FPGA_CR53_LVDS2A_19N_TX_IO21	75	76	FPGA_CP50_LVDS2A_20P_TX_IO16
FPGA_CT52_LVDS2A_19P_TX_IO20	77	78	FPGA_CN51_LVDS2A_20N_TX_IO17
FPGA_K48_LVDS3A_16N_TX_IO33	79	80	FPGA_Y38_LVDS3A_15N_RX_IO39
FPGA_J47_LVDS3A_16P_TX_IO32	81	82	FPGA_W37_LVDS3A_15P_RX_IO38
FPGA_M48_LVDS3A_16N_RX_IO35	83	84	FPGA_T38_LVDS3A_15N_TX_IO37

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
FPGA_L47_LVDS3A_16P_RX_IO34	85	86	FPGA_U37_LVDS3A_15P_TX_IO36
FPGA_R37_LVDS3A_21P_RX_IO14	87	88	FPGA_L37_LVDS3A_21P_TX_IO12
FPGA_P38_LVDS3A_21N_RX_IO15	89	90	FPGA_M38_LVDS3A_21N_TX_IO13
FPGA_G41_LVDS3A_22P_TX_IO8	91	92	FPGA_J39_LVDS3A_23P_RX_IO6
FPGA_F42_LVDS3A_22N_TX_IO9	93	94	FPGA_K40_LVDS3A_23N_RX_IO7
FPGA_G39_LVDS3A_23P_TX_IO4	95	96	FPGA_F38_LVDS3A_24N_TX_IO1
FPGA_F40_LVDS3A_23N_TX_IO5	97	98	FPGA_G37_LVDS3A_24P_TX_IO0
FPGA_A39_LVDS3A_10P_TX_IO56	99	100	FPGA_E35_LVDS3A_12P_RX_IO50
FPGA_B40_LVDS3A_10N_TX_IO57	101	102	FPGA_D36_LVDS3A_12N_RX_IO51
FPGA_A37_LVDS3A_11P_TX_IO52	103	104	FPGA_E37_LVDS3A_11P_RX_IO54
FPGA_B38_LVDS3A_11N_TX_IO53	105	106	FPGA_D38_LVDS3A_11N_RX_IO55
GND	107	108	GND
FPGA_CK50_LVDS2A_20P_RX_IO18/CLKOUT_0P	109	110	FPGA_R39_LVDS3A_20P_RX_IO18/CLKOUT_0P
FPGA_CL51_LVDS2A_20N_RX_IO19/CLKOUT_0N	111	112	FPGA_P40_LVDS3A_20N_RX_IO19/CLKOUT_0N
GND	113	114	GND
FPGA_CM52_LVDS2A_19P_RX_IO22/CLKIN_0P	115	116	SGMII_CLK125*
FPGA_CN53_LVDS2A_19N_RX_IO23/CLKIN_0N	117	118	NC
GND	119	120	GND
FPGA_P46_LVDS3A_17N_RX_IO31	121	122	FPGA_J41_LVDS3A_22P_RX_IO10
FPGA_R45_LVDS3A_17P_RX_IO30	123	124	FPGA_K42_LVDS3A_22N_RX_IO11
FPGA_P44_LVDS3A_18N_RX_IO27	125	126	FPGA_J37_LVDS3A_24P_RX_IO2
FPGA_R43_LVDS3A_18P_RX_IO26	127	128	FPGA_K38_LVDS3A_24N_RX_IO3
GND	129	130	GND
FPGA_CY54_LVDS2A_1P_RX_IO94	131	132	FPGA_DD54_LVDS2A_1P_TX_IO92
FPGA_DA55_LVDS2A_1N_RX_IO95	133	134	FPGA_DC55_LVDS2A_1N_TX_IO93
FPGA_CY52_LVDS2A_2P_RX_IO90	135	136	FPGA_DD52_LVDS2A_2P_TX_IO88*
FPGA_DA53_LVDS2A_2N_RX_IO91	137	138	FPGA_DC53_LVDS2A_2N_TX_IO89
FPGA_CY50_LVDS2A_3P_RX_IO86	139	140	FPGA_DD50_LVDS2A_3P_TX_IO84
FPGA_DA51_LVDS2A_3N_RX_IO87	141	142	FPGA_DC51_LVDS2A_3N_TX_IO85
FPGA_DE53_LVDS2A_4N_RX_IO83	143	144	FPGA_DH50_LVDS2A_4P_TX_IO80
FPGA_DF52_LVDS2A_4P_RX_IO82	145	146	FPGA_DG51_LVDS2A_4N_TX_IO81
FPGA_DF48_LVDS2A_5P_RX_IO78	147	148	FPGA_DF46_LVDS2A_6P_RX_IO74
FPGA_DE49_LVDS2A_5N_RX_IO79	149	150	FPGA_DE47_LVDS2A_6N_RX_IO75
FPGA_DD48_LVDS2A_7P_TX_IO68	151	152	FPGA_DD46_LVDS2A_8P_TX_IO64
FPGA_DC49_LVDS2A_7N_TX_IO69	153	154	FPGA_DC47_LVDS2A_8N_TX_IO65
FPGA_CY44_LVDS2A_9P_RX_IO62	155	156	FPGA_DD44_LVDS2A_9P_TX_IO60
FPGA_DA45_LVDS2A_9N_RX_IO63	157	158	FPGA_DC45_LVDS2A_9N_TX_IO61
FPGA_DF44_LVDS2A_10P_RX_IO58	159	160	FPGA_DJ45_LVDS2A_10N_TX_IO57
FPGA_DE45_LVDS2A_10N_RX_IO59	161	162	FPGA_DH44_LVDS2A_10P_TX_IO56
FPGA_DF42_LVDS2A_11P_RX_IO54	163	164	FPGA_DH42_LVDS2A_11P_TX_IO52
FPGA_DE43_LVDS2A_11N_RX_IO55	165	166	FPGA_DJ43_LVDS2A_11N_TX_IO53
GND	167	168	GND
FPGA_CY46_LVDS2A_8P_RX_IO66/CLKOUT_0P	169	170	FPGA_DH48_LVDS2A_5P_TX_IO76/CLKOUT_1P

Signal Name	B2B-2 Pin	B2B-2 Pin	Signal Name
FPGA_DA47_LVDS2A_8N_RX_IO67/CLKOUT_0N	171	172	FPGA_DJ49_LVDS2A_5N_TX_IO77/CLKOUT_1N
GND	173	174	GND
FPGA_CY48_LVDS2A_7P_RX_IO70/CLKIN_0P	175	176	FPGA_DH46_LVDS2A_6P_TX_IO72/CLKIN_1P
FPGA_DA49_LVDS2A_7N_RX_IO71/CLKIN_0N	177	178	FPGA_DJ47_LVDS2A_6N_TX_IO73/CLKIN_1N
GND	179	180	GND
FPGA_DE41_LVDS2A_12N_RX_IO51	181	182	FPGA_DH40_LVDS2A_12P_TX_IO48
FPGA_DF40_LVDS2A_12P_RX_IO50	183	184	FPGA_DJ41_LVDS2A_12N_TX_IO49
GND	185	186	GND
FGTR13A_RX_Q3_CH0P	187	188	REFCLK_FGTR13A_Q3_RX_CH6P
FGTR13A_RX_Q3_CH0N	189	190	REFCLK_FGTR13A_Q3_RX_CH6N
GND	191	192	GND
FGTR13A_TX_Q3_CH0P	193	194	FGTR13A_RX_Q3_CH3P
FGTR13A_TX_Q3_CH0N	195	196	FGTR13A_RX_Q3_CH3N
GND	197	198	GND
FGTR13A_RX_Q3_CH1P	199	200	FGTR13A_TX_Q3_CH3P
FGTR13A_RX_Q3_CH1N	201	202	FGTR13A_TX_Q3_CH3N
GND	203	204	GND
FGTR13A_TX_Q3_CH1P	205	206	NC
FGTR13A_TX_Q3_CH1N	207	208	NC
GND	209	210	GND
FGTR13A_RX_Q3_CH2P	211	212	NC
FGTR13A_RX_Q3_CH2N	213	214	NC
GND	215	216	GND
FGTR13A_TX_Q3_CH2P	217	218	NC
FGTR13A_TX_Q3_CH2N	219	220	NC
GND	221	222	GND
REFCLK_FGTR13A_Q3_RX_CH7P	223	224	VIO_BANK2A
REFCLK_FGTR13A_Q3_RX_CH7N	225	226	VIO_BANK3A
GND	227	228	GND
NC	229	230	TEMP_CORE_AP*
NC	231	232	TEMP_CORE_AN*
GND	233	234	GND
NC	235	236	CONFIG_DONE/TEMPDIODE_DTS_DP*
NC	237	238	TEMPDIODE_DTS_DN*
GND	239	240	GND

**Optional*

2.7.1 HPS & SDM Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Altera Agilex 7 SoC and FPGA device HPS & SDM banks are explained in the following section.

2.7.1.1 USB2.0 OTG Interface

The Altera Agilex 7 SoC and FPGA SOM supports one USB2.0 OTG interface on Board-to-Board Connector2. USB1 OTG controller of Altera Agilex 7 SoC and FPGA device HPS is used for USB2.0 OTG interface. The USB OTG controller can fulfil a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also, this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the HPS pins. The Altera Agilex 7 SoC and FPGA SOM supports “USB3320” ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Altera Agilex 7 SoC and FPGA SOM, HPS GPIO “HPS_GPIO0_IO10” can be optionally used for USB ULPI PHY reset. It supports active high power enable signal on Board-to-Board Connector2 from USB PHY for external VBUS power control.

Also, Altera Agilex 7 SoC and FPGA SOM supports USB ID & USB VBUS inputs from Board-to-Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
26	HPS_USB_OTG_DM	NA	IO, USB	USB OTG data negative.
28	HPS_USB_OTG_DP	NA	IO, USB	USB OTG data positive.
32	HPS_USB_PWR_EN	NA	O, 3.3V CMOS	USB active high power enable output to control external USB VBUS.
34	HPS_USB_OTG_ID	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
36	HPS_VBUS_USB	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.7.1.2 SD/SDIO Interface (Optional)

The Altera Agilex 7 SoC and FPGA SOM optionally supports SD/SDIO interface on Board-to-Board Connector2. The SDMMC controller of Altera Agilex 7 SoC and FPGA HPS can be used for SD/SDIO interface on the Board-to-Board Connector. By default, these lines are connected to the On SOM eMMC. This SD/SDIO/MMC controller supports One eMMC version 4.5 with DMA and CE-ATA support, SD, including eSD, version 3.0, SDIO, including eSDIO, version 3.0, CE-ATA version 1.1. It supports up to 50MHz operating frequency. Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Altera Agilex 7 SoC and FPGA SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through HPS pins.

For more details on SD/SDIO Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
40	SD_WP(GPIO1_19)	HPS_IOB_20/ AJ13	O, 1.8V LVCMOS	SD Write Protect.
42	SD_CD(GPIO1_18)	HPS_IOB_19/ AB10	I, 1.8V LVCMOS	SD Card Detect.
44	SD_PWR_EN(GPIO1_20)	HPS_IOB_21/ AH14	O, 1.8V LVCMOS	SD Power Enable/Voltage select through HPS GPIO.
62	SD_DATA3	HPS_IOB_18/ AM10	IO, 1.8V LVCMOS	SD DATA3.
64	SD_DATA2	HPS_IOB_17/ AC9	IO, 1.8V LVCMOS	SD DATA2.
66	SD_DATA1	HPS_IOB_16/ AP10	IO, 1.8V LVCMOS	SD DATA1.
63	SD_DATA0	HPS_IOB_13/ AC11	IO, 1.8V LVCMOS	SD DATA0.
71	SD_CMD	HPS_IOB_14/ AT10	IO, 1.8V LVCMOS	SD Command.
72	SD_CLK	HPS_IOB_15/ AD8	O, 1.8V LVCMOS	SD Clock.

2.7.1.3 Debug UART Interface

The Altera Agilex 7 SoC and FPGA SOM supports one Debug UART interface on Board-to-Board Connector2. The UART1 controller of Altera Agilex 7 SoC and FPGA HPS is used for Debug UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
54	HPS_UART1_TX	HPS_IOB_7/ AG13	O, 1.8V LVCMOS	UART1 Transmit data line for Debug.
56	HPS_UART1_RX	HPS_IOB_8/ AP16	I, 1.8V LVCMOS	UART1 Receive data line for Debug.

2.7.1.4 Data UART Interface

The Altera Agilex 7 SoC and FPGA SOM supports one DATA UART interface on Board-to-Board Connector2. The UART0 controller of Altera Agilex 7 SoC and FPGA device HPS is used for Data UART interface through HPS pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates.

For more details on Data UART pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
63	HPS_UART0_TX	HPS_IOA_3/ AJ11	O, 1.8V LVCMOS	UART0 Transmit data line
67	HPS_UART0_RX	HPS_IOA_4/ AM16	I, 1.8V LVCMOS	UART0 Receive data line
61	HPS_UART0_CTS	HPS_IOA_1/ AC15	O, 1.8V LVCMOS	UART0 Clear to Send data line
65	HPS_UART0_RTS	HPS_IOA_2/ AL15	I, 1.8V LVCMOS	UART0 Request to Send data line

2.7.1.5 I2C Interface

The Altera Agilex 7 SoC and FPGA SOM supports one I2C interface from HPS on Board-to-Board Connector2. The I2C0 module of Altera Agilex 7 SoC and FPGA device's HPS is used for I2C interface through HPS pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM On SOM Regulators & Clock Generators in the Altera Agilex 7 SoC and FPGA SOM.

Note: For the same I2C0 On SOM temperature sensor, EPROM and FPGA IO Bank switch voltage regulator is connected with address 0x48, 0x56 and 0x1E respectively.

For more details on I2C Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
46	HPS_I2C0_SDA_1V8	HPS_IOA_5/ AH12	IO, 1.8V OD/ 4.7K PU	I2C0 data.
48	HPS_I2C0_SCL_1V8	HPS_IOA_6/ AN15	O, 1.8V OD/ 4.7K PU	I2C0 clock.

2.7.1.6 JTAG Interface - From SDM Bank

The Altera Agilex 7 SoC and FPGA SOM supports JTAG interface on Board-to-Board Connector2. The Altera Agilex 7 SoC and FPGA device's HPS and SDM share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Altera Agilex 7 SoC and FPGA device. These JTAG interface signals are also connected to on-board JTAG connector. The JTAG connection can be selected to either Board-to-Board Connector2 or On Board JTAG Header using the On-Board Switch.

For more details on JTAG Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
27	SDM_TDI_B2B	TDI/ CC43	I, 1.8V LVCMOS/ 10K PU	JTAG Test Data Input.
29	SDM_TMS_B2B	TMS/ CE43	I, 1.8V LVCMOS/ 10K PU	JTAG Test Mode Select.
31	SDM_TCK_B2B	TCK/ CF44	I, 1.8V LVCMOS/ 1K PD	JTAG Test Clock.
33	SDM_TDO_B2B	TDO/ CC49	O, 1.8V LVCMOS	JTAG Test Data Output.

2.7.1.7 Configuration QSPI Interface – From SDM Bank (Optional)

The Altera Agilex 7 SoC and FPGA SOM the QSPI lines are connected to the On-SOM QSPI Flash and same lines are optionally connected to Board-to-Board Connector2 from the SDM Bank. The QSPI controller of Altera Agilex 7 SoC and FPGA SDM is used for QSPI interface through SDM pins. By default, the On-SOM QSPI Flash will be supported.

For more details on QSPI Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
62	QSPI_CLK	SDM_IO2/ CH48	O, 1.8V LVCMOS	QSPI clock.
71	QSPI_IO0	SDM_IO4/ CG45	IO, 1.8V LVCMOS	QSPI IO0.
72	QSPI_IO1	SDM_IO1/ CA45	IO, 1.8V LVCMOS	QSPI IO1.
50	QSPI_IO2	SDM_IO3/ CF46	IO, 1.8V LVCMOS	QSPI IO2.
52	QSPI_IO3	SDM_IO6/ CH46	IO, 1.8V LVCMOS	QSPI IO3.
69	QSPI_CS	SDM_IO5 / CC45	O, 1.8V LVCMOS	QSPI Chip Select.

2.7.2 HPS to FPGA routed Interfaces.

The Altera Agilex 7 SoC FPGA supports routing of interfaces from HPS to FPGA. The interfaces which are supported in Board-to-Board Connector2 from Altera Agilex 7 SoC and FPGA device that are routed from HPS to FPGA are explained in the following section.

2.7.2.1 Gigabit Ethernet Interface

The Altera Agilex 7 SoC and FPGA SOM supports one 10/100/1000 Mbps Ethernet interface on Board-to-Board Connector2. The MAC is integrated in the Altera Agilex 7 SoC and FPGA Serdes is connected to the external Gigabit Ethernet PHY "88E1512" on SOM. This Gigabit Ethernet PHY is interfaced with EMAC0 interface of Altera Agilex.

In Altera Agilex 7 SoC EMAC0 RGMII Signal are routed to FPGA in internally and RGMII Lines are converted to SGMII Using soft adopter logics. Also, SOM supports Ethernet PHY interrupt through FPGA 13A Bank Quad 3 Channel 2. This PHY supports active high Link and Activity LED indication signals and available on Board-to-Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the Carrier board.

For more details on Gigabit Ethernet Interface pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
39	GPHY_DTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
41	GPHY_DTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
45	GPHY_CTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
47	GPHY_CTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
51	GPHY_BTXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
53	GPHY_BTXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
57	GPHY_ATXRXM	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
59	GPHY_ATXRXP	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
58	B_GPHY_LINK_LED	NA	O, 1.8V CMOS	Gigabit Ethernet 1000Mbps Link status LED (Active High).
60	B_GPHY_ACTIVITY_LED	NA	O, 1.8V CMOS	Gigabit Ethernet Activity LED (Active High).

2.7.3 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector2 from Altera Agilex 7 SoC and FPGA device's FPGA is explained in the following section.

2.7.3.1 High Speed Transceivers

The Altera Agilex 7 SoC and FPGA SOM supports 4 high speed transceiver channels from FGT 13A Bank Quad3 supports 4 Transceiver channels on Board-to-Board connector2. In Altera Agilex 7 SoC and FPGA SOM, the Transceivers connected to Board-to-Board Connector2 is capable of running up to a maximum speed of 17.4Gbps in NRZ Format or 32Gbps in PAM4 Format. These transceivers can be used to interface to multiple high-speed interface protocols. This 4 Channel Transceiver Bank Quad3 supports two reference clock input pairs.

Note2: Based on Device bank names will change. In this datasheet AGF 014 Device considered.

For more details on FGTL 13A transceiver pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT_13A Quad3 Channels				
193	FGTR13A_TX_Q3_CH0P	FGTR13A_TX_Q3_CH0P/ CF4	O, DIFF	Bank FGT13A-Q3 channel0 High speed differential transmitter positive.
195	FGTR13A_TX_Q3_CH0N	FGTR13A_TX_Q3_CH0N/ CG5	O, DIFF	Bank FGT13A-Q3 channel0 High speed differential transmitter negative.
205	FGTR13A_TX_Q3_CH1P	FGTR13A_TX_Q3_CH1P/ CK4	O, DIFF	Bank FGT13A-Q3 channel1 High speed differential transmitter positive.
207	FGTR13A_TX_Q3_CH1N	FGTR13A_TX_Q3_CH1N/ CL5	O, DIFF	Bank FGT13A-Q3 channel1 High speed differential transmitter negative.
217	FGTR13A_TX_Q3_CH2P	FGTR13A_TX_Q3_CH2P/ CN7	O, DIFF	NC. *By default, FGT13A-Q3 channel2 used for On SOM SGMII Ethernet PHY.* *Optionally: Connected to B2B Connector pin no 217.*
219	FGTR13A_TX_Q3_CH2N	FGTR13A_TX_Q3_CH2N/ CM8	O, DIFF	NC. *By default, FGT13A-Q3 channel2 used for On SOM SGMII Ethernet PHY.* *Optionally: Connected to B2B Connector pin no 219.*
200	FGTR13A_TX_Q3_CH3P	FGTR13A_TX_Q3_CH3P/ CU7	O, DIFF	Bank FGT13A-Q3 channel3 High speed differential transmitter positive.

B2B-2 Pin No	B2B Connector2 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
202	FGTR13A_TX_Q3_CH3N	FGTR13A_TX_Q3_CH3N/ CT8	O, DIFF	Bank FGT13A-Q3 channel3 High speed differential transmitter negative.
187	FGTR13A_RX_Q3_CH0P	FGTR13A_RX_Q3_CH0P/ CN1	I, DIFF	Bank FGT13A-Q3 channel0 High speed differential transmitter positive.
189	FGTR13A_RX_Q3_CH0N	FGTR13A_RX_Q3_CH0N/ CM2	I, DIFF	Bank FGT13A-Q3 channel0 High speed differential receiver negative.
199	FGTR13A_RX_Q3_CH1P	FGTR13A_RX_Q3_CH1P/ CP4	I, DIFF	Bank FGT13A-Q3 channel1 High speed differential receiver positive.
201	FGTR13A_RX_Q3_CH1N	FGTR13A_RX_Q3_CH1N/ CR5	I, DIFF	Bank FGT13A-Q3 channel1 High speed differential receiver negative.
211	FGTR13A_RX_Q3_CH2P	FGTR13A_RX_Q3_CH2P/ CU1	I, DIFF	Bank FGT13A-Q3 channel2 High speed differential receiver positive.
213	FGTR13A_RX_Q3_CH2N	FGTR13A_RX_Q3_CH2N/ CT2	I, DIFF	Bank FGT13A-Q3 channel2 High speed differential receiver negative.
194	FGTR13A_RX_Q3_CH3P	FGTR13A_RX_Q3_CH3P/ CV4	I, DIFF	Bank FGT13A-Q3 channel3 High speed differential receiver positive.
196	FGTR13A_RX_Q3_CH3N	FGTR13A_RX_Q3_CH3N/ CW5	I, DIFF	Bank FGT13A-Q3 channel3 High speed differential receiver negative.
188	REFCLK_FGTR13A_Q3_RX_CH6P	REFCLK_FGTR13A_Q3_RX_CH6P/ CJ7	I, DIFF	Bank FGT13A-Q3 High speed differential Clock6 positive. Regional reference clock, this clock can be used for 13A Bank Q3 and Q2 Transceivers.
190	REFCLK_FGTR13A_Q3_RX_CH6N	REFCLK_FGTR13A_Q3_RX_CH6N/ CH8	I, DIFF	Bank FGT13A-Q3 High speed differential Clock6 negative. Regional reference clock, this clock can be used for 13A Bank Q3 and Q2 Transceivers.
223	REFCLK_FGTR13A_Q3_RX_CH7P	REFCLK_FGTR13A_Q3_RX_CH7P/ CF10	I, DIFF	Bank FGT13A-Q3 High speed differential Clock7 positive. Regional reference clock, this clock can be used for 13A Bank Q3 and Q2 Transceivers.
225	REFCLK_FGTR13A_Q3_RX_CH7N	REFCLK_FGTR13A_Q3_RX_CH7N/ CD10	I, DIFF	Bank FGT13A-Q3 High speed differential Clock7 negative. Regional reference clock, this clock can be used for 13A Bank Q3 and Q2 Transceivers.

2.7.4 FPGA IOs & General-Purpose Clocks – Bank2A

The Altera Agilex 7 SoC and FPGA SOM supports up to 28 LVDS or 56 Single Ended IOs and from Altera Agilex 7 FPGA Bank2A and on Board-to-Board connector2. In Altera Agilex 7 SoC and FPGA SOM, Bank2A signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank2A signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

Bank2A and 3A IO Voltage given in Pin 224 and 226 Respectively in Board-to-Board connector2.

In Altera Agilex 7 SoC and FPGA SOM, upon these 28 LVDS or 56 Single Ended IOs from Altera Agilex 7 FPGA Bank2A, Three General Purpose Clock input LVDS pair and Three General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Altera Agilex 7 SoC and FPGA SOM, Bank3A I/O voltage is set to **1.2V**.

For more details on Altera Agilex 7 SoC and FPGA Bank2A pinouts on Board-to-Board Connector1, refer the below table.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
75	FPGA_CR53_LVDS2A_19N_TX_IO21	DIFF_TX_2A19n/CR53	IO, 1.2V LVDS	Bank2A 19n Tx differential Negative. Same pin can be configured as Single ended I/O.
77	FPGA_CT52_LVDS2A_19P_TX_IO20	DIFF_TX_2A19p/CT52	IO, 1.2V LVDS	Bank2A 19p Tx differential Positive. Same pin can be configured as Single ended I/O.
76	FPGA_CP50_LVDS2A_20P_TX_IO16	DIFF_TX_2A20p/CP50	IO, 1.2V LVDS	Bank2A 20p Tx differential Positive. Same pin can be configured as Single ended I/O.
78	FPGA_CN51_LVDS2A_20N_TX_IO17	DIFF_TX_2A20n/CN51	IO, 1.2V LVDS	Bank2A 20n Tx differential Negative. Same pin can be configured as Single ended I/O.
109	FPGA_CK50_LVDS2A_20P_RX_IO18/CLKOUT_0P	DIFF_RX_2A20p/CK50	IO, 1.2V LVDS	Bank2A 20p Rx differential Positive. Same pin can be configured as Clock0 output differential Positive or Single ended I/O
111	FPGA_CL51_LVDS2A_20N_RX_IO19/CLKOUT_0N	DIFF_RX_2A20n/CL51	IO, 1.2V LVDS	Bank2A 20n Rx differential Negative. Same pin can be configured as Clock0 output differential Negative or Single ended I/O.
115	FPGA_CM52_LVDS2A_19P_RX_IO22/CLKIN_0P	DIFF_RX_2A19p/CM52	IO, 1.2V LVDS	Bank2A 19p Rx differential Positive. Same pin can be configured as Clock0 input differential Positive or Single ended I/O

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
117	FPGA_CN53_LVDS2A_19N_RX_IO23/CLKIN_0N	DIFF_RX_2A19n/CN53	IO, 1.2V LVDS	Bank2A 19n Rx differential Negative. Same pin can be configured as Clock0 input differential Negative or Single ended I/O.
131	FPGA_CY54_LVDS2A_1P_RX_IO94	DIFF_RX_2A1p/CY54	IO, 1.2V LVDS	Bank2A 1p Rx differential Positive. Same pin can be configured as Single ended I/O.
133	FPGA_DA55_LVDS2A_1N_RX_IO95	DIFF_RX_2A1n/DA55	IO, 1.2V LVDS	Bank2A 1n Rx differential Negative. Same pin can be configured as Single ended I/O.
135	FPGA_CY52_LVDS2A_2P_RX_IO90	DIFF_RX_2A2p/CY52	IO, 1.2V LVDS	Bank2A 2p Rx differential Positive. Same pin can be configured as Single ended I/O.
137	FPGA_DA53_LVDS2A_2N_RX_IO91	DIFF_RX_2A2n/DA53	IO, 1.2V LVDS	Bank2A 2n Rx differential Negative. Same pin can be configured as Single ended I/O.
139	FPGA_CY50_LVDS2A_3P_RX_IO86	DIFF_RX_2A3p/CY50	IO, 1.2V LVDS	Bank2A 3p Rx differential Positive. Same pin can be configured as Single ended I/O.
141	FPGA_DA51_LVDS2A_3N_RX_IO87	DIFF_RX_2A3n/DA51	IO, 1.2V LVDS	Bank2A 3n Rx differential Negative. Same pin can be configured as Single ended I/O.
143	FPGA_DE53_LVDS2A_4N_RX_IO83	DIFF_RX_2A4n/DE53	IO, 1.2V LVDS	Bank2A 4n Rx differential Negative. Same pin can be configured as Single ended I/O.
145	FPGA_DF52_LVDS2A_4P_RX_IO82	DIFF_RX_2A4p/DF52	IO, 1.2V LVDS	Bank2A 4p Rx differential Positive. Same pin can be configured as Single ended I/O.
147	FPGA_DF48_LVDS2A_5P_RX_IO78	DIFF_RX_2A5p/DF48	IO, 1.2V LVDS	Bank2A 5p Rx differential Positive. Same pin can be configured as Single ended I/O.
149	FPGA_DE49_LVDS2A_5N_RX_IO79	DIFF_RX_2A5n/DE49	IO, 1.2V LVDS	Bank2A 5n Rx differential Negative. Same pin can be configured as Single ended I/O.
151	FPGA_DD48_LVDS2A_7P_TX_IO68	DIFF_TX_2A7p/DD48	IO, 1.2V LVDS	Bank2A 7p Tx differential Positive. Same pin can be configured as Single ended I/O.
153	FPGA_DC49_LVDS2A_7N_TX_IO69	DIFF_TX_2A7n/DC49	IO, 1.2V LVDS	Bank2A 7n Tx differential Negative. Same pin can be configured as Single ended I/O.
155	FPGA_CY44_LVDS2A_9P_RX_IO62	DIFF_RX_2A9p/CY44	IO, 1.2V LVDS	Bank2A 9p Rx differential Positive. Same pin can be configured as Single ended I/O.
157	FPGA_DA45_LVDS2A_9N_RX_IO63	DIFF_RX_2A9n/DA45	IO, 1.2V LVDS	Bank2A 9n Rx differential Negative. Same pin can be configured as Single ended I/O.
159	FPGA_DF44_LVDS2A_10P_RX_IO58	DIFF_RX_2A10p/DF44	IO, 1.2V LVDS	Bank2A 10p Rx differential Positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
161	FPGA_DE45_LVDS2A_10N_RX_IO59	DIFF_RX_2A10n/DE45	IO, 1.2V LVDS	Bank2A 10n Rx differential Negative. Same pin can be configured as Single ended I/O.
163	FPGA_DF42_LVDS2A_11P_RX_IO54	DIFF_RX_2A11p/DF42	IO, 1.2V LVDS	Bank2A 11p Rx differential Positive. Same pin can be configured as Single ended I/O.
165	FPGA_DE43_LVDS2A_11N_RX_IO55	DIFF_RX_2A11n/DE43	IO, 1.2V LVDS	Bank2A 11n Rx differential Negative. Same pin can be configured as Single ended I/O.
132	FPGA_DD54_LVDS2A_1P_TX_IO92	DIFF_TX_2A1p/DD54	IO, 1.2V LVDS	Bank2A 1p Tx differential Positive. Same pin can be configured as Single ended I/O.
134	FPGA_DC55_LVDS2A_1N_TX_IO93	DIFF_TX_2A1n/DC55	IO, 1.2V LVDS	Bank2A 1n Tx differential Negative. Same pin can be configured as Single ended I/O.
136	FPGA_DD52_LVDS2A_2P_TX_IO88*	DIFF_TX_2A2p/DD52	IO, 1.2V LVDS	Bank2A 2p Tx differential Positive. Same pin can be configured as Single ended I/O.
138	FPGA_DC53_LVDS2A_2N_TX_IO89	DIFF_TX_2A2n/DC53	IO, 1.2V LVDS	Bank2A 2n Tx differential Negative. Same pin can be configured as Single ended I/O.
140	FPGA_DD50_LVDS2A_3P_TX_IO84	DIFF_TX_2A3p/DD50	IO, 1.2V LVDS	Bank2A 3p Tx differential Positive. Same pin can be configured as Single ended I/O.
142	FPGA_DC51_LVDS2A_3N_TX_IO85	DIFF_TX_2A3n/DC51	IO, 1.2V LVDS	Bank2A 3n Tx differential Negative. Same pin can be configured as Single ended I/O.
144	FPGA_DH50_LVDS2A_4P_TX_IO80	DIFF_TX_2A4p/DH50	IO, 1.2V LVDS	Bank2A 4p Tx differential Positive. Same pin can be configured as Single ended I/O.
146	FPGA_DG51_LVDS2A_4N_TX_IO81	DIFF_TX_2A4n/DG51	IO, 1.2V LVDS	Bank2A 4n Tx differential Negative. Same pin can be configured as Single ended I/O.
148	FPGA_DF46_LVDS2A_6P_RX_IO74	DIFF_RX_2A6p/DF46	IO, 1.2V LVDS	Bank2A 6p Rx differential Positive. Same pin can be configured as Single ended I/O.
150	FPGA_DE47_LVDS2A_6N_RX_IO75	DIFF_RX_2A6n/DE47	IO, 1.2V LVDS	Bank2A 2n 6x differential Negative. Same pin can be configured as Single ended I/O.
152	FPGA_DD46_LVDS2A_8P_TX_IO64	DIFF_TX_2A8p/DD46	IO, 1.2V LVDS	Bank2A 8p Tx differential Positive. Same pin can be configured as Single ended I/O.
154	FPGA_DC47_LVDS2A_8N_TX_IO65	DIFF_TX_2A8n/DC47	IO, 1.2V LVDS	Bank2A 8n Tx differential Negative. Same pin can be configured as Single ended I/O.
156	FPGA_DD44_LVDS2A_9P_TX_IO60	DIFF_TX_2A9p/DD44	IO, 1.2V LVDS	Bank2A 9p Tx differential Positive. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
158	FPGA_DC45_LVDS2A_9N_TX_IO61	DIFF_TX_2A9n/DC45	IO, 1.2V LVDS	Bank2A 9n Tx differential Negative. Same pin can be configured as Single ended I/O.
160	FPGA_DJ45_LVDS2A_10N_TX_IO57	DIFF_TX_2A10n/DJ45	IO, 1.2V LVDS	Bank2A 10n Tx differential Negative. Same pin can be configured as Single ended I/O.
162	FPGA_DH44_LVDS2A_10P_TX_IO56	DIFF_TX_2A10p/DH44	IO, 1.2V LVDS	Bank2A 10p Tx differential Positive. Same pin can be configured as Single ended I/O.
164	FPGA_DH42_LVDS2A_11P_TX_IO52	DIFF_TX_2A11p/DH42	IO, 1.2V LVDS	Bank2A 11p Tx differential Positive. Same pin can be configured as Single ended I/O.
166	FPGA_DJ43_LVDS2A_11N_TX_IO53	DIFF_TX_2A11n/DJ43	IO, 1.2V LVDS	Bank2A 11n Tx differential Negative. Same pin can be configured as Single ended I/O.
169	FPGA_CY46_LVDS2A_8P_RX_IO66/CLKOUT_0P	DIFF_RX_2A8p/CY46	IO, 1.2V LVDS	Bank2A 8p Rx differential Positive. Same pin can be configured as Clock0 output differential Positive or Single ended I/O
171	FPGA_DA47_LVDS2A_8N_RX_IO67/CLKOUT_0N	DIFF_RX_2A8n/DA47	IO, 1.2V LVDS	Bank2A 8n Rx differential Negative. Same pin can be configured as Clock0 output differential Negative or Single ended I/O.
170	FPGA_DH48_LVDS2A_5P_TX_IO76/CLKOUT_1P	DIFF_TX_2A5p/DH48	IO, 1.2V LVDS	Bank2A 5p Rx differential Positive. Same pin can be configured as Clock1 output differential Positive or Single ended I/O
172	FPGA_DJ49_LVDS2A_5N_TX_IO77/CLKOUT_1N	DIFF_TX_2A5n/DJ49	IO, 1.2V LVDS	Bank2A 5n Rx differential Negative. Same pin can be configured as Clock1 output differential Negative or Single ended I/O.
175	FPGA_CY48_LVDS2A_7P_RX_IO70/CLKIN_0P	DIFF_RX_2A7p/CY48	IO, 1.2V LVDS	Bank2A 7p Rx differential Positive. Same pin can be configured as Clock0 input differential Positive or Single ended I/O
177	FPGA_DA49_LVDS2A_7N_RX_IO71/CLKIN_0N	DIFF_RX_2A7n/DA49	IO, 1.2V LVDS	Bank2A 7n Rx differential Negative. Same pin can be configured as Clock0 input differential Negative or Single ended I/O.
176	FPGA_DH46_LVDS2A_6P_TX_IO72/CLKIN_1P	DIFF_TX_2A6p/DH46	IO, 1.2V LVDS	Bank2A 6p Rx differential Positive. Same pin can be configured as Clock0 input differential Positive or Single ended I/O
178	FPGA_DJ47_LVDS2A_6N_TX_IO73/CLKIN_1N	DIFF_TX_2A6n/DJ47	IO, 1.2V LVDS	Bank2A 6n Rx differential Negative. Same pin can be configured as Clock0 input differential Negative or Single ended I/O.
181	FPGA_DE41_LVDS2A_12N_RX_IO51	DIFF_RX_2A12n/DE41	IO, 1.2V LVDS	Bank2A 12n Rx differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
183	FPGA_DF40_LVDS2A_12P_RX_IO50	DIFF_RX_2A12p/DF40	IO, 1.2V LVDS	Bank2A 12p Rx differential Positive. Same pin can be configured as Single ended I/O.
182	FPGA_DH40_LVDS2A_12P_TX_IO48	DIFF_TX_2A12p/DH40	IO, 1.2V LVDS	Bank2A 12p Tx differential Positive. Same pin can be configured as Single ended I/O.
184	FPGA_DJ41_LVDS2A_12N_TX_IO49	DIFF_TX_2A12n/DJ41	IO, 1.2V LVDS	Bank2A 12n Tx differential Negative. Same pin can be configured as Single ended I/O.
224	VIO_BANK2A	NA	O, 1.2V Power	Bank2A IO Voltage.

2.7.5 FPGA IOs & General-Purpose Clocks – Bank3A

The Altera Agilex 7 SoC and FPGA SOM supports up to 19 LVDS or 38 Single Ended IOs and from Altera Agilex 7 FPGA Bank3A on Board-to-Board connector2. In Altera Agilex 7 SoC and FPGA SOM, Bank3A signals are routed as LVDS IOs to Board-to-Board Connector1. Even though Bank3A signals are routed as LVDS IOs, these pins can be used as SE IOs if required.

In Altera Agilex 7 SoC and FPGA SOM, upon these 19 LVDS or 38 Single Ended IOs from Altera Agilex 7 FPGA Bank3A, One General Purpose Clock Output LVDS pairs are supported on Board-to-Board connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General-Purpose single ended clock. In Altera Agilex 7 SoC and FPGA SOM, Bank3A I/O voltage is set to **1.2V.** Contact iWave if **1.5V** voltage support is required. For Bank3A IO Output Voltage refer B2B-2 Pin 226.

For more details on Altera Agilex 7 SoC and FPGA Bank3A pinouts on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
79	FPGA_K48_LVDS3A_16N_TX_IO33	DIFF_TX_3A16n/ K48	IO, 1.2V LVCMOS	Bank3A 16n Tx differential Negative. Same pin can be configured as Single ended I/O.
81	FPGA_J47_LVDS3A_16P_TX_IO32	DIFF_TX_3A16p/ J47	IO, 1.2V LVCMOS	Bank3A 16p Tx differential Positive. Same pin can be configured as Single ended I/O.
83	FPGA_M48_LVDS3A_16N_RX_IO35	DIFF_RX_3A16n/ M48	IO, 1.2V LVCMOS	Bank3A 16n Rx differential Negative. Same pin can be configured as Single ended I/O.
85	FPGA_L47_LVDS3A_16P_RX_IO34	DIFF_RX_3A16p/ M48	IO, 1.2V LVCMOS	Bank3A 16p Rx differential Positive. Same pin can be configured as Single ended I/O.
87	FPGA_R37_LVDS3A_21P_RX_IO14	DIFF_RX_3A21p/ R37	IO, 1.2V LVCMOS	Bank3A 21p Rx differential Positive. Same pin can be configured as Single ended I/O.
89	FPGA_P38_LVDS3A_21N_RX_IO15	DIFF_RX_3A21n/ P38	IO, 1.2V LVCMOS	Bank3A 21n Rx differential Negative. Same pin can be configured as Single ended I/O.
91	FPGA_G41_LVDS3A_22P_TX_IO8	DIFF_TX_3A22p/ G41	IO, 1.2V LVCMOS	Bank3A 22p Tx differential Positive. Same pin can be configured as Single ended I/O.
93	FPGA_F42_LVDS3A_22N_TX_IO9	DIFF_TX_3A22n/ F42	IO, 1.2V LVCMOS	Bank3A 22n Tx differential Negative. Same pin can be configured as Single ended I/O.
95	FPGA_G39_LVDS3A_23P_TX_IO4	DIFF_TX_3A23p/ G39	IO, 1.2V LVCMOS	Bank3A 23p Tx differential Positive. Same pin can be configured as Single ended I/O.
97	FPGA_F40_LVDS3A_23N_TX_IO5	DIFF_TX_3A23n/ F40	IO, 1.2V LVCMOS	Bank3A 23n Tx differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
99	FPGA_A39_LVDS3A_10P_TX_IO56	DIFF_TX_3A10p/ A39	IO, 1.2V LVCMOS	Bank3A 10p Tx differential Positive. Same pin can be configured as Single ended I/O.
101	FPGA_B40_LVDS3A_10N_TX_IO57	DIFF_TX_3A10n/ B40	IO, 1.2V LVCMOS	Bank3A 10n Tx differential Negative. Same pin can be configured as Single ended I/O.
103	FPGA_A37_LVDS3A_11P_TX_IO52	DIFF_TX_3A11p/ A37	IO, 1.2V LVCMOS	Bank3A 11p Tx differential Positive. Same pin can be configured as Single ended I/O.
105	FPGA_B38_LVDS3A_11N_TX_IO53	DIFF_TX_3A11n/ B38	IO, 1.2V LVCMOS	Bank3A 11n Tx differential Negative. Same pin can be configured as Single ended I/O.
121	FPGA_P46_LVDS3A_17N_RX_IO31	DIFF_RX_3A17n/ P46	IO, 1.2V LVCMOS	Bank3A 17n Rx differential Negative. Same pin can be configured as Single ended I/O.
123	FPGA_R45_LVDS3A_17P_RX_IO30	DIFF_RX_3A17p/ R45	IO, 1.2V LVCMOS	Bank3A 17p Rx differential Positive. Same pin can be configured as Single ended I/O.
125	FPGA_P44_LVDS3A_18N_RX_IO27	DIFF_RX_3A18n/ P44	IO, 1.2V LVCMOS	Bank3A 18n Rx differential Negative. Same pin can be configured as Single ended I/O.
127	FPGA_R43_LVDS3A_18P_RX_IO26	DIFF_RX_3A18p/ R43	IO, 1.2V LVCMOS	Bank3A 18p Rx differential Positive. Same pin can be configured as Single ended I/O.
80	FPGA_Y38_LVDS3A_15N_RX_IO39	DIFF_RX_3A15n/ Y38	IO, 1.2V LVCMOS	Bank3A 15n Rx differential Negative. Same pin can be configured as Single ended I/O.
82	FPGA_W37_LVDS3A_15P_RX_IO38	DIFF_RX_3A15p/ W37	IO, 1.2V LVCMOS	Bank3A 15p Rx differential Positive. Same pin can be configured as Single ended I/O.
84	FPGA_T38_LVDS3A_15N_TX_IO37	DIFF_TX_3A15n/ T38	IO, 1.2V LVCMOS	Bank3A 15n Tx differential Negative. Same pin can be configured as Single ended I/O.
86	FPGA_U37_LVDS3A_15P_TX_IO36	DIFF_TX_3A15p/ U37	IO, 1.2V LVCMOS	Bank3A 15p Tx differential Positive. Same pin can be configured as Single ended I/O.
88	FPGA_L37_LVDS3A_21P_TX_IO12	DIFF_TX_3A21p/ L37	IO, 1.2V LVCMOS	Bank3A 21p Tx differential Positive. Same pin can be configured as Single ended I/O.
90	FPGA_M38_LVDS3A_21N_TX_IO13	DIFF_TX_3A21n/ M38	IO, 1.2V LVCMOS	Bank3A 21n Tx differential Negative. Same pin can be configured as Single ended I/O.
92	FPGA_J39_LVDS3A_23P_RX_IO6	DIFF_RX_3A23p/ J39	IO, 1.2V LVCMOS	Bank3A 23p Rx differential Positive. Same pin can be configured as Single ended I/O.
94	FPGA_K40_LVDS3A_23N_RX_IO7	DIFF_RX_3A23n/ K40	IO, 1.2V LVCMOS	Bank3A 23n Rx differential Negative. Same pin can be configured as Single ended I/O.
96	FPGA_F38_LVDS3A_24N_TX_IO1	DIFF_TX_3A24n/ F38	IO, 1.2V LVCMOS	Bank3A 24n Tx differential Negative. Same pin can be configured as Single ended I/O.

B2B-2 Pin No	B2B Connector2 Net Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
98	FPGA_G37_LVDS3A_24P_TX_IO0	DIFF_TX_3A24p/ G37	IO, 1.2V LVCMOS	Bank3A 24p Tx differential Positive. Same pin can be configured as Single ended I/O.
100	FPGA_E35_LVDS3A_12P_RX_IO50	DIFF_RX_3A12p/ E35	IO, 1.2V LVCMOS	Bank3A 12p Rx differential Positive. Same pin can be configured as Single ended I/O.
102	FPGA_D36_LVDS3A_12N_RX_IO51	DIFF_RX_3A12n/ D36	IO, 1.2V LVCMOS	Bank3A 12n Rx differential Negative. Same pin can be configured as Single ended I/O.
104	FPGA_E37_LVDS3A_11P_RX_IO54	DIFF_RX_3A11p/ E37	IO, 1.2V LVCMOS	Bank3A 11p Rx differential Positive. Same pin can be configured as Single ended I/O.
106	FPGA_D38_LVDS3A_11N_RX_IO55	DIFF_RX_3A11n/ D38	IO, 1.2V LVCMOS	Bank3A 11n Rx differential Negative. Same pin can be configured as Single ended I/O.
110	FPGA_R39_LVDS3A_20P_RX_IO18/CLKOUT_0P	DIFF_RX_3A20p/ R39	IO, 1.2V LVCMOS	Bank3A 20p Rx differential Positive. Same pin can be configured as Clock0 output differential Positive or Single ended I/O.
112	FPGA_P40_LVDS3A_20N_RX_IO19/CLKOUT_0N	DIFF_RX_3A20n/ P40	IO, 1.2V LVCMOS	Bank3A 20n Rx differential Negative. Same pin can be configured as Clock0 output differential Negative or Single ended I/O.
122	FPGA_J41_LVDS3A_22P_RX_IO10	DIFF_RX_3A22p/ J41	IO, 1.2V LVCMOS	Bank3A 22p Rx differential Positive. Same pin can be configured as Single ended I/O.
124	FPGA_K42_LVDS3A_22N_RX_IO11	DIFF_RX_3A22n/ K42	IO, 1.2V LVCMOS	Bank3A 22n Rx differential Negative. Same pin can be configured as Single ended I/O.
126	FPGA_J37_LVDS3A_24P_RX_IO2	DIFF_RX_3A24p/ J37	IO, 1.2V LVCMOS	Bank3A 24p Rx differential Positive. Same pin can be configured as Single ended I/O.
128	FPGA_K38_LVDS3A_24N_RX_IO3	DIFF_RX_3A24n/ K38	IO, 1.2V LVCMOS	Bank3A 24n Rx differential Negative. Same pin can be configured as Single ended I/O.
226	VIO_BANK3A	NA	O, 1.2V/1.5V Power	Bank3A IO Voltage.

2.7.6 Power, Control, Reset & Miscellaneous Signals

The Altera Agilex 7 SoC and FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. In Board-to-Board Connector1, Ground pins are also distributed throughout the connector for better performance. In Board-to-Board Connector2, there are also Hardware Reset signal for resetting the SoC from Carrier Board and SOM Power Enable Signal for turning ON/OFF the SOM Power from the Carrier Board. Also, 3V RTC Power & 5V standby powers are connected to Board-to-Board Connector2.

For more details on Power pins on Board-to-Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	I, 5V Power	5V SOM Input Power.
68	VRTC_1V8	NA	Power	1.8V RTC Power.
35	SDM_HPS_nRESET_1V8	SDM_IO13/ CA43	I, 1.8V LVCMOS	Control Signal to reset the SoC.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	Power	Ground.
238	TEMPDIODE_DTS_DN	TEMPDIODE0CN/ AE43	I, DIFF	NC. *Note: This pins optionally connect to the internal temperature sensing diodes cathode in the FPGA core and corner areas of the FPGA.*

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
236	CONFIG_DONE/TEMPDIODE_DTS_DP	CONFIG_DONE/ CH44 or TEMPDIODE0CP/ AC43	I, DIFF	Option1: CONFIG_DONE, By default connected and this CONF_DONE pin indicates all configuration data has been received. Option2: NC. TEMPDIODE0CP *Note: This pins optionally connect to the internal temperature sensing diodes anode in the FPGA core and corner areas of the FPGA.*
230	TEMP_CORE_AP	TEMPDIODE0Ap/ CE49	I, DIFF	NC. *Note: This pins optionally connect to the internal temperature sensing diodes anode in the FPGA core and corner areas of the FPGA.*
232	TEMP_CORE_AN	TEMPDIODE0An/ CD50	I, DIFF	NC. *Note: This pins optionally connect to the internal temperature sensing diodes cathode in the FPGA core and corner areas of the FPGA.*
116	SGMII_CLK125	CLK_B_3A_1P/ L43	I/O, 1.2V/1.8V LVCMOS	NC. *Note: Optionally connected to Bank3A Clock input pin or from on board Ethernet PHY CLK125. Any one can be supported at a time.*
66	SDM_nCONFIG_B2B	nCONFIG / CC47	I, 1.8V LVCMOS/ 10K PU	This nCONFIG pin is used to clear the device and prepare for reconfiguration.
68	SDM_nSTATUS	NSTATUS/ CE47	O, 1.8V LVCMOS/ 10K PU	NC. *Note: Configuration status pin. This pin is used for synchronization with the configuration host driving nCONFIG and to report errors.*

B2B-2 Pin No	B2B Connector2 Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
70	nCATTRIP_1V8	nCATTRIP / CD45	O, 1.8V LVCMOS	NC. *Note: Connect this output pin to an external device that monitors the nCATTRIP event.*

2.8 Board to Board Connector3

The Altera Agilex 7 SoC and FPGA SOM Board to Board Connector3 pinout is provided in the below table and the interfaces which are available at Board-to-Board Connector3 are explained in the following sections. The Board-to-Board Connector3 (J5) is physically located on bottom side of the SOM as shown below.

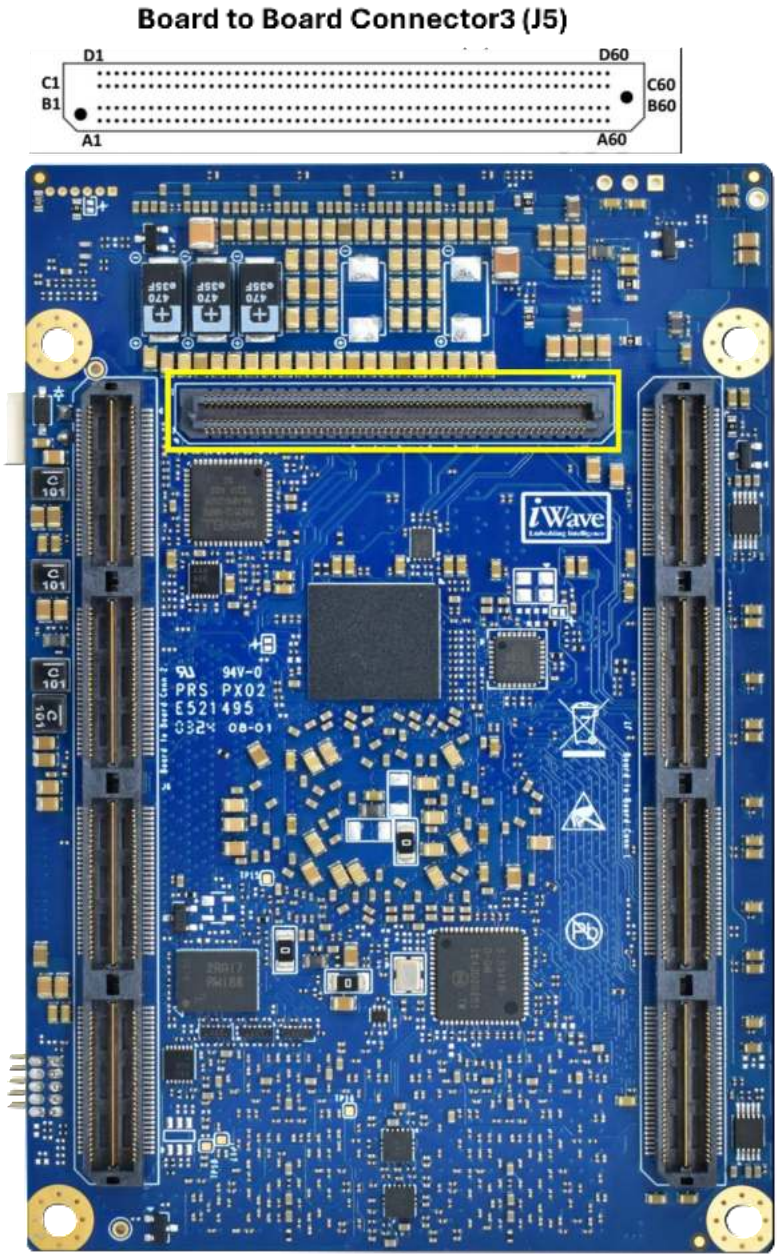

Figure 8: Board-to-Board Connector3

Number of Pins - 240

Connector Part Number - ADM6-60-01.5-L-4-2-A from Samtech

Mating Connector - ADF6-60-03.5-L-4-2-A from Samtech

Staking Height - 5mm

Table 12: Board to Board Connector3 Pinout

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
Row-A		Row-B	
A1	REFCLK_FGTL12A_Q2_CH8N	**B1**	GND
A2	REFCLK_FGTL12A_Q2_CH8P	**B2**	FGTL12A_RX_Q3_CH2N
A3	GND	**B3**	FGTL12A_RX_Q3_CH2P
A4	FGTL12A_RX_Q3_CH0N	**B4**	GND
A5	FGTL12A_RX_Q3_CH0P	**B5**	GND
A6	GND	**B6**	FGTL12A_RX_Q3_CH3N
A7	GND	**B7**	FGTL12A_RX_Q3_CH3P
A8	FGTL12A_RX_Q3_CH1N	**B8**	GND
A9	FGTL12A_RX_Q3_CH1P	**B9**	GND
A10	GND	**B10**	FGTL12A_TX_Q3_CH1N
A11	GND	**B11**	FGTL12A_TX_Q3_CH1P
A12	FGTL12A_TX_Q3_CH3N	**B12**	GND
A13	FGTL12A_TX_Q3_CH3P	**B13**	GND
A14	GND	**B14**	FGTL12A_TX_Q3_CH0N
A15	GND	**B15**	FGTL12A_TX_Q3_CH0P
A16	FGTL12A_TX_Q3_CH2N	**B16**	GND
A17	FGTL12A_TX_Q3_CH2P	**B17**	GND
A18	GND	**B18**	REFCLK_FGTL12A_Q3_RX_CH6N
A19	GND	**B19**	REFCLK_FGTL12A_Q3_RX_CH6P
A20	REFCLK_FGTL12A_Q3_RX_CH7N	**B20**	GND
A21	REFCLK_FGTL12A_Q3_RX_CH7P	**B21**	GND
A22	GND	**B22**	FGTL12A_RX_Q0_CH3N
A23	GND	**B23**	FGTL12A_RX_Q0_CH3P
A24	FGTL12A_RX_Q0_CH2N	**B24**	GND
A25	FGTL12A_RX_Q0_CH2P	**B25**	GND
A26	GND	**B26**	FGTL12A_TX_Q0_CH3P
A27	GND	**B27**	FGTL12A_TX_Q0_CH3N
A28	FGTL12A_TX_Q0_CH2P	**B28**	GND
A29	FGTL12A_TX_Q0_CH2N	**B29**	GND
A30	GND	**B30**	FGTL12A_TX_Q0_CH1P
A31	GND	**B31**	FGTL12A_TX_Q0_CH1N
A32	FGTL12A_TX_Q0_CH0P	**B32**	GND
A33	FGTL12A_TX_Q0_CH0N	**B33**	GND
A34	GND	**B34**	REFCLK_FGTL12A_Q0_RX_CH1P
A35	GND	**B35**	REFCLK_FGTL12A_Q0_RX_CH1N
A36	FGTL12A_RX_Q0_CH1P	**B36**	GND
A37	FGTL12A_RX_Q0_CH1N	**B37**	GND
A38	GND	**B38**	REFCLK_FGTL12A_Q0_RX_CH0P
A39	GND	**B39**	REFCLK_FGTL12A_Q0_RX_CH0N
A40	FGTL12A_RX_Q0_CH0P	**B40**	GND
A41	FGTL12A_RX_Q0_CH0N	**B41**	GND

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
A42	GND	**B42**	NC
A43	GND	**B43**	NC
A44	NC	**B44**	GND
A45	NC	**B45**	GND
A46	GND	**B46**	NC
A47	GND	**B47**	NC
A48	NC	**B48**	GND
A49	NC	**B49**	GND
A50	GND	**B50**	NC
A51	GND	**B51**	NC
A52	NC	**B52**	GND
A53	NC	**B53**	GND
A54	GND	**B54**	NC
A55	GND	**B55**	NC
A56	NC	**B56**	GND
A57	NC	**B57**	GND
A58	GND	**B58**	NC
A59	REFCLK_FGTL12A_Q3_CH9N	**B59**	NC
A60	REFCLK_FGTL12A_Q3_CH9P	**B60**	GND
Row-C		**Row-D**	
C1	NC	**D1**	GND
C2	GND	**D2**	NC
C3	GND	**D3**	NC
C4	FGTL12A_RX_Q1_CH2P	**D4**	GND
C5	FGTL12A_RX_Q1_CH2N	**D5**	GND
C6	GND	**D6**	NC
C7	GND	**D7**	NC
C8	FGTL12A_RX_Q1_CH0N	**D8**	GND
C9	FGTL12A_RX_Q1_CH0P	**D9**	GND
C10	GND	**D10**	NC
C11	GND	**D11**	NC
C12	FGTL12A_TX_Q1_CH1N	**D12**	GND
C13	FGTL12A_TX_Q1_CH1P	**D13**	GND
C14	GND	**D14**	NC
C15	GND	**D15**	NC
C16	REFCLK_FGTL12A_Q1_RX_CH3N	**D16**	GND
C17	REFCLK_FGTL12A_Q1_RX_CH3P	**D17**	GND
C18	GND	**D18**	NC
C19	GND	**D19**	NC
C20	REFCLK_FGTL12A_Q1_RX_CH2P	**D20**	GND
C21	REFCLK_FGTL12A_Q1_RX_CH2N	**D21**	GND
C22	GND	**D22**	NC
C23	GND	**D23**	NC

B2B3 Pin No	Signal Name	B2B3 Pin No	Signal Name
C24	FGTL12A_RX_Q1_CH3N	**D24**	GND
C25	FGTL12A_RX_Q1_CH3P	**D25**	GND
C26	GND	**D26**	NC
C27	GND	**D27**	NC
C28	FGTL12A_RX_Q1_CH1N	**D28**	GND
C29	FGTL12A_RX_Q1_CH1P	**D29**	GND
C30	GND	**D30**	NC
C31	GND	**D31**	NC
C32	FGTL12A_TX_Q1_CH3N	**D32**	GND
C33	FGTL12A_TX_Q1_CH3P	**D33**	GND
C34	GND	**D34**	NC
C35	GND	**D35**	NC
C36	FGTL12A_TX_Q1_CH2N	**D36**	GND
C37	FGTL12A_TX_Q1_CH2P	**D37**	GND
C38	GND	**D38**	REFCLK_FGTR13A_Q3_CH9N
C39	GND	**D39**	REFCLK_FGTR13A_Q3_CH9P
C40	FGTL12A_TX_Q1_CH0N	**D40**	GND
C41	FGTL12A_TX_Q1_CH0P	**D41**	GND
C42	GND	**D42**	FGTL12A_RX_Q2_CH1N
C43	GND	**D43**	FGTL12A_RX_Q2_CH1P
C44	FGTL12A_RX_Q2_CH2N	**D44**	GND
C45	FGTL12A_RX_Q2_CH2P	**D45**	GND
C46	GND	**D46**	FGTL12A_RX_Q2_CH3N
C47	GND	**D47**	FGTL12A_RX_Q2_CH3P
C48	REFCLK_FGTL12A_Q2_RX_CH4P	**D48**	GND
C49	REFCLK_FGTL12A_Q2_RX_CH4N	**D49**	GND
C50	GND	**D50**	FGTL12A_RX_Q2_CH0N
C51	GND	**D51**	FGTL12A_RX_Q2_CH0P
C52	FGTL12A_TX_Q2_CH0P	**D52**	GND
C53	FGTL12A_TX_Q2_CH0N	**D53**	GND
C54	GND	**D54**	FGTL12A_TX_Q2_CH2P
C55	GND	**D55**	FGTL12A_TX_Q2_CH2N
C56	FGTL12A_TX_Q2_CH1N	**D56**	GND
C57	FGTL12A_TX_Q2_CH1P	**D57**	GND
C58	GND	**D58**	FGTL12A_TX_Q2_CH3P
C59	GND	**D59**	FGTL12A_TX_Q2_CH3N
C60	NC	**D60**	GND

2.8.1 FPGA Interfaces

The interfaces which are supported in Board-to-Board Connector3 from Altera Agilex 7 SoC and FPGA device's FPGA is explained in the following section.

2.8.1.1 High Speed Transceivers

The Altera Agilex 7 SoC and FPGA SOM supports 16 high speed transceiver channels (16 Channels from FGT 12A Bank Quad [3:0] and Each quad supports 4 Transceiver channels) on Board-to-Board connector3. In Altera Agilex 7 SoC and FPGA SOM, the FGT Transceivers connected to Board-to-Board Connector3 is capable of running up to a maximum speed of 32Gbps in NRZ Format or 58Gbps in PAM4 Format. These transceivers can be used to interface to multiple high-speed interface protocols. Each 4 Channel Transceiver Bank supports two dedicated reference clock input pairs.

Note1: FGT Quad0 can only support 20-32 Gbps PAM4. FGT Quad1, Quad2, and Quad3 can ***support 20-58 Gbps PAM4***

Note2: Based on Device bank names will change. In this datasheet AGF 014 Device considered.

For more details on FGTL 12A transceiver pinouts on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
BANK-FGT12A Q0 Channels				
A32	FGTL12A_TX_Q0_CH0P	FGTL12A_TX_Q0_CH0p/ BW49	O, DIFF	Bank FGTL12A-Q0 channel0 High speed differential transmitter positive.
A33	FGTL12A_TX_Q0_CH0N	FGTL12A_TX_Q0_CH0n/ BY48	O, DIFF	Bank FGT12A-Q0 channel0 High speed differential transmitter negative.
B30	FGTL12A_TX_Q0_CH1P	FGTL12A_TX_Q0_CH1p/ BV52	O, DIFF	Bank FGTL12A-Q0 channel1 High speed differential transmitter positive.
B31	FGTL12A_TX_Q0_CH1N	FGTL12A_TX_Q0_CH1n/ BU51	O, DIFF	Bank FGT12A-Q0 channel1 High speed differential transmitter negative.
A28	FGTL12A_TX_Q0_CH2P	FGTL12A_TX_Q0_CH2p/ BR49	O, DIFF	Bank FGTL12A-Q0 channel2 High speed differential transmitter positive.
A29	FGTL12A_TX_Q0_CH2N	FGTL12A_TX_Q0_CH2n/ BT48	O, DIFF	Bank FGT12A-Q0 channel2 High speed differential transmitter negative.
B26	FGTL12A_TX_Q0_CH3P	FGTL12A_TX_Q0_CH3p/ BP52	O, DIFF	Bank FGTL12A-Q0 channel3 High speed differential transmitter positive.
B27	FGTL12A_TX_Q0_CH3N	FGTL12A_TX_Q0_CH3n/ BN51	O, DIFF	Bank FGT12A-Q0 channel3 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A40	FGTL12A_RX_Q0_CH0P	FGTL12A_RX_Q0_CH0p/ CC55	I, DIFF	Bank FGT12A-Q0 channel0 High speed differential receiver positive.
A41	FGTL12A_RX_Q0_CH0N	FGTL12A_RX_Q0_CH0n/ CD54	I, DIFF	Bank FGT13A-Q0 channel0 High speed differential receiver negative.
A36	FGTL12A_RX_Q0_CH1P	FGTL12A_RX_Q0_CH1p/ CB52	I, DIFF	Bank FGT12A-Q0 channel1 High speed differential receiver positive.
A37	FGTL12A_RX_Q0_CH1N	FGTL12A_RX_Q0_CH1n/ CA51	I, DIFF	Bank FGT13A-Q0 channel1 High speed differential receiver negative.
A24	FGTL12A_RX_Q0_CH2N	FGTL12A_RX_Q0_CH2n/ BY54	I, DIFF	Bank FGT13A-Q0 channel2 High speed differential receiver negative
A25	FGTL12A_RX_Q0_CH2P	FGTL12A_RX_Q0_CH2p/ BW55	I, DIFF	Bank FGT12A-Q0 channel2 High speed differential receiver positive.
B22	FGTL12A_RX_Q0_CH3N	FGTL12A_RX_Q0_CH3n/ BT54	I, DIFF	Bank FGT13A-Q0 channel3 High speed differential receiver negative.
B23	FGTL12A_RX_Q0_CH3P	FGTL12A_RX_Q0_CH3p/ BR55	I, DIFF	Bank FGT12A-Q0 channel3 High speed differential receiver positive
B38	REFCLK_FGTL12A_Q0_ RX_CH0P	REFCLK_FGTL12A_Q0_R X_CH0p/BC49	I, DIFF	Bank FGT12A-Q0 High speed differential Clock0 positive. Regional reference clock, this clock can be used for 12A Bank Q0 and Q1 Transceivers.
B39	REFCLK_FGTL12A_Q0_ RX_CH0N	REFCLK_FGTL12A_Q0_R X_CH0n/BE49	I, DIFF	Bank FGT12A-Q0 High speed differential Clock0 negative. Regional reference clock, this clock can be used for 12A Bank Q0 and Q1 Transceivers.
B34	REFCLK_FGTL12A_Q0_ RX_CH1P	REFCLK_FGTL12A_Q0_R X_CH1p/BG49	I, DIFF	Bank FGT12A-Q0 High speed differential Clock1 positive. Regional reference clock, this clock can be used for 12A Bank Q0 and Q1 Transceivers.
B35	REFCLK_FGTL12A_Q0_ RX_CH1N	REFCLK_FGTL12A_Q0_R X_CH1n/BF48	I, DIFF	Bank FGT12A-Q0 High speed differential Clock1 negative. Regional reference clock, this clock can be used for 12A Bank Q0 and Q1 Transceivers.
BANK-FGT12A Q1 Channels				
C40	FGTL12A_TX_Q1_CH0N	FGTL12A_TX_Q1_CH0n/ BM48	O, DIFF	Bank FGT12A-Q1 channel0 High speed differential transmitter negative.
C41	FGTL12A_TX_Q1_CH0P	FGTL12A_TX_Q1_CH0p/ BL49	O, DIFF	Bank FGTL12A-Q1 channel0 High speed differential transmitter positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C12	FGTL12A_TX_Q1_CH1N	FGTL12A_TX_Q1_CH1n/ BJ51	O, DIFF	Bank FGT12A-Q1 channel1 High speed differential transmitter negative.
C13	FGTL12A_TX_Q1_CH1P	FGTL12A_TX_Q1_CH1p/ BK52	O, DIFF	Bank FGTL12A-Q1 channel1 High speed differential transmitter positive.
C36	FGTL12A_TX_Q1_CH2N	FGTL12A_TX_Q1_CH2n/ BE51	O, DIFF	Bank FGT12A-Q1 channel2 High speed differential transmitter negative.
C37	FGTL12A_TX_Q1_CH2P	FGTL12A_TX_Q1_CH2p/ BF52	O, DIFF	Bank FGTL12A-Q1 channel1 High speed differential transmitter positive.
C32	FGTL12A_TX_Q1_CH3N	FGTL12A_TX_Q1_CH3n/ BA51	O, DIFF	Bank FGT12A-Q1 channel3 High speed differential transmitter negative.
C33	FGTL12A_TX_Q1_CH3P	FGTL12A_TX_Q1_CH3p/ BB52	O, DIFF	Bank FGTL12A-Q1 channel1 High speed differential transmitter positive.
C8	FGTL12A_RX_Q1_CH0N	FGTL12A_RX_Q1_CH0n/ BM54	I, DIFF	Bank FGT12A-Q1 channel0 High speed differential receiver negative.
C9	FGTL12A_RX_Q1_CH0P	FGTL12A_RX_Q1_CH0p/ BL55	I, DIFF	Bank FGTL12A-Q1 channel0 High speed differential receiver positive.
C28	FGTL12A_RX_Q1_CH1N	FGTL12A_RX_Q1_CH1n/ BH54	I, DIFF	Bank FGT12A-Q1 channel1 High speed differential receiver negative.
C29	FGTL12A_RX_Q1_CH1P	FGTL12A_RX_Q1_CH1p/ BG55	I, DIFF	Bank FGTL12A-Q1 channel1 High speed differential receiver positive.
C4	FGTL12A_RX_Q1_CH2P	FGTL12A_RX_Q1_CH2n/ BD54	I, DIFF	Bank FGT12A-Q1 channel2 High speed differential receiver negative.
C5	FGTL12A_RX_Q1_CH2N	FGTL12A_RX_Q1_CH2p/ BC55	I, DIFF	Bank FGTL12A-Q1 channel1 High speed differential receiver positive.
C24	FGTL12A_RX_Q1_CH3N	FGTL12A_RX_Q1_CH3n/ AY54	I, DIFF	Bank FGT12A-Q1 channel3 High speed differential receiver negative.
C25	FGTL12A_RX_Q1_CH3P	FGTL12A_RX_Q1_CH3p/ AW55	I, DIFF	Bank FGTL12A-Q1 channel1 High speed differential receiver positive.
C20	REFCLK_FGTL12A_Q1_ RX_CH2P	REFCLK_FGTL12A_Q1_R X_CH2p/AW49	I, DIFF	Bank FGT12A-Q1 High speed differential Clock2 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.
C21	REFCLK_FGTL12A_Q1_ RX_CH2N	REFCLK_FGTL12A_Q1_R X_CH2n/AV48	I, DIFF	Bank FGT12A-Q1 High speed differential Clock2 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C16	REFCLK_FGTL12A_Q1_RX_CH3N	REFCLK_FGTL12A_Q1_RX_CH3n/AU49	I, DIFF	Bank FGT12A-Q1 High speed differential Clock3 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.
C17	REFCLK_FGTL12A_Q1_RX_CH3P	REFCLK_FGTL12A_Q1_RX_CH3p/AR49	I, DIFF	Bank FGT12A-Q1 High speed differential Clock3 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.
BANK-FGT12A Q2 Channels				
C52	FGTL12A_TX_Q2_CH0P	FGTL12A_TX_Q2_CH0p/AV52	O, DIFF	Bank FGTL12A-Q2 channel0 High speed differential transmitter positive.
C53	FGTL12A_TX_Q2_CH0N	FGTL12A_TX_Q2_CH0n/AU51	O, DIFF	Bank FGT12A-Q2 channel0 High speed differential transmitter negative.
C56	FGTL12A_TX_Q2_CH1N	FGTL12A_TX_Q2_CH1n/AN51	O, DIFF	Bank FGT12A-Q2 channel1 High speed differential transmitter negative.
C57	FGTL12A_TX_Q2_CH1P	FGTL12A_TX_Q2_CH1p/AP52	O, DIFF	Bank FGTL12A-Q2 channel1 High speed differential transmitter positive.
D54	FGTL12A_TX_Q2_CH2P	FGTL12A_TX_Q2_CH2p/AK52	O, DIFF	Bank FGTL12A-Q2 channel2 High speed differential transmitter positive.
D55	FGTL12A_TX_Q2_CH2N	FGTL12A_TX_Q2_CH2n/AJ51	O, DIFF	Bank FGT12A-Q2 channel2 High speed differential transmitter negative.
D58	FGTL12A_TX_Q2_CH3P	FGTL12A_TX_Q2_CH3p/AF52	O, DIFF	Bank FGTL12A-Q2 channel3 High speed differential transmitter positive.
D59	FGTL12A_TX_Q2_CH3N	FGTL12A_TX_Q2_CH3n/AE51	O, DIFF	Bank FGT12A-Q2 channel3 High speed differential transmitter negative.
D50	FGTL12A_RX_Q2_CH0N	FGTL12A_RX_Q2_CH0n/AT54	I, DIFF	Bank FGT13A-Q2 channel0 High speed differential receiver negative.
D51	FGTL12A_RX_Q2_CH0P	FGTL12A_RX_Q2_CH0p/AR55	I, DIFF	Bank FGT12A-Q2 channel0 High speed differential receiver positive.
D42	FGTL12A_RX_Q2_CH1N	FGTL12A_RX_Q2_CH1n/AM54	I, DIFF	Bank FGT13A-Q2 channel1 High speed differential receiver negative.
D43	FGTL12A_RX_Q2_CH1P	FGTL12A_RX_Q2_CH1p/AL55	I, DIFF	Bank FGT12A-Q2 channel1 High speed differential receiver positive.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
C44	FGTL12A_RX_Q2_CH2N	FGTL12A_RX_Q2_CH2n/ AH54	I, DIFF	Bank FGT13A-Q2 channel2 High speed differential receiver negative
C45	FGTL12A_RX_Q2_CH2P	FGTL12A_RX_Q2_CH2p/ AG55	I, DIFF	Bank FGT12A-Q2 channel2 High speed differential receiver positive.
D46	FGTL12A_RX_Q2_CH3N	FGTL12A_RX_Q2_CH3n/ AD54	I, DIFF	Bank FGT13A-Q2 channel3 High speed differential receiver negative.
D47	FGTL12A_RX_Q2_CH3P	FGTL12A_RX_Q2_CH3p/ AC55	I, DIFF	Bank FGT12A-Q2 channel3 High speed differential receiver positive
C48	REFCLK_FGTL12A_Q2_ RX_CH4P	REFCLK_FGTL12A_Q2_R X_CH4p/AN49	I, DIFF	Bank FGT12A-Q2 High speed differential Clock4 positive. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.
C49	REFCLK_FGTL12A_Q2_ RX_CH4N	REFCLK_FGTL12A_Q2_R X_CH4n/AP48	I, DIFF	Bank FGT12A-Q2 High speed differential Clock4 negative. Global reference clock, this clock can be used for 12A Bank Q0, Q1, Q2 & Q3 Transceivers.
A1	REFCLK_FGTL12A_Q2_ CH8N	REFCLK_FGTL12A_Q2_C H8n/AE49	IO, DIFF	Bank FGT12A-Q2 High speed differential Clock8 positive. Local In/out reference clock, this clock can be used for 12A Bank Q2 Transceivers.
A2	REFCLK_FGTL12A_Q2_ CH8P	REFCLK_FGTL12A_Q2_C H8p/AG49	IO, DIFF	Bank FGT12A-Q2 High speed differential Clock8 negative. Local In/out reference clock, this clock can be used for 12A Bank Q2 Transceivers.
BANK-FGT12A Q3 Channels				
B14	FGTL12A_TX_Q3_CH0N	FGTL12A_TX_Q3_CH0n/ AA51	O, DIFF	Bank FGT12A-Q3 channel0 High speed differential transmitter negative.
B15	FGTL12A_TX_Q3_CH0P	FGTL12A_TX_Q3_CH0p/ AB52	O, DIFF	Bank FGTL12A-Q3 channel0 High speed differential transmitter positive.
B10	FGTL12A_TX_Q3_CH1N	FGTL12A_TX_Q3_CH1n/ Y48	O, DIFF	Bank FGT12A-Q3 channel1 High speed differential transmitter negative.
B11	FGTL12A_TX_Q3_CH1P	FGTL12A_TX_Q3_CH1p/ W49	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential transmitter positive.
A16	FGTL12A_TX_Q3_CH2N	FGTL12A_TX_Q3_CH2n/ U51	O, DIFF	Bank FGT12A-Q3 channel2 High speed differential transmitter negative.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A17	FGTL12A_TX_Q3_CH2P	FGTL12A_TX_Q3_CH2p/ V52	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential transmitter positive.
A12	FGTL12A_TX_Q3_CH3N	FGTL12A_TX_Q3_CH3n/ T48	O, DIFF	Bank FGT12A-Q3 channel3 High speed differential transmitter negative.
A13	FGTL12A_TX_Q3_CH3P	FGTL12A_TX_Q3_CH3p/ R49	O, DIFF	Bank FGTL12A-Q3 channel1 High speed differential transmitter positive.
A4	FGTL12A_RX_Q3_CH0N	FGTL12A_RX_Q3_CH0n/ Y54	I, DIFF	Bank FGT12A-Q3 channel0 High speed differential receiver negative.
A5	FGTL12A_RX_Q3_CH0P	FGTL12A_RX_Q3_CH0p/ W55	I, DIFF	Bank FGTL12A-Q3 channel0 High speed differential receiver positive.
A8	FGTL12A_RX_Q3_CH1N	FGTL12A_RX_Q3_CH1n/ T54	I, DIFF	Bank FGT12A-Q3 channel1 High speed differential receiver negative.
A9	FGTL12A_RX_Q3_CH1P	FGTL12A_RX_Q3_CH1p/ R55	I, DIFF	Bank FGTL12A-Q3 channel1 High speed differential receiver positive.
B2	FGTL12A_RX_Q3_CH2N	FGTL12A_RX_Q3_CH2n/ N51	I, DIFF	Bank FGT12A-Q3 channel2 High speed differential receiver negative.
B3	FGTL12A_RX_Q3_CH2P	FGTL12A_RX_Q3_CH2p/ P52	I, DIFF	Bank FGTL12A-Q3 channel1 High speed differential receiver positive.
B6	FGTL12A_RX_Q3_CH3N	FGTL12A_RX_Q3_CH3n/ J51	I, DIFF	Bank FGT12A-Q3 channel3 High speed differential receiver negative.
B7	FGTL12A_RX_Q3_CH3P	FGTL12A_RX_Q3_CH3p/ K52	I, DIFF	Bank FGTL12A-Q3 channel1 High speed differential receiver positive.
B18	REFCLK_FGTL12A_Q3_ RX_CH6N	REFCLK_FGTL12A_Q3_R X_CH6n/AC49	I, DIFF	Bank FGT12A-Q3 High speed differential Clock6 negative. Regional reference clock, this clock can be used for 12A Bank Q2 & Q3 Transceivers.
B19	REFCLK_FGTL12A_Q3_ RX_CH6P	REFCLK_FGTL12A_Q3_R X_CH6p/AD48	I, DIFF	Bank FGT12A-Q3 High speed differential Clock6 positive. Regional reference clock, this clock can be used for 12A Bank Q2 & Q3 Transceivers.
A20	REFCLK_FGTL12A_Q3_ RX_CH7N	REFCLK_FGTL12A_Q3_R X_CH7N/Y46	I, DIFF	Bank FGT12A-Q3 High speed differential Clock7 negative. Regional reference clock, this clock can be used for 12A Bank Q2 & Q3 Transceivers.

B2B-3 Pin No	B2B Connector3 Pin Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
A21	REFCLK_FGTL12A_Q3_RX_CH7P	REFCLK_FGTL12A_Q3_RX_CH7P/AB46	I, DIFF	Bank FGT12A-Q3 High speed differential Clock7 positive. Regional reference clock, this clock can be used for 12A Bank Q2 & Q3 Transceivers.
A59	REFCLK_FGTL12A_Q3_CH9N	REFCLK_FGTL12A_Q3_CH9n/V46	IO, DIFF	Bank FGT12A-Q3 High speed differential Clock3 negative. Local In/Out reference clock, this clock can be used for 12A Bank Q3 Transceivers.
A60	REFCLK_FGTL12A_Q3_CH9P	REFCLK_FGTL12A_Q3_CH9p/W45	IO, DIFF	Bank FGT12A-Q3 High speed differential Clock3 positive. Local In/Out reference clock, this clock can be used for 12A Bank Q3 Transceivers.

2.8.2 Power, Control & Miscellaneous Signals

The Altera Agilex 7 SoC and FPGA SOM works with 5V power input (VCC) from Board-to-Board Connector2 and generates all other required powers internally On-SOM itself. Also, in Board-to-Board Connector3, Ground pins are distributed throughout the connector for better performance.

For more details on Power pins on Board-to-Board Connector3, refer the below table.

B2B-3 Pin No	B2B Connector3 Signal Name	Pin Name	Signal Type/ Termination	Description
A3, A6, A7, A10, A11, A14, A15, A18, A19, A22, A23, A26, A27, A30, A31, A34, A35, A38, A39, A42, A43, A46, A47, A50, A51, A54, A55, A58, B1, B4, B5, B8, B9, B12, B13, B16, B17, B20, B21, B24, B25, B28, B29, B32, B33, B36, B37, B40, B41, B44, B45, B48, B49, B52, B53, B56, B57, B60, C2, C3, C6, C7, C10, C11, C14, C15, C18, C19, C22, C23, C26, C27, C30, C31, C34, C35, C38, C39, C42, C43, C46, C47, C50, C51, C54, C55, C58, C59, D1, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, D24, D25, D28, D29, D32, D33, D36, D37, D40, D41, D44, D45, D48, D49, D52, D53, D56, D57, D60,	GND	NA	Power	Ground.

2.9 Altera Agilex 7 SoC and FPGA HPS Pin Multiplexing

The Altera Agilex 7 SoC and FPGA HPS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also, most of Altera Agilex 7 SoC HPS IO pins can be configured as GPIOs if required. The below table provides the details of HPS pin connections on Altera Agilex 7 SoC and FPGA with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring HPS I/O configuration in Quartus Tool. To know the complete available alternate functions, refer the HPS I/O configuration in the latest Quartus Tool

Table 13: HPS IOMUX on Altera Agilex 7 SoC and FPGA SOM

Interface/ Function	B2B Connector Pin Number	Altera Agilex 7 SoC & FPGA Pin Name	GPIO	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8
On SOM Features from Altera Agilex 7 SoC HPS												
eMMC FLASH	NA	HPS_IOB_13	GPIO1_IO12	EMAC2_TX_CLK	SDMMC_DATA0	Trace_D10	NAND_ALE	I2C1_SDA				GPIO1_IO12
	NA	HPS_IOB_14	GPIO1_IO13	EMAC2_TX_CTL	SDMMC_CMD	Trace_D9	NAND_RB	I2C1_SCL				GPIO1_IO13
	NA	HPS_IOB_15	GPIO1_IO14	EMAC2_RX_CLK	SDMMC_CCLK	Trace_D8	NAND_CE_N		UART1_TX			GPIO1_IO14
	NA	HPS_IOB_16	GPIO1_IO15	EMAC2_RX_CTL	SDMMC_DATA1	Trace_D7			UART1_RX			GPIO1_IO15
	NA	HPS_IOB_17	GPIO1_IO16	EMAC2_TXD0	SDMMC_DATA2	Trace_D6	NAND_ADQ8		UART1_CTS_N			GPIO1_IO16
	NA	HPS_IOB_18	GPIO1_IO17	EMAC2_TXD1	SDMMC_DATA3	Trace_D5	NAND_ADQ9		UART1_RTS_N		SPIM0_SS1_N	GPIO1_IO17
	NA	HPS_IOB_19	GPIO1_IO18	EMAC2_RXD0	SDMMC_DATA4	Trace_D4	NAND_ADQ10	I2C_EMAC1_SDA	MDIO1_MDIO		SPIM0_MISO	GPIO1_IO18
	NA	HPS_IOB_20	GPIO1_IO19	EMAC2_RXD1	SDMMC_DATA5	Trace_CLK	NAND_ADQ11	I2C_EMAC1_SCL	MDIO1_MDC		SPIM0_SS0_N	GPIO1_IO19
	NA	HPS_IOB_21	GPIO1_IO20	EMAC2_TXD2	SDMMC_DATA6	Trace_D0	NAND_ADQ12	I2C_EMAC2_SDA		SPIS1_CLK	SPIM0_CLK	GPIO1_IO20
	NA	HPS_IOB_22	GPIO1_IO21	EMAC2_TXD3	SDMMC_DATA7	Trace_D1	NAND_ADQ13	I2C_EMAC2_SCL		SPIS1_MOSI	SPIM0_MOSI	GPIO1_IO21
	NA	HPS_IOB_23	GPIO1_IO22	EMAC2_RXD2	SDMMC_PWR_EN	Trace_D2	NAND_ADQ14	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS1_SS0_N	SPIM0_MISO	GPIO1_IO22
ENET	NA	HPS_IOB_1	GPIO1_IO0	EMAC1_TX_CLK		Trace_D10	NAND_ADQ0		UART0_CTS_N		SPIM1_CLK	GPIO1_IO0
	NA	HPS_IOB_2	GPIO1_IO1	EMAC1_TX_CTL		Trace_D9	NAND_ADQ1		UART0_RTS_N		SPIM1_MOSI	GPIO1_IO1
	NA	HPS_IOB_3	GPIO1_IO2	EMAC1_RX_CLK		Trace_D8	NAND_WE_N	I2C0_SDA	UART0_TX		SPIM1_MISO	GPIO1_IO2
	NA	HPS_IOB_4	GPIO1_IO3	EMAC1_RX_CTL		Trace_D7	NAND_RE_N	I2C0_SCL	UART0_RX		SPIM1_SS0_N	GPIO1_IO3
	NA	HPS_IOB_5	GPIO1_IO4	EMAC1_TXD0		Trace_D6	NAND_WP_N		UART1_CTS_N	SPIS1_CLK	SPIM1_SS1_N	GPIO1_IO4
	NA	HPS_IOB_6	GPIO1_IO5	EMAC1_TXD1		Trace_D5	NAND_ADQ2		UART1_RTS_N	SPIS1_MOSI		GPIO1_IO5
	NA	HPS_IOB_7	GPIO1_IO6	EMAC1_RXD0		Trace_D4	NAND_ADQ3	I2C1_SDA	UART1_TX	SPIS1_SS0_N		GPIO1_IO6
	NA	HPS_IOB_8	GPIO1_IO7	EMAC1_RXD1		Trace_D15	NAND_CLE	I2C1_SCL	UART1_RX	SPIS1_MISO		GPIO1_IO7
	NA	HPS_IOB_9	GPIO1_IO8	EMAC1_TXD2		Trace_D14	NAND_ADQ4	I2C_EMAC2_SDA	MDIO2_MDIO	SPIS0_CLK	JTAG_TCK	GPIO1_IO8
	NA	HPS_IOB_10	GPIO1_IO9	EMAC1_TXD3		Trace_D13	NAND_ADQ5	I2C_EMAC2_SCL	MDIO2_MDC	SPIS0_MOSI	JTAG_TMS	GPIO1_IO9
	NA	HPS_IOB_11	GPIO1_IO10	EMAC1_RXD2		Trace_D12	NAND_ADQ6	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS0_SS0_N	JTAG_TDO	GPIO1_IO10
	NA	HPS_IOB_12	GPIO1_IO11	EMAC1_RXD3		Trace_D11	NAND_ADQ7	I2C_EMAC0_SCL	MDIO0_MDC	SPIS0_MISO	JTAG_TDI	GPIO1_IO11
	NA	HPS_IOA_9	GPIO0_IO8	SDMMC_DATA6	USB0_DATA4	Trace_D14	NAND_ADQ4	I2C_EMAC1_SDA	MDIO1_MDIO	SPIS1_CLK	SPIM1_CLK	GPIO0_IO8
	NA	HPS_IOA_10	GPIO0_IO9	SDMMC_DATA7	USB0_DATA5	Trace_D13	NAND_ADQ5	I2C_EMAC1_SCL	MDIO1_MDC	SPIS1_MOSI	SPIM1_MOSI	GPIO0_IO9
	NA	HPS_IOA_12	GPIO0_IO11		USB0_DATA7	Trace_D11	NAND_ADQ7	I2C_EMAC0_SCL	MDIO0_MDC	SPIS1_MISO	SPIM1_SS0_N	GPIO0_IO11
USB2.0	NA	HPS_IOA_13	GPIO0_IO12	EMAC0_TX_CLK	USB1_CLK	Trace_D10	NAND_ALE					GPIO0_IO12
	NA	HPS_IOA_14	GPIO0_IO13	EMAC0_TX_CTL	USB1_STP	Trace_D9	NAND_RB					GPIO0_IO13
	NA	HPS_IOA_15	GPIO0_IO14	EMAC0_RX_CLK	USB1_DIR	Trace_D8	NAND_CE_N					GPIO0_IO14
	NA	HPS_IOA_16	GPIO0_IO15	EMAC0_RX_CTL	USB1_DATA0	Trace_D7						GPIO0_IO15
	NA	HPS_IOA_17	GPIO0_IO16	EMAC0_TXD0	USB1_DATA1	Trace_D6	NAND_ADQ8					GPIO0_IO16
	NA	HPS_IOA_18	GPIO0_IO17	EMAC0_TXD1	USB1_NXT	Trace_D5	NAND_ADQ9					GPIO0_IO17
	NA	HPS_IOA_19	GPIO0_IO18	EMAC0_RXD0	USB1_DATA2	Trace_D4	NAND_ADQ10					GPIO0_IO18
	NA	HPS_IOA_20	GPIO0_IO19	EMAC0_RXD1	USB1_DATA3	Trace_CLK	NAND_ADQ11				SPIM1_SS1_N	GPIO0_IO19
	NA	HPS_IOA_21	GPIO0_IO20	EMAC0_TXD2	USB1_DATA4	Trace_D0	NAND_ADQ12	I2C1_SDA	UART0_CTS_N	SPIS0_CLK	SPIM1_CLK	GPIO0_IO20
	NA	HPS_IOA_22	GPIO0_IO21	EMAC0_TXD3	USB1_DATA5	Trace_D1	NAND_ADQ13	I2C1_SCL	UART0_RTS_N	SPIS0_MOSI	SPIM1_MOSI	GPIO0_IO21
	NA	HPS_IOA_23	GPIO0_IO22	EMAC0_RXD2	USB1_DATA6	Trace_D2	NAND_ADQ14	I2C0_SDA	UART0_TX	SPIS0_SS0_N	SPIM1_MISO	GPIO0_IO22
	NA	HPS_IOA_24	GPIO0_IO23	EMAC0_RXD3	USB1_DATA7	Trace_D3	NAND_ADQ15	I2C0_SCL	UART0_RX	SPIS0_MISO	SPIM1_SS0_N	GPIO0_IO23
	NA	HPS_IOA_11	GPIO0_IO10	SDMMC_PWR_EN	USB0_DATA6	Trace_D12	NAND_ADQ6	I2C_EMAC0_SDA	MDIO0_MDIO	SPIS1_SS0_N	SPIM1_MISO	GPIO0_IO10

Board-to-Board Connector2 Features from HPS												
UART0	B29	HPS_IOA_1	GPIO0_IO0	SDMMC_CCLK	USB0_CLK	Trace_D10	NAND_ADQ0		UART0_CTS_N	SPIS0_CLK	SPIM0_SS1_N	GPIO0_IO0
	B30	HPS_IOA_2	GPIO0_IO1	SDMMC_CMD	USB0_STP	Trace_D9	NAND_ADQ1		UART0_RTS_N	SPIS0_MOSI	SPIM1_SS1_N	GPIO0_IO1
	B27	HPS_IOA_3	GPIO0_IO2	SDMMC_DATA0	USB0_DIR	Trace_D8	NAND_WE_N	I2C1_SDA	UART0_TX	SPIS0_SS0_N		GPIO0_IO2
	B28	HPS_IOA_4	GPIO0_IO3	SDMMC_DATA1	USB0_DATA0	Trace_D7	NAND_RE_N	I2C1_SCL	UART0_RX	SPIS0_MISO		GPIO0_IO3
I2C	A27	HPS_IOA_5	GPIO0_IO4	SDMMC_DATA2	USB0_DATA1	Trace_D6	NAND_WP_N	I2C0_SDA	UART1_CTS_N		SPIM0_CLK	GPIO0_IO4
	A26	HPS_IOA_6	GPIO0_IO5	SDMMC_DATA3	USB0_NXT	Trace_D5	NAND_ADQ2	I2C0_SCL	UART1_RTS_N		SPIM0_MOSI	GPIO0_IO5
Debug UART	A30	HPS_IOB_7	GPIO0_IO6	SDMMC_DATA4	USB0_DATA2	Trace_D4	NAND_ADQ3	I2C_EMAC2_SDA	UART1_TX	MDIO2_MDIO	SPIM0_MISO	GPIO0_IO6
	A31	HPS_IOB_8	GPIO0_IO7	SDMMC_DATA5	USB0_DATA3	Trace_D15	NAND_CLE	I2C_EMAC2_SCL	UART1_RX	MDIO2_MDC	SPIM0_SS0_N	GPIO0_IO7

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Altera Agilex 7 SoC and FPGA SOM technical specifications with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Altera Agilex 7 SoC and FPGA SOM.

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75	5V	5.25V	±50mV
2	VRTC_1V8	0V	1.8V	1.8V	±20mV

[1] Altera Agilex 7 SoC and FPGA *SOM is designed to work with VCC_5V input power rail from Board-to-Board Connector2.*

3.1.2 Power Input Sequencing

The Altera Agilex 7 SoC and FPGA SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_1V8 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board-to-Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board-to-Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_1V8 goes down.

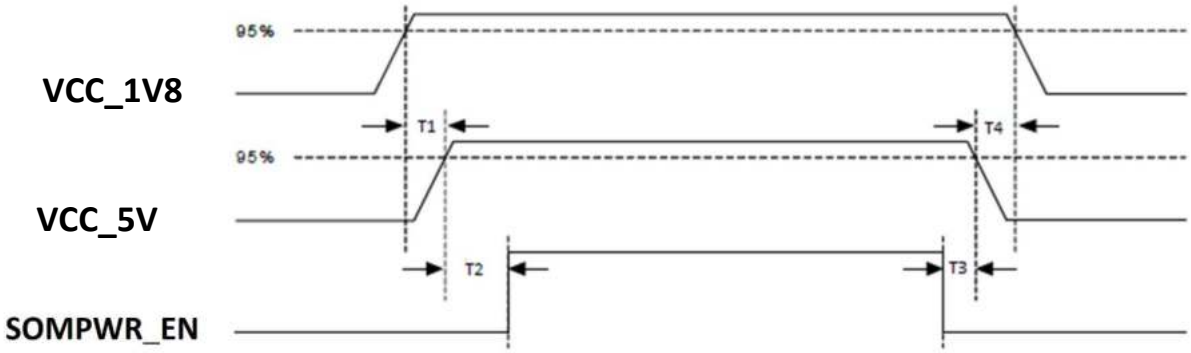

Figure 9: Power Input Sequencing

Table 15: Power Sequence Timing

Item	Description	Value
T1	VRTC_1V8[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_1V8 fall time	≥ 0 ms

[1] VRTC_1V8 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_5V input power to other all the powers are getting stable around 100ms in SOM, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

Table 16: Power Consumption

TBD.

For more accurate power estimation, iWave recommends using Altera Power Estimator (IPE) tool and calculate the SoC and FPGA power. Also add extra power for other On-SOM peripherals power.

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Altera Agilex 7 SoC and FPGA SOM.

Table 17: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS3 Compliance

iWave's Altera Agilex 7 SoC and FPGA SOM is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Altera Agilex 7 SoC and FPGA SOM is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the FPGA.

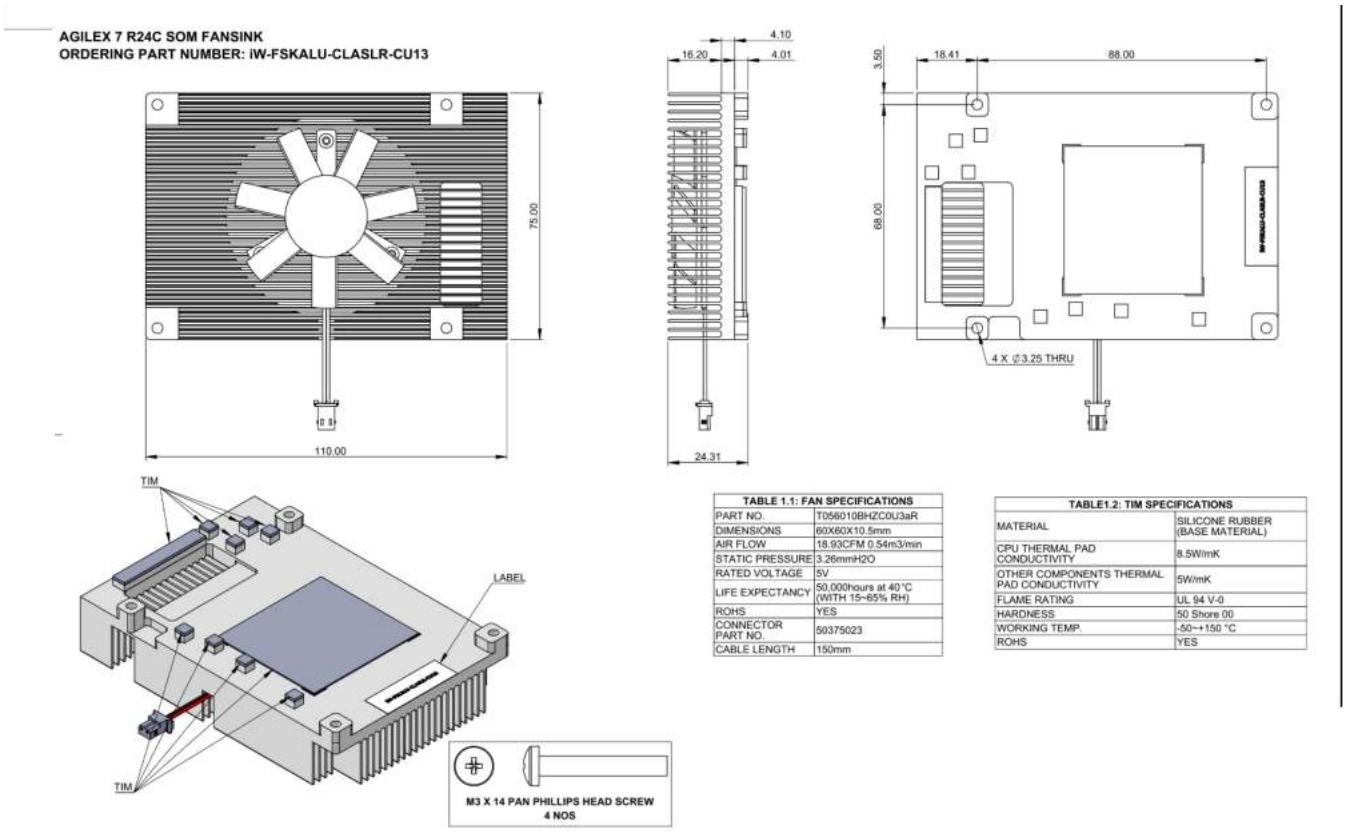

TABLE 1.1: FAN SPECIFICATIONS	
PART NO.	T056010BHZC0U3aR
DIMENSIONS	60X60X10.5mm
AIR FLOW	18.93CFM 0.54m3/min
STATIC PRESSURE	3.26mmH2O
RATED VOLTAGE	5V
LIFE EXPECTANCY	50,000hours at 40°C (WITH 15~65% RH)
ROHS	YES
CONNECTOR PART NO.	50375023
CABLE LENGTH	150mm

TABLE1.2: TIM SPECIFICATIONS	
MATERIAL	SILICONE RUBBER (BASE MATERIAL)
CPU THERMAL PAD CONDUCTIVITY	8.5W/mK
OTHER COMPONENTS THERMAL PAD CONDUCTIVITY	5W/mK
FLAME RATING	UL 94 V-0
HARDNESS	50 Shore 00
WORKING TEMP.	-50~+150 °C
ROHS	YES

Figure 10: Heat Sink

3.3 Mechanical Characteristics

3.3.1 Altera Agilex 7 SoC and FPGA SOM Mechanical Dimensions

Altera Agilex 7 SoC and FPGA SOM PCB size is 110mm x 75mm x 2.05mm and weight is 130gm. SOM mechanical dimension is shown below.

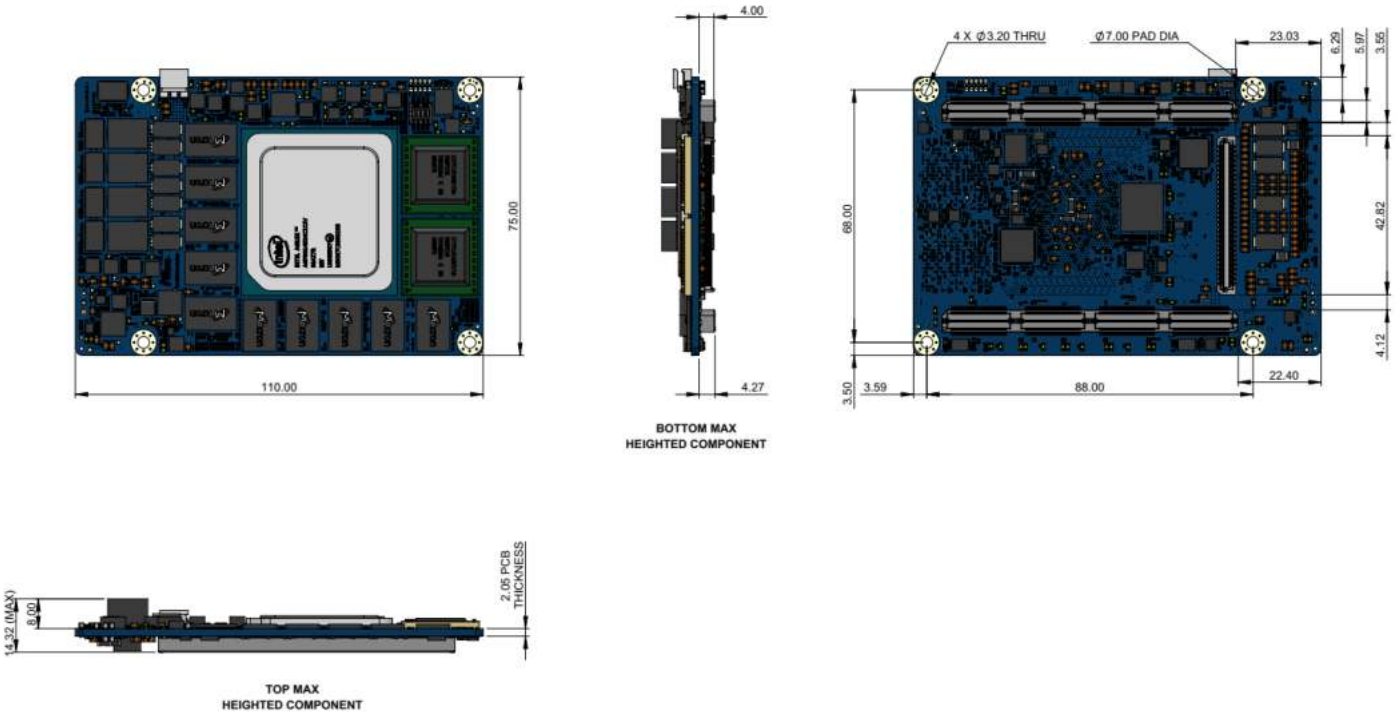

Figure 11: Mechanical dimension of Altera Agilex 7 SoC and FPGA SOM

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Altera Agilex 7 SoC and FPGA SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 18: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G51M - AGFB014 R24C Agilex 7 SOC SOM		
iW-G51M-FB14-4E008G-E032G-BIC	AGFB014R24C2I2V Agilex 7 R24C SOC SOM with 8GB HPS DDR4 with ECC, 8GB FPGA DDR4 with ECC, Dual 144Mb FPGA QDR-IV, 32GB eMMC SOM, Industrial	Industrial
iW-G51M-FB14-4E008G-E032G-BID	AGFB014R24C2I2V Agilex 7 R24C SOC SOM with 8GB HPS DDR4 with ECC, 8GB FPGA DDR4 with ECC, 32GB eMMC SOM, Industrial (No FPGA QDR-IV support)	Industrial
iW-Rainbow G51M - AGFB027 R24C Agilex 7 SOC SOM		
iW-G51M-FB27-4E008G-E032G-BIC	AGFB027R24C2I2V Agilex 7 R24C SOC SOM with 8GB HPS DDR4 with ECC, 8GB FPGA DDR4 with ECC, Dual 144Mb FPGA QDR-IV, 32GB eMMC SOM, Industrial	Industrial
iW-G51M-FB27-4E008G-E032G-BID	AGFB027R24C2I2V Agilex 7 R24C SOC SOM with 8GB HPS DDR4 with ECC, 8GB FPGA DDR4 with ECC, 32GB eMMC SOM, Industrial (No FPGA QDR-IV support)	Industrial
iW-Rainbow G51M - AGFB006 R24D Agilex 7 SOC SOM		
iW-G51M-FB06-4E008G-E032G-BID	AGFB006R24D2I2V Agilex 7 R24C SOC SOM with 8GB HPS DDR4 with ECC, 32GB eMMC SOM, Industrial (No FPGA QDR-IV support)	Industrial

5. APPENDIX

5.1 Altera Agilex 7 SoC and FPGA SOM Development Platform

iWave supports iW-RainboW-G51D – Altera Agilex 7 SoC and FPGA SOM Development Platform which is targeted for quick validation of Altera Agilex 7 SoC and FPGA based SOM. iWave's Altera Agilex 7 SoC and FPGA Development Board incorporates Altera Agilex 7 SoC and FPGA SOM and High-performance Carrier board with complete BSP support.

For more details on Altera Agilex 7 SoC and FPGA SOM Development Platform, visit the below web link:

Link: *https://www.iwavesystems.com/product/Agilex 7-R24C-R24C-soc-fpga-som/*

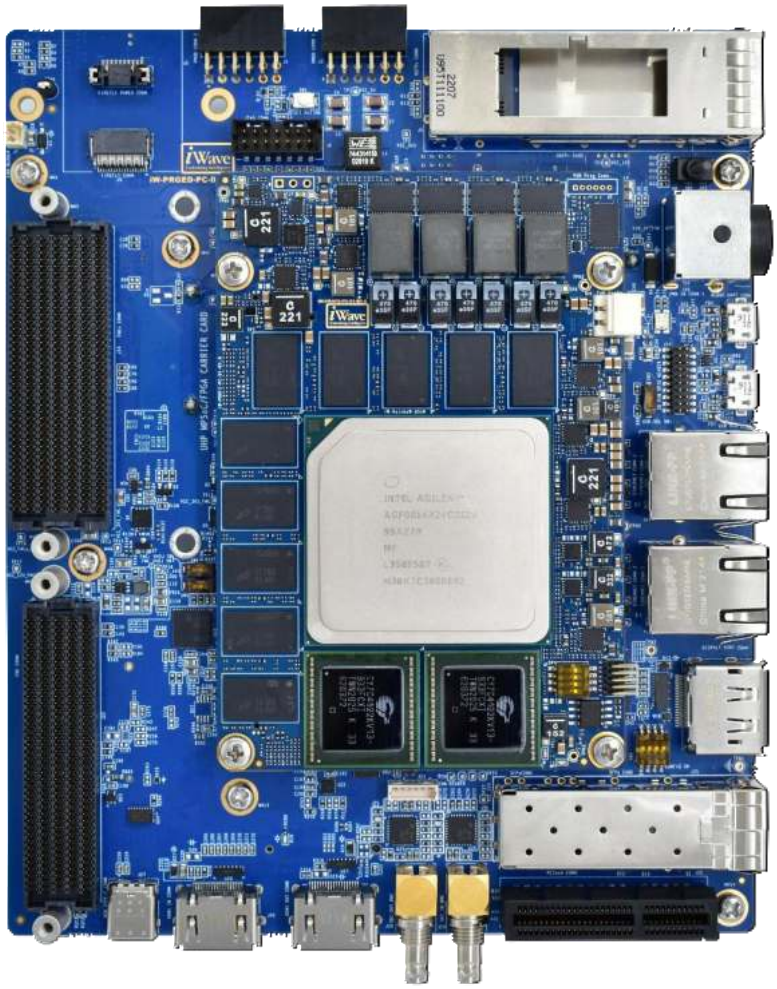

Figure 12: Altera Agilex 7 SoC and FPGA SOM Development Platform

A Global Leader in Embedded Systems Engineering and Solutions

Since 1999, we have pioneered leadership in embedded systems technology, establishing ourselves as a strategic embedded technology partner for advanced solutions. Our comprehensive portfolio encompasses ARM and FPGA System on Modules, COTS FPGA solutions, and ODM solutions which include Telematics, Gateways & HMI Solutions.

Beyond our robust product ecosystem, we provide comprehensive ODM support with specialized custom design and manufacturing capabilities, enabling customers to accelerate and optimize their product development roadmaps. With a strategic focus on industrial, automotive, medical, and avionics markets, we deliver innovative technology solutions to global clients.

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