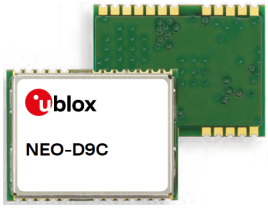
NEO-D9C-00B

QZSS correction service receiver
Professional grade
Data sheet



Abstract

This data sheet describes the NEO-D9C QZSS L6 receiver for CLAS and MADOCA. This NEO form factor module provides easy integration of QZSS augmentation services and enables GNSS receivers to reach cm-level accuracies.

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Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	FW version	IN/PCN reference	Product status
NEO-D9C	NEO-D9C-00B-02	QZS 1.01	UBX-22003112 UBX-22039049 UBX-23000084	Mass production

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1 Functional description

1.1 Overview

NEO-D9C-00B is a QZSS L6 receiver that brings QZSS Centimeter Level Augmentation Service (CLAS) support to u-blox GNSS products, enabling centimeter-level navigation. The receiver can also track the experimental MADOCA service transmitted on the QZSS L6 signal.

When combined with other u-blox products, the NEO-D9C-00B can be used to build a complete and stand-alone high precision system providing users with access to free high accuracy correction services and ultimately centimeter-level GNSS accuracy.

1.2 Performance

Parameter	Specification
Receiver type	u-blox D9 engine QZSS L2C and L6 receiver

QZSS L2C and L6		Specification
Time to first frame [1]		Hot start 3 s, Cold start 18 s
Decoding sensitivity [2]		90% frame rate at -136 dBm
Acquisition sensitivity [3]		Hot start: -154 dBm, Cold start: -137 dBm
Specification compliance		PS-QZSS-001
Number of concurrent L6 reception channels		2
Frequency range		1227.60 MHz +/- 5 MHz and 1278.75 MHz +/- 5 MHz
Communication interface		UART/USB/I2C/SPI
Communication speed		Up to 921600 baud UART, USB 2.0, SPI 125 kB/s, I2C 400 kbit/s
Vehicle dynamics	Dynamics	≤ 4 g
	Velocity	500 m/s

Table 1: u-blox NEO-D9C-00B performance

1.3 Supported GNSS augmentation systems

1.3.1 Quasi-Zenith Satellite System (QZSS)

The Quasi-Zenith Satellite System (QZSS) is a Japanese satellite positioning system. With satellites in quasi-zenith orbits, three satellites will be visible at all times from locations in the Asia-Oceania region. The QZSS correction stream is provided on the L6 band for free.

Signal	QZS1	QZS2/4	QZS3	Service	Frequency
Orbit	QZO	QZO	GEO		
L2C	Transmit	Transmit	Transmit	PNT	1227.60 MHz
L6	L6D	L6D/L6E	L6D/L6E	CLAS/MADOCA	1278.75 MHz

Table 2: QZSS satellites and signals

1 With ZED-F9P aiding messages provided, open sky conditions from QZS-1

2 Power with respect to single component L6D/L6E using a 20-25 dB external LNA

3 Success rate of acquiring at least one L2 QZSS signal > 95% using constellation of 4 visible QZSS satellites using a 20-25 dB external LNA

☞ QZS1 only transmits the CLAS L6D message, while QZS2, QZS3 and QZS4 transmit both CLAS L6D and MADOCA L6E messages.

1.4 Supported protocols

NEO-D9C-00B supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary

Table 3: Supported protocols

For specification of the protocols, see the Interface description [2].

2 System description

2.1 Block diagram

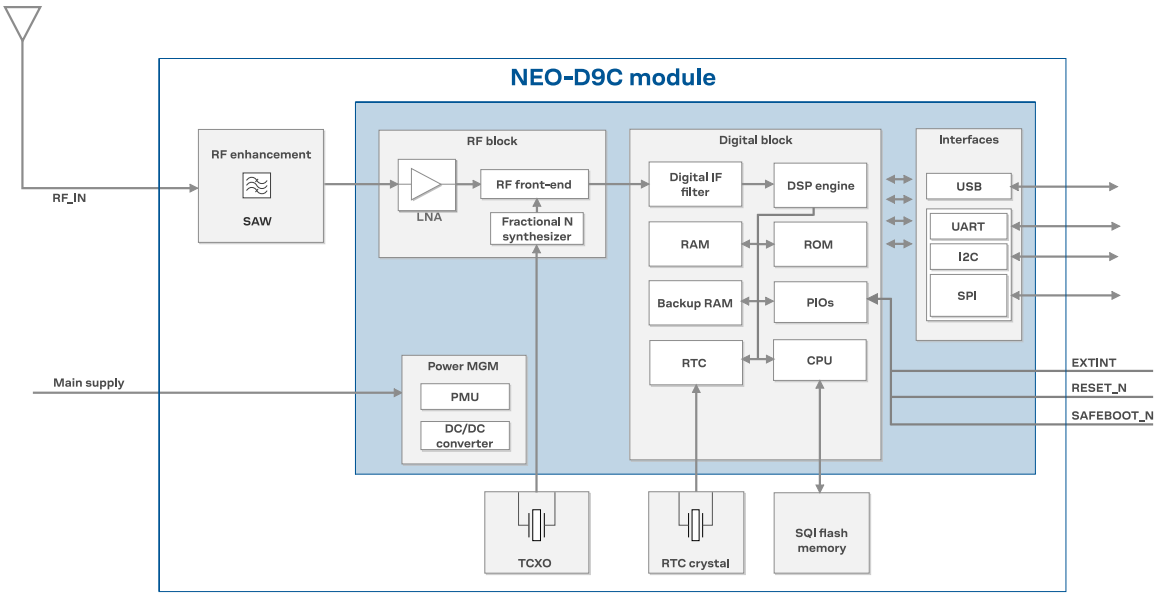


Figure 1: NEO-D9C-00B block diagram

An active antenna is mandatory with the NEO-D9C-00B.

3 Pin definition

3.1 Pin assignment

The pin assignment of the NEO-D9C-00B module is shown in Figure 2. The defined configuration of the PIOs is listed in Table 4.

☞ V_BCKP functionality (pin 22: Reserved), ANT_OFF, ANT_DETECT, ANT_SHORT_N are not available.

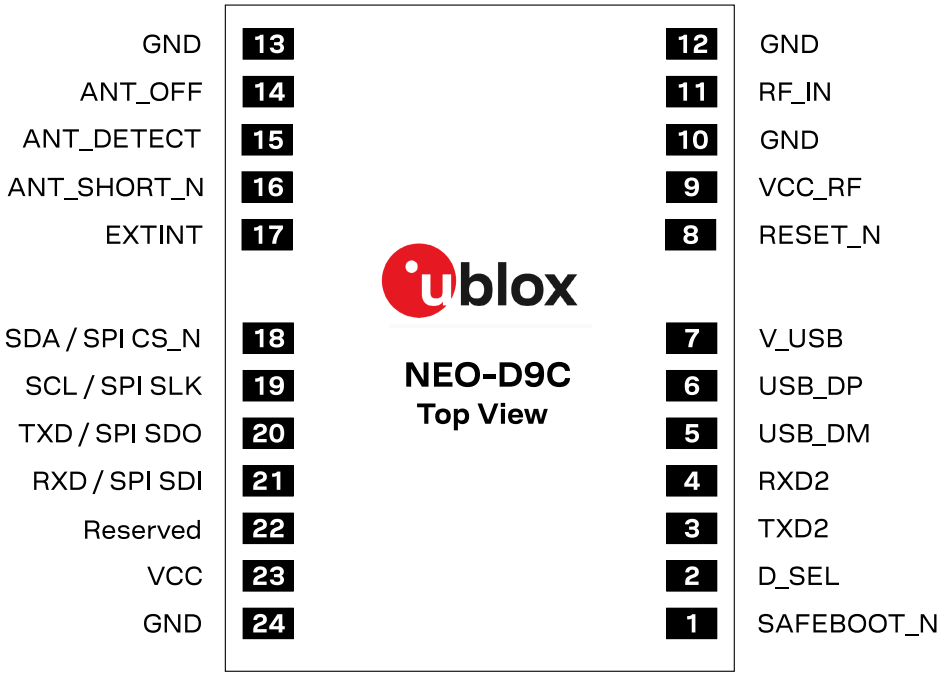


Figure 2: NEO-D9C-00B pin assignment

Pin no.	Name	I/O	Description
1	SAFEBOOT_N	I	SAFEBOOT_N (used for FW updates and reconfiguration, leave open)
2	D_SEL	I	UART 1 / SPI select. (open or high = UART 1)
3	TXD2	O	UART 2 TXD
4	RXD2	I	UART 2 RXD
5	USB_DM	I/O	USB data (DM)
6	USB_DP	I/O	USB data (DP)
7	V_USB	I	USB supply
8	RESET_N	I	RESET (active low)
9	VCC_RF	O	External LNA power
10	GND	I	Ground
11	RF_IN	I	Active antenna L2/L6 band signal input
12	GND	I	Ground
13	GND	I	Ground

Pin no.	Name	I/O	Description
14	ANT_OFF	O	External LNA disable - default active high
15	ANT_DETECT	I	Active antenna detect - default active high
16	ANT_SHORT_N	O	Active antenna short detect - default active low
17	EXTINT	I	External interrupt pin
18	SDA / SPI CS_N	I/O	I2C data if D_SEL = VCC (or open); SPI chip select if D_SEL = GND
19	SCL / SPI SLK	I/O	I2C clock if D_SEL = VCC (or open); SPI clock if D_SEL = GND
20	TXD / SPI SDO	O	UART1 output if D_SEL = VCC (or open); SPI SDO if D_SEL = GND
21	RXD / SPI SDI	I	UART1 input if D_SEL = VCC (or open); SPI SDI if D_SEL = GND
22	Reserved	-	No connection
23	VCC	I	Supply voltage
24	GND	I	Ground

Table 4: NEO-D9C-00B pin assignment

☞ For detailed information on the pin functions and characteristics see the Integration manual [1].

4 Electrical specifications

4.1 Absolute maximum ratings

⚠ CAUTION. Risk of device damage. Exceeding the absolute maximum ratings may affect the lifetime and reliability of the device or permanently damage it. Do not exceed the absolute maximum ratings.

⚠ This product is not protected against overvoltage or reversed voltages. Use appropriate protection to avoid device damage from voltage spikes exceeding the specified boundaries.

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		–0.5	3.6	V
Voltage ramp on VCC[4]			20	8000	µs/V
Input pin voltage	Vin		–0.5	VCC + 0.5	V
VCC_RF output current	ICC_RF			200	mA
Supply voltage USB	V_USB		–0.5	3.6	V
USB signals	USB_DM, USB_DP		–0.5	V_USB + 0.5	V
Input power at RF_IN	Prfin	Source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	Tstg		–40	+85	°C

Table 5: Absolute maximum ratings

4.2 Operating conditions

☞ Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
Supply voltage for USB interface	V_USB	3.0		3.6	V	
V_USB current	I_USB		2.0		mA	
SW backup current	I_SWBCKP		0.07		mA	
Input pin voltage range	Vin	0		VCC	V	
Digital IO pin low level input voltage	Vil			0.4	V	
Digital IO pin high level input voltage	Vih	0.8 * VCC			V	
Digital IO pin low level output voltage	Vol			0.4	V	Iol = 2 mA
Digital IO pin high level output voltage	Voh	VCC – 0.4			V	Ioh = 2 mA
DC current through any digital I/O pin (except supplies)	Ipin			5	mA	
Pull-up resistance for RXD2, TXD2, SDA / SPI_CS_N, SCL / SPI_CLK	R_{pu}	7	15	30	kΩ	
Pull-up resistance for ANT_DETECT, ANT_OFF, ANT_SHORT_N, TXD / SPI_SDO, RXD / SPI_SDI, EXTINT	R_{pu}	30	75	130	kΩ	
Pull-up resistance for RESET_N	R_{pu}	7	10	13	kΩ	
VCC_RF voltage	VCC_RF		VCC – 0.1		V	

[4] Exceeding the ramp speed may permanently damage the device

Parameter	Symbol	Min	Typical	Max	Units	Condition
VCC_RF output current	ICC_RF			50	mA	
Input impedance at RF_IN	Z_{in}		50		Ω	
Receiver chain noise figure[5]	NFtot		11		dB	
Recommended LNA gain into module	LNA_gain		20		dB	
Operating temperature	Topr	–40	+25	+85	°C	

Table 6: Operating conditions

4.3 Indicative power requirements

Table 7 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

All values in Table 7 have been measured at 25 °C ambient temperature.

☞ The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	QZSS L6	Unit
I_{PEAK}	Peak current	Acquisition & tracking	130	mA
$I_{AVERAGE}$	Average current	Acquisition & tracking	55	mA

Table 7: Currents to calculate the indicative power requirements

[5] Only valid for the QZSS L2 band

5 Communications interfaces

NEO-D9C-00B has several communications interfaces[6], including UART, SPI, I2C and USB.

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

5.1 UART

The UART interfaces support configurable baud rates. For further information, see the Integration manual [1].

Hardware flow control is not supported.

UART1 is the primary host communications interface.

Symbol	Parameter	Min	Max	Unit
R_u	Baud rate	9600	921600	bit/s
Δ_{Tx}	Tx baud rate accuracy	-1%	+1%	-
Δ_{Rx}	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 8: NEO-D9C-00B UART specifications

5.2 SPI

The SPI interface is disabled by default. The SPI interface shares pins with UART and I2C and can be selected by setting D_SEL = 0. The SPI interface can be operated in peripheral mode only. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

The SPI timing parameters for peripheral operation are defined in Figure 3. Default SPI configuration is CPOL = 0 and CPHA = 0.

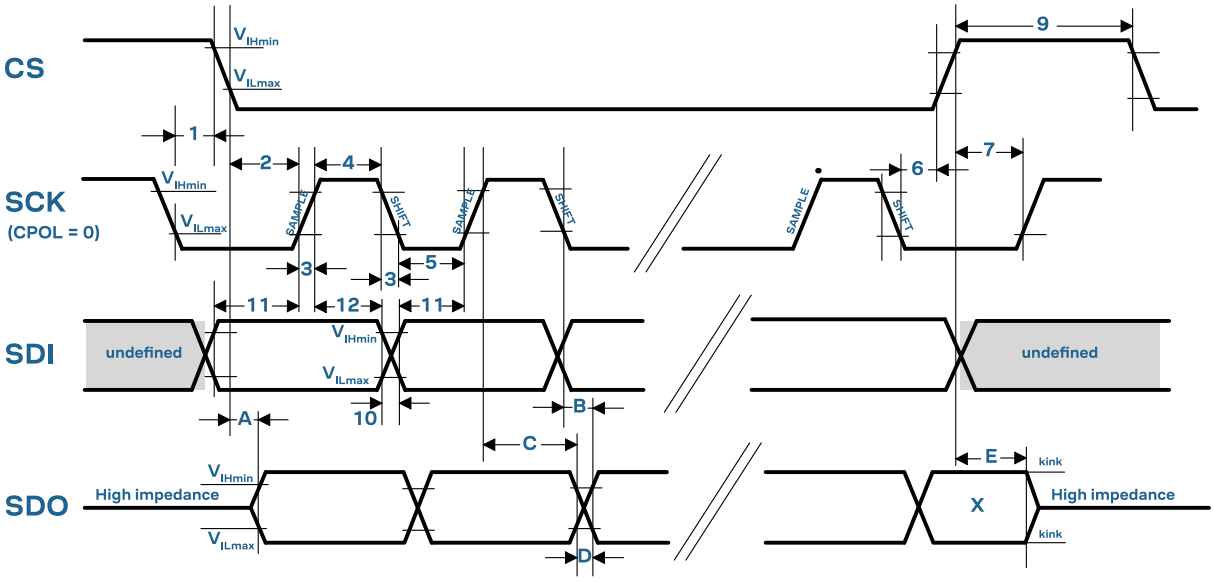


Figure 3: NEO-D9C-00B SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

6 The signal names and related terms have been replaced with new terminology in this document.

Symbol	Parameter	Min	Max	Unit
1	CS deassertion hold time	23	-	ns
2	Chip select time (CS to SCK)	20	-	ns
3	SCK rise/fall time	-	7	ns
4	SCK high time	24	-	ns
5	SCK low time	24	-	ns
6	Chip deselect time (SCK falling to CS)	30	-	ns
7	Chip deselect time (CS to SCK)	30	-	ns
9	CS high time	32	-	ns
10	SDI transition time	-	7	ns
11	SDI setup time	16	-	ns
12	SDI hold time	24	-	ns

Table 9: SPI peripheral input timing parameters 1 - 12

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	12	40	ns
B	SDO data valid time (SCK), weak driver mode	15	40	ns
C	SDO data hold time	100	140	ns
D	SDO rise/fall time, weak driver mode	0	5	ns
E	SDO data disable lag time	15	35	ns

Table 10: SPI peripheral timing parameters A - E, 2 pF load capacitance

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	16	55	ns
B	SDO data valid time (SCK), weak driver mode	20	55	ns
C	SDO data hold time	100	150	ns
D	SDO rise/fall time, weak driver mode	3	20	ns
E	SDO data disable lag time	15	35	ns

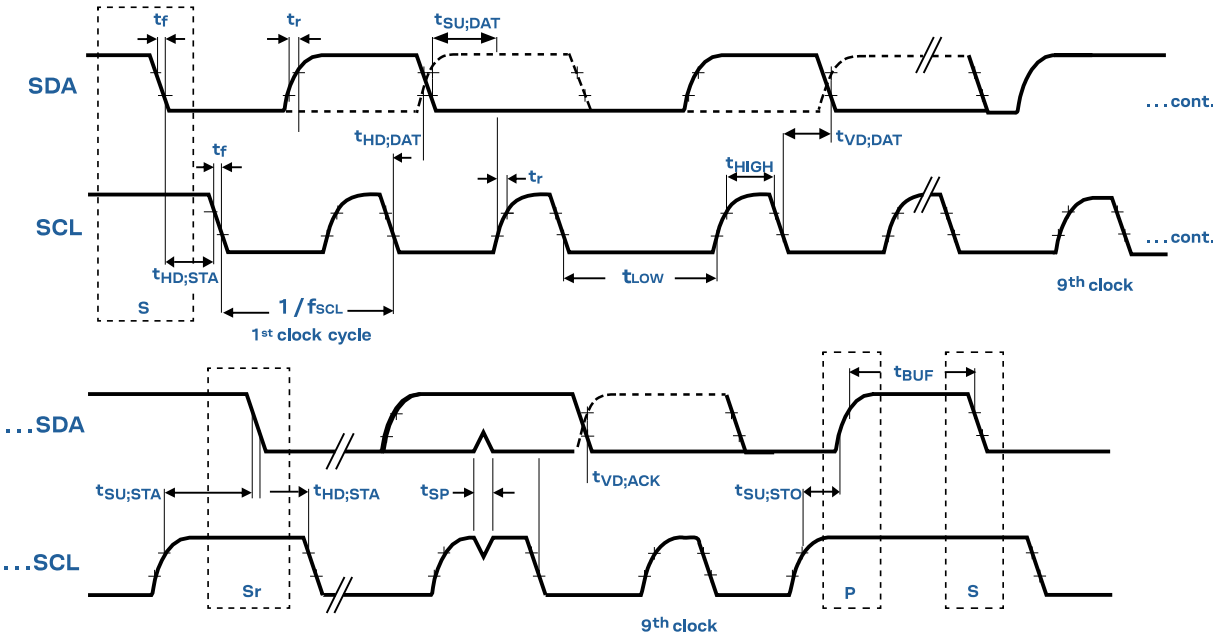
Table 11: SPI peripheral timing parameters A - E, 20 pF load capacitance

Symbol	Parameter	Min	Max	Unit
A	SDO data valid time (CS)	26	85	ns
B	SDO data valid time (SCK), weak driver mode	30	85	ns
C	SDO data hold time	110	160	ns
D	SDO rise/fall time, weak driver mode	13	45	ns
E	SDO data disable lag time	15	35	ns

Table 12: SPI peripheral timing parameters A - E, 60 pF load capacitance

5.3 I2C

An I2C interface is available for communication with an external host CPU in I2C Fast-mode. Backwards compatibility with Standard-mode I2C bus operation is not supported. The interface can be operated only in peripheral mode with a maximum bit rate of 400 kbit/s. The interface can make use of clock stretching by holding the SCL line LOW to pause a transaction. In this case, the bit transfer rate is reduced. The maximum clock stretching time is 20 ms.



V_{IL} = 0.3 V_{DD}
V_{IH} = 0.7 V_{DD}

Figure 4: NEO-D9C-00B I2C peripheral specification

		I2C Fast-mode		
Symbol	**Parameter**	**Min**	**Max**	**Unit**
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.6	-	µs
t_{LOW}	Low period of the SCL clock	1.3	-	µs
t_{HIGH}	High period of the SCL clock	0.6	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6	-	µs
$t_{HD;DAT}$	Data hold time	0 [7]	- [8]	µs
$t_{SU;DAT}$	Data setup time	100 [9]		ns
t_r	Rise time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
t_f	Fall time of both SDA and SCL signals	-	300 (for C = 400pF)	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6	-	µs
t_{BUF}	Bus-free time between a STOP and START condition	1.3	-	µs
$t_{VD;DAT}$	Data valid time	-	0.9 [8]	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	0.9 [8]	µs
V_{nL}	Noise margin at the low level	0.1 V_IO	-	V

7 External device must provide a hold time of at least one transition time (max 300 ns) for the SDA signal (with respect to the min Vih of the SCL signal) to bridge the undefined region of the falling edge of SCL.
8 The maximum $t_{HD;DAT}$ must be less than the maximum $t_{VD;DAT}$ or $t_{VD;ACK}$ with a maximum of 0.9 µs by a transition time. This maximum must only be met if the device does not stretch the LOW period (tLOW) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
9 When the I2C peripheral is stretching the clock, the $t_{SU;DAT}$ of the first bit of the next byte is 62.5 ns.

		I2C Fast-mode		
Symbol	**Parameter**	**Min**	**Max**	**Unit**
V_{nH}	Noise margin at the high level	0.2 V_IO	-	V

Table 13: NEO-D9C-00B I2C peripheral timings and specifications

☞ The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D_SEL = 0, the I2C interface is not available.

5.4 USB

The USB 2.0 FS (full speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V_USB pin supplies the USB interface.

5.5 Default interface settings

Interface	Settings
UART	9600 baud, 8 bits, no parity bit, 1 stop bit. Output protocol: UBX. Only the following UBX message (if enabled) will be output if there is valid data: **UBX-RXM-QZSSL6**. Input protocols without need of additional configuration: UBX.
USB	Output messages activated as in UART. Input protocols available as in UART.
I2C	Output messages activated as in UART. Input protocols available as in UART.
SPI	Output messages activated as in UART. Input protocols available as in UART.

Table 14: Default interface settings

☞ The boot message is still output using $GNTXT messages. The messages are output when the NEO-D9C-00B is powered up.

☞ Refer to the applicable Interface description [2] for information about further settings.

6 Mechanical specifications

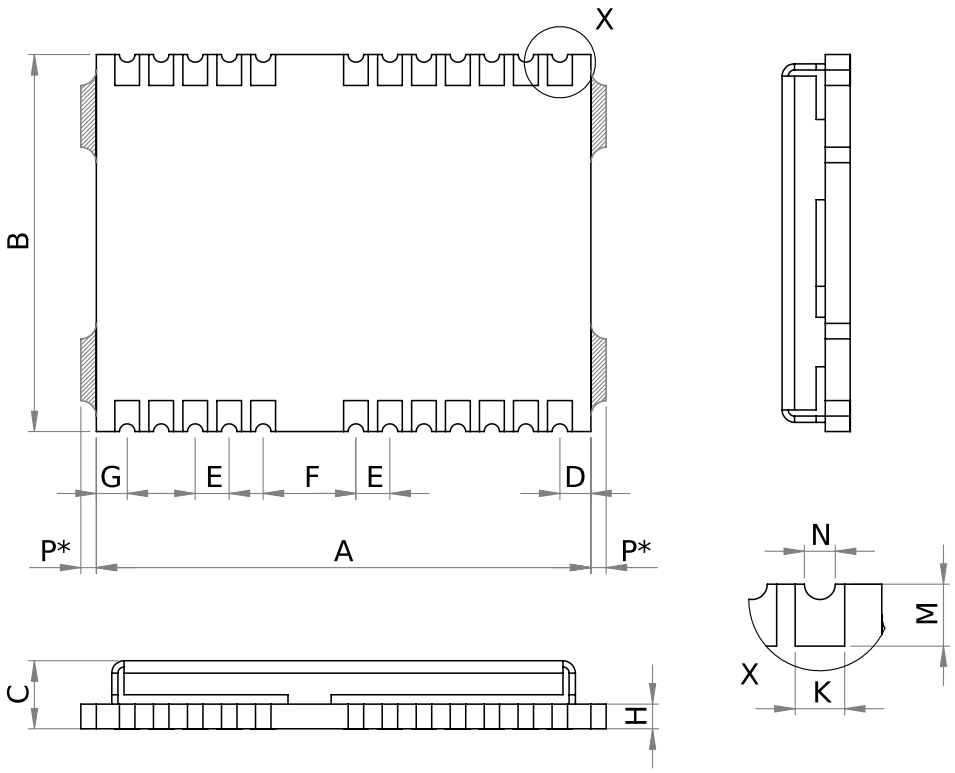


Figure 5: NEO-D9C-00B mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)	
A	15.9	16.0	16.1	
B	12.1	12.2	12.3	
C	2.2	2.4	2.6	
D	0.9	1.0	1.1	
E	1.0	1.1	1.2	
F	2.9	3.0	3.1	
G	0.9	1.0	1.1	
H	-	0.82	-	
K	0.7	0.8	0.9	
M	0.8	0.9	1.0	
N	0.4	0.5	0.6	
P*	0.0	-	0.5	The de-paneling residual tabs may be on either side (not both).
Weight		1.0 g		

Table 15: NEO-D9C-00B mechanical dimensions

☞ The mechanical picture of the de-paneling residual tabs (P*) is an approximate representation. The shape and position may vary, but the overall size of the residual tabs remains within the maximum dimensions even when the tab sizes differ.

☞ Take the size of the de-paneling residual tabs into account when designing the component keep-out area.

7 Qualifications and approvals

Quality and reliability	
Product qualification	Qualified according to ISO 16750
Chip qualification	Modules are based on AEC-Q100 qualified GNSS chips
Manufacturing	Manufactured at ISO/TS 16949 certified sites
Environmental	
RoHS compliance	Yes
Moisture sensitivity level (MSL) [10, 11]	4
Type approvals	
European RED certification (CE)	Declaration of Conformity (DoC) is available on the u-blox website.
UK conformity assessment (UKCA)	Yes

Table 16: Qualifications and approvals

10 For the MSL standard, see IPC/JEDEC J-STD-020 and J-STD-033, available on www.jedec.org

11 For more information regarding moisture sensitivity levels, labelling, storage and drying, see the Product packaging reference guide [3]

8 Product marking and ordering information

This section provides information about product marking and ordering.

8.1 Product marking

The product marking provides information on NEO-D9C-00B and its revision, as in Figure 6. For a description of the product marking, see Table 17.

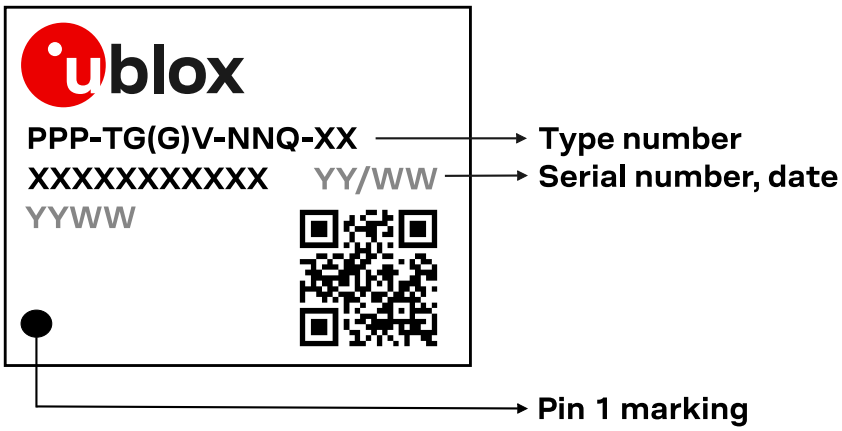


Figure 6: Example of NEO-D9C-00B product marking

Code	Meaning	Example
PPP	Form factor	NEO
TG(G)	Platform	D9 = u-blox D9
V	Variant	C = QZSS corrections
NN	Major product version	00, 01, ..., 99
Q	Product grade	A = Automotive, B = Professional, C= Standard
XX	Revision	Hardware and firmware revisions
YY/WW or YYWW	Production date	Year/week, e.g. 24/04 or 2404
XXXXXXXXXXX	Serial number	Alphanumeric characters, e.g. BN600001181
Other information	QR code	For internal/technical use.

Table 17: Description of product marking

8.2 Product identifiers

The NEO-D9C-00B label features three product identifiers: product name, ordering code, and type number. The product name identifies all u-blox products. It is used in documentation such as this Data sheet and is independent of packaging and product grade. The ordering code indicates the major product version and product grade, and the type number additionally specifies the hardware and firmware revisions.

Table 18 describes the three different product identifiers used in the NEO-D9C-00B label

Identifier	Format	Example
Product name	PPP-TG(G)V	NEO-D9C
Ordering code	PPP-TG(G)V-NNQ	NEO-D9C-00B
Type number	PPP-TG(G)V-NNQ-XX	NEO-D9C-00B-02

Table 18: Product identifiers

8.3 Ordering codes

Ordering code	Product	Remark
NEO-D9C-00B	NEO-D9C	u-blox D9 correction module QZSS L6 receiver for CLAS and MADOCA service

Table 19: Product ordering codes

u-blox provides information on product changes affecting the form factor, size or function of the product. For the Product change notifications (PCNs), see our website at https://www.u-blox.com/en/product-resources.

Related documents

[1] NEO-D9C Integration manual, UBX-21031631
[2] QZS 1.01 Interface description, UBX-21031777
[3] Product packaging reference guide, UBX-14001652

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage https://www.u-blox.com.

Revision history

Revision	Date	Status / comments
R01	15-Sep-2017	Draft
R02	29-Sep-2017	Draft / updated pins 15 and 16
R03	29-Apr-2019	Objective Specification
R04	23-May-2019	Advance Information
R05	27-June-2019	Early Production Information - V_BCKP not used
R06	25-Mar-2020	PCN UBX-19057484 added and module type number updated. Absolute maximum ratings and Operating conditions tables updated.
R07	27-Oct-2020	USB interface section update. UART interface section update. SW backup current update
R08	15-Sep-2021	Update average current value. firmware QZS 1.01 update.
R09	17-Dec-2021	Overall text improvement and typo corrections. Disclosure restriction C1-Public
R10	09-Feb-2022	Production information
R11	16-Dec-2022	Overall text improvement Updated the section Mechanical specification
R12	29-Mar-2023	Updated I2C and SPI timing specifications in section Communications interfaces Updated VCC_RF output current in table Absolute maximum ratings
R13	29-Oct-2025	Updated weight in Mechanical specifications Editorial changes in sections Qualifications and approvals and Product marking

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