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MAYA-W3 series

Host-based multiradio modules with Wi-Fi 6/6E and Bluetooth® Dual Mode

Data sheet

Abstract

Targeted towards system integrators and design engineers, this technical data sheet includes the functional description, pin definition, specifications, country approval status, handling instructions, and ordering information for MAYA-W3 short-range radio modules. This range of ultra-compact, cost-efficient, host-based, multiradio modules support single-stream, tri-band Wi-Fi 6/6E, and Bluetooth® Dual Mode connectivity. Designed for a wide range of industrial applications, MAYA-W3 modules incorporate a MAC/Baseband processor and front-end RF components. The modules connect to a host processor through various interfaces, including SDIO/gSPI for Wi-Fi and High-Speed UART for Bluetooth. Different module variants for single/dual/tri-band Wi-Fi, supplied with or without an onboard antenna, are available.

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Document information

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Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Chipset	PCN reference	Product status
MAYA-W380	MAYA-W380-00B-00	CYW55513	N/A	Functional sample
MAYA-W381	MAYA-W381-00B-00	CYW55513	N/A	Initial production
MAYA-W382	MAYA-W382-00B-00	CYW55513	N/A	Initial production
MAYA-W383	MAYA-W383-00B-00	CYW55513	N/A	Initial production
MAYA-W386	MAYA-W386-00B-00	CYW55513	N/A	Initial production
MAYA-W361	MAYA-W361-00B-00	CYW55512	N/A	Initial production
MAYA-W362	MAYA-W362-00B-00	CYW55512	N/A	Initial production
MAYA-W363	MAYA-W363-00B-00	CYW55512	N/A	Initial production
MAYA-W366	MAYA-W366-00B-00	CYW55512	N/A	Initial production
MAYA-W330	MAYA-W330-00B-00	CYW55511	N/A	Functional sample
MAYA-W331	MAYA-W331-00B-00	CYW55511	N/A	Initial production
MAYA-W332	MAYA-W332-00B-00	CYW55511	N/A	Initial production
MAYA-W333	MAYA-W333-00B-00	CYW55511	N/A	Initial production
MAYA-W336	MAYA-W336-00B-00	CYW55511	N/A	Initial production

Contents

1 Functional description

1.1 Overview

The MAYA-W3 series comprises ultra-compact multiradio modules with Wi-Fi 6/6E and Bluetooth® Dual Mode, including variants with or without an on-board antenna. The series supports IEEE 802.11a/b/g/n/ac/ax Wi-Fi standards, operating in tri-band 2.4/5/6 GHz. It achieves PHY data rates up to 802.11ax MCS11 (1024-QAM 5/6) in 20 MHz channels.

The modules can engage in P2P communication, function as a station with different types of access-points, or a simple access-point, or operate as a combination of these. MAYA-W3 supports Bluetooth® Classic (BR/EDR) and Bluetooth® Low Energy (LE), including long-range PHY and isochronous channels for LE audio. MAYA-W3 is verified against Bluetooth® Core 6.0.

The MAYA-W3 series supports an optional LTE filter and is available with various antenna options, including variants with U.FL connectors, antenna pins, or an on-board antenna. MAYA-W3 modules come with MAC addresses available in the integrated OTP memory.

The modules are developed for reliable, high-demanding, industrial devices, and applications that demand high performance.

Radio type approvals for Europe (RED/UKCA), the United States (FCC), Canada (ISED), and Japan (Giteki) are completed. See also Qualification and approvals.

The MAYA-W3 series is based on the Infineon CYW55513, CYW55512 and CYW55511 chipsets.

Key features

- Variants with antenna pins, U.FL connectors, and embedded PCB antenna
- Wi-Fi 6/6E, tri-band, dual-band, and single-band; single stream, supporting MU-MIMO
- 20 MHz Wi-Fi channels
- Wi-Fi 802.11a/b/g/n/ac/ax
- Bluetooth® 6.0 Dual Mode supporting LE Audio
- Wi-Fi security: WPA3, WPA2, WAPI, AES
- Secure boot
- Industrial temperature range -40 °C to +85 °C

1.2 Product features

Product features	Description
Variants	MAYA-W38x: Triple-band 2.4/5/6 GHz Wi-Fi 6E + Bluetooth BR/EDR/LE MAYA-W36x: Dual-band 2.4/5 GHz Wi-Fi 6 + Bluetooth BR/EDR/LE MAYA-W33x: Single-band 2.4 GHz Wi-Fi 6 + Bluetooth BR/EDR/LE
Wi-Fi Standards	Wi-Fi 6/6E IEEE 802.11a/b/g/n/ac/ax
Wi-Fi frequency bands	2.4 GHz, channel 1–13 5 GHz, channel 36–165 6 GHz, channel 1–233
Bluetooth	Bluetooth Core 6.0 specification support, BR/EDR, Low Energy
Antenna configurations	Dual antenna pins or U.FL connectors for simultaneous Wi-Fi and Bluetooth operation
	Single antenna pin or U.FL connector for shared 2.4 GHz Wi-Fi and Bluetooth operation
	Single embedded antenna and antenna pin for shared 2.4 GHz Wi-Fi and Bluetooth operation
Software features	
Security	WPA3, WPA2, and WPA mixed mode
MAC addresses	Available in on-board OTP memory
Wi-Fi operational modes	Station, Access-Point, Wi-Fi direct, or combination of these
Driver support	Free drivers for Linux and Android
Interfaces	
Wi-Fi	SDIO 3.0 (4-bit, up to 100 MHz clock)
Bluetooth	HCI transport layer via High-speed UART (4-wire) or shared SDIO[1] with Wi-Fi. PCM/I2S for audio
Other	GPIOs
Package	
Dimensions	10.4 x 14.3 x 2.0 mm
Mounting	Soldering, 90 pins (LGA)
Environmental data, quality, and reliability	
Operating temperature	-40 °C to +85 °C
Moisture Sensitivity Level (MSL)	4
RoHS and REACH compliance	Yes
Electrical data	
RF power supply	3.3 VDC
I / O power supply	1.8 VDC
Certifications and approvals	
Type approvals	Europe (RED/UKCA), US (FCC), Canada (ISED), Japan (Giteki) Other country certifications can be provided on request
Bluetooth qualification	Bluetooth Core v6.0 (BR/EDR and LE)
Support Products	
EVK-MAYA-W381	Evaluation kit for MAYA-W381-00B
EVK-MAYA-W386	Evaluation kit for MAYA-W386-00B

Table 1: MAYA-W3 series product features

☞ For information about the supported product variants of MAYA-W3 series, see Ordering information.

[1] Can be provided on request

1.3 Block diagrams

Figure 1 shows the block diagram for the single embedded antenna module variants in the MAYA-W3 series. These modules are equipped with an internal, on-board PCB antenna and a single RF pin (**RF_ANT1**) with which to feed the on-board antenna (**ANT_EXT_FEED**).

For antenna diversity configuration, an external RF switch can be placed instead of the antenna feed network to switch the RF signal between the on-board and external antenna. One of **RF_CNTL** outputs can be used for antenna diversity switch control. Similar configuration can be used for other module variants.

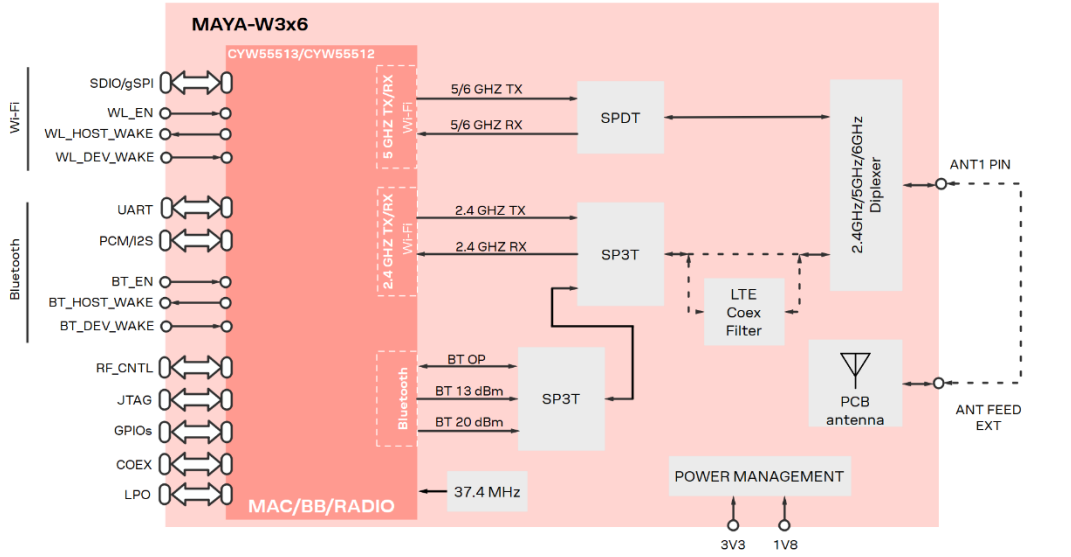


Figure 1: MAYA-W3 single embedded antenna variant block diagram

Figure 2 shows the block diagram of the dual- and single-antenna variants of MAYA-W3 series. The dual-antenna modules are equipped with two RF pins or U.FL connectors for simultaneous Wi-Fi (**RF_ANT1/J1**) and Bluetooth (**RF_ANT0/J2**) operation. The single-antenna modules support shared Wi-Fi and Bluetooth operation on a single RF pin (**RF_ANT1**) or U.FL connector (**J1**).

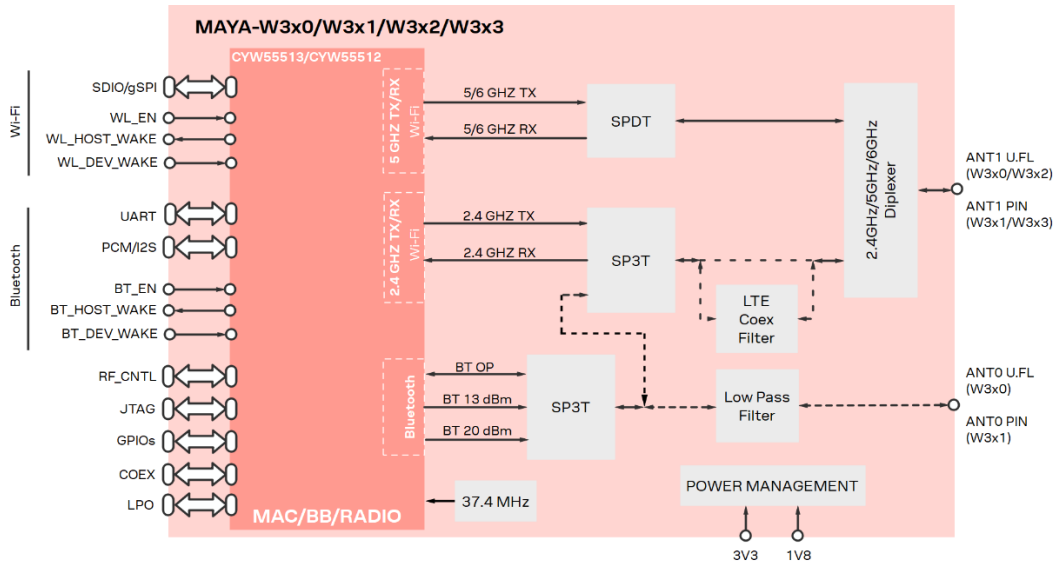


Figure 2: MAYA-W dual- and single-antenna variant block diagram

1.4 Product description

With a footprint of only 14.3 x 10.4 mm, the MAYA-W3 series of ultra-compact Wi-Fi/Bluetooth modules is developed for reliable, high-demanding, industrial devices and applications. Based on the Infineon CYW55513, CYW55512 and CYW55511 chipsets, MAYA-W3 includes an integrated MAC/Baseband processor and RF front-end components.

The MAYA-W3 series offers multiple antenna solutions, as described in Antenna interfaces.

- An optional LTE filter for improved coexistence with LTE bands 7, 38, 40, and 41 can be included in all module variants.
- All module variants also include discrete and integrated filters in the 2.4 GHz band and 5/6 GHz band.

1.5 Supported features

- Highly effective integrated antenna, antenna pins, or U.FL connectors
- Extended operating temperature range of -40 °C to +85 °C
- Dual antenna configurations: Simultaneous Wi-Fi and Bluetooth operation
- Single antenna configurations: Shared 2.4 GHz Wi-Fi and Bluetooth operation with shared LNA receiver
- Internal Wi-Fi/Bluetooth coexistence support

1.5.1 Wi-Fi features

- Supports Wi-Fi 6/6E, IEEE 802.11 a/b/g/n/ac/ax
- Variants with tri-band, dual-band, or single-band Wi-Fi
- Single stream 802.11ax with 20 MHz channel width, 1024-QAM
- Data rates up to 143 Mbps (MCS11)
- 802.11n short and long guard interval
- 802.11ax Extended Range, DCM and TWT
- Dynamic frequency selection (radar detection)
- Power saving features.
- SDIO 3.0 device interface
- Security: WPA3, WPA2, WEP, and TKIP
- Wi-Fi Standards IEEE 802.11e/d/h/i/r/w
- Supports Wi-Fi direct/P2P mode
- Supports up to 16 stations in AP mode

1.5.2 Bluetooth features

- Dual-mode Bluetooth Low Energy (LE) and Bluetooth BR/EDR
- Bluetooth Core 6.0 specification support
- Bluetooth Class 1 and Class 2 operation
- Bluetooth LE long range (125/500 kbps) support
- Bluetooth LE 1 and 2 Mbps PHY
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting Bluetooth LE audio

- High-speed UART host interface with standard HCI transport layer
- I2S and PCM interface for voice applications
- Encryption (AES) support
- Bluetooth LE Broadcaster, Observer, Central, and Peripheral roles
- Bluetooth LE link layer topology (connects to 7 links)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length and Advertising Extension

1.6 Reserved MAC addresses

MAYA-W3 series modules have four consecutive MAC addresses that are unique for each module variant. The first two of these four addresses are configured during production.

The first address is used for Bluetooth communication, while the second address is configured for Wi-Fi communication. The Data Matrix Code shown on the product label includes the Bluetooth MAC address. See also Product labeling. The remaining two MAC addresses are not used in the manufacturing configuration but are reserved for module usage.

MAC address	Assignment	Last two bits of MAC address	Example
Module1, address 1	Bluetooth	0b00	D4:CA:6E:44:00:04
Module1, address 2	Wi-Fi	0b01	D4:CA:6E:44:00:05
Module1, address 3	(free for use)	0b10	D4:CA:6E:44:00:06
Module1, address 4	(free for use)	0b11	D4:CA:6E:44:00:07
Module2, address 1	Bluetooth	0b00	D4:CA:6E:44:00:08
Module2, address 2	Wi-Fi	0b01	D4:CA:6E:44:00:09
Module2, address 3	(free for use)	0b10	D4:CA:6E:44:00:0A
Module2, address 4	(free for use)	0b11	D4:CA:6E:44:00:0B

Table 2: MAC address assignment

2 Interfaces

2.1 Interface configuration

The hardware state at power-on can differ depending on the pin multiplexing and strap settings. The state of the hardware is determined by the pin state at power-on after the boot code finishes and before the firmware download begins.

MAYA-W3 supports one configuration pin, **SD_DAT[2]**, for selecting the host interface configuration for Wi-Fi operation, as shown in Table 3. The configuration pins revert to their normal function after boot-up.

To set a configuration bit to 0, attach a 10 kΩ resistor from the pin to ground. A 10 kΩ pull-up resistor to **1V8** is required to set a configuration bit to 1.

SD_DAT[2]	Wi-Fi
0	gSPI
1	SDIO

Table 3: Firmware boot options

2.2 Host interfaces

MAYA-W3 supports the following high-speed host interfaces:

- SDIO 3.0 or gSPI interface for Wi-Fi, see Interface configuration for firmware boot options
- Standard Host Controller Interface (HCI) via high-speed UART or shared SDIO[2] interface for Bluetooth

2.2.1 SDIO interface

MAYA-W3 supports an SDIO device interface that conforms to the industry standard SDIO 3.0 specification, including default speed (25 MHz), high-speed (50 MHz), SDR12/25/50 (12/25/50 MB/s), and DDR50 (50 MB/s) modes. The interface supports 1-bit and 4-bit SDIO transfer modes at the full clock range up to 100 MHz for SDR50. All mandatory SDIO commands are supported.

In 4-bit SDIO mode, data is transferred on all four data pins (**SD_DAT**[3:0]). The interrupt pin is not available for exclusive use as it is utilized as a data transfer line. If the interrupt function is required, special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible with speeds up to 50 MB/s in SDR50 mode.

The pull-up resistors required for the SD interface on **SD_CMD**, **SD_DAT** [3:0] must be provided by the host or external resistors can be used. The value of resistors should be between 10–100 kΩ.

Low value series termination resistors can be required to help with signal integrity.

Table 4 describes the required pins for the SDIO interface.

Pin name	I/O type	1-bit mode	4-bit mode
SD_DAT[0]	I/O	DATA: Data line	Data line 0
SD_DAT[1]	I/O	IRQ: Interrupt	Data line 1
SD_DAT[2]	I/O	RW: Read Wait	Data line 2
SD_DAT[3]	I/O	N/C: Not used	Data line 3
SD_CMD	I/O	Command line	Command line
SD_CLK	I	Clock input	Clock input

Table 4: SDIO interface pin description

[2] Can be provided on request

2.2.1.1 Default speed and high-speed modes (1.8 V)

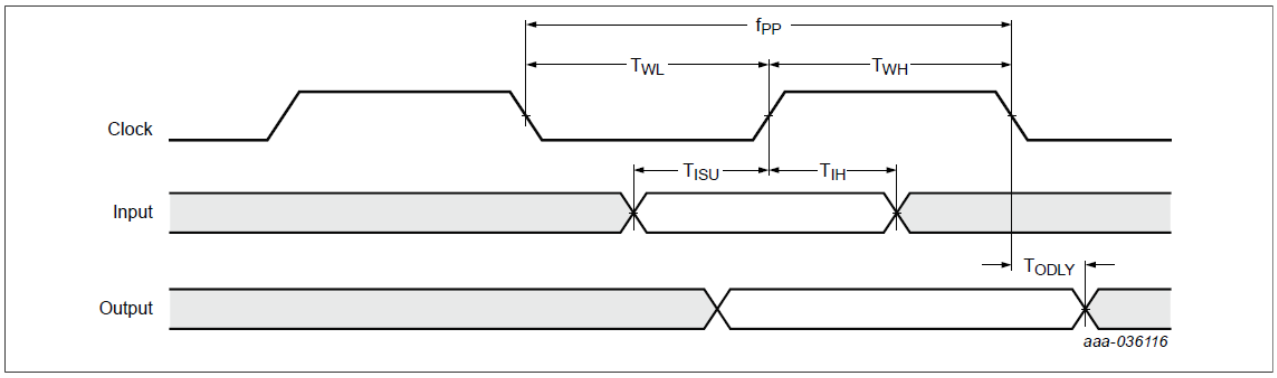


Figure 3: SDIO protocol timing diagram - default speed mode

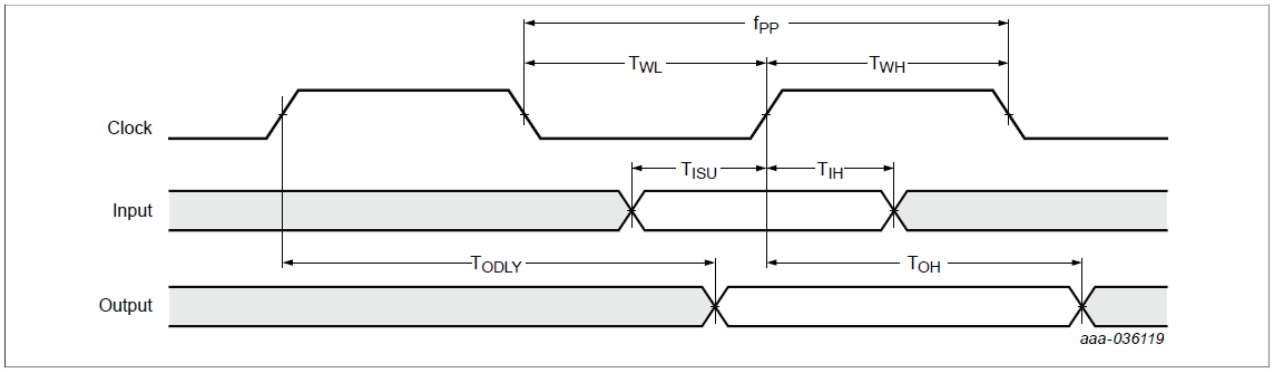


Figure 4: SDIO protocol timing diagram – high speed mode

Table 5 describes the SDIO timing data for the default and high-speed modes with the SDIO clock running at 25 MHz or 50 MHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{pp}	Clock frequency	Default speed	0	-	25	MHz
		High speed	0	-	50	MHz
T_{WL}	Clock low time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{WH}	Clock high time	Default speed	10	-	-	ns
		High speed	7	-	-	ns
T_{ISU}	Input setup time	Default speed	5	-	-	ns
		High speed	6	-	-	ns
T_{IH}	Input hold time	Default speed	5	-	-	ns
		High speed	2	-	-	ns
T_{ODLY}	Output Delay Time	Default speed	-	-	14	ns
		High speed	-	-	14	ns
T_{OH}	CL≤40 pF (1 card)	Default speed	2.5	-	-	ns
		High speed	-	-	-	ns

Table 5: SDIO timing data – default and high-speed modes

2.2.1.2 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

Table 6 describes the SDIO timing data for the SDR12/25/50 modes with the SDIO clock running at up to 100 MHz.

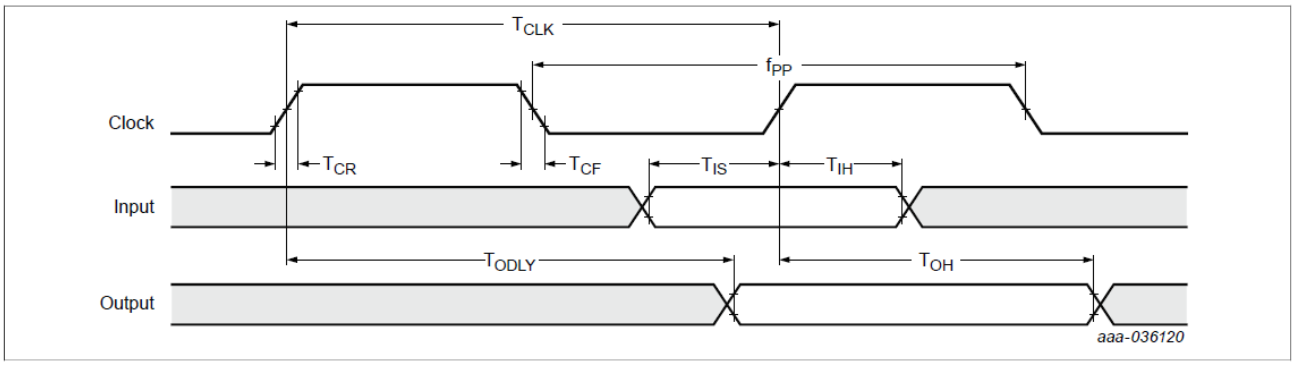


Figure 5: SDIO protocol timing diagram – SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8 V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{pp}	Clock frequency	SDR12	0	–	25	MHz
		SDR25	0	-	50	
		SDR50	0	-	100	
T_{IS}	Input setup time	SDR12	5	–	–	ns
		SDR25	6	-	-	
		SDR50	3	-	-	
T_{IH}	Input hold time	SDR12	5	–	–	ns
		SDR25	2			
		SDR50	0.8			
T_{CLK}	Clock time	SDR12	40	–	40	ns
		SDR25	10	-	20	
		SDR50	10	-	10	
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12	–	–	0.2*T_{CLK}	ns
		SDR25	–	–	0.2*T_{CLK}	ns
		SDR50	–	–	0.2*T_{CLK}	ns
T_{OLDY}	Output delay time $C_L \leq 30$ pF	SDR12	–	–	7.5	ns
		SDR25	–	–	14	ns
		SDR50	–	–	14	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12	1.5	–	–	ns
		SDR25	1.5	–	–	ns
		SDR50	1.5	–	–	ns

Table 6: SDIO timing data – SDR12, SDR25, SRD50 modes (up to 100 MHz) (1.8 V)

2.2.1.3 DDR50 mode (50 MHz) (1.8 V)

Table 7 describes the SDIO timing data for the DDR50 mode with the SDIO clock running at 50 MHz.

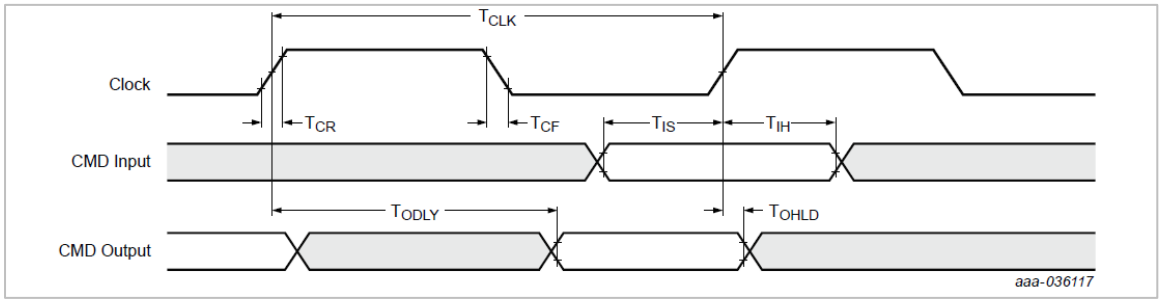


Figure 6: SDIO CMD timing diagram – DDR50 mode (50 MHz)

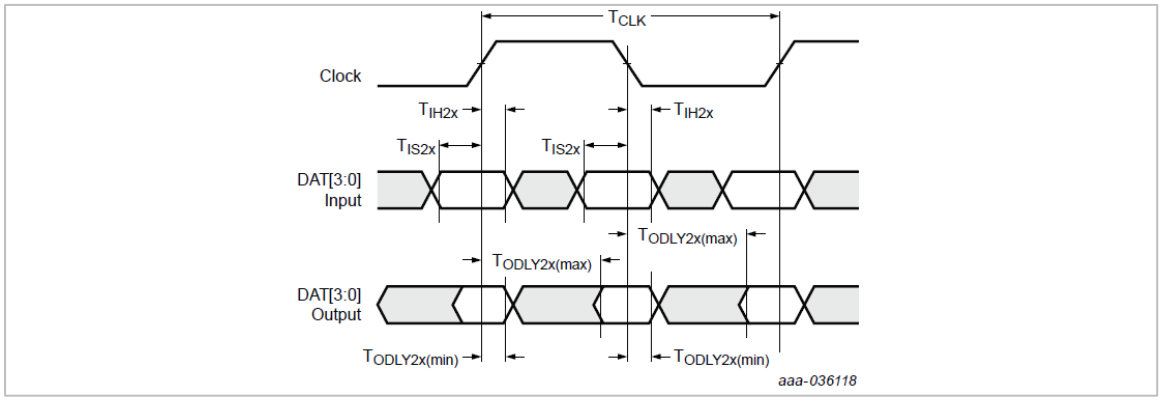


Figure 7: SDIO DAT[3:0] timing diagram – DDR50 mode

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	–	–	ns
T_{CR} ,T_{CF}	Rise time, fall time T_{CR} ,T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	–	–	0.2*T_{CLK}	ns
Clock duty	–	DDR50	45	–	55	%
CMD input (with reference to rising clock edge)						
T_{IS}	Input setup time C_{CARD} = 10 pF (1 card)	DDR50	6	–	–	ns
T_{IH}	Input hold time C_{CARD} = 10 pF (1 card)	DDR50	0.8	–	–	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode $C_L \leq$ 30 pF (1 card)	DDR50	–	–	13.7	ns
T_{OHLD}	Output hold $C_L \geq$15 pF (1 card)	DDR50	1.5	–	–	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time $C_{CARD} \leq$10 pF (1 card)	DDR50	3	–	–	ns
T_{IH2x}	Input hold time $C_{CARD} \leq$10 pF (1 card)	DDR50	0.8	–	–	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\,(max)}$	Output delay time during data transfer mode $C_L \leq 25$ pF (1 card)	DDR50	–	–	7.0	ns
$T_{ODLY2x\,(min)}$	Output hold time $C_L \geq 15$ pF (1 card)	DDR 50	1.5	–	–	ns

Table 7: SDIO timing data – DDR50 mode (50 MHz)

2.2.2 UART interface

MAYA-W3 supports a high-speed UART host interface for Bluetooth operation. The baud rate is adjustable from 9600 bps to 4.0 Mbps. The default baud rate is 115.2 Kbaud. The UART supports RX/TX pins and mandatory RTS/CTS flow control signals. Table 8 describes the module pins on the UART interface.

Pin name	I/O type	Description
UART_CTS	I	Active low clear-to-send input signal
UART_TX	O	UART serial output signal
UART_RX	I	UART serial input signal
UART_RTS	O	Active low request-to-send signal

Table 8: Bluetooth UART interface description

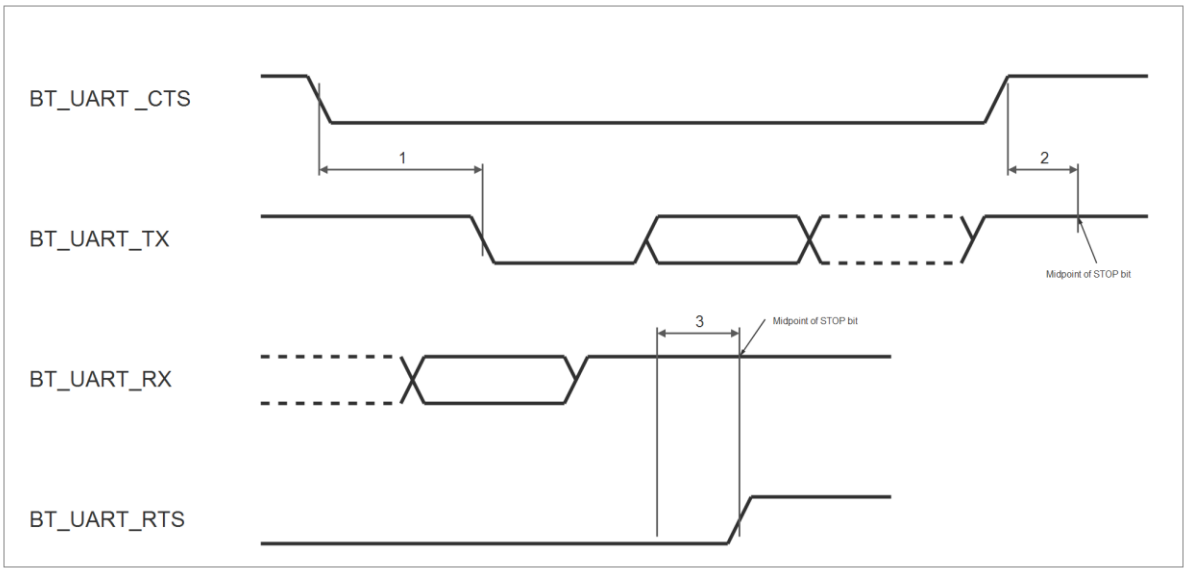


Figure 8: UART timing

Reference	Characteristic	Min.	Typ	Max.	Units
1	Delay time, BT_UART_CTS low to BT_UART_TX valid	-	-	1.5	Bit period
2	Setup time, BT_UART_CTS high before midpoint of stop bit	-	-	0.5	Bit period
3	Delay time, midpoint of stop bit to BT_UART_RTS high	-	-	0.5	Bit period

Table 9: UART timing specification

2.2.3 gSPI interface

MAYA-W3 supports a generic SPI (gSPI) host interface for Wi-Fi operation with a maximum clock speed of 50 MHz and up to 20 Mbps sustained throughput. The pins are shared with the SDIO interface.

Table 10 describes the module pins for the gSPI interface. To select the gSPI host interface it is necessary to set the configuration pin **SD_DAT[2]** to logic-level 0 by attaching 10 kΩ resistor to ground.

Pin name	I/O type	Description	SDIO pin multiplexing
GSPI_CS	I	gSPI chip select input signal	SD_DAT[3]
GSPI_IRQ	O	gSPI interrupt request signal	SD_DAT[1]
GSPI_SCLK	I	gSPI clock input signal	SD_CLK
GSPI_MISO	O	gSPI main in/sub out signal	SD_DAT[0]
GSPI_MOSI	I	gSPI main out/sub in signal	SD_CMD

Table 10: gSPI interface description

2.3 Antenna interfaces

The MAYA-W3 series supports multiple single- and dual-antenna configurations:

- Single on-board antenna or antenna pin – configured externally by a 0 Ω jumper
- One or two external antennas connected through antenna pins
- One or two external antennas connected through on-module U.FL connectors

To prevent mutual interference and improve coexistence performance with LTE bands, MAYA-W3 also supports an optionally integrated, high-performance, 2.4 GHz SAW LTE band pass filter.

Table 11 shows the antenna interfaces and supported frequency bands for each module variant.

Product name	Wi-Fi band[3]	Interface	Description
MAYA-W380 MAYA-W330	3b 1b	J1	U.FL connector for external Wi-Fi antenna
		J2	U.FL connector for external Bluetooth antenna
MAYA-W381 MAYA-W361 MAYA-W331	3b 2b 1b	RF_ANT1	Antenna pin for external Wi-Fi antenna
		RF_ANT0	Antenna pin for external Bluetooth antenna
MAYA-W382 MAYA-W362 MAYA-W332	3b 2b 1b	J1	Single U.FL connector for external Wi-Fi and Bluetooth antenna. Bluetooth and 2.4 GHz Wi-Fi are time-shared with a shared RX LNA.
MAYA-W383 MAYA-W363 MAYA-W333	3b 2b 1b	RF_ANT1	Single antenna pin for external Wi-Fi and Bluetooth antenna. Bluetooth and 2.4 GHz Wi-Fi are time-shared with a shared RX LNA.
MAYA-W386 MAYA-W366 MAYA-W336	3b 2b 1b	RF_ANT1	Single antenna pin for external Wi-Fi and Bluetooth antenna. Bluetooth and 2.4 GHz Wi-Fi are time-shared with a shared RX LNA.
		ANT_EXT_FEED	Antenna feed pin from RF_ANT1 for embedded PCB antenna

Table 11: MAYA-W3 antenna configurations

2.3.1 Internal (on-board) antenna

MAYA-W3 variants with embedded antenna include a 2.4/5/6 GHz internal, niche antenna. The antenna is embedded into the module design and optimized for the MAYA form factor. These modules support an RF signal pin and embedded antenna feed pin, so it is possible to use an external antenna, or an embedded antenna connected by external 0 Ω jumper to the RF signal pin.

[3] 3b=tri-band 2.4/5/6 GHz, 2b=dual-band 2.4/5 GHz, 1b=single-band 2.4 GHz.

2.3.2 External RF antenna interface

MAYA-W3 variants equipped with single/dual RF pins (**RF_ANT1**, **RF_ANT0**) or correspondent U.FL connectors (**J1**, **J2**) provide antenna interfaces with a 50 Ω characteristic impedance for use with external antennas. The antenna signal supports both Tx and Rx.

Figure 9 shows the antenna assignment for the U.FL connector module variants.

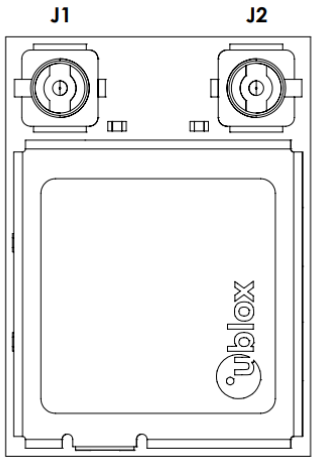


Figure 9: MAYA-W3x0 antenna configuration (top view)

The external antenna can be an SMD antenna (or PCB integrated antenna) mounted on the host board. An antenna connector for use with an external antenna through a coaxial cable can also be considered. If the module is mounted in a shielded enclosure, such as a metal box or cabinet, an appropriate cable antenna might be more suitable. See the list of approved antennas [5].

2.4 Power supply interfaces

The DC power for MAYA-W3 series modules is supplied through **3V3** and **1V8** pins.

2.4.1 Power up sequence

Figure 10 shows the recommended power-up sequence of a MAYA-W3 series module.

Start with applying **3V3** before or at the same time as **1V8**. Once these voltages have reached 90% of their target levels, **WL_EN** and **BT_EN** can be set high after at least 50 us (or two 32 kHz LPO clock cycles) to enable internal power management circuitry. SDIO host can access the device after 78 ms from WL_EN assertion and UART host can access the device after 65.5 ms from BT_EN assertion.

- **3V3** and **1V8** should not rise faster than 10%-90% of their target levels within 40 microseconds.
- **3V3** should be up and have reached its target level before or at the same time as **1V8**.
- **1V8** should NOT reach its target level or be held high before **3V3** has done so.

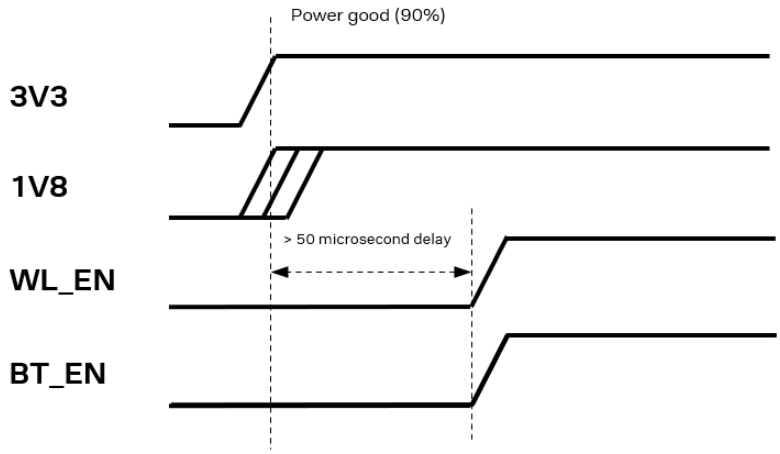


Figure 10: Power sequence of MAYA-W3 module

2.4.2 Power down

MAYA-W3 modules WLAN and Bluetooth section enter "Power Down" mode when **WL_EN** or **BT_EN** are asserted. After assertion, the power on **3V3** and **1V8** supplies can be removed and the module then enters the "Power Off" mode.

2.4.3 Reset

Although external reset is not a prerequisite for correct operation. In the event of any abnormal module behavior, an external reset can be asserted by the host controller through **WL_EN** and **BT_EN**.

MAYA-W3 series modules are reset to a default operating state by any of the following events:

- **WL_EN** asserted. This controls the CYW5551x power management regulators. The WLAN section is in reset when this signal is in a low-level logic state. This pin has a 50 kΩ pull-down (PD) resistor.
- **BT_EN** asserted. This controls the CYW5551x power management regulators. The Bluetooth section is in reset when this signal is in a low-level logic state. This pin has a 50 kΩ PD resistor.

☞ As the firmware is stored in volatile memory only, the firmware must be downloaded to the module after each reset.

2.5 Wake-up signals

In sleep mode, MAYA-W3 operates with reduced power consumption.

Table 12 shows optional, out-of-band wake-up pins (input) that wake the radios from sleep mode. Radio-to-host, wake-up output signals can be used to wake the host from sleep mode.

Pin name	I/O type	Description
WL_WAKE_HOST	O	Wi-Fi radio to host wake-up output signal
WL_DEV_WAKE	I	Wi-Fi radio wake-up input signal
BT_WAKE_HOST	O	Bluetooth radio to host wake-up output signal
BT_DEV_WAKE	I	Bluetooth radio wake-up input signal

Table 12: Wake-up pins

2.6 GPIOs

MAYA-W3 supports various GPIO pins. On power-up and reset, the GPIO pins assume a high-impedance tristate. The JTAG and coexistence interfaces can be assigned to the GPIO pins. After initialization, firmware is downloaded, and the pads are programmed in line with the functionality of the GPIOs. See also Pin assignment.

For information about the purpose of the GPIOs, see Coexistence interfaces and JTAG. Descriptions of all other used GPIOs are in the Pin definition.

2.7 PCM interface

MAYA-W3 series modules include a bidirectional Pulse Code Modulation (PCM) interface that supports:

- Central or Peripheral modes
- Sample rate 8 kHz for NBS and 16 kHz for WBS
- PCM sample width of 16 bits
- Bit clocks of 128 k, 256k, 512k, 1024k and 2048k with different number of 16-bit slots

In PCM central mode, the interface generates the **PCM_CLK** and **PCM_SYNC** signals. In peripheral mode, **PCM_CLK** and **PCM_SYNC** are generated by another central mode device on the bus and MAYA-W3 configures these pins as inputs. The PCM interface shares the pins with the I2S interface. PCM and I2S interfaces are multiplexed with the chipset's TDM2 audio interface.

Table 13 describes the pins supported in the PCM interface.

Pin name	I/O type	Description	I2S pin multiplexing
PCM_DOUT	O	PCM data out	I2S_DOUT
PCM_DIN	I	PCM data in	I2S_DIN
PCM_CLK	I/O	PCM clock, can be output (if central) or input (if peripheral)	I2S_BCLK
PCM_SYNC	I/O	PCM sync, can be output (if central) or input (if peripheral)	I2S_LRCLK
PCM_MCLK	O	Optional clock pins	I2S_CCLK

Table 13: PCM interface description

Figure 11 describes the timing specifications for short frame synchronization in central mode. Table 14 describes the timing references and parameter values shown in the diagram.

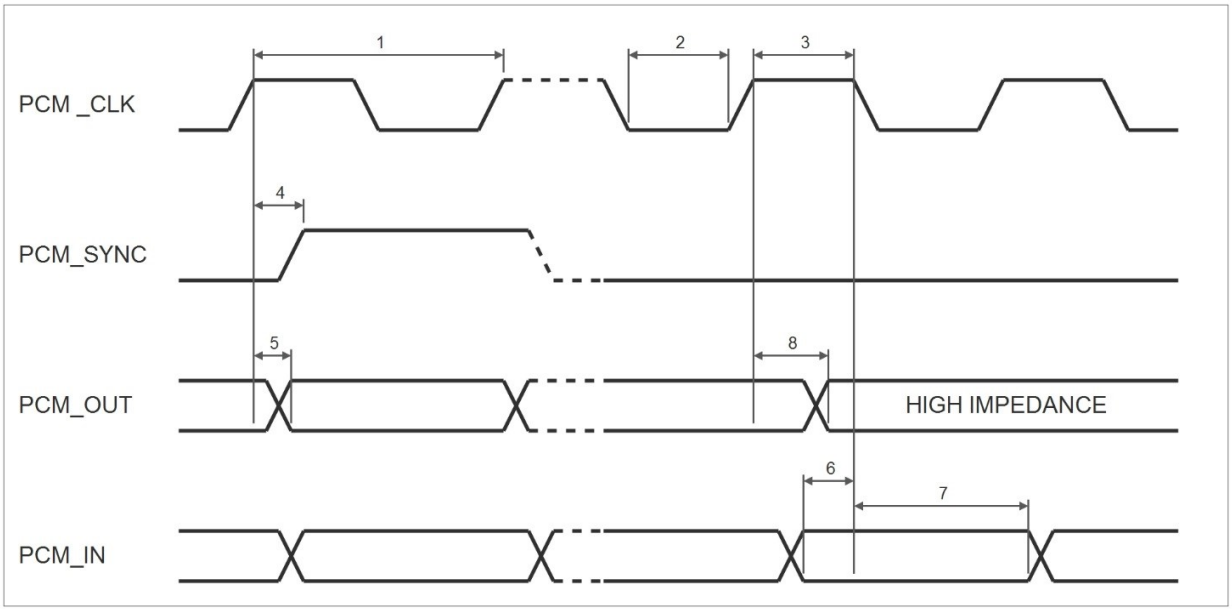


Figure 11: PCM timing diagram showing short frame synchronization in central mode

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
1	PCM clock frequency	-	-	-	12	MHz
2	PCM bit clock LOW	-	41	-	-	ns
3	PCM bit clock HIGH	-	41	-	-	ns
4	PCM_SYNC delay	-	0	-	25	ns
5	PCM_OUT delay	-	0	-	25	ns
6	PCM_IN setup	-	8	-	-	ns
7	PCM_IN hold	-	8	-	-	ns
8	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	-	0	-	25	ns

Table 14: Symbols and parameter values for frame synchronization in central mode

Figure 12 describes the timing specifications for short frame synchronization in peripheral mode. Table 15 describes the timing references and parameter values shown in the diagram.

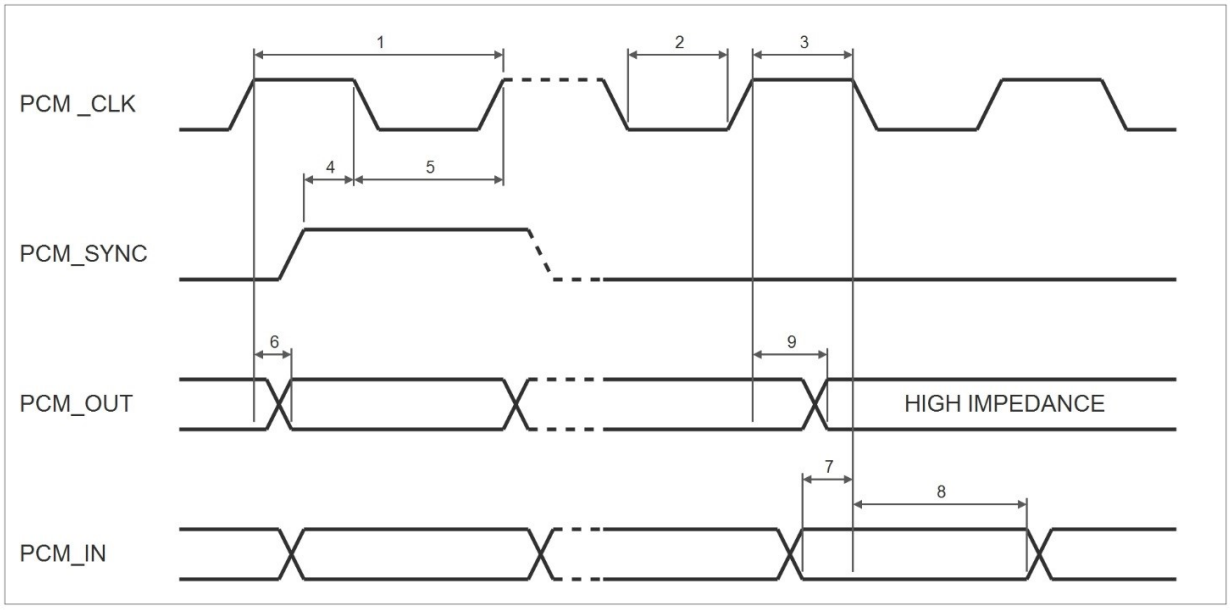


Figure 12: PCM timing diagram showing short frame synchronization in peripheral mode

Symbol	Parameter	Condition	Min.	Typ	Max.	Units
1	PCM clock frequency	-	-	-	12	MHz
2	PCM bit clock LOW	-	41	-	-	ns
3	PCM bit clock HIGH	-	41	-	-	ns
4	PCM_SYNC setup	-	8	-	-	ns
5	PCM_SYNC hold		8	-	-	ns
6	PCM_OUT delay	-	0	-	25	ns
7	PCM_IN setup	-	8	-	-	ns
8	PCM_IN hold	-	8	-	-	ns
9	Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance	-	0	-	25	ns

Table 15: Symbols and parameter values for frame synchronization in peripheral mode

2.8 I2S interface

MAYA-W3 series modules provide an I2S interface that supports bit clocks of 256 kHz (NBS) and 512 kHz (WBS). The interface is shared with the PCM pins and configuration is done through vendor specific HCI commands. The I2S interface shares the pins with the PCM interface. PCM and I2S interfaces are multiplexed with the chipset's TDM2 audio interface.

Figure 13 shows the transmitter timing for the Continuous Serial Clock (SCK), Word Select (WS) and Serial Data (SD) signaling for the transmitter.

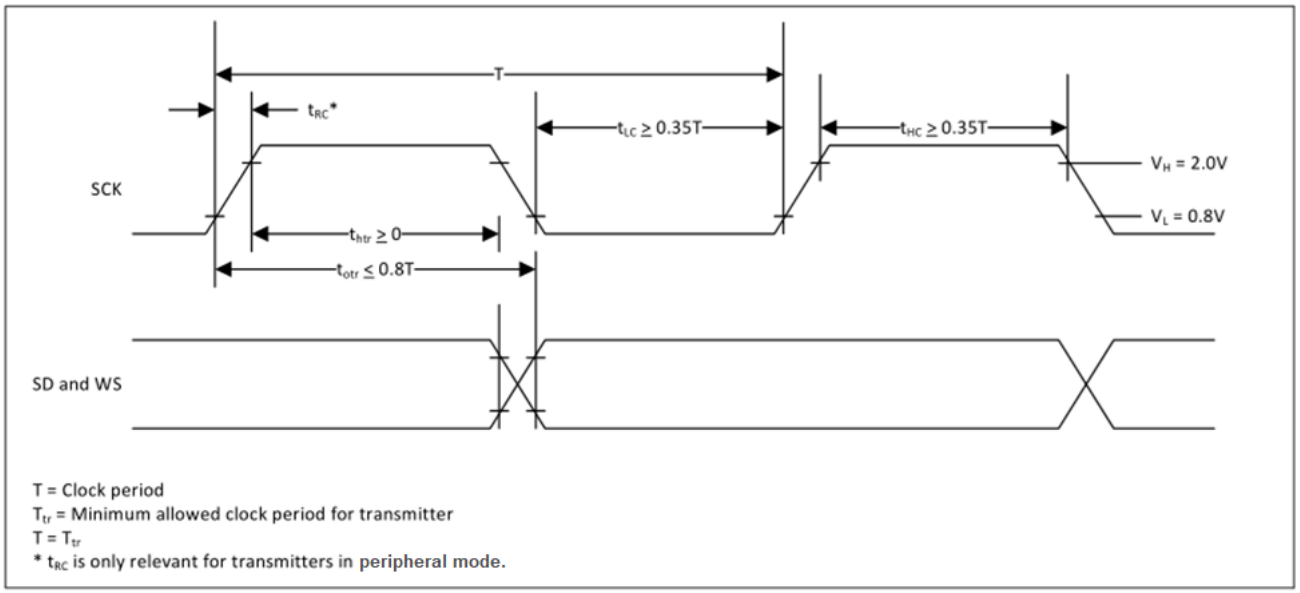


Figure 13: I2S transmitter timing

Figure 14 shows the transmitter timing for the Continuous Serial Clock (SCK), Word Select (WS) and Serial Data (SD) signaling for the receiver.

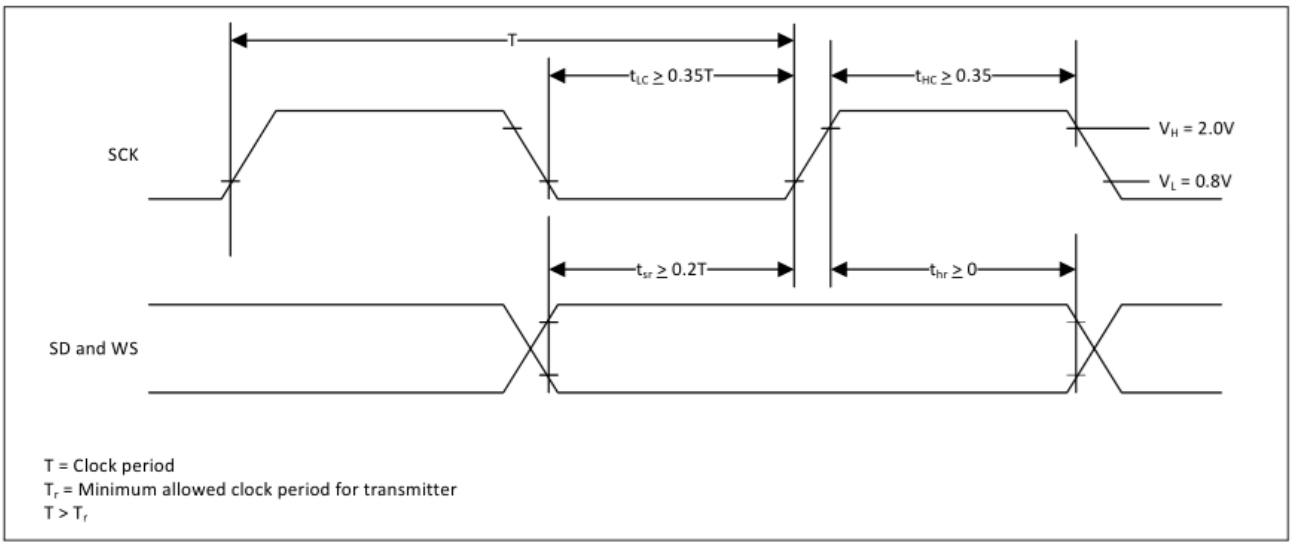


Figure 14: I2S receiver timing

2.9 Coexistence interfaces

External coexistence interfaces enable signaling between the internal radios and external co-located wireless devices for optimal performance when sharing the wireless medium.

External radios can be connected to the:

- 4-wire LTE coexistence interface
- 2-wire wireless coexistence interface 2 (WCI-2)
- 3-wire Zigbee/Ultra-wide band (UWB) coexistence interface

WCI-2 message format and message type comply with Bluetooth special interest group (SIG) core specification volume 7, part C.

Table 16 describes each of the pins supported on the 4-wire LTE coexistence interface.

Pin name	I/O type	Description	GPIO pin multiplexing
FRAME_SYNC	I	Frame sync pulse every 10 ms frame boundary	GPIO[2]
LTE_TX_IN	I	Advanced notice of upcoming LTE TX activity	GPIO[3]
LTE_RX_IN	I	Advanced notice of upcoming LTE RX activity	GPIO[4]
WL_PRIORITY	O	Indication of Bluetooth or WLAN priority. LTE to back off transmission for the duration of this event.	GPIO[5]

Table 16: 4-wire LTE external coexistence interface description

Table 17 describes each of the pins supported on the 2-wire WCI-2 interface.

Pin name	I/O type	Description	GPIO pin multiplexing
WCI-2_SIN	I	WCI-2 serial interface input	GPIO[4]
WCI-2_SOUT	O	WCI-2 serial interface output	GPIO[5]

Table 17: WCI-2 external coexistence interface description

Table 18 describes each of the pins supported on the 3-wire Zigbee/UWB interface.

Pin name	I/O type	Description	GPIO pin multiplexing
RF_ACTIV	I	Request for the medium	GPIO[2]
PRIORITY	I	Priority of the medium	GPIO[3]
TXCONF	O	Grant/deny	GPIO[5]

Table 18: 3-wire Zigbee/UWB external coexistence interface description

2.10 JTAG

The module includes a JTAG test interface that is supported using the GPIO pins, as described in Table 19.

Pin name	I/O type	Description	GPIO pin multiplexing
JTAG_SEL	I	JTAG select input: • Pull high to select JTAG interface • Pull down if the JTAG interface is not used Internal 4.7kΩ pull-down resistor on this pin	-
JTAG_TCK	I	JTAG test clock input signal	GPIO[2]
JTAG_TMS	I	JTAG controller select input signal	GPIO[3]
JTAG_TDI	I	JTAG test data input signal	GPIO[4]
JTAG_TDO	O	JTAG test data output signal	GPIO[5]
JTAG_TRST_L	I	JTAG test reset signal	GPIO[6]

Table 19: JTAG interface description

3 Pin definition

3.1 Pin assignment

Figure 15: MAYA-W3 series pin assignment (top view)

All signal pins are mounted in a land grid array (LGA) package on the bottom side of the PCB. The RF pins are not available on all module variants that support U.FL connectors.

No.	Name	I/O[4]	Description	Alt. functions	Power domain
A1	GND	-	Ground		
A2	1V8	-	1.8 V supply		1V8
A3	SD_DAT[1]	I/O	SDIO data 1	gSPI mode : GSPI_IRQ	1V8
A4	SD_CLK	I	SDIO clock	gSPI mode : GSPI_CLK	1V8
A5	SD_DAT[3]	I/O	SDIO data 3	gSPI mode : GSPI_CS	1V8
A6	NC	-	-		
A7	3V3	-	3.3 V supply		3V3
A8	NC	-	-		
A9	GND	-	Ground		
B1	SLP_CLK_IN_OUT	I/O	Sleep clock. Based on configuration can be: • As an external 32 kHz clock source input • As a 32 kHz clock output if crystal is connected to SLP_XTAL_IN and SLP_XTAL_OUT		1V8
B2	GND	-	Ground		
B3	SD_DAT[0]	I/O	SDIO data 0	gSPI mode : GSPI_MISO	1V8
B4	SD_CMD	I/O	SDIO command	gSPI mode : GSPI_MOSI	1V8
B5	SD_DAT[2]	I/O	SDIO data 2 Also used as boot strap pin for Interface configuration: 1-SDIO, 0-gSPI mode		1V8
B6	GPIO[5]	I/O	Wi-Fi GPIO	WCI-2 mode: WCI_SIN LTE_Coex mode: WL_PRIORITY ZB/UWB_Coex mode: TXCONF GPIO mode: GPIO[5]	1V8
B7	3V3	-	3.3 V supply		3V3
B8	GND	-	Ground		
B9	MIC_P	AI	Analog microphone input		
C1	SMIF_SPHB_DQ3	I/O	SMIF Data line 3		1V8
C2	SLP_XTAL_IN	I	Clock input for external crystal (32.768 kHz)		
C3	BT_GPIO[4]	I/O	Bluetooth GPIO		1V8
C4	GPIO[3]	I/O	Wi-Fi GPIO	LTE_Coex mode: LTE_TX_IN ZB/UWB_Coex mode: PRIORITY JTAG mode: JTAG_TMS	1V8
C5	GPIO[2]	I/O	Wi-Fi GPIO	LTE_Coex mode: FRAME_SYNC ZB/UWB_Coex mode: RF_ACTIV JTAG mode: JTAG_TCK	1V8
C6	GPIO[4]	I/O	Wi-Fi GPIO	WCI-2 mode : WCI_SOUT LTE_Coex mode: LTE_RX_IN JTAG mode: JTAG_TDI	1V8
C7	BT_GPIO[5]	I/O	Bluetooth GPIO		1V8

[4] I/O notations: I=Input, O=Output, I/O=Input or Output, PU=Pull Up, PD=Pull Down, D=Default, PP=Push-Pull, OD=Open Drain, AI/AO=Analog Input/Output, NC=Not Connected.

No.	Name	I/O[4]	Description	Alt. functions	Power domain
C8	BT_GPIO[7]	I/O	Bluetooth GPIO		1V8
C9	DMIC_CK	I/O	Digital microphone clock		
D1	SMIF_SPHB_CK	O	SMIF Clock output		1V8
D2	SLP_XTAL_OUT	O	Clock output for external crystal (32.768 kHz)		
D3	BT_GPIO[16]	I/O	Bluetooth GPIO		1V8
D4	BT_GPIO[2]	I/O	Bluetooth GPIO		1V8
D5	BT_GPIO[3]	I/O	Bluetooth GPIO		1V8
D7	BT_GPIO[6]	I/O	Bluetooth GPIO		1V8
D8	PCM_CLK	I/O	PCM data clock	I2S mode: I2S_BCLK	1V8
D9	DMIC_DQ	I/O	Digital microphone data		
E1	SMIF_SPHB_DQ0	I/O	SMIF Data line 0		1V8
E2	BT_GPIO[0]	I/O	Bluetooth GPIO		1V8
E3	BT_GPIO[17]	I/O	Bluetooth GPIO		1V8
E4	GND	-	Ground		
E5	GND	-	Ground		
E7	BT_HOST_WAKE	O	Bluetooth to host wake-up output signal		1V8
E8	PCM_MCLK	I/O	PCM clock output signal (optional)	I2S mode: I2S_CCLK	1V8
E9	PCM_DIN	I/O	PCM data input signal	I2S mode: I2S_DIN	1V8
F1	SMIF_SPHB_DQ2	I/O	SMIF Data line 2		
F2	LHL_GPIO[9]	I/O	Miscellaneous GPIO		1V8
F3	LHL_GPIO[8]	I/O	Miscellaneous GPIO		1V8
F4	GND	-	Ground		
F5	GND	-	Ground		
F7	WL_HOST_WAKE	O	Wi-Fi radio to host wake-up output signal		1V8
F8	PCM_SYNC	I/O	PCM frame sync	I2S mode: I2S_LRCLK	1V8
F9	PCM_DOUT	I/O	PCM data output signal	I2S mode: I2S_DOUT	1V8
G1	SMIF_SPHB_DQ1	I/O	SMIF Data line 1		
G2	LHL_GPIO[6]	I/O	Miscellaneous GPIO		1V8
G3	LHL_GPIO[5]	I/O	Miscellaneous GPIO		1V8
G4	RF_CNTL5	O	RF control		3V3
G5	RF_CNTL3	O	RF control Do not connect for MAYA-W3x2/3x3/3x6		3V3
G7	GPIO[6]	I/O	Wi-Fi GPIO	JTAG mode: JTAG_TRST	1V8
G8	UART_RX	I	UART serial data input		1V8
G9	UART_TX	O	UART serial data output		1V8
H1	SMIF_SPHB_CS0n	O	SMIF Chip select 0 active-low signal		1V8
H2	LHL_GPIO[4]	I/O	Miscellaneous GPIO		1V8
H3	LHL_GPIO[3]	I/O	Miscellaneous GPIO		1V8
H4	GND	-	Ground		
H5	GND	-	Ground		

No.	Name	I/O[4]	Description	Alt. functions	Power domain
H7	JTAG_SEL	I	JTAG select input: • Pull high to select JTAG interface • Pull down if the JTAG interface is not used • Internal 4.7kΩ pull-down resistor on this pin		1V8
H8	UART_CTSn	I	UART clear-to-send. Active-low clear-to-send signal for HCI UART interface		1V8
H9	UART_RTSn	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface		1V8
J1	SMIF_SPHB_CS1n	O	SMIF Chip select 1 active-low signal		1V8
J2	LHL_GPIO[2]	I/O	Miscellaneous GPIO		1V8
J3	WL_EN	I	Power Up or Power Down Signal for Wi-Fi section of the chipset (like a reset) 0 - power-down mode 1 - normal mode This pin has an internal 50 kΩ pull-down resistor that is enabled by default. It can be disabled through programming		1V8
J4	RF_CNTL0	O	RF control		3V3
J5	RF_CNTL4	O	RF control		3V3
J7	BT_EN	I	Power Up or Power Down Signal for Bluetooth section of the chipset (like a reset) 0 - power-down mode 1 - normal mode This pin has an internal 50 kΩ pull-down resistor that is enabled by default. It can be disabled through programming		1V8
J8	WL_DEV_WAKE	I	Wi-Fi radio wake-up signal		1V8
J9	BT_DEV_WAKE	I	Bluetooth radio wake-up signal		1V8
K1	RF_ANT0	RF	External antenna pin for Bluetooth I/O on MAYA-W3x1 Others: NC See also Antenna interfaces		
K2	GND	-	Ground		
K3	GND	-	Ground		
K4	GND	-	Ground		
K5	GND	-	Ground		1V8
K6	GND	-	Ground		
K7	GND	-	Ground		
K8	GND	-	Ground		
K9	RF_ANT1	RF	External antenna pin: • MAYA-W3x1: Wi-Fi I/O • MAYA-W3x3, and MAYA-W3x6: Combined Bluetooth and Wi-Fi I/O • Others: NC See also Antenna interfaces		
L1	GND	-	Ground		

No.	Name	I/O[4]	Description	Alt. functions	Power domain
L9	ANT_EXT_FEED	RF	Antenna feed pin for embedded PCB antenna on MAYA-W3x6 Others: NC See also Antenna interfaces		
M1	GND	-	Ground		
M2	GND	-	Ground		
M8	GND	-	Ground		
M9	GND	-	Ground		

Table 20: MAYA-W3 series pin description

4 Electrical specifications

⚠ Stressing the device above one or more of the ratings of the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these ratings or in conditions other than those specified in the Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

4.1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Units
3V3	Power supply voltage	-0.5	6.0	V
1V8	Power supply voltage 1.8 V	-0.5	2.2	V
$T_{STORAGE}$	Storage temperature	-40	+85	°C

Table 21: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specifications given in Table 21 must be limited to values within the specified boundaries by using appropriate protection devices.

4.1.1 Maximum ESD ratings

MAYA-W3 modules are manufactured using a highly automated process, which complies with IEC61340-5-1 (STM5.2-1999 Class M1 devices) standard. Customer on-site manufacturing processes that satisfy the basic ESD control program are sufficient to comply with the necessary precautions[5] for handling the modules.

Table 22 describes the target ESD ratings of the MAYA-W3 pins – subject to module qualification.

Applicability	Min.	Max.	Units
Human Body Model (HBM), ANSA/ESDA/JEDEC JS-001-2014.	-2000	+2000	V
Charged Device Model (CDM), JESD22-C101.	-500	+500	V

Table 22: ESD immunity rating for pins of the MAYA-W3 module

4.2 Recommended operating conditions

Symbol	Parameter	Min.	Typ	Max.	Units
3V3	Power supply voltage	3.13	3.3	3.6	V
1V8	Power supply voltage 1.8 V	1.71	1.80	1.89	V
T_A	Ambient operating temperature[6]	-40		+85	°C
T_J	Junction temperature	-40		125	°C

Table 23: Operating conditions

[5] Minimum ESD protection level for safe handling is specified in JEDEC JEP155 (HBM) and JEP157 (CDM) for ±500 V and ±250 V respectively.

[6] The device is functional across this range of temperature. The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

4.3 Digital pad ratings

Symbol	Parameter	VIO	Min.	Max.	Units
V_{IH}	Input high voltage	1.8V	0.65×VIO	-	V
V_{IL}	Input low voltage	1.8V		0.35×VIO	V
V_{HYS}	Input hysteresis	1.8V	100	-	mV
V_{OH}	Output high voltage	1.8V	VIO-0.4	-	V
V_{OL}	Output low voltage	1.8V	-	0.45	V

Table 24: DC characteristics

4.4 WL_EN/BT_EN pad ratings

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	1.2	-	-	V
V_{IL}	Input low voltage	GND	-	0.3	V
R_{PD}	Pull-down resistor	-	50	-	kΩ

Table 25: DC characteristics WL_EN/BT_EN pins

4.5 Sleep clock

MAYA-W3 series requires a 32.768 kHz reference oscillator for the sleep clock, used for low-power mode timing. The possible sleep clock configurations are:

- Internal low-power oscillator[7]
- External 32.768 kHz crystal connected to **SLP_XTAL_IN** and **SLP_XTAL_OUT**. If the external crystal is not used, **SLP_XTAL_IN** should be connected to ground.
- External 32.768 kHz clock connected to **SLP_CLK_IN_OUT**. If the external clock is not used, **SLP_CLK_IN_OUT** should be connected to ground.

The external 32.768 kHz low-power oscillator must meet the requirements described in Table 26.

Parameter	LPO clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	> 100k	Ω
	< 5	pF
Clock jitter (during initial startup)	< 10,000	ppm

Table 26: External LPO specifications

[7] The internal low-power oscillator accuracy is only adequate for WLAN, and not for Bluetooth.

4.6 Power consumption

4.6.1 Wi-Fi power consumption

Conditions: 25 °C, **1V8**=1.8 V, **3V3**=3.3 V, SDIO-UART Host Interface configuration, SDIO 3.0 SDR50 (4-bit mode), Bluetooth is OFF (BT_EN is LOW), TX power at module antenna port, unless otherwise specified.

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]
Power – save modes		
Power down (WL_EN, BT_EN both LOW)	0.0003	0.0005
Sleep	0.054	0.010
IEEE Power Save DTIM 10, 2G	0.111	0.010
IEEE Power Save DTIM 3, 2G	0.230	0.014
IEEE Power Save DTIM 1, 2G	0.560	0.028
IEEE Power Save DTIM 10, 5G	0.100	0.010
IEEE Power Save DTIM 3, 5G	0.188	0.013
IEEE Power Save DTIM 1, 5G	0.435	0.023
IEEE Power Save DTIM 10, 6G	0.100	0.009
IEEE Power Save DTIM 3, 6G	0.195	0.012
IEEE Power Save DTIM 1, 6G	0.460	0.023
Active transmit modes for 2G Wi-Fi operation		
DSSS/CCK, Ch7, 100% duty cycle, 18 dBm	240	5.2
OFDM, BPSK, 1/2, Ch7, 100% duty cycle, 18 dBm	250	5.2
OFDM, 64-QAM, 5/6, Ch7, 100% duty cycle, 16 dBm	210	5.2
OFDM, 1024-QAM, 5/6, Ch7, 100% duty cycle, 14 dBm	190	5.2
Active transmit modes for 5G Wi-Fi operation		
OFDM, BPSK, 1/2, Ch40/U-NII-1, 100% duty cycle, 16 dBm	340	5.2
OFDM, 64-QAM, 5/6, Ch40/U-NII-1, 100% duty cycle, 14 dBm	300	5.2
OFDM, 1024-QAM, 5/6, Ch40/U-NII-1, 100% duty cycle, 9 dBm	230	5.2
OFDM, BPSK, 1/2, Ch60/U-NII-2A, 100% duty cycle, 16 dBm	330	5.2
OFDM, 64-QAM, 5/6, Ch60/U-NII-2A, 100% duty cycle, 14 dBm	280	5.2
OFDM, 1024-QAM, 5/6, Ch60/U-NII-2A, 100% duty cycle, 9 dBm	230	5.2
OFDM, BPSK, 1/2, Ch144/U-NII-2C, 100% duty cycle, 16 dBm	300	5.2
OFDM, 64-QAM, 5/6, Ch144/U-NII-2C, 100% duty cycle, 14 dBm	260	5.2
OFDM, 1024-QAM, 5/6, Ch144/U-NII-2C, 100% duty cycle, 9 dBm	220	5.2
OFDM, BPSK, 1/2, Ch157/U-NII-3, 100% duty cycle, 16 dBm	310	5.2
OFDM, 64-QAM, 5/6, Ch157/U-NII-3, 100% duty cycle, 14 dBm	270	5.2
OFDM, 1024-QAM, 5/6, Ch157/U-NII-3, 100% duty cycle, 9 dBm	220	5.2
Active transmit modes for 6G Wi-Fi operation		
OFDM, BPSK, 1/2, Ch89/U-NII-5, 100% duty cycle, 16 dBm	390	5.2
OFDM, 64-QAM, 5/6, Ch89/U-NII-5, 100% duty cycle, 14 dBm	340	5.2
OFDM, 1024-QAM, 5/6, Ch89/U-NII-5, 100% duty cycle, 9 dBm	260	5.2
OFDM, BPSK, 1/2, Ch105/U-NII-6, 100% duty cycle, 16 dBm	390	5.2
OFDM, 64-QAM, 5/6, Ch105/U-NII-6, 100% duty cycle, 14 dBm	340	5.2
OFDM, 1024-QAM, 5/6, Ch105/U-NII-6, 100% duty cycle, 9 dBm	270	5.2
OFDM, BPSK, 1/2, Ch121/U-NII-7, 100% duty cycle, 16 dBm	380	5.2
OFDM, 64-QAM, 5/6, Ch121/U-NII-7, 100% duty cycle, 14 dBm	330	5.2
OFDM, 1024-QAM, 5/6, Ch121/U-NII-7, 100% duty cycle, 9 dBm	260	5.2

Wi-Fi operation modes	3V3 (3.3V) [mA]	1V8 (1.8 V) [mA]
OFDM, BPSK, 1/2, Ch233/U-NII-8, 100% duty cycle, 16 dBm	350	5.2
OFDM, 64-QAM, 5/6, Ch233/U-NII-8, 100% duty cycle, 14 dBm	310	5.2
OFDM, 1024-QAM, 5/6, Ch233/U-NII-8, 100% duty cycle, 9 dBm	250	5.2
Receive modes for 2G Wi-Fi operation		
DSSS 1Mbps	31.2	0.9
OFDM, BPSK, 1/2	31.5	0.9
OFDM, 1024-QAM, 5/6	32.8	0.9
Receive modes for 5G Wi-Fi operation		
OFDM, BPSK, 1/2	40.3	0.9
OFDM, 1024-QAM, 5/6	42.3	0.9
Receive modes for 6G Wi-Fi operation		
OFDM, BPSK, 1/2	44.1	0.9
OFDM, 1024-QAM, 5/6	44.9	0.9
Maximum Peak current (at room temperature)		
Receive mode	50	1.0
Active transmission	480	5.4
Firmware initialization / self-calibration	850	10.0

Table 27: Wi-Fi radio typical current consumption with different modes of operation

4.6.2 Bluetooth power consumption

Conditions: 25 °C, **1V8**=1.8 V, **3V3**=3.3 V, SDIO-UART Host Interface configuration, WLAN section is in reset state (**WL_EN**=low), TX power at module antenna port, unless otherwise specified.

Bluetooth operation modes	3V3 (3.3 V) [mA]	1V8 (1.8 V) [mA]
Operating modes		
Sleep	0.032	0.008
Bluetooth classic inquiry scan	0.136	0.011
500 ms sniff central	0.110	0.011
Bluetooth LE advertisement (interval = 1.28 s)	0.111	0.009
Bluetooth LE advertisement (interval = 1.28 s, low-power TX)	0.070	0.009
Bluetooth TX BDR, 16 dBm	140	0.3
Bluetooth TX BDR, 13 dBm	105	0.3
Bluetooth TX BDR, 9 dBm	25	0.3
Bluetooth TX EDR, 9 dBm	155	0.3
Bluetooth TX EDR, 6 dBm	25	0.3
Bluetooth TX LE, 16 dBm	140	0.3
Bluetooth TX LE, 9 dBm	27	0.3
Bluetooth TX LE, 5 dBm	22	0.3
Active receive mode [1]		
Bluetooth, BDR, EDR	10.5	0.3
Bluetooth, LE	11.5	0.3

Table 28: Bluetooth typical current consumption with different modes of operation

4.7 Radio specification

4.7.1 Bluetooth

Parameter	Specification (typical values)
RF Frequency Range	2.402 – 2.480 GHz
Supported Modes	Bluetooth Core 6.0 Bluetooth Classic (BR/EDR) Bluetooth Low Energy (LE) • LE long range • Shared RF with BDR/EDR • 2 Mbps LE
Modulation	1 Mbit/s: GFSK (BR) 2 Mbit/s: π/4 DQPSK (EDR) 3 Mbit/s: 8DPSK (EDR)
Transmit Power	Class 1 BR: 16 dBm
	Class 1 EDR: 10 dBm
	Bluetooth LE: 16 dBm
Receiver sensitivity	Bluetooth BR 1DH1: -93 dBm
	Bluetooth EDR 2DH1: -95.5 dBm
	Bluetooth EDR 3DH1: -89.5 dBm
	Bluetooth LE 125 Kbps: -109.5 dBm Bluetooth LE 500 Kbps: -103.5 dBm Bluetooth LE 1M: -97.5 dBm Bluetooth LE 2M: -94.5dBm

Table 29: Bluetooth radio parameters

4.7.2 Wi-Fi

MAYA-W3 series modules support tri-band Wi-Fi with 802.11a/b/g/n/ac/ax operation in the 2.4 GHz, 5 GHz, and 6 GHz radio bands. The module is designed to operate in only one frequency band at a time.

Parameter	Operation mode	Specification
RF Frequency range	802.11b/g/n/ax	2.400 – 2.500 GHz
	802.11a/n/ac/ax	5.170 – 5.835 GHz
	802.11ax	5.945 – 7.125 GHz
Modulation	802.11b	CCK and DSSS
	802.11a/g/n/ac/ax	OFDM
Supported data rates	802.11b	1, 2, 5.5, 11 Mbps
	802.11a/g	6, 9, 12, 18, 24, 36, 48, 54 Mbps
	802.11n	MCS0 – MCS7
	802.11 ac	MCS0 – MCS8
	802.11.ax	MCS0 – MCS11
Supported channel bandwidth	802.11b/g	20 MHz
	802.11n	
	802.11ac/ax	
Supported guard interval (GI)	802.11ax	800, 1600, 3200 ns

Table 30: Wi-Fi radio parameters

Parameter	Band	Operation mode	802.11 EVM limit	Specification (typical values, ±2 dB) [8]
Maximum transmit power	2.4 GHz	DSSS/CCK	-9 dB	18 dBm
		OFDM, BPSK, 1/2	-5 dB	18 dBm
		OFDM, QPSK, 3/4	-13 dB	18 dBm
		OFDM, 16-QAM, 3/4	-19 dB	18 dBm
		OFDM, 64-QAM, 3/4	-25 dB	18 dBm
		OFDM, 64-QAM, 5/6	-27 dB	16 dBm
		OFDM, 256-QAM, 5/6	-32 dB	16 dBm
		OFDM, 1024-QAM, 5/6	-35 dB	14 dBm
	5 GHz 6 GHz	OFDM, BPSK, 1/2	-5 dB	16 dBm
		OFDM, QPSK, 3/4	-13 dB	16 dBm
		OFDM, 16-QAM, 3/4	-19 dB	16 dBm
		OFDM, 64-QAM, 3/4	-25 dB	14 dBm
		OFDM, 64-QAM, 5/6	-27 dB	14 dBm
		OFDM, 256-QAM, 5/6	-32 dB	12 dBm
		OFDM, 1024-QAM, 5/6	-35 dB	9 dBm

Table 31: Wi-Fi transmitter characteristics

Band	Operating mode	Data rate	Bandwidth	Specification (typical values) [6]
2.4 GHz	802.11b	1 Mbps / 2 Mbps	20 MHz	-99 dBm / -95 dBm
		5.5 Mbps / 11 Mbps		-94 dBm / -90 dBm
	802.11g	6 Mbps / 9 Mbps	20 MHz	-95 dBm / -93 dBm
		12 Mbps / 18 Mbps		-92 dBm / -90 dBm
		24 Mbps / 36 Mbps		-87 dBm / -84 dBm
		48 Mbps / 54 Mbps		-79 dBm / -78 dBm
	802.11n	MCS0 / MCS1	20 MHz	-95 dBm / -92 dBm
		MCS2 / MCS3		-90 dBm / -87 dBm
		MCS4 / MCS5		-83 dBm / -79 dBm
		MCS6 / MCS7		-77 dBm / -76 dBm
	802.11ax	MCS0 / MCS1	20 MHz	-94 dBm / -93 dBm
		MCS2 / MCS3		-91 dBm / -88 dBm
		MCS4 / MCS5		-85 dBm / -81 dBm
		MCS6 / MCS7		-79 dBm / -77 dBm
		MCS8 / MCS9		-74 dBm / -71 dBm
		MCS10 / MCS11		-67 dBm / -63 dBm
5 GHz	802.11a	6 Mbps/9 Mbps	20 MHz	-91 dBm / -90 dBm
		12 Mbps/18 Mbps		-89 dBm / -86 dBm
		24 Mbps/36 Mbps		-83 dBm / -80 dBm
		48 Mbps/54 Mbps		-76 dBm / -74 dBm
	802.11n	MCS0 / MCS1	20 MHz	-91 dBm / -88 dBm
		MCS2 / MCS3		-86 dBm / -83 dBm
		MCS4 / MCS5		-79 dBm / -75 dBm
		MCS6 / MCS7		-74 dBm / -72 dBm

[8] Values are valid at antenna pin ports and room temperature.

Band	Operating mode	Data rate	Bandwidth	Specification (typical values) [6]
	802.11ac	MCS0 / MCS1	20 MHz	-91 dBm / -88 dBm
		MCS2 / MCS3		-86 dBm / -83 dBm
		MCS4 / MCS5		-80 dBm / -76 dBm
		MCS6 / MCS7		-74 dBm / -72 dBm
		MCS8		-68 dBm
	802.11ax	MCS0 / MCS1	20 MHz	-91 dBm / -90 dBm
		MCS2 / MCS3		-87 dBm / -84 dBm
		MCS4 / MCS5		-81 dBm / -77 dBm
		MCS6 / MCS7		-75 dBm / -73 dBm
		MCS8 / MCS9		-69 dBm / -67 dBm
		MCS10 / MCS11		-63 dBm / -59 dBm
6 GHz	802.11ax	MCS0 / MCS1	20 MHz	-91 dBm / -90 dBm
		MCS2 / MCS3		-87 dBm / -85 dBm
		MCS4 / MCS5		-81 dBm / -77 dBm
		MCS6 / MCS7		-76 dBm / -74 dBm
		MCS8 / MCS9		-70 dBm / -68 dBm
		MCS10 / MCS11		-62 dBm / -59 dBm

Table 32: Wi-Fi receiver sensitivity

4.7.3 Antenna radiation patterns

The radiation patterns displayed in Table 33, Table 34, and Table 35 show the radiation patterns of MAYA-W3x6-00B with internal PCB trace antenna for 2.44 GHz, 5.5 GHz and 6.08 GHz. Table 36 shows the TRP and peak gain for the low, mid, and high channel of the 2.4 GHz, 5 GHz and 6 GHz frequency bands.

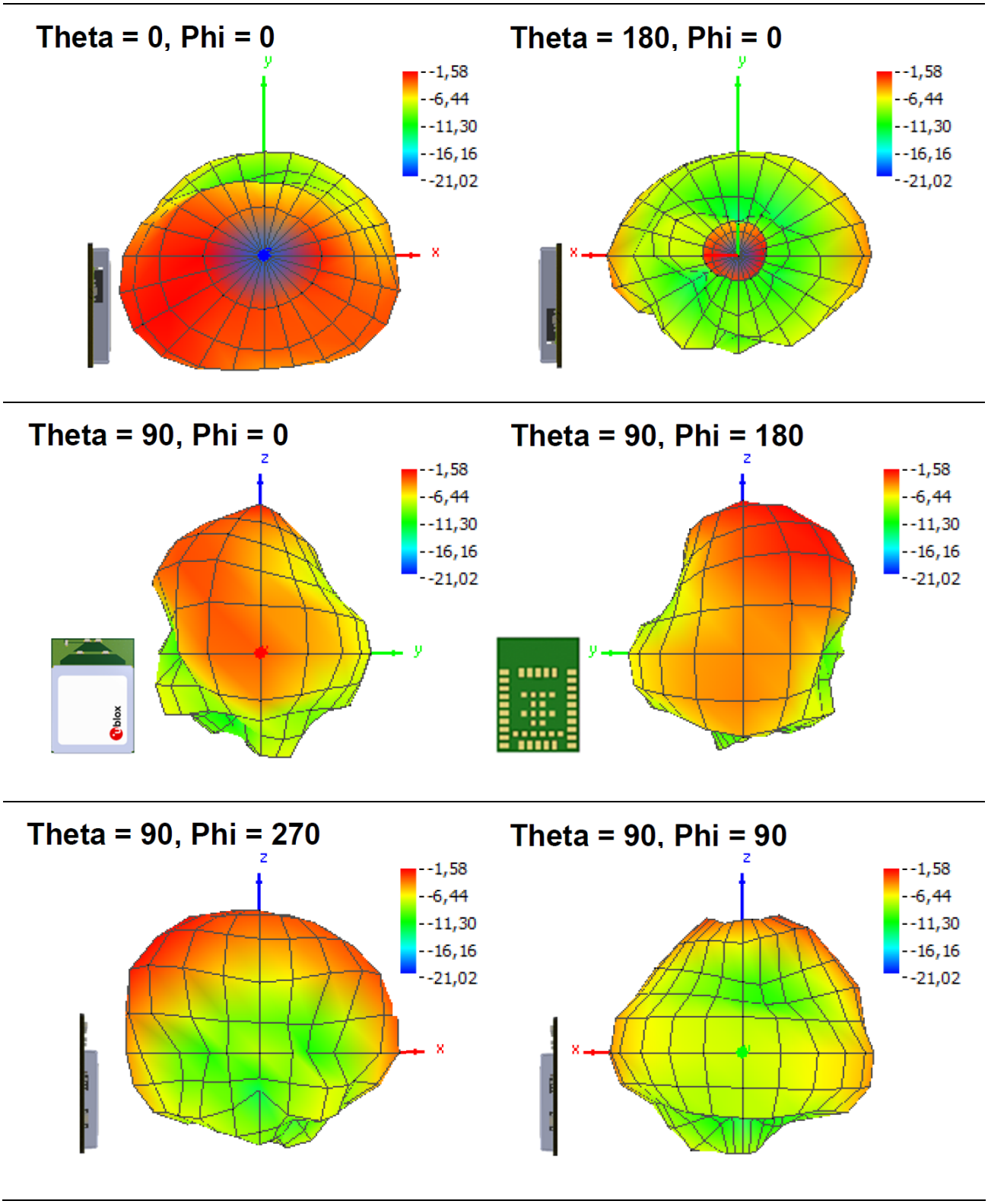


Table 33: MAYA-W3x6 Wi-Fi and Bluetooth antenna characteristics at 2.442 GHz

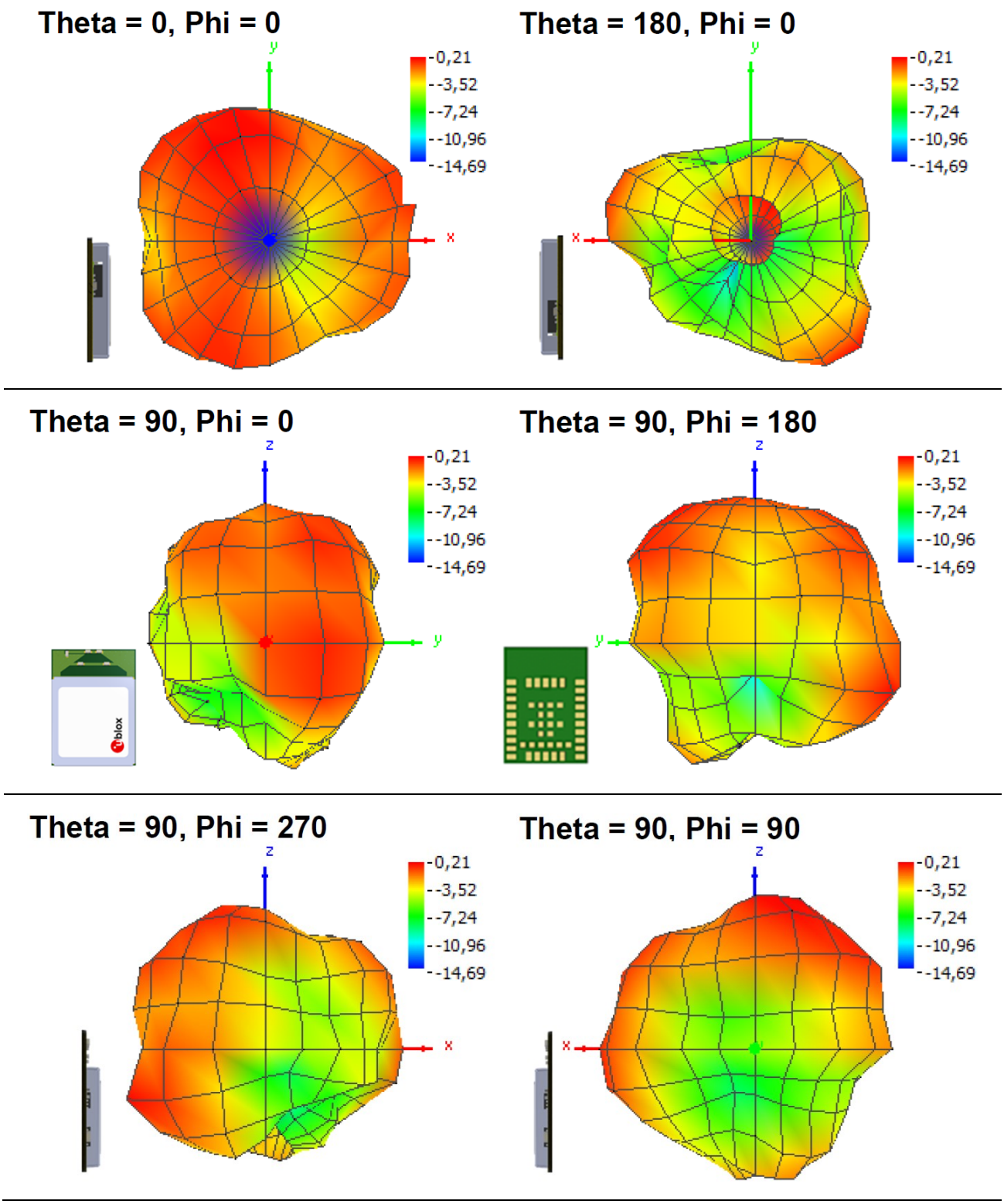


Table 34: MAYA-W3x6 Wi-Fi antenna characteristics at 5.500 GHz

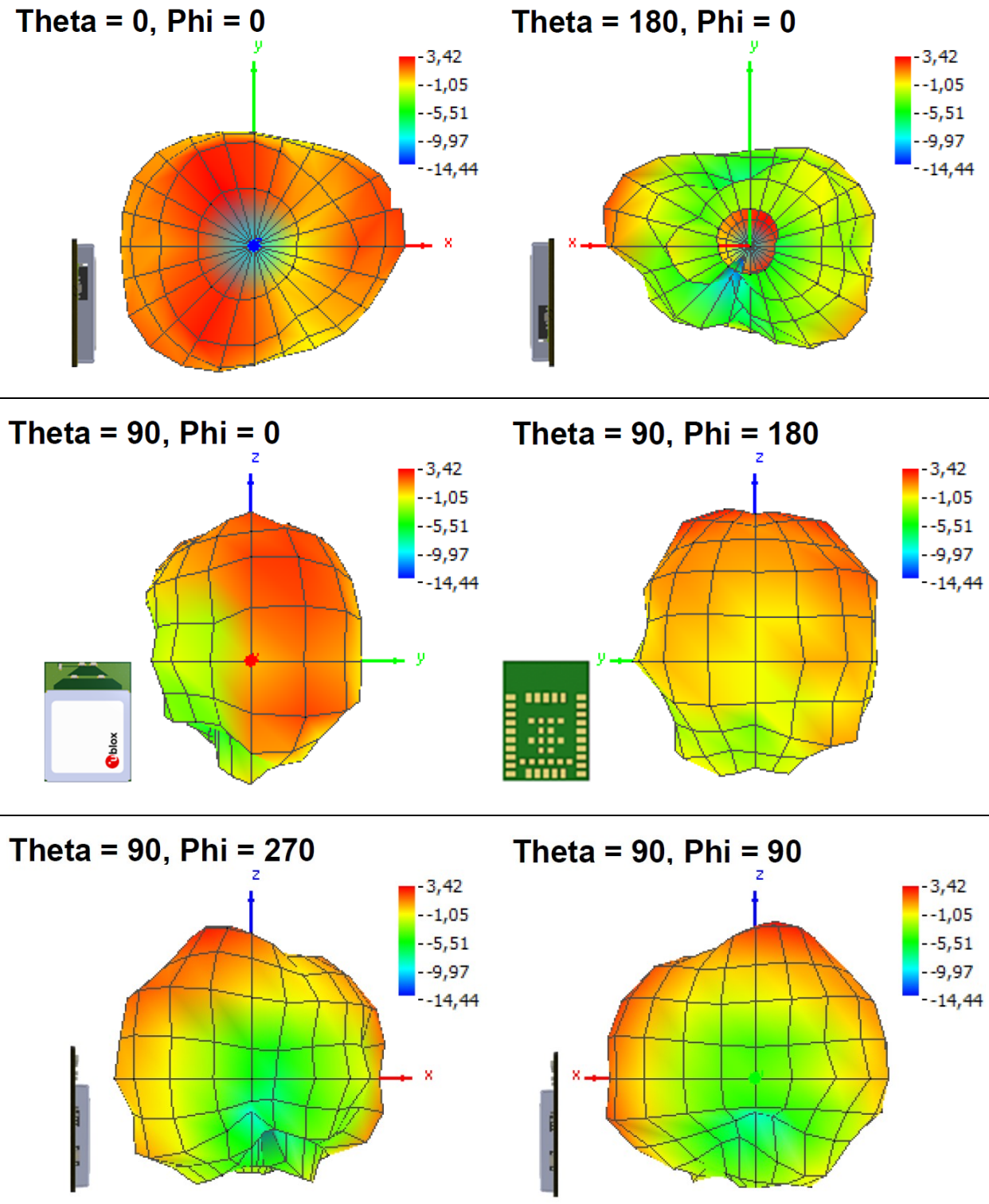


Table 35: MAYA-W3x6 Wi-Fi antenna characteristics at 6.075 GHz

Transmission	Measured TRP	Measured peak gain
2.4 GHz channel 1 (2.412 GHz)	-6.75 dBm	-1.34 dBi
2.4 GHz channel 7 (2.442 GHz)	-6.15 dBm	-1.58 dBi
2.4 GHz channel 13 (2.472 GHz)	-7.61 dBm	-2.83 dBi
5 GHz channel 36 (5.180 GHz)	-3.80 dBm	-0.71 dBi
5 GHz channel 100 (5.500 GHz)	-2.93 dBm	0.21 dBi
5 GHz channel 165 (5.825 GHz)	-1.26 dBm	2.41 dBi
6 GHz channel 25 (6.075 GHz)	-0.89 dBm	3.42 dBi
6 GHz channel 233 (7.115 GHz)	-4.34 dBm	0.39 dBi

Table 36: Measured total radiated power and peak gain for 0 dBm transmission power

5 Software support

MAYA-W3 series modules are based on the Infineon CYW5551x chipsets and the drivers and firmware required to operate the modules are developed by Infineon. A firmware binary is downloaded by the host operating system driver at start-up.

Linux/Android device drivers are available free of charge from the chipset manufacturer.

The software packages typically include:

- Dedicated kernel driver that binds the Wi-Fi device to the kernel. Driver sources are provided.
- Dedicated Wi-Fi firmware image that is uploaded during initialization of the Wi-Fi device.
- Dedicated Bluetooth firmware image that is uploaded during initialization of the Bluetooth device.
- Wi-Fi and Bluetooth release notes and a list of supported software features.
- Laboratory and manufacturing tools for RF testing.

6 Mechanical specifications

6.1 MAYA-W3 footprint dimensions

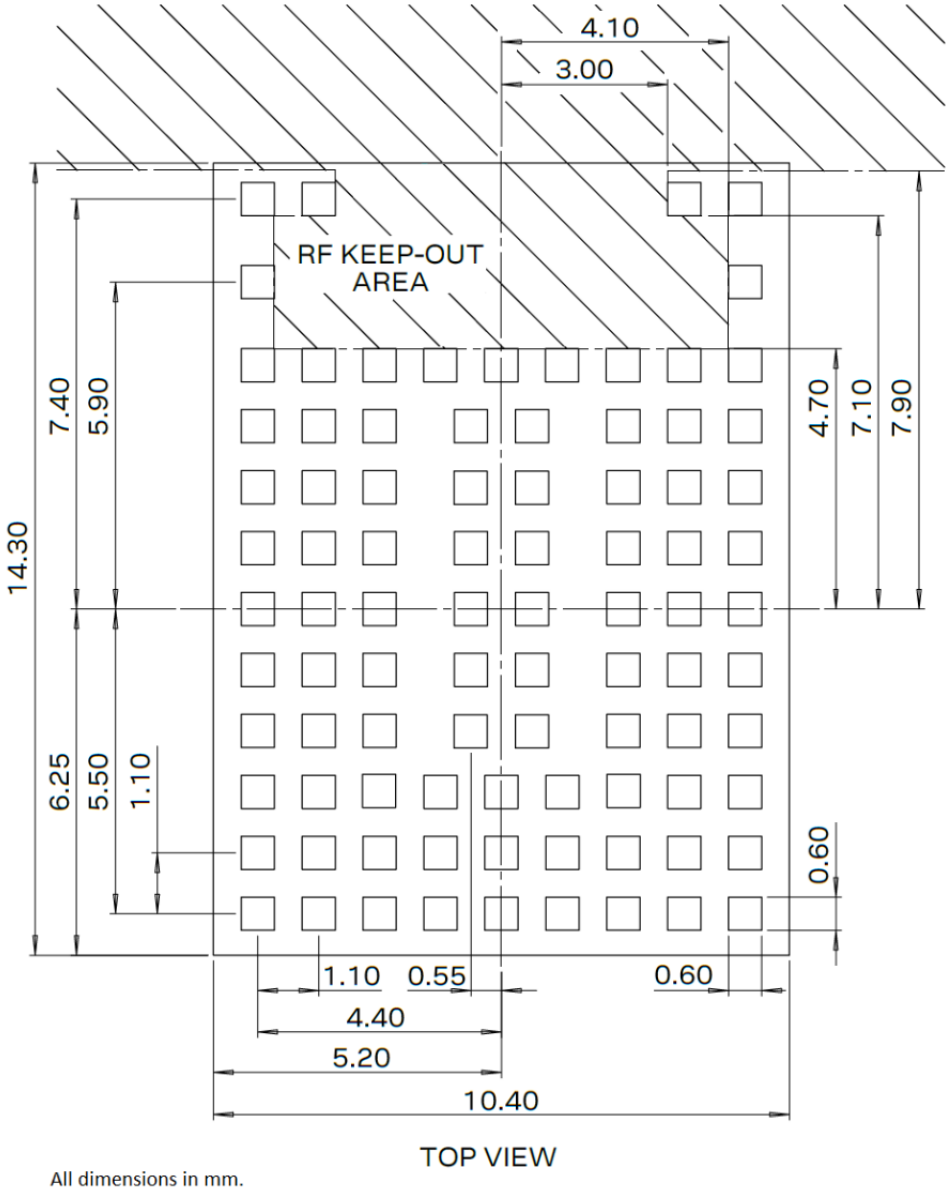


Figure 16: MAYA-W3 footprint dimensions

☞ The RF keep-out area is only required for MAYA-W3x6 modules

Parameter	Typical	Tolerance
Seating Plane Coplanarity [mm]	<0.1	
Pin Width [mm]	0.60	+0.015/-0.015
Pin Length [mm]	0.60	+0.015/-0.015

Table 37: Dimensions parameters

6.2 MAYA-W3 mechanical specification

6.2.1 MAYA-W3x6

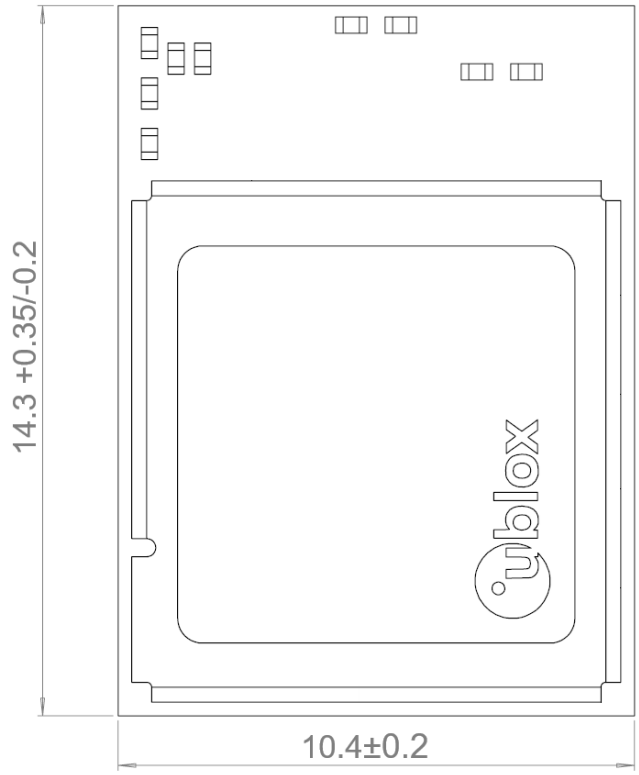


Figure 17: MAYA-W3x6 mechanical specifications (top view) - dimensions in mm

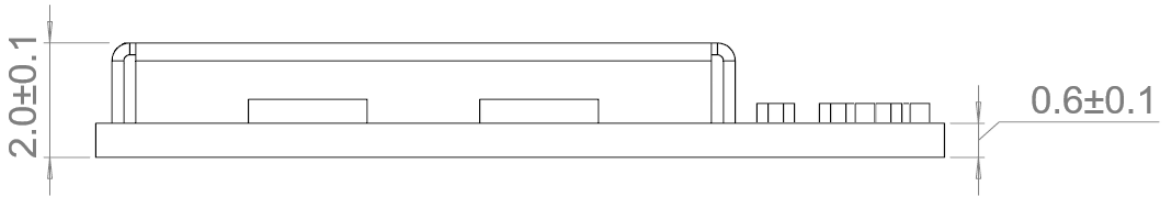


Figure 18: MAYA-W3x6 mechanical specification (side view) – dimensions in mm

6.2.2 MAYA-W3x1 and MAYA-W3x3

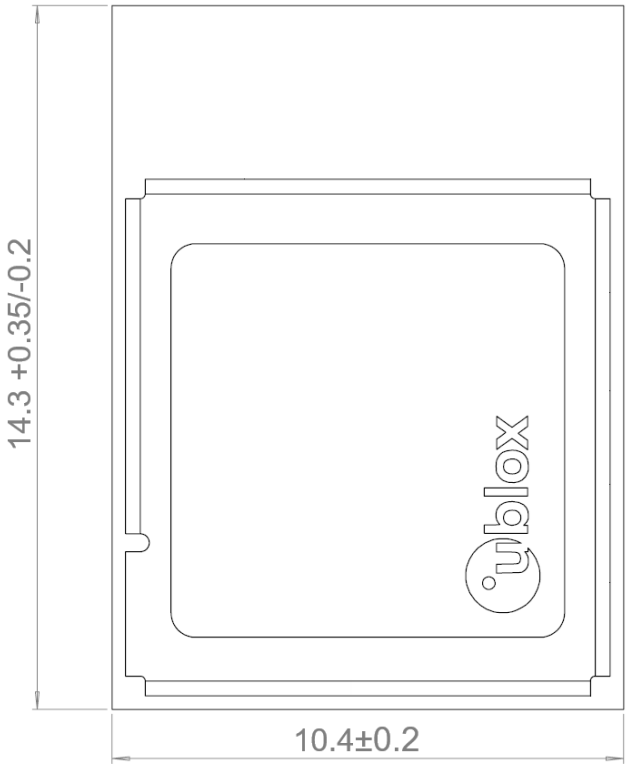


Figure 19: MAYA-W3x1/W3x3 mechanical specification (top view) - dimensions in mm

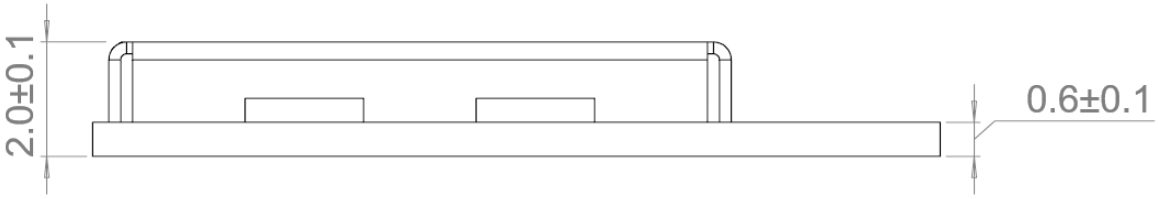


Figure 20: MAYA-W3x1/W3x3 mechanical specification (side view) - dimensions in mm

6.2.3 MAYA-W3x0

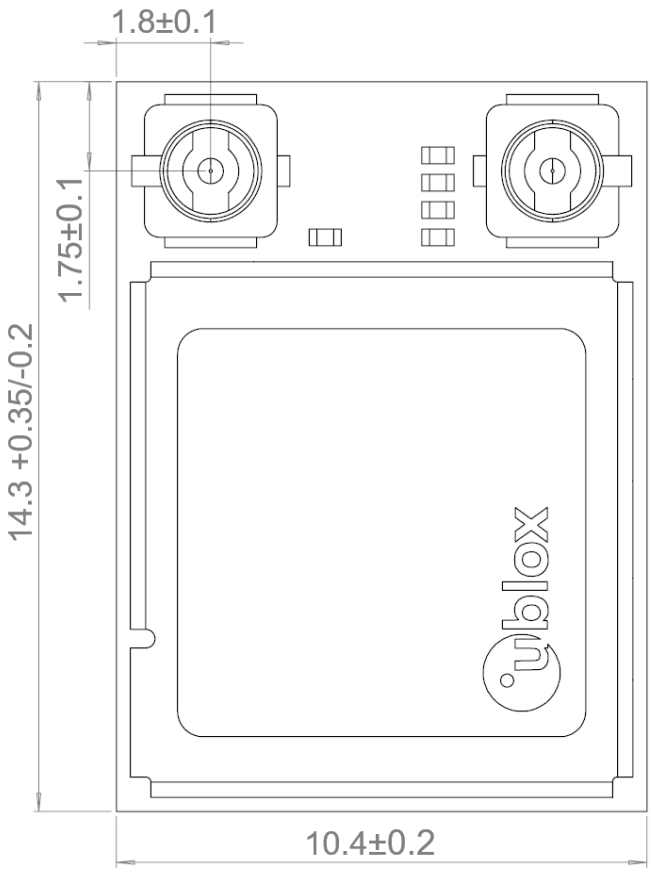


Figure 21: MAYA-W3x0 mechanical specification (top view) - dimensions in mm

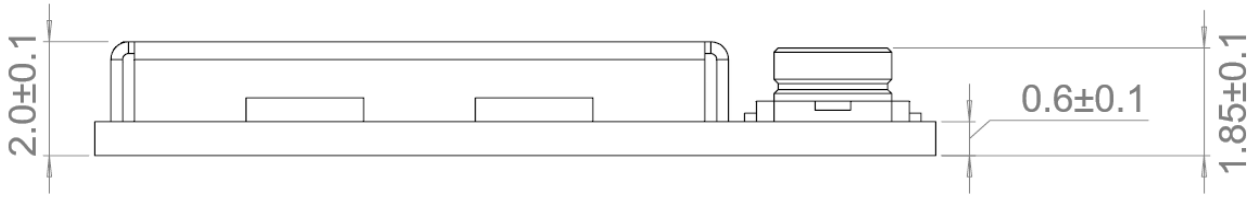


Figure 22: MAYA- W3x0 mechanical specification (side view) - dimensions in mm

6.2.4 MAYA-W3x2

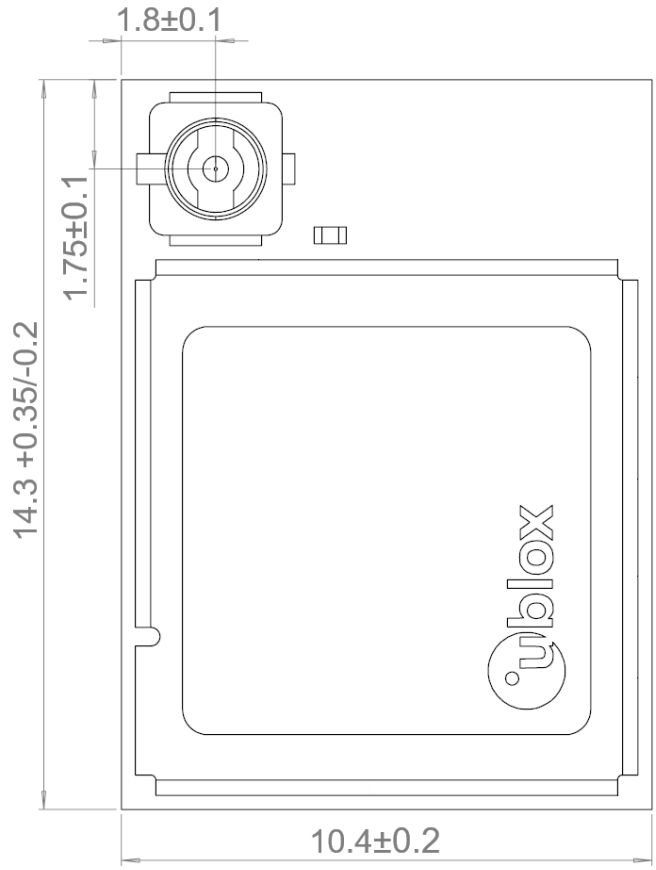


Figure 23: MAYA-W3x2 mechanical specification (top view) - dimensions in mm

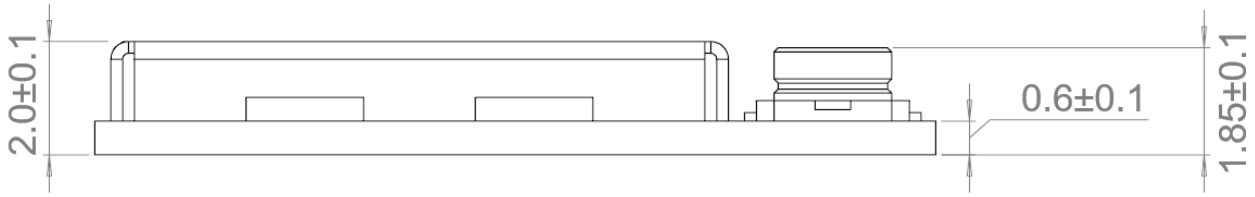


Figure 24: MAYA- W3x2 mechanical specification (Side View) - dimensions in mm

6.3 Module weight

Module	Typ	Unit
MAYA-W3xx	<1	g

Table 38: Module weight

7 Qualification and approvals

The MAYA-W3 module series is certified for use in the countries/regions shown in Table 39. Other country certifications can be scheduled on request.

Country/region	MAYA-W3x0	MAYA-W3x1	MAYA-W3x2	MAYA-W3x3	MAYA-W3x6
Europe (RED)	Planned	Approved	Approved	Approved	Approved
Great Britain (UKCA)	Planned	Approved	Approved	Approved	Approved
USA (FCC)	Planned	Approved	Approved	Approved	Approved
Canada (ISED)	Planned	Approved	Approved	Approved	Approved
Japan (Giteki)	Approved	Approved	Approved	Approved	Approved

Table 39: Certification status

For detailed information about the regulatory requirements that must be met when using MAYA-W3 modules in an end product, see the MAYA-W3 system integration manual [2].

7.1 Bluetooth qualification

End products must be qualified and listed with the Bluetooth Special Interest Group (SIG).

Product declarations are submitted through the Bluetooth Launch Studio website.

MAYA-W3 series modules are qualified as Core-Controller Configuration in accordance with the Bluetooth 6.0 specification.

To list your product that integrates MAYA-W3 with no additional testing required, combine the DN for the Bluetooth stack implemented in the Core-Host Configuration with the DN of the Core-Controller Configuration shown in Table 40.

Product name	Product type	DN	Product qualification date
MAYA-W381-00B, MAYA-W386-00B, MAYA-W380-00B, MAYA-W383-00B, MAYA-W382-00B, MAYA-W361-00B, MAYA-W366-00B, MAYA-W360-00B, MAYA-W363-00B, MAYA-W362-00B, MAYA-W331-00B, MAYA-W336-00B, MAYA-W330-00B, MAYA-W333-00B, MAYA-W332-00B	Core-Controller Configuration	Q371075	2025-09-01

Table 40: Bluetooth DN

All companies that use Bluetooth technology are requested to join the Bluetooth SIG. Bluetooth SIG membership is required to use the Bluetooth trademarks and logos. The Bluetooth SIG also requires all Bluetooth SIG members that place devices using Bluetooth technology on the market, to qualify and declare the device / device family.

8 Product handling

8.1 Packaging

MAYA-W3 series modules are delivered as hermetically sealed, reeled tapes to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the Product packaging guide [1].

8.1.1 Reels

MAYA-W3 series modules are deliverable in quantities of 500 pieces on a reel. MAYA-W3 series modules are shipped on reel Type A3 as described in the Product packaging guide [1].

8.1.2 Tapes

Figure 25 shows the position and orientation of MAYA-W3 series modules as they are delivered on tape. The dimensions of the tapes are specified in Figure 26.

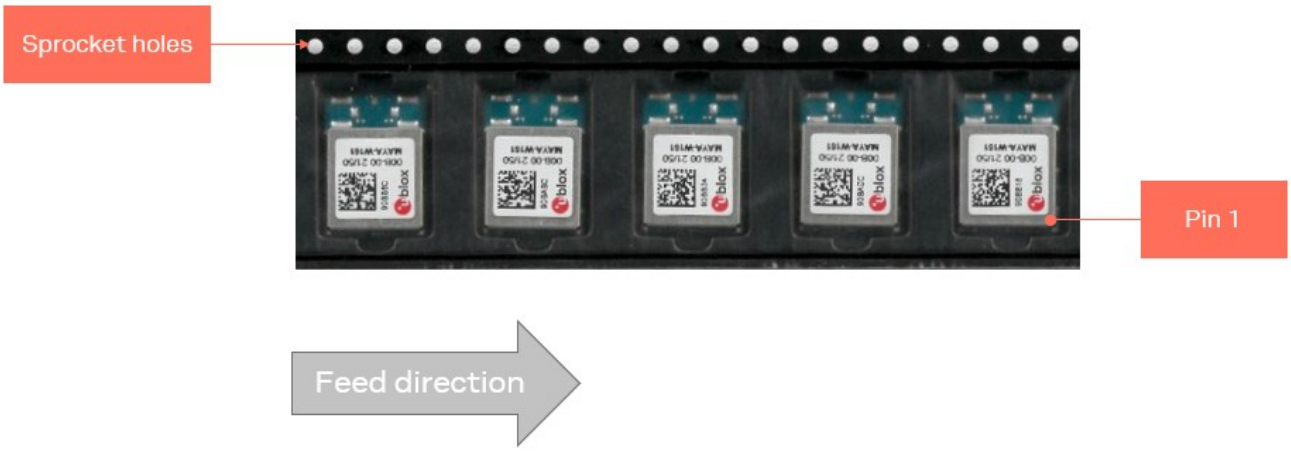
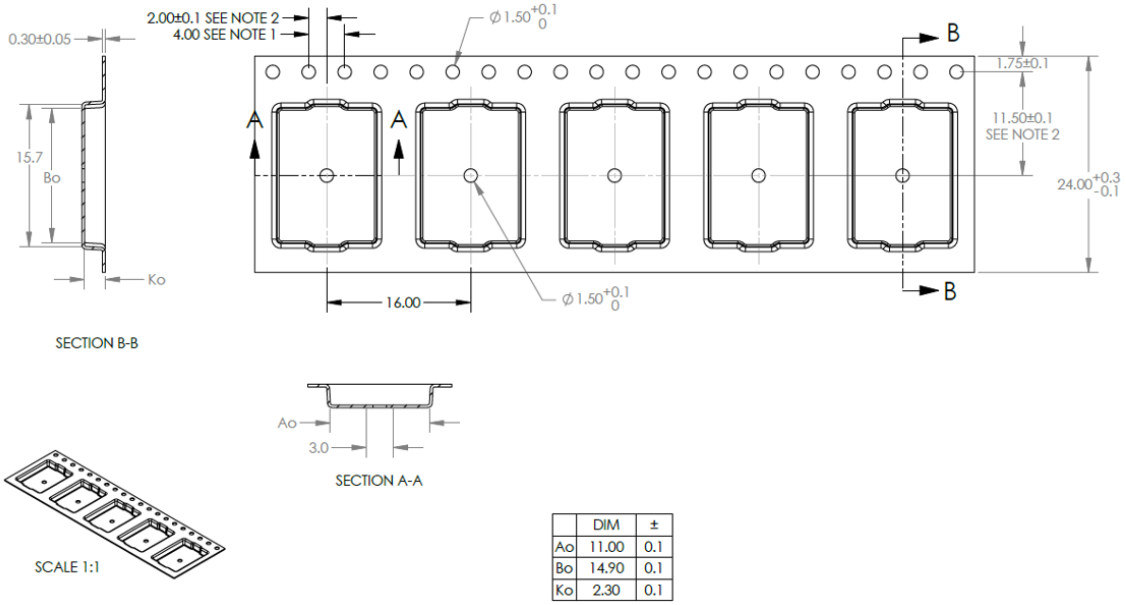


Figure 25: Orientation of MAYA-W3 modules on tape



	DIM	±
Ao	11.00	0.1
Bo	14.90	0.1
Ko	2.30	0.1

Figure 26: MAYA-W3 tape dimensions

8.2 Moisture sensitivity levels

⚠ MAYA-W3 series modules are rated as MSL Level 4 devices in accordance with the IPC/JEDEC J STD-020 standard. For detailed information, see the moisture sensitive warning label on the MBB (Moisture Barrier Bag).

After opening the dry pack, the modules must be mounted within 72 hours in factory conditions of maximum 30 °C/60%RH or must be stored at less than 10%RH. The modules require baking if the humidity indicator card shows more than 10% when read at 23±5 °C or if the conditions mentioned above are not met. For information about the bake procedure, see also the J-STD-033B standard.

For more information regarding MSL (Moisture Sensitivity Level), labeling, and storage, see also the Packaging information guide [1].

8.3 Reflow soldering

Reflow profiles must be selected in accordance with u-blox recommendations:

- The U.FL connector variants MAYA-W3x0 and MAYA-W3x2 are suitable for one time reflow
- Other MAYA-W3 variants are suitable for two time reflow

⚠ Reflow soldering profiles must be selected in accordance with u-blox soldering recommendations described in the system integration manual [2]. Failure to observe these recommendations can result in severe damage to the product.

8.4 ESD handling precautions

⚠ MAYA-W3 series modules are electrostatic sensitive devices (ESD) that demand adherence to special ESD precautions. Failure to observe these recommendations can result in severe damage to the product.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates MAYA-W3. We recommend that the module is not handled in a non-ESD protected environment. The RF pins (**RF_ANT0** and **RF_ANT1)** are especially sensitive to ESD, and special care must be taken when connecting antennas. ESD safe soldering equipment is recommended.

9 Labeling and ordering information

9.1 Product labeling

The labels applied to MAYA-W3 series modules include important product information. Figure 27 shows the given label information, where each of the given references are described in Table 41.

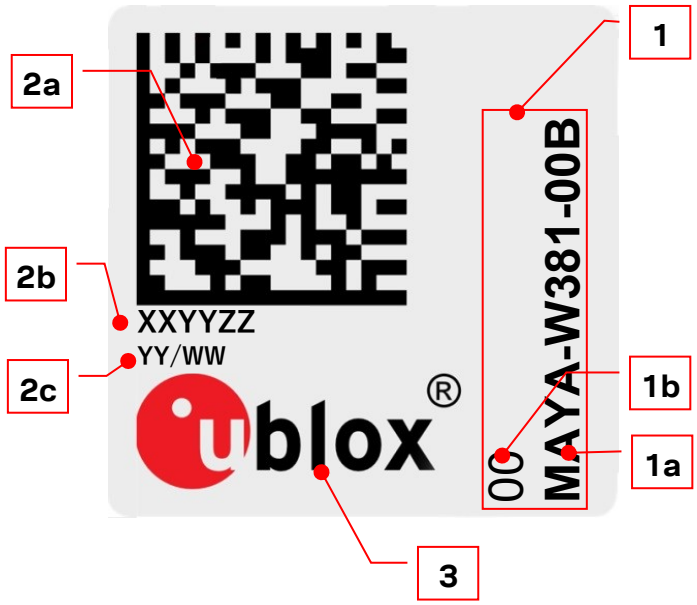


Figure 27: Label information shown on the MAYA-W3 series modules

Reference	Description
1	Text box containing product name and version
1a	Text MODEL: and Product name (ID)
1b	Product version
2a	Data Matrix with unique serial number of 19 alphanumeric symbols: • The first 3 symbols are used for production tracking and are an abbreviated representation of the Type number that is unique to each module variant. • The following 12 symbols represent the unique hexadecimal Bluetooth address of the module AABBCCDDEEFF. See also MAC addresses. • The last 4 symbols represent the hardware and firmware version encoded HHFF.
2b	The six last hex symbols in the MAC address (AABBCCDDEEFF)
2c	Date of production in the format YY/WW (year/week)
3	u-blox logo, where the red dot indicates the position of pin no 1

Table 41: MAYA-W3 series label references

9.2 Explanation of codes

Table 42 describes the product identifiers, namely the Type number, Model name and Ordering code.

Format	Description	Nomenclature
Product name	Describes the form factor, platform technology and platform variant. Used mostly in product documentation like this data sheet, the model name represents the most common identity for all u-blox products.	PPPP-TGVV
Ordering code	Comprises the model name – with additional identifiers to describe the major product version and quality grade.	PPPP -TGVV-TTQ
Type number	Comprises the model name and ordering code – with additional identifiers that describe minor product versions.	PPPP -TGVV-TTQ-XX

Table 42: Product code formats

9.3 Identification codes

Code	Meaning	Example
PPPP	Form factor	MAYA
TG	Platform (Technology and Generation) T – Dominant technology, For example, W: Wi-Fi, B: Bluetooth® G - Generation	W3: Wi-Fi, Generation 3
VV	Variant based on the same platform; range [00…99]	80, 81, 83, or 86
TT	Major Product Version	00: first version
Q	Quality grade A: Automotive B: Professional C: Standard	B: Professional grade
XX	Minor product version (not relevant for certification)	Default value: 00

Table 43: Part identification code

9.4 Ordering information

Ordering code	Product
MAYA-W380-00B	MAYA-W380 tri-band Wi-Fi 6E and Bluetooth BR/EDR/LE module with two U.FL connectors, 500 pcs/reel, Infineon CYW55513
MAYA-W381-00B	MAYA-W381 tri-band Wi-Fi 6E and Bluetooth BR/EDR/LE module with two antenna pins, 500 pcs/reel, Infineon CYW55513
MAYA-W382-00B	MAYA-W382 tri-band Wi-Fi 6E and Bluetooth BR/EDR/LE module with single U.FL connector, 500 pcs/reel, Infineon CYW55513
MAYA-W383-00B	MAYA-W383 tri-band Wi-Fi 6E and Bluetooth BR/EDR/LE module with single antenna pin, 500 pcs/reel, Infineon CYW55513
MAYA-W386-00B	MAYA-W386 tri-band Wi-Fi 6E and Bluetooth BR/EDR/LE module with single antenna pin and embedded PCB antenna, 500 pcs/reel, Infineon CYW55513
MAYA-W361-00B	MAYA-W361 dual-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with two antenna pins, 500 pcs/reel, Infineon CYW55512
MAYA-W362-00B	MAYA-W362 dual-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single U.FL connector, 500 pcs/reel, Infineon CYW55512
MAYA-W363-00B	MAYA-W363 dual-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single antenna pin, 500 pcs/reel, Infineon CYW55512
MAYA-W366-00B	MAYA-W366 dual-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single antenna pin and embedded PCB antenna, 500 pcs/reel, Infineon CYW55512
MAYA-W330-00B	MAYA-W330 single-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with two U.FL connectors, 500 pcs/reel, Infineon CYW55511
MAYA-W331-00B	MAYA-W331 single-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with two antenna pins, 500 pcs/reel, Infineon CYW55511

Ordering code	Product
MAYA-W332-00B	MAYA-W332 single-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single U.FL connector, 500 pcs/reel, Infineon CYW55511
MAYA-W333-00B	MAYA-W333 single-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single antenna pin, 500 pcs/reel, Infineon CYW55511
MAYA-W336-00B	MAYA-W336 single-band Wi-Fi 6 and Bluetooth BR/EDR/LE module with single antenna pin and embedded PCB antenna, 500 pcs/reel, Infineon CYW55511

Table 44: Product ordering codes

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to digital converter
BPF	Band pass filter
CAN	Controller area network
CTS	Clear to send
DC	Direct current
DSR	Data set ready
DTR	Data terminal ready
EIRP	Effective isotropic radiated power
GND	Ground
GPIO	General purpose input/output
H	High
I	Input (means that this is an input port of the module)
IEEE	Institute of Electrical and Electronics Engineers
I2C	Inter-integrated circuit
L	Low
LPO	Low power oscillator
MIMO	Multi-input multi-output
MSD	Moisture sensitive device
N/A	Not applicable
O	Output (means that this is an output port of the module)
PCN/IN	Product change notification / Information note
PD	Pull-down
PU	Pull-up
RMII	Reduced media independent interface
RTS	Request to send
RXD	Receive data
SDIO	Secure digital input output
SPI	Serial peripheral interface
TXD	Transmit data
UART	Universal asynchronous Receiver/Transmitter
USB	Universal serial bus

Table 45: Explanation of the abbreviations and terms used

Related documents

[1] Product packaging reference guide, UBX-14001652
[2] MAYA-W3 system integration manual, UBXDOC-465451970-2522
[3] MAYA-W3 product summary, UBX-23011166

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Revision history

Revision	Date	Name	Comments
R01	01-Mar-2024	epla	Initial release
R02	21-Feb-2025	sebs, mzes	Updated product status of MAYA-W333 and -W336 to Engineering Samples and added additional variants under Document information. Updated Table 11: MAYA-W3 antenna configurations. Added footnote about thermal throttling in Table 23: Operating conditions. Updated Table 31: Wi-Fi transmitter characteristics. Updated Sleep clock description. Added requirement for pull-up resistor for SDIO Interface configuration.
R03	18-Sep-2025	ishe	Updated product status in Document information. Updated Table 1: MAYA-W3 series product features (Wi-Fi Frequency bands, 5 GHz channels). Updated Qualification and approvals and Bluetooth qualification. Updated Table 21: Absolute maximum ratings (Storage temperature). Updated Table 27: Wi-Fi radio typical current consumption with different modes of operation. Updated Table 28: Bluetooth typical current consumption with different modes of operation. Updated Table 29: Bluetooth radio parameters. Updated Table 31: Wi-Fi transmitter characteristics. Added Table 37: Dimensions parameters.
R04	11-Dec-2025	ishe	Added BT_GPIO[2] and BT_GPIO[3] to pin Table 20.
R05	27-Mar-2026	ishe, mzes	Updated chapter GPIOs. Updated Pin assignment in Table 20 for pin B1 - SLP_CLK_IN_OUT (removed alternative function). PCM interface, I2S interface: Added information about TDM2 multiplexing. Updated Coexistence interfaces. Added footnote that shared SDIO interface for Wi-Fi and Bluetooth can be provided on request.

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