TE0835 TRM

Revision v.74

Exported on 2025-06-05

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Current online version of this document.

4 Overview

The Trenz Electronic TE0835 is an extended-grade module based on AMD Zynq UltraScale+ RFSoC.

The Zynq UltraScale+ RFSoC family integrates key subsystems for multiband, multi-mode cellular radios and cable infrastructure (DOCSIS) into an SoC platform that contains a feature-rich 64-bit quad-core Arm Cortex-A53 Application Processing Unit and dual-core Arm Cortex-R5 Real-Time Processing Unit. It integrates the necessary RF-ADCs and RF-DACs.

The module is equipped with DDR4 SDRAM Memory, SPI Flash Memory, USB2.0, Ethernet Transceiver, and 2x Samtec Razor Beam Board to Board (B2B) Connectors. The System Controller (SC) is provided by Lattice MachXO2. A Jitter Attenuator/Clock Multiplier to ITU-T G.8262.1 standard is onboard for high performance applications.

Refer to http://trenz.org/te0835-info for current online available documentation.

4.1 Key Features

- **SoC/FPGA/Module**
  - AMD SoC: XCZU25DR / XCZU27DR / XCZU28DR / XCZU43DR / XCZU47DR / XCZU48DR
  - Speedgrade: -1 / -2 / -L1 / -L2 [1)]
  - Temperature Range: Industrial / Extended [1)]
  - Package: FFVE1156 / FSVE1156 [2)]
- **RAM/Storage**
  - DDR4 SDRAM 4x 8 Gbit [3)]
  - QSPI Flash 2x 512 Mbit (with XiP support) [3)]
  - EEPROM with unique "EUI-48 ™ Node Identity" / MAC address and 192 Byte usable storage
- **On Board**
  - 1 Gbit Ethernet Transceiver
  - USB 2.0 ULPI Transceiver
  - Clock Generator / Jitter Cleaner for SoC logic, ADC, DAC and External Periphery on the Baseboard
  - Secure Authentication device
- **Interface**
  - 3x Pin Header 2.54 mm for I2C
  - 2x B2B Connector (Samtec ST5) for Trenz 6.5 x 9 SoM socket
    - PS: 32x MIO
    - HD: 16x IOs / 8x DIFF
    - HP: 24x IOs / 12x DIFF
    - MGT:
      - 4x GTR
      - 8x GTY
    - ADC: 8x DIFF
    - DAC: 8x DIFF
- **Power**
  - 5 V ... 12 V Input Supply Voltage
- **Dimension**
  - 90 x 65 mm
- **Notes**

  [1)] Available as assembly variant or upon request.

  [2)] Sockets FFVE1156 and SFVE1156 are Footprint-compatible.

  [3)] Other sizes/devices, which are pin/package-compatible, upon request.

4.2 Block Diagram

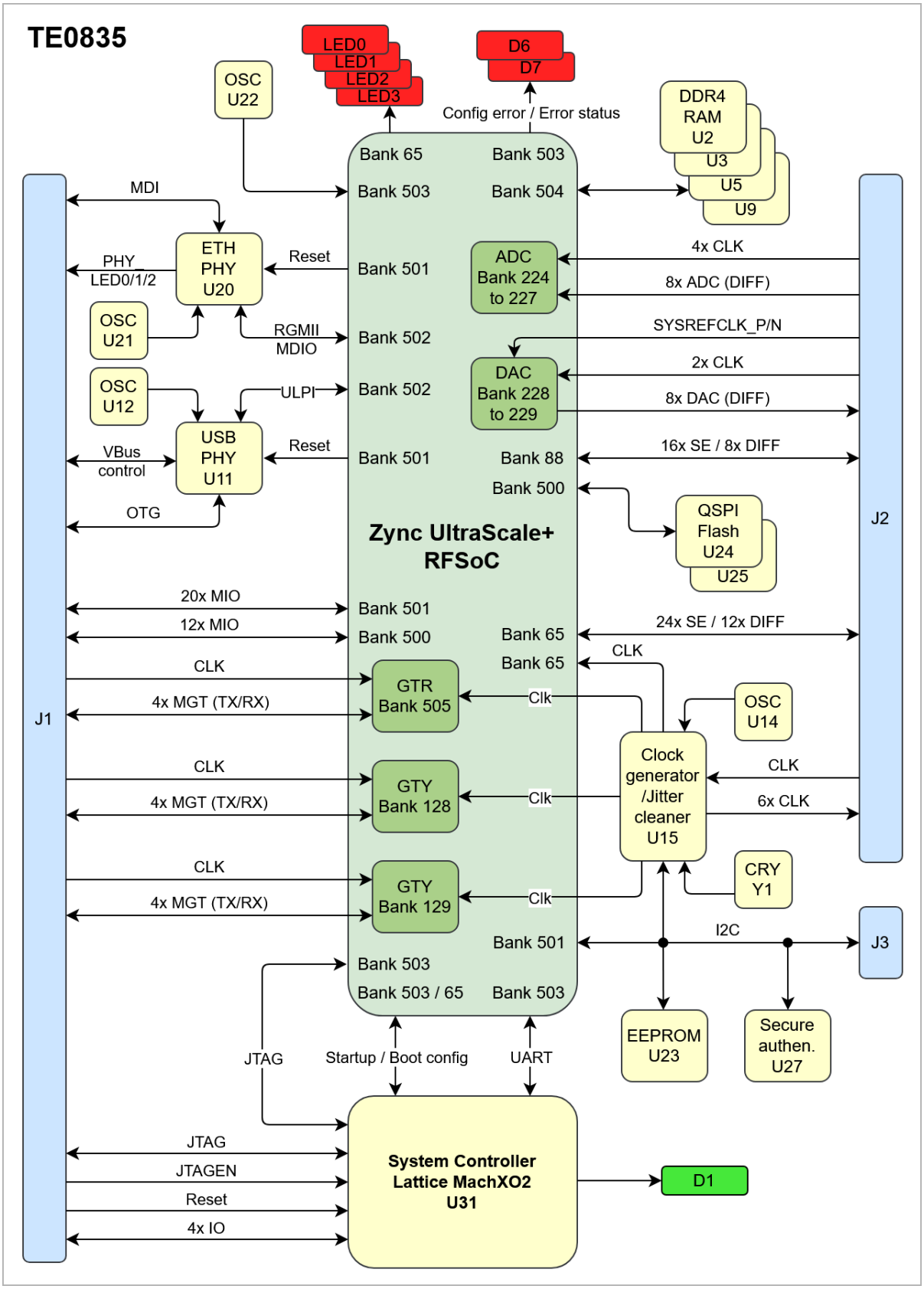

Figure 1: TE0835 block diagram

4.3 Main Components

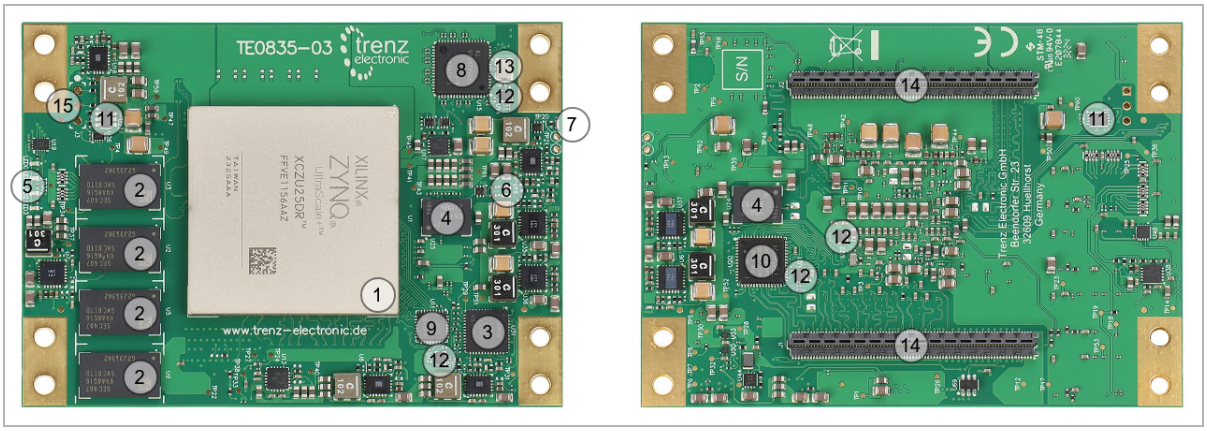

Figure 2: TE0835 main components

1. AMD Zync UltraScale+ RFSoC, U1
2. DDR4 SDRAM, U2, U3, U5, U9
3. System Controller, U31
4. QSPI Flash, U24, U25
5. LEDs, red, user, LED0, LED1, LED2, LED3
6. LEDs, red, SoC status, D6, D7
7. LED, green, SoM Power, D1
8. Clock generator/Jitter cleaner, U15
9. USB 2.0 ULPI Transceiver, U11
10. 1 Gbit Ethernet, U20
11. I2C EEPROM, I2C Secure authentification, U23, U27
12. Oscillators, U12, U14, U21, U22
13. Crystal, Y1
14. B2B Connectors J1, J2
15. Pin Header 2.54 mm for I2C, J3

4.4 Initial Delivery State

Storage device name	Content	Notes
QSPI Flash, U24, U25	Not programmed	
EEPROM, U23	Not programmed	Contains write protected Unique Node ID / MAC .
System Controller, U31	Programmed	Visit TE0835 CPLD Firmware / TE0835 CPLD for further information / firmware description.
DDR4 SDRAM, U2, U3, U5, U9	Not programmed	

Storage device name	Content	Notes
Programmable Clock Generator, U15	Not programmed	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	J1	MIO	32	
B2B	J1	JTAG	4	For SoC and SC, selectable via JTAGEN.
B2B	J1	SC IO	4	
B2B	J1	CLK MGT / GTR reference	2	Clock input to Bank 505
B2B	J1	MGT / GTR	16 (8 DIFF)	Bank 505 GTR
B2B	J1	CLK MGT / GTY reference	2	Clock input to Bank 128
B2B	J1	MGT / GTY	16 (8 DIFF)	Bank 128
B2B	J1	CLK MGT / GTY reference	2	Clock input Bank 129
B2B	J1	MGT / GTY	16 (8 DIFF)	Bank 129
B2B	J1	ETH MDI	8 (4 DIFF)	
B2B	J1	USB OTG	5	
B2B	J1	CLK Gen output	2	
B2B	J2	IO	24 SE / 12 DIFF	
B2B	J2	IO	16 SE / 8 DIFF	

Connector Type	Designator	Interface	IO CNT	Notes
B2B	J2	CLK DAC	4 (2 DIFF)	
B2B	J2	DAC	16 (8 DIFF)	
B2B	J2	CLK ADC	8 (4 DIFF)	
B2B	J2	ADC	24 (8 DIFF + Common mode voltage)	
B2B	J2	CLK Gen input	12 (6 DIFF)	
B2B	J2	CLK Gen output	2 (1 DIFF)	
B2B	J2	CLK SoC input	2 (1 DIFF)	
Pin Header	J3	12C	2	2.54 mm
B2B	J1	ETH PHY LED	3	

Table 2: Board Connectors

5.2 Test Points

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP1		x	Voltage Regulator U8 output	V_1V8_IO	U7 CLKOUT	U7 CLKOUT

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP2		x	Programmable Clock Generator U15 reset input	PLL_RSTN		
TP3		x	Voltage Regulator U13 output	V_0V9_MGTY_AVCC	-	3.3V_CPLD
TP4	x		DDR Termination Regulator U48 reference voltage output	DDR_VREFA	3.3V_CPLD	CPLD_JTAGEN
TP5		x	B2B J1 / SC U31	JTAG_TDO		
TP6		x	B2B J1 / SC U31	JTAG_TDI		
TP7		x	B2B J1 / SC U31	JTAG_TCK		
TP8		x	B2B J1 / SC U31	JTAG_TMS		
TP9		x		GND		
TP10		x	SoC U1 Bank 88	IO_L1P_AD15P_88		

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP11		x	SoC U1 Bank 88	IO_L4P_AD12P_88		
TP12		x	B2B J1	VIN		
TP13		x		GND		
TP14		x		GND		
TP15		x	I2C SCL	MIO32_I2C1_SCL		
Tp16		x	I2C SDA	MIO33_I2C1_SDA		
TP17		x		GND		
TP18		x	LDO Voltage Regulator U38 output	V_2V5_DDRVPP	U8 ADC_AVCC	U8 ADC_AVCC
TP19		x	DDR4 U2 TEN input	DDR4-TEN	U10 ADC_AVCCAUX	U10 ADC_AVCCAUX
TP20	x		B2B J1 / SC U31	V_3V3_AO	3.3V_CPLD	-
TP21	x		B2B J1 / SC U31	CPLD_JTAGEN	GND	-
TP22	x		B2B J1	VIN	-	-
TP23		x	Voltage Regulator U7 output	V_1V2	-	-

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP24	x		Voltage Regulator U44 output	V_4V5_BIAS	-	-
TP25		x	RAM reset signal	DDR4-RESET	-	-
TP26			Voltage Regulator U44 output	V_4V5_BIAS	-	-
TP27	x		Voltage Regulator U44 output	V_4V5_AO	-	-
TP28		x	Voltage Regulator U44 output	V_4V5_AO	-	-
TP29	x		LDO Voltage Regulator U33 output	V_3V3_AO	-	-
TP30		x	LDO Voltage Regulator U33 output	V_3V3_AO	-	-
TP31	x		LDO Voltage Regulator U30 output	V_1V8_AO	-	-
TP32		x	LDO Voltage Regulator U30 output	V_1V8_AO	-	-

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP33	x		Voltage Regulator U8 output	V_1V8_IO	-	-
TP34	x		LDO Voltage Regulator U38 output	V_2V5_DDRVPP	-	-
TP35	x		RAM Termination Regulator U48 output	DDR_VTT	-	-
TP36		x	RAM Termination Regulator U48 output	DDR_VTT	-	-
TP37	x		Voltage Regulator U7 output	V_1V2	-	-
TP38	x		Voltage Regulator U10 output	V_3V3_IO	-	-
TP39		x	Voltage Regulator U10 output	V_3V3_IO	-	-
TP40	x		Voltage Regulator U13 output	V_0V9_MGTY_AVCC	-	-

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP41	x		Voltage Regulator U16 output	V_0V925_DAC_AVCC	-	-
TP42		x	Voltage Regulator U16 output	V_0V925_DAC_AVCC	-	-
TP43	x		Voltage Regulator U16 output	V_0V925_DAC_AVCC	-	-
TP44		x	Voltage Regulator U16 output	V_0V925_DAC_AVCC	-	-
TP45	x		LDO Voltage Regulator U17 output	V_DAC_AVTT	-	-
TP46		x	LDO Voltage Regulator U17 output	V_DAC_AVTT	-	-
TP47	x		Voltage Regulator U18 output	V_1V8_DAC_AVCCAUX	-	-
TP48		x	Voltage Regulator U18 output	V_1V8_DAC_AVCCAUX	-	-
TP49	x		Voltage Regulator U18 output	V_1V8_DAC_AVCCAUX	-	-

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP50		x	Voltage Regulator U18 output	V_1V8_DAC_AVCCAUX	-	-
TP51	x		Voltage Regulator U35 output	V_0V85	-	-
TP52		x	Voltage Regulator U35 output	V_0V85	-	-
TP53		x	RAM Termination Regulator U48 reference voltage output	DDR_VREFA	-	-
TP54	x		Voltage Regulator U7 CLKOUT. No net name.	-	-	-
TP55		x	Voltage Regulator U8 CLKOUT. No net name.	-	-	-
TP56		x	Voltage Regulator U10 CLKOUT. No net name.	-	-	-

Test Point	REV03				REV02	REV01
	Top	Bottom	Notes	Signal	- = Test Point not used Designator and or only net name	
TP57	x		Voltage Regulator U16 CLKOUT. No net name.	-	-	-
TP58	x		Voltage Regulator U18 CLKOUT. No net name.	-	-	-
TP59	x		Voltage Regulator U18 output	V_1V8_DAC	-	-
TP60		x	Voltage Regulator U18 output	V_1V8_DAC	-	-
TP61	x		Voltage Regulator U16 output	V_0V925_RF	-	-
TP62		x	Voltage Regulator U16 output	V_0V925_RF	-	-

Table 3: Test Points Information

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
Zynq UltraScale+ RFSoC	U1	• DDR4 SDRAM U2, U3, U5, U9 • QSPI Flash U24, U25 • I2C • B2B J1, J2	
DDR4 RAM	U2, U3, U5, U9	• Zynq SoC U1	
QSPI Flash	U24, U25	• Zynq SoC U1	
System Controller	U31	• Zynq SoC U1 • B2B J1	
USB 2.0 ULPI Transceiver	U11	• Zynq SoC U1 • Oscillator U12 • B2B J1	
Gigabit Ethernet transceiver	U20	• Zynq SoC U1 • Oscillator U21 • B2B J1	
EEPROM with EUID/MAC	U23	• I2C	
Secure authentication	U27	• I2C	

Chip/Interface	Designator	Connected To	Notes
Clock Synthesizer/Jitter Cleaner	U15	• Zynq SoC U1 • Oscillator U14 • I2C • B2B J2, J3	
Oscillator	U22	• Zynq SoC U1	33 ⅓ MHz
Oscillator	U12	• USB 2.0 ULPI Transceiver U11	52 MHz
Oscillator	U14	• Clock Synthesizer U15	25 MHz
Oscillator	U21	• Gigabit Ethernet transceiver U20	25 MHz
Crystal	Y1	• Clock Synthesizer U15	54 MHz

Table 4: On board peripherals

7 Configuration and System Control Signals

Signal Name	Connector.Pin	Direction[1)]	Description
CPLD_JTAGEN	J1.30	IN	JTAG. Selects the interface target between the SoC and SC.
RESETN	J1.36	IN	SoM reset signal to SC (Active low).
MIO33_I2C1_SDA/SDL	J3.1 / J3.2	Signal dependend	12C
USB0_VBUS	J1.155	IN	USB Bus voltage signal.
USB0_CPEN	J1.157	OUT	USB Bus voltage enable.

Table 5: Controller signal.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.
- INOUT: Bidirectional signal.
- Signal dependend: A Signal can have different functions and directions as part of a Bus.

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction[1)]	Notes
VIN	J1.1 / J1.3 / J1.5 / 1.2 / J1.4 / J1.6 / J1.8	IN	SoM supply.
PSBATT	J1.14	IN	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.
V_3V3_AO	J1.16	OUT	System Controller supply.
ADC0/../7_VCM	J1.30 / J1.32 / J1.42 / J1.44 / J1.48 / J1.50 / J1.60 / J1.62 / J1.66 / J1.68 / J1.78 / J1.80 / J1.84 / J1.86 / J1.96 / J1.98	OUT	ADC common mode voltage.

Table 6: Module power rails.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

A good starting point into your own custom carrier board design can be the familiarization with Trenz Electronic's Carrier designs for the TEB0835. The Trenz 4 x 5 SoM Integration Guide and our FAQ - PCB Design hold valuable information.

See also AMD datasheet AMD datasheets and guides for additional information.

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
1	VIN	5.0 V (± 5 %)	-	Apply power to the SoM.	
2	RESETN	3.3 V (± 5 %)	-[1)]	Release (set low) signal when to begin with the SoM startup.	
3	CPLD_IO3	3.3 V (± 5 %)	-[1)]	Signals power good, use to enable periphery.	

Table 7: Baseboard Design Hints

[1)] Firmware dependent. Refer to TE0835 CPLD Firmware / TE0835 CPLD for further information.

9 Board to Board Connectors

The module has two 160-pin double-row REF-192552-02 connector on the bottom side. The counterpart REF-192552-01 is placed on the Baseboard.

Order number	REF Number	Samtec Number	Type	Mated Height	Data sheet	Comment
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	5 mm	http://suddendocs.samtec.com/catalog_english/st5.pdf	Standard connector used on module
27219	REF-192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	5 mm	http://suddendocs.samtec.com/catalog_english/ss5.pdf	Standard connector used on board

Table 8: Connectors.
With different connectors from the used series other mating heights are possible (according to the Datasheet). The module and base board can be manufactured using other connectors upon request.

Connector Specifications	Value
Insulator material	Liquid crystal polymer
Stacking height	5 mm
Contact material	Phosphor-bronze
Plating	Au or Sn over 50 µ" (1.27 µm) Ni
Current rating	1.6 A per pin (2 pins powered)
Operating temperature range	-55 °C to +125 °C
RoHS compliant	Yes

Table 9: Connector specifications.

9.1 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm, Single-Ended	13.5GHz / 27Gbps
5 mm, Differential	20GHz / 40Gbps
4 mm, Single-Ended	13GHz / 26Gbps
4 mm, Differential	13.5GHz / 27Gbps

Table 10: Speed rating.

9.2 Current Rating

Current rating of Samtec Razor Beam™ SS5/ST5 B2B connectors is 1.6A per pin (2 pins powered).

9.3 Connector Mechanical Ratings

- Shock: 100G, 6 ms sawtooth wave
- Vibration: 7.56G 'RMS', 2 hours per axis, 3 axes total

10 Technical Specifications

This TRM is generic for all variants.

- The voltage ranges are generally the same across variants (exceptions are possible, depending on custom requests).
- The temperature range can differ depending on the assembly version.
- The combination of a carrier and a SoM might have different requirements.

Variants of modules are described here: Article Number Information. Please contact us for options.

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VIN	Supply power from carrier.	0	18	V
PSBATT	PS battery-backed RAM and real-time clock (RTC) supply voltage.	-0.5	2.00	V

Table 11: Absolute maximum ratings

*) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Condition". Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

Trenz Electronic classifies modules into temperature range categories by subsumption of its component data (PCB, ICs, connectors, passive components). The temperature ranges are values for ambient air temperature and do not reflect the junction temperature of individual components.

The categories are:

- Modules with commercial temperature grade are equipped with components that cover at least the ambient temperature range of 0°C to 75°C.
- Modules with extended temperature grade are equipped with components that cover at least the ambient temperature range of 0°C to 85°C.
- Modules with industrial temperature grade are equipped with components that cover at least the ambient temperature range of -40°C to 85°C.

These categories do not take into account the entire custom system consisting of:

- Customer SoC/FPGA design.
- Cooling solution, active and or passive cooling.
- Climate or enviromental conditions besides ambient temperature range.

- Module orientation, neigboring assemblies, neither other heat sources nor the SoC/FPGA as heat source to other components.

10.2.1 Temperature range

This SoM's components are capable of being operated at industrial-grade temperatures, which cover at least the range of -40 °C to +85 °C.

The temperature of individual components should not exceed the specified range due to self-heating or heating by adjacent components.

The Operating temperature range depends also on customer design and cooling solution.

10.2.2 Voltage rails

Parameter	Min	Max	Units	Reference Document
VIN	4.75	5.25	V	
PSBATT	1.200	1.500	V	See AMD DS926 datasheet.

Table 12: Recommended operating conditions.

10.3 Physical Dimensions

- Module size: 90 mm × 65 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.
- PCB thickness: : 2.027mm ±10 %.

All dimensions are shown in millimeters.

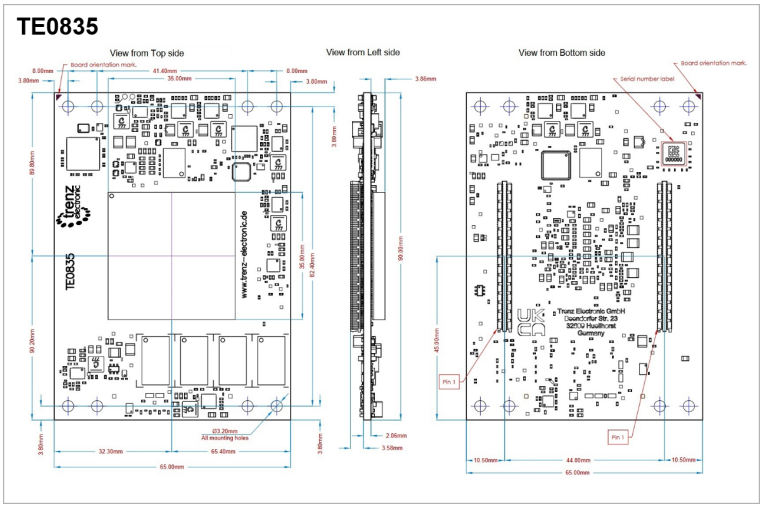

Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0835 overview page*	
English page	German page

Table 13: Trenz Electronic Shop Overview
*) Module article name encoding table: Zynq Ultrascale+ based modules (MPSoC, RFSoC)

12 Revision History

12.1 Hardware Revision History

The hardware revision number is located on the PCB next to the module identifier, separated by a dash.

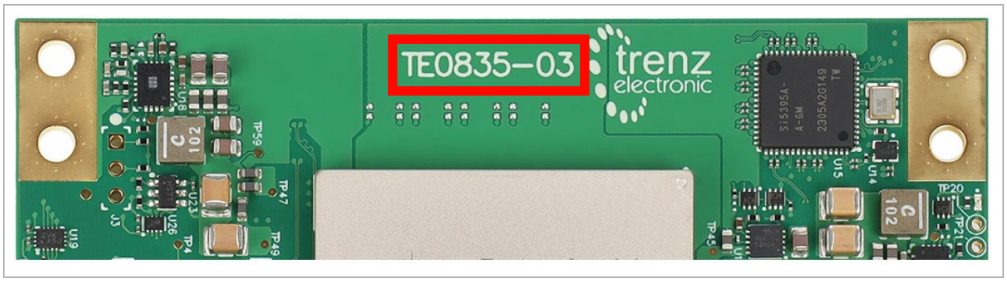

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Link
2023-10	03	1. Added Legal Notices. 2. Added Power Diagram. 3. Added a DC-DCs synchronization circuit to spread spectrum. 4. Changed the core power supply schematic to 4 phases to increase current and reduce noise. 5. The power supply circuit of the module supports input voltage 5...12V. 6. EOL components are replaced: 6.1. L10, L12, L13, L14, L16 Ferrit beads BKP0603HS121-T replaced with MPZ0603S121HT000. 7. Updated layerstack to enhance power supply circuits and improve signal impedance matching. 8. Added POR_OVERRIDE configuration. 9. U25 (Pin 33) PS_SRST_B signal was removed. POR_OVERRIDE_N connected. 10. Added transistor T2A. 11. C180 is removed from schematic. 12. Networks to power the banks have been renamed. 13. Added Level shifter U19. 14. LEDs renamed: D1 --> LED0; D2 --> LED1; D3 --> LED2; D4 --> LED3 and connected to V_3V3_IO. Resistors R77A, R77B, R77C, R77D (39 R) replaced with R77, R130, R132, R134 (1K)	REV03 PCN

Date	Revision	Changes	Documentation Link
		respectively according to new shematic. 15. Added pull-up resistors R157, R158, R159, R161, R162, R163 to synchronise the power supplies. 16. Added resistors R142-R145. 17. U23 connected to V_3V3_IO (was 1.8V). 18. ZU_PWR: L9 removed from shematic. 19. Added resistors R46, R90, R98, R146, R149. 20. Added U44. 21. U33 (ADP7102ACPZ) replaced with MIC5504-3.3YMT. 22. Added two capasitors 4.7uF C355 and C488 on DDR_VTT. 23. Added signal SEL_2V5_DAC to Bank 65HP. Pin AD16. 24. Capasitors C24, C32, C97, C130-136, 150-152, 155, 190,191, C203, C204, C214, C216 are replaced with 100 nF. 25. Y1 CX3225SB54000 is EOL, it is replaced with ECS-540-8-33-JTN-TR 26. Added a VIN voltage sensor R121, R124, R150, R122, R153, C489. 27. Added R154, R155 to implement I2C interface between SC and RFSoC. 28. Clock CLK0A_100MHz renamed to PLL_CLKOUT 29. Changed CPLD LCMXO2-640HC-4SG48C (U31) to LCMXO2-640HC-4SG48I.	

Date	Revision	Changes	Documentation Link
2020-07	02	1. Added a VRP resistor on bank 65. 2. LDO U33 is changed on ADP7102ACPZ. 3. Signal FPGA IO0 is connected on AE18 pin of FPGA. 4. Signal DBG_LED3 is connected on AD18 pin of FPGA. 5. Signal MIO13_25 connected to J1 pin 33 instead MIO25. 6. Resistor R84 is removed. 7. LED D1 moved on edge of PCB. 8. Added THT testpoints J4 on CPLD_JTAGEN, R76 was removed. 9. Signals B49_XX_X are renamed in B88_XX_X. 10. C241 is changed on 1nF. 11. Length of CLK signals on RFADC and RFDAC are adjusted. 12. Wrong connection on U8 is fixed (PCB). 13. Wrong connection PGOOD1 pin of U7 is fixed. 14. R17 is changed from 35,5K to 33K for VCC_PL_PS correction. 15. APRE_3V3 ranamed to APRE_4V5, voltage of the power rail incrised from 3.3V to 4,58V. 16. Resistor R15 is changed from 13,3K to 9,09K. AN: 24671 → 25969. 17. Capasitor C27 is changed from 100uF x 4V to 47uF x 6,3V. AN: 28940->24718.	REV02 PCN
2019-06	01	Initial revision	REV01

Table 14: Hardware Revision History

12.2 Document Change History

Date	Revision	Contributor	Description
2025-05-21	v.74	Kilian Jahn	• Updated to TRM version 4.3 • Updated TRM to hardware revision 03 • Minor error corrections • Adepted link "Download PDF version of this document." • Block Diagramm: Corrected LED name error and moved signal names above the arrows
2024-08-27	v.61	John Hartfiel	• Board to Board Connector Section: Bugfix Include Macro
2024-02-19	v.60	Martin Rohrmüller	• Bugfix Overview Picture
2021-12-21	v.58	John Hartfiel	• Bugfix B2B section • Replace GTH with GTY
2021-05-28	v.55	John Hartfiel	• Style update • Bugfix PDF Link • Key features update

Date	Revision	Contributor	Description
2020-11-23	v.51	Pedram Babakhani	• Update to REV02
--	all	Pedram Babakhani , John Hartfiel , Kilian Jahn , Martin Rohrmüller	• --

Table 15: Document change history.

13 Disclaimer

13.1 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

13.2 Document Warranty

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13.4 Copyright Notice

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13.5 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

13.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

13.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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