TE0813 TRM

Revision v.46

Exported on 2023-10-11

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0813+TRM

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4 Overview

The Trenz Electronic TE0813 is an industrial grade MPSoC SOM integrating an AMD Zynq™ UltraScale+™, DDR4 SDRAM with 64-Bit width data bus connection, SPI Boot Flash memory for configuration and operation, transceivers and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking connections in a compact 5.2 cm x 7.6 cm form factor.

Refer to http://trenz.org/te0813-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC**
  - Device: ZU1 / ZU2 / ZU3 / ZU4 / ZU5 [1)]
  - Engine: CG / EG / EV [1)]
  - Speedgrade: -1 / -1L / -2 / -2L / -3 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: SFVC784
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM [2)]
  - 2 x 64 MByte Serial Flash [3)]
  - EEPROM with MAC address
- **On Board**
  - Oscillator
- **Interface**
  - 4 x B2B Connector (ADM6)
    - up to 204 PL IO
      - HP: 156
      - HD: 0 / 48 [4)]
    - up to 65 PS MIO
    - 4 GTR
    - 4 GTH (with ZU4 and higher)
    - I2C, JTAG
- **Power**
  - 3.3 V power supply via B2B Connector needed [5)].
- **Dimension**
  - 76 mm x 52 mm
- **Notes**

  [1)] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

  [2)] Up to 8 GByte are possible with a maximum bandwidth of 2400 MBit/s.

  [3)] Please, take care of the possible assembly options.

  [4)] Please, take care of the possible assembly options.

  [5)] Dependant on the assembly option a higher input voltage may be possible.

4.2 Block Diagram

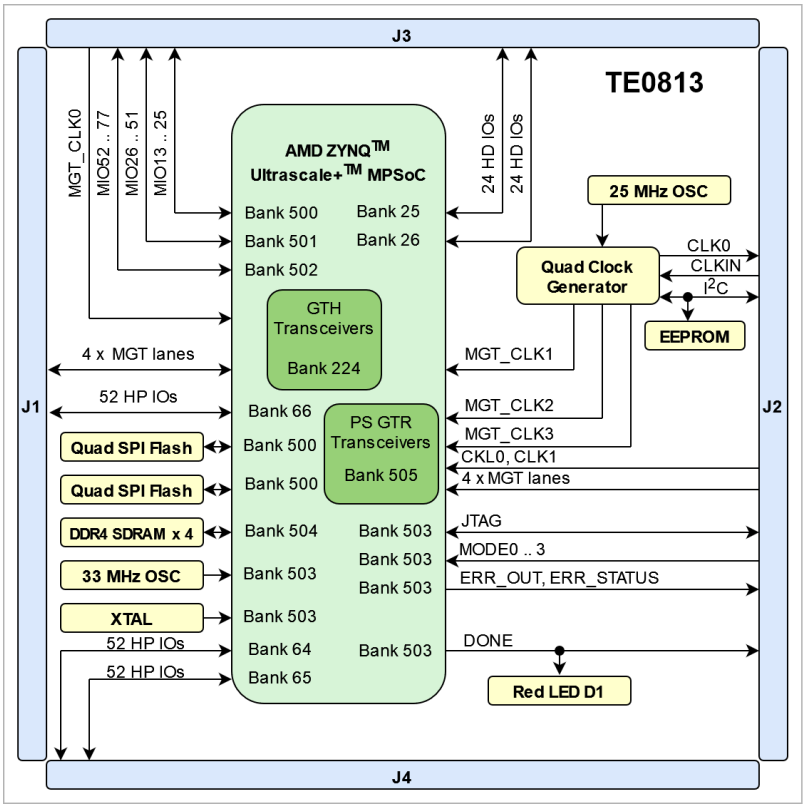


Figure 1: TE0813 block diagram

4.3 Main Components

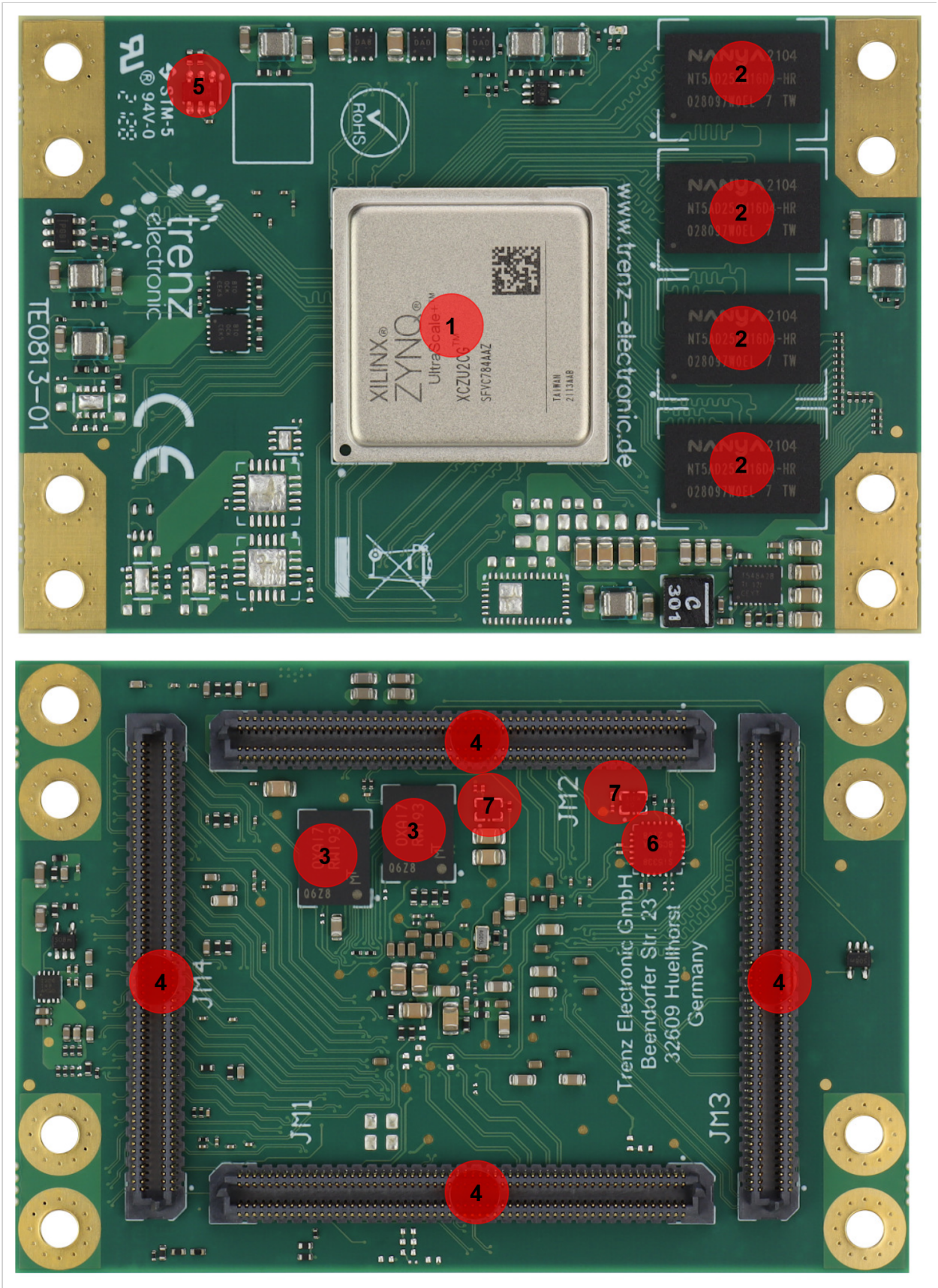
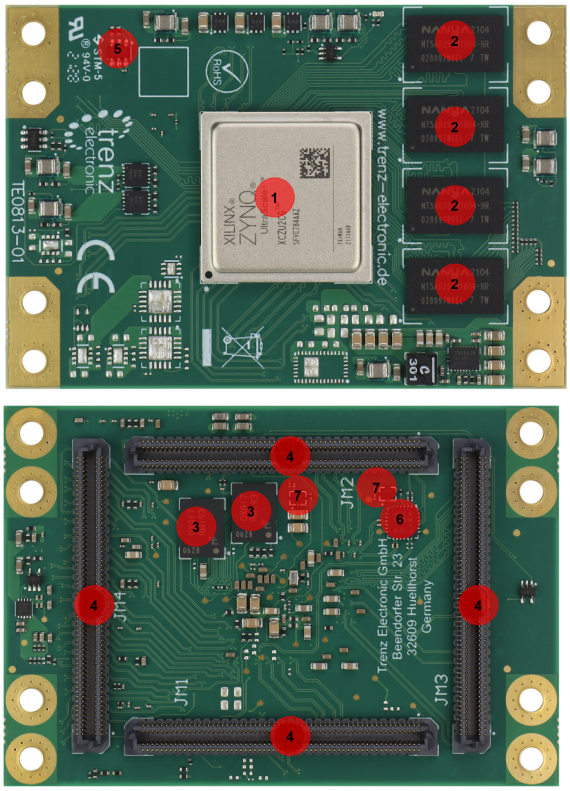


Figure 2: TE0813 main components



1. SoC, U1
2. DDR4, U2, U3, U9, U12
3. Quad SPI Flash, U7, U17
4. Connector, JM1, JM2, JM3, JM4
5. EEPROM, U28
6. Clock Generator, U5
7. Oscillator, U6, U32

4.4 Initial Delivery State

Storage device name	Content	Notes
DDR4 SDRAM	not programmed	
Quad SPI Flash	not programmed	
EEPROM	not programmed besides factory programmed MAC address	
Programmable Clock Generator	not programmed	

Table 1: Initial delivery state of programmable devices on the module

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT [1)]	Notes
B2B	JM1	MGT PL	4 x MGT (RX/TX)	
B2B	JM1	HP	52 SE / 24 DIFF	
B2B	JM2	MGT PS	2 x MGT CLK	
B2B	JM2	MGT PS	4 x MGT (RX/TX)	
B2B	JM2	CFG	JTAG	
B2B	JM2	CFG	I2C	
B2B	JM2	CFG	MODE	
B2B	JM3	HD	48 SE / 24 DIFF	
B2B	JM3	MGT PL	MGT CLK	
B2B	JM3	MIO	65 GPIO	
B2B	JM4	HP	104 SE / 48 DIFF	

Table 2: Board Connectors

[1)] IO CNT depends on assembly variant. E.g. the MGTs are not available for all FPGAs

5.2 Test Points

Test Point	Signal	Notes[1)]
TP1	PLL_SCL	pulled-up to PS_1V8

Test Point	Signal	Notes[1)]
TP2	PLL_SDA	pulled-up to PS_1V8
TP3	DDR4-TEN	pulled-down to GND
TP4	DCDC_2V0	
TP5	GND	
TP6	PL_1V8	
TP7	GND	
TP8	GND	
TP9	PL_VCCINT_IO	
TP10	GND	
TP11	PL_VCCINT	
TP12	PL_VCU_0V9	
TP13	FP_0V85	
TP14	PS_1V8	
TP15	GND	
TP16	DDR_2V5	
TP17	DDR_PLL	
TP18	DDR_1V2	
TP19	PS_GT_1V0	
TP20	MGTAVTT	

Test Point	Signal	Notes[1)]
TP21	VTT	
TP22	PL_GT_1V15	was PL_GT_1V05 in REV01.
TP23	VREFA	
TP24	MGTVCCAUX	
TP25	MGTAVCC	
TP26	PL_GT_1V45	
TP27	PS_PLL	
TP28	PS_AVTT	
TP29	LP_0V85	
TP30	PS_AUX	
TP31	PS_AVCC	
TP34	POR_B	pulled-up to PS_1V8

Table 3: Test Points Information

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12	SoC - PS	
Quad SPI Flash	U7, U17	SoC - PS	Booting.
EEPROM	U28	B2B - J2	MAC address
Clock Generator	U5	SoC, B2B	
Oscillator	U6	Clock Generator	25 MHz
Oscillator	U32	SoC	33.333333 MHz

Table 4: On board peripherals

7 Configuration and System Control Signals

Connector+Pin	Signal Name	Direction[1)]	Description
JM1.A45	POR_OVERRIDE	IN	Override power-on reset delay [2)].
JM2.A31	ERR_OUT	OUT	PS error indication [2)].
JM2.A34	ERR_STATUS	OUT	PS error status [2)].
JM2.A35	LP_GOOD	OUT	Low-power domain powered-up. Pulled up to 3.3VIN
JM2.A36	PLL_SCL	IN	I2C clock
JM2.A37	PLL_SDA	IN/ OUT	I2C data
JM2.A40	PG_VCU	OUT	Programmable logic powered-up.
JM2.A41	EN_PSGT	IN	Enable GTR transceiver power-up.
JM2.A44 / JM2.A45 / JM2.A46 / JM2.A47	TCK / TDI / TDO / TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: PS_1V8
JM2.B29	PG_PSGT	OUT	GTR transceivers powered-up.
JM2.B30	PROG_B	IN/ OUT	Power-on reset [2)]. Pulled-up to PS_1V8.
JM2.B33	SRST_B	IN	System reset [2)]. Pulled-up to PS_1V8.
JM2.B34	INIT_B	IN/ OUT	Initialization completion indicator after POR [2)]. Pulled-up to PS_1V8.

Connector+Pin	Signal Name	Direction[1)]	Description
JM2.B37	PG_PL	OUT	VCU powered-up.
JM2.B38	EN_FPD	IN	Enable full-power domain power-up.
JM2.B41	PG_FPD	OUT	Full-power domain powered-up.
JM2.B42	EN_LPD	IN	Enable low-power domain power-up.
JM2.B45	PG_DDR	OUT	DDR power supply powered-up.
JM2.B46	DONE	OUT	PS done signal [2)]. Pulled-up to PS_1V8.
JM2.B47	EN_DDR	IN	Enable DDR power-up.
JM2.C31	MR	IN	Manual reset.
JM2.C35	EN_PL	IN	Enable programable logic power-up.
JM2.C36	EN_GT_R	IN	Enable GTH/GTY transceiver power-up.
JM2.C44 / JM2.C45 / JM2.C46 / JM2.C47	MODE3..0	IN	Boot mode selection [2)]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
JM2.D33	PG_GT_R	OUT	GTH/GTY Transceivers powered-up.
JM2.D37	PSBATT	IN	PS RTC Battery supply voltage [2) 3)].
JM2.D38	PUDC_B	IN	Enable/Disable internal pull-ups during configuration on all SelectIO pins.

Connector+Pin	Signal Name	Direction[1)]	Description
JM2.D45 / JM2.D46	DX_P / DX_N	-	SoC temperatur sensing diode pins [2)].

Table 5: Controller signal.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2)] See UG1085 for additional information.

[3)] See Recommended Operating Conditions(see page 27).

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction[1)]	Notes
VCCO_66	JM1.A32 / JM1.A33	IN	
VREF_66	JM1.A41	IN	
3.3VIN	JM1.A54 / JM1.A55 / JM1.B55 / JM1.B56	IN	
PL_1V8	JM1.C32 / JM1.C33 / JM1.D33 / JM1.D34	OUT	
PL_DCIN	JM1.C56 / JM1.C57 / JM1.C58 / JM1.C59 / JM1.C60 / JM1.D56 / JM1.D57 / JM1.D58 / JM1.D59 / JM1.D60	IN	
LP_DCDC	JM2.A50 / JM2.A51 / JM2.A52 / JM2.B50 / JM2.B51 / JM2.B52 / JM2.C50 / JM2.C51 / JM2.C52 / JM2.D50 / JM2.D51 / JM2.D52	IN	
DCDCIN	JM2.A57 / JM2.A58 / JM2.A59 / JM2.A60 / JM2.B57 / JM2.B58 / JM2.B59 / JM2.B60 / JM2.C57 / JM2.C58 / JM2.C59 / JM2.C60 / JM2.D57 / JM2.D58 / JM2.D59 / JM2.D60 /	IN	
PS_BATT	JM2.D37	IN	
DDR_1V2	JM2.D47	OUT	

Power Rail Name/ Schematic Name	Connector.Pin	Direction[1)]	Notes
PS_1V8	JM2.C34 / JM2.D34 / JM3.A56 / JM3.B56 / JM3.C56 / JM3.D56	OUT	
GT_DCDC	JM3.A59 / JM3.A60 / JM3.B59 / JM3.B60 / JM3.C59 / JM3.C60 / JM3.D59 / JM3.D60 /	IN	
VCCO_25	JM3.C7 / JM3.C8 / JM3.D8 / JM3.D9	IN	
VCCO_26	JM3.C19 / JM3.C20 / JM3.D20 / JM3.D21	IN	
VCCO_64	JM4.B21 / JM4.B39	IN	
VREF_64	JM4.B30	IN	
VCCO_65	JM4.C21 / JM4.C39	IN	
VREF_65	JM4.C30	IN	

Table 6: Module power rails.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

The power up sequencing highly depends on the use case. In general, it should be possible to enable/disable the processing system (PS) / programmable logic (PL) independently. Furthermore, within the processing logic it should be possible to enable/disable only low-power domain and/or low-power and full-power domain. Additionally, usage of GTR for PS side and GTH/GTY for PL side should be possible. Because of this flexibility the needed parts of the following table needs to be selected individually. For detailed information take a look into schematics.

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals(see page 15).
1 [1)]	PSBATT	1.2 V ... 1.5 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.
1 [2)]	3.3VIN	3.3 V (± 5 %)	-	Management power supply.	Management module power supply. 0.5 A recommended. Consider note [2)] for modules with VCU and/or low-power SoC.
2	Processing System (PS):			Procedure for PS starting.	
2.1	Low-power domain:			Bring-up for low-power domain PS.	
2.1.1	LP_DCDC	3.3 V (± 3 %) [3)]	-	Low-power domain power supply.	Main module power supply for low-power domain. 5.5 A recommended. Power consumption depends mainly on design and cooling solution.
2.1.2	EN_LPD	-	PU [4)], 3.3 V	Low-power domain power enable.	
2.1.3	LP_GOOD	-	PU [4)], 3.3 V	Low-power domain power good status.	Module power-on sequencing for low-power domain finished.

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
2.2	Full-power domain:			Bring-up for full-power domain PS.	Full-power PS domain needs powered low-power PS domain.
2.2.1	DCDCIN	3.3 V (± 5 %) [3]		Full-power domain and GTR transceiver power supply.	Main module power supply for full-power domain. 7 A recommended. Power consumption depends mainly on design and cooling solution.
2.2.2	EN_FPD	3.3 V	-	Full-power domain power enable.	
2.2.3	PG_FPD	-	PU [4], 3.3 V	Full-power domain power good status.	Module power-on sequencing for full-power domain finished.
2.2.4	EN_DDR	3.3 V	-	DDR memory power enable.	
2.2.5	PG_DDR		PU [4], 3.3 V	DDR memory power good status.	Module power-on sequencing for DDR memory finished.
2.3	GTR Transceiver			Procedure for GTR transceiver starting.	PS transceiver usage needs powered PS (low- and full-power domain).
2.3.1	EN_PSGT	3.3 V	-	GTR transceiver power enable.	
2.3.2	PG_PSGT	-	PU [4], 3.3 V	GTR transceiver power good status.	Module power-on sequencing for GTR transceiver finished.

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2	Programmable Logic (PL)			Procedure for PL starting.	PS and PL can be started independently.
2.1	PL_DCIN	3.3 V (± 5 %) 3) 5)	-	Programmable logic power supply.	Main module power supply for programmable logic. 12 A recommended. Power consumption depends mainly on design and cooling solution.
2.2	EN_PL	-	PU 4), 3.3 V	Programmable logic power enable.	
2.3	PG_PL	-	PU 4), 3.3 V	Programmable logic power good status.	Module power-on sequencing for programmable logic finished. Periphery and variable bank voltages can be enabled on carrier.
2.4	VCCO_25 / VCCO_26 / VCCO_64 / VCCO_65 / VCCO_66	6)	-	Module bank voltages.	Enable bank voltages after PG_PL deassertion.
2.5	PG_VCU	-	PU 4), 3.3 V	VCU power good status.	
3	GTH / GTY Transceiver			Procedure for GTH / GTY transceiver starting.	PL transceiver usage needs powered PL and low-power PS domain.

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
3.1	GT_DCDC	3.3 V (± 3 %) [3]	-	GTH / GTY transceiver power supply.	Main module power supply for GTH / GTY transceiver. 3 A recommended. Power consumption depends mainly on design and cooling solution.
3.2	EN_GT_R	3.3 V	-	GTH / GTY transceiver power enable.	
3.3	PG_GT_R	-	PU [4], 3.3 V	GTH / GTY transceiver power good status.	

Table 7: Baseboard Design Hints

[1] (optional)

[2] On TE0813 REV01 boards it is necessary for modules with VCU and/or low-power speedgrade to either connect signal EN_PL to voltage 3.3VIN or to enable EN_PL together with 3.3VIN. This should be changed in a newer revision.

[3] Dependent on the assembly option a higher input voltage may be possible.

[4] (on module)

[5] This value depends highly on DCDC U4. Higher values may be possible with different DCDCs. For more information consult schematic and according datasheets.

[6] See DS925 for additional information.

9 Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec AcceleRate HD High-Density Slim Body Arrays on bottom side.

- 4x ADM6-60-01.5-L-4-2 (240 pins, 60 per row)
  - Mates with ADF6-60-01.5-L-4-2

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec AcceleRate HD High-Density Slim Body Arrays on top side.

- 4x ADF6-60-03.5-L-4-2 (160-pins)
  - Mates with ADM6-60-01.5-L-4-2

9.1 Features

- Board-to-Board Connector 240-pins, 60 contacts per row
- 0.025" (0.635 mm) pitch
- Data Rate: max 56 Gbps
- Mates with: ADM6/APF6
- Insulator Material: LCP, Black
- Contact Material: Copper Alloy
- Plating: Au or Sn over 50 µ" (1.27 µm) N
- Operating Temperature Range: -55 °C to +125 °C
- PCIe 5.0 capable: Yes
- Lead-Free Solderable: Yes
- RoHS Compliant: Yes

9.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
30095	REF-30095	ADM6-60-01.5-L-4-2	Module connector	1.5 mm	Standard connector used on modules
31137	REF-31137	ADF6-60-03.5-L-4-2	Baseboard connector	3.5 mm	Standard connector used on carrier

Table 8: Connectors.

9.3 Connector Speed Ratings

The AcceleRate HD High-Density connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm	56 Gbps

Table 9: Speed rating.

9.4 Current Rating

Current rating of Samtec AcceleRate HD High-Density B2B connectors is 1.34 A per pin (4 pins powered)

9.5 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
LP_DCDC	Micromodule Power	-0.300	6.0	V
DCDCIN	Micromodule Power	-0.300	7.0	V
GT_DCDC	Micromodule Power	-0.300	6.0	V
PL_DCIN 1)	Micromodule Power	-0.300	4.5	V
3.3VIN	Micromodule Power	-0.300	3.600	V
PS_BATT	RTC / BBRAM	-0.500	2.000	V
VCCO_25	HD IO Bank power supply	-0.500	3.400	V
VCCO_26	HD IO Bank power supply	-0.500	3.400	V
VCCO_64	HP IO Bank power supply	-0.500	2.000	V
VCCO_65	HP IO Bank power supply	-0.500	2.000	V

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VCCO_66	HP IO Bank power supply	-0.500	2.000	V
VREF_64	Bank input reference voltage	-0.500	2.000	V
VREF_65	Bank input reference voltage	-0.500	2.000	V
VREF_66	Bank input reference voltage	-0.500	2.000	V

Table 10: Absolute maximum ratings

[1)] This value depends on DCDC U4 circuit. If resistor R133 is fitted and R132 is not fitted (default) 7.0 V is allowed. If resistor R133 is not fitted and R132 is fitted only 4.5 V is allowed. For more information consult schematic and according datasheets.

[*)] Stresses beyond those listed under Absolute Maximum Ratings(see page 0) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition(see page 0). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be different depending on assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information[1]
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

1 https://wiki.trenz-electronic.de/display/PD/Article+Number+Information

Parameter	Min	Max	Units	Reference Document
LP_DCDC [1)]	3.201	3.399	V	
DCDCIN [1)]	3.135	3.465	V	
GT_DCDC [1)]	3.201	3.399	V	
PL_DCIN [1) 2) 3)]	3.135	3.465	V	
3.3VIN	3.135	3.465	V	
PS_BATT	1.2	1.5	V	See FPGA datasheet.
VCCO_25	1.140	3.400	V	See FPGA datasheet.
VCCO_26	1.140	3.400	V	See FPGA datasheet.
VCCO_64	0.95	1.900	V	See FPGA datasheet.
VCCO_65	0.95	1.900	V	See FPGA datasheet.
VCCO_66	0.95	1.900	V	See FPGA datasheet.
VREF_64	0.6	1.2	V	See FPGA datasheet.
VREF_65	0.6	1.2	V	See FPGA datasheet.
VREF_66	0.6	1.2	V	See FPGA datasheet.

Table 11: Recommended operating conditions.

[1)] Dependent on the assembly option a higher input voltage may be possible.

[2)] This value depends on DCDC U4 circuit. If resistor R133 is fitted and R132 is not fitted (default) 7.0 V are allowed. If resistor R133 is not fitted and R132 is fitted only 4.5 V are allowed. For more information consult schematic and according datasheets.

[3)] For U4 either TPS548A28RWWR or MPQ8633BGLE-Z is assembled which is up to Trenz Electronic GmbH.

10.3 Physical Dimensions

- Module size: 76 mm × 52 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.74 mm (± 10 %).

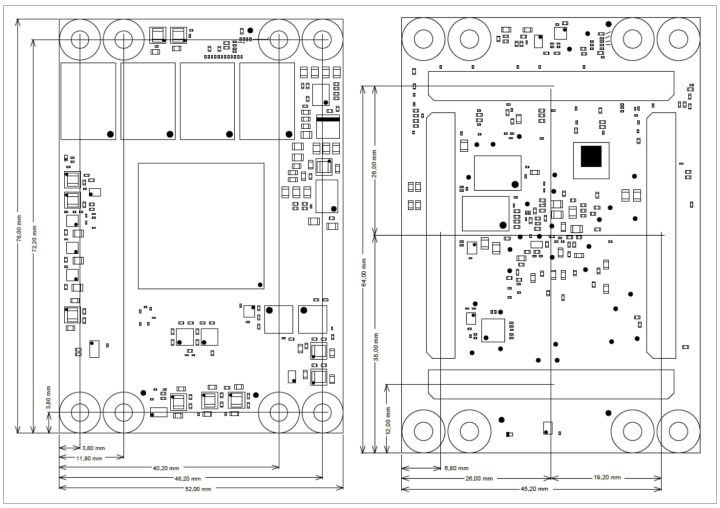


Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0813 overview page	
English page[2]	German page[3]

Table 12: Trenz Electronic Shop Overview

2 https://shop.trenz-electronic.de/en/search?sSearch=TE0813
3 https://shop.trenz-electronic.de/de/search?sSearch=TE0813

12 Revision History

12.1 Hardware Revision History

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Link
-	REV 02	1. Change DCDC U11 from EN6347QI to MPM3860GQW-Z and adapted according circuits. 2. Connected DDR4-TEN signals together for U2, U3, U9, and U12 and pulled them low via 499 Ohm resistor R131. Added a testpoint TP3 for DDR4-TEN. 3. Changed voltage rail from 1.35 V to 1.45 V via adapting voltage divider resistors R33 and R38 and changed according voltage rail name PL_GT_1V35 to PL_GT_1V45. 4. Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R44 and R46 and changed according rail name PL_GT_1V05 to PL_GT_1V15. 5. Added diode D2 between U41 pin 3 net MR and voltage rail 3.3VIN. 6. Connected enable signal for U11 and U33 from "3.3VIN" to "PG_PL_VCCINT". 7. Added capacitors C137, C147, and C148 for VTT voltage rail. 8. Added resistors R132 (default: not fitted) and R133 to supply U4 VCC either from "PL_DCIN" or from "3.3VIN". 9. Change resistor R92 from 4.22 kOhm to 9.09 kOhm to set current limit to nearly 14.5 A for U4. 10. Added remote sense option: a. R134 for U30 b. R135 for U29 c. R136 for U31 11. Added decoupling capacitors: a. C210 and C211 for U5. b. C190 for U7. c. C198, C199, and C213 for U8. d. C153, C170...172 for U9 e. C196 C197, and C212 for U10. f. C156 and C157 for U12 g. C207 and C208 for U14. h. C189 for U17. i. C149...152, C205, and C206 for U18 j. C209 and C217 for U21. k. C214...216 for U22. l. C154 and C155 for U24 m. C188 and C191 for U26. n. C187 and C195 for U27. o. C203 and C204 for U34. p. C201 for U39. q. C202 for U40. r. C178 for U41. s. C200 for U44. 12. Added testpoints TP4, TP19, TP26. 13. Added UKCA logo. 14. Change 100 nF capacitors C135 and C136 from 6.3 V to 25 V for BOM optimization.	REV02[4]

4 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0813/REV02/Documents

Date	Revision	Changes	Documentation Link
-	REV 01	First Production Release	REV01[5]

Table 13: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

12.2 Document Change History

Date	Revision	Contributor	Description
2023-06-14	v.46(see page 5)	ED[6]	• Updated TRM to REV02.
2023-03-02	v.43	Martin Rohrmüller	• Corrected Note 4 about max DDR4 capacity
2023-01-16	v.41	ED	• Fixed issue in absolute maximum rating
2023-01-13	v.39	ED	• Initial Document
--	all	ED[7] , Martin Rohrmüller[8]	• --

Table 14: Document change history.

5 https://shop.trenz-electronic.de/de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0813/REV01/Documents
6 https://wiki.trenz-electronic.de/display/~e.dyck
7 https://wiki.trenz-electronic.de/display/~e.dyck
8 https://wiki.trenz-electronic.de/display/~m.rohrmueller

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2019-06-07

9 http://guidance.echa.europa.eu/
10 https://echa.europa.eu/candidate-list-table
11 http://www.echa.europa.eu/