TE0803 TRM

Revision v.55

Exported on 2024-09-24

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0803+TRM

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4 Overview

The Trenz Electronic TE0803 is an industrial grade MPSoC SOM integrating an AMD Zynq UltraScale+, DDR4 SDRAM with 64-Bit width data bus connection, SPI Boot Flash memory for configuration and operation, transceivers (SoC/Variant-dependent) and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking connections in a compact 5.2 cm x 7.6 cm form factor.

Refer to http://trenz.org/te0803-info for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC**
  - Device: ZU1 / ZU2 / ZU3 / ZU4 / ZU5 [1)]
  - Engine: CG / EG / EV [1)]
  - Speedgrade: -1 / -1L / -2 / -2L / -3 [1)]
  - Temperature Range: Extended / Industrial [1)]
  - Package: SFVC784
- **RAM/Storage**
  - 4 GByte DDR4 SDRAM [2) 3)]
  - 2 x 64 MByte Serial Flash [3)]
  - EEPROM with MAC address
- **On Board**
  - Clock Generator
  - Oscillator
- **Interface**
  - 4 x B2B Connector (ST5)
    - up to 204 PL IO
      - HP: 156
      - HD: 0 / 48 [3)]
    - up to 65 PS MIO
    - 4 GTR
    - 4 GTH (with ZU3T, ZU4 and higher)
    - I2C, JTAG, CONFIG
- **Power**
  - 3.3 V power supply via B2B Connector needed [5)].
- **Dimension**
  - 76 mm x 52 mm
- **Notes**

  [1)] Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.

  [2)] Up to 8 GByte are possible with a maximum bandwidth of 2400 MBit/s.

  [3)] Please, take care of the possible assembly options.

  [5)] Dependent on the assembly option a higher input voltage may be possible.

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4.2 Block Diagram

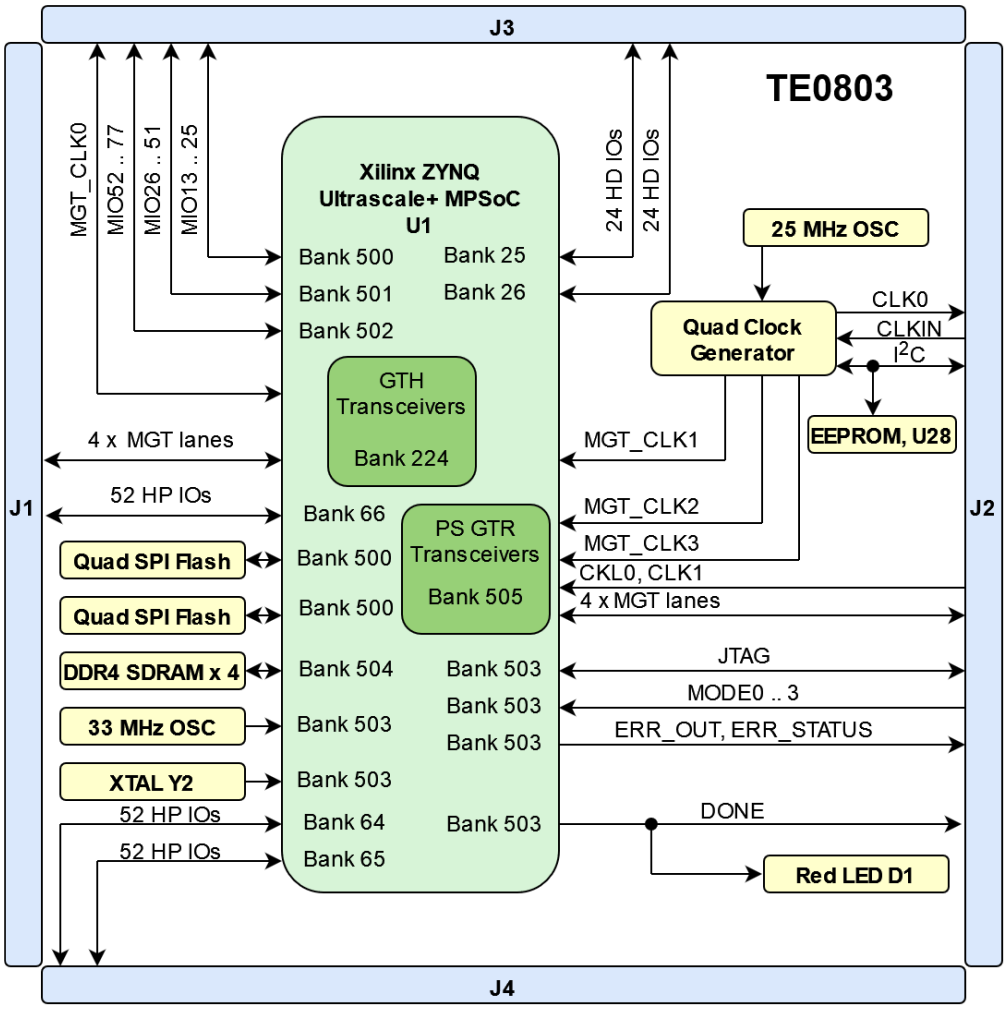

Figure 1: TE0808 block diagram

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4.3 Main Components

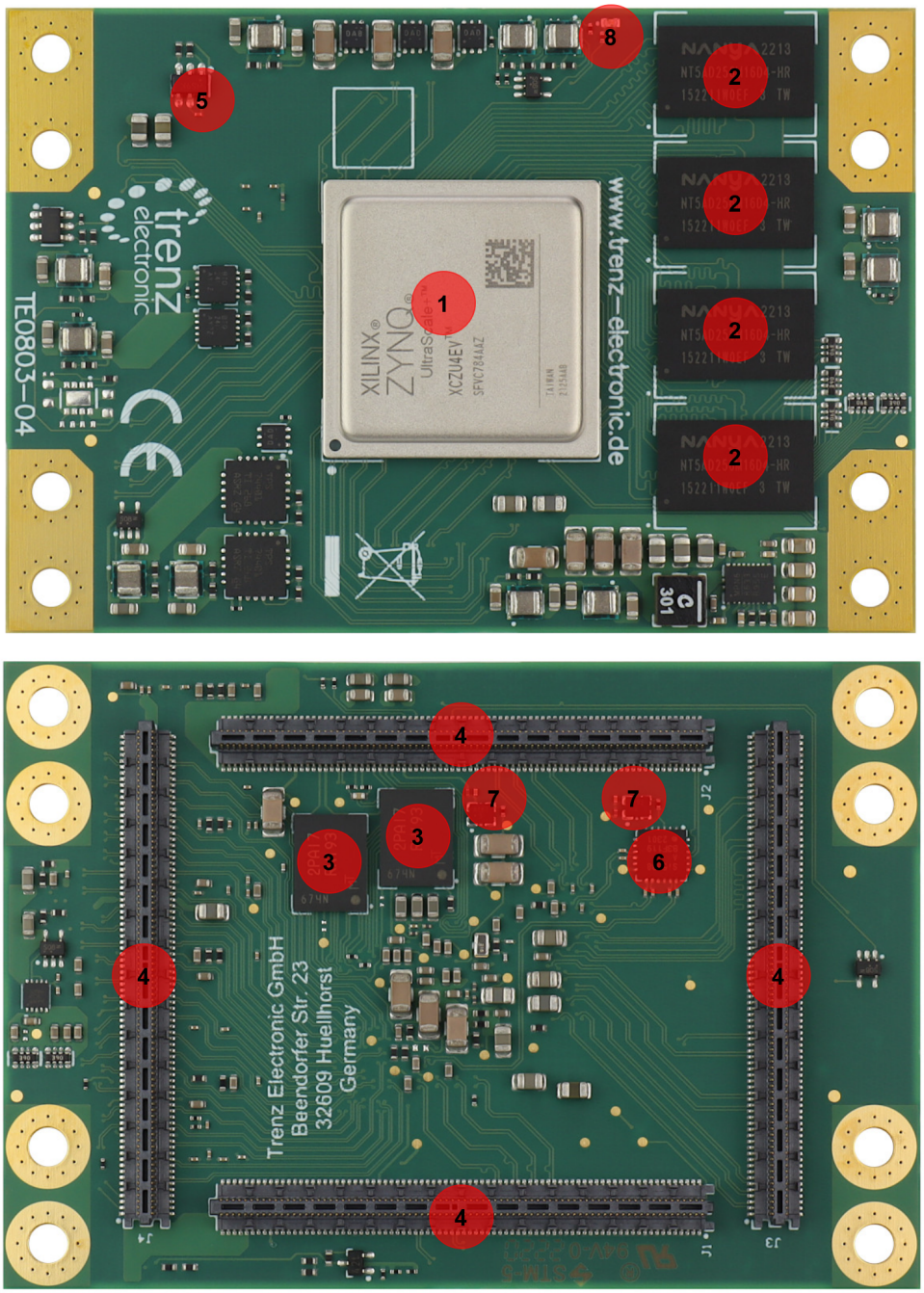

Figure 2: TE0803 main components

1. SoC, U1
2. DDR4, U2, U3, U9, U12
3. Quad SPI Flash, U7, U17
4. Connector, J1, J2, J3, J4
5. EEPROM, U28
6. Clock Generator, U5
7. Oscillator, U6, U32
8. Done LED D1

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4.4 Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash	not programmed	
EEPROM	not programmed besides factory programmed MAC address	
DDR4 SDRAM	not programmed	
Programmable Clock Generator	not programmed	

Table 1: Initial delivery state of programmable devices on the module

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5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	JM1	MGT PL	up to 4 x MGT (RX/TX)	Assembly option dependent.
B2B	JM1	HP	52 SE / 24 DIFF	
B2B	JM2	MGT PS	2 x MGT CLK	
B2B	JM2	CLK	2 x DIFF CLK	PLL, 1 x Input, 1 x Output
B2B	JM2	MGT PS	4 x MGT (RX/TX)	
B2B	JM2	CFG[1)]	1x JTAG	
B2B	JM2	CFG[1)]	4x MODE	
B2B	JM2	CFG[1)]	1 x I2C	PLL, EEPROM
B2B	JM2	CFG[1)]	29 CTRL/Status	
B2B	JM3	HD	up to 48 SE / 24 DIFF	Assembly option dependent.
B2B	JM3	MGT PL	MGT CLK	
B2B	JM3	MIO	65 GPIO	
B2B	JM4	HP	104 SE / 48 DIFF	

Table 2: Board Connectors

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1) see Configuration and System Control Signals (see page 13)

5.2 Test Points

Test Point	Signal	Notes[1)]
TP1	PLL_SCL	pulled-up to PS_1V8
TP2	PLL_SDA	pulled-up to PS_1V8
TP3	GND	
TP4	GND	
TP5	GND	
TP6	PL_1V8	
TP7	GND	
TP8	GND	
TP9	PL_VCCINT_IO	
TP10	GND	
TP11	PL_VCCINT	
TP12	PL_VCU_0V9	
TP13	FP_0V85	
TP14	PS_1V8	
TP15	GND	
TP16	DDR_2V5	

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Test Point	Signal	Notes[1)]
TP17	DDR_PLL	
TP18	DDR_1V2	
TP20	MGTAVTT	
TP21	VTT	
TP22	PL_GT_1V05	
TP23	VREFA	
TP24	MGTVCCAUX	
TP25	MGTAVCC	
TP27	PS_PLL	
TP28	PS_AVTT	
TP29	LP_0V85	
TP30	PS_AUX	
TP31	PS_AVCC	
TP32	PS_CLK	
TP34	POR_B	pulled-up to PS_1V8

Table 3: Test Points Information

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

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6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
DDR4 SDRAM	U2, U3, U9, U12	SoC - PS	
Quad SPI Flash	U7, U17	SoC - PS	Booting.
EEPROM	U28	B2B - J2	
Clock Generator	U5	B2B - J2 SoC -MGT	
Oscillator	U6	Clock Generator	25 MHz
Oscillator	U32	SoC	33.333333 MHz

Table 4: On board peripherals

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7 Configuration and System Control Signals

Connector+ Pin	Signal Name	Direction[1)]	Description
J2-82	PG_PSGT	OUT	GTR transceivers powered-up.
J2-83	MR	IN	Manual reset.
J2-84	EN_PSGT	IN	Enable GTR transceiver power-up.
J2-86	ERR_STATUS	OUT	PS error status [2)].
J2-88	ERR_OUT	OUT	PS error indication [2)].
J2-90	PLL_SCL	IN	I2C clock. Pulled up to PS_1V8.
J2-91	PG_GT_R	OUT	Right GTH Transceivers powered-up.
J2-92	PLL_SDA	IN/OUT	I2C data. Pulled up to PS_1V8.
J2-95	EN_GT_R	IN	Enable right GTH transceiver power-up.
J2-96	SRST_B	IN	System reset [2)]. Pulled-up to PS_1V8.
J2-97	PG_VCU	OUT	VCU powered-up.
J2-98	INIT_B	IN/OUT	Initialization completion indicator after POR [2)]. Pulled-up to PS_1V8.
J2-100	PROG_B	IN/OUT	Power-on reset [2)]. Pulled-up to PS_1V8.

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Connector+ Pin	Signal Name	Direction[1)]	Description
J2-101	EN_PL	IN	Enable programable logic power-up.
J2-102	EN_FPD	IN	Enable full-power domain power-up.
J2-103 / J2-105 / J2-107 / J2-109	MODE3. .0	IN	Boot mode selection [2)]: • JTAG • QUAD-SPI (32 Bit) • SD1 (2.0) • eMMC (1.8 V) • SD1 LS (3.0) Supported Modes depends also on used Carrier.
J2-104	PG_PL	OUT	Programmable logic powered-up. Pulled-up to PL_DCIN.
J2-106	LP_GOOD	OUT	Low-power domain powered-up. Pulled up to LP_DCDC.
J2-108	EN_LPD	IN	Enable low-power domain power-up.
J2-110	PG_FPD	OUT	Full-power domain powered-up. Pulled-up to DCDCIN.
J2-112	EN_DDR	IN	Enable DDR power-up.
J2-114	PG_DDR	OUT	DDR power supply powered-up. Pulled-up to DCDCIN.
J2-116	DONE	OUT	PS done signal [2)]. Pulled-up to PS_1V8.
J2-119 / J2-121	DX_P / DX_N	-	SoC temperatur sensing diode pins [2)].
J2-120 / J2-122 / J2-124 / J2-126	TCK / TDI / TDO / TMS	Signal-dependent	JTAG configuration and debugging interface. JTAG reference voltage: PS_1V8

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Connector+ Pin	Signal Name	Direction[1)]	Description
J2-125	PSBATT	IN	PS RTC Battery supply voltage [2) 3)].
J2-127	PUDC_B	IN	Configuration pull-ups setting [2)]. Pulled-up to PL_1V8.

Table 5: Controller signal.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

[2)] See UG1085 for additional information.

[3)] See Recommended Operating Conditions (see page 25).

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8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector + Pin	Direction[1)]	Notes
VCCO_66	J1-90 / J1-120	IN	
VREF_66	J1-108	IN	
PL_1V8	J1-91 / J1-121	OUT	
PL_DCIN	J1-151 / J1-153 / J1-155 / J1-157 / J1-159	IN	
LP_DCDC	J2-138 / J2-140 / J2-142 / J2-144	IN	
DCDCIN	J2-153 / J2-154 / J2-155 / J2-156 / J2-157 / J2-158 / J2-159 / J2-160	IN	
PS_1V8	J2-99 / J3-147 / J3-148	OUT	
PS_BATT	J2-125	IN	
DDR_1V2	J2-135	OUT	
VCCO_25	J3-15 / J3-16	IN	
VCCO_26	J3-43 / J3-44	IN	
GT_DCDC	J3-157 / J3-158 / J3-159 / J3-160	IN	
VCCO_64	J4-58 / J4-106	IN	
VREF_64	J4-88	IN	

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Power Rail Name/ Schematic Name	Connector + Pin	Direction[1)]	Notes
VCCO_65	J4-69 / J4-105	IN	
VREF_65	J4-15	IN	

Table 6: Module power rails.

[1)] Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals (see page 13).
1 [1)]	PSBATT	1.2 V ... 1.5 V	-	Battery connection.	Battery Power Domain usage. When not used, tie to GND.
2	Processing System (PS):			Procedure for PS starting.	
2.1	Low-power domain:			Bring-up for low-power domain PS.	
2.1.1	LP_DCDC	3.3 V (± 5 %) [2)]	-	Low-power domain power supply.	Main module power supply for low-power domain. 5.5 A recommended. Power consumption depends

Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
					mainly on design and cooling solution.
2.1.2	EN_LPD	-	-	Low-power domain power enable.	
2.1.3	LP_GOOD	-	PU [3], LP_DCDC	Low-power domain power good status.	Module power-on sequencing for low-power domain finished.
2.2	Full-power domain:			Bring-up for full-power domain PS.	Full-power PS domain needs powered low-power PS domain.
2.2.1	DCDCIN	3.3 V (± 5 %) [2]		Full-power domain and GTR transceiver power supply.	Main module power supply for full-power domain. 7 A recommended. Power consumption depends mainly on design and cooling solution.
2.2.2	EN_FPD	DCDCIN	-	Full-power domain power enable.	
2.2.3	PG_FPD	-	PU [3], DCDCIN	Full-power domain power good status.	Module power-on sequencing for full-power domain finished.
2.2.4	EN_DDR	DCDCIN	-	DDR memory power enable.	

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Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2.2.5	PG_DDR	-	PU [3], DCDCIN	DDR memory power good status.	Module power-on sequencing for DDR memory finished.
2.3	GTR Transceiver			Procedure for GTR transceiver starting.	PS transceiver usage needs powered PS (low- and full-power domain).
2.3.1	EN_PSGT	DCDCIN	-	GTR transceiver power enable.	
2.3.2	PG_PSGT	-	-	GTR transceiver power good status.	Module power-on sequencing for GTR transceiver finished.
2	Programmable Logic (PL)			Procedure for PL starting.	PL usage needs powered PS low-power domain.
2.1	PL_DCIN	3.3 V (± 5 %) [2]	-	Programmable logic power supply.	Main module power supply for programmable logic. 12 A recommended. Power consumption depends mainly on design and cooling solution.
2.2	EN_PL	-	PU [3], PL_DCIN	Programmable logic power enable.	
2.3	PG_PL	-	PU [3], PL_DCIN	Programmable logic power good status.	Module power-on sequencing for programmable logic finished. Periphery and variable bank voltages can be enabled on carrier.

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Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
2.4	PG_VCU	-	PU [3], PL_DCIN	Video codec unit power good status.	Assembly variant dependent.
2.5	VCCO_25 / VCCO_26 / VCCO_64 / VCCO_65 / VCCO_66	[4]	-	Module bank voltages.	Enable bank voltages after PG_PL deassertion.
3	GTH / GTY Transceiver			Procedure for GTH / GTY transceiver starting.	PL transceiver usage needs powered PL and low-power PS domain.
3.1	GT_DCDC	3.3 V (± 5 %) [2]	-	GTH transceiver power supply.	Main module power supply for GTH transceiver. 5 A recommended. Power consumption depends mainly on design and cooling solution.
3.2	EN_GT_R	GT_DCDC	-	GTH right transceiver power enable.	
3.3	PG_GT_R	-	-	GTH transceiver power good status.	

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Sequence	Net name	Recommended Voltage Range	Pull-up/ down	Description	Notes
4	MR			Manual Reset	Low active release after all needed power domains are enabled.

Table 7: Baseboard Design Hints

[1] Optional

[2] Dependent on the assembly option a higher input voltage may be possible.

[3] On module

[4] See DS925 for additional information.

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9 Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5[1]) on the bottom side.

- 4x REF-192552-02 (160-pins)
  - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5[2]) on the top side.

- 4x REF192552-01 (160-pins)
  - SS5 Mates with ST5

9.1 Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5
- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

9.2 Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5mm	Standard connector used on carrier
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	Standard connector

1 https://www.samtec.com/products/st5
2 https://www.samtec.com/products/st5

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Order number	REF number	Samtec Number	Type	Contribution to stacking height	Comment
					used on modules
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	Assembly option on request

Table 8: Connectors.

The module can be manufactured using other connectors upon request.

9.3 Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

9.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

Table 9: Speed rating.
The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

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10 Technical Specifications

10.1 Absolute Maximum Ratings *)

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
LP_DCDC	Micromodule Power	-0.300	4.0	V
DCDCIN	Micromodule Power	-0.300	6.5	V
GT_DCDC	Micromodule Power	-0.300	6.0	V
PL_DCIN	Micromodule Power	-0.300	4.0	V
PS_BATT	RTC / BBRAM	-0.500	2.000	V
VCCO_25	HD IO Bank power supply	-0.500	3.400	V
VCCO_26	HD IO Bank power supply	-0.500	3.400	V
VCCO_64	HP IO Bank power supply	-0.500	2.000	V
VCCO_65	HP IO Bank power supply	-0.500	2.000	V
VCCO_66	HP IO Bank power supply	-0.500	2.000	V
VREF_64	Bank input reference voltage	-0.500	2.000	V

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Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VREF_65	Bank input reference voltage	-0.500	2.000	V
VREF_66	Bank input reference voltage	-0.500	2.000	V

Table 10: Absolute maximum ratings

*) Stresses beyond those listed under Absolute Maximum Ratings (see page 24) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition (see page 0). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: Article Number Information[3]
- Modules with commercial temperature grade are equipped with components that cover at least the range of 0°C to 75°C
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C
- The actual operating temperature range will depend on the FPGA / SoC design / usage and cooling and other variables.

Parameter	Min	Max	Units	Reference Document
LP_DCDC 1)	3.135	3.465	V	
DCDCIN 1)	3.135	3.465	V	
GT_DCDC 1)	3.135	3.465	V	

3 https://wiki.trenz-electronic.de/display/PD/Article+Number+Information

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Parameter	Min	Max	Units	Reference Document
PL_DCIN [1)]	3.135	3.465	V	
PS_BATT	1.200	1.500	V	See FPGA datasheet.
VCCO_25	1.140	3.400	V	See FPGA datasheet.
VCCO_26	1.140	3.400	V	See FPGA datasheet.
VCCO_64	0.950	1.900	V	See FPGA datasheet.
VCCO_65	0.950	1.900	V	See FPGA datasheet.
VCCO_66	0.950	1.900	V	See FPGA datasheet.
VREF_64	0.6	1.2	V	See FPGA datasheet.
VREF_65	0.6	1.2	V	See FPGA datasheet.
VREF_66	0.6	1.2	V	See FPGA datasheet.

Table 11: Recommended operating conditions.

[1)] Higher values may possible. For more information consult schematic and according datasheets.

10.3 Physical Dimensions

- Module size: 76 mm × 52 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.

PCB thickness: 1.740 mm (± 10 %).

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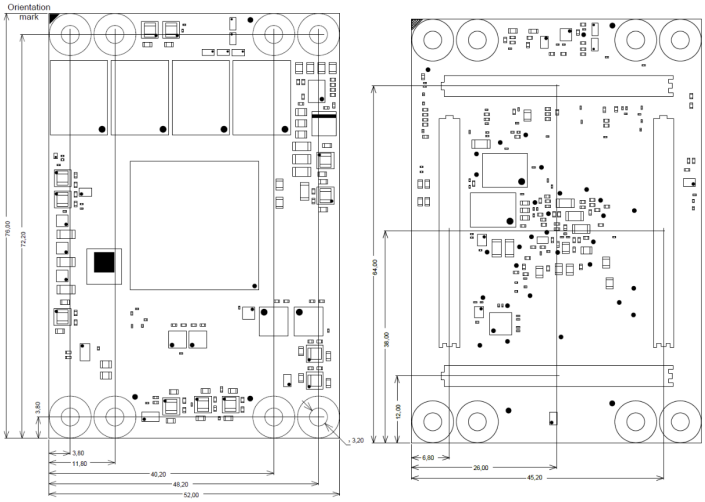

Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0803 overview page	
English page[4]	German page[5]

Table 12: Trenz Electronic Shop Overview

4 https://shop.trenz-electronic.de/en/search?sSearch=TE0803
5 https://shop.trenz-electronic.de/de/search?sSearch=TE0803

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12 Revision History

12.1 Hardware Revision History

Figure 4: Board hardware revision number.

Date	Revision	Changes	Documentation Link
2020-12-15	04	• Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; • Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; • Added option to select POR_OVERRIDE level (R12 and R93) • VCCO pins for unused Bank 44 connected together. Same for unused Bank 24 (UG583 recomendation) • PCB: updated signal trace lengths. • PCB: updated silkscreen. Added company address, CE and WEEE symbols; • PCB: added module orientation rectangle pointer • Changed resistor values of R29, R31, R35, R39, R44-R47 (BOM optimization) • Removed traceability part (Obsolete component) • Changed capacitor C92 for all variants from 100 nF to 1 nF. • U4 can be either TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.	TE0803-04[6]

6 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/REV04/Documents

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Date	Revision	Changes	Documentation Link
2019-03-18	03	• Added support of DDP DDR4 • Added support of Low power FPGA (-L1/L2). • Revised testpoints • Revised J1-J4 connectors net label style	TE0803-03[7]
2018-07-19	02	• Added LDO to DDR_PLL • All differential pairs length matched with tollerance 0.1mm (excluding package delays) • Added MAC EEPROM U28 • VPS_MGTRAVCC set to 0.85V • Added pull-up resistors R68, R69	TE0803-02[8]
2016-12-23	01	First production release	TE0803-01[9]

Table 13: Hardware Revision History
Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

12.2 Document Change History

Date	Revision	Contributor	Description
2024-09-24	v.55 (see page 5)	John Hartfiel[10]	• Review and publishing
2023-10-06	v.52	ED	• Updated to new TRM style • Updated for REV04
2022-05-19	v.51	ED	• Added note regarding DCDC U4.
2022-02-25	v.50	John Hartfiel	• Add Note to PLL
2022-02-08	v.46	John Hartfiel	• Correction on Power section

7 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/REV03/Documents
8 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/REV02/Documents
9 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/REV01/Documents
10 https://wiki.trenz-electronic.de/display/~j.hartfiel

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Date	Revision	Contributor	Description
			• Correction GTH Clock connection
2021-05-17	v.41	John Hartfiel	• typo correction in DDR section
2021-03-11	v.40	John Hartfiel	• typo • fixed MGT Lanes RX/TX order
2019-07-15	v.36	John Hartfiel	• correction SPLL section
2019-07-02	v.35	John Hartfiel	• add eeprom section • update PCB Revision section
2019-06-19	v.33	John Hartfiel	• update links • correction flash section
2018-08-20	v.29	John Hartfiel	• power section: add missing PS_1V8 output pin
2018-08-06	v.28	John Hartfiel	• typo correction
2017-11-13	v.23	Ali Naseri	• updated B2B connector max. current rating per pin
2017-11-13	v.19	John Hartfiel	• rework B2B section
2017-10-19	v.18	John Hartfiel	• Removed ES1 Note
2017-08-15	v.17	Vitali Tsiukala	• Changed Signals Count in the table B2B-connectors
2017-08-07	v.14	Jan Kumann	• New smaller images. • New QSPI Flash MIO mapping table. • Temperature information changes. • Few corrections.
2017-05-17	V.4	Ali Naseri	Current TRM release.

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Date	Revision	Contributor	Description
2017-05-10	v.1	Ali Naseri	Initial document.
--	all	Vitali Tsiukala[11] , Ali Naseri[12] , Antti Lukats[13] , ED[14] , GH[15] , John Hartfiel[16] , Jan Kumann[17] , Martin Rohrmüller[18] , Susanne Kunath[19] , Thorsten Trenz[20]	• --

Table 14: Document change history.

11 https://wiki.trenz-electronic.de/display/~Vitali.Tsiukala
12 https://wiki.trenz-electronic.de/display/~a.naseri
13 https://wiki.trenz-electronic.de/display/~antti.lukats
14 https://wiki.trenz-electronic.de/display/~e.dyck
15 https://wiki.trenz-electronic.de/display/~gherrera
16 https://wiki.trenz-electronic.de/display/~j.hartfiel
17 https://wiki.trenz-electronic.de/display/~j.kumann
18 https://wiki.trenz-electronic.de/display/~m.rohrmueller
19 https://wiki.trenz-electronic.de/display/~s.kunath
20 https://wiki.trenz-electronic.de/display/~tht

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2019-06-07

21 http://guidance.echa.europa.eu/
22 https://echa.europa.eu/candidate-list-table
23 http://www.echa.europa.eu/

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