REV	Description	
-01	Initial revision	MT

Title: TEG2000 - Changes list		
A4	Number: TEG2000 A1I-1A	Rev. 01
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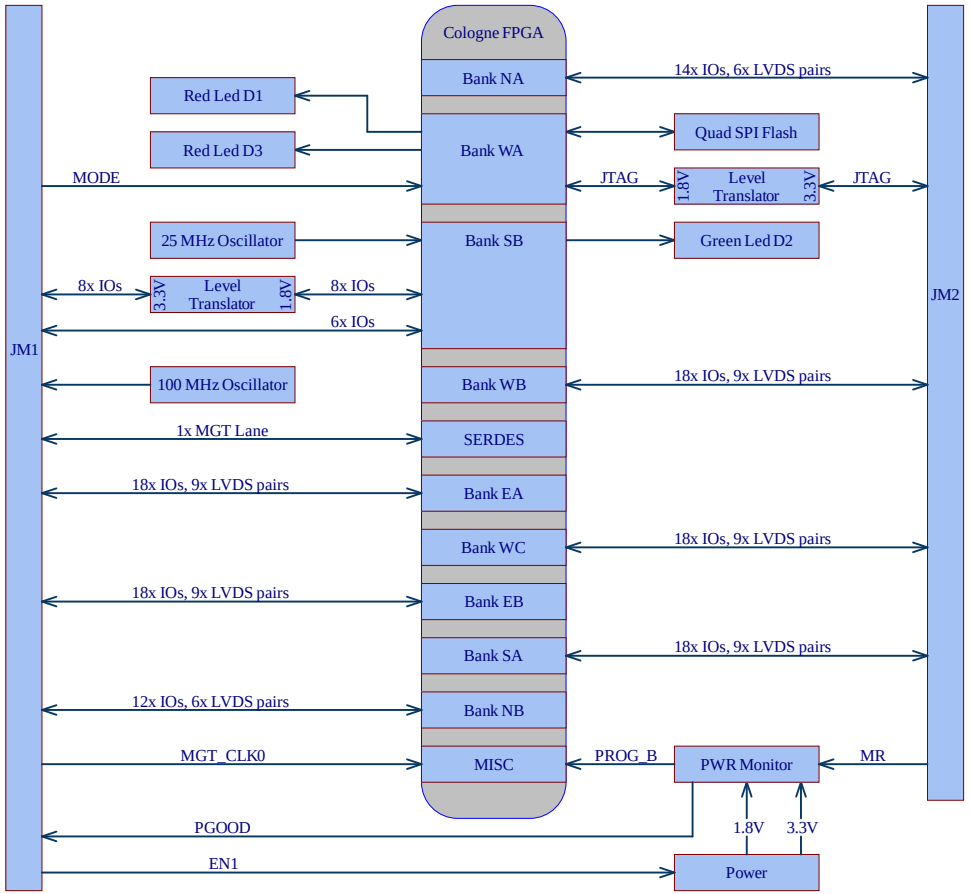
Filename: Revision_Changes.SchDoc		

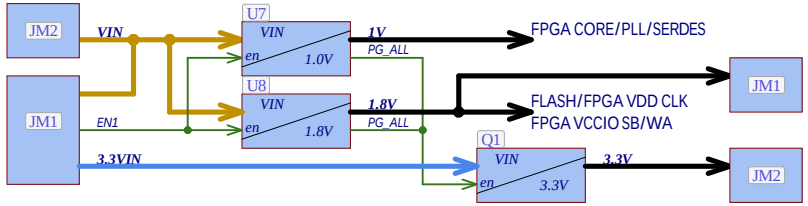
System Overview



TEG2000.SchDoc

FPGA-PWR.SchDoc

Power Sequence



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIOA	IN	1.1 - 2.7V	+/-3%	IO Banks NB/EB/EA	-
VCCIOC	IN	1.1 - 2.7V	+/-3%	IO Bank SA	-
VCCIOD	IN	1.1 - 2.7V	+/-5%	IO Banks NA/WB/WC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-5%	Power for Carrier	-

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Title: TEG2000 - System Overview

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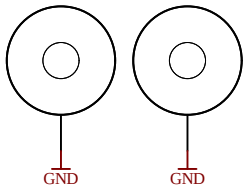
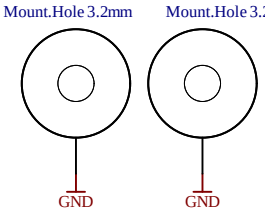
Mount.Hole 3.2mm



Mount.Hole 3.2mm



Serial

Serial

Serialnumber 6,3 x 6.3mm

LOGO

TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

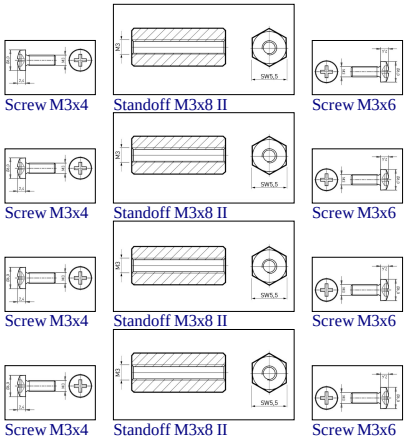
RoHS-TOPOVERLAY

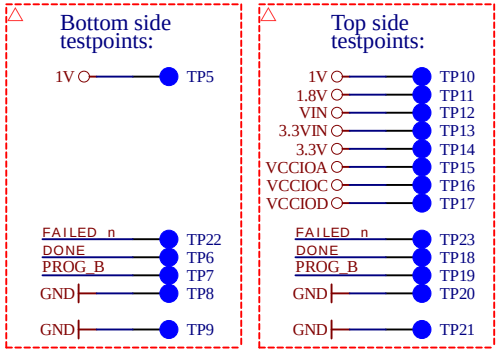
WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

Top of Board





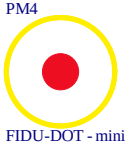
Special notes:

Based on P001

PM1

FIDU-DOT - mini

PM4

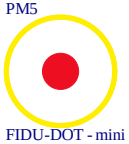


FIDU-DOT - mini

PM2

FIDU-DOT - mini

PM5

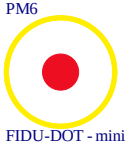


FIDU-DOT - mini

PM3

FIDU-DOT - mini

PM6



FIDU-DOT - mini

Assembly variant	A1I-1A
Created by	MT
Modified by	-
Modified at	-
SVN Revision	18871 [Locally Modified]

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Title: TEG2000		
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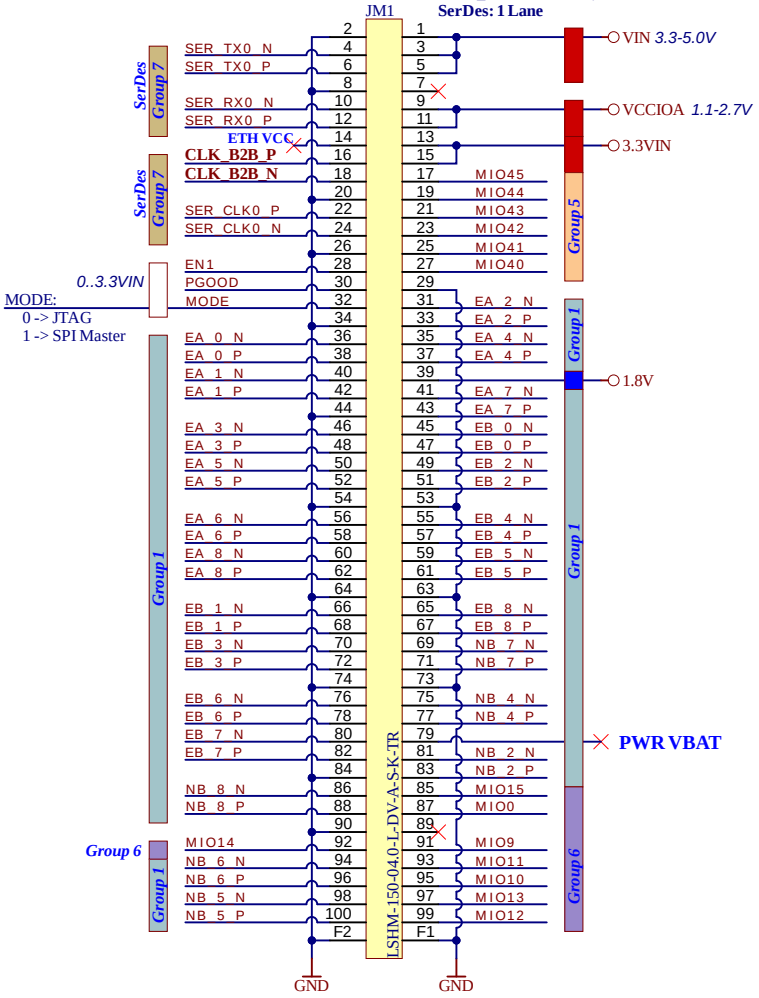
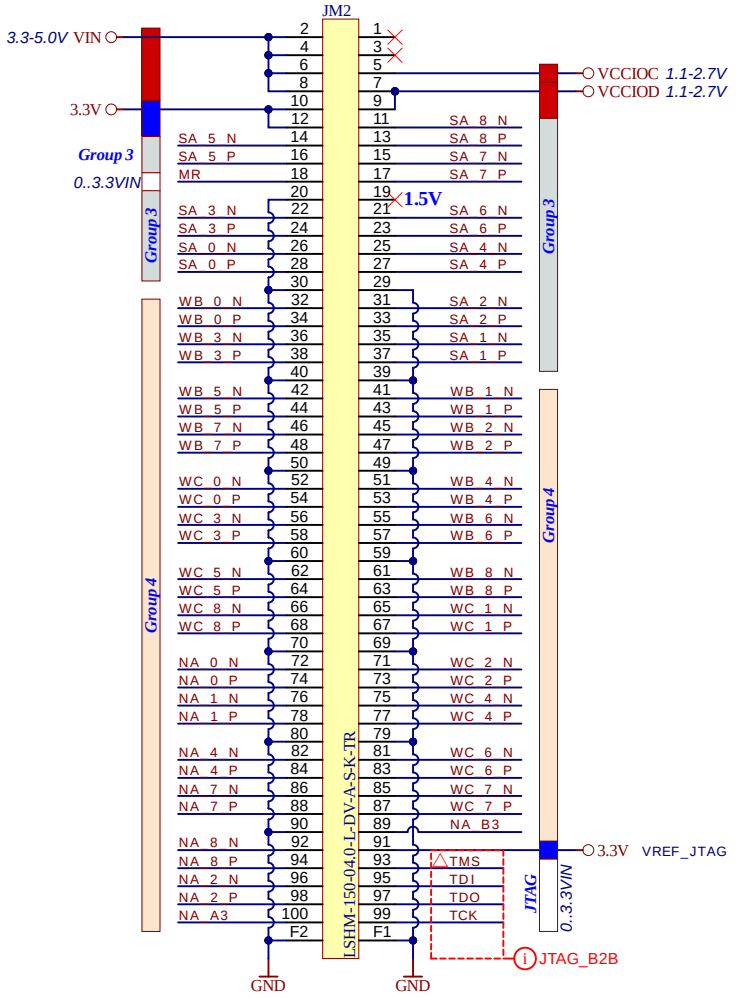
Bank_EA: 18 Single ended, 9 Differential pairs, Variable VCCIOA
Bank_EB: 18 Single ended, 9 Differential pairs, Variable VCCIOA
Bank_NB: 12 Single ended, 6 Differential pairs, Variable VCCIOA
Bank_SB: 6 MIO Pins, 1.8V Fixed VCCIO
Bank_SB: 8 MIO Pins, 3.3V Fixed VCCIO
SerDes: 1 Lane



Bank_SA: 18 Single ended, 9 Differential pairs, Variable VCCIOC
Bank_WB: 18 Single ended, 9 Differential pairs, Variable VCCIOD
Bank_WC: 18 Single ended, 9 Differential pairs, Variable VCCIOD
Bank_NA: 14 Single ended, 6 Differential pairs, Variable VCCIOD
JTAG: 4 Pins 3.3V



VCCIOA	1.1..2.7V
VCCIOC	1.1..2.7V
VCCIOD	1.1..2.7V
Group 1	0..VCCIOA
Group 3	0..VCCIOC
Group 4	0..VCCIOD
Group 5	0..1.8V
Group 6	0..3.3V
Group 7	SerDes
Special	
	PWR_in
	PWR_out

Some information about Trenz modules compatibility and differences here

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Title: TEG2000 - B2B Connectors		
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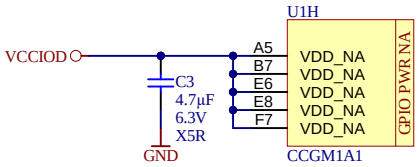
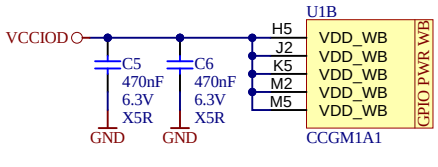
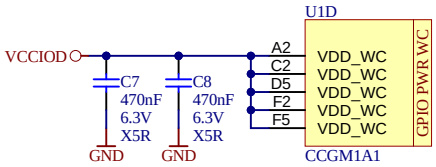
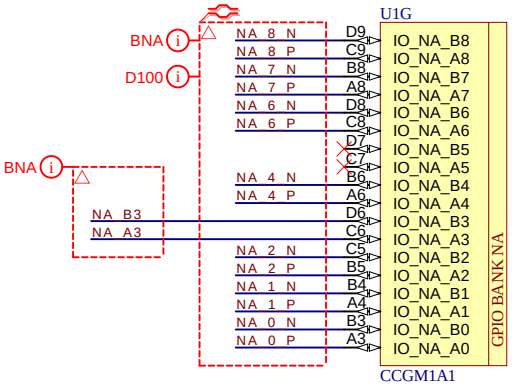
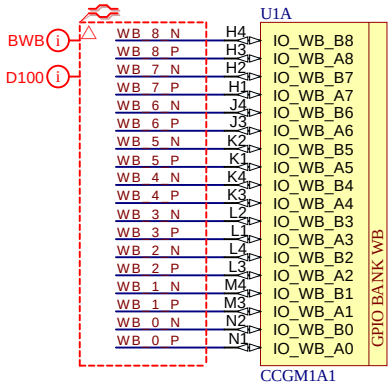
Filename: B2B-Connectors.SchDoc		

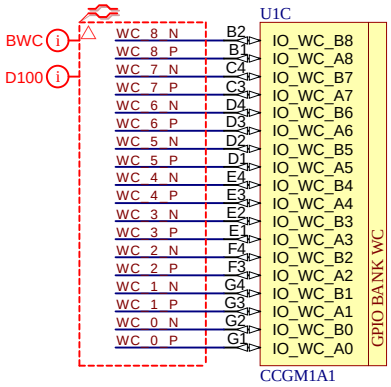


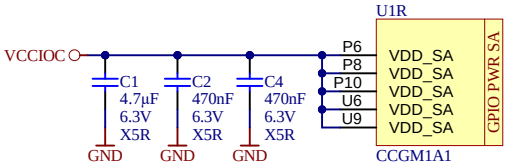


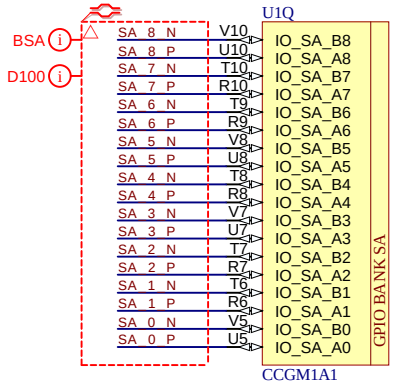


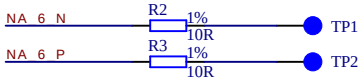












trenz electronic	Title: TEG2000 - Banks NA/WB/WC/SA		
	A4	Number: TEG2000 A1I-1A	Rev. 01
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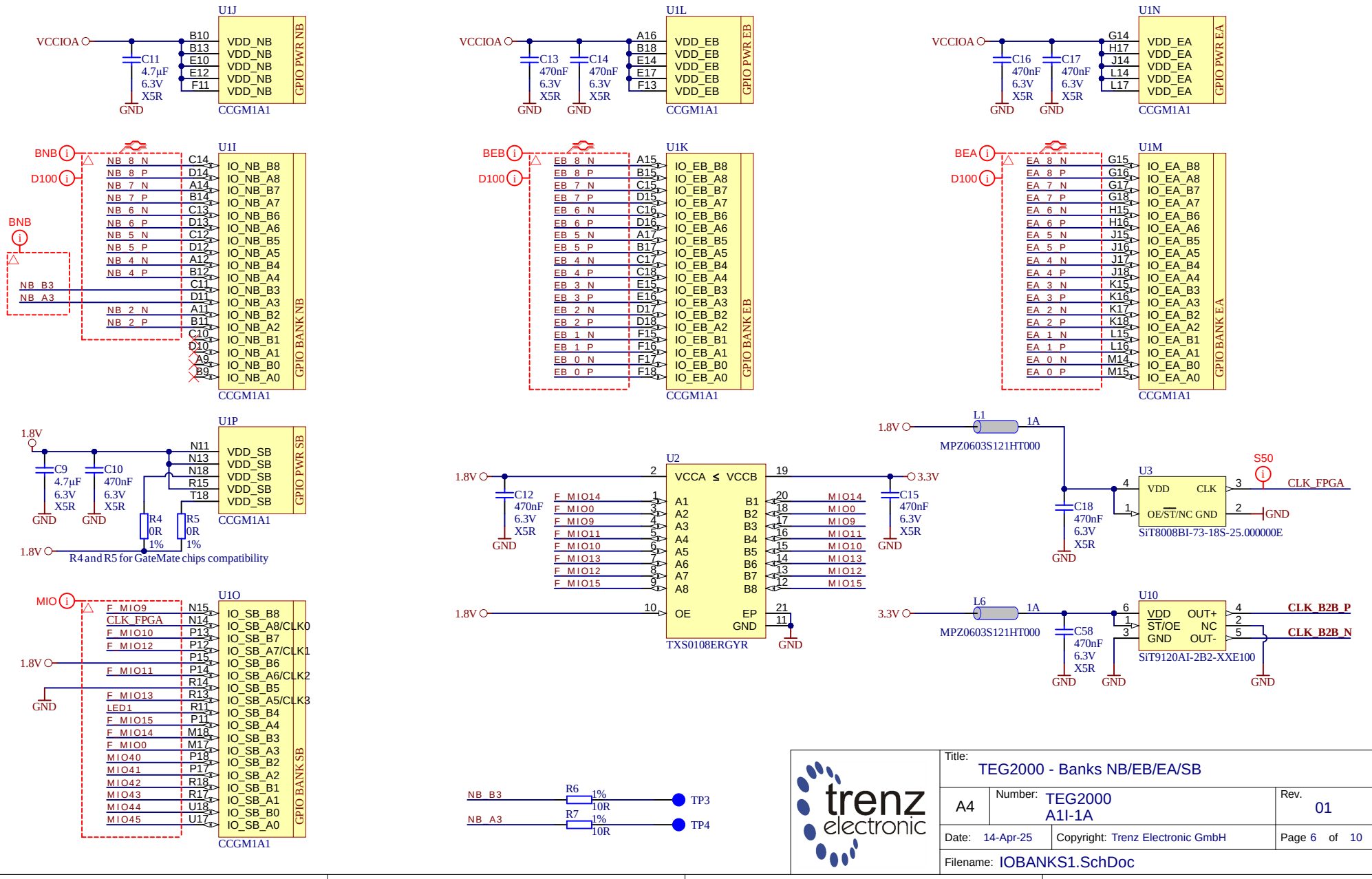
	Filename: IOBANKS0.SchDoc		


U1J
VCCIOA
B10
B13
E10
E12
F11
VDD_NB
VDD_NB
VDD_NB
VDD_NB
VDD_NB
GPIO PWR NB
C11
4.7µF
6.3V
X5R
GND
CCGM1A1
U1L
VCCIOA
A16
B18
E14
E17
F13
VDD_EB
VDD_EB
VDD_EB
VDD_EB
VDD_EB
GPIO PWR EB
C13
470nF
6.3V
X5R
C14
470nF
6.3V
X5R
GND
GND
CCGM1A1
U1N
VCCIOA
G14
H17
J14
L14
L17
VDD_EA
VDD_EA
VDD_EA
VDD_EA
VDD_EA
GPIO PWR EA
C16
470nF
6.3V
X5R
C17
470nF
6.3V
X5R
GND
GND
CCGM1A1
U1I
BNB
D100
BNB
NB_8_N
NB_8_P
NB_7_N
NB_7_P
NB_6_N
NB_6_P
NB_5_N
NB_5_P
NB_4_N
NB_4_P
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NB_A3
NB_2_N
NB_2_P
C14
D14
A14
B14
C13
D13
C12
D12
A12
B12
C11
D11
A11
B11
C10
D10
A9
B9
IO_NB_B8
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IO_NB_B7
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IO_NB_B5
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IO_NB_B1
IO_NB_A1
IO_NB_B0
IO_NB_A0
GPIO BANK NB
CCGM1A1
U1K
BEB
D100
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EB_1_P
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EB_0_P
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B15
C15
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C16
D16
A17
B17
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C18
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E16
D17
D18
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F16
F17
F18
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IO_EB_A8
IO_EB_B7
IO_EB_A7
IO_EB_B6
IO_EB_A6
IO_EB_B5
IO_EB_A5
IO_EB_B4
IO_EB_A4
IO_EB_B3
IO_EB_A3
IO_EB_B2
IO_EB_A2
IO_EB_B1
IO_EB_A1
IO_EB_B0
IO_EB_A0
GPIO BANK EB
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U1M
BEA
D100
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EA_8_P
EA_7_N
EA_7_P
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L16
M14
M15
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IO_EA_A8
IO_EA_B7
IO_EA_A7
IO_EA_B6
IO_EA_A6
IO_EA_B5
IO_EA_A5
IO_EA_B4
IO_EA_A4
IO_EA_B3
IO_EA_A3
IO_EA_B2
IO_EA_A2
IO_EA_B1
IO_EA_A1
IO_EA_B0
IO_EA_A0
GPIO BANK EA
CCGM1A1
U1P
1.8V
C9
4.7µF
6.3V
X5R
C10
470nF
6.3V
X5R
GND
GND
R4
0R
1%
R5
0R
1%
1.8V
N11
N13
N18
R15
T18
VDD_SB
VDD_SB
VDD_SB
VDD_SB
VDD_SB
GPIO PWR SB
CCGM1A1
R4 and R5 for GateMate chips compatibility
U2
1.8V
C12
470nF
6.3V
X5R
GND
F_MIO14
F_MIO0
F_MIO9
F_MIO11
F_MIO10
F_MIO13
F_MIO12
F_MIO15
1.8V
2
1
3
4
5
6
7
8
9
10
VCCA
VCCB
A1
A2
A3
A4
A5
A6
A7
A8
OE
19
20
18
17
16
15
14
13
12
21
11
B1
B2
B3
B4
B5
B6
B7
B8
EP
GND
MIO14
MIO0
MIO9
MIO11
MIO10
MIO13
MIO12
MIO15
3.3V
C15
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GND
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C18
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X5R
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U3
VDD
CLK
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S50
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GND
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OUT+
NC
OUT-
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4
2
5
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CLK_B2B_N
SiT9120AI-2B2-XXE100
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MIO
F_MIO9
CLK_FPGA
F_MIO10
F_MIO12
1.8V
F_MIO11
GND
F_MIO13
LED1
F_MIO15
F_MIO14
F_MIO0
MIO40
MIO41
MIO42
MIO43
MIO44
MIO45
N15
N14
P13
P12
P15
P14
R14
R13
R11
P11
M18
M17
P18
P17
R18
R17
U18
U17
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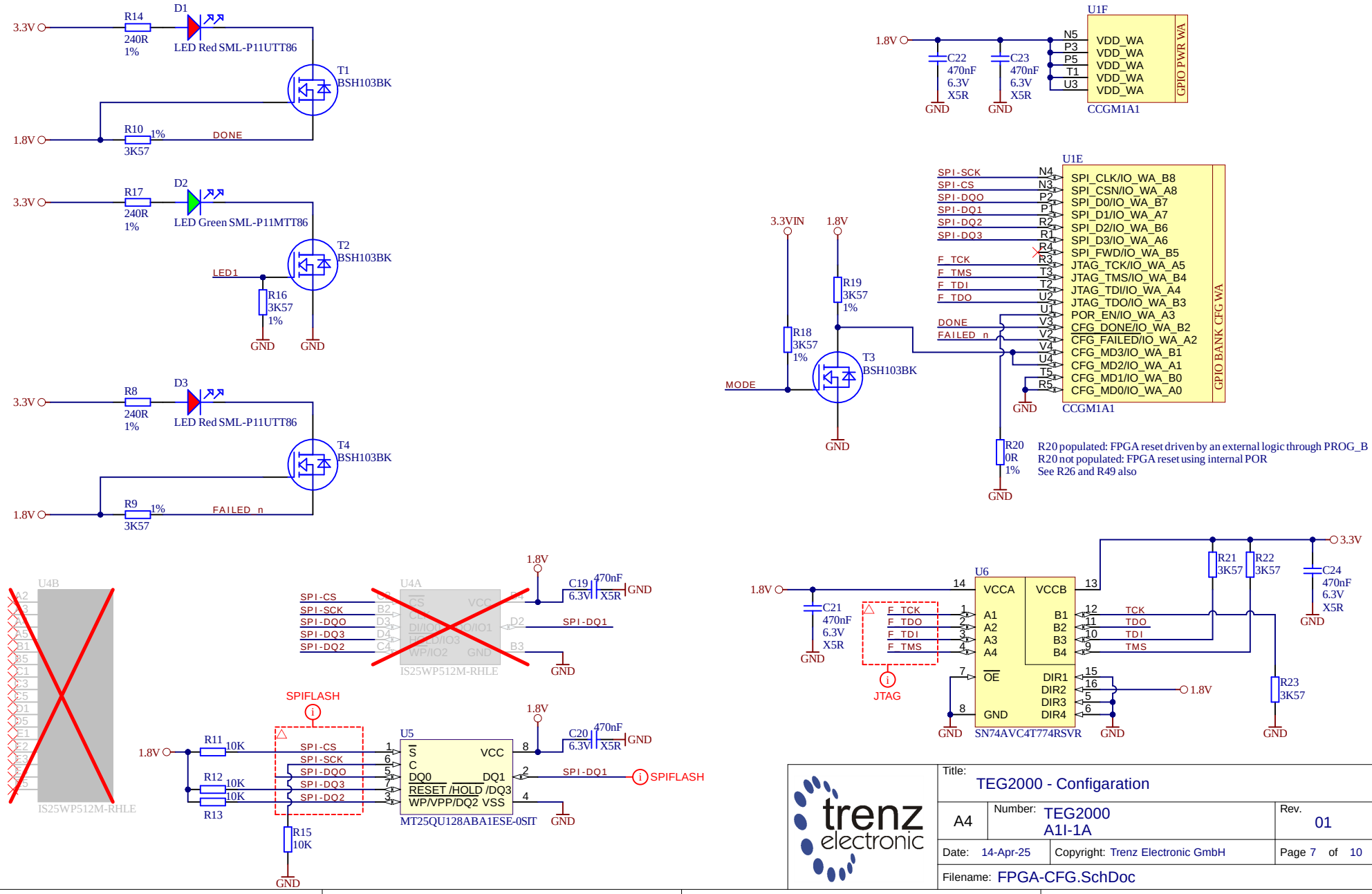
IO_SB_B7
IO_SB_A7/CLK1
IO_SB_B6
IO_SB_A6/CLK2
IO_SB_B5
IO_SB_A5/CLK3
IO_SB_B4
IO_SB_A4
IO_SB_B3
IO_SB_A3
IO_SB_B2
IO_SB_A2
IO_SB_B1
IO_SB_A1
IO_SB_B0
IO_SB_A0
GPIO BANK SB
CCGM1A1
NB_B3
R6
1%
10R
TP3
NB_A3
R7
1%
10R
TP4
trenz
electronic
Title:
TEG2000 - Banks NB/EB/EA/SB
A4
Number:
TEG2000
A1I-1A
Rev.
01
Date:
14-Apr-25
Copyright:
Trenz Electronic GmbH
Page 6 of 10
Filename:
IOBANKS1.SchDoc



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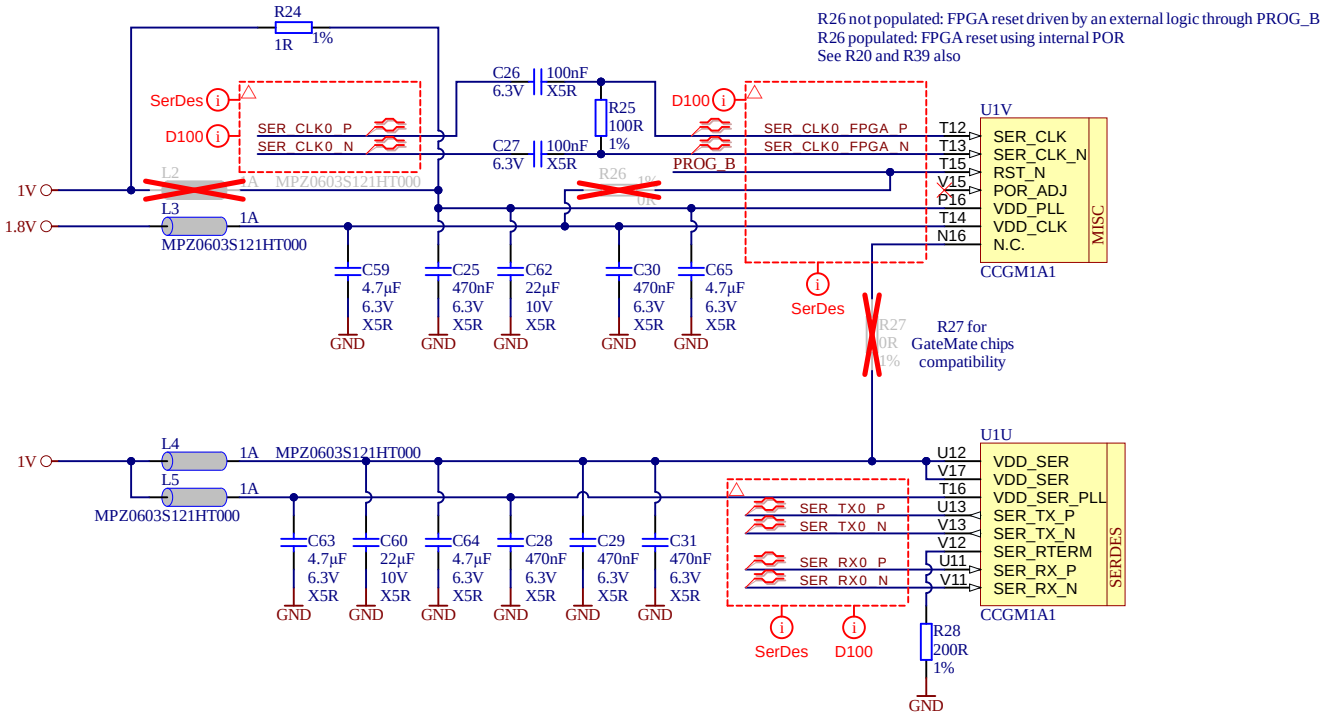
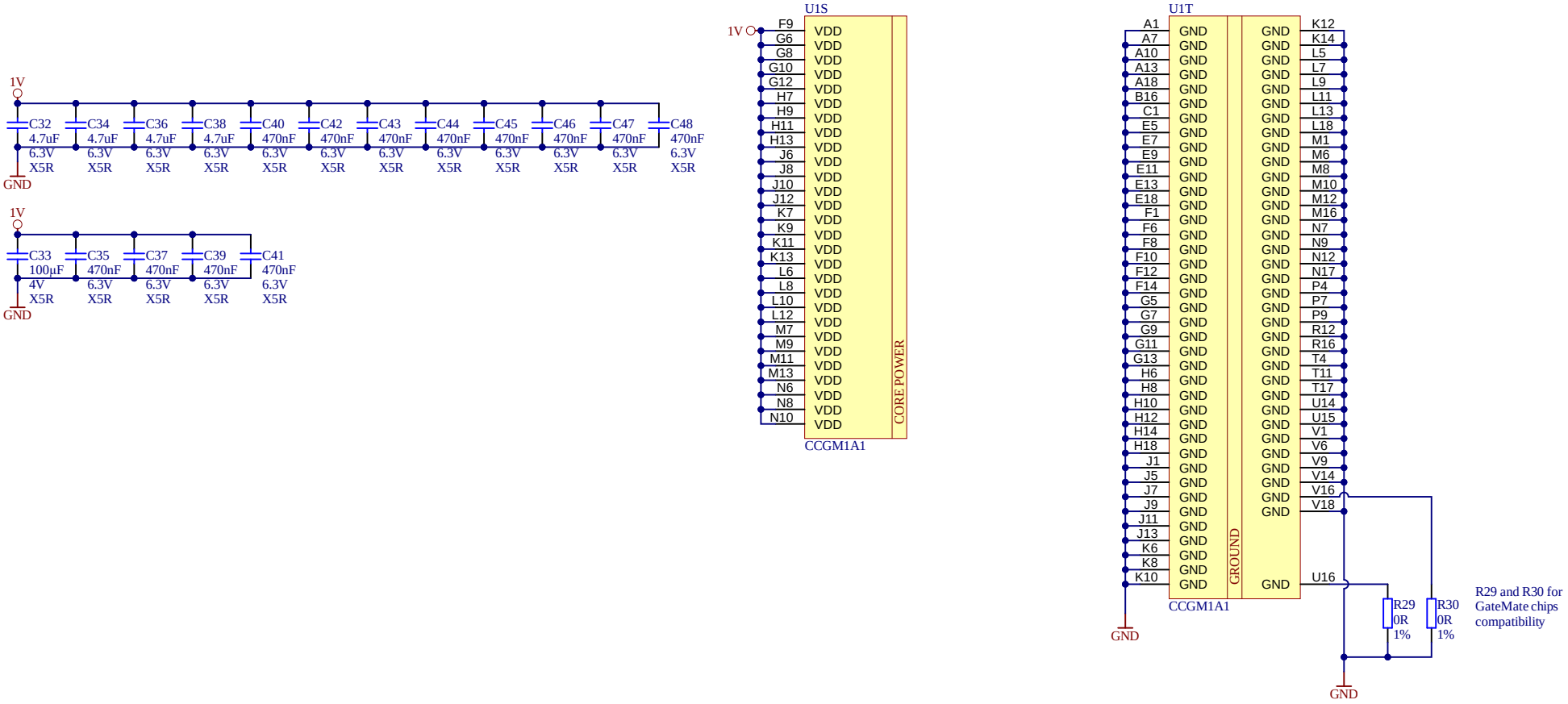
Title: TEG2000 - Configaration		
A4	Number: TEG2000 A1I-1A	Rev. 01
Date: 14-Apr-25	Copyright: Trenz Electronic GmbH	Page 7 of 10
Filename: FPGA-CFG.SchDoc		



trenz electronic	Title: TEG2000 - MGT		
	A4	Number: TEG2000 A1I-1A	Rev. 01
	Date: 14-Apr-25	Copyright: Trenz Electronic GmbH	Page 8 of 10
	Filename: FPGA-MGT.SchDoc		



trenz electronic	Title: TEG2000 - FPGA PWR		
	A4	Number: TEG2000 A1I-1A	Rev. 01
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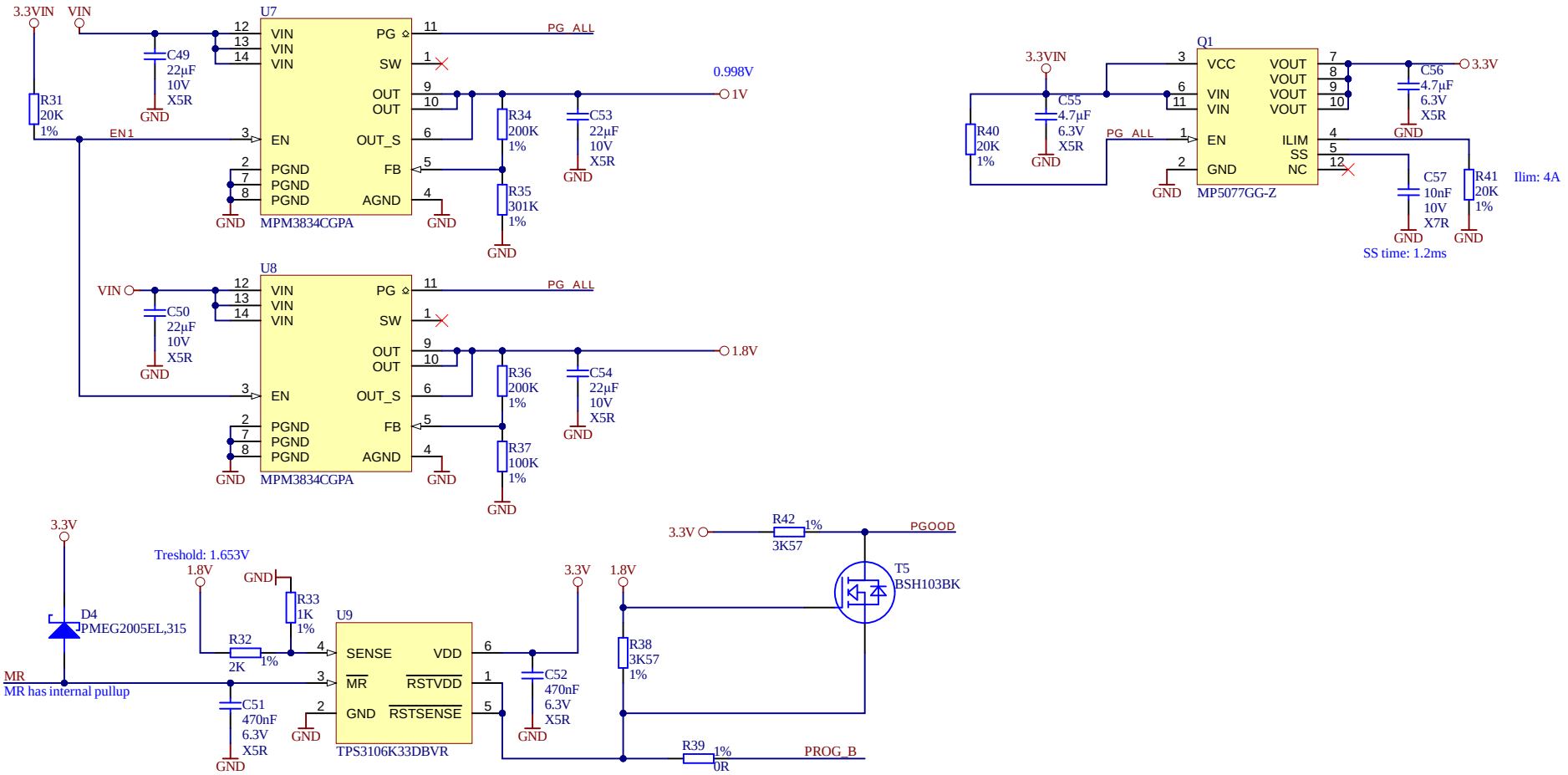

Title: TEG2000 - POWER		
A4	Number: TEG2000 A1I-1A	Rev. 01
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