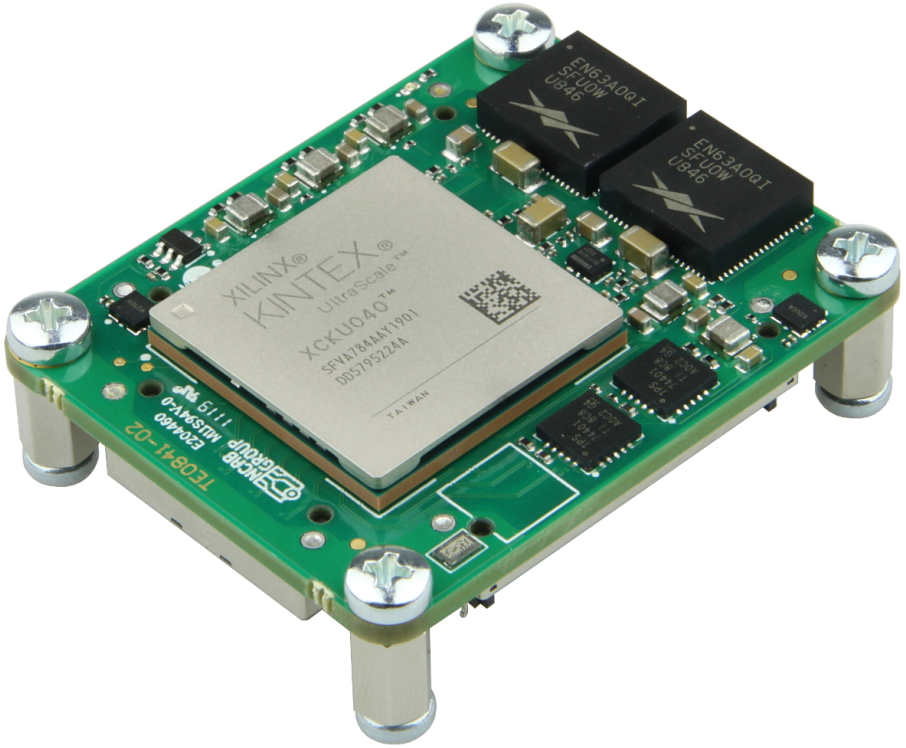
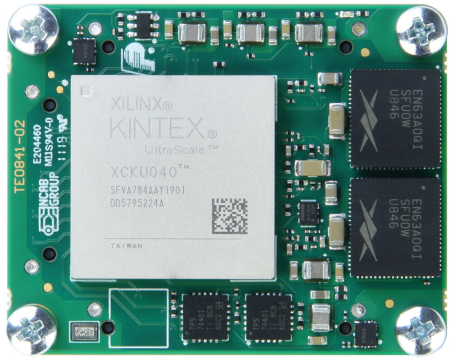
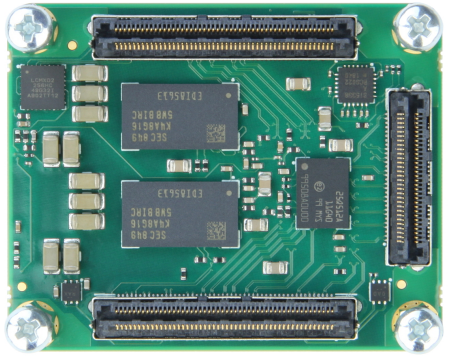






Regarding the usage of our schematics and alike documentation for Trenz module .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0841 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0841 - Legal Notices		
	A4	Number: TE0841 32I31-A	Rev. 03
	Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 1 of 24
	Filename: Legal_Notices.SchDoc		

REV	Description	
-01	Initial revision	
-01A	1) U1: changed schematic symbol. Next pins swapped to match same polarity order: -- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64) -- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66) 2) Net names changed (no electrical changes): JM1: swapped signals B64_L6: -- B64_L6_N - pin 40 (was pin 42) -- B64_L6_P - pin 42 (was pin 40) JM3: swapped signals B64_L6: -- B66_L18_N - pin 52 (was pin 54) -- B66_L18_P - pin 54 (was pin 52)	
-02	1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC) 2) Fixed sense connection on DCDC 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E 4) Full update LIB 5) Added additional resistors for support 16GBit DDR chips 6) Added strong pull-down to EN_PL 7) Added additional testpoints for I2C bus 8) Added additional MEMS oscillator (25MHz) 9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net 10) Added pull-down on the EN_DDR (04.05.2022) 11) S/N Track-it pad set not fitted 12) Change Resistor value R27 (49k9 -> 80k6), rename net "PL_GT_1V05 -> PL_GT_1V2" ----- (23.10.2023)	
-03	1) L1, L2, L3, L4, L5, L6 were changed from BKP0603HS121-T to MPZ0603S121HT000 2) D2 was added 3) Q1 TPS27082LDDCR was changed to MP5077GG-Z 4) U21 STM6710LWB6F was added 5) U7 and U14 were changed from EN63A0QI to LTM4638EY 6) Signal trace lengths were changed. PCB routing was improved 7) Legal Notices and Power diagram pages were added 8) System Overview was added on page TE0841.SchDoc 9) Net names for pins 4 and 5 for U11 were swapped 10) C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C89 were added 11) R79, R80, R81, R82, R83 were added 12) R35 was changed from 4.7k to 2.37k 13) C49 was changed from 4u7 6.3V 0402 to 10u 16V 0603 14) TP3 - TP37 were added 15) R25, R26, R52, R57 were changed from 4k7 to 23k7 16) U11 was changed from DSC1123DL5-200 to SIT9121AI-2B1-XXE-200.00000 17) All SCH symbols and PCB footprints were updated from library 18) R11 was changed from 110k to 124k, net "PL_GT_1V35" was renamed to "PL_GT_1V42" 19) R71 setted as "DNP"	MT

trenz electronic

Title: TE0841 - Changes List		
A4	Number: TE0841 32I31-A	Rev. 03
Date: 27-May-24	Copyright: Trenz Electronic GmbH	Page 2 of 24
Filename: Revision_Changes.SchDoc		

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc

U_PWR3
PWR3.SchDoc

U_PWR-DIAGRAM
Power_Diagram.SchDoc

Mount.Hole 3.2mm
GND

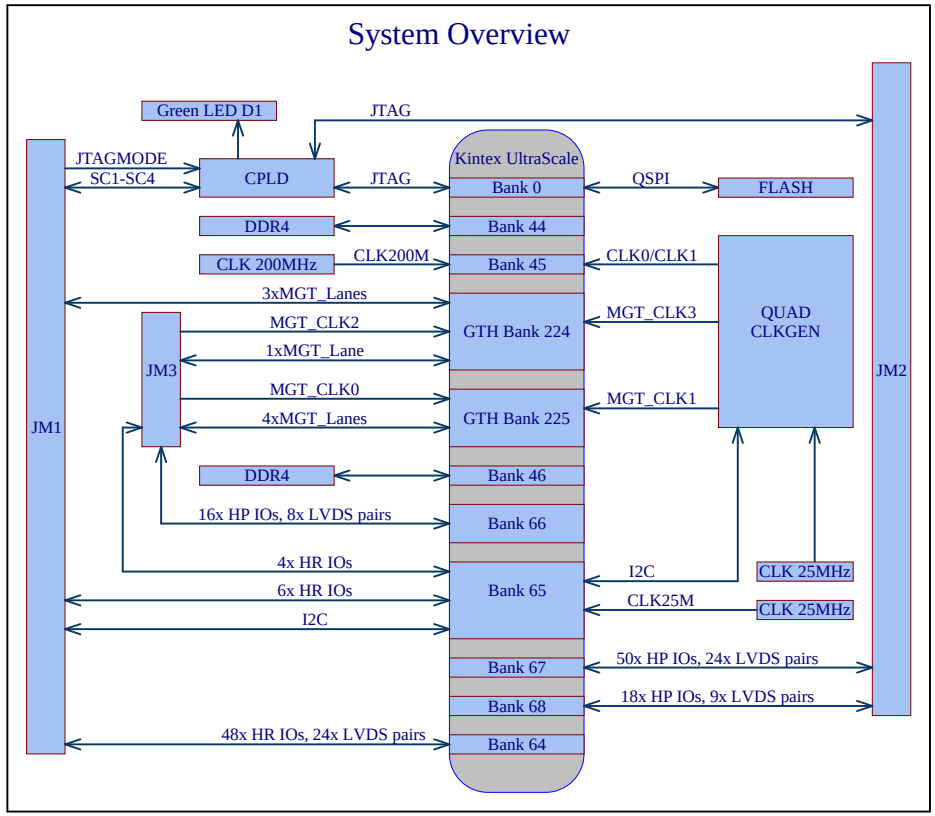
Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

PM1
PM2
PM3
PM4
PM5
PM6

System Overview



UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

Serial

Serial

Serialnumber 6,3 x 6.3mm

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

Special notes:

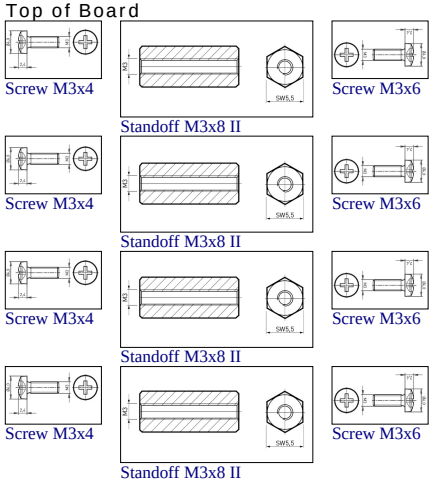
Top side testpoints:

PLL_SCL	TP1	
PLL_SDA	TP2	
	TP3	
3.3VIN	TP4	
PL_1V8	TP5	
B64_VCO	TP6	
B66_VCO	TP7	
B67_VCO	TP8	
B68_VCO	TP9	
VBAT_IN	TP10	
VBATT	TP11	
MGTAUX	TP12	
GND		
PROG_B	TP13	
DONE	TP14	
INIT_B	TP15	
	TP16	
GND		

Bottom side testpoints:

PLL_SCL	TP17	
PLL_SDA	TP18	
PL_GT_1V42	TP19	
PL_GT_1V2	TP20	
DDR_2V5	TP21	
DDR_1V2	TP22	
0.95V	TP23	
MGTAVCC	TP24	
MGTAVTT	TP25	
VBATT	TP26	
MGTAUX	TP27	
AVCC	TP28	
PROG_B	TP29	
DONE	TP30	
INIT_B	TP31	
GND	TP32	
PG_ALL	TP33	
A_DDR4-TEN	TP34	
	TP35	
VREFA	TP36	
VREFA2		
B_DDR4-TEN	TP37	

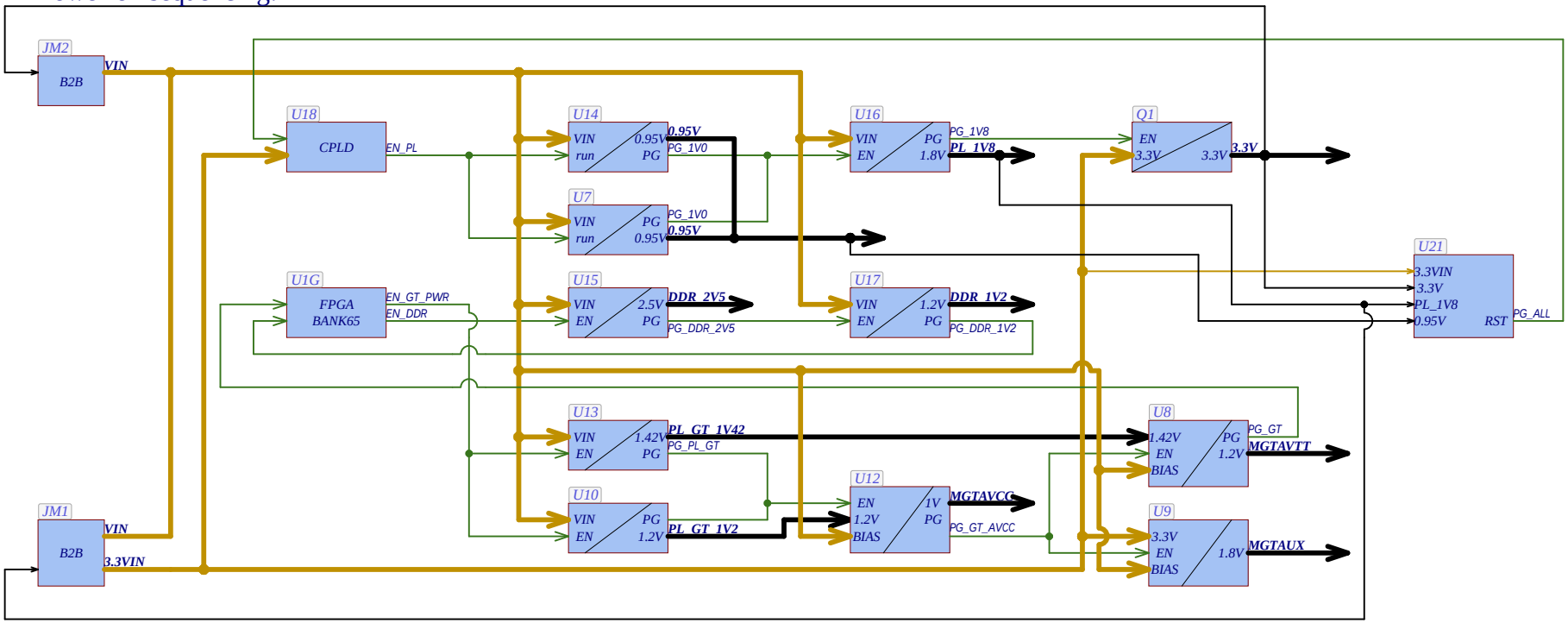
Top of Board



trenz electronic

Title: TE0841			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 28-May-24	Copyright: Trenz Electronic GmbH		Page 3 of 24
Filename: TE0841.SchDoc			

Power-on sequencing:



Current Consumers:

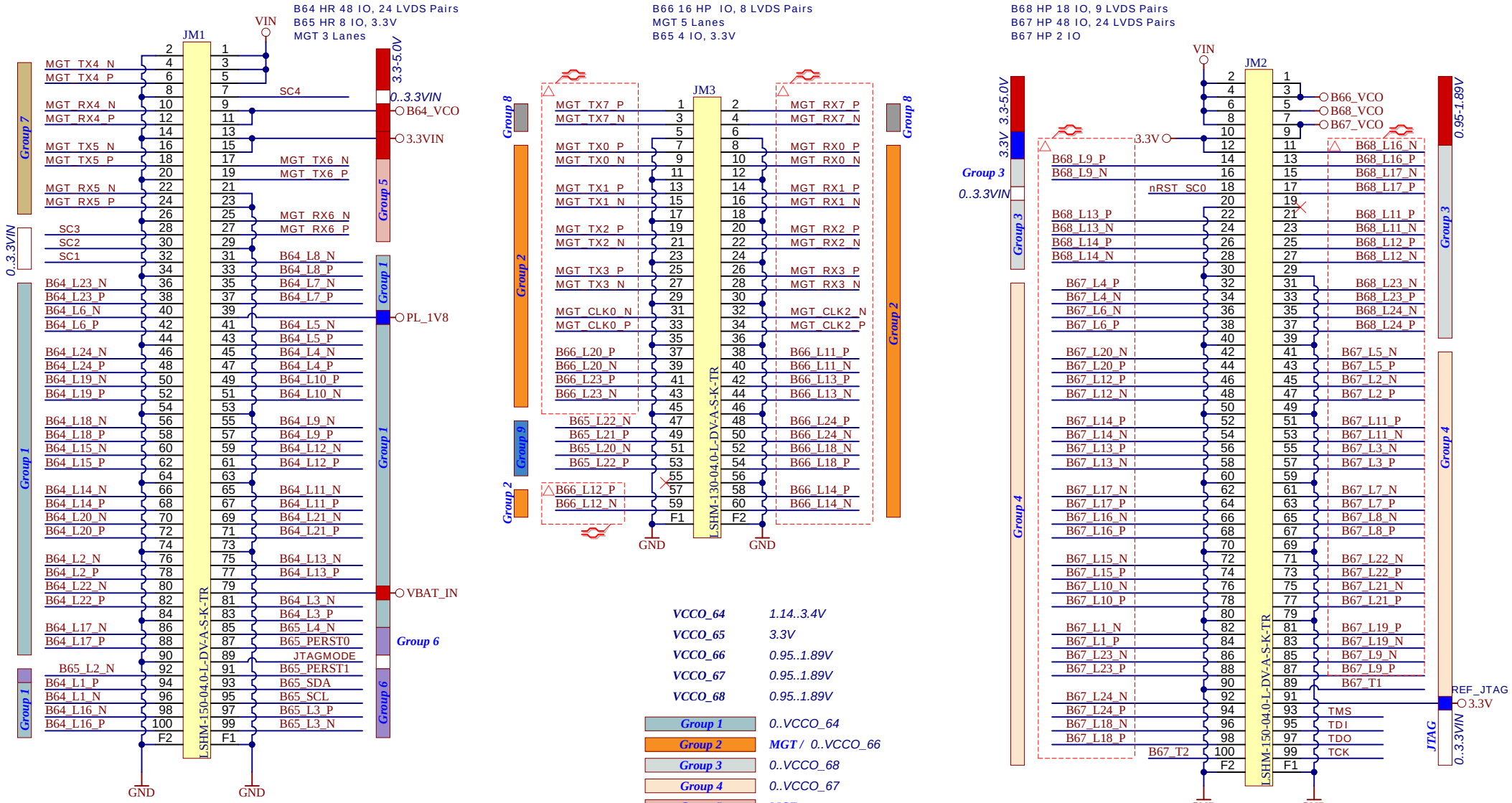
Power Rail	Voltage	Consumer	Note
0.95V	0.95V	FPGA VCCINT FPGA VCCBRAM FPGA VCCINT_IO	-
DDR_2V5	2.5V	DDR4 VPP	-
DDR_1V2	1.2V	FPGA VCCO_44 FPGA VCCO_46 DDR4 VDD	-
PL_1V8	1.8V	FPGA VCCO_0 FPGA VCCO_45 QUAD CLK VDDO CPLD VCCIO2 FPGA VCCAUX FPGA VCCAUX_IO QSPI FLASH VCC FPGA VCC_ADC	-
MGTAVCC	1.0V	FPGA MGTAVCC	-
MGTAVTT	1.2V	FPGA MGTAVTT	-
MGTAUX	1.8V	FPGA MGTAUX	-
3.3V	3.3V	FPGA VCCO_65 QUAD CLK VDD	-

Supported Voltage Ranges:

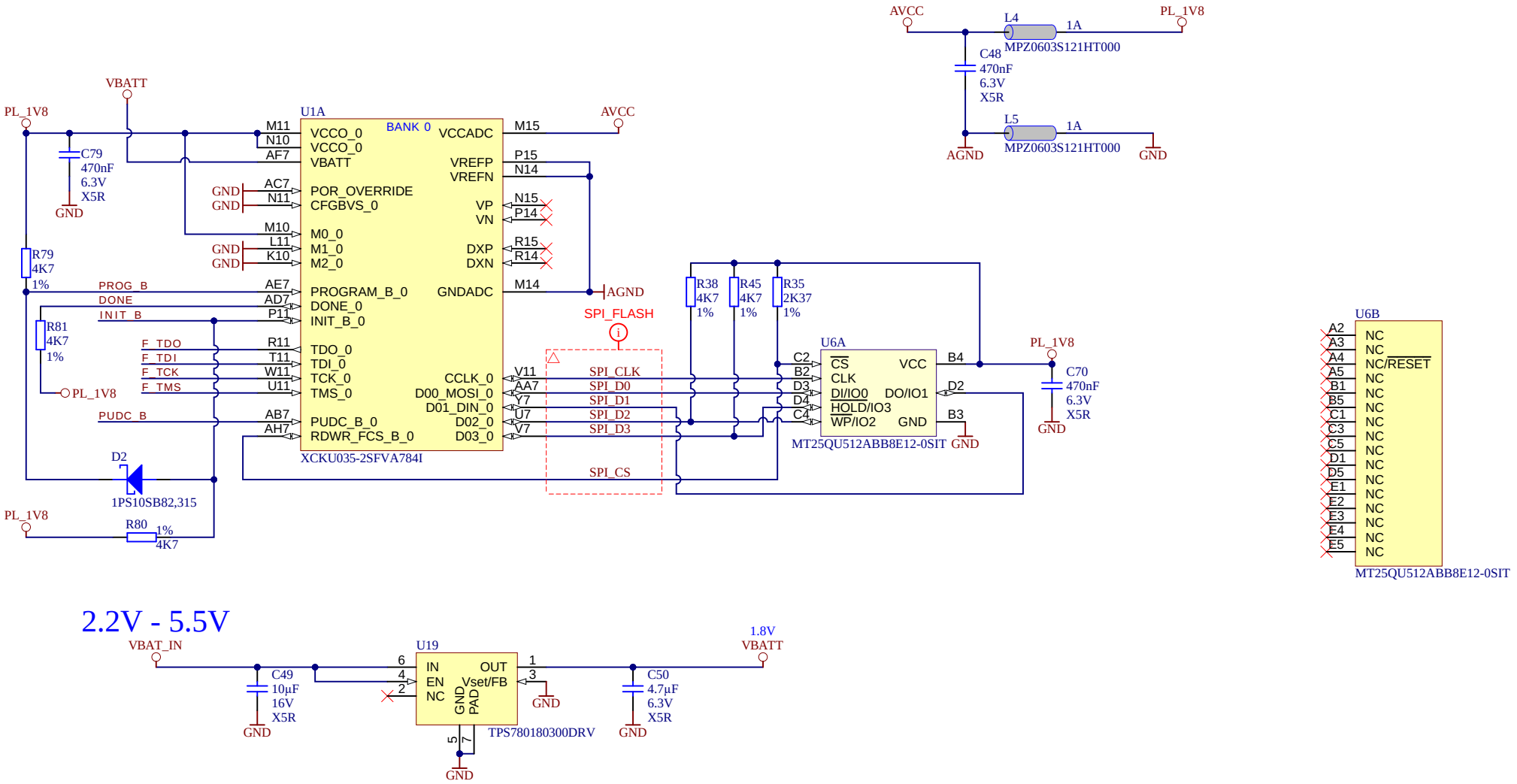
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V-5.0V	+5%/-3%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VBAT_IN	IN	2.2 - 5.5V	-	Fpga Vbatt	-
B64_VCCO	IN	1.14 - 3.4V	-	IO Bank64	-
B66_VCCO	IN	0.95 - 1.89V	-	IO Bank66	-
B67_VCCO	IN	0.95 - 1.89V	-	IO Bank67	-
B68_VCCO	IN	0.95 - 1.89V	-	IO Bank68	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-
PL_1V8	OUT	1.8V	+/-3%	Power for Carrier	-

trenz electronic

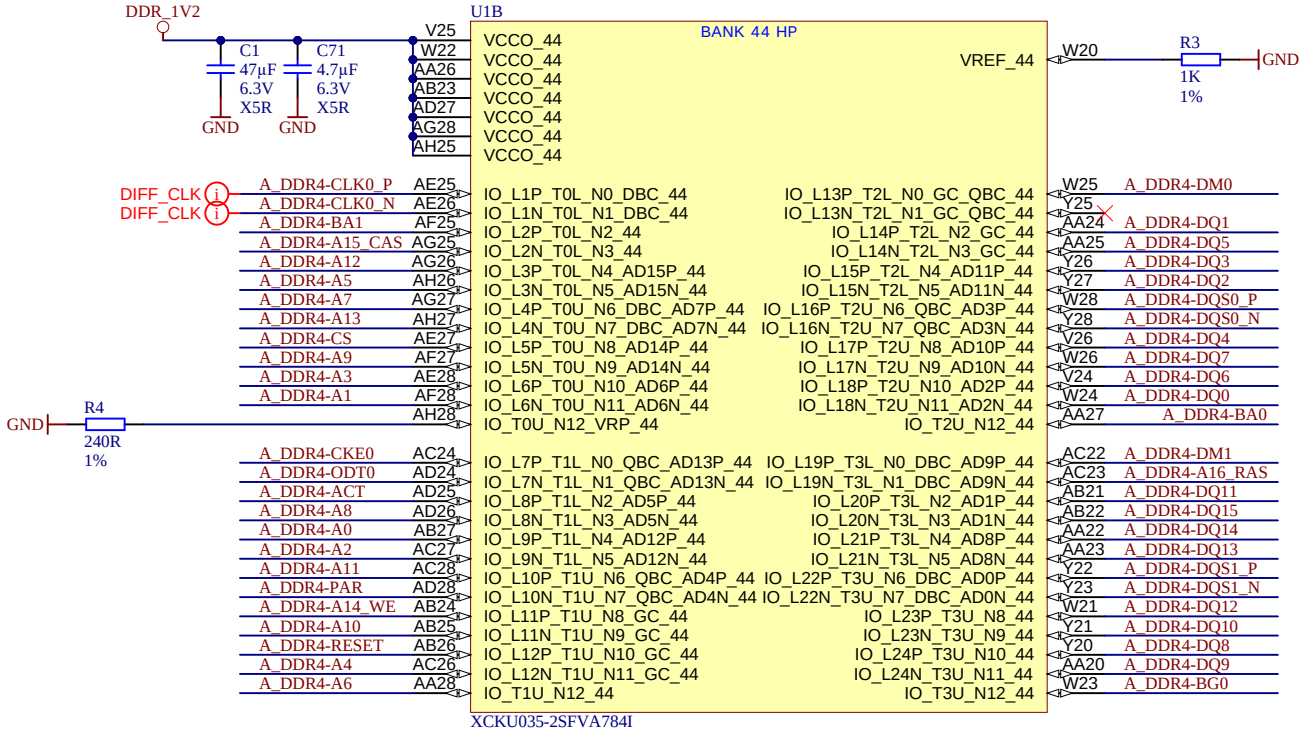
Title: TE0841 - Power Diagram		
A4	Number: TE0841 32I31-A	Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH	Page 4 of 24
Filename: Power_Diagram.SchDoc		



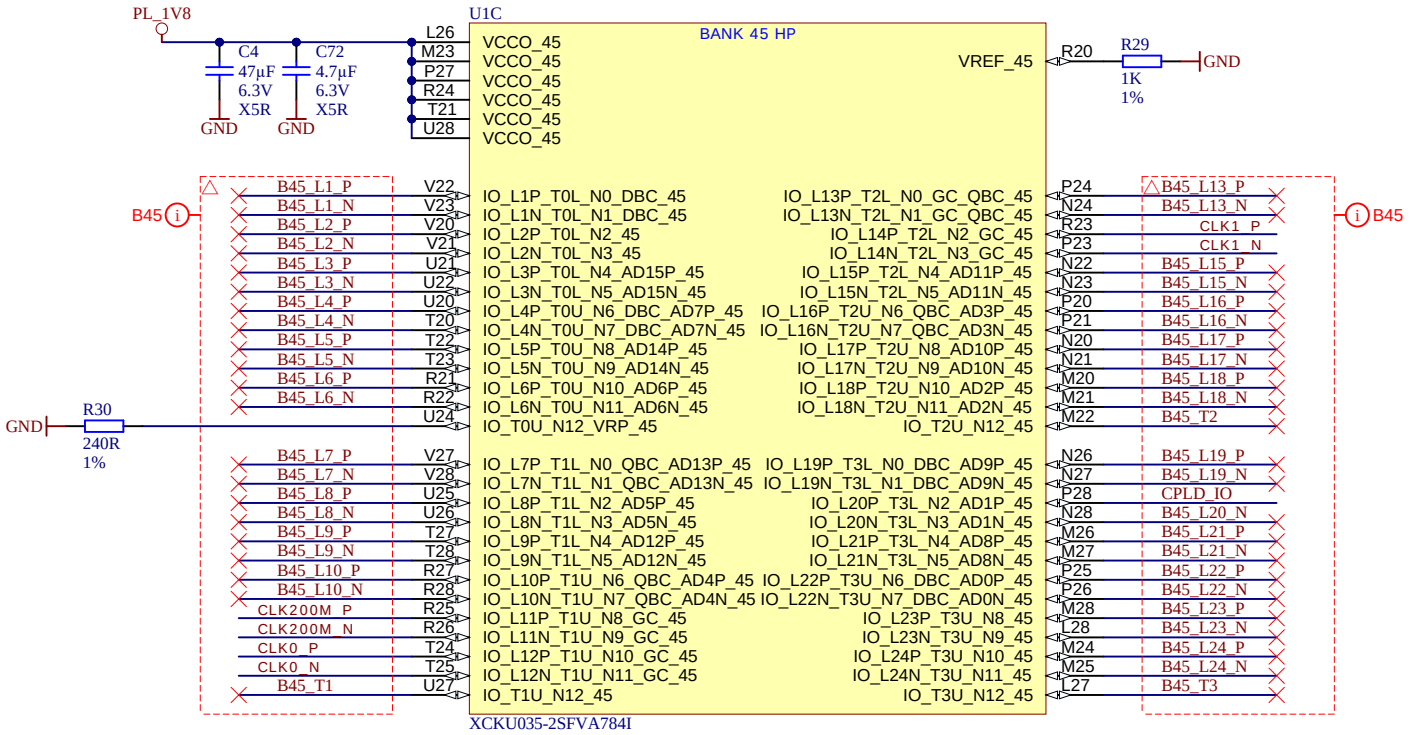
Title: TE0841 - B2B Connectors			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH		Page 5 of 24
Filename: B2B-Connectors.SchDoc			



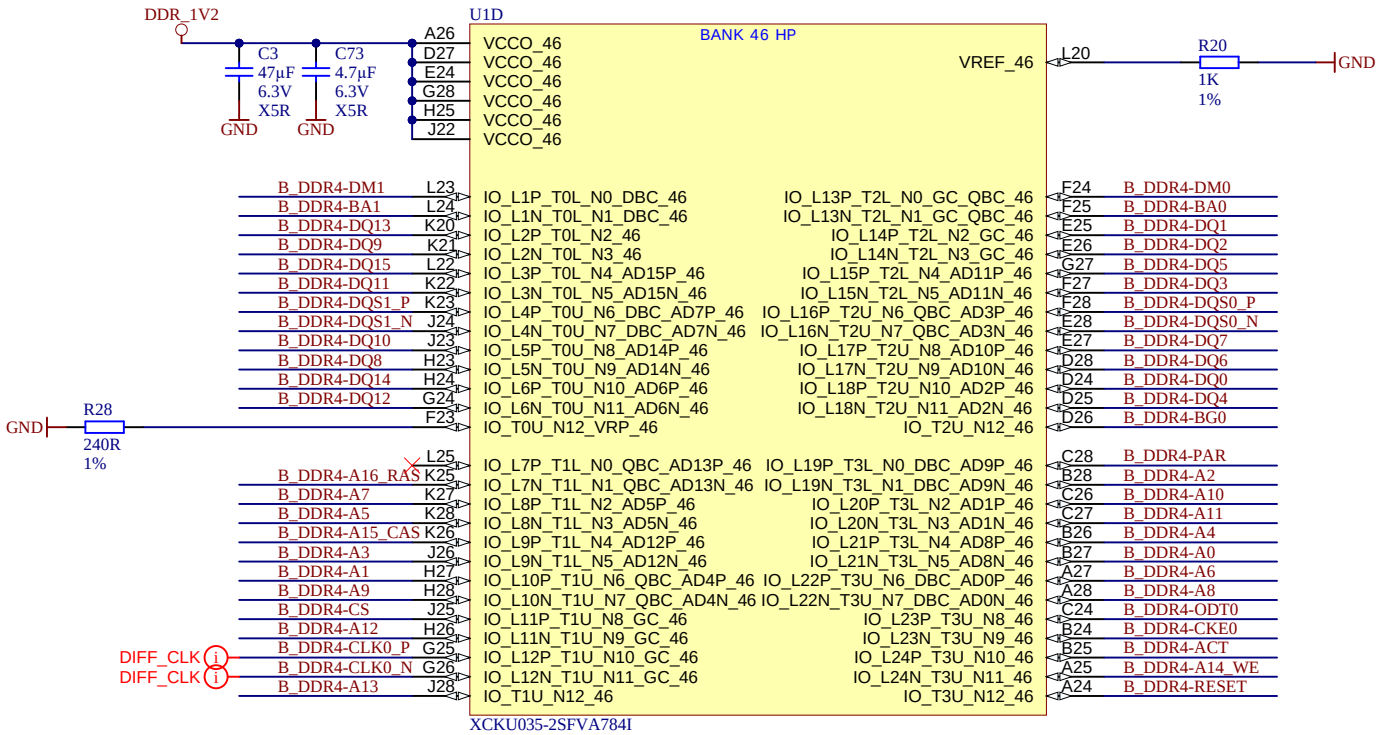
trenz electronic	Title: TE0841 - MISC		
	A4	Number: TE0841 32I31-A	Rev. 03
	Date: 22-May-24	Copyright: Trenz Electronic GmbH	Page 6 of 24
	Filename: FPGA-MISC.SchDoc		



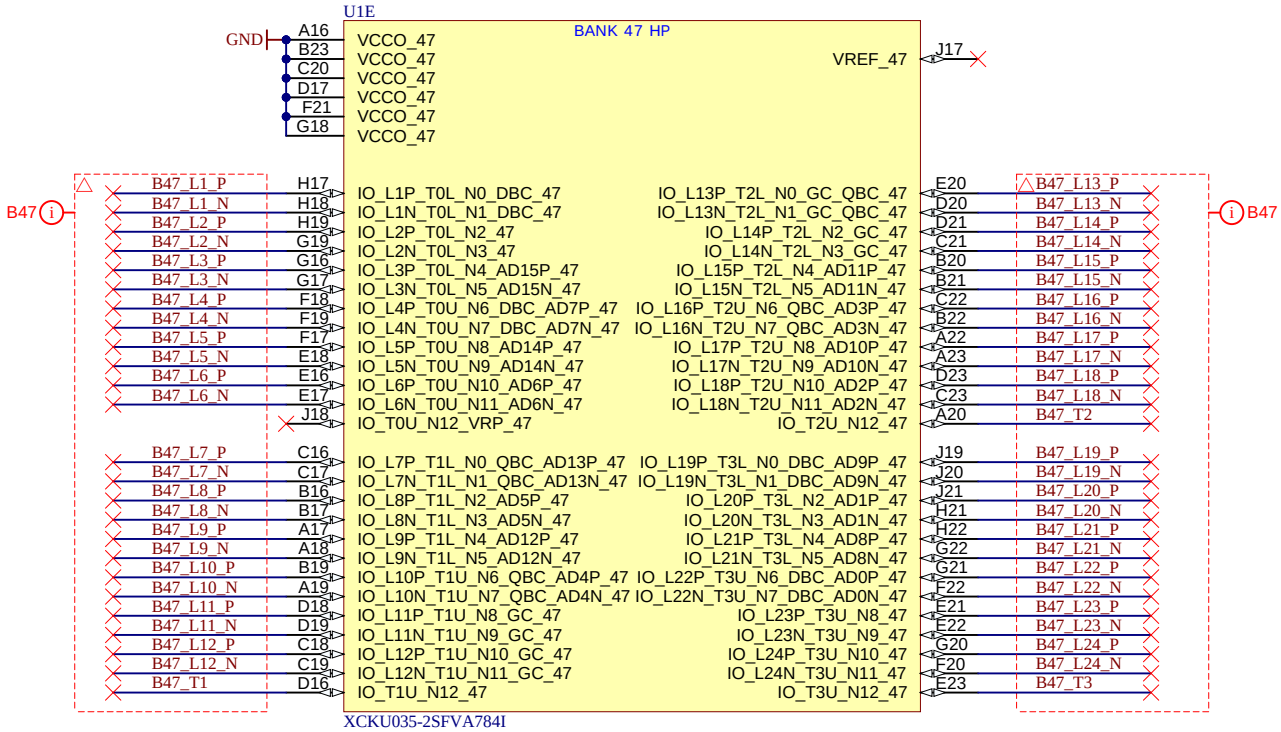
trenz electronic	Title: TE0841 - BANK44		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 27-May-24	Copyright: Trenz Electronic GmbH		Page 7 of 24
Filename: FPGA-B44.SchDoc			



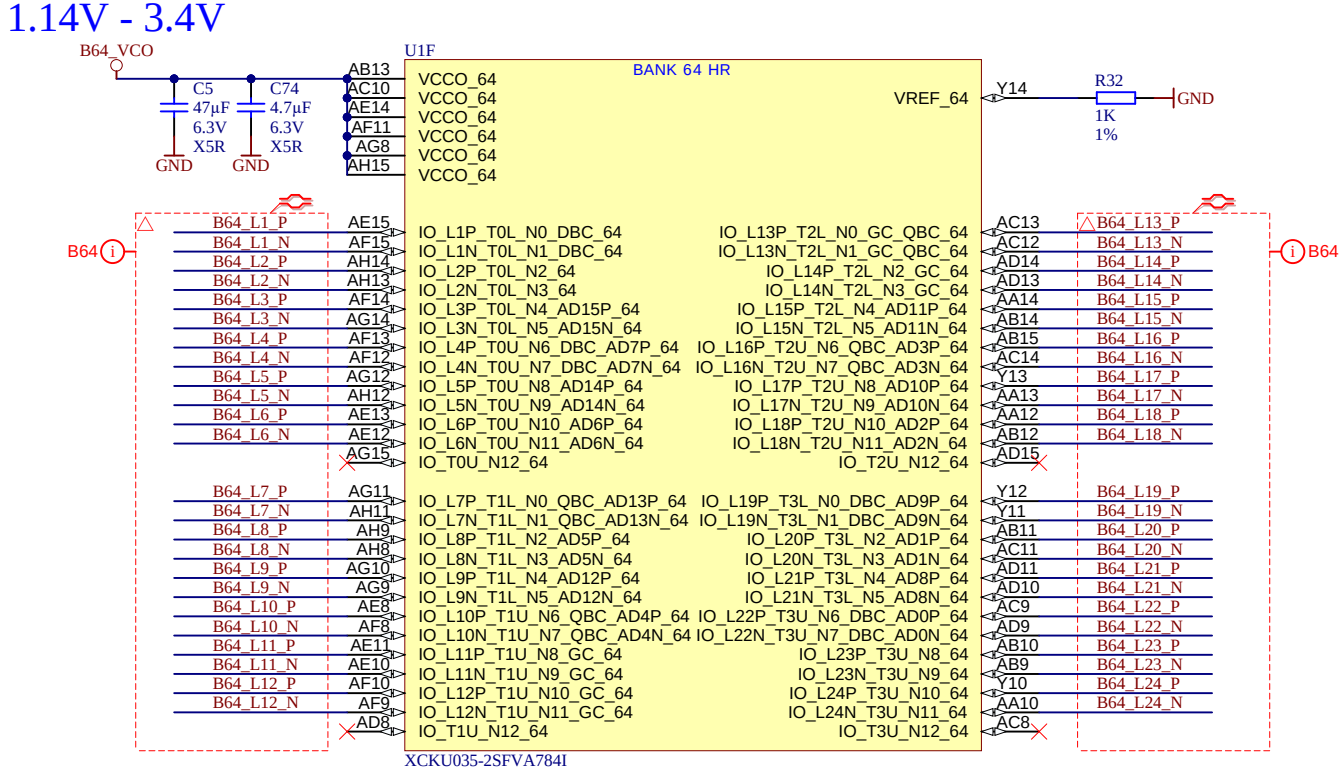
trenz electronic	Title: TE0841 - BANK45		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 8 of 24
Filename: FPGA-B45.SchDoc			



trenz electronic	Title: TE0841 - BANK46		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 27-May-24	Copyright: Trenz Electronic GmbH		Page 9 of 24
Filename: FPGA-B46.SchDoc			

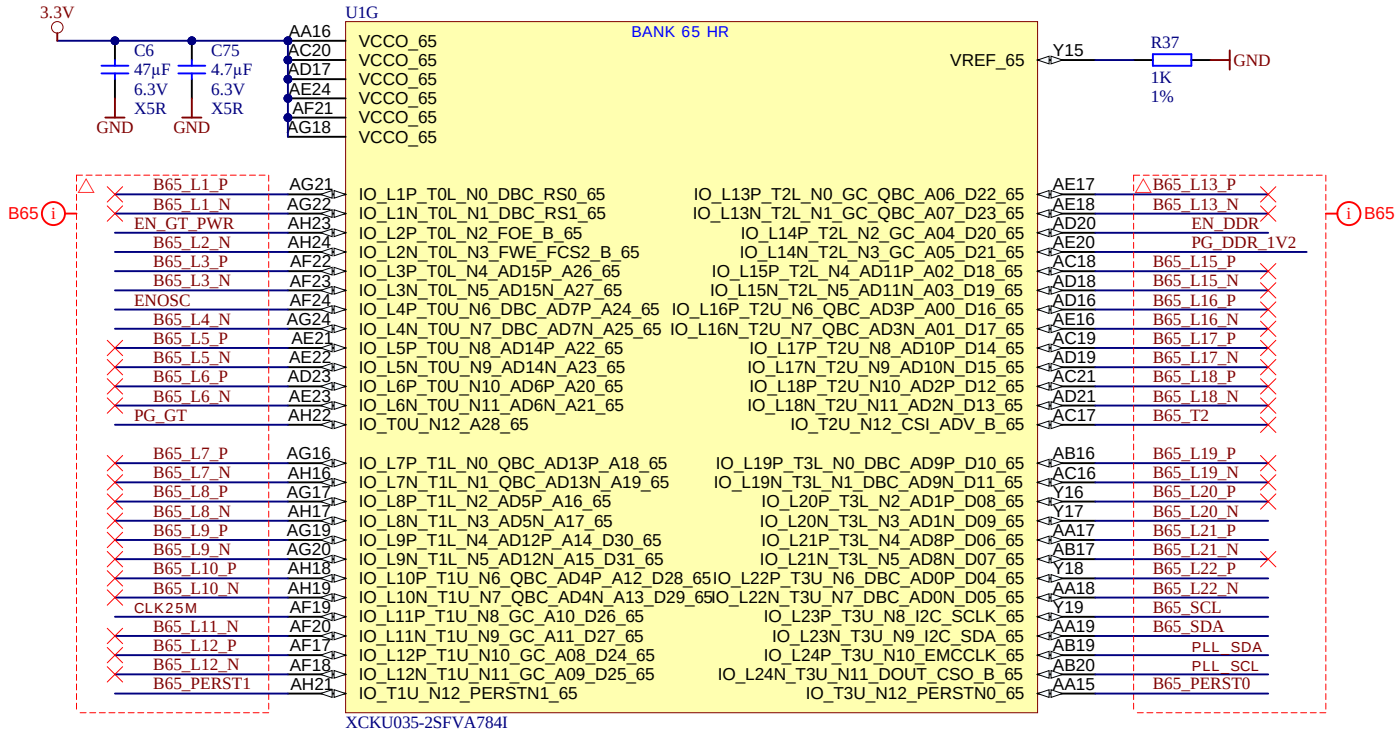


trenz electronic	Title: TE0841 - BANK47	
A4	Number: TE0841 32I31-A	Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 10 of 24
	Filename: FPGA-B47.SchDoc	

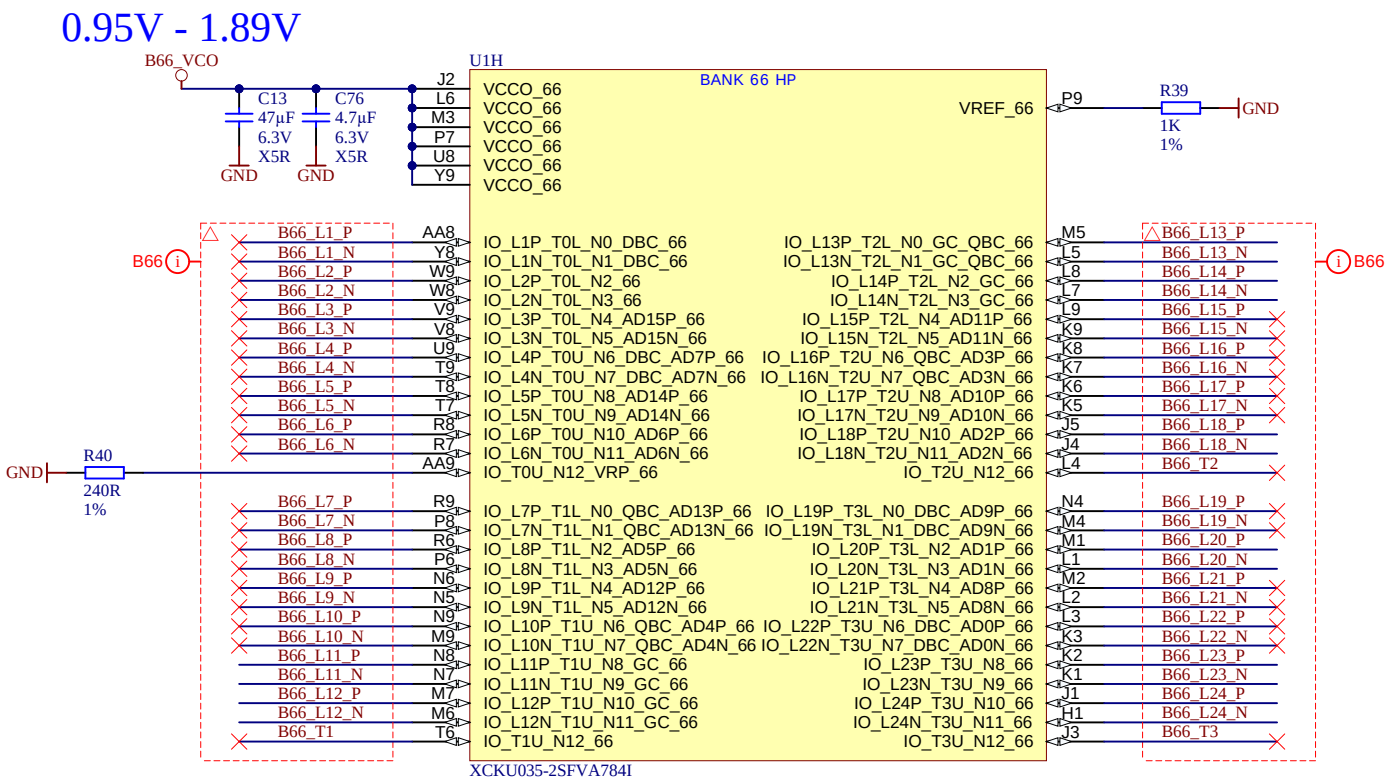


B64_L1_P	AE15	IO_L1P_T0L_N0_DBC_64	IO_L13P_T2L_N0_GC_QBC_64	AC13	B64_L13_P
B64_L1_N	AF15	IO_L1N_T0L_N1_DBC_64	IO_L13N_T2L_N1_GC_QBC_64	AC12	B64_L13_N
B64_L2_P	AH14	IO_L2P_T0L_N2_64	IO_L14P_T2L_N2_GC_64	AD14	B64_L14_P
B64_L2_N	AH13	IO_L2N_T0L_N3_64	IO_L14N_T2L_N3_GC_64	AD13	B64_L14_N
B64_L3_P	AF14	IO_L3P_T0L_N4_AD15P_64	IO_L15P_T2L_N4_AD11P_64	AA14	B64_L15_P
B64_L3_N	AG14	IO_L3N_T0L_N5_AD15N_64	IO_L15N_T2L_N5_AD11N_64	AB14	B64_L15_N
B64_L4_P	AF13	IO_L4P_T0U_N6_DBC_AD7P_64	IO_L16P_T2U_N6_QBC_AD3P_64	AB15	B64_L16_P
B64_L4_N	AF12	IO_L4N_T0U_N7_DBC_AD7N_64	IO_L16N_T2U_N7_QBC_AD3N_64	AC14	B64_L16_N
B64_L5_P	AG12	IO_L5P_T0U_N8_AD14P_64	IO_L17P_T2U_N8_AD10P_64	Y13	B64_L17_P
B64_L5_N	AH12	IO_L5N_T0U_N9_AD14N_64	IO_L17N_T2U_N9_AD10N_64	AA13	B64_L17_N
B64_L6_P	AE13	IO_L6P_T0U_N10_AD6P_64	IO_L18P_T2U_N10_AD2P_64	AA12	B64_L18_P
B64_L6_N	AE12	IO_L6N_T0U_N11_AD6N_64	IO_L18N_T2U_N11_AD2N_64	AB12	B64_L18_N
	AG15	IO_T0U_N12_64	IO_T2U_N12_64	AD15	
B64_L7_P	AG11	IO_L7P_T1L_N0_QBC_AD13P_64	IO_L19P_T3L_N0_DBC_AD9P_64	Y12	B64_L19_P
B64_L7_N	AH11	IO_L7N_T1L_N1_QBC_AD13N_64	IO_L19N_T3L_N1_DBC_AD9N_64	Y11	B64_L19_N
B64_L8_P	AH9	IO_L8P_T1L_N2_AD5P_64	IO_L20P_T3L_N2_AD1P_64	AB11	B64_L20_P
B64_L8_N	AH8	IO_L8N_T1L_N3_AD5N_64	IO_L20N_T3L_N3_AD1N_64	AC11	B64_L20_N
B64_L9_P	AG10	IO_L9P_T1L_N4_AD12P_64	IO_L21P_T3L_N4_AD8P_64	AD11	B64_L21_P
B64_L9_N	AG9	IO_L9N_T1L_N5_AD12N_64	IO_L21N_T3L_N5_AD8N_64	AD10	B64_L21_N
B64_L10_P	AE8	IO_L10P_T1U_N6_QBC_AD4P_64	IO_L22P_T3U_N6_DBC_AD0P_64	AC9	B64_L22_P
B64_L10_N	AF8	IO_L10N_T1U_N7_QBC_AD4N_64	IO_L22N_T3U_N7_DBC_AD0N_64	AD9	B64_L22_N
B64_L11_P	AE11	IO_L11P_T1U_N8_GC_64	IO_L23P_T3U_N8_64	AB10	B64_L23_P
B64_L11_N	AE10	IO_L11N_T1U_N9_GC_64	IO_L23N_T3U_N9_64	AB9	B64_L23_N
B64_L12_P	AF10	IO_L12P_T1U_N10_GC_64	IO_L24P_T3U_N10_64	Y10	B64_L24_P
B64_L12_N	AF9	IO_L12N_T1U_N11_GC_64	IO_L24N_T3U_N11_64	AA10	B64_L24_N
	AD8	IO_T1U_N12_64	IO_T3U_N12_64	AC8	

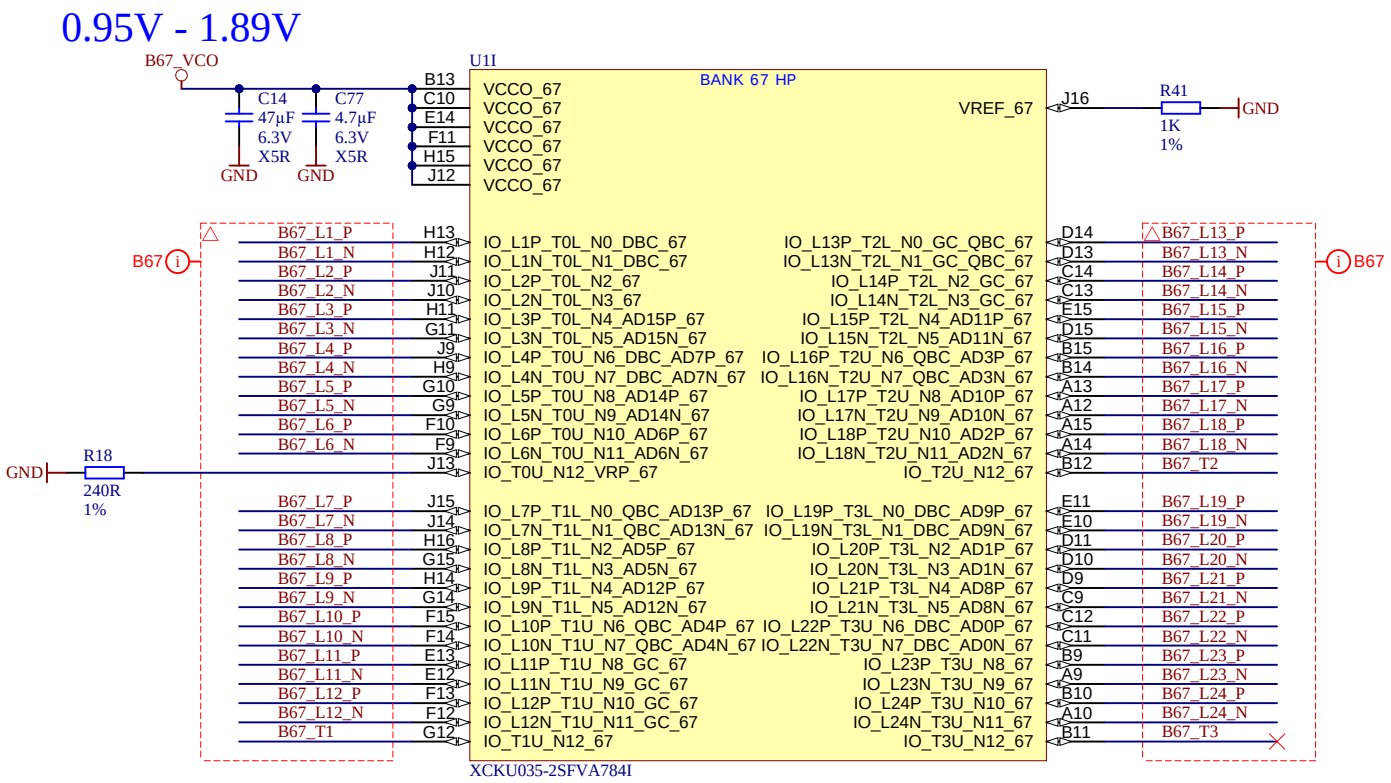
Title: TE0841 - BANK64			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 11 of 24
Filename: FPGA-B64.SchDoc			



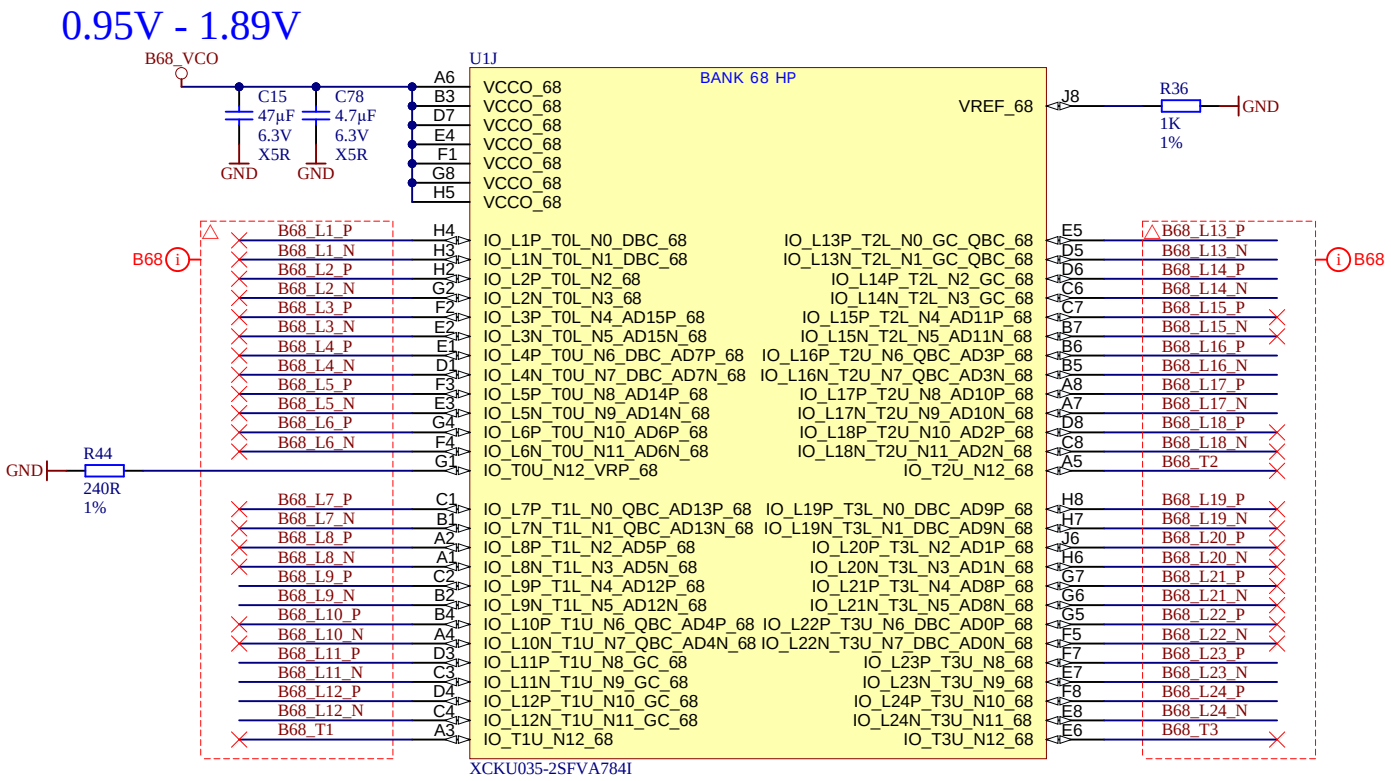
trenz electronic	Title: TE0841 - BANK65		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH		Page 12 of 24
Filename: FPGA-B65.SchDoc			



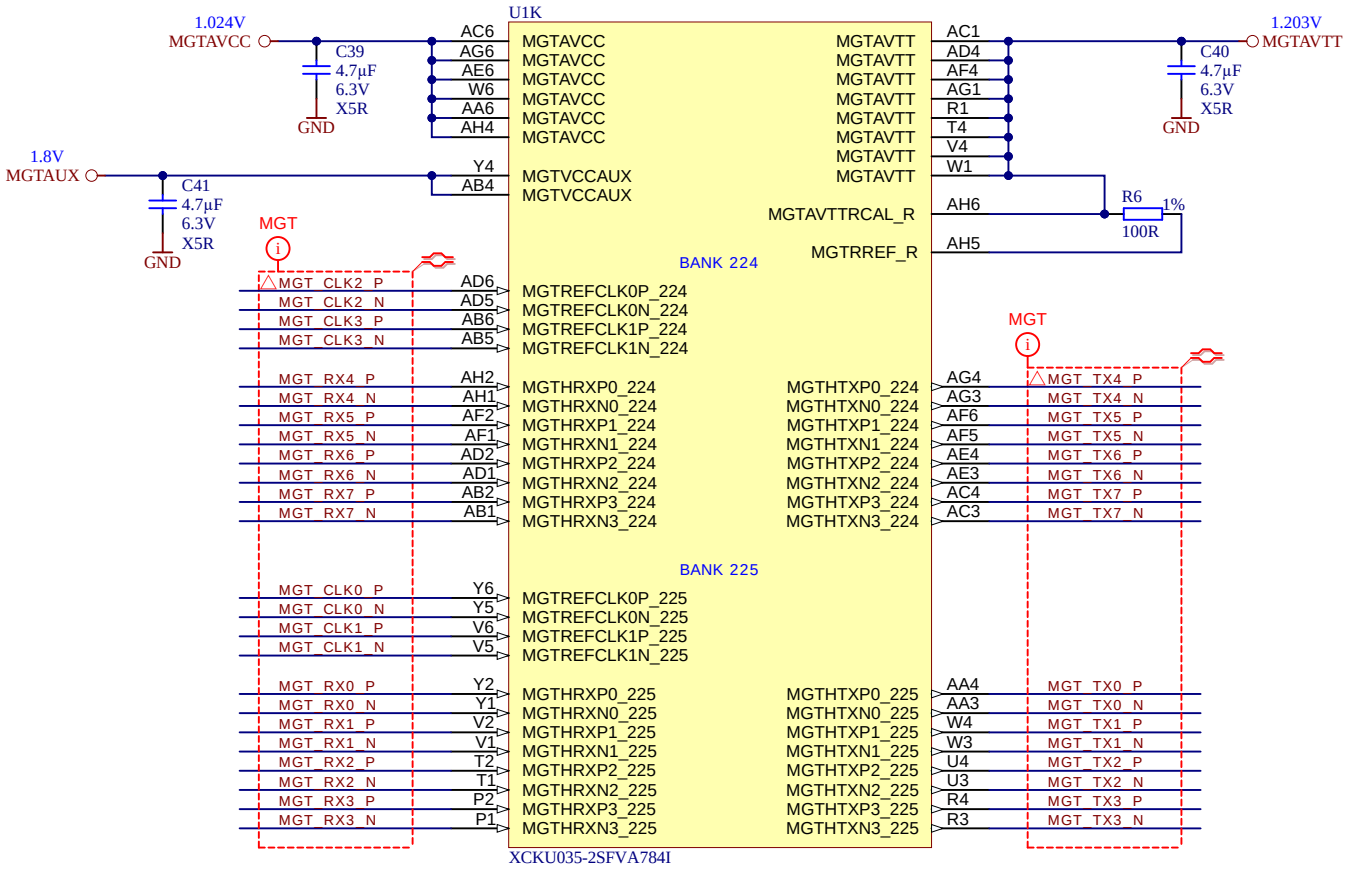
Title: TE0841 - BANK66		
A4	Number: TE0841 32I31-A	Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 13 of 24
Filename: FPGA-B66.SchDoc		



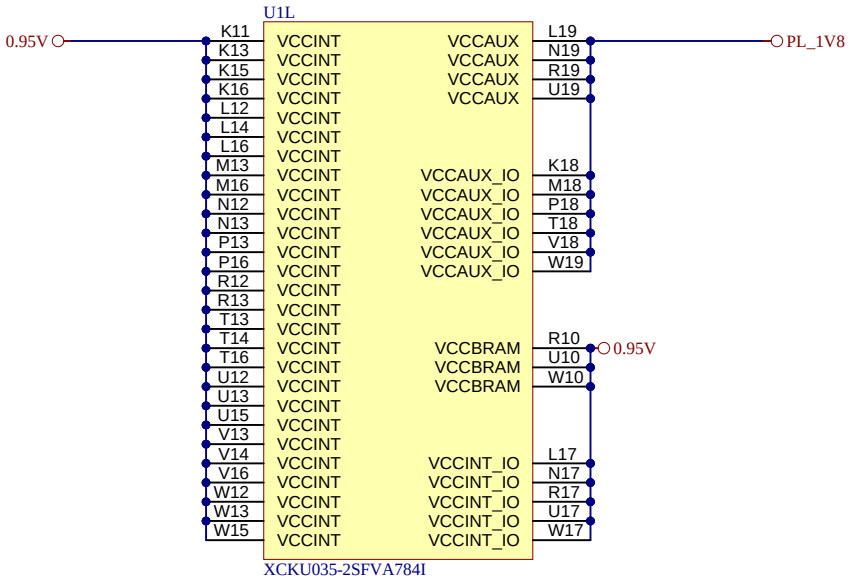
Title: TE0841 - BANK67		
A4	Number: TE0841 32I31-A	Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 14 of 24
Filename: FPGA-B67.SchDoc		

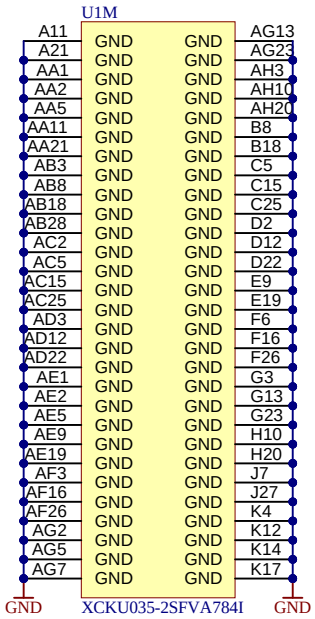


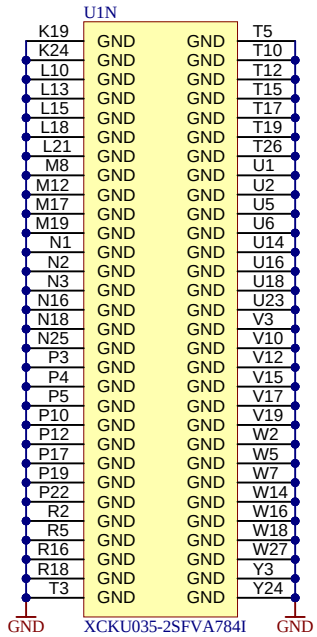
Title: TE0841 - BANK68			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 15 of 24
Filename: FPGA-B68.SchDoc			

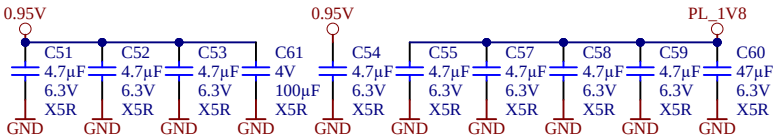


trenz electronic	Title: TE0841 - MGT		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 16 of 24
Filename: FPGA-MGT.SchDoc			



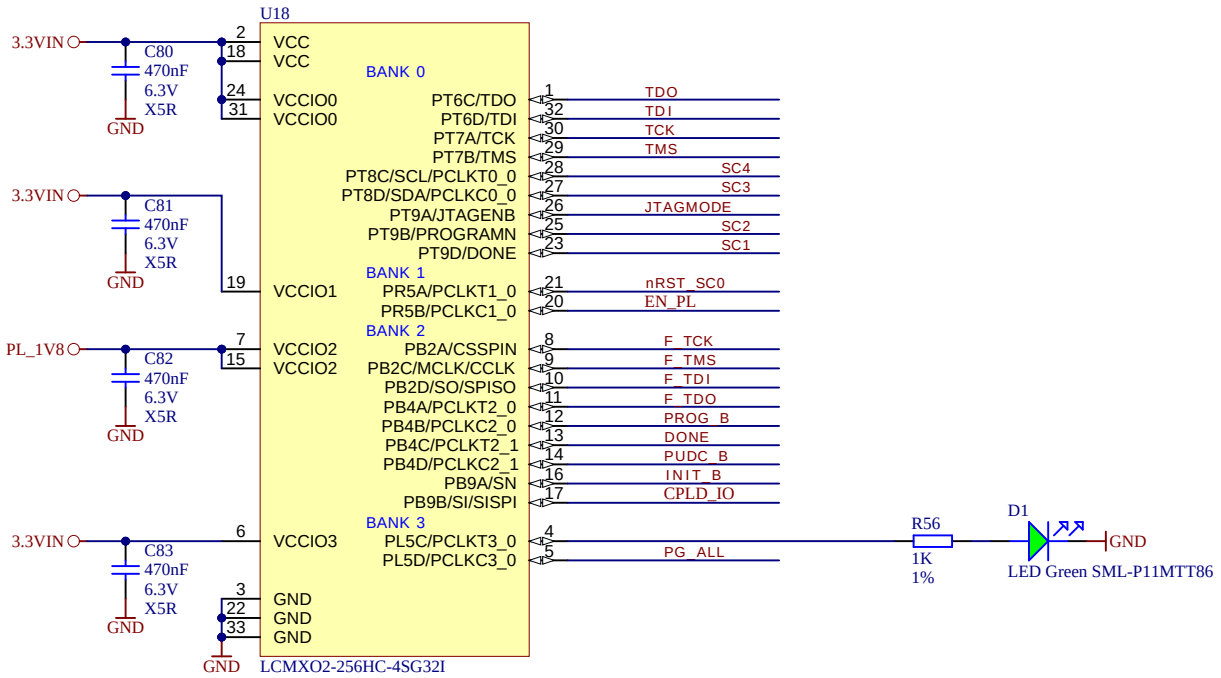




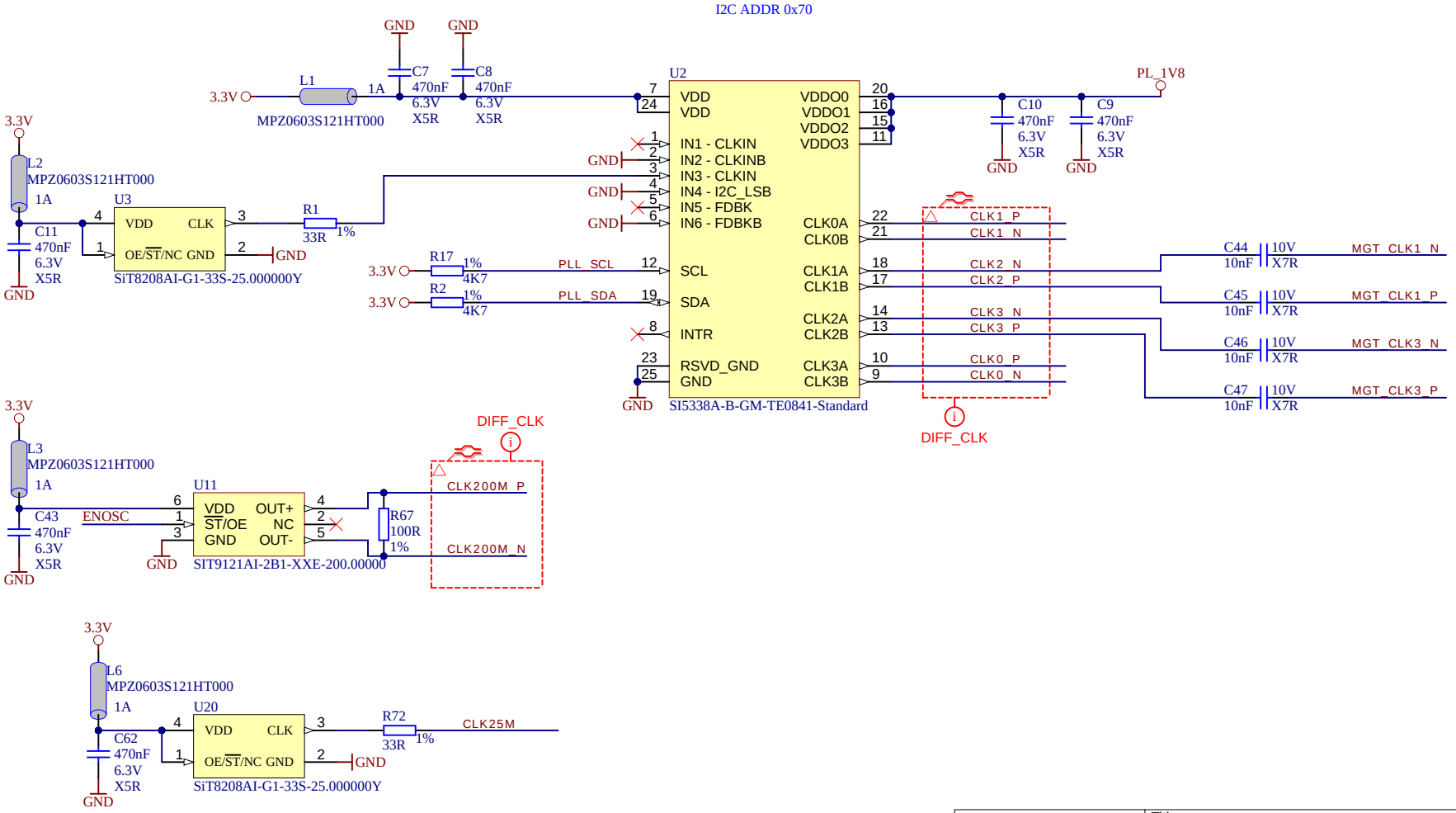


trenz electronic

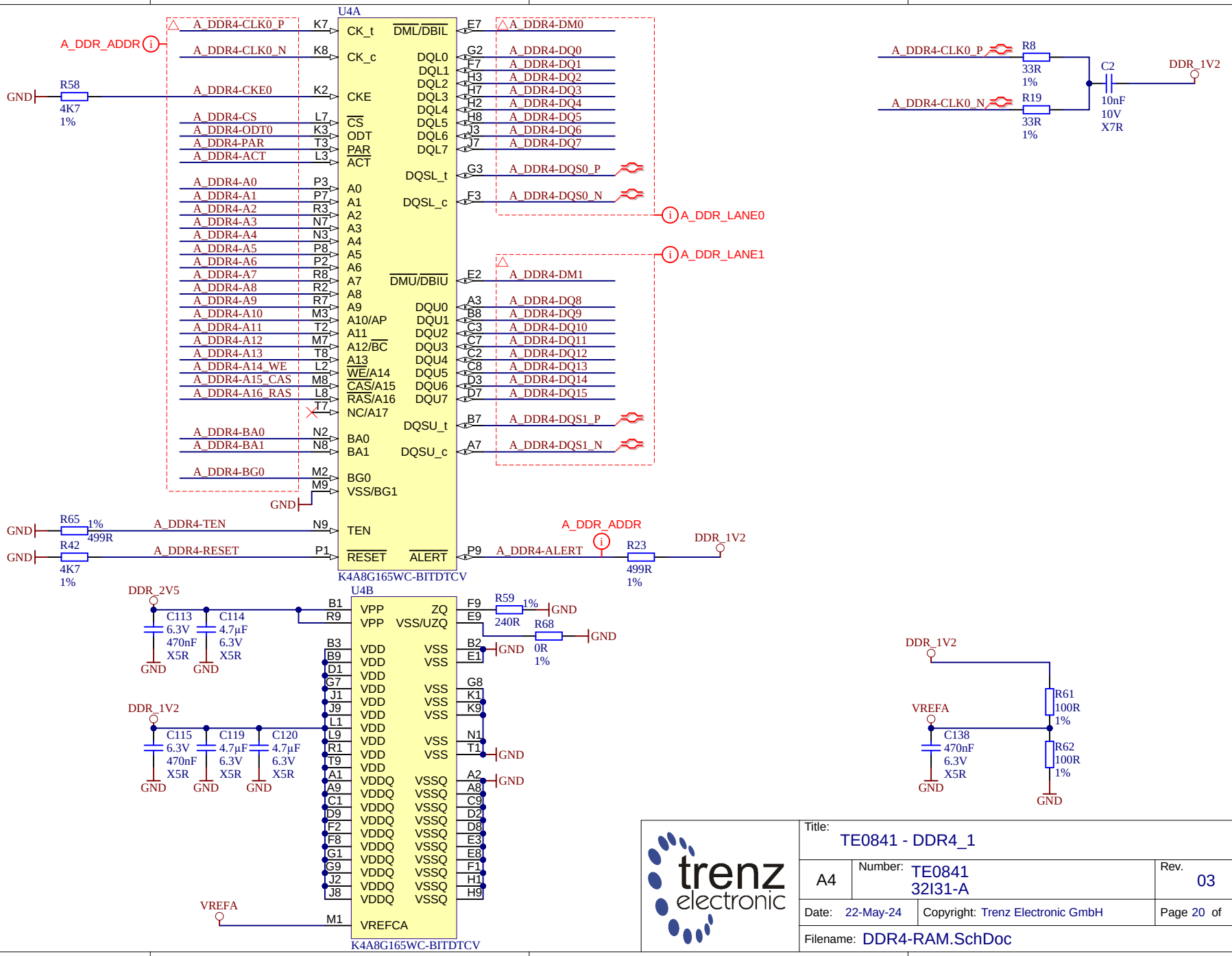
Title: TE0841 - FPGA POWER		
A4	Number: TE0841 32I31-A	Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 17 of 24
Filename: FPGA-PWR.SchDoc		

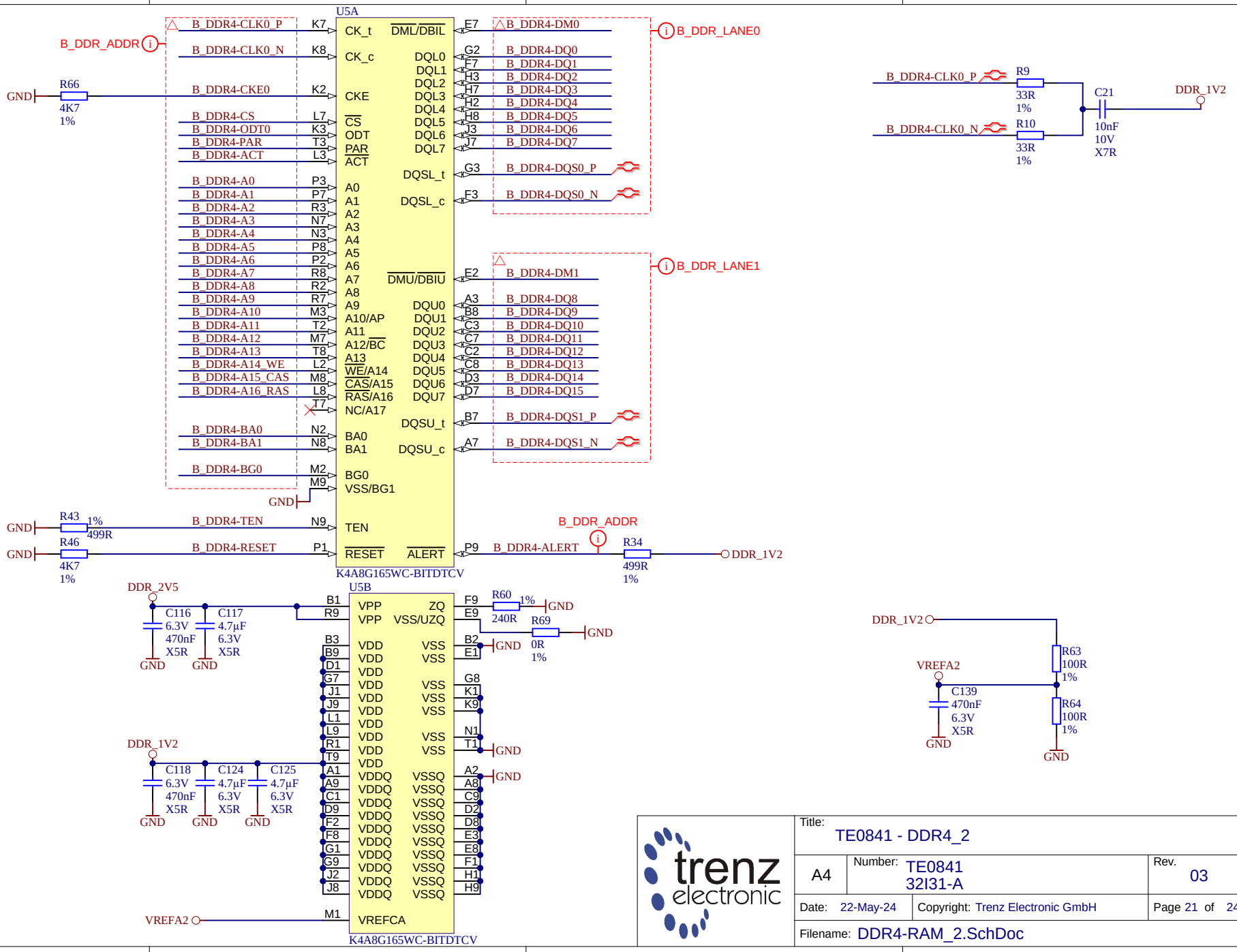


trenz electronic	Title: TE0841 - CPLD		
A4	Number: TE0841 32I31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 18 of 24
Filename: CPLD.SchDoc			



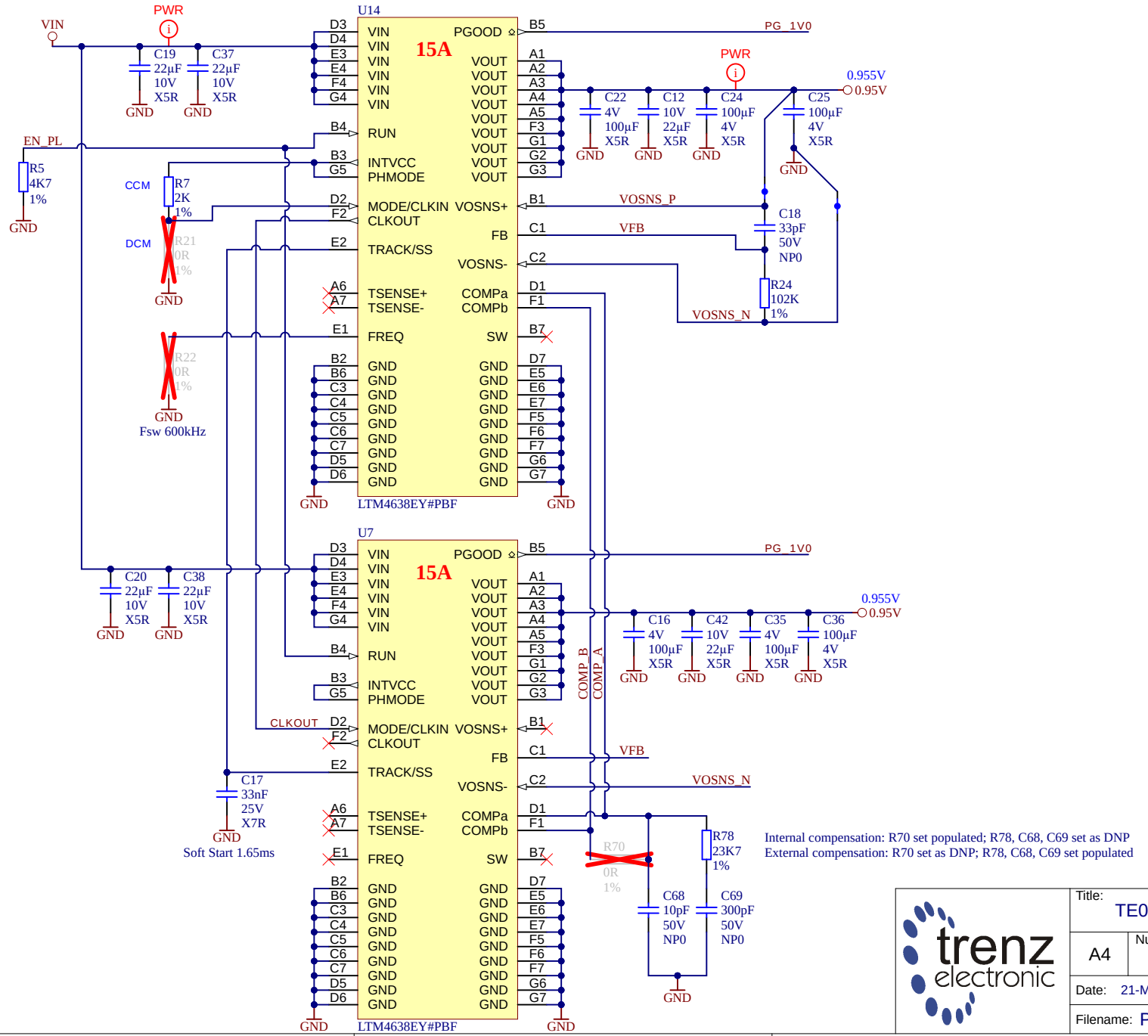
Title: TE0841 - CLOCK			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 23-May-24	Copyright: Trenz Electronic GmbH		Page 19 of 24
Filename: Clock.SchDoc			


U4A
A_DDR_ADDR
A_DDR4-CLK0_P
A_DDR4-CLK0_N
A_DDR4-CKE0
A_DDR4-CS
A_DDR4-ODT0
A_DDR4-PAR
A_DDR4-ACT
A_DDR4-A0
A_DDR4-A1
A_DDR4-A2
A_DDR4-A3
A_DDR4-A4
A_DDR4-A5
A_DDR4-A6
A_DDR4-A7
A_DDR4-A8
A_DDR4-A9
A_DDR4-A10
A_DDR4-A11
A_DDR4-A12
A_DDR4-A13
A_DDR4-A14_WE
A_DDR4-A15_CAS
A_DDR4-A16_RAS
A_DDR4-BA0
A_DDR4-BA1
A_DDR4-BG0
A_DDR4-TEN
A_DDR4-RESET
A_DDR4-ALERT
A_DDR4-DM0
A_DDR4-DQ0
A_DDR4-DQ1
A_DDR4-DQ2
A_DDR4-DQ3
A_DDR4-DQ4
A_DDR4-DQ5
A_DDR4-DQ6
A_DDR4-DQ7
A_DDR4-DQS0_P
A_DDR4-DQS0_N
A_DDR_LANE0
A_DDR_LANE1
A_DDR4-DM1
A_DDR4-DQ8
A_DDR4-DQ9
A_DDR4-DQ10
A_DDR4-DQ11
A_DDR4-DQ12
A_DDR4-DQ13
A_DDR4-DQ14
A_DDR4-DQ15
A_DDR4-DQS1_P
A_DDR4-DQS1_N
CK_t
CK_c
CKE
CS
ODT
PAR
ACT
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
WE/A14
CAS/A15
RAS/A16
NC/A17
BA0
BA1
BG0
VSS/BG1
TEN
RESET
DML/DBIL
DQL0
DQL1
DQL2
DQL3
DQL4
DQL5
DQL6
DQL7
DQSL_t
DQSL_c
DMU/DBIU
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7
DQSU_t
DQSU_c
ALERT
K4A8G165WC-BITDTCV
R58
4K7
1%
R65
499R
1%
R42
4K7
1%
R23
499R
1%
GND
DDR_1V2
U4B
DDR_2V5
VPP
VDD
VDDQ
VSS
VSSQ
ZQ
VSS/UZQ
VREFCA
VREFA
C113
C114
C115
C119
C120
6.3V
470nF
X5R
4.7µF
R59
240R
R68
0R
1%
R8
R19
33R
C2
10nF
10V
X7R
R61
R62
100R
C138
470nF
6.3V
X5R
Title: TE0841 - DDR4_1
A4
Number: TE0841 32I31-A
Rev. 03
Date: 22-May-24
Copyright: Trenz Electronic GmbH
Page 20 of 24
Filename: DDR4-RAM.SchDoc
trenz electronic



trenz electronic

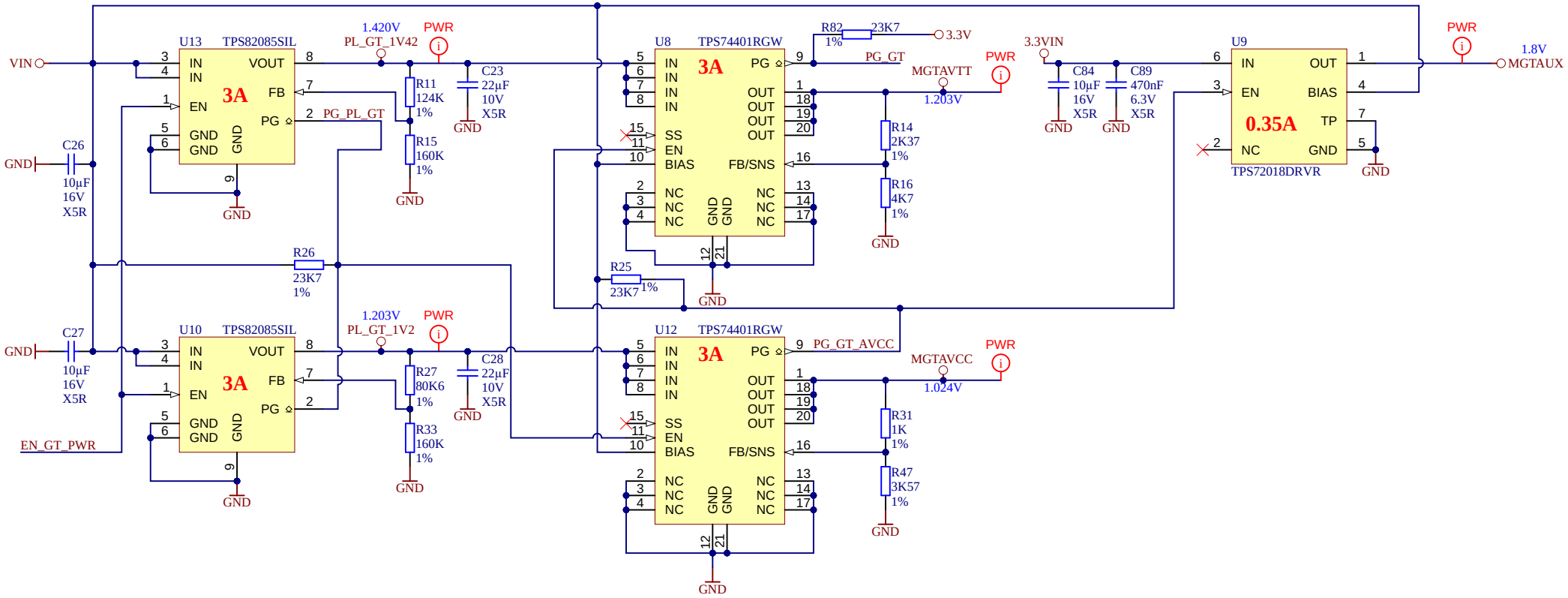
Title: TE0841 - DDR4_2			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 22-May-24	Copyright: Trenz Electronic GmbH		Page 21 of 24
Filename: DDR4-RAM_2.SchDoc			



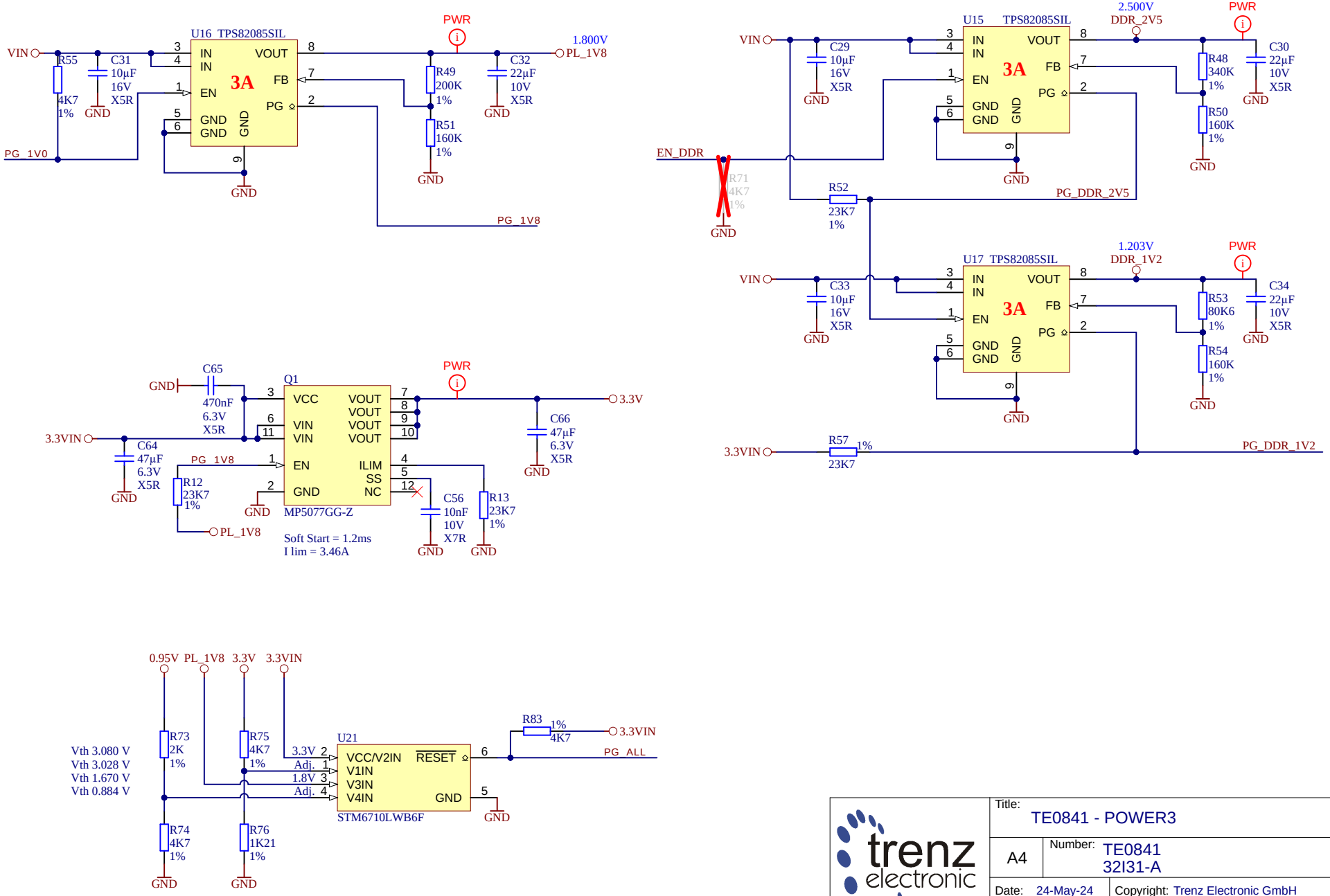
Internal compensation: R70 set populated; R78, C68, C69 set as DNP
External compensation: R70 set as DNP; R78, C68, C69 set populated

trenz electronic

Title: TE0841 - POWER1			
A4	Number: TE0841 32I31-A		Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH		Page 22 of 24
Filename: PWR1.SchDoc			



trenz electronic	Title: TE0841 - POWER2		
	A4	Number: TE0841 32I31-A	Rev. 03
	Date: 22-May-24	Copyright: Trenz Electronic GmbH	Page 23 of 24
	Filename: PWR2.SchDoc		



trenz electronic	Title: TE0841 - POWER3		
	A4	Number: TE0841 32I31-A	Rev. 03
	Date: 24-May-24	Copyright: Trenz Electronic GmbH	Page 24 of 24
	Filename: PWR3.SchDoc		