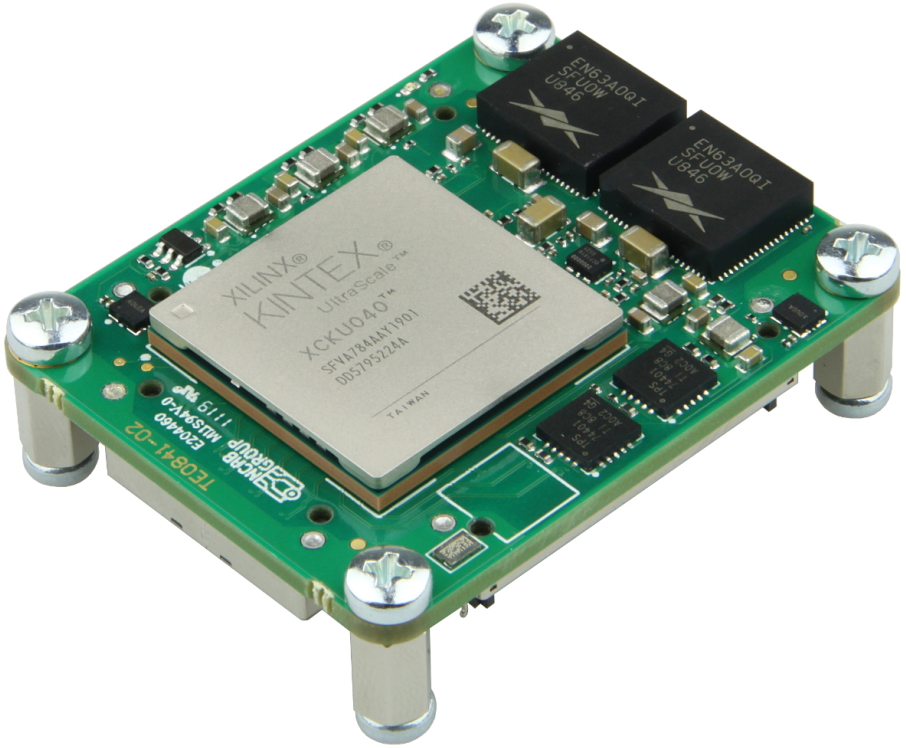

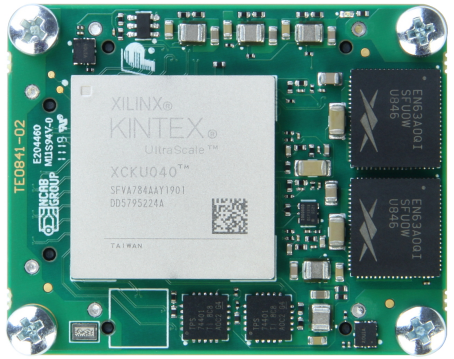

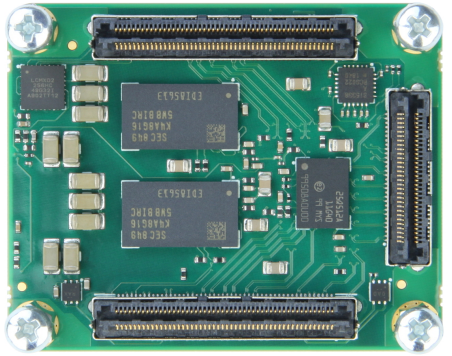

Regarding the usage of our schematics and alike documentation for Trenz module .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0841 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0841 - Legal Notices		
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REV	Description	
-01	Initial revision	
-01A	1) U1: changed schematic symbol. Next pins swapped to match same polarity order: -- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64) -- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66) 2) Net names changed (no electrical changes): JM1: swapped signals B64_L6: -- B64_L6_N - pin 40 (was pin 42) -- B64_L6_P - pin 42 (was pin 40) JM3: swapped signals B64_L6: -- B66_L18_N - pin 52 (was pin 54) -- B66_L18_P - pin 54 (was pin 52)	
-02	1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC) 2) Fixed sense connection on DCDC 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E 4) Full update LIB 5) Added additional resistors for support 16GBit DDR chips 6) Added strong pull-down to EN_PL 7) Added additional testpoints for I2C bus 8) Added additional MEMS oscillator (25MHz) 9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net 10) Added pull-down on the EN_DDR (04.05.2022) 11) S/N Track-it pad set not fitted 12) Change Resistor value R27 (49k9 -> 80k6), rename net "PL_GT_1V05 -> PL_GT_1V2" -----(23.10.2023)	
-03	1) L1, L2, L3, L4, L5, L6 were changed from BKP0603HS121-T to MPZ0603S121HT000 2) D2 was added 3) Q1 TPS27082LDDCR was changed to MP5077GG-Z 4) U21 STM6710LWB6F was added 5) U7 and U14 were changed from EN63A0QI to LTM4638EY 6) Signal trace lengths were changed. PCB routing was improved 7) Legal Notices and Power diagram pages were added 8) System Overview was added on page TE0841.SchDoc 9) Net names for pins 4 and 5 for U11 were swapped 10) C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C89 were added 11) R79, R80, R81, R82, R83 were added 12) R35 was changed from 4.7k to 2.37k 13) C49 was changed from 4u7 6.3V 0402 to 10u 16V 0603 14) TP3 - TP37 were added 15) R25, R26, R52, R57 were changed from 4k7 to 23k7 16) U11 was changed from DSC1123DL5-200 to SIT9121AI-2B1-XXE-200.00000 17) All SCH symbols and PCB footprints were updated from library 18) R11 was changed from 110k to 124k, net "PL_GT_1V35" was renamed to "PL_GT_1V42" 19) R71 setted as "DNP"	MT

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Title: TE0841 - Changes List		
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Filename: Revision_Changes.SchDoc		

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc

U_PWR3
PWR3.SchDoc

U_PWR-DIAGRAM
Power_Diagram.SchDoc

Mount.Hole 3.2mm GND

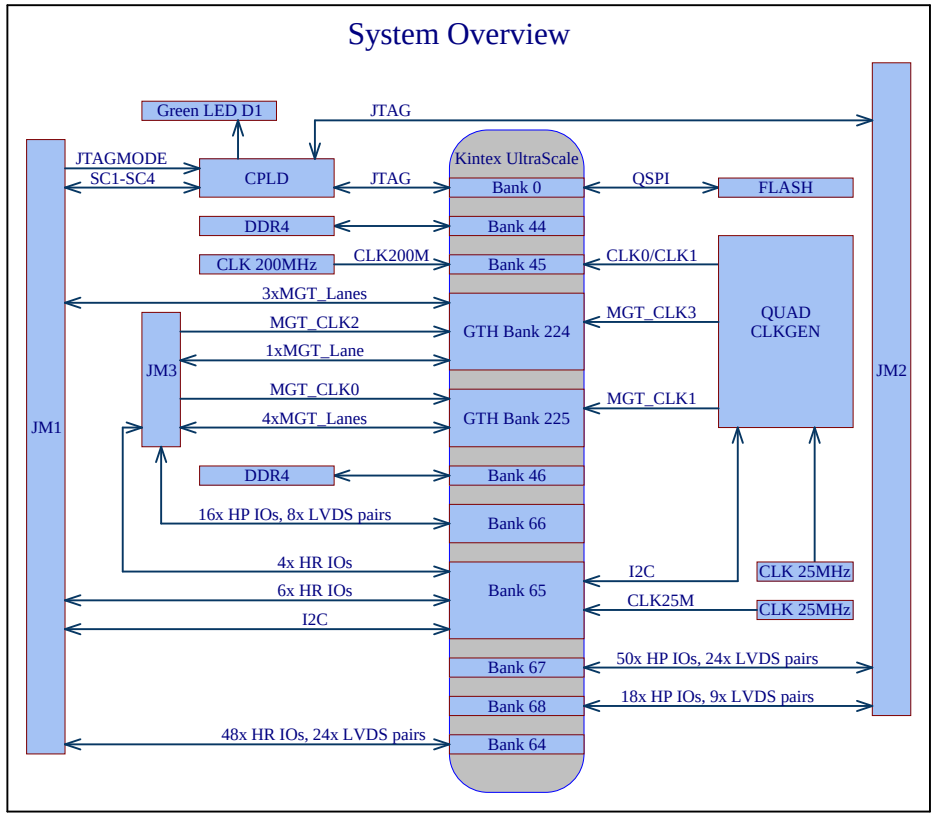
Mount.Hole 3.2mm GND

Mount.Hole 3.2mm GND

Mount.Hole 3.2mm GND

PM1 PM2 PM3 PM4 PM5 PM6

System Overview



Top side testpoints:

PLL_SCL	TP1	
PLL_SDA	TP2	
	TP3	
3.3VIN	TP4	
PL_1V8	TP5	
B64_VCO	TP6	
B66_VCO	TP7	
B67_VCO	TP8	
B68_VCO	TP9	
VBAT_IN	TP10	
VBATT	TP11	
MGTAUX	TP12	
GND		
PROG_B	TP13	
DONE	TP14	
INIT_B	TP15	
	TP16	
GND		

Bottom side testpoints:

PLL_SCL	TP17	
PLL_SDA	TP18	
PL_GT_1V42	TP19	
PL_GT_1V2	TP20	
DDR_2V5	TP21	
DDR_1V2	TP22	
0.95V	TP23	
MGTAVCC	TP24	
MGTAVTT	TP25	
VBATT	TP26	
MGTAUX	TP27	
AVCC	TP28	
PROG_B	TP29	
DONE	TP30	
INIT_B	TP31	
GND	TP32	
PG_ALL	TP33	
A_DDR4-TEN	TP34	
	TP35	
VREFA	TP36	
VREFA2		
B_DDR4-TEN	TP37	

Top of Board

Screw M3x4 — Standoff M3x8 II — Screw M3x6

Screw M3x4 — Standoff M3x8 II — Screw M3x6

Screw M3x4 — Standoff M3x8 II — Screw M3x6

Screw M3x4 — Standoff M3x8 II — Screw M3x6

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

Serial

Serial

Serialnumber 6,3 x 6.3mm

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

Special notes:

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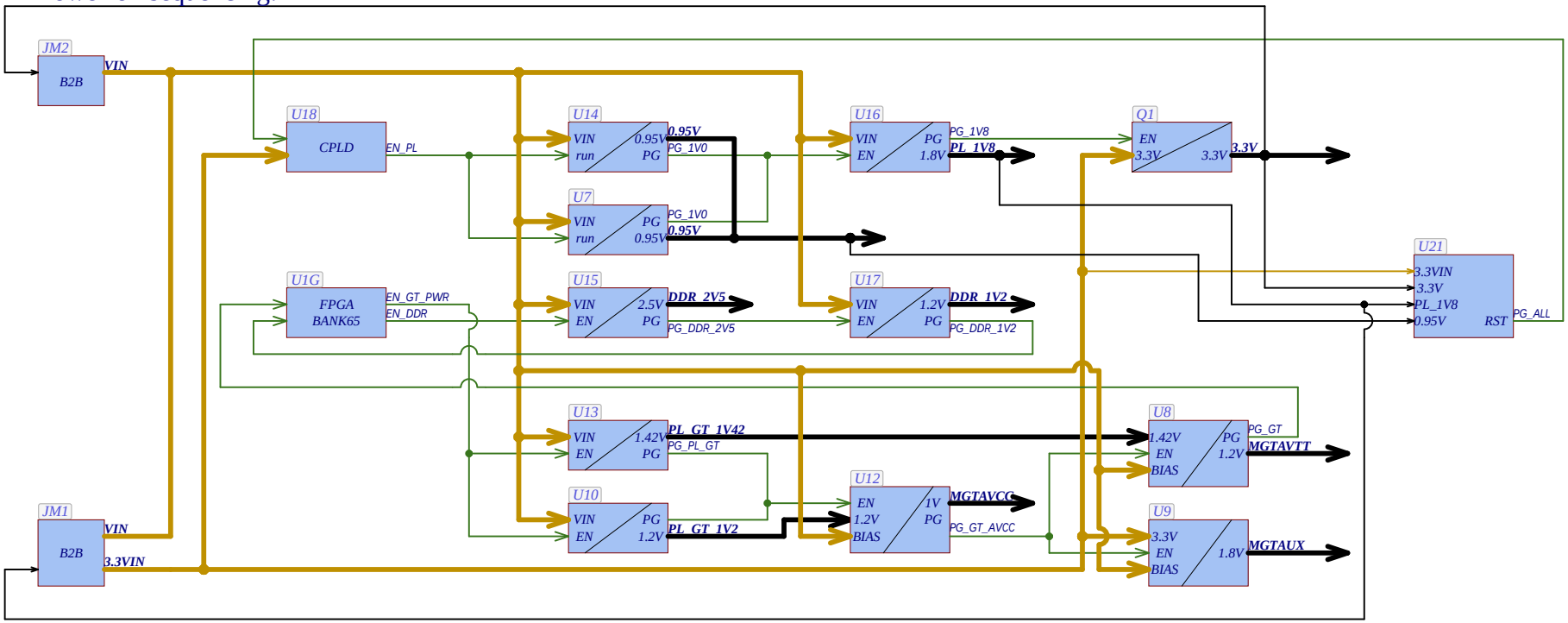
Power-on sequencing:



Current Consumers:

Power Rail	Voltage	Consumer	Note
0.95V	0.95V	FPGA VCCINT FPGA VCCBRAM FPGA VCCINT_IO	-
DDR_2V5	2.5V	DDR4 VPP	-
DDR_1V2	1.2V	FPGA VCCO_44 FPGA VCCO_46 DDR4 VDD	-
PL_1V8	1.8V	FPGA VCCO_0 FPGA VCCO_45 QUAD CLK VDDO CPLD VCCIO2 FPGA VCCAUX FPGA VCCAUX_IO QSPI FLASH VCC FPGA VCC_ADC	-
MGTAVCC	1.0V	FPGA MGTAVCC	-
MGTAVTT	1.2V	FPGA MGTAVTT	-
MGTAUX	1.8V	FPGA MGTAUX	-
3.3V	3.3V	FPGA VCCO_65 QUAD CLK VDD	-

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3V-5.0V	+5%/-3%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VBAT_IN	IN	2.2 - 5.5V	-	Fpga Vbatt	-
B64_VCCO	IN	1.14 - 3.4V	-	IO Bank64	-
B66_VCCO	IN	0.95 - 1.89V	-	IO Bank66	-
B67_VCCO	IN	0.95 - 1.89V	-	IO Bank67	-
B68_VCCO	IN	0.95 - 1.89V	-	IO Bank68	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-
PL_1V8	OUT	1.8V	+/-3%	Power for Carrier	-

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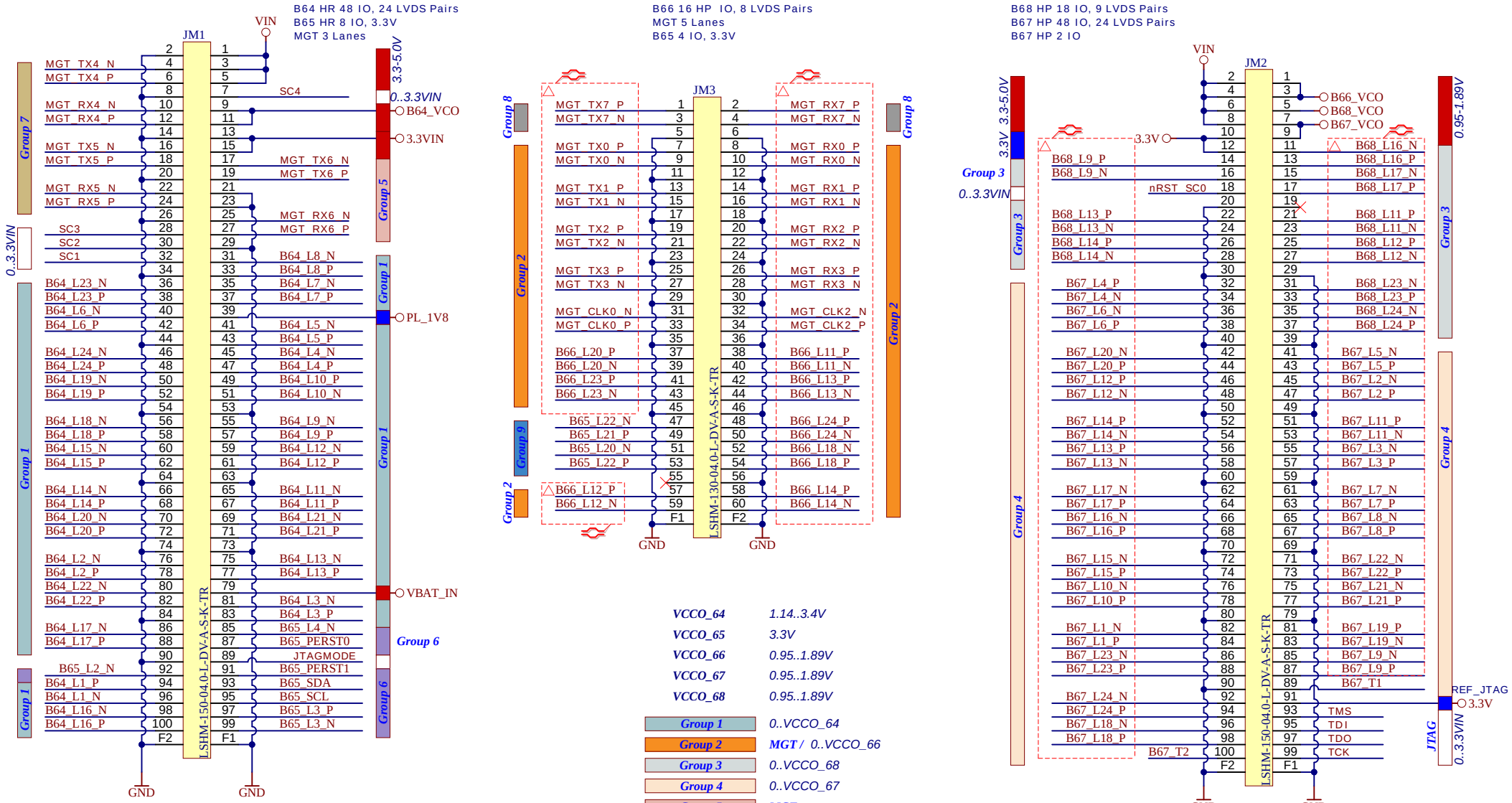
Title: TE0841 - Power Diagram		
A4	Number: TE0841 31C31-A	Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH	Page 4 of 24
Filename: Power_Diagram.SchDoc		



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Title: TE0841 - B2B Connectors			
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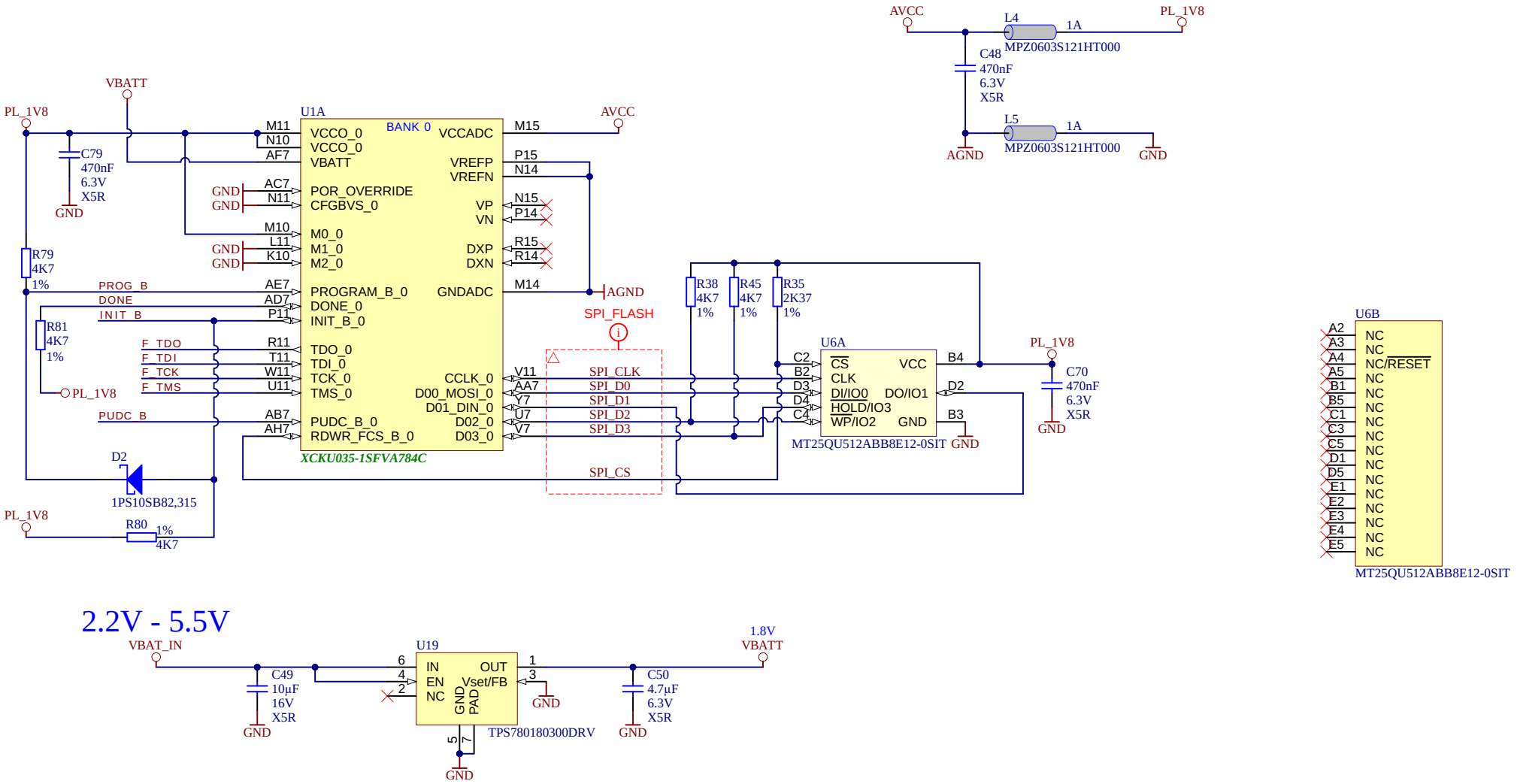
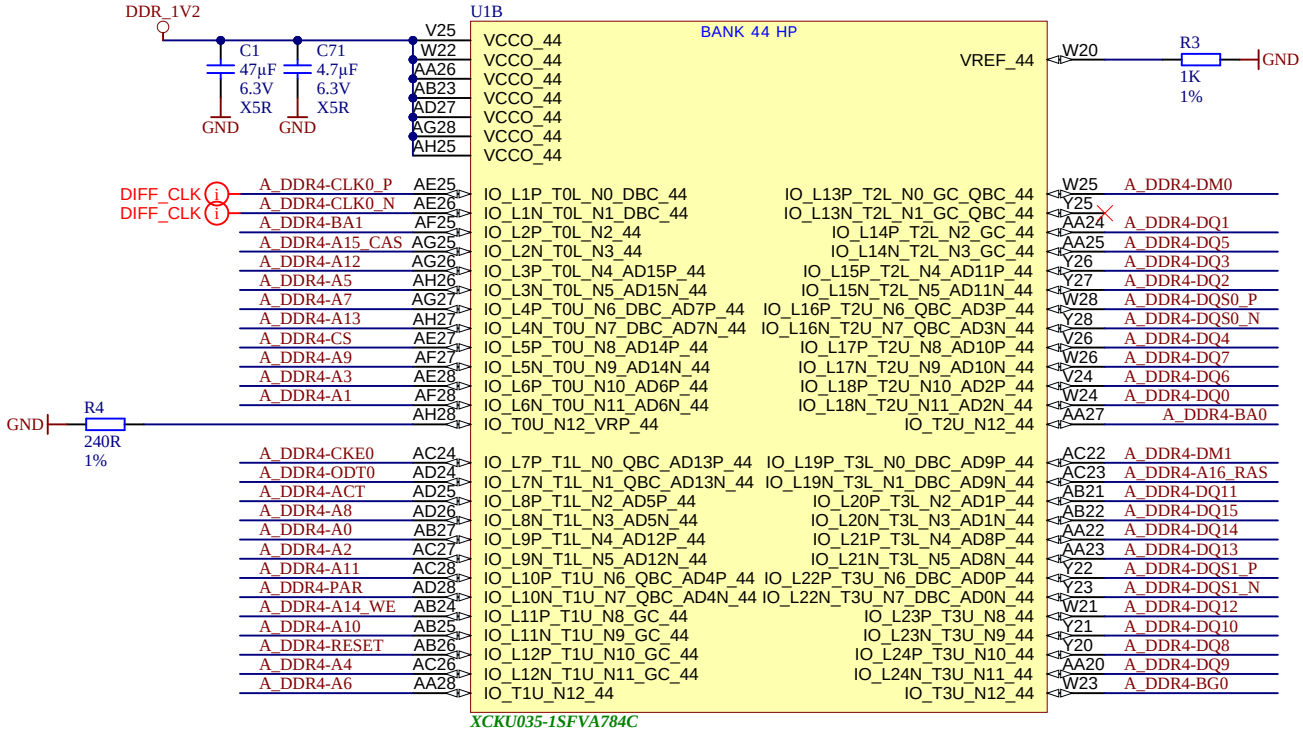
Date: 21-May-24	Copyright: Trenz Electronic GmbH		Page 5 of 24
Filename: B2B-Connectors.SchDoc			



trenz electronic	Title: TE0841 - MISC		
	A4	Number: TE0841 31C31-A	Rev. 03
	Date: 22-May-24	Copyright: Trenz Electronic GmbH	Page 6 of 24
	Filename: FPGA-MISC.SchDoc		



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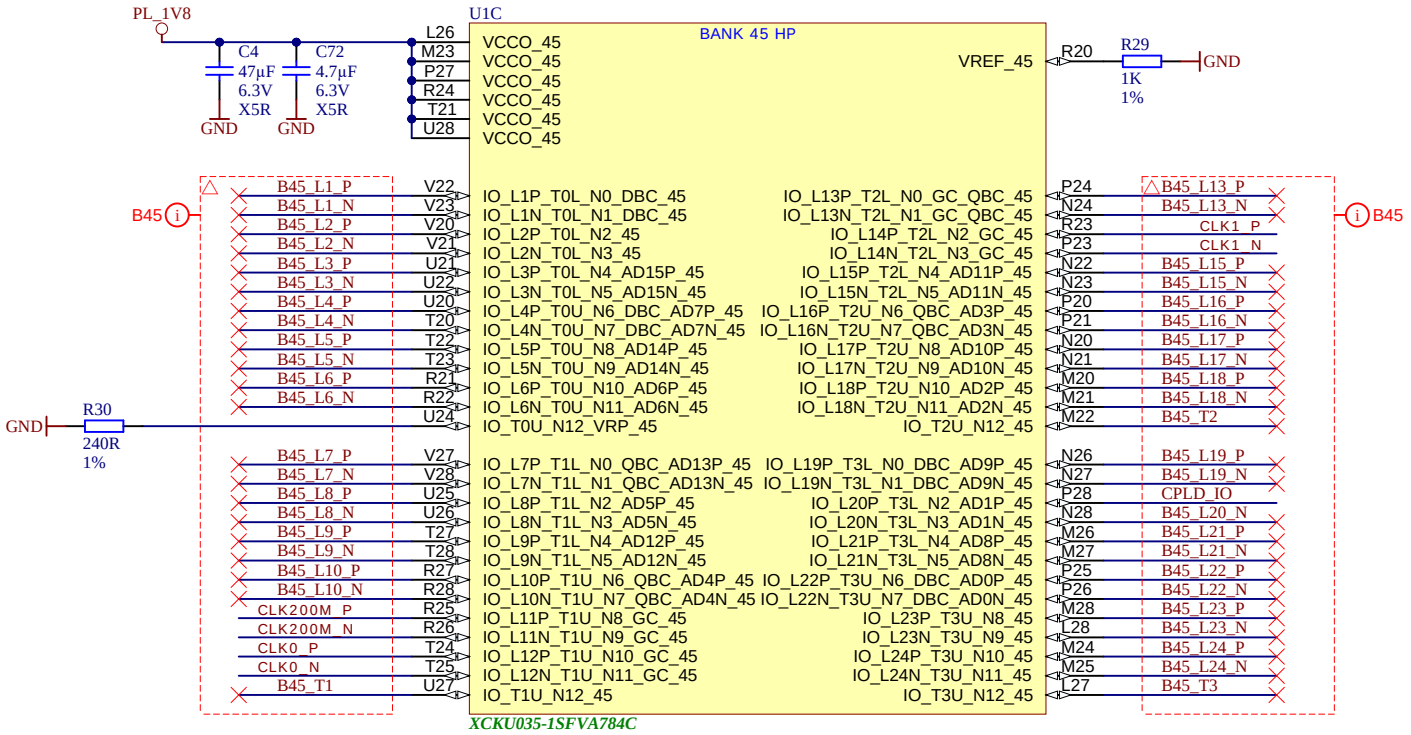
Date: 27-May-24	Copyright: Trenz Electronic GmbH		Page 7 of 24
Filename: FPGA-B44.SchDoc			



trenz electronic	Title: TE0841 - BANK45		
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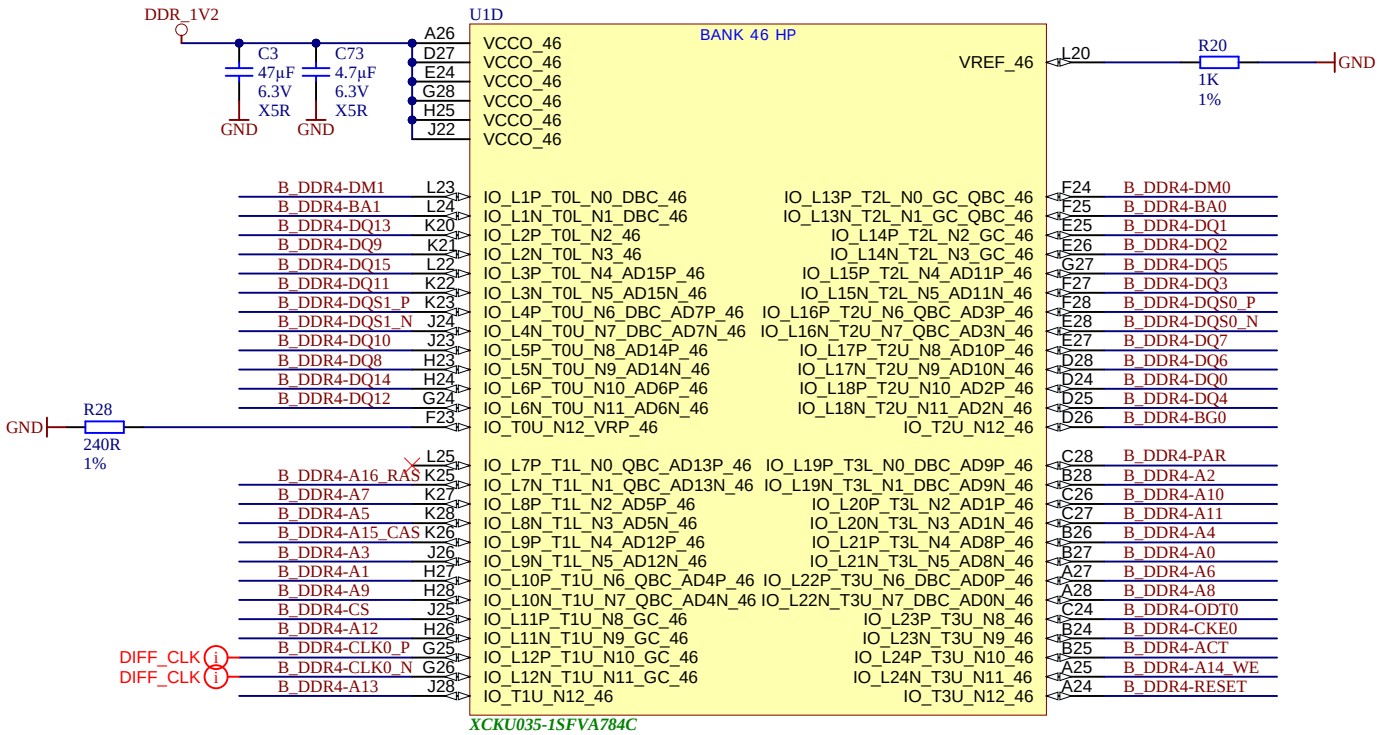
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 8 of 24
Filename: FPGA-B45.SchDoc			



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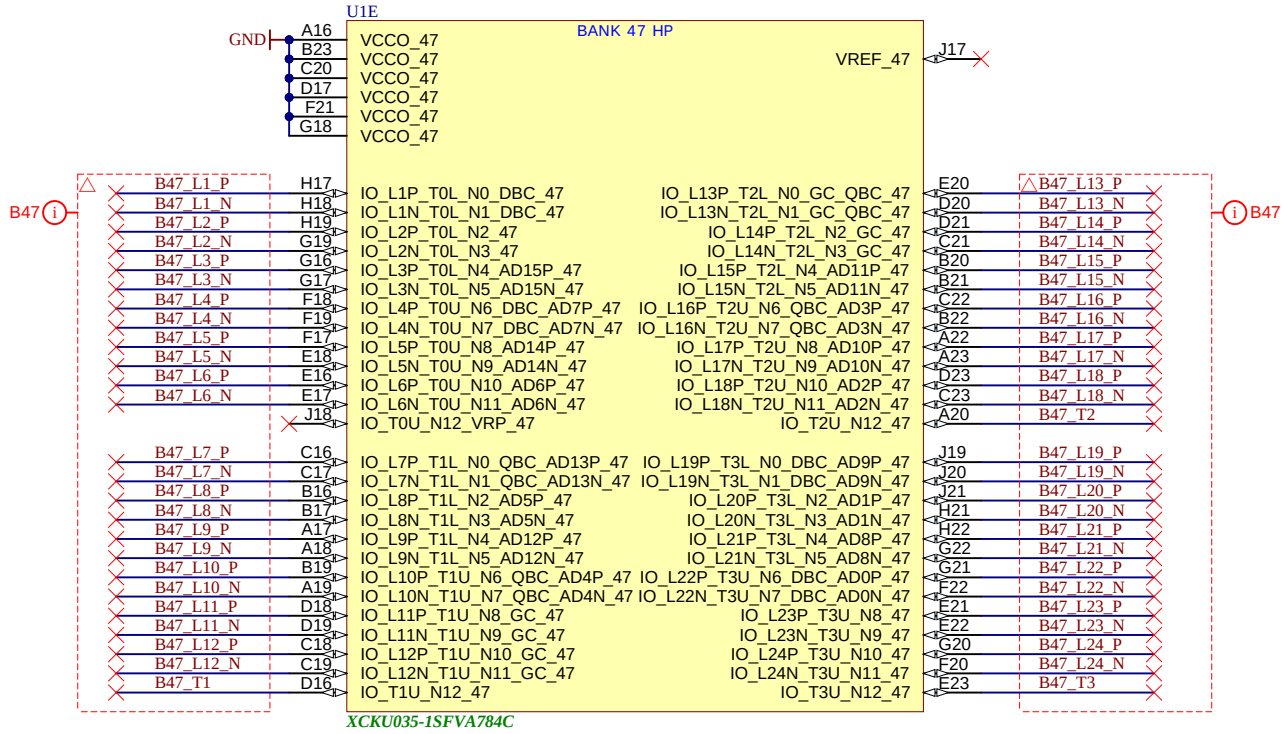
Date: 27-May-24	Copyright: Trenz Electronic GmbH		Page 9 of 24
Filename: FPGA-B46.SchDoc			



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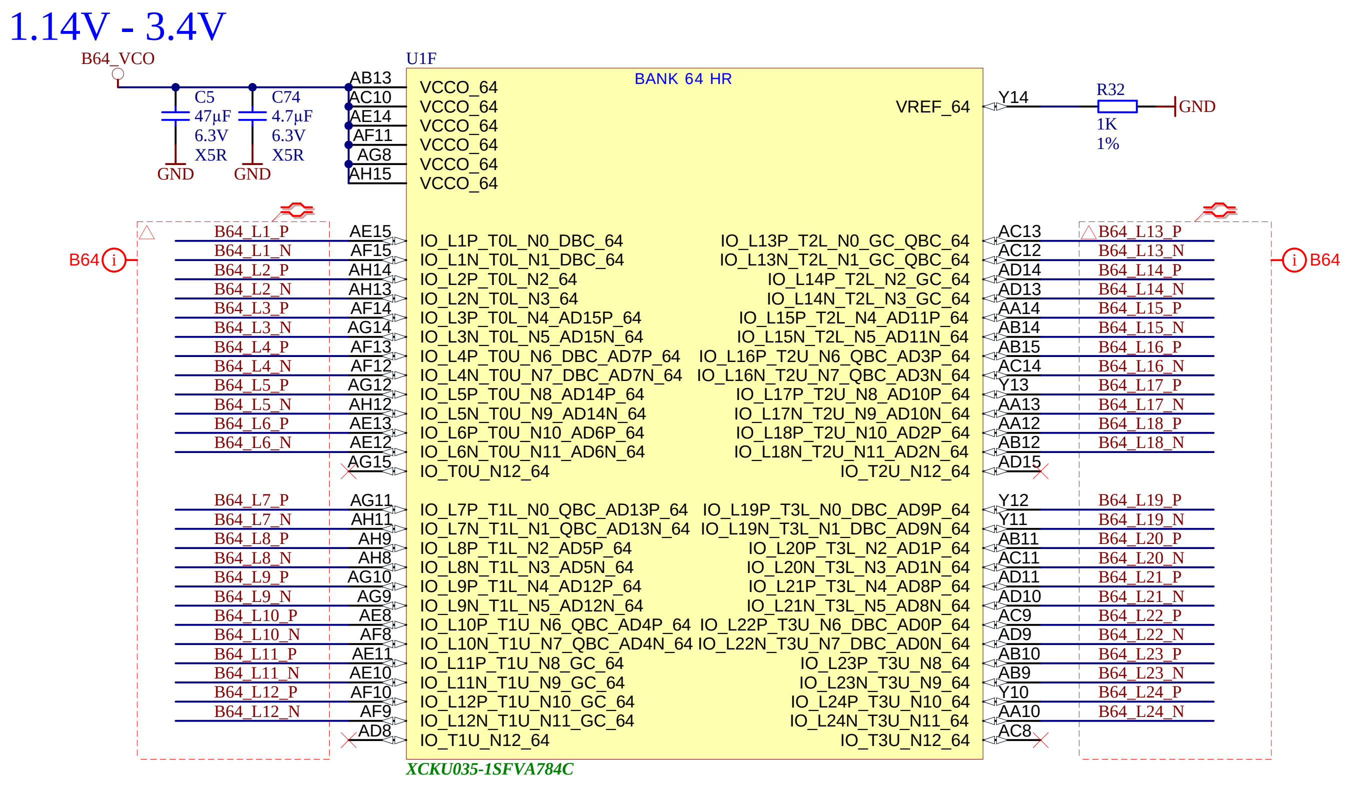
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 10 of 24
	Filename: FPGA-B47.SchDoc	



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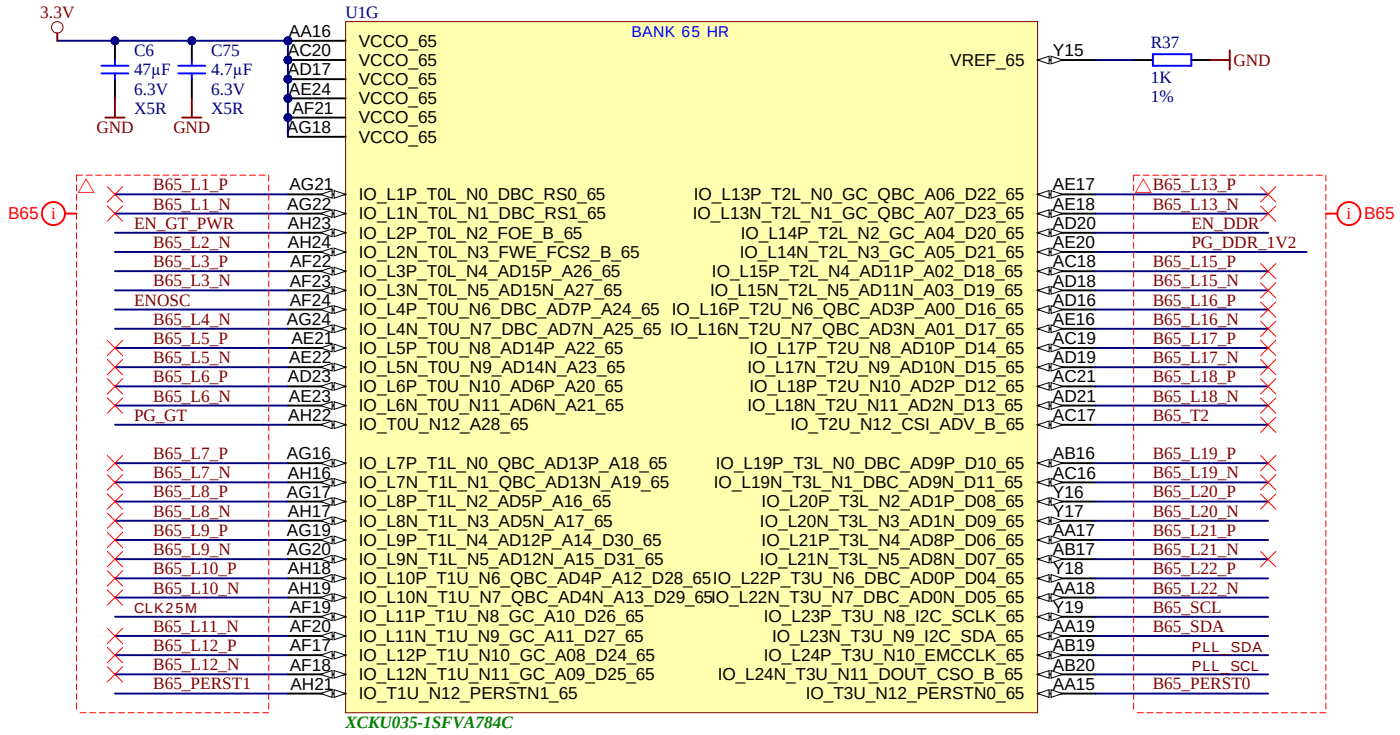
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 11 of 24
Filename: FPGA-B64.SchDoc			



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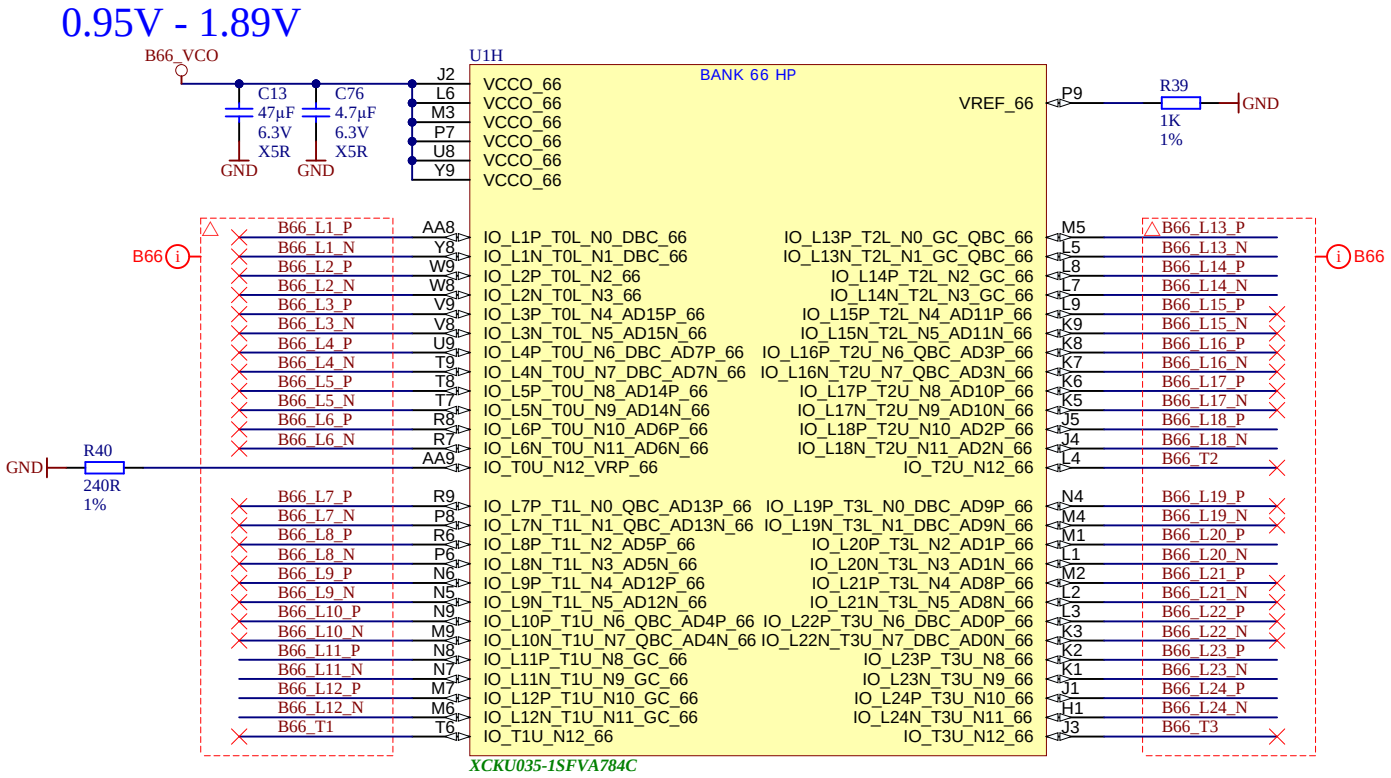
Date: 21-May-24	Copyright: Trenz Electronic GmbH		Page 12 of 24
Filename: FPGA-B65.SchDoc			



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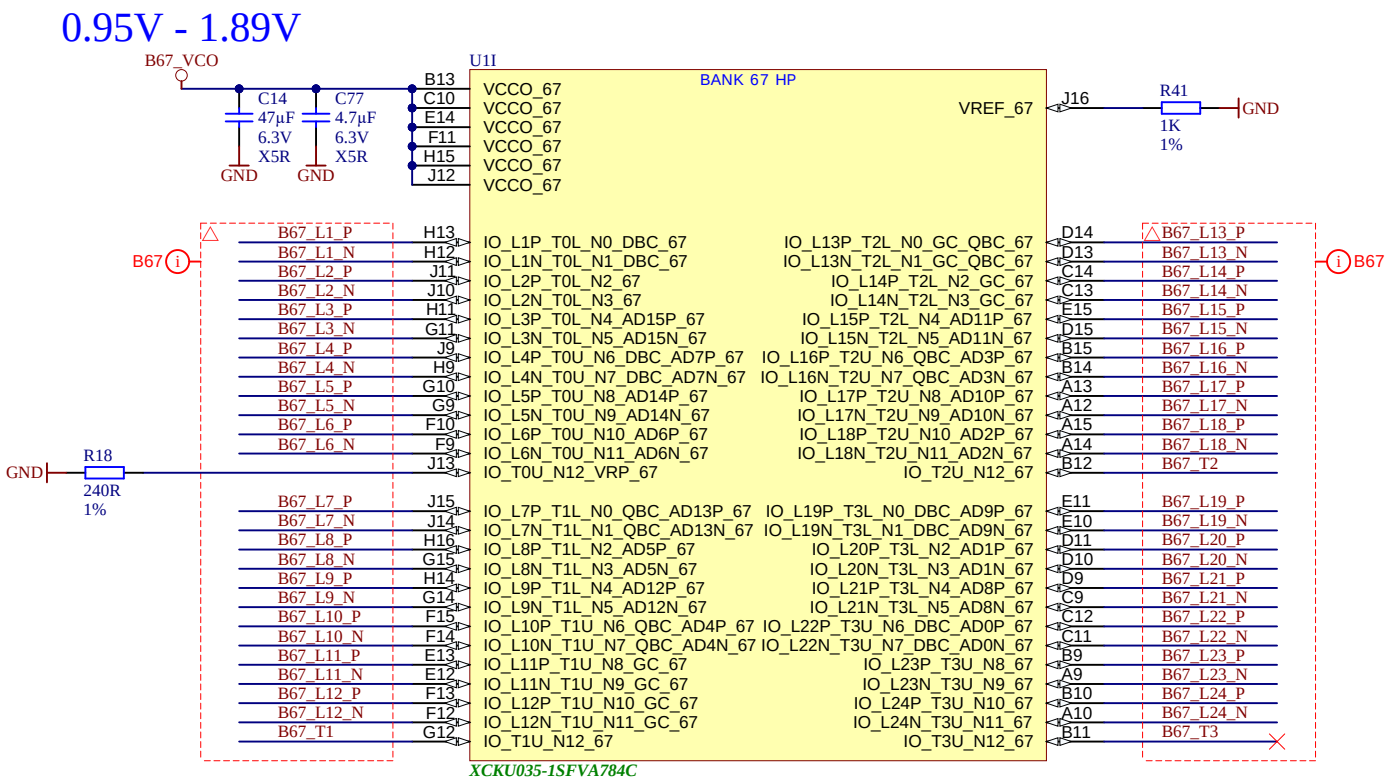
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 13 of 24
Filename: FPGA-B66.SchDoc		



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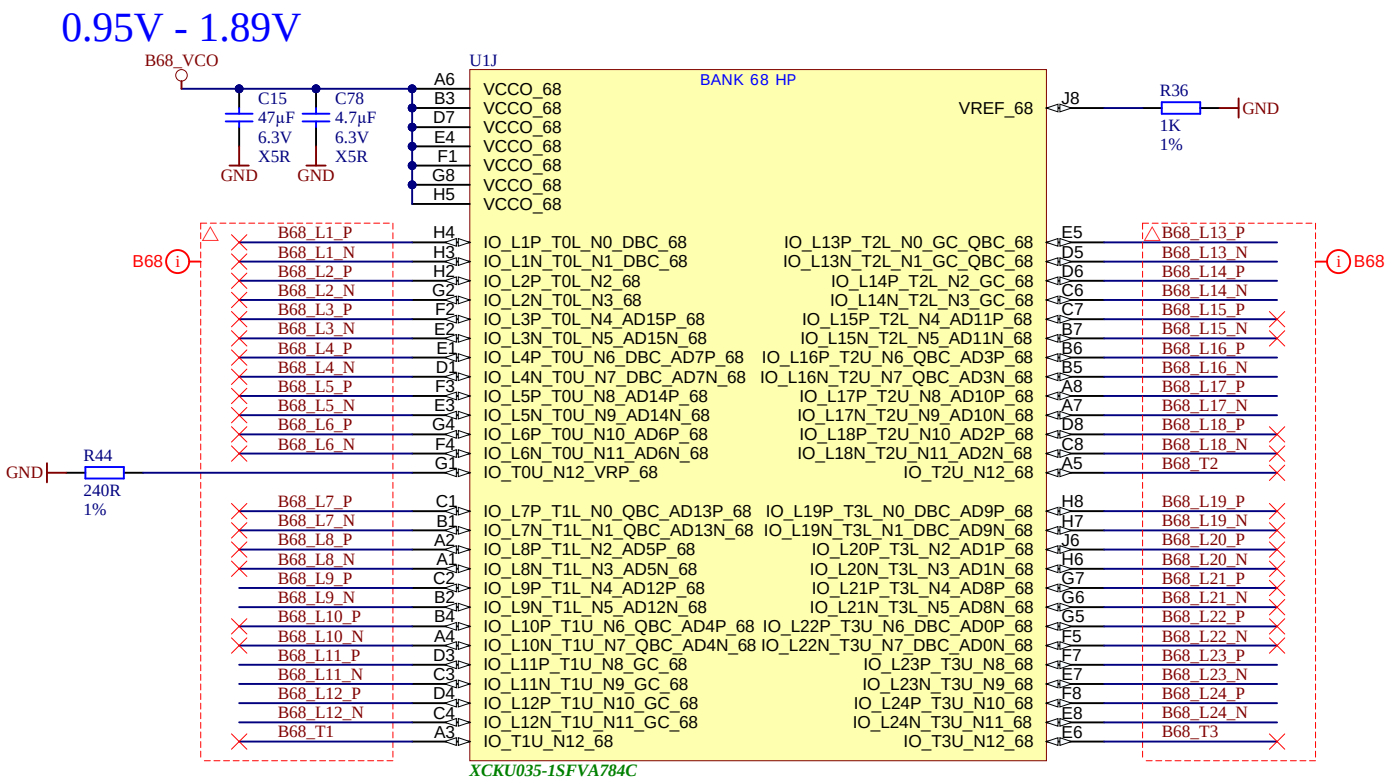
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 14 of 24
Filename: FPGA-B67.SchDoc		



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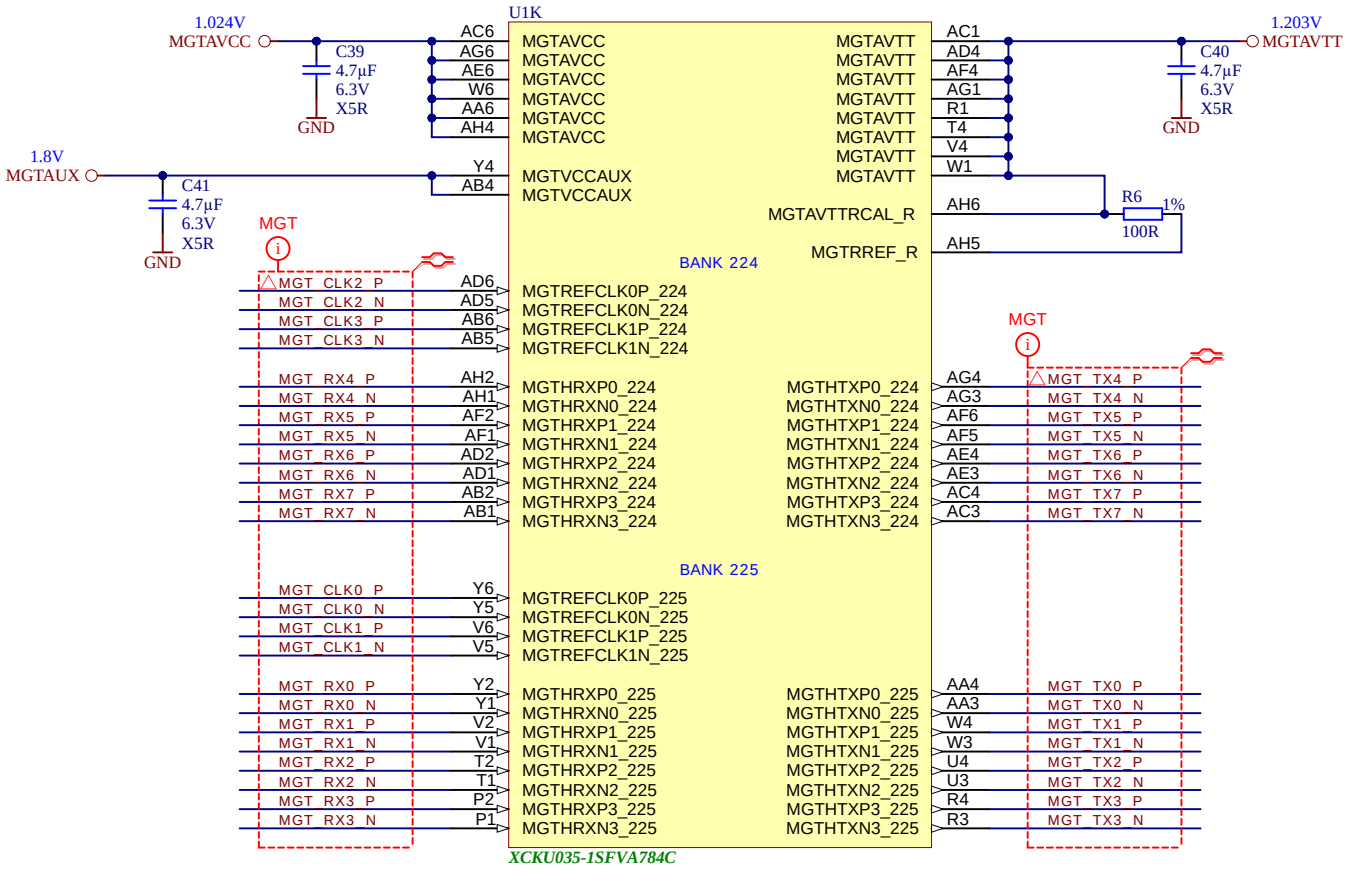
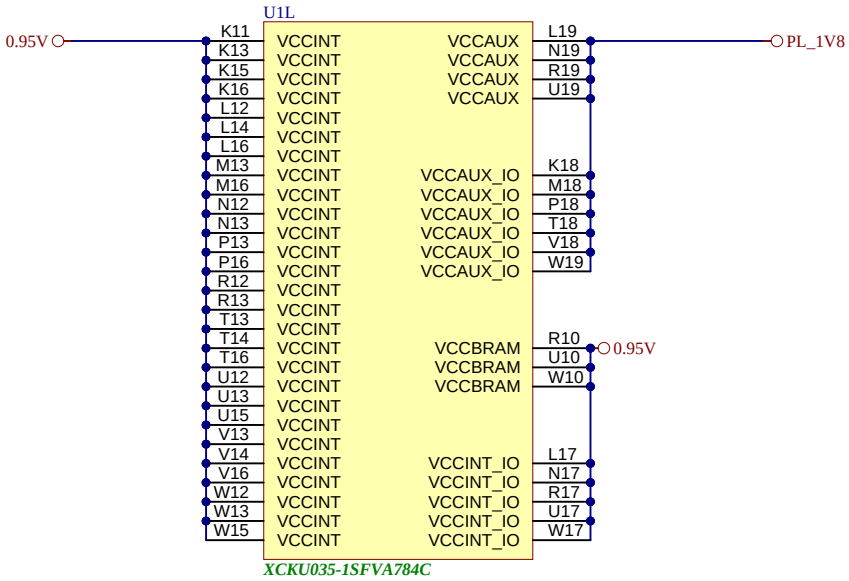
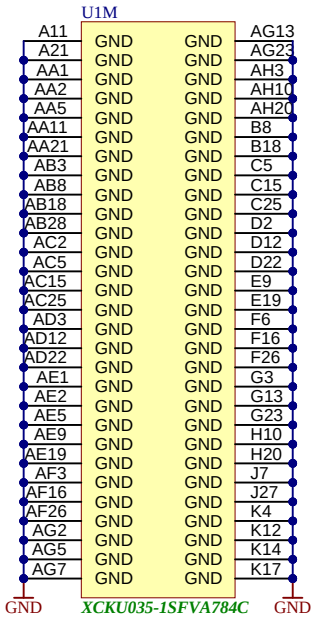
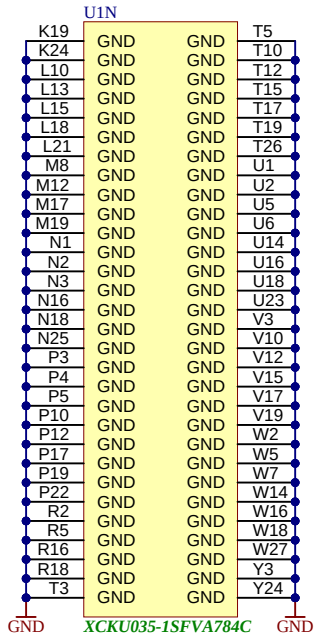
	Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 15 of 24
	Filename: FPGA-B68.SchDoc		

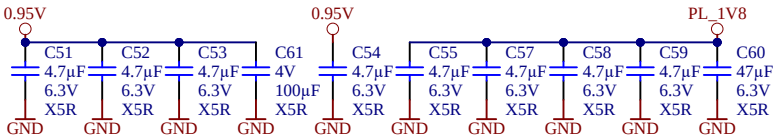


trenz electronic	Title: TE0841 - MGT		
A4	Number: TE0841 31C31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 16 of 24
Filename: FPGA-MGT.SchDoc			









Title: TE0841 - FPGA POWER		
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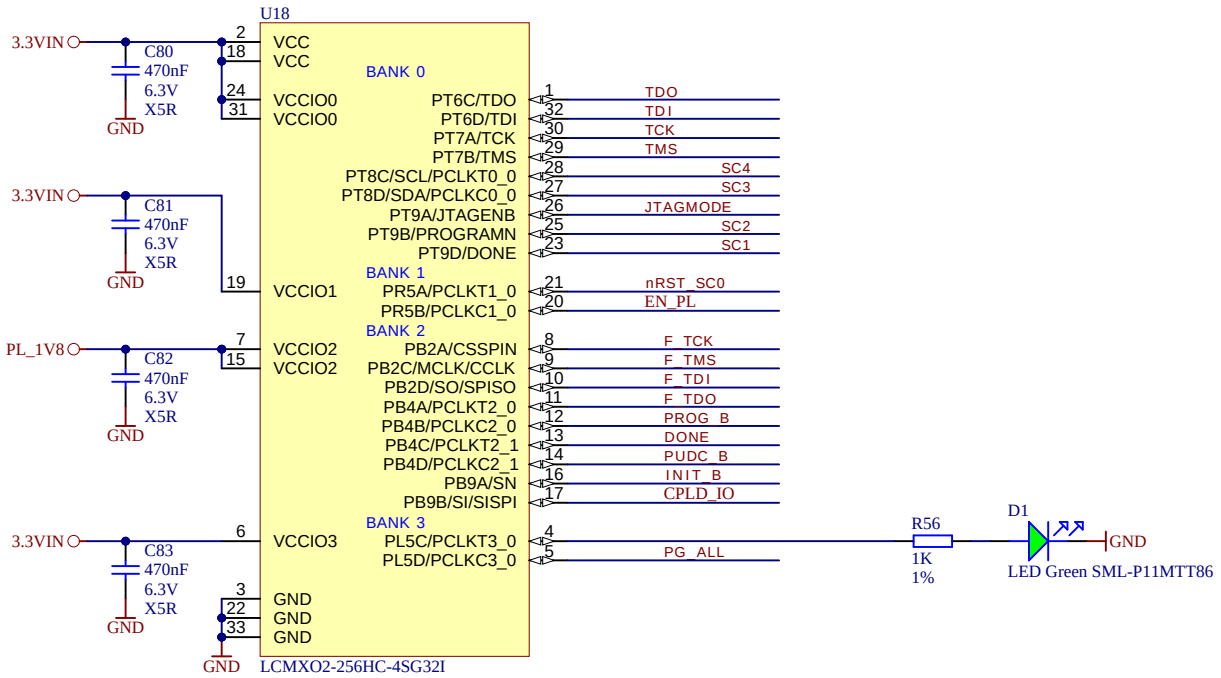
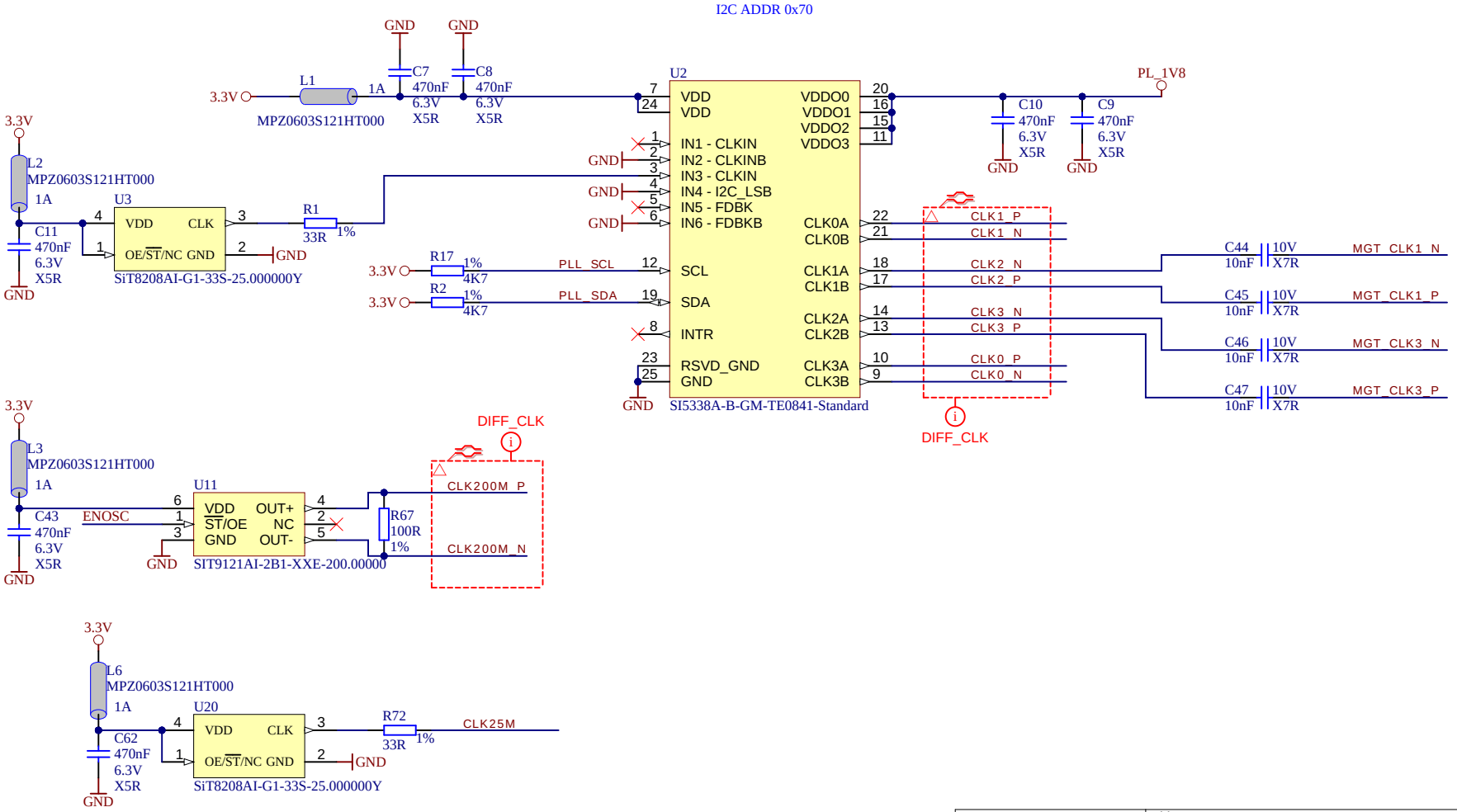
Date: 17-May-24	Copyright: Trenz Electronic GmbH	Page 17 of 24
Filename: FPGA-PWR.SchDoc		



trenz electronic	Title: TE0841 - CPLD		
A4	Number: TE0841 31C31-A		Rev. 03
Date: 17-May-24	Copyright: Trenz Electronic GmbH		Page 18 of 24
Filename: CPLD.SchDoc			



trenz electronic	Title: TE0841 - CLOCK		
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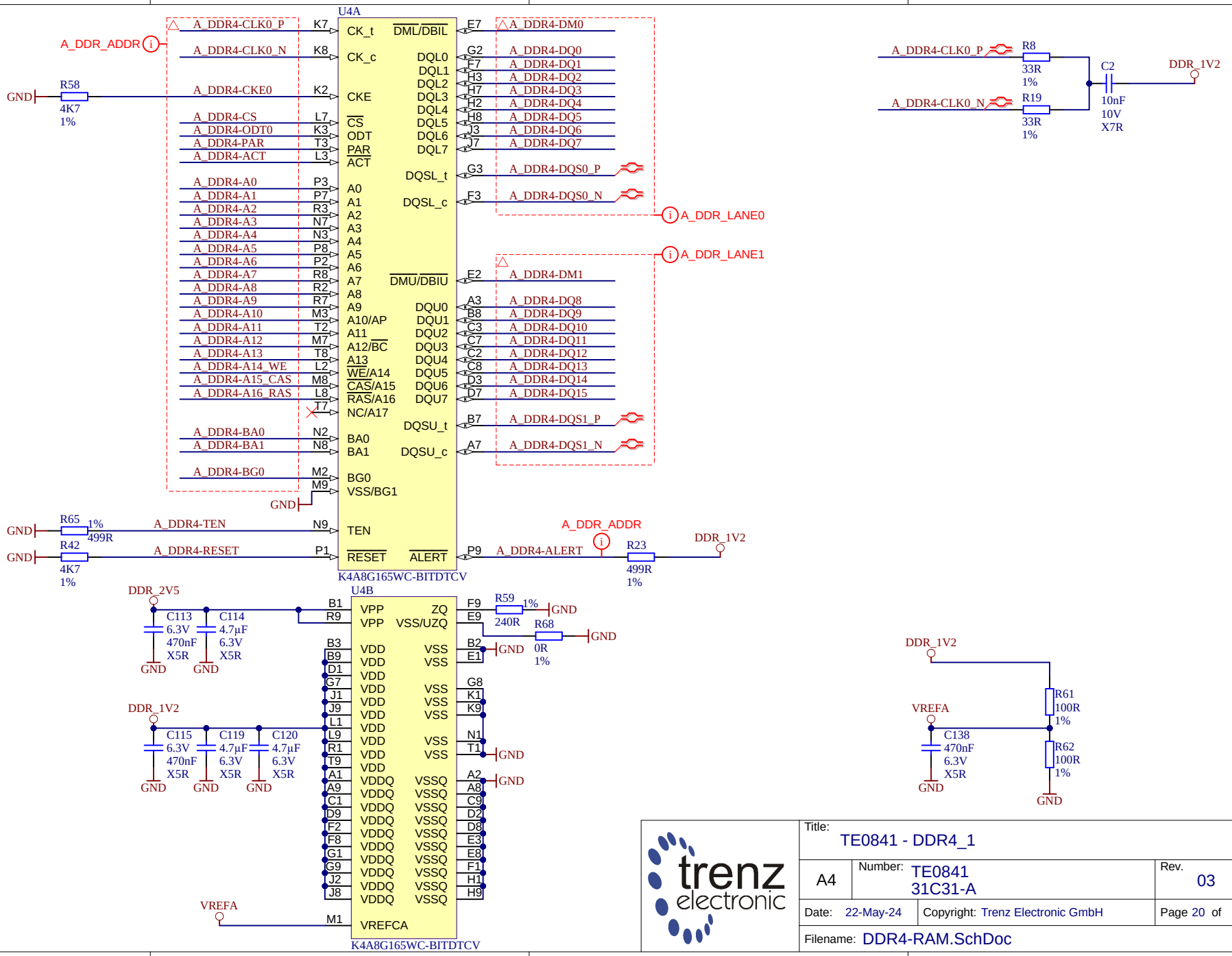
Date: 23-May-24	Copyright: Trenz Electronic GmbH		Page 19 of 24
Filename: Clock.SchDoc			



Title: TE0841 - DDR4_1			
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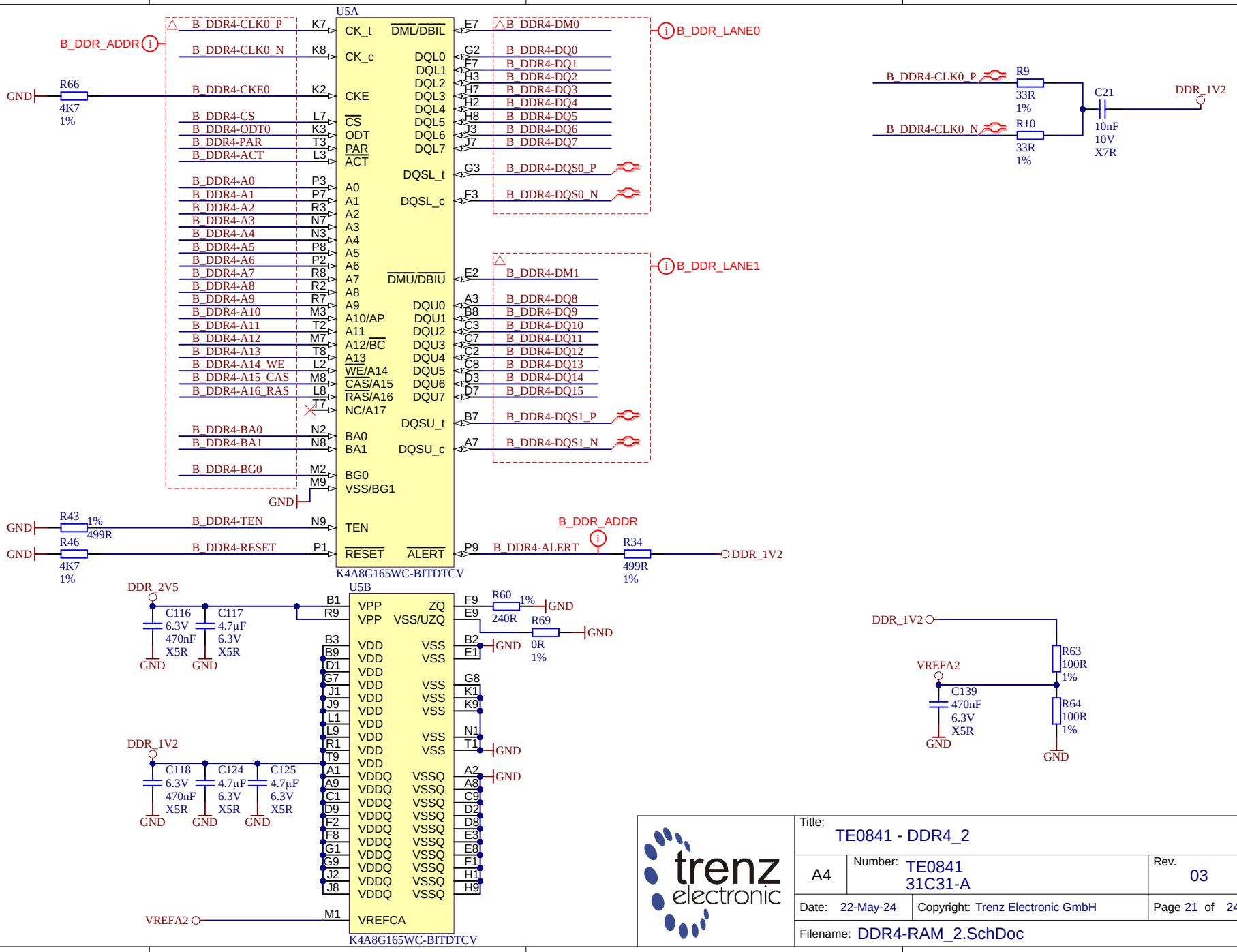
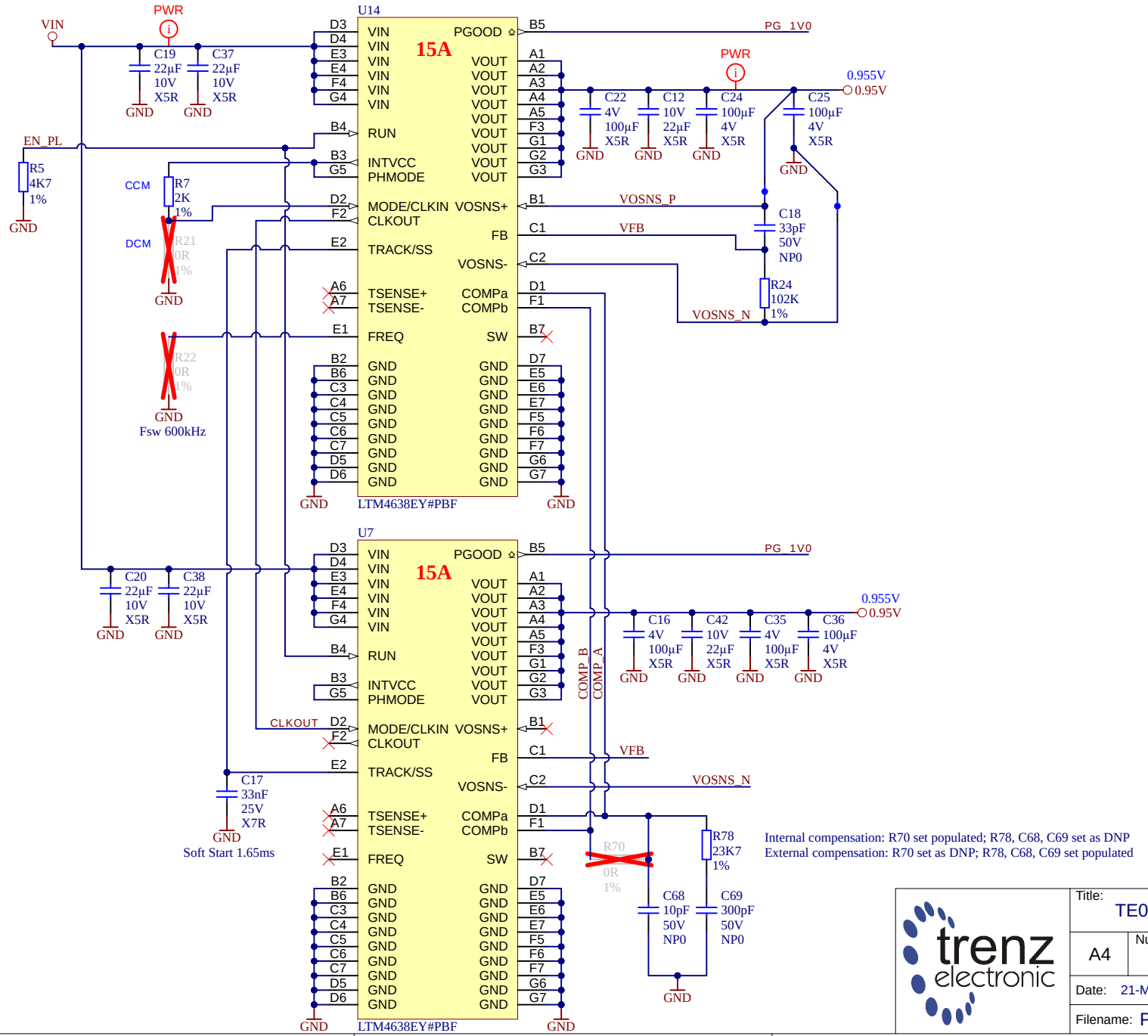
Date: 22-May-24	Copyright: Trenz Electronic GmbH		Page 20 of 24
Filename: DDR4-RAM.SchDoc			



Title: TE0841 - DDR4_2			
A4	Number: TE0841 31C31-A		Rev. 03
Date: 22-May-24	Copyright: Trenz Electronic GmbH		Page 21 of 24
Filename: DDR4-RAM_2.SchDoc			



Internal compensation: R70 set populated; R78, C68, C69 set as DNP
External compensation: R70 set as DNP; R78, C68, C69 set populated

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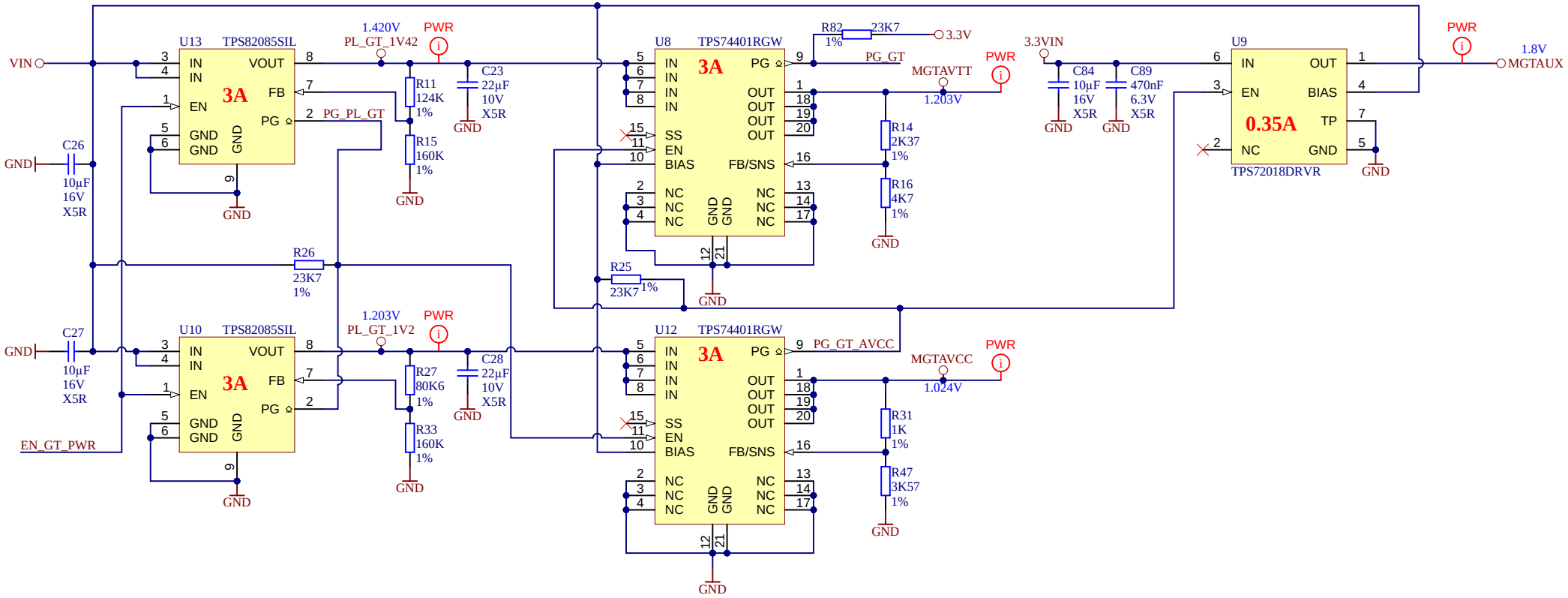
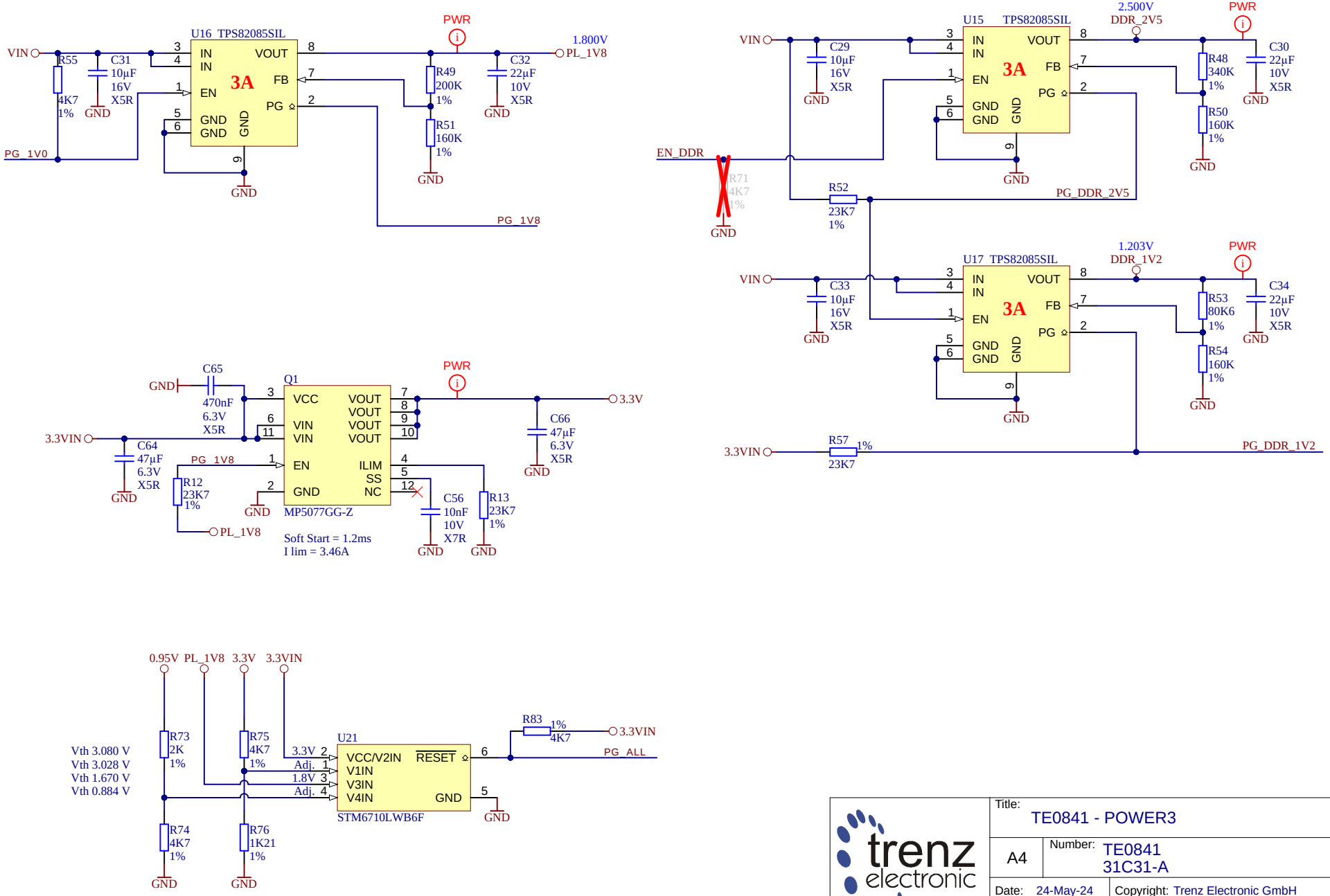
Title: TE0841 - POWER1		
A4	Number: TE0841 31C31-A	Rev. 03
Date: 21-May-24	Copyright: Trenz Electronic GmbH	Page 22 of 24
Filename: PWR1.SchDoc		



trenz electronic	Title: TE0841 - POWER2		
	A4	Number: TE0841 31C31-A	Rev. 03
	Date: 22-May-24	Copyright: Trenz Electronic GmbH	Page 23 of 24
	Filename: PWR2.SchDoc		



trenz electronic	Title: TE0841 - POWER3		
	A4	Number: TE0841 31C31-A	Rev. 03
	Date: 24-May-24	Copyright: Trenz Electronic GmbH	Page 24 of 24
	Filename: PWR3.SchDoc		