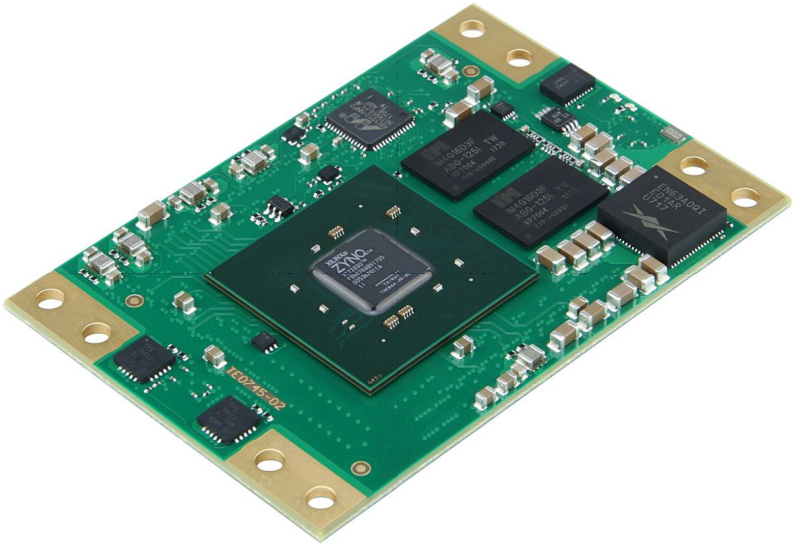

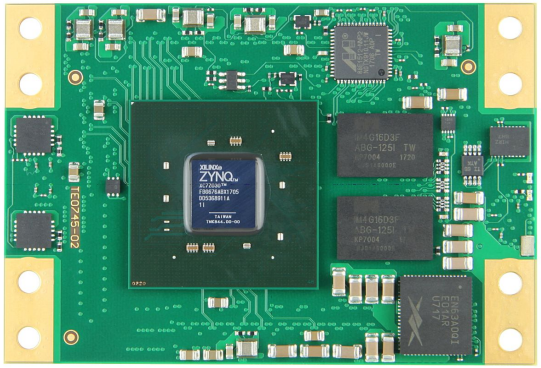

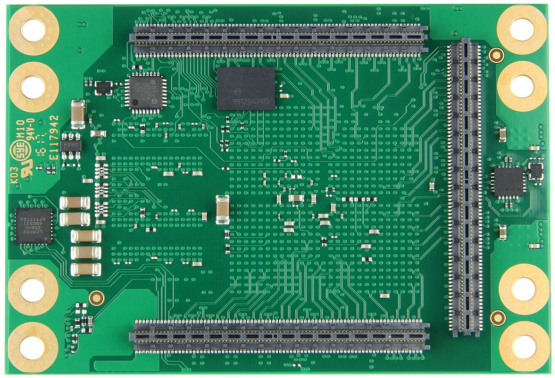

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation,
even if the design is just adapted or modified.
TE0745 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.
Schematics and other handouts serve for informational purposes only!

Design drawn by:	ED
Checked by:	MR
Assembly variant:	92I31-A
Created by:	MR
Modified by:	MR
Modified at:	2021-02-19

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Title: TE0745 - Legal Notices Modules

A4	Number: TE0745 92I31-A	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH	Page 1 of 26
Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02	1. MAC EEPROM Address patch fixed on PCB. 2. Lib components update.	
-03	1. Removed serial number S/N. Connected U2 pin 20 to net "BOOTMODE". 2. Changed DCDC (U4) from EN63A0QI to MP8869SGL-Z and adapted corresponding circuit. Added assembly option to connect U4 to I2C bus via R91/R101 (I2C address 0x61). 3. Increase rated voltage for capacitors C108, C142, C147, C148, and C149 from 6.3 V to 25 V. 4. Added diode D3 between signal "RST_IN_N" and "PS_1.8V". 5. Added resistor R106 between CPLD U2 pin 25 and signal "RST_IN_N". 6. Added option for diode D4 population between signal "PROG_B" and "INIT". 7. Changed clock U33 from SiT8008AI-73-XXS-52.000000E to SiT8008BI-73-XXS-52.000000E. 8. Added testpoints TP1...43. 9. Added voltage monitors U20 and U22 with according circuits. 10. Added pull-up resistor R73 for net "PWR_PL_OK". 11. Added resistor R103 to optionally connect U31 PG to signal "PWR_PS_OK" or voltage monitor U20. 12. Changed supply voltage for VCCPLL from PL_1.8V to PS_1.8V. 13. Tied DXP/DXN (U1 pins R14 and R13) directly to GND. 14. Added soft start capacitor options C62 for U8 and C78 for U11. 15. Added decoupling capacitors - C126, C127 for U16, - C129 for U14, - C130 for U19, - C131 for U18, - C144 for U8, - C150 for U11, - C151/C152 for U6, - C153/C154 for U17, - C155/C156 for U32, and - C128 and C157 for U1. 16. Changed voltage rating from 6.3 V to 10 V for 100 uF capacitors. 17. Changed voltage rating from 6.3 V to 16 V for 10 uF capacitors. 18. Changed voltage rating from 6.3 V to 10 V and size from 0402 to 0603 for capacitors C21 and C29. 19. Changed size from 0201 to 0402 for 1 kOhm resistors R104 and R105. 20. Added 100 Ohm termination resistors R109 and R110 for MGT_REF_CLKs. 21. Changed VCCADC_0 supply from VCCIO_0 to PL_1.8V. 22. Added UKCA logo. 23. Changed voltage divider R21 and R22 to set threshold to 0.936 V. 24. Changed DDR clock termination resistor R9 placement position. 25. Changed fiducials to standard fiducial type. 26. Update revision history. 27. Update schematic template. 28. Updated power overview. 29. Removed page "ZYNQ.SchDoc" and added pages Legal Notices, System Overview.	ED

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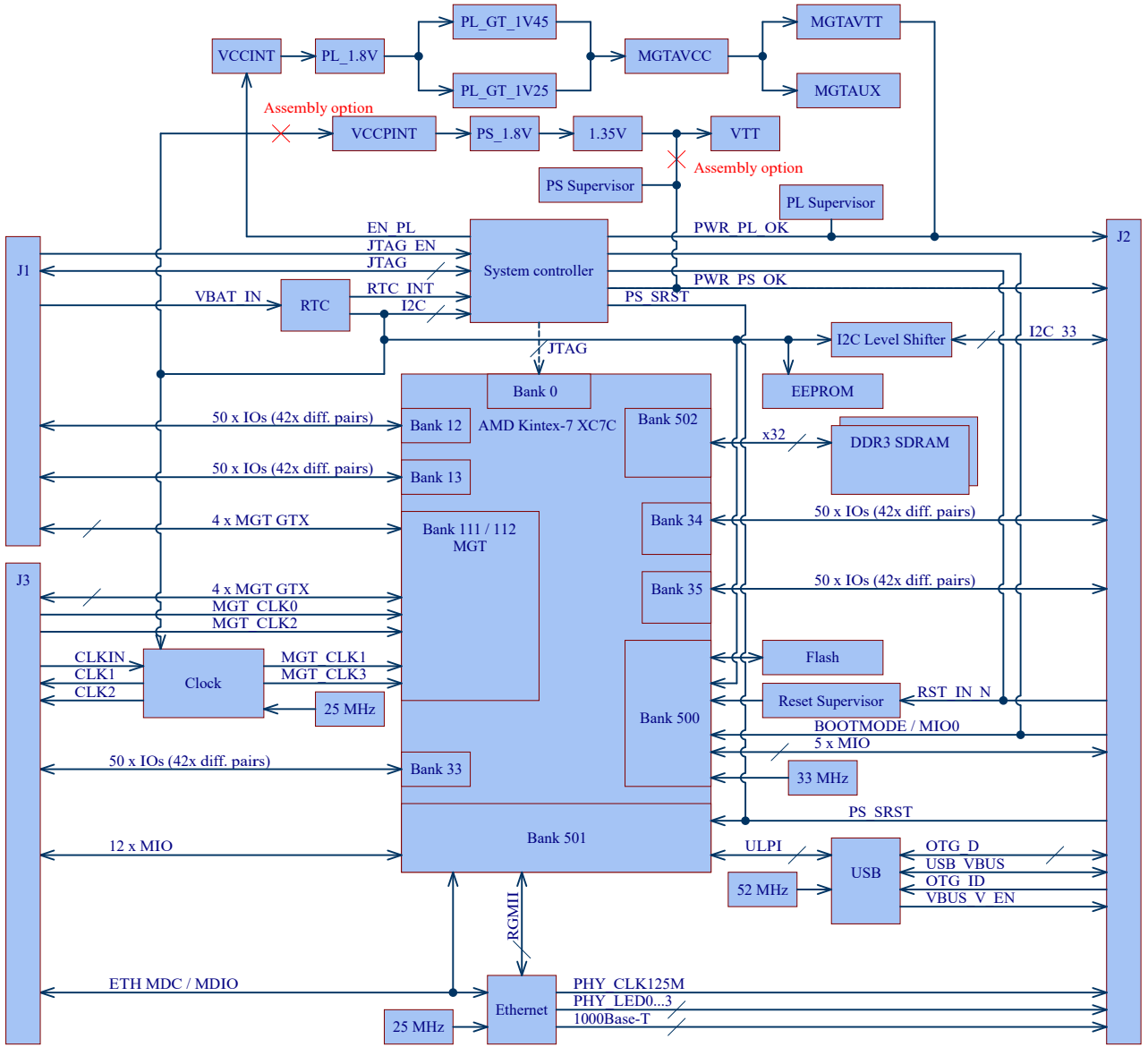
Title: TE0745 - Revision Changes		
A4	Number: TE0745 92I31-A	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH	Page 2 of 26
Filename: Revision Changes.SchDoc		

I2C Address:

Device	I2C ADDR	Note
SoC U1G	-	I2C Master
CPLD U2	0x30	Firmware dependent
DCDC U4	0x61	Assembly option
PLL U16	0x70	-
RTC U24	0x6F	RTC register
RTC U24	0x57	User SRAM
EEPROM U23	0x53	-

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
PS_3.3V	IN	3.3 V	+/- 5 %	Micromodule Power	-
PS_VIN	IN	3.3 V	+/- 5 %	Micromodule Power	-
PL_VIN	IN	3.2 V - 4.5 V	-	Micromodule Power	within given range
VCCIO_12	IN	1.2 V - 3.3 V	+/- 3 %	HR IO Bank 12	-
VCCIO_13	IN	1.2 V - 3.3 V	+/- 3 %	HR IO Bank 13	-
VCCIO_33	IN	1.2 V - 1.8 V	+/- 3 %	HP IO Bank 33	-
VCCIO_34	IN	1.2 V - 1.8 V	+/- 3 %	HP IO Bank 34	-
VCCIO_35	IN	1.2 V - 1.8 V	+/- 3 %	HP IO Bank 35	-
VBAT_IN	IN	1.8 V - 3.3 V	-	RTC	within given range
PS_1.8V	OUT	1.8 V	+/- 3 %	Power for Carrier	-
PL_1.8V	OUT	1.8 V	+/- 3 %	Power for Carrier	-



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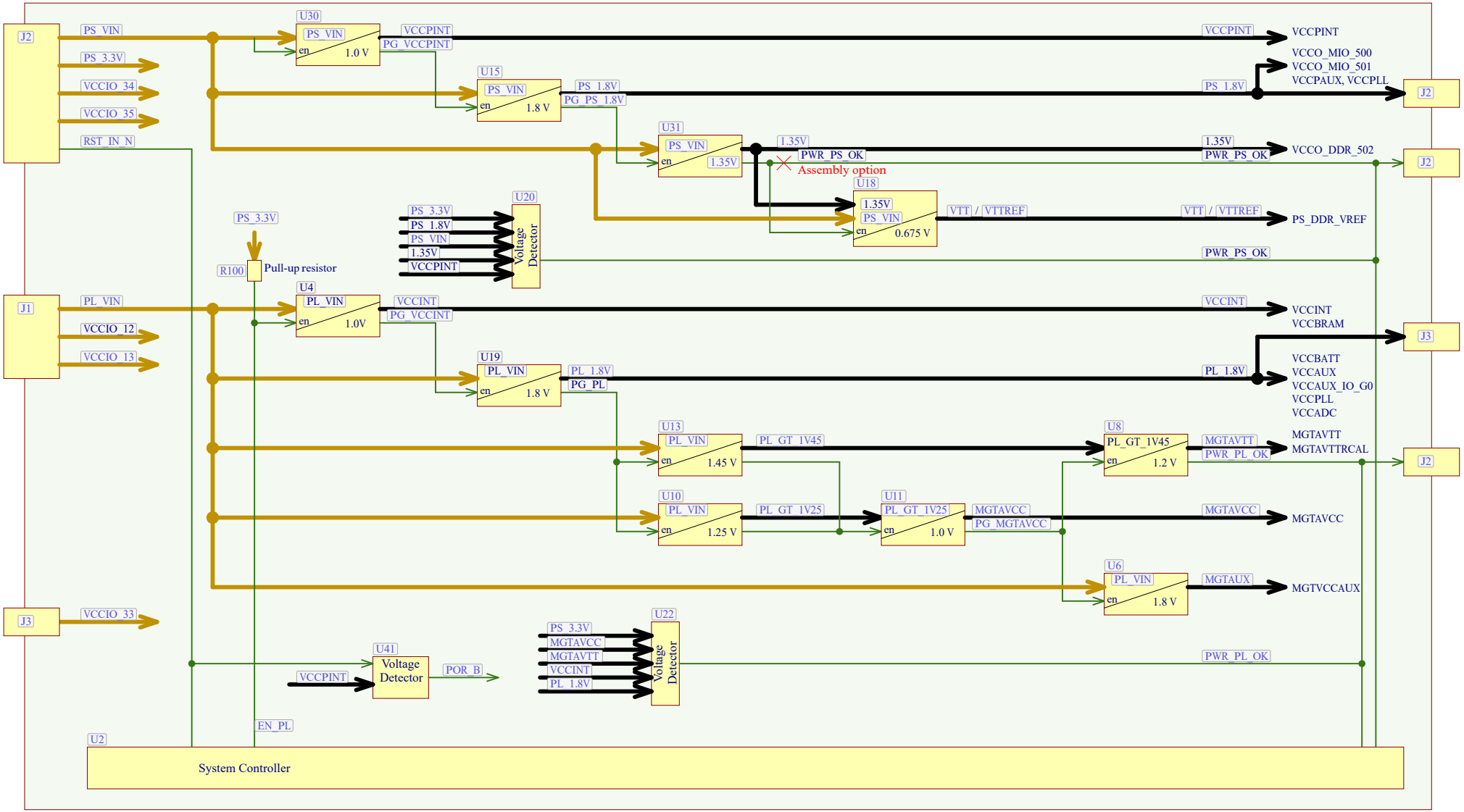
Title: TE0745 - System Overview			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 17.06.2025	Copyright: Trenz Electronic GmbH		Page 3 of 26
Filename: Overview.SchDoc			

Power-on sequencing:



trenz electronic	Title: TE0745 - Power overview	
A4	Number: TE0745 92I31-A	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH	Page 4 of 26
Filename: PowerOverview.SchDoc		

Special notes:

UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

LOGO1

TE Logo PRINT Layer

LOGO PRINT

FIDU-DOT - small PM1

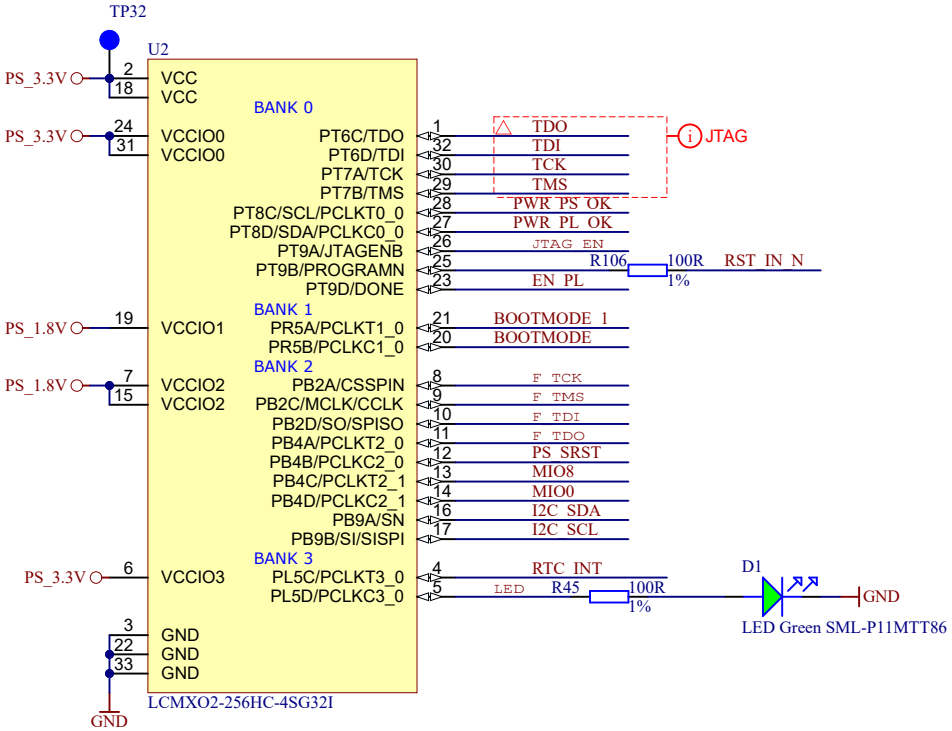
FIDU-DOT - small PM2

FIDU-DOT - small PM3

FIDU-DOT - small PM4

FIDU-DOT - small PM5

FIDU-DOT - small PM6



Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

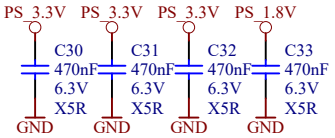
Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe

Mount.Hole 3.2mm für Unterlegscheibe



Serial

Serial

Serialnumber 6,3 x 6.3mm

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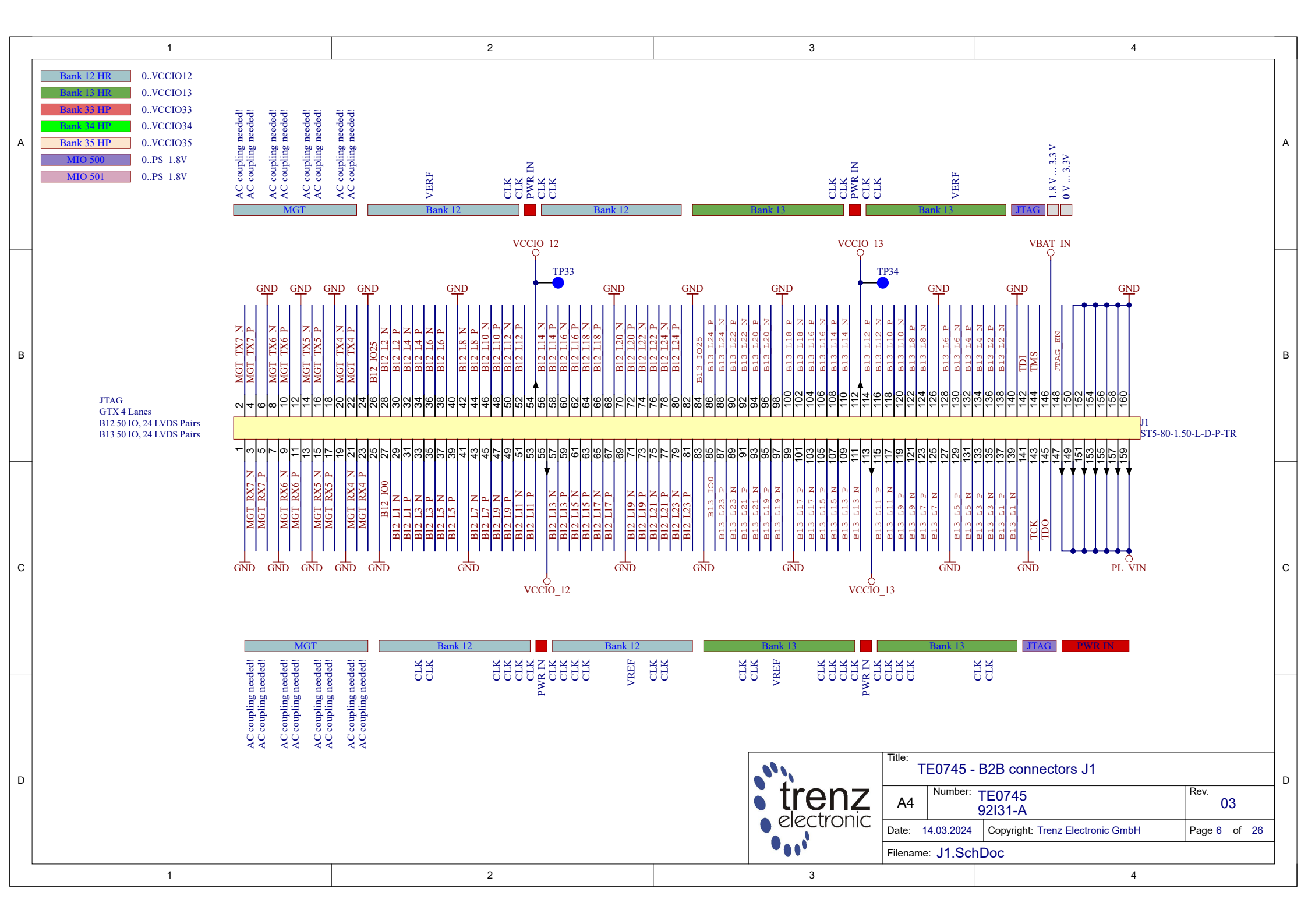
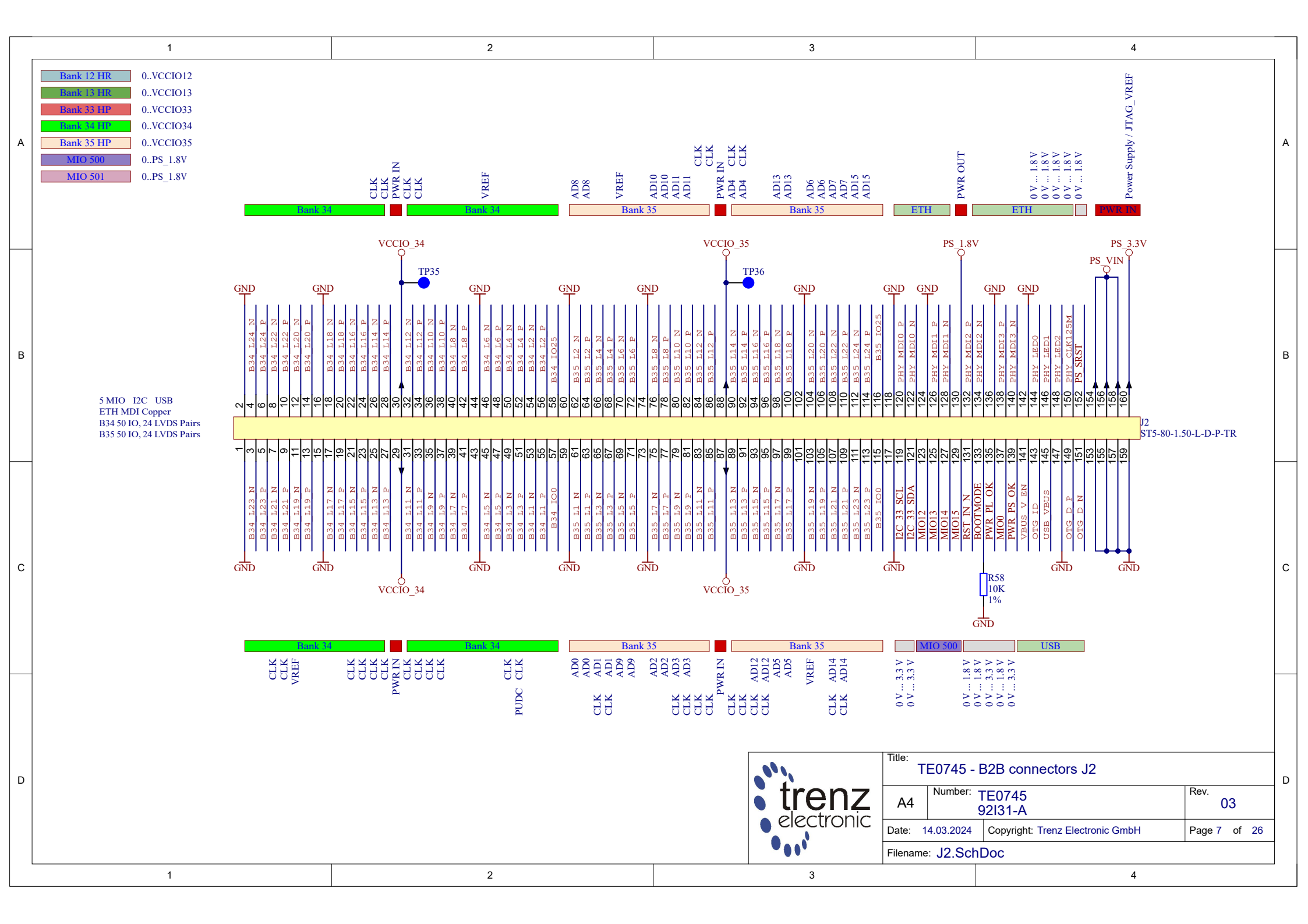
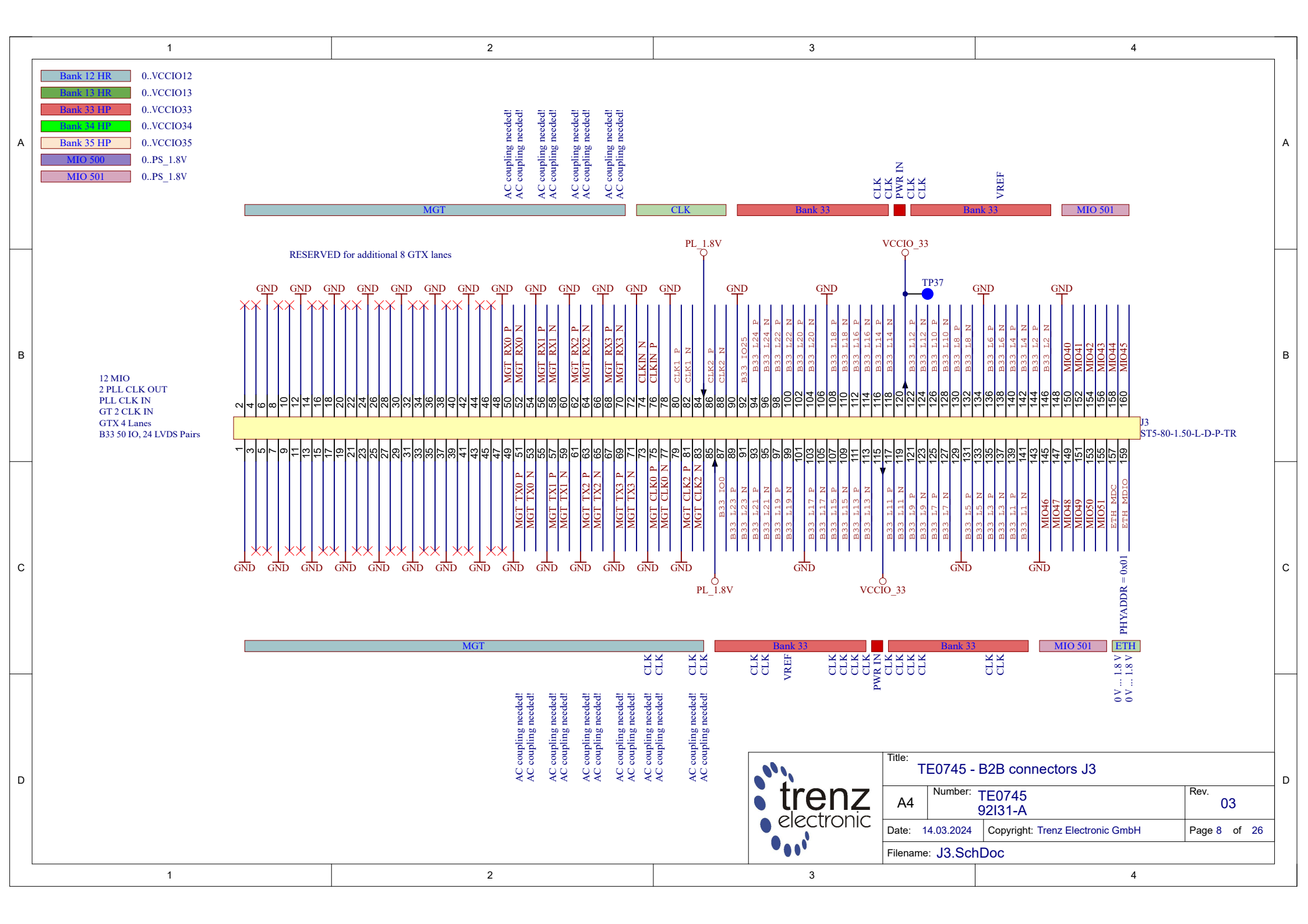
Title: TE0745 - System Controller		
A4	Number: TE0745 92I31-A	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH	Page 5 of 26
Filename: TE0745.SchDoc		



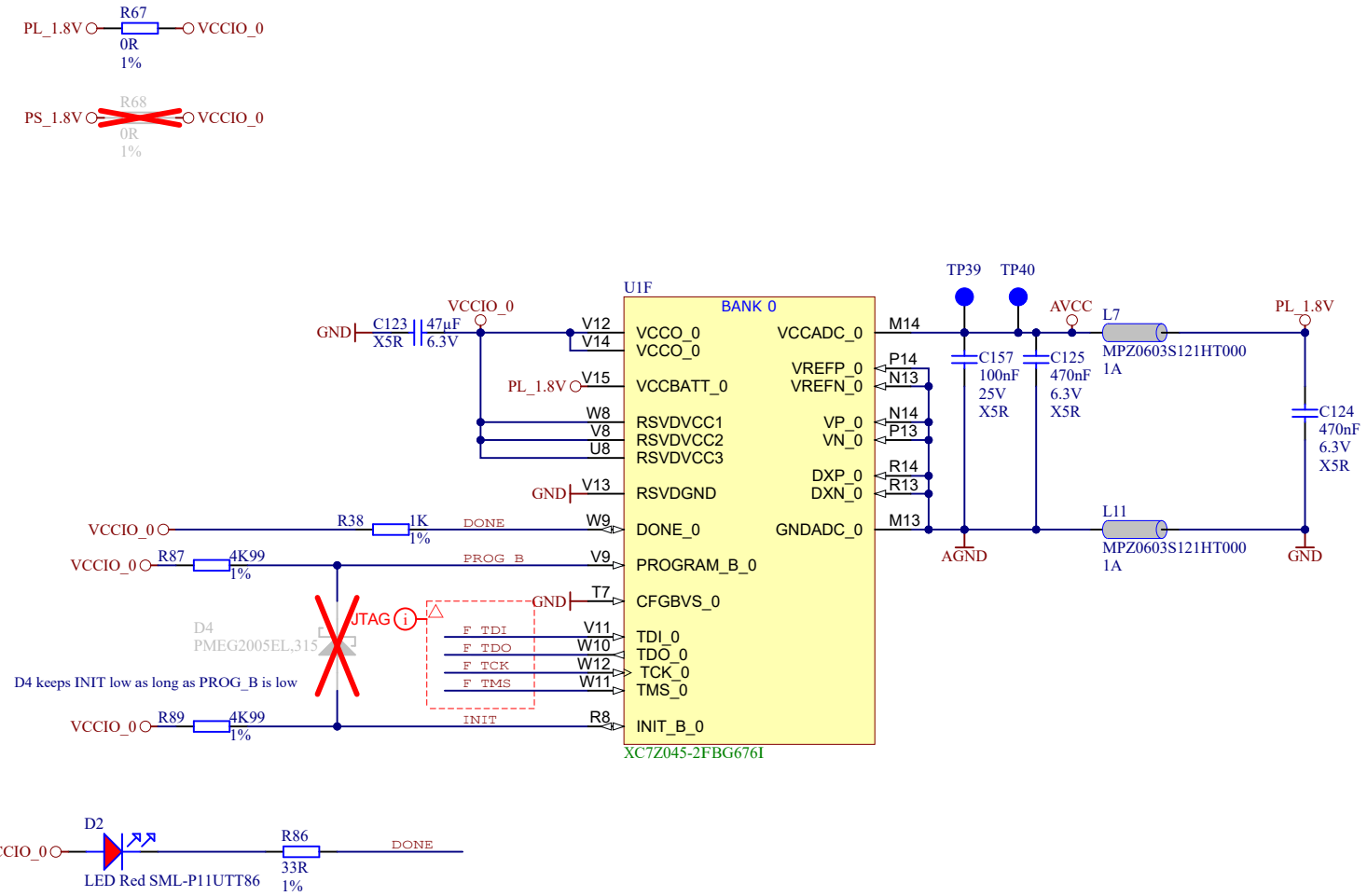
Title:	TE0745 - B2B connectors J1
A4	Number: TE0745 92I31-A
	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH
	Page 6 of 26
Filename: J1.SchDoc	



Title: TE0745 - B2B connectors J2			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 7 of 26
Filename: J2.SchDoc			



Title: TE0745 - B2B connectors J3			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 8 of 26
Filename: J3.SchDoc			



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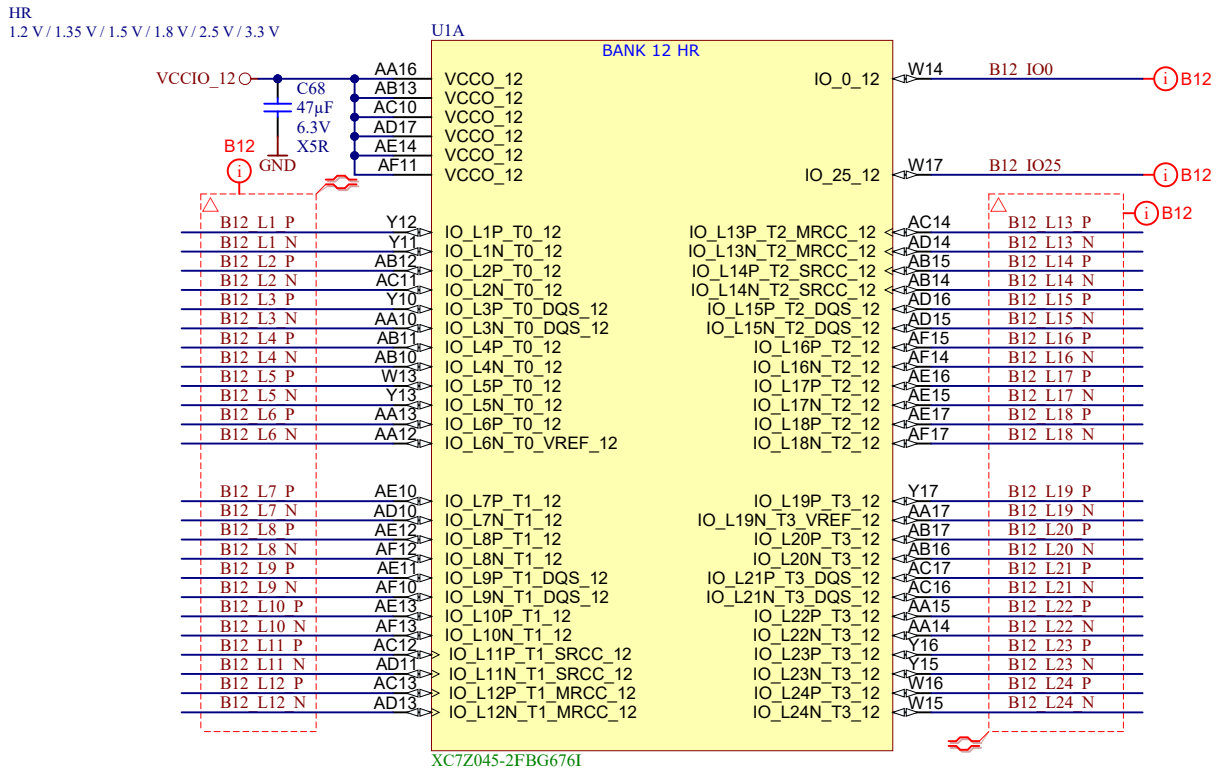
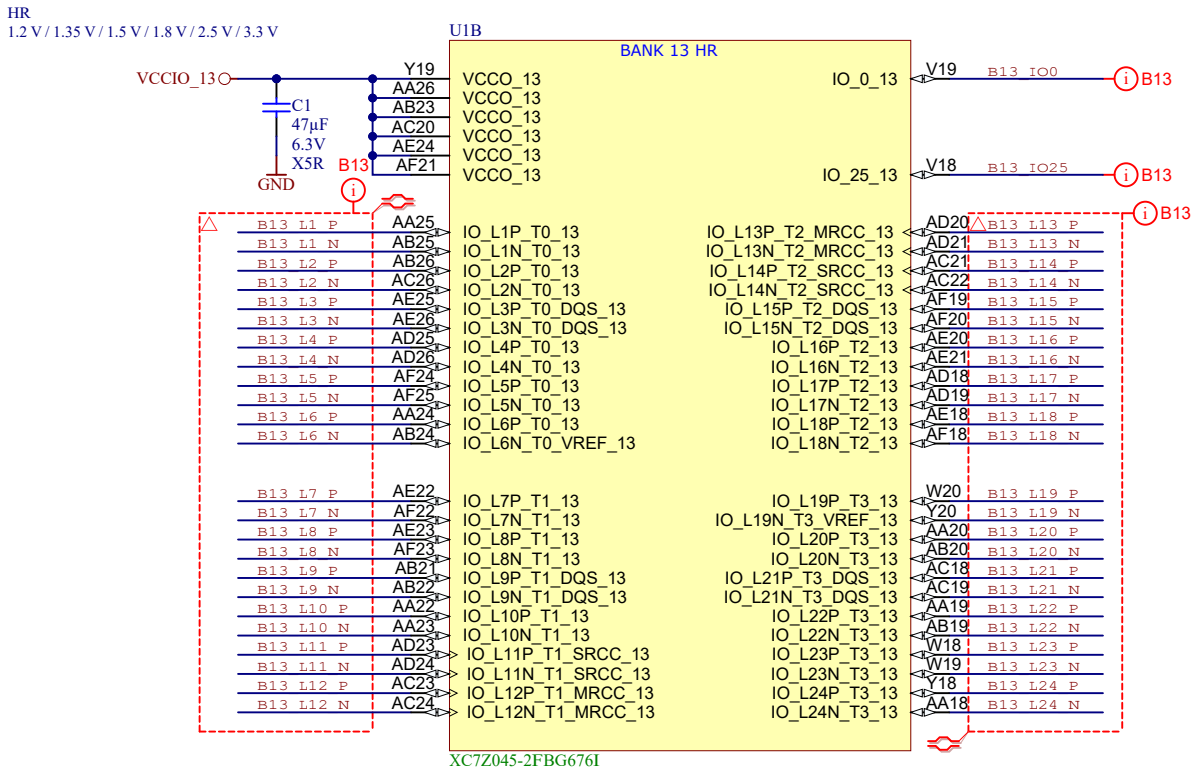
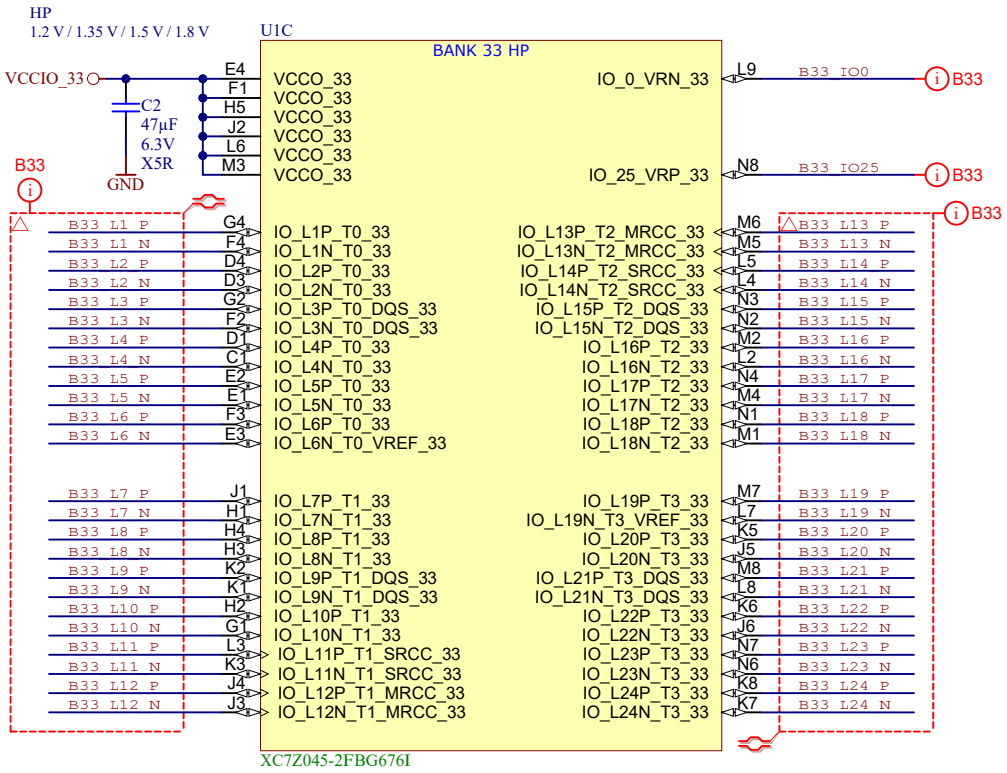
Title: TE0745 - Zynq_MISC			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 9 of 26
Filename: ZYNQ_MISC.SchDoc			



trenz electronic	Title: TE0745 - Zynq_B12		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 10 of 26
Filename: B12.SchDoc			



trenz electronic	Title: TE0745 - Zynq_B13		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 11 of 26
Filename: B13.SchDoc			



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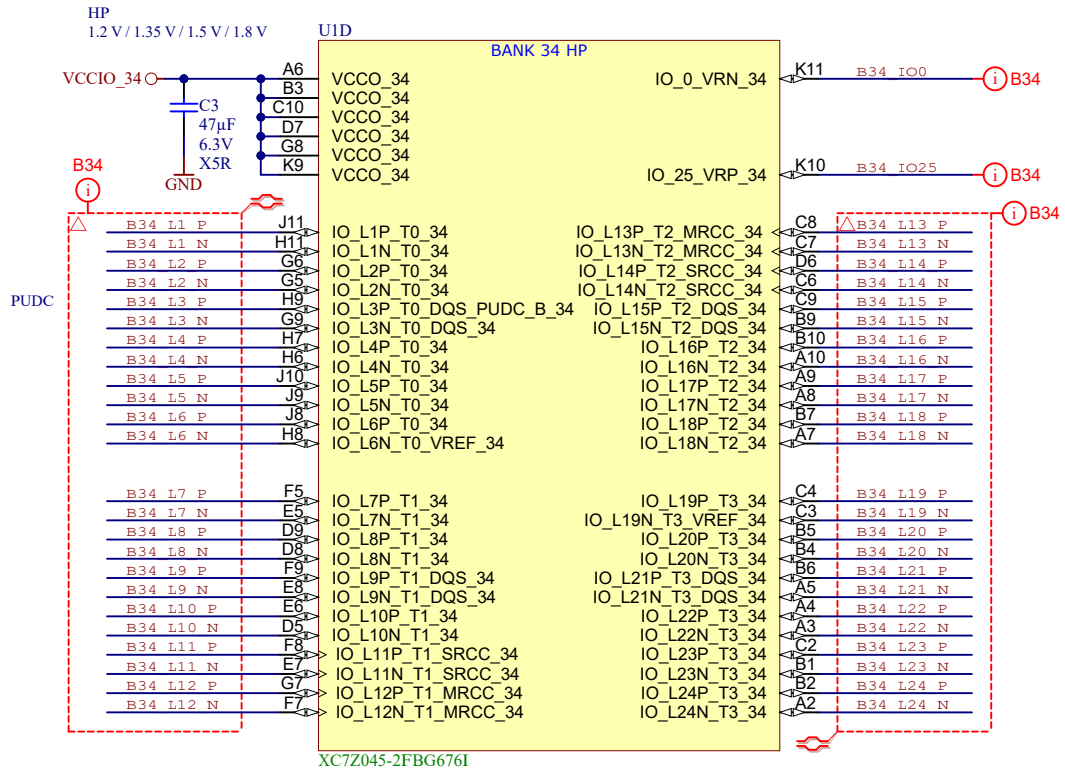
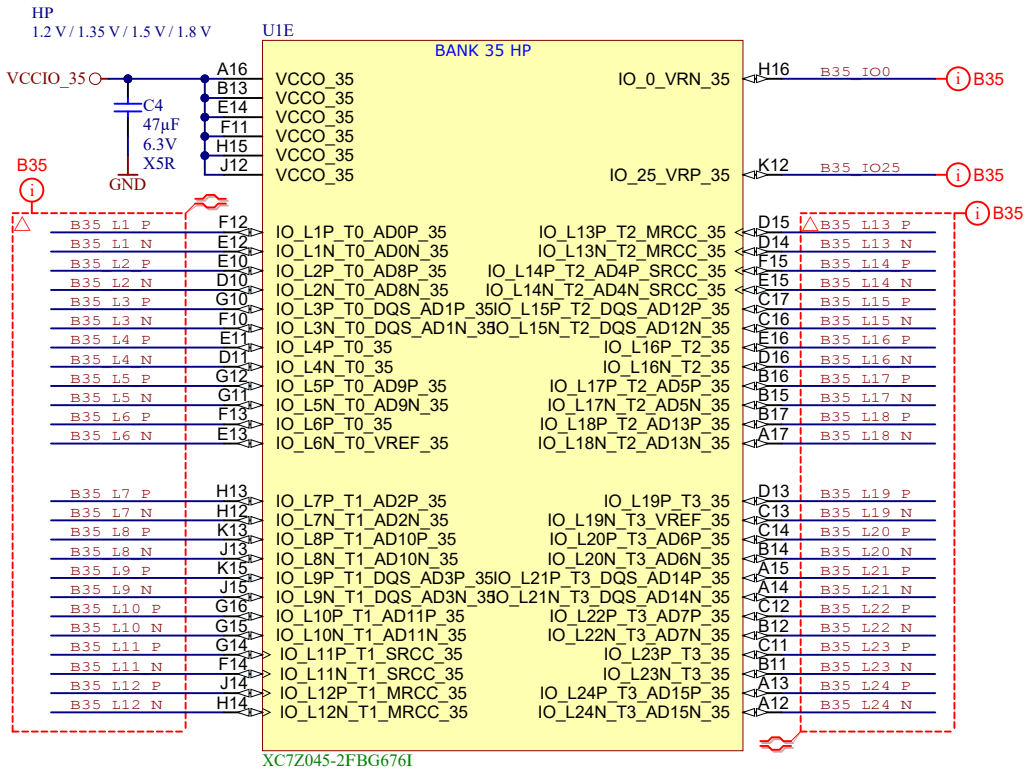
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 12 of 26
Filename: B33.SchDoc			



Title: TE0745 - Zynq_B34			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 13 of 26
Filename: B34.SchDoc			



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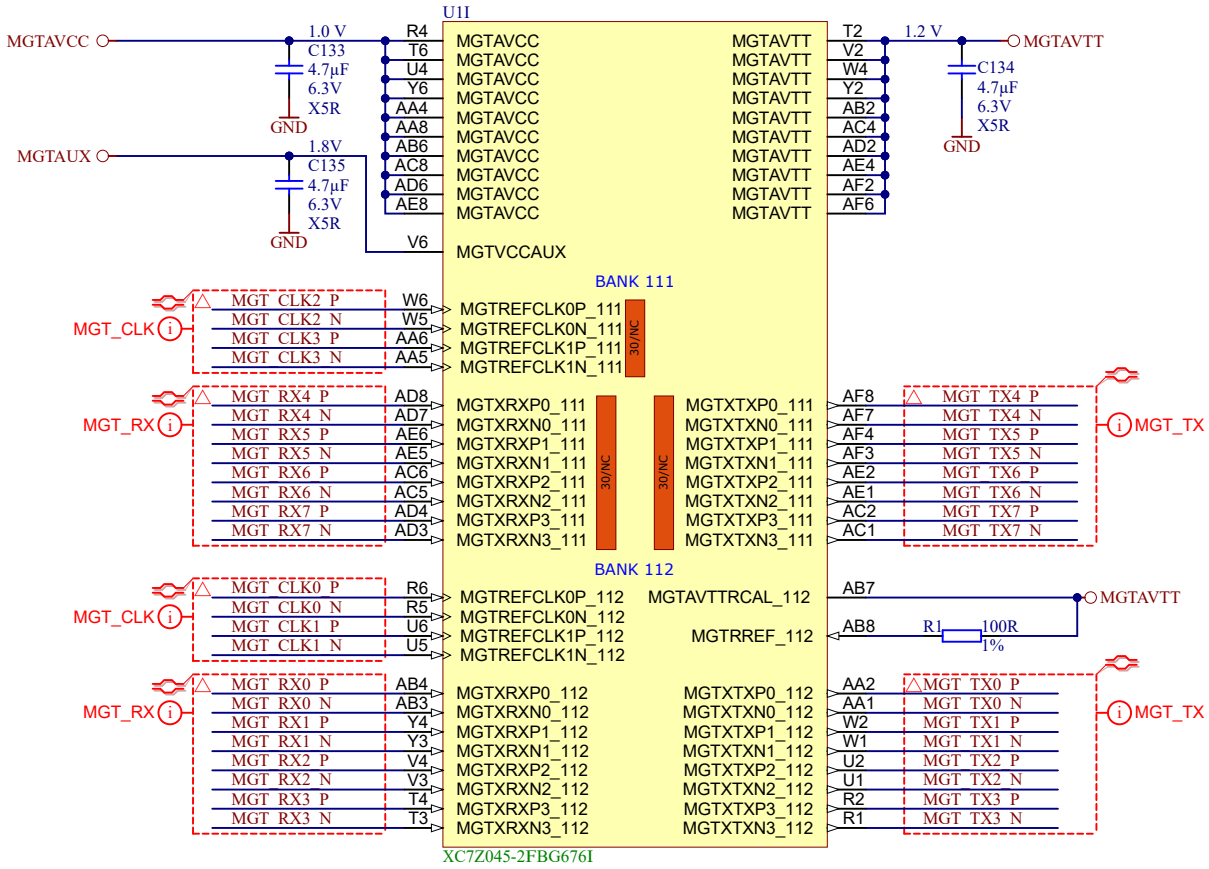
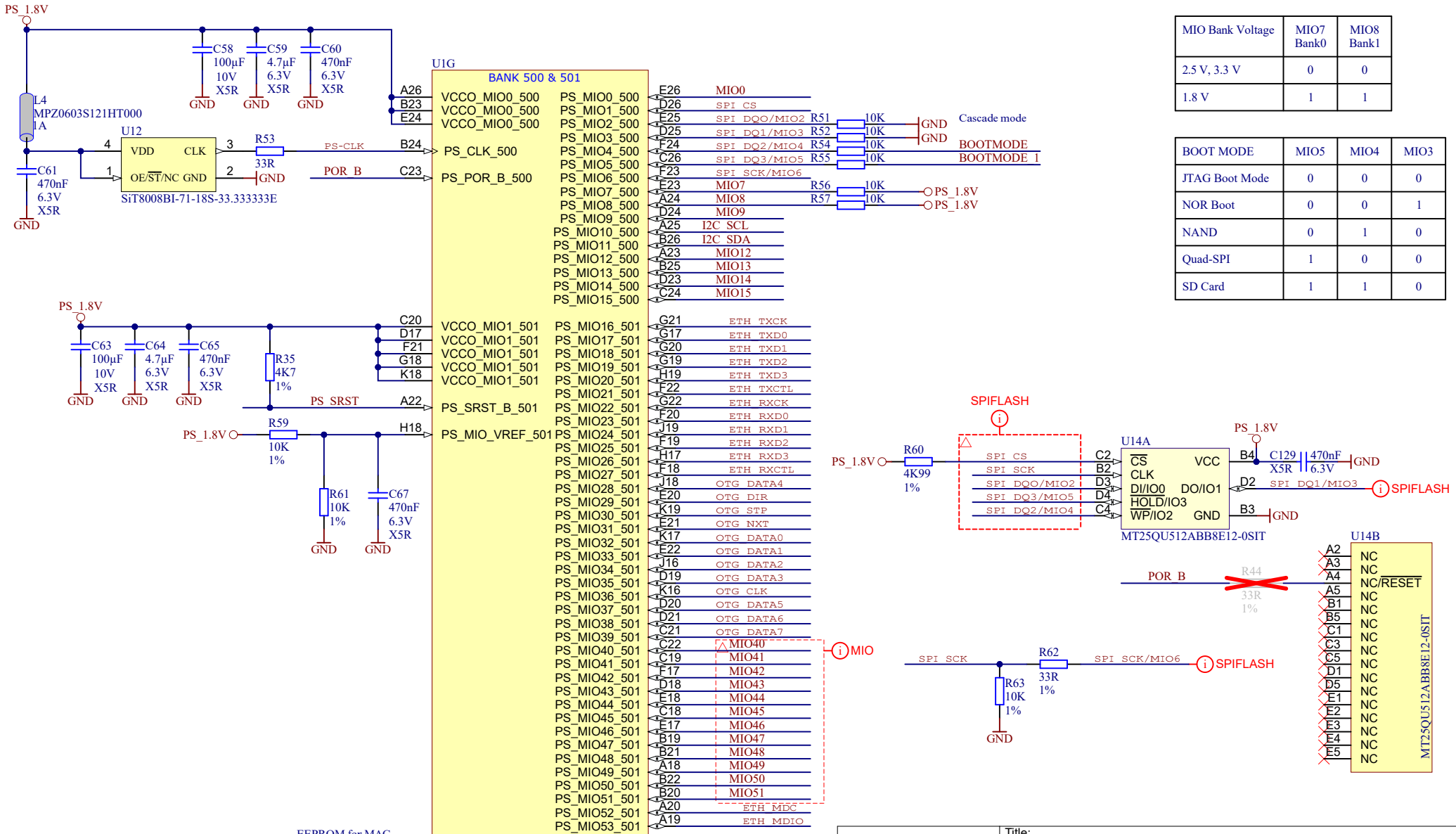
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 14 of 26
Filename: B35.SchDoc			



trenz electronic	Title: TE0745 - Zynq_MGT		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 15 of 26
Filename: FPGA_MGT.SchDoc			



MIO Bank Voltage	MIO7 Bank0	MIO8 Bank1
2.5 V, 3.3 V	0	0
1.8 V	1	1

BOOT MODE	MIO5	MIO4	MIO3
JTAG Boot Mode	0	0	0
NOR Boot	0	0	1
NAND	0	1	0
Quad-SPI	1	0	0
SD Card	1	1	0

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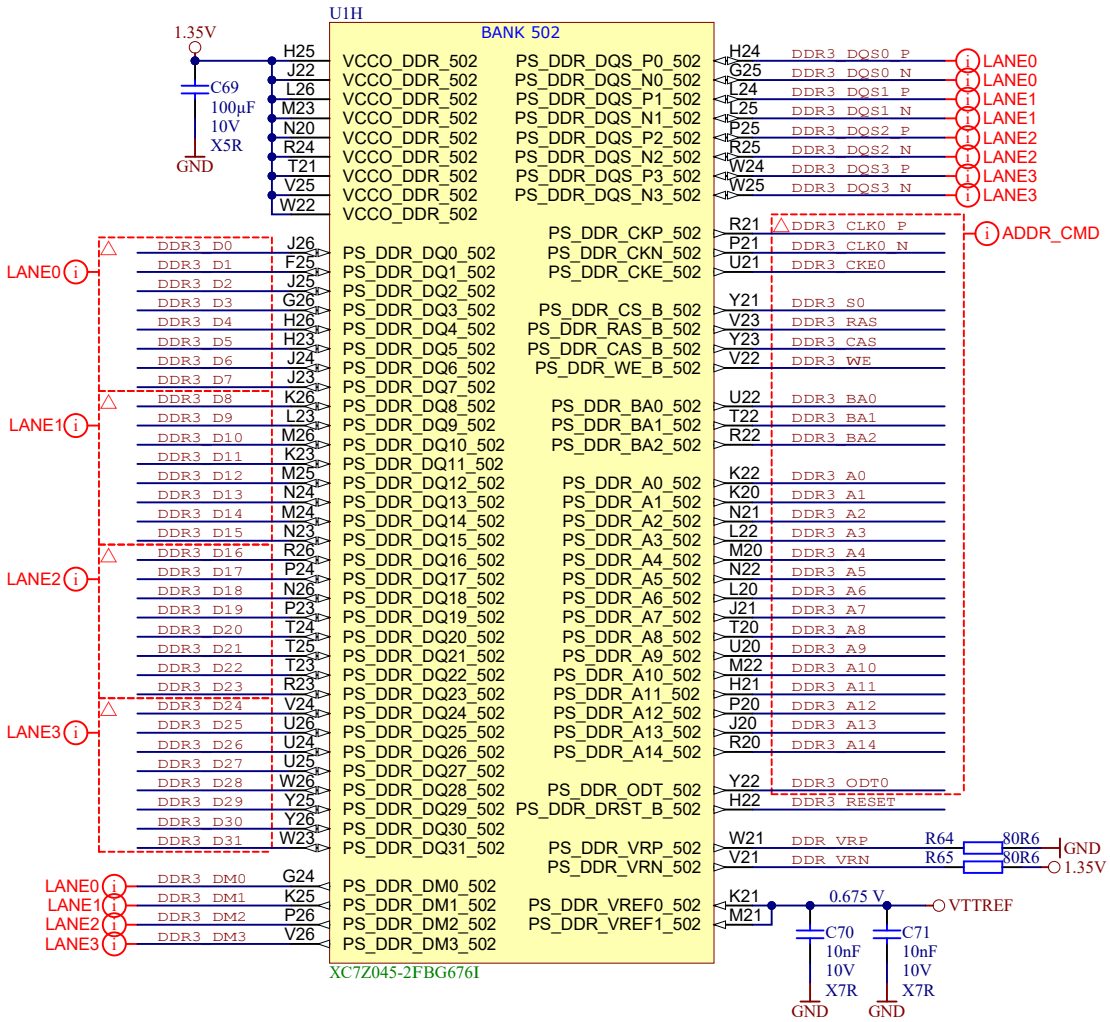
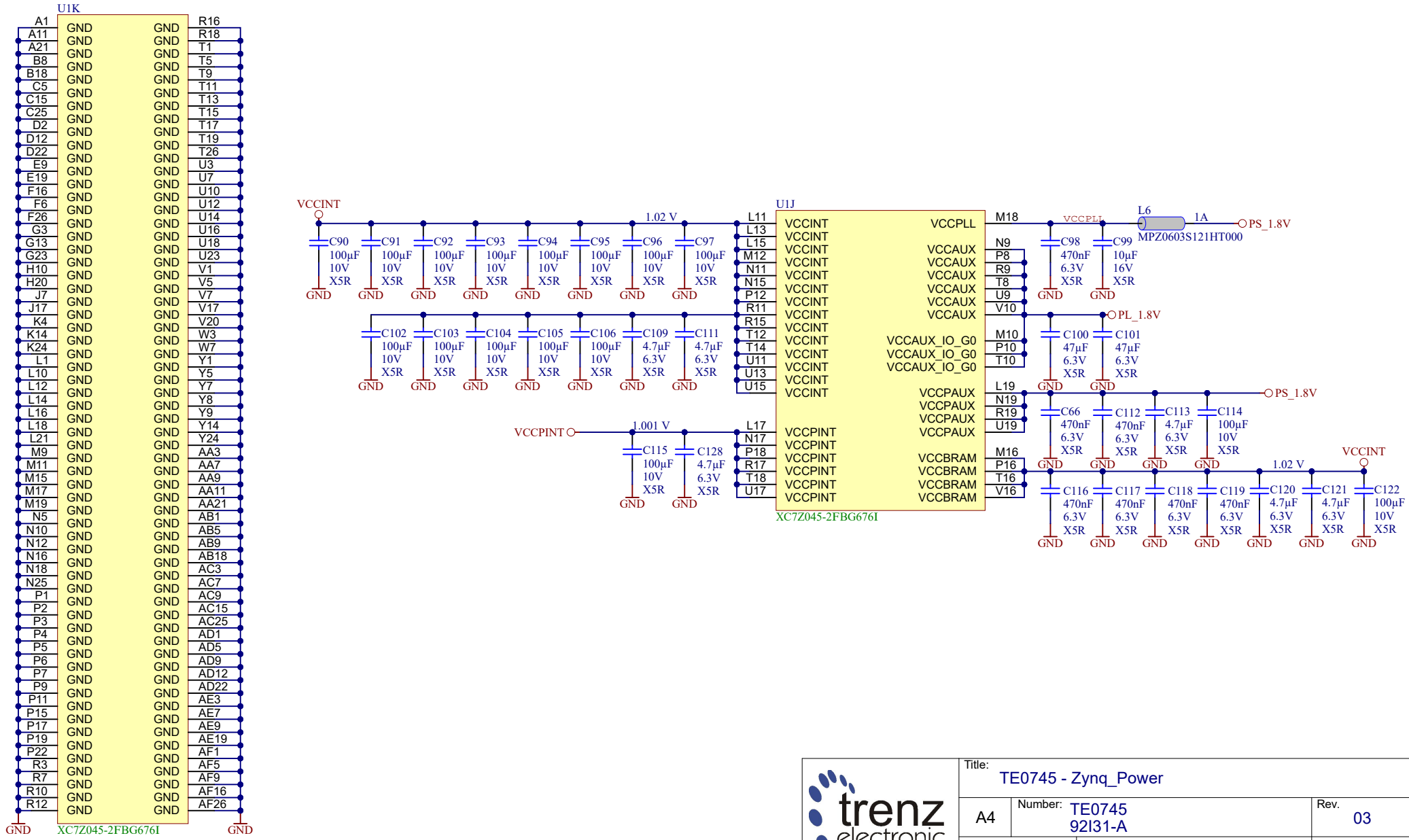
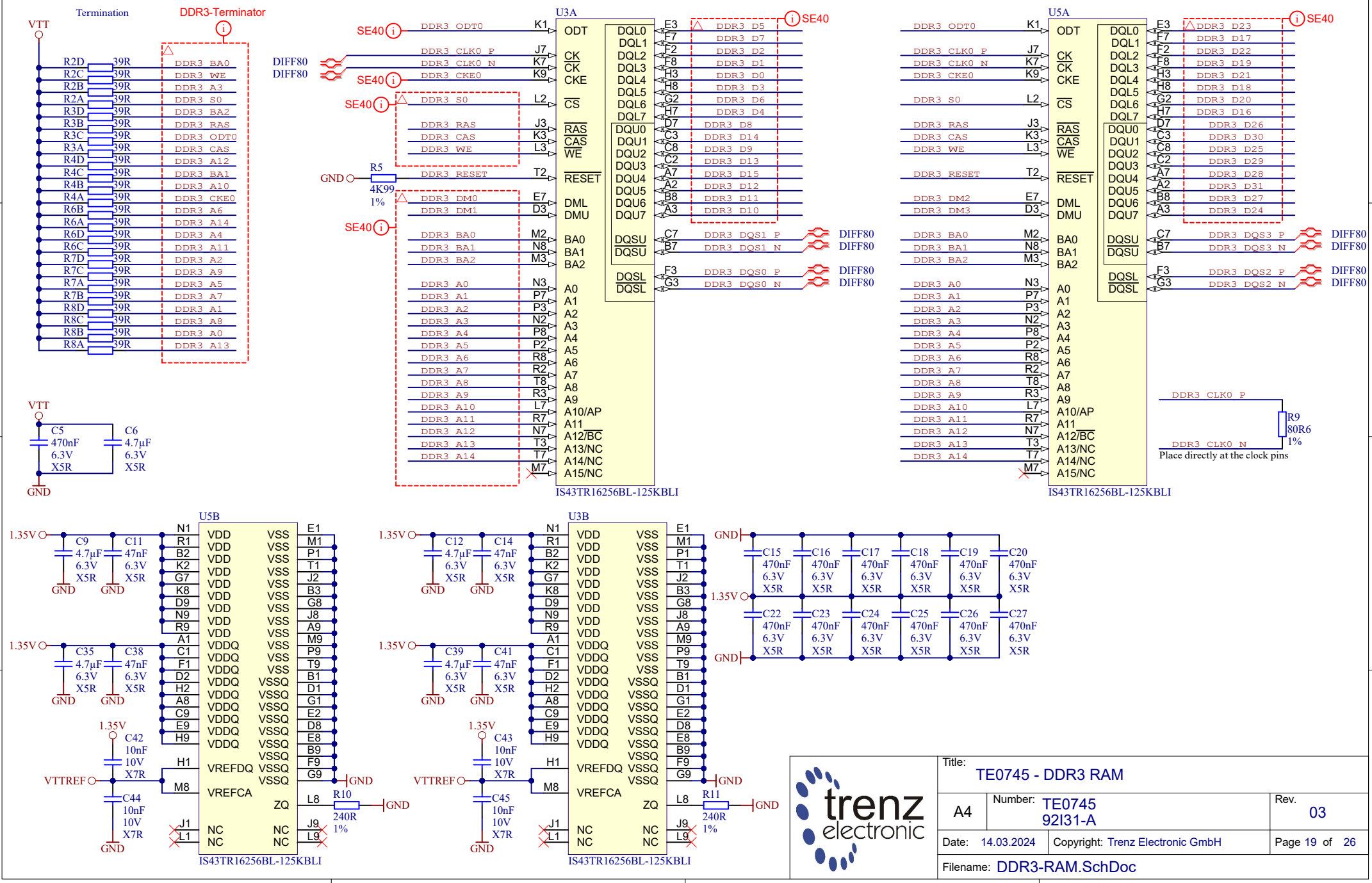
Title: TE0745 - Zynq_MIO_Banks		
A4	Number: TE0745 92I31-A	Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH	Page 16 of 26
Filename: MIO_B500.SchDoc		



trenz electronic	Title: TE0745 - Zynq_PS_DDR		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 17 of 26
Filename: PS-DDR.SchDoc			



Title: TE0745 - Zynq_Power			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 18 of 26
Filename: ZYNC_POWER.SchDoc			


Termination
DDR3-Terminator
VTT
R2D 39R DDR3_BA0
R2C 39R DDR3_WE
R2B 39R DDR3_A3
R2A 39R DDR3_S0
R3D 39R DDR3_BA2
R3B 39R DDR3_RAS
R3C 39R DDR3_ODT0
R3A 39R DDR3_CAS
R4D 39R DDR3_A12
R4C 39R DDR3_BA1
R4B 39R DDR3_A10
R4A 39R DDR3_CKE0
R6B 39R DDR3_A6
R6A 39R DDR3_A14
R6D 39R DDR3_A4
R6C 39R DDR3_A11
R7D 39R DDR3_A2
R7C 39R DDR3_A9
R7A 39R DDR3_A5
R7B 39R DDR3_A7
R8D 39R DDR3_A1
R8C 39R DDR3_A8
R8B 39R DDR3_A0
R8A 39R DDR3_A13
VTT
C5 470nF 6.3V X5R
C6 4.7µF 6.3V X5R
GND
U3A
SE40
DDR3_ODT0 K1 ODT
DIFF80 DDR3_CLK0_P J7 CK
DIFF80 DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
R5 4K99 1%
DDR3_RESET T2 RESET
DDR3_DM0 E7 DML
DDR3_DM1 D3 DMU
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13/NC
DDR3_A14 T7 A14/NC
M7 A15/NC
DQL0 E3 DDR3_D5
DQL1 F7 DDR3_D7
DQL2 F2 DDR3_D2
DQL3 F8 DDR3_D1
DQL4 H3 DDR3_D0
DQL5 H8 DDR3_D3
DQL6 G2 DDR3_D6
DQL7 H7 DDR3_D4
DQU0 D7 DDR3_D8
DQU1 C3 DDR3_D14
DQU2 C8 DDR3_D9
DQU3 C2 DDR3_D13
DQU4 A7 DDR3_D15
DQU5 A2 DDR3_D12
DQU6 B8 DDR3_D11
DQU7 A3 DDR3_D10
DQSU C7 DDR3_DQS1_P DIFF80
DQSU B7 DDR3_DQS1_N DIFF80
DQSL F3 DDR3_DQS0_P DIFF80
DQSL G3 DDR3_DQS0_N DIFF80
IS43TR16256BL-125KBLI
U5A
DDR3_ODT0 K1 ODT
DDR3_CLK0_P J7 CK
DDR3_CLK0_N K7 CK
DDR3_CKE0 K9 CKE
DDR3_S0 L2 CS
DDR3_RAS J3 RAS
DDR3_CAS K3 CAS
DDR3_WE L3 WE
DDR3_RESET T2 RESET
DDR3_DM2 E7 DML
DDR3_DM3 D3 DMU
DDR3_BA0 M2 BA0
DDR3_BA1 N8 BA1
DDR3_BA2 M3 BA2
DDR3_A0 N3 A0
DDR3_A1 P7 A1
DDR3_A2 P3 A2
DDR3_A3 N2 A3
DDR3_A4 P8 A4
DDR3_A5 P2 A5
DDR3_A6 R8 A6
DDR3_A7 R2 A7
DDR3_A8 T8 A8
DDR3_A9 R3 A9
DDR3_A10 L7 A10/AP
DDR3_A11 R7 A11
DDR3_A12 N7 A12/BC
DDR3_A13 T3 A13/NC
DDR3_A14 T7 A14/NC
M7 A15/NC
DQL0 E3 DDR3_D23
DQL1 F7 DDR3_D17
DQL2 F2 DDR3_D22
DQL3 F8 DDR3_D19
DQL4 H3 DDR3_D21
DQL5 H8 DDR3_D18
DQL6 G2 DDR3_D20
DQL7 H7 DDR3_D16
DQU0 D7 DDR3_D26
DQU1 C3 DDR3_D30
DQU2 C8 DDR3_D25
DQU3 C2 DDR3_D29
DQU4 A7 DDR3_D28
DQU5 A2 DDR3_D31
DQU6 B8 DDR3_D27
DQU7 A3 DDR3_D24
DQSU C7 DDR3_DQS3_P DIFF80
DQSU B7 DDR3_DQS3_N DIFF80
DQSL F3 DDR3_DQS2_P DIFF80
DQSL G3 DDR3_DQS2_N DIFF80
IS43TR16256BL-125KBLI
DDR3_CLK0_P
R9 80R6 1%
DDR3_CLK0_N
Place directly at the clock pins
U5B
1.35V
C9 4.7µF 6.3V X5R
C11 47nF 6.3V X5R
C35 4.7µF 6.3V X5R
C38 47nF 6.3V X5R
C42 10nF 10V X7R
C44 10nF 10V X7R
VTTREF
GND
N1 R1 B2 K2 G7 K8 D9 N9 R9 VDD
A1 C1 F1 D2 H2 A8 C9 E9 H9 VDDQ
H1 VREFDQ
M8 VREFCA
J1 L1 NC
VSS E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9 B1 D1 G1 E2 D8 E8 B9 F9 G9
VSSQ
ZQ L8
R10 240R 1%
IS43TR16256BL-125KBLI
U3B
C12 4.7µF 6.3V X5R
C14 47nF 6.3V X5R
C39 4.7µF 6.3V X5R
C41 47nF 6.3V X5R
C43 10nF 10V X7R
C45 10nF 10V X7R
C15 C16 C17 C18 C19 C20 470nF 6.3V X5R
C22 C23 C24 C25 C26 C27 470nF 6.3V X5R
R11 240R 1%
IS43TR16256BL-125KBLI
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Title: TE0745 - DDR3 RAM
A4
Number: TE0745 92I31-A
Rev. 03
Date: 14.03.2024
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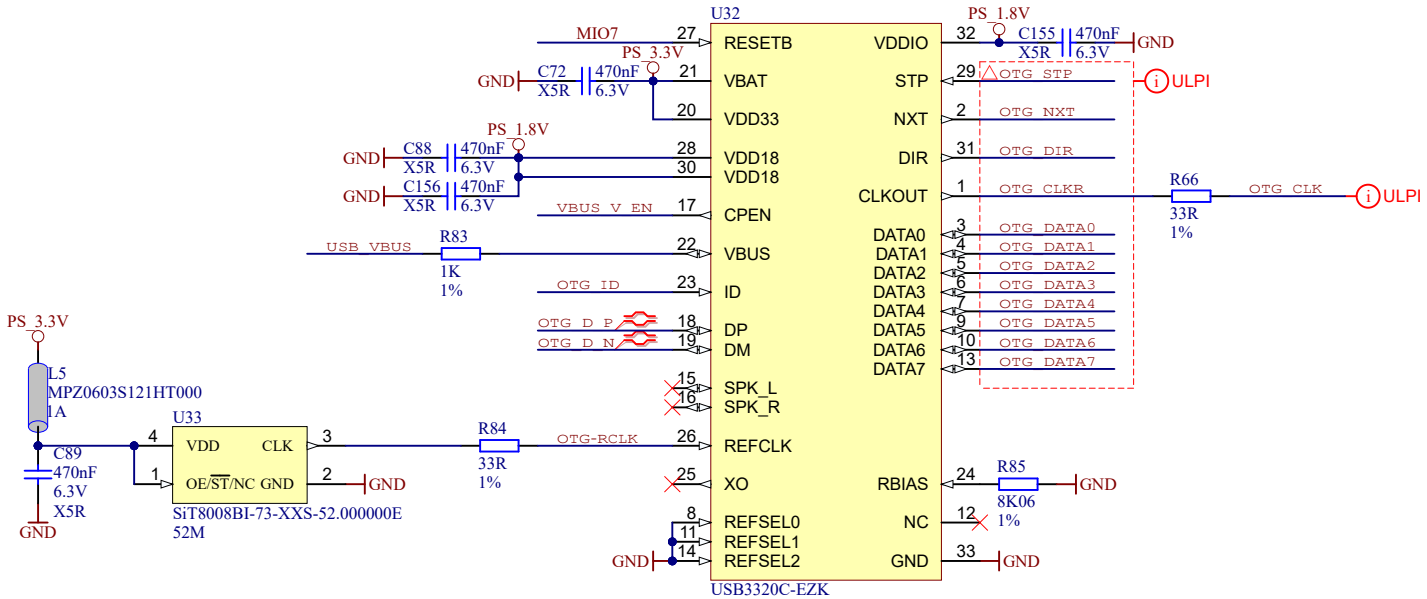
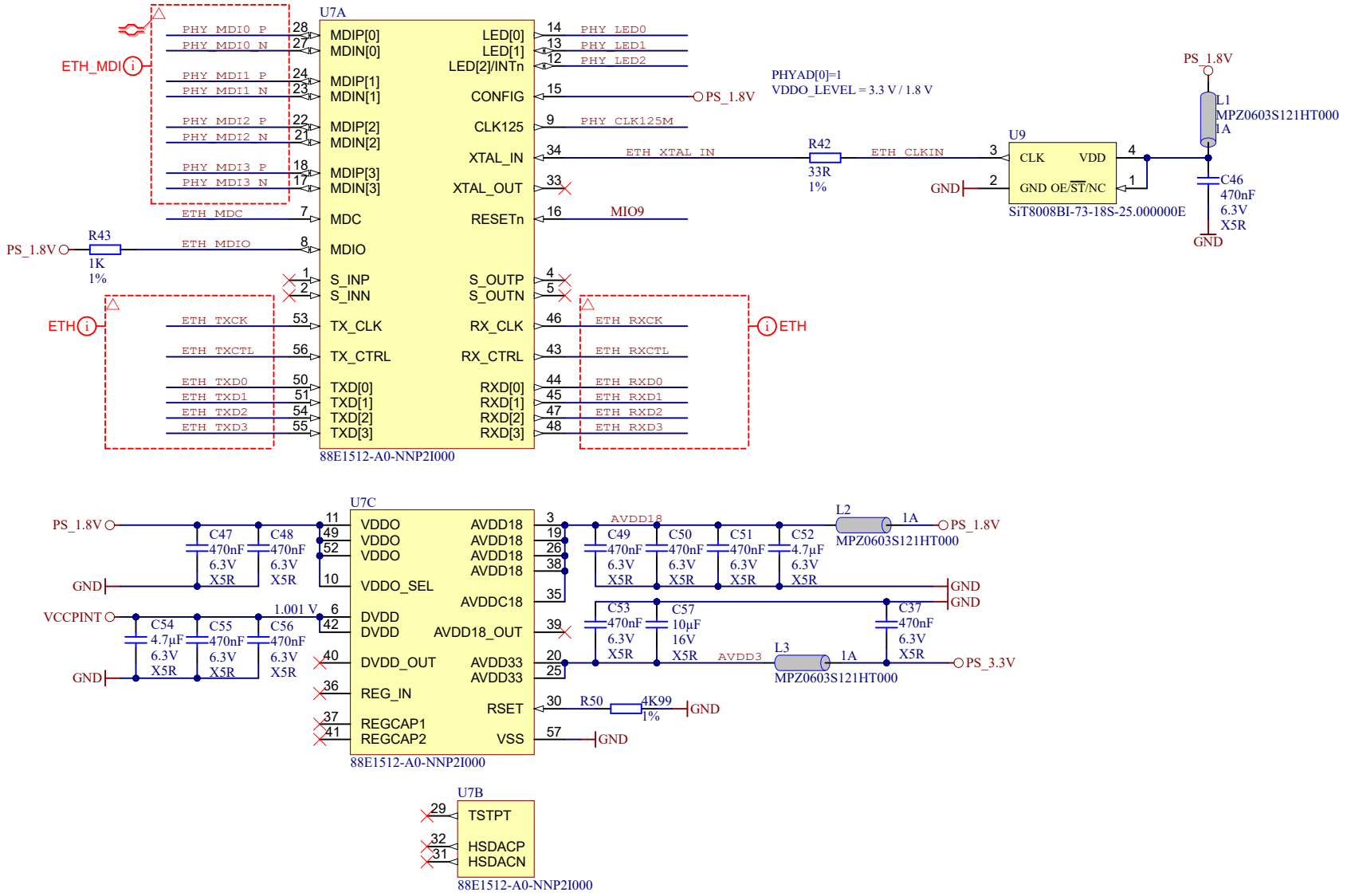
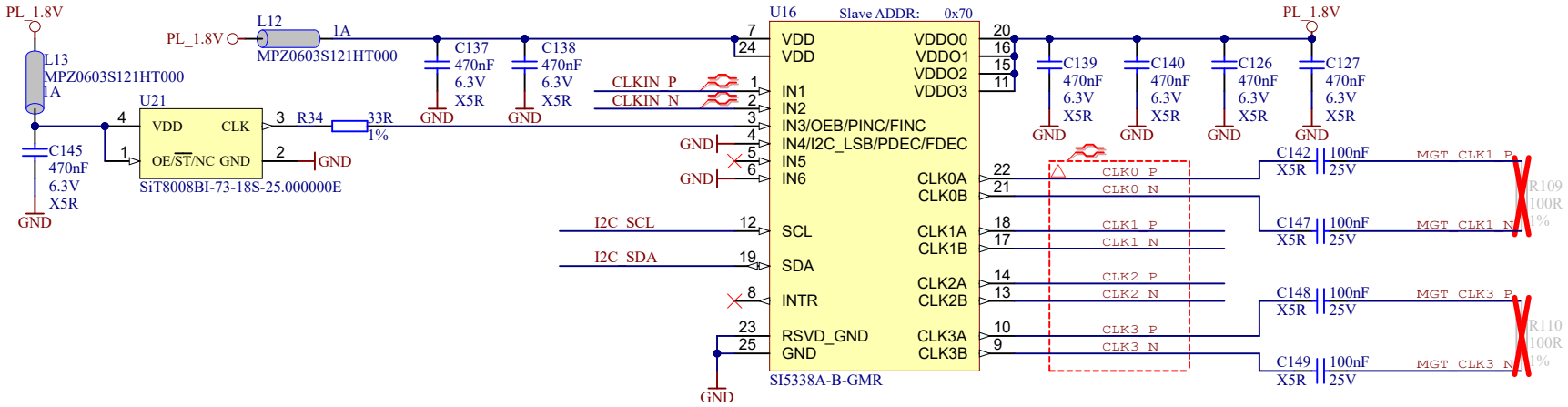
Page 19 of 26
Filename: DDR3-RAM.SchDoc



Title: TE0745 - USB_PHY			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 20 of 26
Filename: USB-PHY.SchDoc			



	Title: TE0745 - ETH_PHY		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 21 of 26
Filename: ETH-PHY.SchDoc			

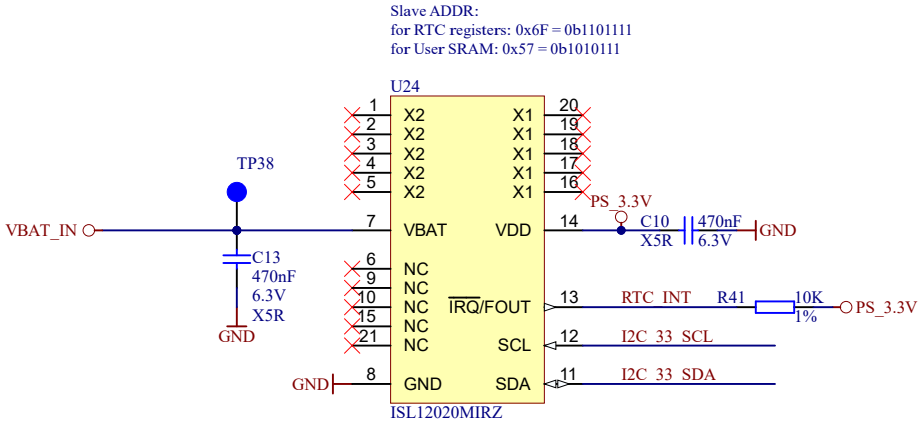


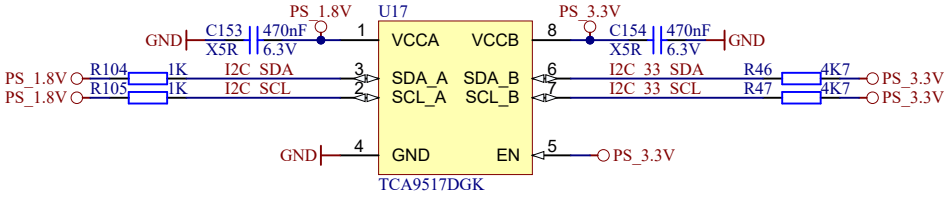
Datasheet Si5338:

IN1/IN2

These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.
When not in use, leave IN1 unconnected and IN2 connected to GND.

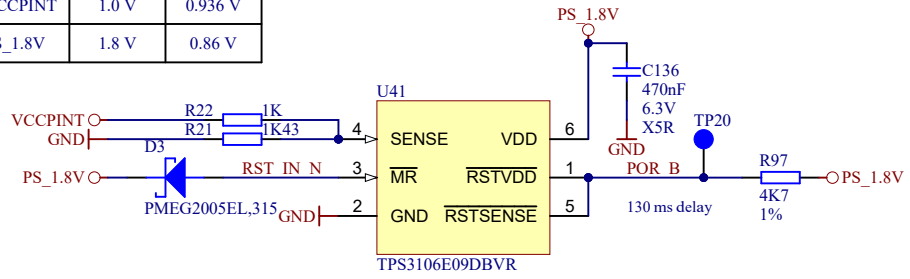
trenz electronic	Title: TE0745 - CLK		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 22 of 26
Filename: CLK.SchDoc			

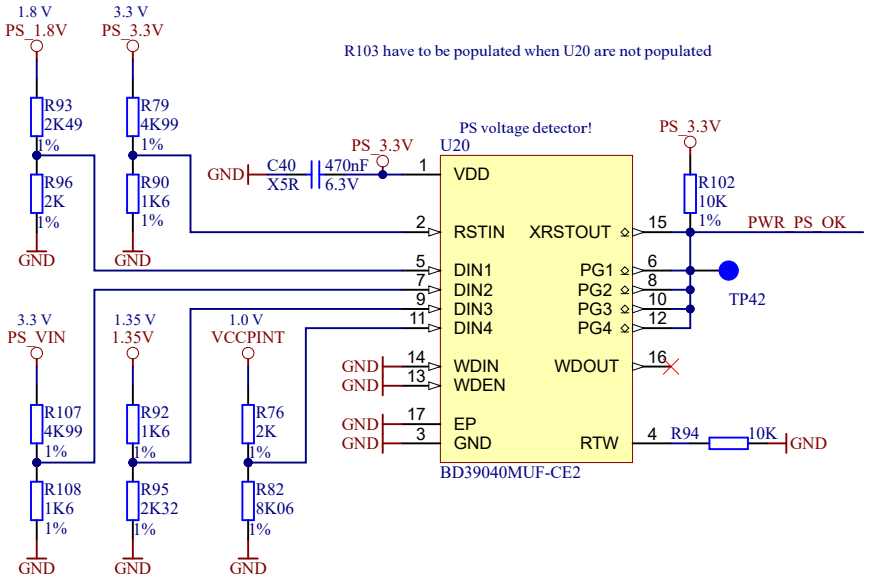


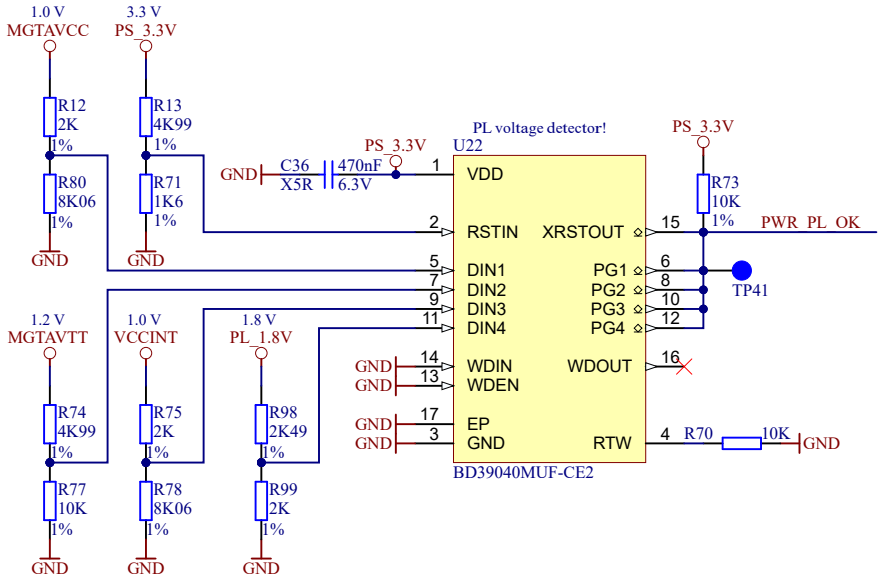


	Title: TE0745 - RTC		
A4	Number: TE0745 92I31-A		Rev. 03
Date: 17.06.2025	Copyright: Trenz Electronic GmbH		Page 23 of 26
Filename: SENSOR-RTC.SchDoc			

Net Name	Voltage Rail	Low Detect
VCCPINT	1.0 V	0.936 V
PS_1.8V	1.8 V	0.86 V







Net Name	Voltage Rail	Low Detect	High Detect
PS_3.3V	3.3 V	2.97 V	3.62 V
PS_1.8V	1.8 V	1.62 V	1.98 V
PS_VIN	3.3 V	2.97 V	3.62 V
1.35V	1.35 V	1.22 V	1.49 V
VCCPINT	1.0 V	0.90 V	1.10 V

Net Name	Voltage Rail	Low Detect	High Detect
PS_3.3V	3.3 V	2.97 V	3.62 V
MGTAVCC	1.0 V	0.90 V	1.10 V
MGTAVTT	1.2 V	1.08 V	1.32 V
VCCINT	1.0 V	0.90 V	1.10 V
PL_1.8V	1.8 V	1.62 V	1.98 V

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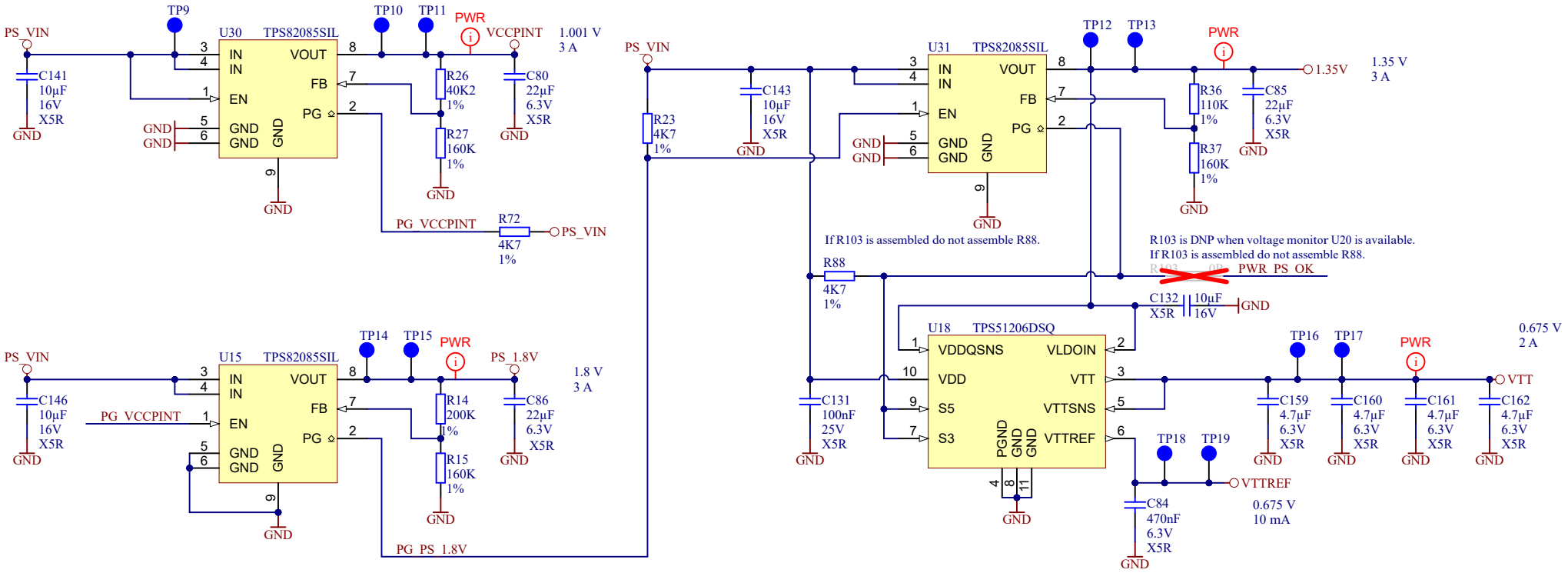
Title: TE0745 - Power

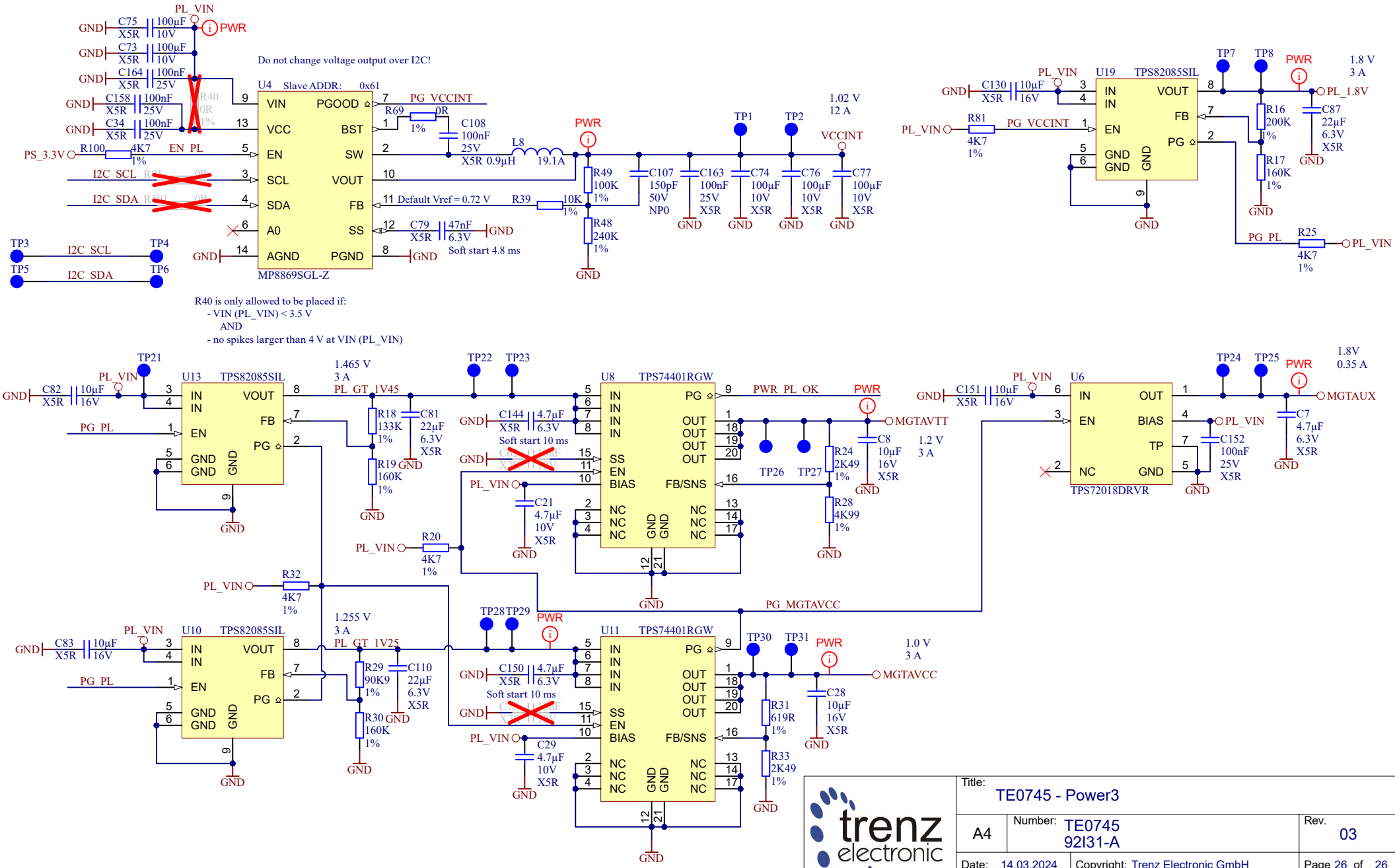
A4 | Number: TE0745 92I31-A | Rev. 03

Date: 17.06.2025 | Copyright: Trenz Electronic GmbH | Page 24 of 26

Filename: POWER.SchDoc



Title: TE0745 - Power2			
A4	Number: TE0745 92I31-A		Rev. 03
Date: 14.03.2024	Copyright: Trenz Electronic GmbH		Page 25 of 26
Filename: POWER_2.SchDoc			


PL_VIN
PWR
Do not change voltage output over I2C!
U4 Slave ADDR: 0x61
MP8869SGL-Z
PG_VCCINT
1.02 V
12 A
VCCINT
PS_3.3V
EN_PL
I2C_SCL
I2C_SDA
Soft start 4.8 ms
Default Vref = 0.72 V
L8
0.9µH
19.1A
U19 TPS82085SIL
PL_1.8V
1.8 V
3 A
R40 is only allowed to be placed if:
- VIN (PL_VIN) < 3.5 V
AND
- no spikes larger than 4 V at VIN (PL_VIN)
U13 TPS82085SIL
1.465 V
3 A
PL_GT_1V45
U8 TPS74401RGW
PWR_PL_OK
MGTAVTT
1.2 V
3 A
Soft start 10 ms
U6
TPS72018DRVR
MGTAUX
1.8V
0.35 A
U10 TPS82085SIL
1.255 V
3 A
PL_GT_1V25
U11 TPS74401RGW
MGTAVCC
1.0 V
3 A
PG_MGTAVCC
PG_PL
Title: TE0745 - Power3
A4
Number: TE0745 92I31-A
Rev. 03
Date: 14.03.2024
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Page 26 of 26
Filename: POWER_3.SchDoc
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