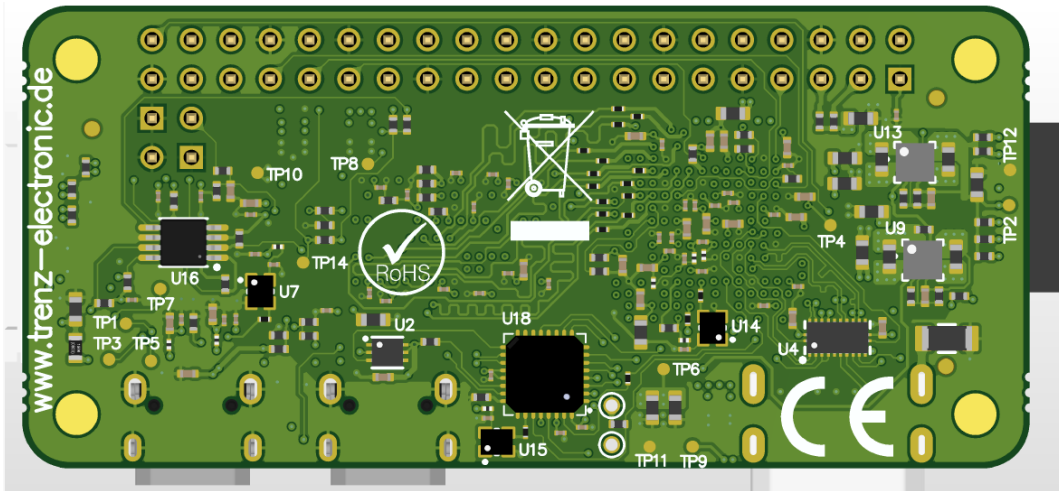
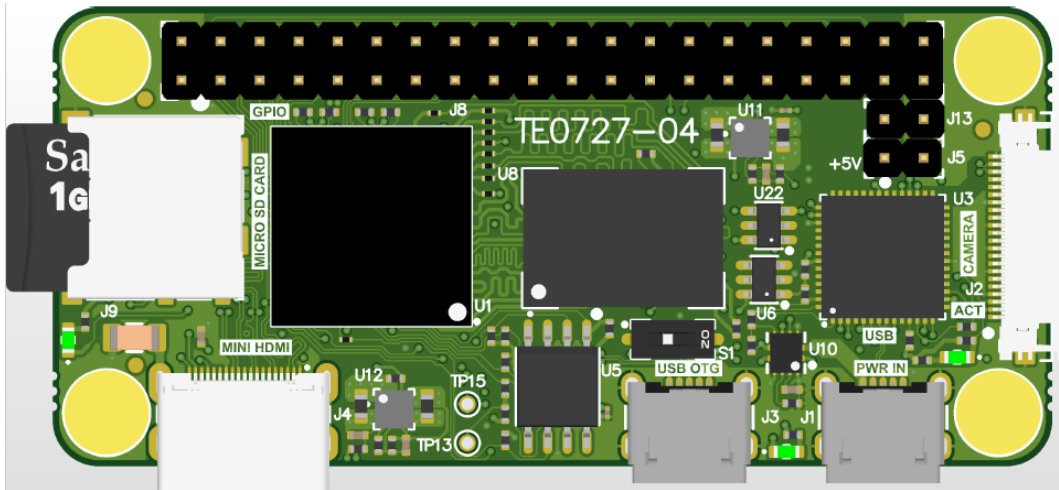




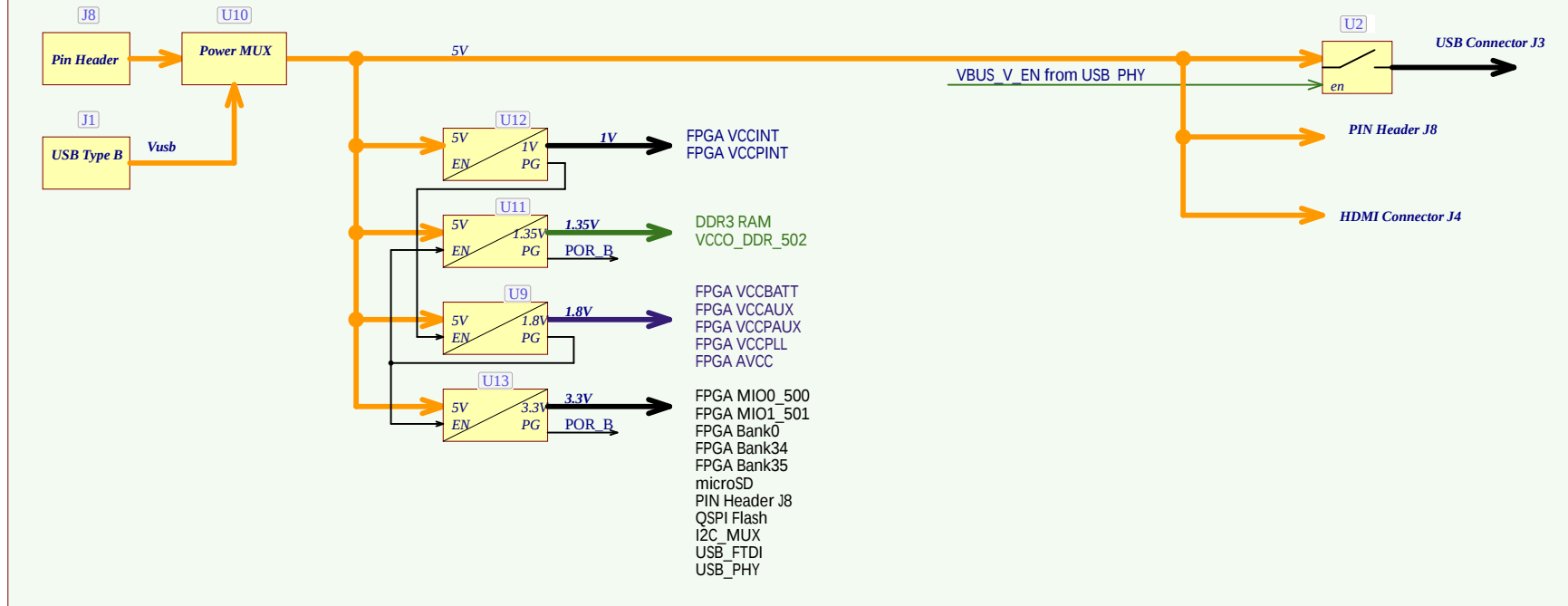
Regarding the usage of our schematics and alike documentation for Trenz module TE0727 .

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0727 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

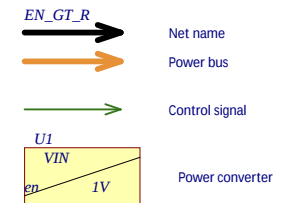
	Title: Legal Notices		
	A4	Number: TE0727 41C38	Rev. 04
	Date: 2023-05-23	Copyright: Trenz Electronic GmbH / TT	Page 1 of 15
	Filename: Legal Notices Modules.SchDoc		

Power-on sequencing:



Supported Voltage Ranges:

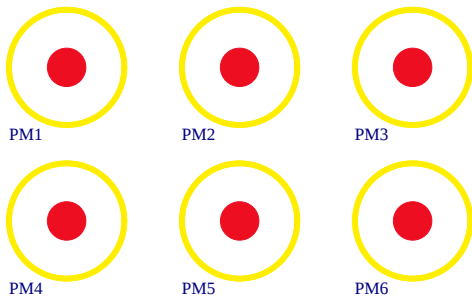
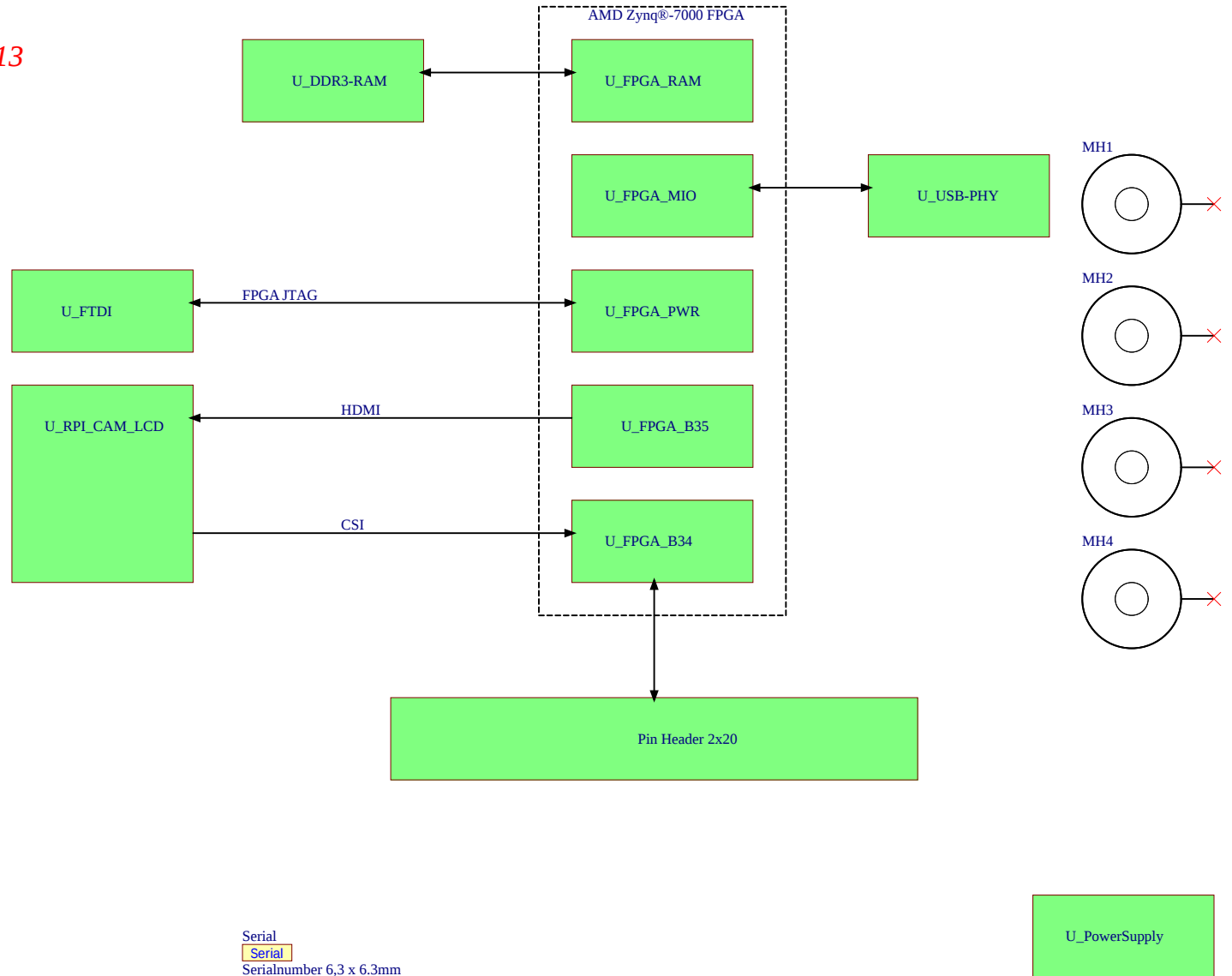
Power Rail	Direction	Range	Tolerance	Description	Note
5V	OUT	5V	+/-5%	Micromodule Power	-
USB_B_Vbus	IN	5V	+/-5%	Micromodule Power	-
USB_Vbus	IN	5V	+/-5%	Internal Power	-
3.3V	OUT	3.3V	+/-3%	Internal Power	-



		Title: Power_Diagram	
		A4	Number: TE0727 41C38
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Rev. 04
Filename: Power_Diagram.SchDoc		Page 3	of 15

Special notes:

U5 replaced with S25FL128LAGMFI013

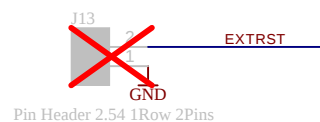
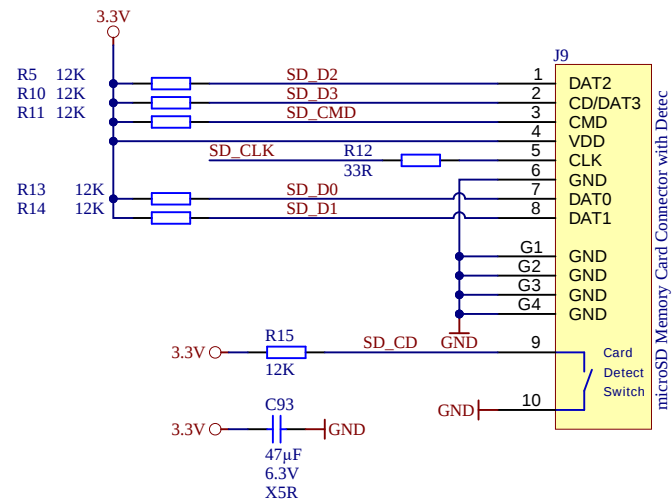
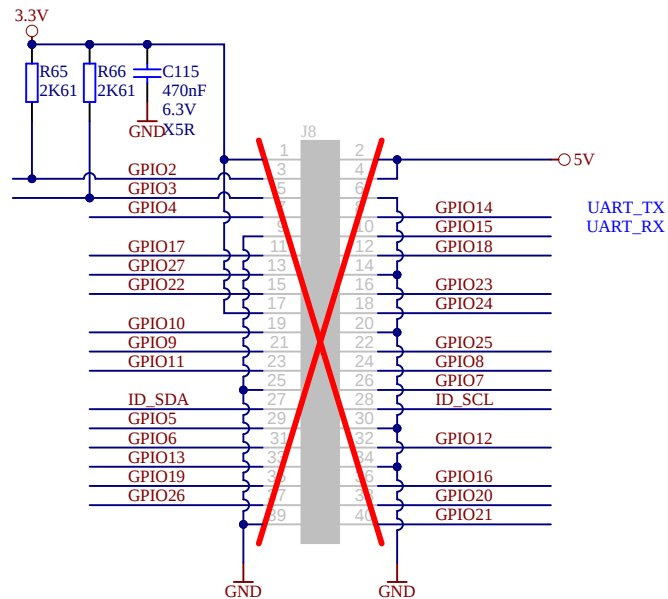


Serial
Serial
Serialnumber 6,3 x 6,3mm

Drawn by	VG
Checked by	IG
Assembly variant	41C38
Created by	VG
Modified by	
Modified at	



Title: Overview		
A4	Number: TE0727 41C38	Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page 4 of 15
Filename: TE0727.SchDoc		



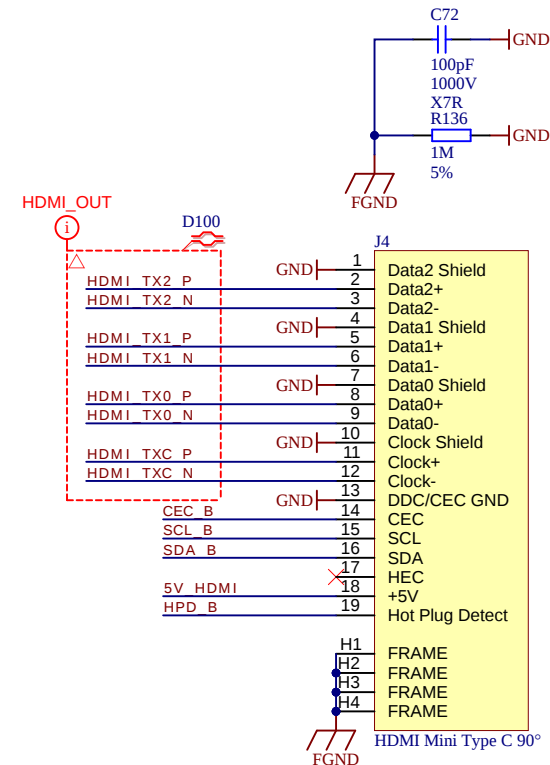
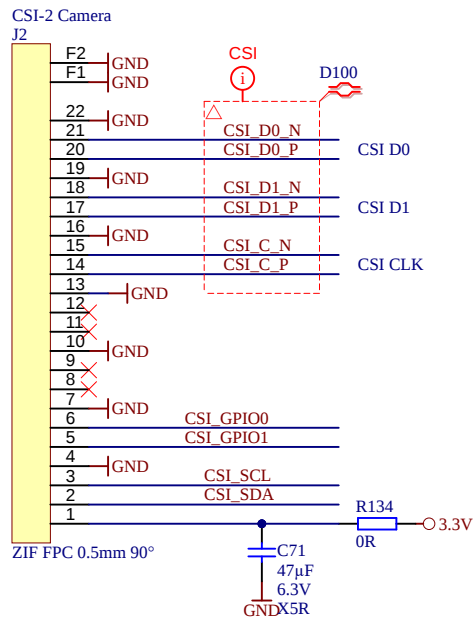
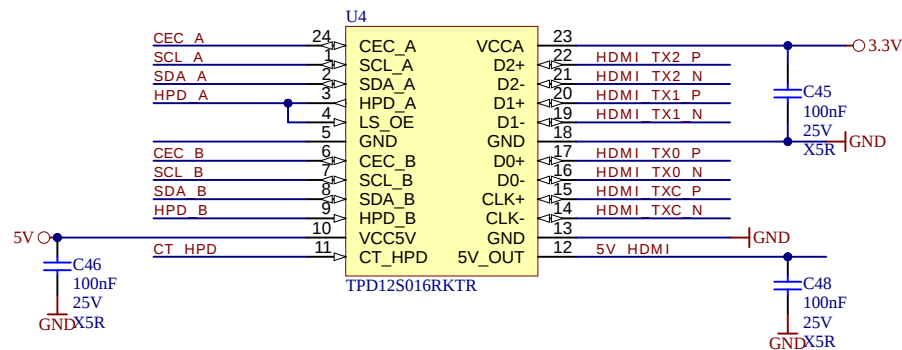
		Title: Connectors	
		A4	Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page5	of 15
Filename: RPi-Headers.SchDoc			

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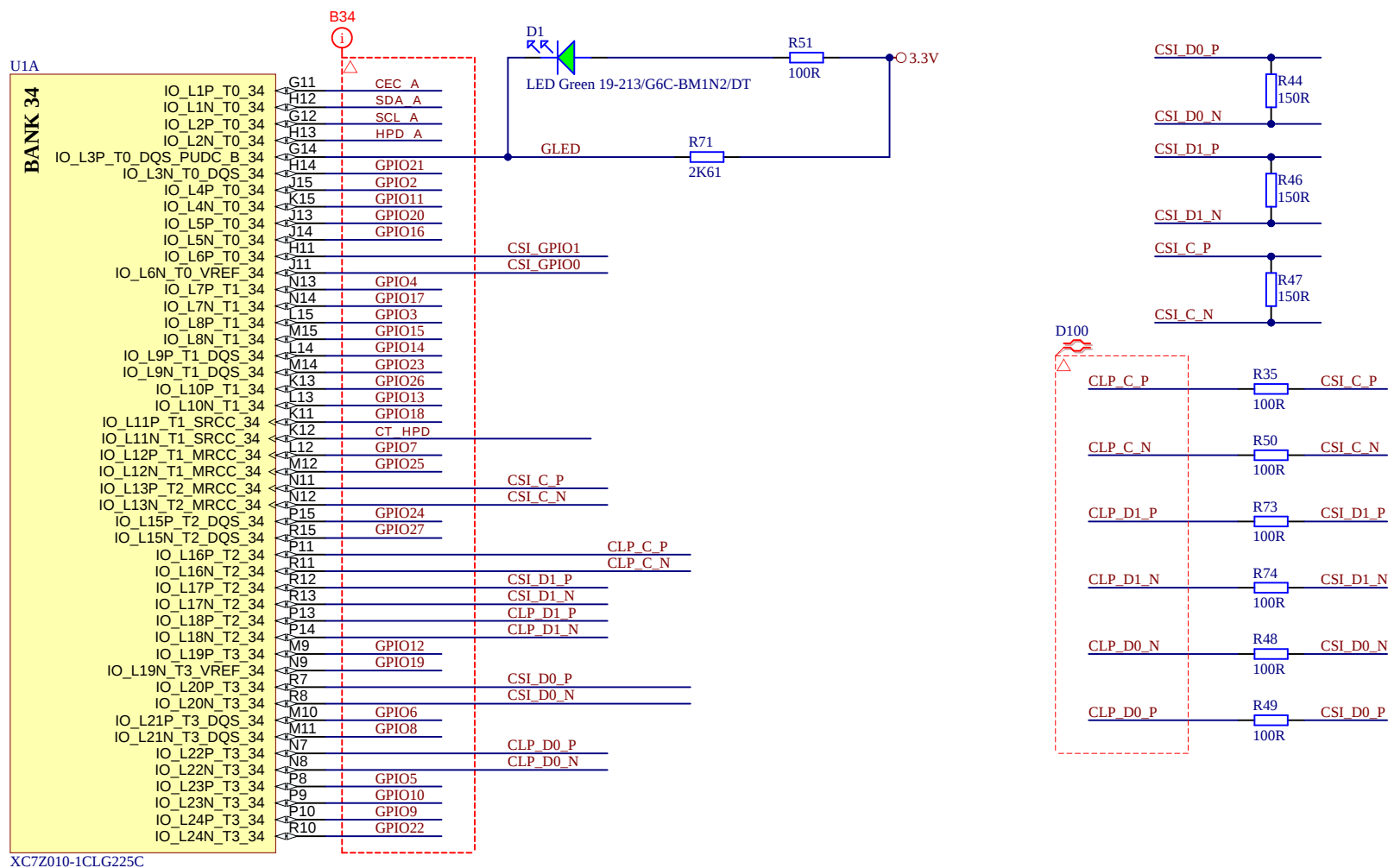
Title: Connectors			
A4	Number: TE0727 41C38		Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page6 of 15
Filename: RPi-CAM-LCD.SchDoc			

1

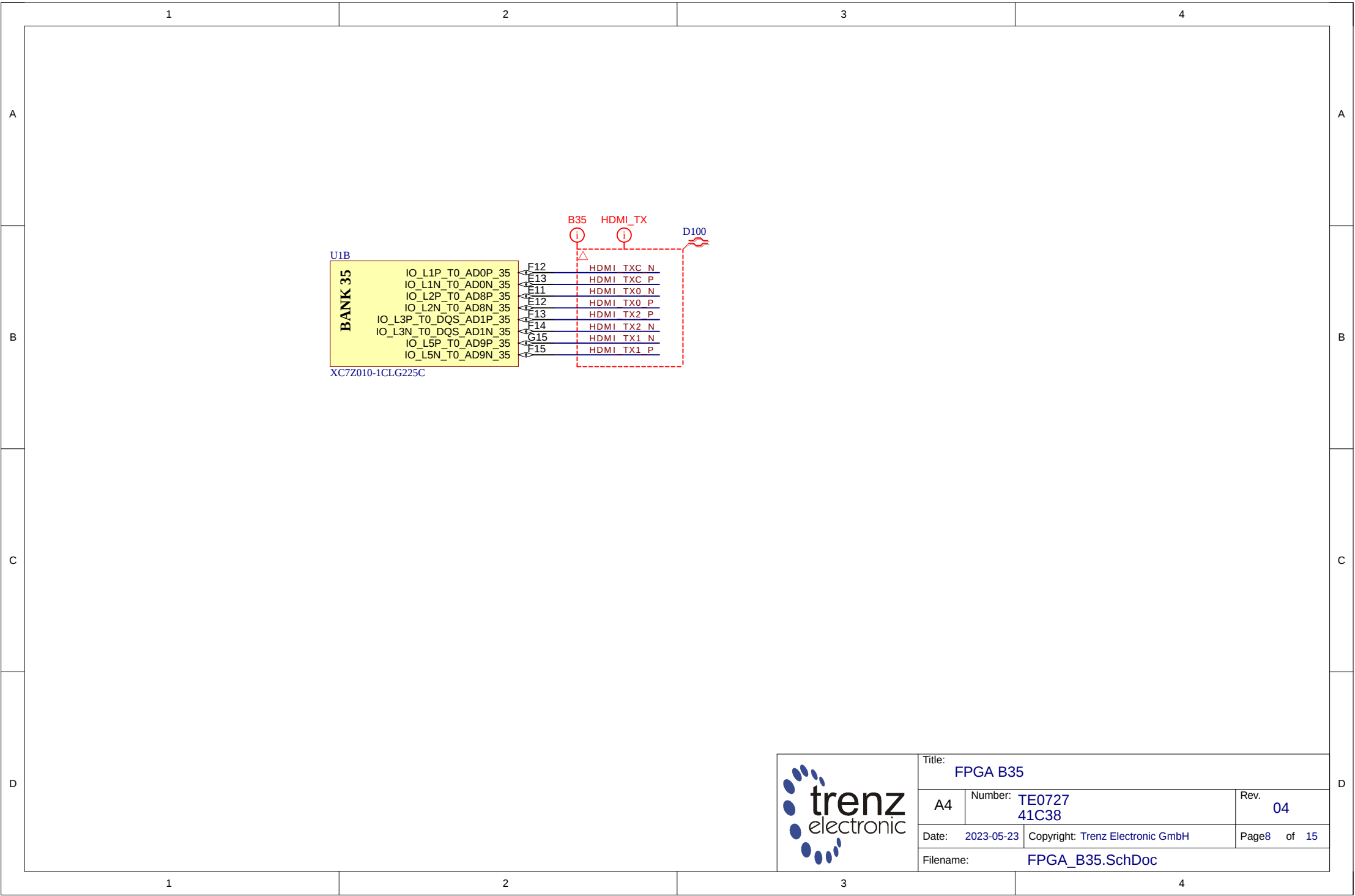
2

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Title: FPGA B34			
A4	Number: TE0727 41C38	Rev. 04	
Date: 2023-05-23	Copyright: Trenz Electronic GmbH		Page 7 of 15
Filename: FPGA_B34.SchDoc			



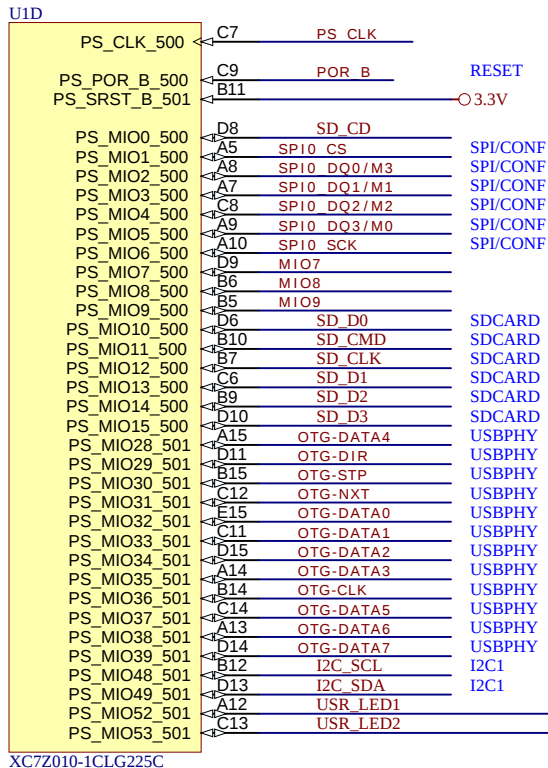
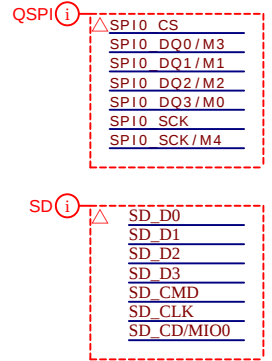
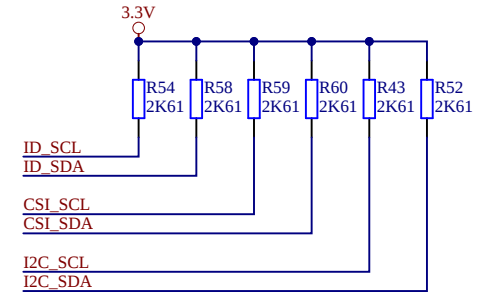
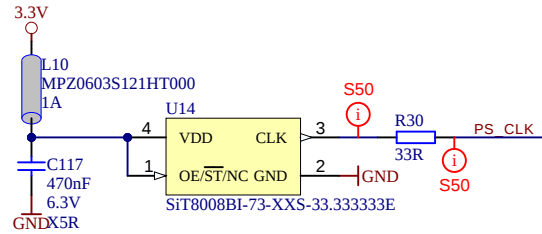
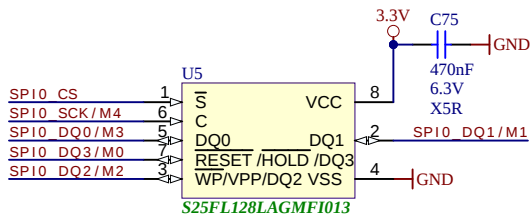
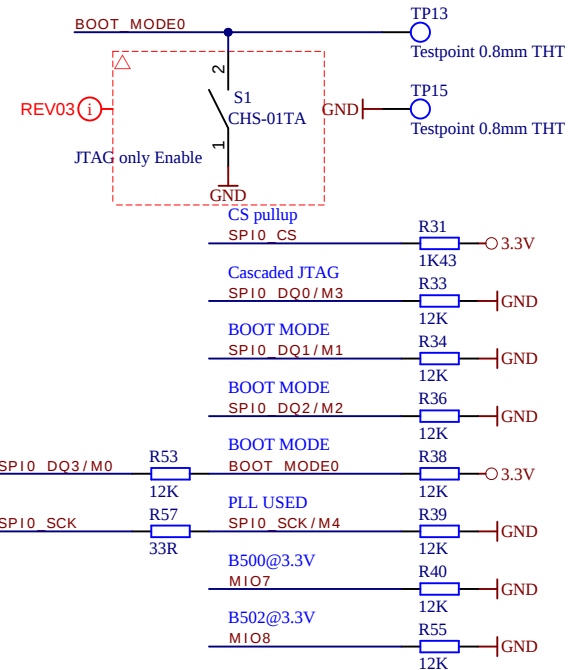
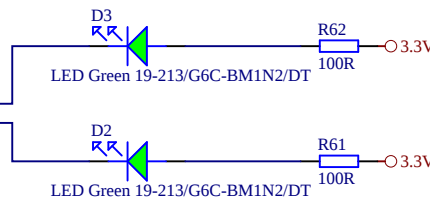
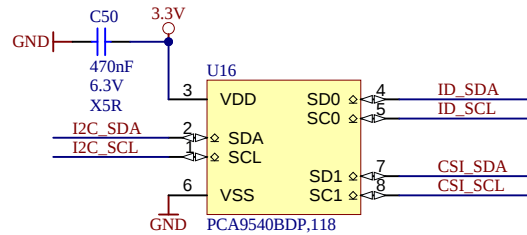


Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common ⁽¹⁾			0	0	0		JTAG Chain Routing ⁽²⁾
NOR Boot ⁽⁹⁾			0	0	1		0: Cascade mode
NAND			0	1	0		1: Independent mode
Quad-SPI ⁽⁹⁾			1	0	0		
SD Card			1	1	0		



Title: FPGA MIO		
A4	Number: TE0727 41C38	Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page 9 of 15
Filename: FPGA_MIO.SchDoc		

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4

A

A

B

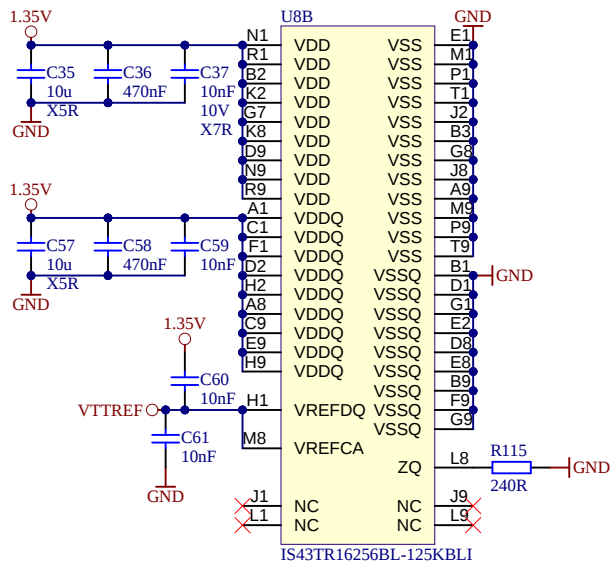
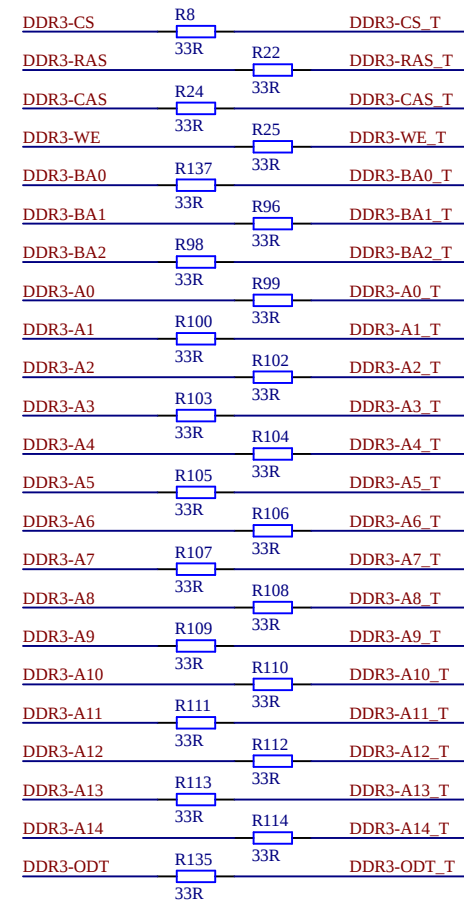
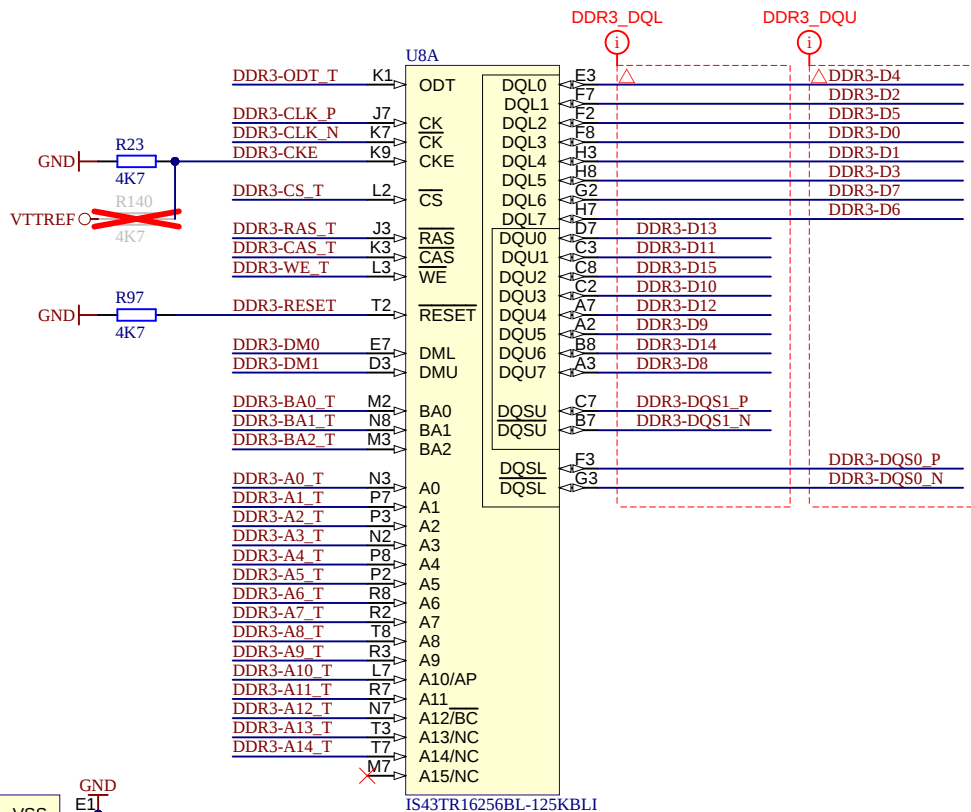
B

C

C

D

D



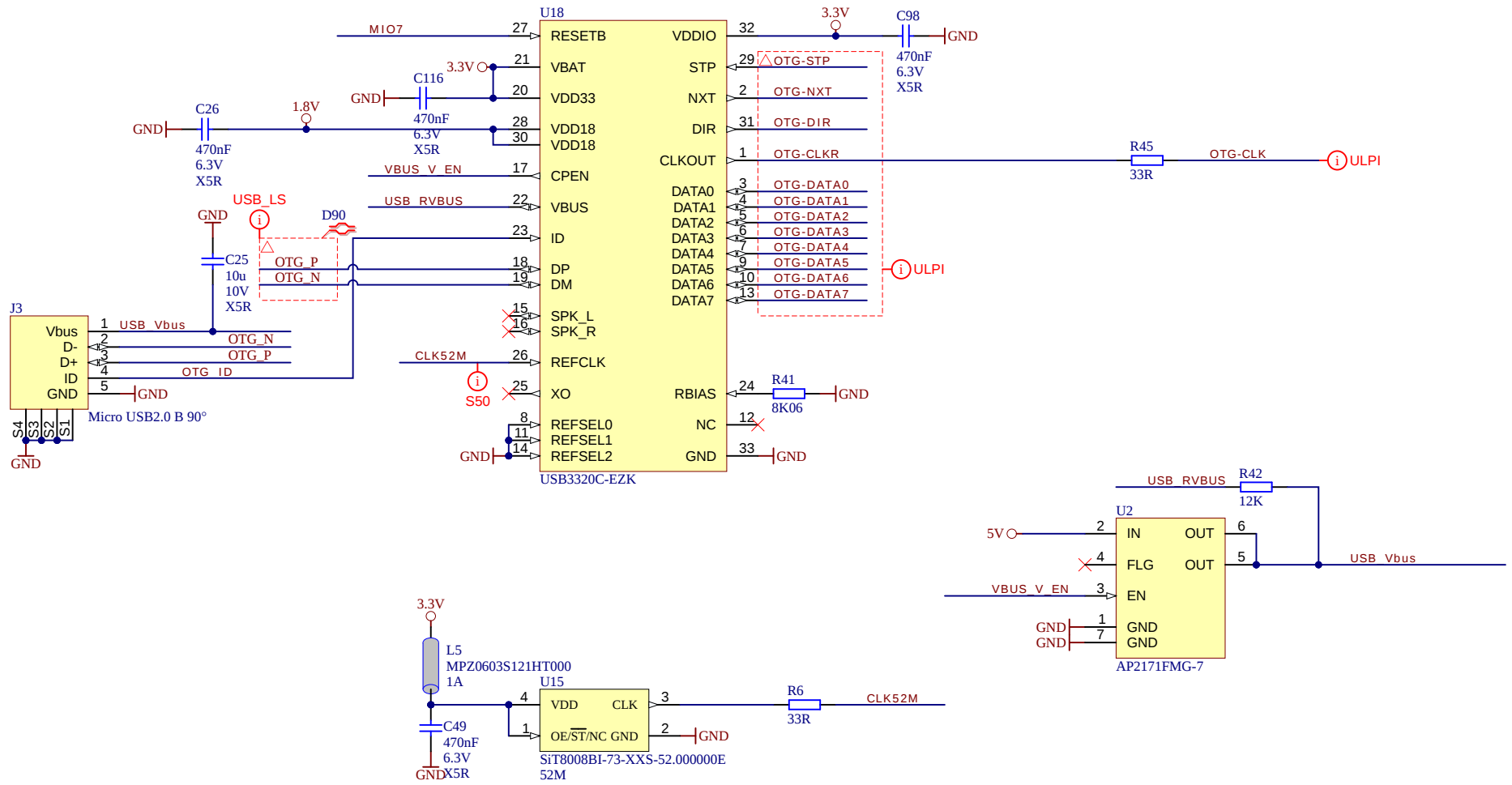
Title: DDR Memory		
A4	Number: TE0727 41C38	Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH	
Filename: DDR3-RAM.SchDoc		Page12 of 15

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	Title: USB		
	A4	Number: TE0727 41C38	Rev. 04
	Date: 2023-05-23	Copyright: Trenz Electronic GmbH	Page13 of 15
	Filename: USB-PHY.SchDoc		



1

2

3

4

A

A

B

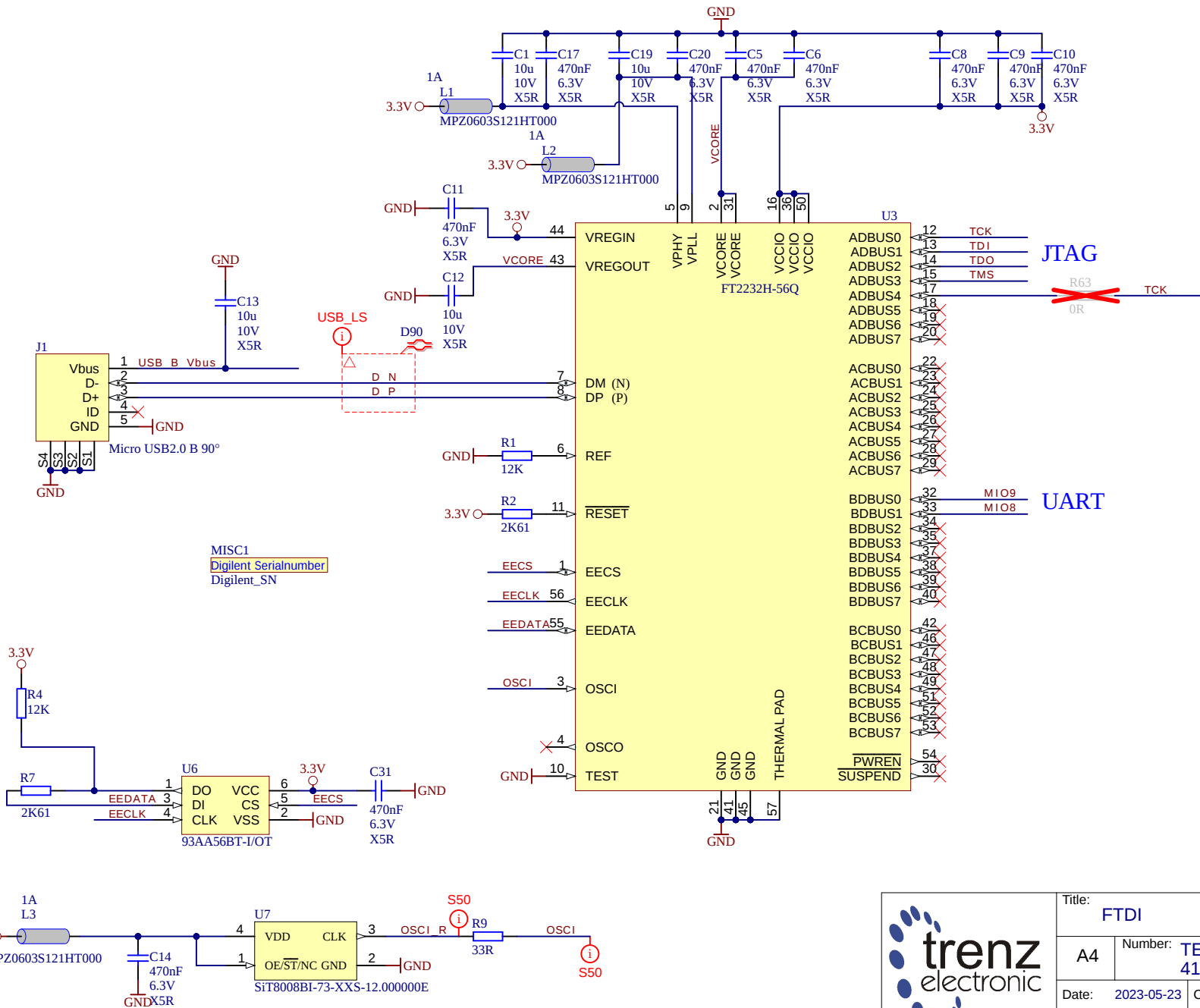
B

C

C

D

D



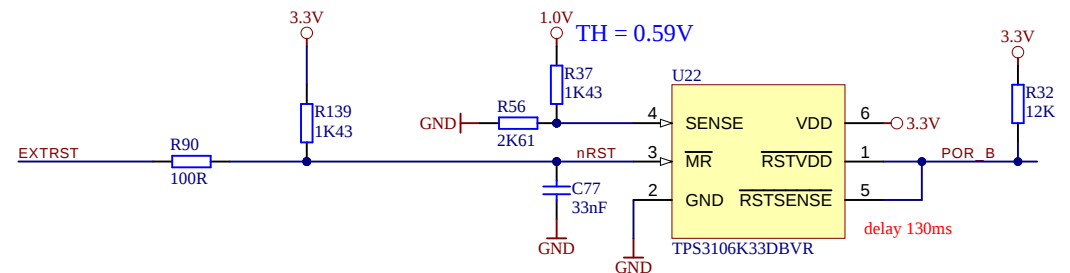
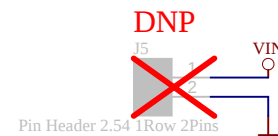
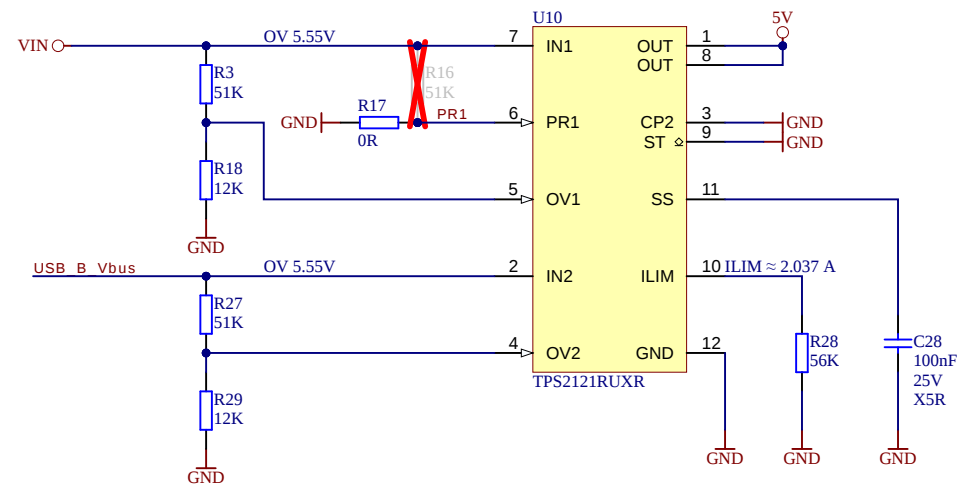
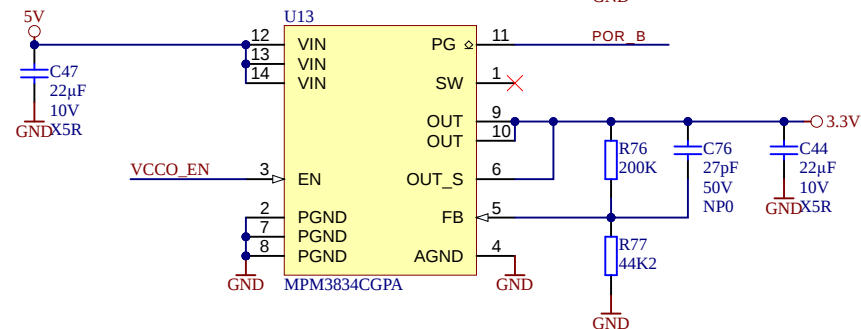
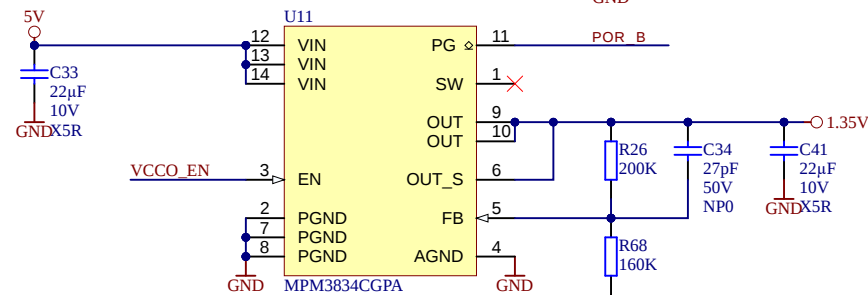
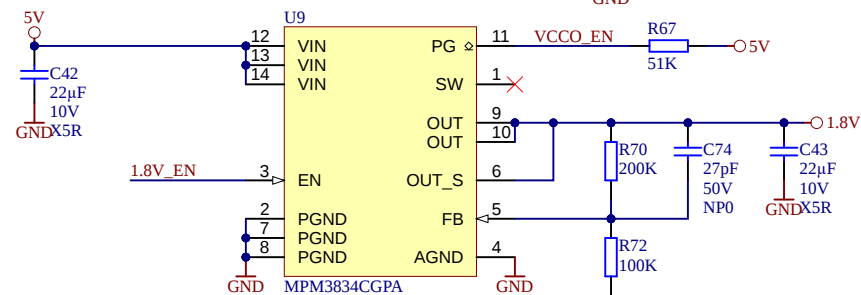
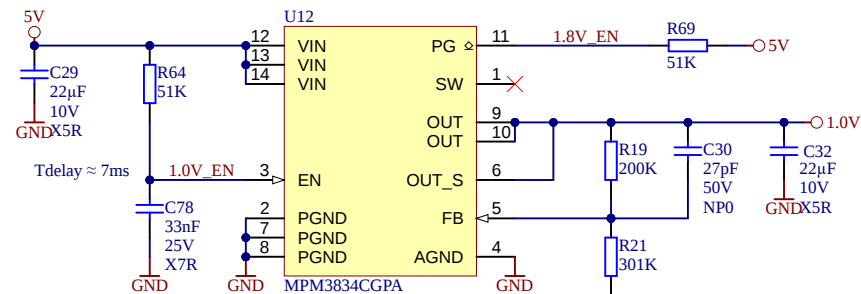
Title: FTDI		
A4	Number: TE0727 41C38	Rev. 04
Date: 2023-05-23	Copyright: Trenz Electronic GmbH	
Filename: FTDI.SchDoc		Page14 of 15

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4



		Title: PowerSupply	
		A4	Number: TE0727 41C38
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Filename: PowerSupply.SchDoc		Page15 of 15	