PE0004
Evaluation Kit
Interface Card

UM0004/1 Jan 26 **USER MANUAL** Provisional

Features

- **Interface control card for EV9180 evaluation**
- **Target IC C-BUS read and write operations**
- **32-Bit Dual core ARM Microprocessor Cortex-M4/Cortex-M0**
- **PC GUI and hardware provided**
- **PC control/communications via USB**

1 Brief Description

The PE0004 Evaluation Kit Interface Card is an interface system for use with a range of evaluation kits.

Based around the NXP ARM microprocessor LPC4337 and using a PC GUI, the information generated is formatted, timed and delivered to the connected evaluation kit via selected C-BUS/SPI serial interfaces or a host port. The supplied control software can be used to perform C-BUS/SPI read and write operations or read or write sample data.

Communication with the PE0004 is via high-speed USB 2.0 compatible port.

The PE0004 is currently used with the following CML Evaluation kits:

- EV9180 Evaluation kit for the CMX918 Low Power Software Defined Radio (SDR) Receiver

CONTENTS

It is recommended that you check for the latest product datasheet version from the Products page of the CML website: www.cmlmicro.com.

History

Version	Changes	Date
1	Initial release for product launch	January 26

2 Block Diagrams

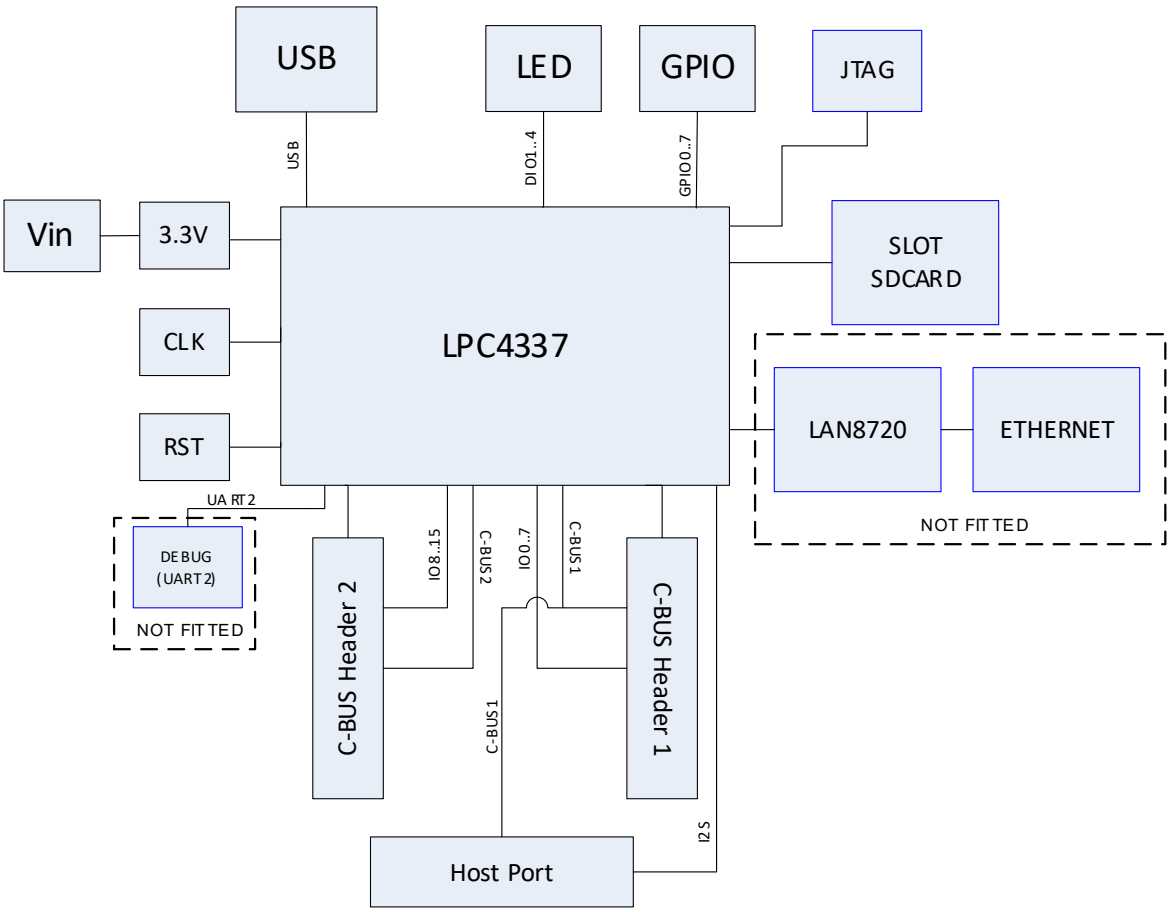

Figure 1 - Device Block Diagram

3 Preliminary Information

3.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

3.1.1 Power Supply

A 5 V DC power supply

3.1.2 PC

With the following requirements: -

- Windows 10 64-bit (or later) installed
- USB port
- Minimum screen resolution 800 x 600. Recommended minimum resolution 1024 x 768.
- 500 MB disc space available

3.1.3 USB cable

A standard USB type A male to mini B male cable

3.2 Handling Precautions

This product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

3.2.1 SSD Devices

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

3.2.2 RoHS Compliance

All devices and evaluation kits supplied by CML Micro are compliant with the latest EU RoHS directive, for further details see RoHS | CMLMicro.

3.2.3 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK0004) and notify CML within seven working days if the delivery is incomplete.

3.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

4 Quick Start

This section provides instructions for users who wish to experiment immediately with this Evaluation Kit. A more complete description of the kit and its uses appear later in this document. See the application specific evaluation kit user manual for details on setup and operation.

- Connect the power supply to the PE0004
- Connect the PE0004 controller to the evaluation kit
- Install the relevant GUI on the PC
- Connect the USB cable between the PE0004 and PC
- The PE0004 uses the WinUSB driver that should be preinstalled on Windows 10 or later, therefore no driver installation is required.
- Connect the relevant input signals to the evaluation kit
- Apply power to the PE0004 and evaluation kit (if required)
- Configure the CMX device through the GUI and begin evaluation

5 Signal Lists

Table 1 - Connector List

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1				Ethernet – not fitted
	1	TD+	DP+	Transmit data +
	2	TD-	DP-	Transmit data -
	3	RD+	RD+	Receive data +
	4	unused		
	5	unused		
	6	RD-	RD-	Receive data -
	7	unused		
	8	unused		
J2				GPIOs
	1	GPIO0	BI	GPIO
	2	GPIO4	BI	GPIO
	3	GPIO1	BI	GPIO
	4	GPIO5	BI	GPIO
	5	GPIO2	BI	GPIO
	6	GPIO6	BI	GPIO
	7	GPIO3	BI	GPIO
	8	GPIO7	BI	GPIO
	9	GND	Power	Ground
	10	3V3	Power	3.3 V power supply
J3[3]				C-BUS 1 port
	1[1]	IO0/RESET1/	BI	Spare I/O / Reset / C-BUS chip
	2	CSN1	O/P	C-BUS 1 chip select
	3	IO1	BI	Spare I/O
	4	CDATA1	O/P	C-BUS 1 command data
	5	IO2	BI	Spare I/O
	6	SCLK1	O/P	C-BUS 1 serial clock
	7	IO3	BI	Spare I/O
	8	RDATA1	I/P	C-BUS 1 reply data
	9	IO4	BI	Spare I/O
	10	IRQN1	I/P	C-BUS 1 interrupt request
	11,12	GND	Power	Ground
	13	BOOTEN1_1	O/P	Hardware boot control
	14	BOOTEN1_2	O/P	Hardware boot control
	15	n/c		
	16	IO5	BI	Spare I/O
	17	IO6	BI	Spare I/O
	18	IO7	BI	Spare I/O
	19	n/c		
	20[2]	n/c or Power		

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J4[3]				C-BUS 1 power bridge
	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0 V power supply
J5				Host port power bridge
	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0 V power supply
J6				Host port
	1	IRQN1	I/P	C-BUS 1 interrupt request
	2	RDATA1	I/P	C-BUS 1 reply data
	3	CDATA1	O/P	C-BUS 1 command data
	4	CSN1	O/P	C-BUS 1 chip select
	5	SCLK1	O/P	C-BUS 1 serial clock
	6	IO0/RESET1/	BI	Spare I/O / C-BUS chip select
	7	GND	Power	Ground
	8	GND	Power	Ground
	9,10,11,12	n/c		
	13	RXCLK	I/P	I2S Receive Clock
	14	TXCLK	I/P	I2S Transmit Clock
	15	RXFS	I/P	I2S Receive Frame Select
	16	TXFS	I/P	I2S Transmit Frame Select
	17	RXD	I/P	I2S Receive Data
	18	TXD	O/P	I2S Transmit Data
	19, 20	GND	Power	Ground
J7				C-BUS 2 port
	1	IO8/RESET2	BI	Spare I/O
	2	CSN2	O/P	C-BUS 2 chip select
	3	IO9	BI	Spare I/O
	4	CDATA2	O/P	C-BUS 2 command data
	5	IO10	BI	Spare I/O
	6	SCLK2	O/P	C-BUS 2 serial clock
	7	IO11	BI	Spare I/O
	8	RDATA2	I/P	C-BUS 2 reply data
	9	IO12	BI	Spare I/O
	10	IRQN2	I/P	C-BUS 2 interrupt request
	11,12	GND	Power	Ground
	13	BOOTEN2_1	O/P	Hardware boot control
	14	BOOTEN2_2	O/P	Hardware boot control
	15	n/c		
	16	IO13	BI	Spare I/O
	17	IO14	BI	Spare I/O
	18	IO15	BI	Spare I/O
	19, 20	n/c		

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J8				C-BUS 2 power bridge
	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0 V power supply
J9				USB
	1	VBUS		USB Mini B type connector - USB
	2	D-		USB Mini B type connector - USB
	3	D+		USB Mini B type connector - USB
	4	n/c		
	5	GNDD		USB Mini B type connector -
	6	SHELL		USB Mini B type connector - USB
	7	n/c		
J10				UART – not fitted
	1	GND	Power	GND
	2	U2_TXD	O/P	Transmit data UART2
	3	U2_RXD	I/P	Receive data UART2
	4	5V	Power	5 V Power supply
J11				Power connector
	1	GND	Power	GND
	2	VIN	Power	5 V regulated power supply
J13				JTAG interface
	1	3V3	Power	
	2	SWIO/TMS	I/P	JTAG test mode select
	3	GND	Power	
	4	SWDCLK/TCL	I/P	JTAG test clock
	5	GND	Power	
	6	SWO/TDO	O/P	JTAG test data output
	7	n/c		
	8	TDI	I/P	JTAG test data In
	9	GND	Power	
	10	RESET#	I/P	Reset. Active low

Table 2 - Test Points

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	-	WAKEUP - Wake up from low power mode pin (input).
TP2	-	E_RXER - Ethernet receive error
TP3	+5 V	+5 V power supply
TP4	+3V3	+3V3 power supply
TP5	GND	Ground
TP6	GND	Ground
TP7	-	TRST
TP8	-	E_TX_CLOCK - ethernet clock input
TP9	12 MHz	XTAL - LPC4337 clock input

Table 3 - Switches

Switches		
Ref.	**Default Position**	**Description**
SW1	O/C	Push to reset the LPC4337 microprocessor

Notes:
I/P = Input
O/P = Output
TL = Test Loop
TP = Test Point

Note[1] : pin J3-1 can be used as an extra CSN for the C-BUS1
Note[2] : used for providing power supply when isolators are fitted
Note[3] : J3 and J4 connectors can be isolated

6 Circuit Schematics and Board Layouts

For clarity, the circuit schematic diagrams are available as separate high-resolution files, which can be downloaded from the CML website. The layout on each side of the PCB is shown in Figure 2 and Figure 3.

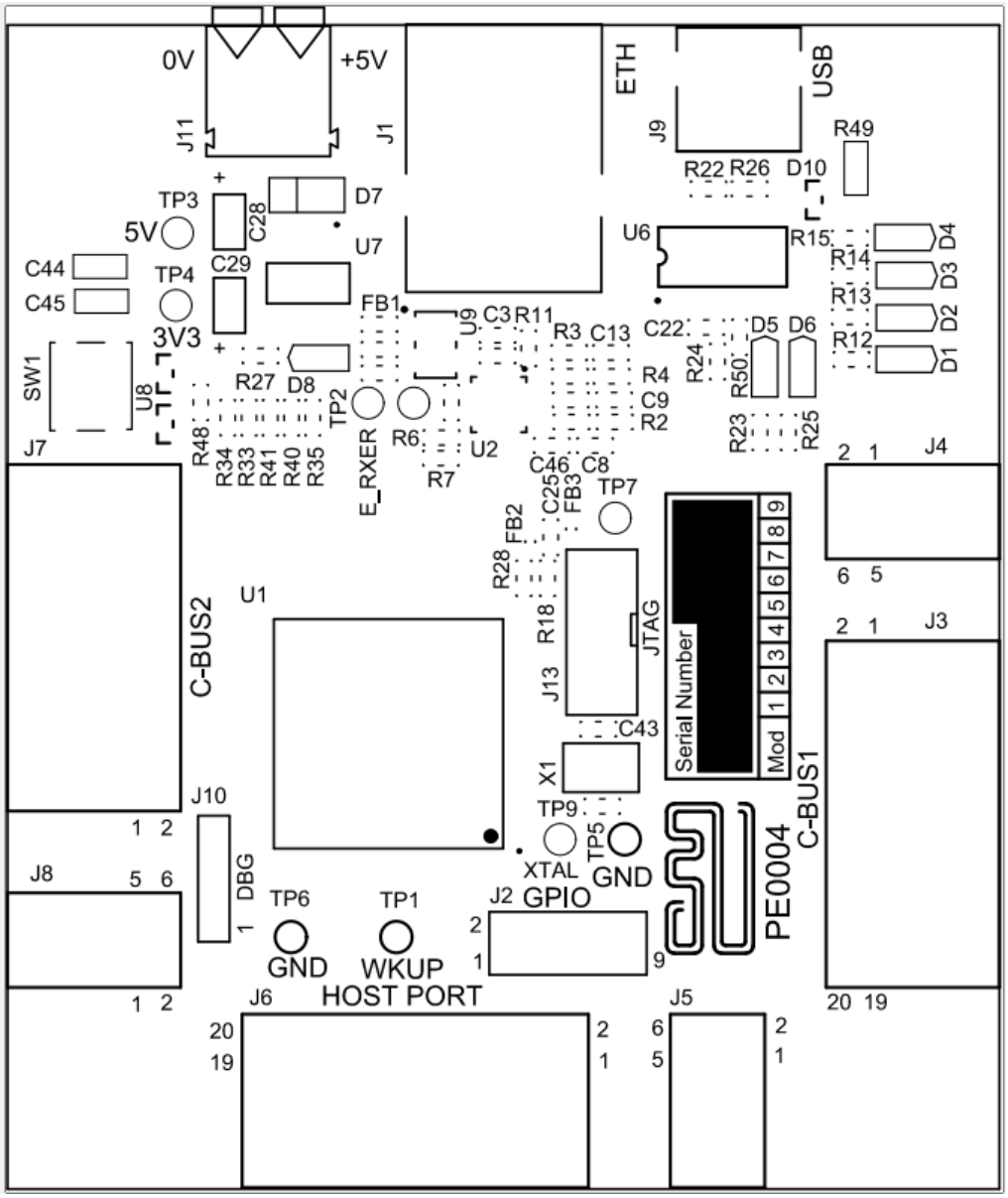

Figure 2 - PCB Layout: Top

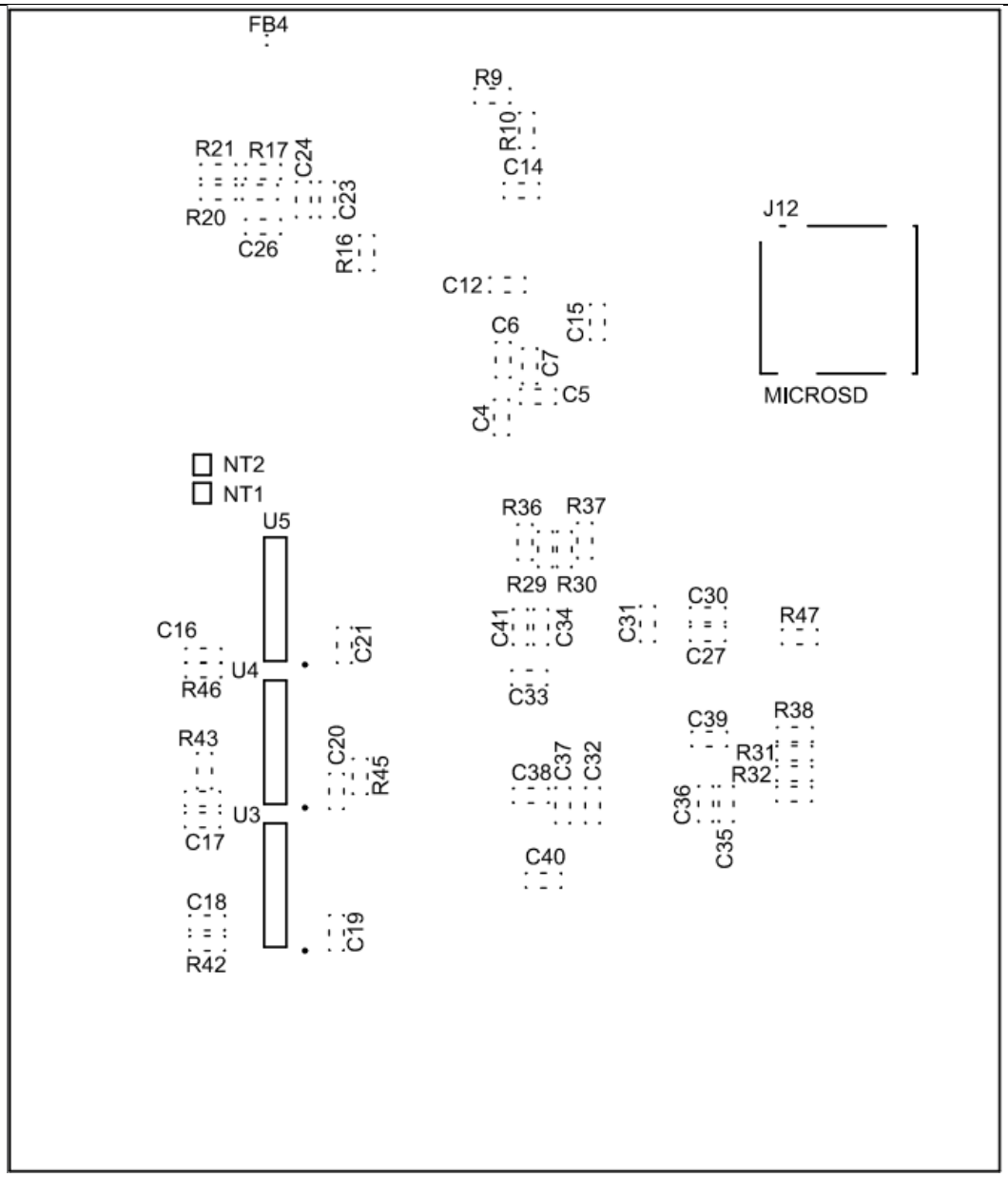

Figure 3 - PCB Layout: Bottom

7 Detailed Description

7.1 Hardware Description

The board is fitted with a voltage regulator, U7, providing the +3.3 V digital supply rail. The input to this regulator is provided by an external un-regulated power supply at, nominally, 5 V DC, which is connected to the board via connector J11 (2-position terminal block). The external unregulated power supply is available at connectors J4 and J8 (right-angle female headers) for mating to target cards at C-BUS1 and C-BUS2 respectively. Similarly, connector J5 for the mating to target cards at the host port.

The nominal 5 V supply and the +3.3 V regulated supply voltage levels can be monitored on test points TP3 and TP4 respectively.

Digital grounds are on test points TP5 and TP6.

D8 will illuminate, confirming presence of the on-board regulated +3.3 V DC digital voltage supply.

The PE0004 uses the NXP LPC4337 microprocessor which combines a 32-bit ARM Cortex-M4 and a 32-bit ARM Cortex-M0 co-processor. The LPC4337 runs at 204 MHz, has 136 kB of SRAM, 1 MB Flash, a USB and Ethernet interface. The LPC4337 toolchain from NXP, including low cost debugging tools, can be used with the PE0004. The board uses a 12 MHz integrated crystal as clock source for the LPC4337 processor. The internal PLLs generate the 204 MHz clock signals.

Two LPC4337 SSP controllers are utilised for C-BUS1 and C-BUS2 and an I2S controller, combined with a the C-BUS1 SSP port utilised for the host port. The C-BUS ports have eight independent I/O pins on each C-BUS port. C-BUS 1 and C-BUS 2 operation can be multiplexed onto C-BUS 1 where pin 1 (IO0) of C-BUS1 provides the second CSN signal.

Isolators can be fitted at C-BUS1 to galvanically isolate the target card from the PE0004. This can increase the noise immunity, particularly that caused by conducted noise and ground loops.

There are eight software-configurable general purpose I/O signals available at connector J2 and four software-configurable LEDs.

The PE0004 improves on the PE0003 by providing higher data rates to the PC and removing the requirements for additional drivers[1]. This is done by utilising the LPC4337 USB peripheral. This change results in a high-speed USB 2.0 compatible port via connector J9.

7.1.1 C-BUS Interface

The C-BUS interfaces transfer data control and status information between the target device's internal registers and the microprocessor over the C-BUS serial bus. Each transaction consists of a single register address byte sent from the microprocessor, which may be followed by one or more data bytes sent from the microprocessor to be written into one of the target device's registers, or one or more bytes of data read out from one of the target device's registers, as illustrated in Figure 4.

[1] The driver used by the PE0004 is installed by default on Windows 10 or later.

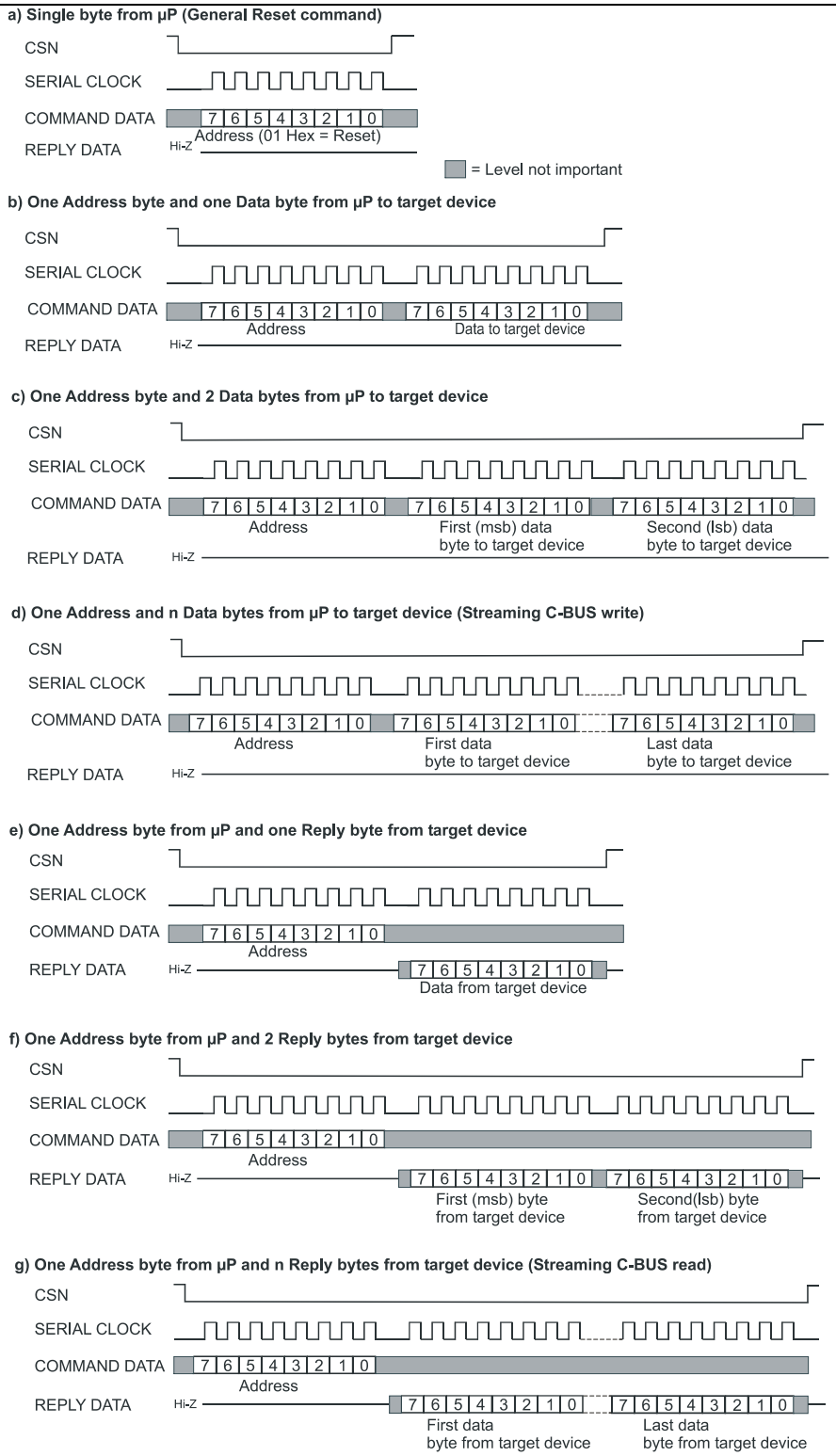

Figure 4 - C-BUS Transactions

All writes and reads to C-BUS1/2 occur via the SSP0/1 peripherals of the LPC4337 Microprocessor.

Two different target devices can be selected by taking CSN1 or CSN2 low on connectors J3 and J7 respectively. If C-BUS1 and C-BUS2 are multiplexed, then C-BUS1/2 signals are routed to J3 and CSN2 is routed to J3:1.

The target device can issue an interrupt by taking IRQN1 or IRQN2 low on connectors J3 and J7 respectively.

7.1.2 Host Port

The Host Port is a merge of C-BUS1 and an I2S port. Pins 1 to 6 are mapped to C-BUS 1 and pins 13 to 19 are mapped to the I2S port. The I2S port consists of three lines for transmission and three for reception. Those three lines are a continuous serial clock, RXCLK/TXCLK, a Frame Sync, RXFS/TXFS (also known as word select WS) and serial data, RXD/TXD.

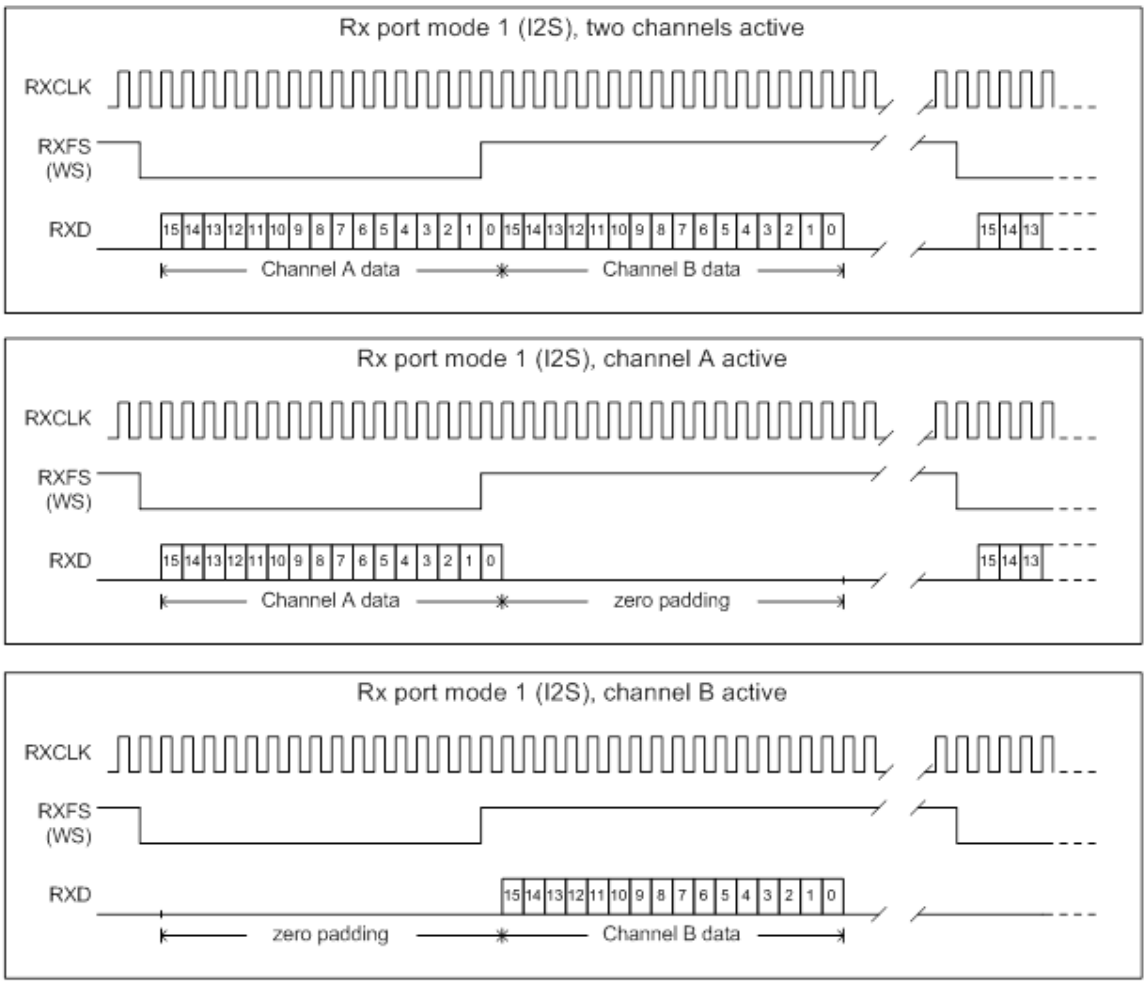

Figure 5 - Rx I2S Timing (identical for Tx)

7.2 Adjustments and Controls

7.2.1 Galvanic Isolation of C-BUS1

The PE0004 has been designed to minimise radiated and conducted noise. If galvanic isolation is required between the PE0004 and the target card, NVE IL715 and IL716 isolators or equivalent can be fitted at C-BUS1. The following steps must be completed:

- On the bottom side of the board, cut the net ties placed within the footprints for U3, U4 and U5, see Figure 6, to isolate the C-BUS1 port
- If the power connector, J4, mates to the target card, cut net ties NT1 and NT2. Pin 20 of C-BUS 1 must be wired to supply power to the isolated side of the PE0004.
- Fit an IL716 at U4 and a UL715 at both U5 and U3. U3 need only be fitted if the signals BOOTEN1, BOOTEN2, IO5 and IO6 are required.
- Fit decoupling components C16, C17, C18, C19, C20, C21, R42, R44, R46, R43 and R45.

Note that if isolation is used signals IO3, IO4 and IO7, J3 pins 7, 9 and 18 respectively, must NOT be connected on the target card because these IO signals are not isolated.

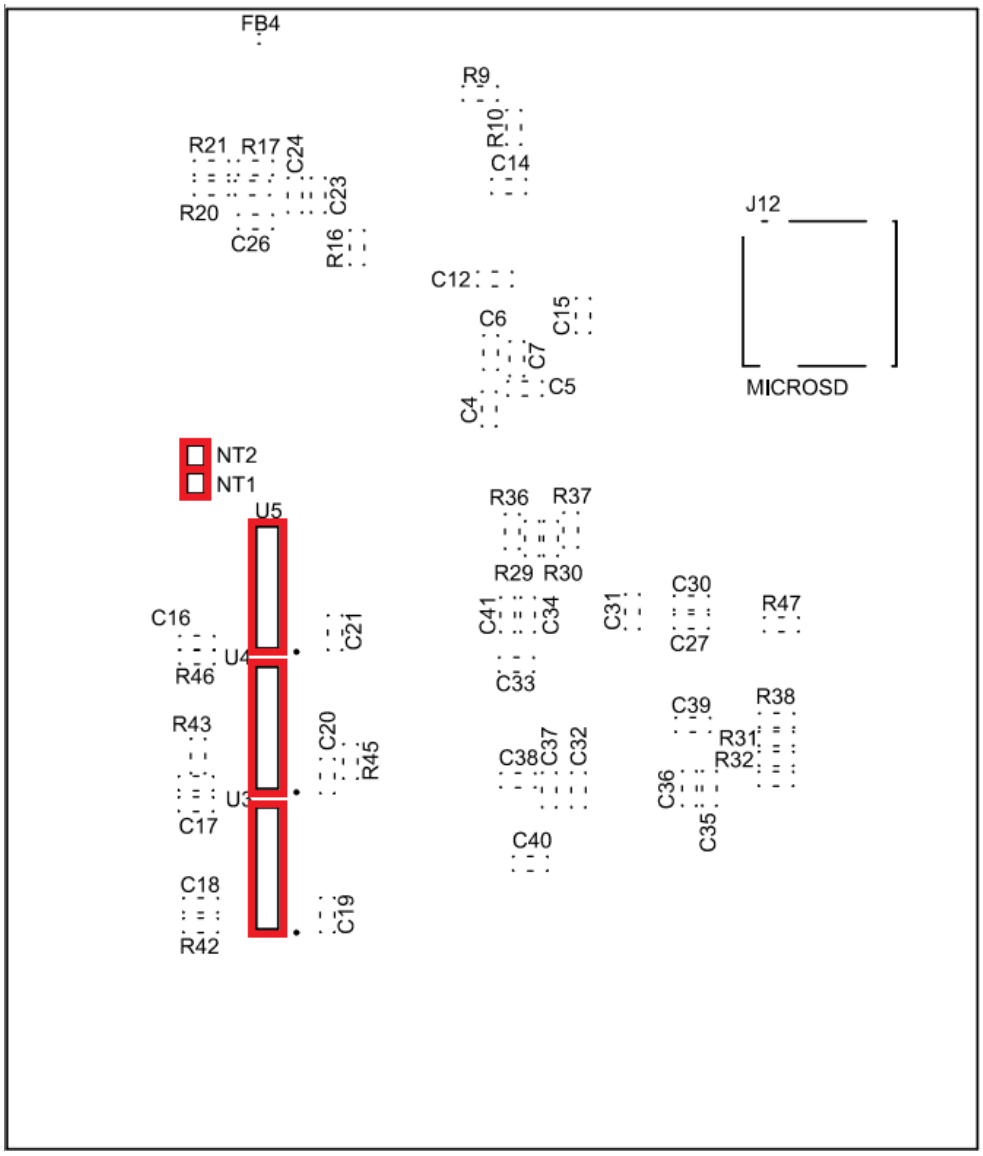

Figure 6 - Net Tie Locations

7.3 Embedded Software Description

On power up the microprocessor will load firmware from internal Flash and run enter an idle state. The firmware will monitor the USB port for an instruction to use the current firmware or download new firmware from the host PC to the internal Flash. The host will read firmware version information from the microprocessor and load new firmware if required.

7.4 Software Description

See the application evaluation kit user manual for details of the software to be used with the PE0004.

7.5 Driver Installation

If using a Windows 10 or later host PC then no driver installation should be required for using the PE0004, as it uses the WinUSB driver (pre-installed on Windows). The PE0004 is a WCID (Windows Compatible ID) device and uses Microsoft OS descriptors to allow the host PC to load the correct driver. Additional information about 'Microsoft OS descriptors for USB devices' and WinUSB is available from Microsoft.

When connected to the host PC at least one device should be listed 'CML Device Firmware Upgrade' in the device manager, other devices may show depending on the firmware loaded into the PE0004.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (VCCIN - GNDD)	4.8	6.8	V
Voltage on any connector pin to GNDD	2.2	3.6	V
Current into or out of VCCIN and GNDD pins	-50	+300	mA
Current into or out of any other connector pin	-20	+20	mA
Storage Temperature	-10	+70	°C
Operating Temperature	+10	+35	°C

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (VCCIN - GNDD)		4.8	6	V
Operating Temperature		+10	+35	°C
Xtal Clock Frequency		11.99	12.01	MHz

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 12 MHz
VCCIN = 5.0 V, T_{AMB} = +25 °C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{CCIN} (5 V) LPC4337 M4 only, all peripherals disabled, 204 MHz	1, 2		96		mA
I/O pins					
V_{IH}	3	2.33		5.5	V
V_{IL}	3	0		1	V
V_{OH} (I_{OH}=-6 mA)	3	2.9			V
V_{OL} (I_{OL}=6 mA)	3			0.4	V
I_{OH}	3	-6			mA
I_{OL}	3	6			mA
I_{OHS} (short-circuit)	3			86.5	mA
I_{OLS} (short-circuit)	3			76.5	mA
I_{pd} (pull-down current) (V_I = 5 V)	3		93		µA
I_{pu} (pull-up current)(V_I = 0 V)	3		-62		µA
V_{IH}	4	2.33		5.5	V
V_{IL}	4	0		1	V
V_{OH} (I_{OH}=-8 mA)	4	2.9			V
V_{OL} (I_{OL}=8 mA)	4			0.4	V
I_{OH}	4	-8			mA
I_{OL}	4	8			mA
I_{OHS} (short-circuit)	4			86	mA
I_{OLS} (short-circuit)	4			76	mA
I_{pd} (pull-down current) (V_I = 3.3 V)	4		62		µA
I_{pu} (pull-up current)(V_I = 0 V)	4		-62		µA
Input/Output Capacitance	4			2	pF
C-BUS clock frequency		1.0	10.0		MHz
I2S Interface					
V_{IH}	5	2.33		5.5	V
V_{IL}	5	0		1	V
V_{OH} (I_{OH}=-8 mA)	5	2.9			V
V_{OL} (I_{OL}=8 mA)	5			0.4	V
I_{OH}	5	-8			mA
I_{OL}	5	8			mA
I_{OHS} (short-circuit)	5			86	mA
I_{OLS} (short-circuit)	5			76	mA
I_{pd} (pull-down current) (V_I = 3.3 V)	5		62		µA
I_{pu} (pull-up current)(V_I = 0 V)	5		-62		µA
Input/Output Capacitance	5			2	pF
I2S clock frequency				12.6	MHz

Notes:

1. Not including any current drawn from the output pins by external circuitry.
2. No Target Card connected.
3. BOOTEN1, BOOTEN2, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO8, IO9, IO10, IO11, IO12, IO13, IO14 and IO15.
   Normal drive strength. The IO pins have another option for high currents. In case of using the Isolators the pins IO0,IO1, IO2, IO5 and IO6 do not follow the values of the table (depends on the isolator fitted).
4. CSN1, CSN2, IRQN1, IRQN2, RDATA1, RDATA2, CDATA1, CDATA2 SCLK1 and SCLK2 pins.
5. TXD, RXD, TXFS, RXFS, RXCLK and TXCLK.

Contact information

For further information please contact your local CML sales representative.
Contact details can be found at www.cmlmicro.com