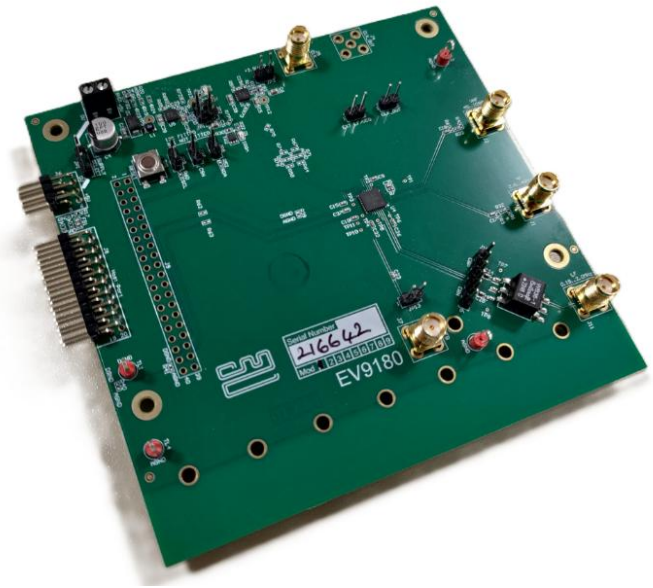
EV9180
Evaluation Kit for CMX918

Features

- **CMX918 Low Power SDR Evaluation**
- **Flexible LF /MF Input 150 kHz – 2000 kHz**
- **HF Input (50 Ω) 2 MHz – 40 MHz**
- **VHF Input (50 Ω) 40 MHz to 108 MHz**
- **Integrated PLL and VCO**
- **I2S/SPI Output Data Interface**
- **On-board Voltage Regulators**
- **38.4 MHz XTAL with optional external reference input**
- **Used with the PE0004 PC Control and data interface board – available separately**
- **Control, measurement and analysis tools based on Microsoft Windows™**



1 Brief Description

The EV9180 is a demonstration, evaluation and development platform for the CMX918 integrated circuit. The CMX918 a low power software defined radio (SDR) tuner supporting operation from 150 kHz to 108 MHz. The evaluation kit plus the associated Windows™ application (ES9180) allows the user to investigate all aspects of the CMX918 and provides graphical display of the IQ sampled output data stream, in both time and frequency domains. With separated RF inputs, the user can control the PLL / local oscillator, mixer, IF filtering, AGC, ADC functions, and digital filtering. An output IQ data interface to an appropriate host processor for demodulation functions is provided. The IC is suitable for receiving a huge variety of signals including AM, FM (wide and narrow), SSB, RTTY, NAVDAT, DRM and DRM+ signals. The CMX918 can also be used as a tuned IF sub-system within a high performance super-heterodyne receiver.

The EV9180 is controlled via the serial interface provided on the CMX918 (SPI/C-BUS). The PE0004 Interface card is available separately to support the PC-based control of the EV9180, graphical display of the IQ output data and for grabbing IQ output data for further simulation analysis. The PE0004 uses ES9180xx.exe PC software, part of the ES9180xx.zip file, which is available on the CML Micro website.

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It is recommended that you check for the latest product datasheet version from the Products page of the CML website: www.cmlmicro.com.

History

Version	Changes	Date
1.0	Initial release for product launch	January 2026

2 Block Diagrams

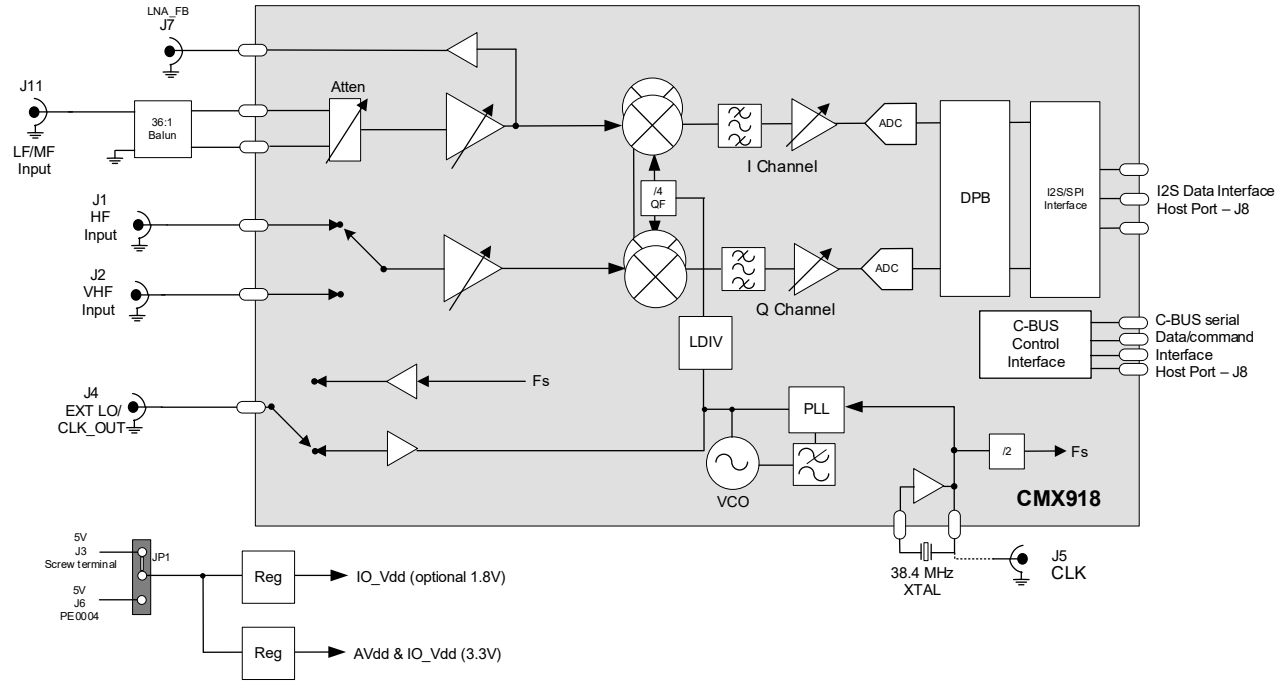


Figure 1 - Block Diagram

3 Preliminary Information

The EV9180 provides a complete platform for evaluation of the CMX918 (device U4). This document refers to revision D of the EV9180 PCB (PCB779D).

Key features

- LF and MF bands (150 kHz to 2000 kHz) input via 50 Ω SMA or differential via pin headers.
- HF band (2.0 MHz … 40 MHz) and VHF band (40 MHz … 108 MHz) inputs via 50 Ω SMA connectors
- IQ channels baseband data outputs via an I2S/SPI interface
- PLL test output signals
- On-board reference frequency source (Crystal – XL1 – Optional external reference frequency input (e.g. TCXO))
- Connector for CMX918 register configuration via host controller and USB / Windows PC GUI
- 5 V power supply connector with reverse polarity protection
- All required regulated power supplies with options for current monitoring etc.

3.1 Laboratory Equipment

The following items are required for evaluation of the EV9180:

- Laboratory power supply
- PE0004 Universal Interface Controller and USB lead (Type A to Mini B)
- PC (Windows 10 or later, 64 bit), 500 MB of free storage is advised
- ES9180xx.exe Graphical User Interface software (available from the CMX918 Knowledge Base, www.cmlmicro.com)
- Oscilloscope
- RF signal generator
- Digital Multi-Meter

This document refers to latest revision of the of the ES9180 GUI (ES9180xx.exe). GUI Installation is covered in Section 7.4.1. System connectivity is shown in Figure 2.

3.1.1 Power Supply

The input voltage to the PCB at J3 is nominally 5.0 V. The input power supply should be rated at 200 mA. On-board regulators are provided; a 3.3 V with an optional 1.8 V supply to the circuits used on the PCB.

NOTE: Care should be exercised with the supplies as there is the option to power the EV9180 directly from the PE0004 +5 V supply via J6, selected via JP1.

3.2 Handling Precautions

This product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

3.2.1 RF Levels

The level applied to any of the EV9180 RF inputs must be kept below +10 dBm maximum. Suitable precautions must be taken (e.g. use of external attenuators or limiters) if using the EV9180 with antennas in high RF environments to prevent damage.

3.2.2 SSD Devices

This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Always observe ESD precautions when handling this product.

3.2.3 RoHS Compliance

All devices and evaluation kits supplied by CML Micro are compliant with the latest EU RoHS directive, for further details see RoHS | CMLMicro.

3.2.4 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EKA9180) and notify CML within seven working days if the delivery is incomplete.

3.3 Approvals

This product is not approved to any EMC or other regulatory standard, as it is an evaluation board intended for lab and test use. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

4 Quick Start

This section provides instructions for users who wish to experiment immediately with this Evaluation Kit. A more complete description of the kit and its uses appear later in this document. The user should also refer to the CMX918 datasheet for a comprehensive description of its operation and features.

4.1 Setting Up

Power-up sequence.

1. Connect the boards as shown in Figure 2.
2. Ensure that the power supply JP1 link is correctly configured (1-2 for external supply)
3. Connect a PE0004 controller board to the EV9180 using the host port of the PE0004 (J6 on the PE0004 and J8 on the EV9180). This will then enable CMX918 register control.
4. Connect a USB cable between the PC and J9 (Mini B) of the PE0004.
5. Ensure that the EV9180 regulator output links are fitted for analogue supply (JP3) and JP11 (IO_VDD)
6. To prevent chip damage in case of incorrect connection, it is recommended to set the power supply current limit to 200 mA for the EV9180 and 700 mA for the PE0004.
7. Apply power to the PE0004 (J11) and then the EV9180 (J3). Green LED D2 on the EV9180 should be lit.
8. The CMX918 powers up in standby mode.
9. The EV9180 can then be configured via the PE0004 from a PC using the ES9180 GUI software.
10. A receive signal can be applied to an RF input (e.g. J1 for the HF signal path).

The EV9180 is now ready for operation.

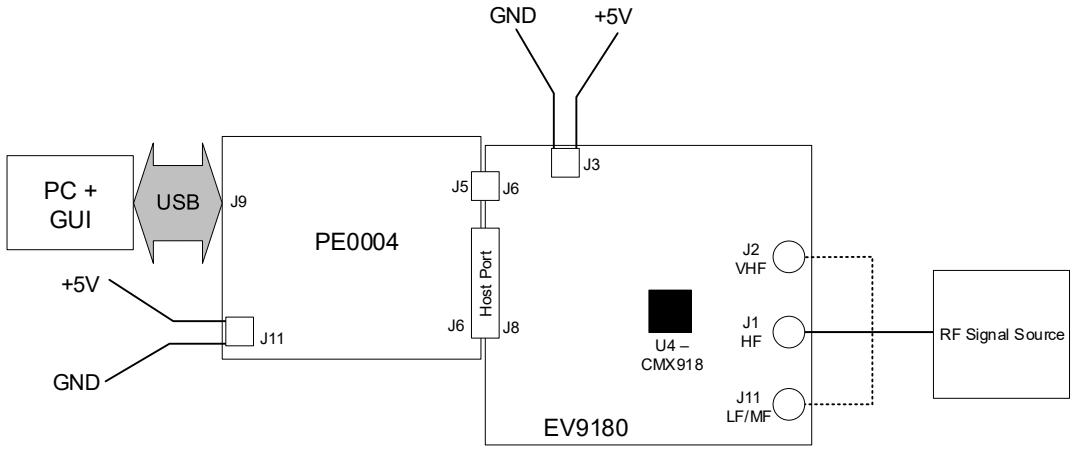


Figure 2 - Typical Evaluation Connections for EV9180

The above configures the EV9180 for SPI/C-BUS control interface operation. For use with an I2C controller, jumpers JP7, JP8 and JP9 should be fitted on the EV9180. Note the PE0004 does not support I2C communications.

4.2 Operation

For GUI installation, refer to section 7.4.1

When power is applied to the PE0004 and EV9180, the CMX918 will be reset.

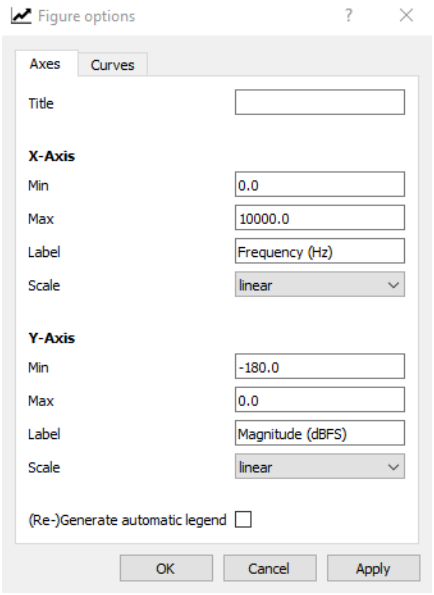
Run the ES9180 PC GUI. (The GUI will halt and give a warning if no connection can be established to either the PE0004 or the CMX918). For ease of use select / tick the Auto Write box in the bottom left corner and the Poll Enabled box.

In the General tab, select Normal from the mode drop-down selection.
Enter 152000 in the Fc box (this corresponds to 15.200 MHz – note the Fc value is in units of 100 Hz).

Select BW = 10 kHz from the drop-down menu.

Check that indicator PLL_LOCK is red.
Click on the PLL_CALC EXE button.
The PLL_LOCK, PLL_SAS_CMPL and PLL_SAS_CMPH indicators should now all be green.
The IC is now tuned for an input signal at 15.200 MHz.
Apply 15.202 MHz at -90 dBm CW to connector J1 (HF) (note 2 kHz offset in signal which will output a 2 kHz signal in the IQ data output).
The reported DPB_RSSI_OUT RSSI value should be very close to -90 dBm.

In the FFT tab, click on Start. Click on the 'edit axis' button at the top, and for the X-Axis select min 0 and max 10000. For the Y-Axis select min -180 and max 0. Note that a title can be optionally added to the plot. Click 'apply' followed by OK.



The following should then be displayed, showing a tone at ~2 kHz in the IQ baseband output.

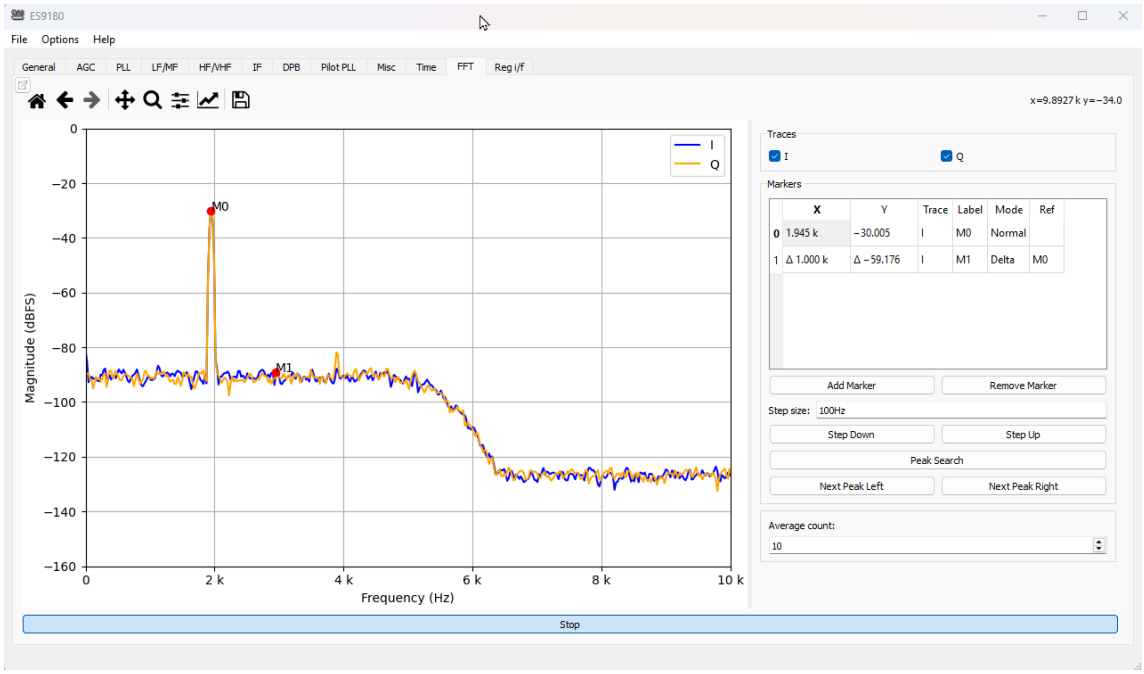


Figure 3 – Typical result of -90 dBm applied to the HF input at 15.202 MHz, 10 kHz BW selected. Note the RF and IF gains are at maximum. Average count of 10 selected.

A small error in the output tone frequency is due to a tuning error in the 38.4 MHz XTAL (XL1) and therefore an offset between the input signal and the internal LO signal. The frequency offset can be adjusted for minimum error from 2 kHz using the PLL_XTAL_Caps value in the PLL tab.

The IQ sample values can also be observed in the time domain using the Time tab.

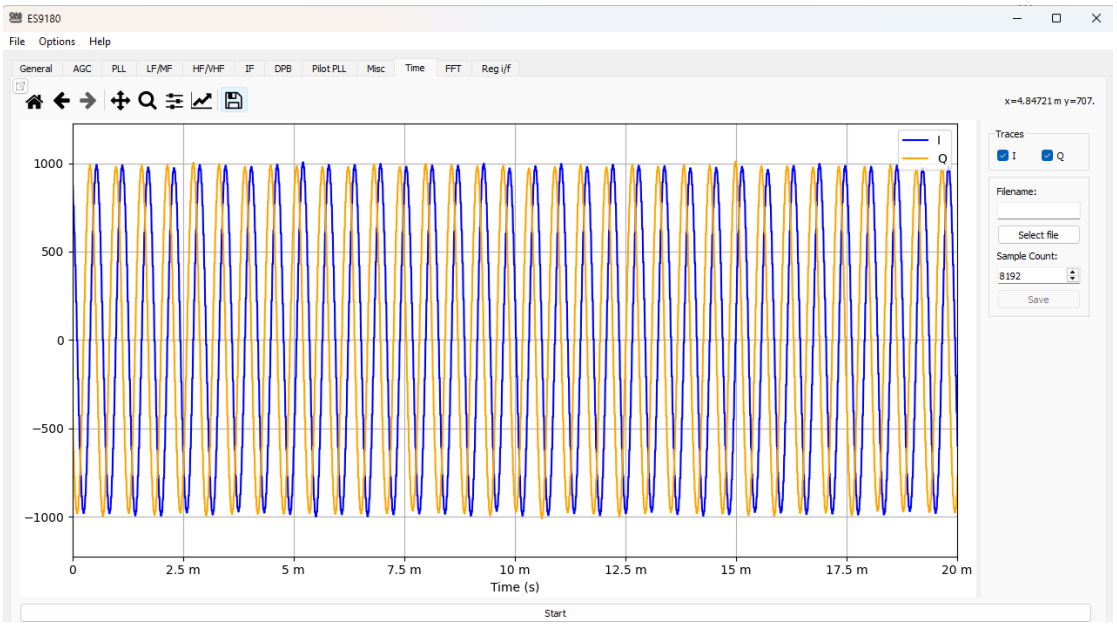


Figure 4 – Typical time tab display of -90 dBm into the HF input at 15.202 MHz, 10 kHz BW selected.

5 Signal Lists

Table 1 - Connector List

RF CONNECTORS				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	N/A	HF_IN	RF	50Ω input connector for HF band
J2	N/A	VHF_IN	RF	50Ω input connector for VHF band
J4	N/A	CLK_OUT	RF	CLK Output divide by 2 or External LO input (SMA – Not Fitted)
J5	N/A	XTALp/CLK	RF	External reference frequency input (SMA). See Table 8 - Reference source configuration.
J7	N/A	LNA_FB	RF	Integrated LNA feedback follower output (SMA)
J11	N/A	LF_MF	RF	50Ω input connector for LF and MF bands (150 kHz to 2000 kHz) input (SMA)
J15	1,6 2 3 4 5	AGND CBP LF_MF_INP LF_MF_INN CBN	RF	Connections for LF and MF band (150 kHz to 2000 kHz) differential inputs and capacitor bank.
J3	1 2	+5V 0V	DC DC	Input +5V supply Ground

Table 2 - PE0004 Host Interface

CONNECTOR PINOUT for J8				
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**	
1	IRQN	I/P	Interrupt Request	
2	RDATA	O/P	Reply Data (SPI/C-BUS)	
3	CDATA /SDA	I/P	Command Data (SPI/C-BUS)	SDA (I2C)
4	CSN	I/P	Chip Select	
5	SCLK / SCK	I/P	Serial Clock (SPI/C-BUS)	SCK (I2C)
6	RESETN	I/P	Hardware reset	Low to reset, pulled high by R10
7, 8	DGND	-	Connection to Digital Ground	
13	I2S SCLK/SCLK	O/P	I2S serial clock / SPI Serial Clock	
15	I2S FRAME/CS	O/P	I2S Frame / SPI CS	
17	I2S DATA/SDA	O/P	I2S Serial Data / SPI Data	
9, 10, 11, 12, 14, 16, 18	N/C	-	No Connection	
19, 20	DGND	-	Connection to Digital Ground	

Table 3 - Optional EV9180 Host Interface (not fitted as default)

CONNECTOR PINOUT for J9				
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**	
1	IRQN	O/P	Interrupt Request	
5	RESETN	I/P	Hardware reset	Low to reset, pulled high by R10
6	C-BUS_CSN	I/P	Chip Select	
9	C-BUS_CDATA /SDA	I/P	Command Data	
20	C-BUS_SCLK / SCK	I/P	Serial Clock	
21	C-BUS_CDATA /SDA	I/P	Command Data	Duplicate of pin 9
23, 26	DGND	-	Connection to Digital Ground	
27	C-BUS_SCLK / SCK	I/P	Serial Clock	Duplicate of pin 20
28	C-BUS RDATA	O/P	Reply Data	
36	I2S DATA/SDA	O/P	I2S Serial Data / SPI Data	
37	I2S FRAME/CS	O/P	I2S Frame / SPI CS	
38	I2S SCLK/SCLK	O/P	I2S serial clock / SPI Serial Clock	
40	3V3	-	Positive supply	
2, 3, 4, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 22, 24, 25, 29, 30, 31, 32, 33, 34, 35, 39	N/C	-	No Connection	

Table 4 - PE0004 Host /Interface DC connector

CONNECTOR PINOUT for J6			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
A/1	DGND_PE0004	Power	Connection to Digital Ground for PE0004
B/2	DGND_PE0004	Power	Connection to Digital Ground for PE0004
C/3	+5V_PE0004	Power	Connection to +5V supply from PE0004
D/4	+5V_PE0004	Power	Connection to +5V supply from PE0004
E/5	+5V_PE0004	Power	Connection to +5V supply from PE0004
F/6	+5V_PE0004	Power	Connection to +5V supply from PE0004

Table 5 – EV9180 Test Points

TEST POINTS		
Test Point Ref.	**Nominal Measurement**	**Description**
TP1	+1.2 V	VBIAS – internal bias voltage
TP2	+1.8 V	PLL_VDD – PLL LDO Output
TP3	+1.8 V	D_VDD – Digital circuits LDO Output
TP4	+1.8 V	ADC_VDD – ADC LDO Output
TP5	+2.7 V	IF_VDD – IF section LDO Output
TP6	+2.5 V	RF_VDD – RF section LDO output
TP7	0V	LF/MF signal input
TP8	0V	LF/MF signal input
TP9	+5.0 V	Input to voltage regulators
TP10	0V	-
TP11	0V	-
TP12	+3.3 V	U1 regulator output
TP13	+3.3 V	U5 regulator output (as built - adjustable)

Table 6 – EV9180 Test Loops

TEST LOOPS		
Test Point Ref.	**Default Measurement**	**Description**
TL1	0V	DGND – Digital ground
TL2, TL3, TL4	0V	AGND – Analogue ground

Table 7 – EV9180 Jumpers

JUMPERS		
Ref.	**Default Setting**	**Description**
JP1	1-2	3-way jumper to select power input. Fitting a jumper 1-2 selects input from screw terminal connector J3 Fitting a jumper 2-3 selects input from J6 (PE0004)
JP2	NF	Link to supply IO_VDD from regulator U1 (remove JP11). Allows current monitoring
JP3	Fitted	Link to supply AVDD from regulator U1 Allows current monitoring
JP4	NF	CLK_OUT /_EXT_LO_IN (measurement point)
JP5	NF	No user connection
JP7	NF	Fit to pull CSN high through R11 and select I2C control interface at power-up (not supported using PE0004).
JP8	NF	Fit to pull CDATA high through R12 for I2C control interface (SDA) (not supported using PE0004).
JP9	NF	Fit to pull SCLK high through R13 for I2C control interface (SCK) (not supported using PE0004).
JP11	Fitted	Link to supply IO_VDD from regulator U5 Allows current monitoring
JP13	NF	Pin header for LNA_FB output (measurement point)

Notes:

I/P	=	Input
O/P	=	Output
TL	=	Test Loop
TP	=	Test Point
NF	=	Not Fitted

6 Circuit Schematics and Board Layouts

For clarity, the circuit schematic diagrams are available as separate high-resolution files, which can be downloaded from the CML website. The layout on each side of the PCB is shown in Figure 5 and Figure 6.

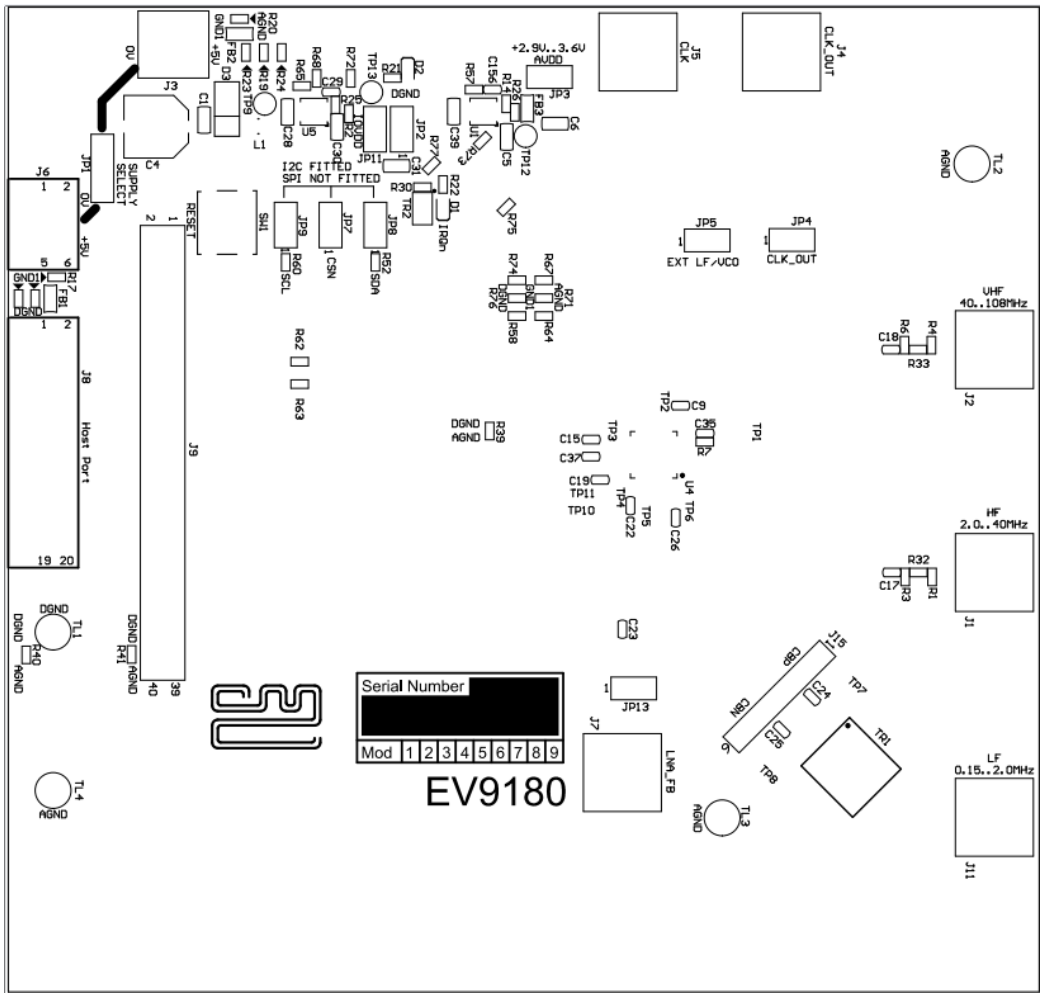


Figure 5 - PCB Layout: Top

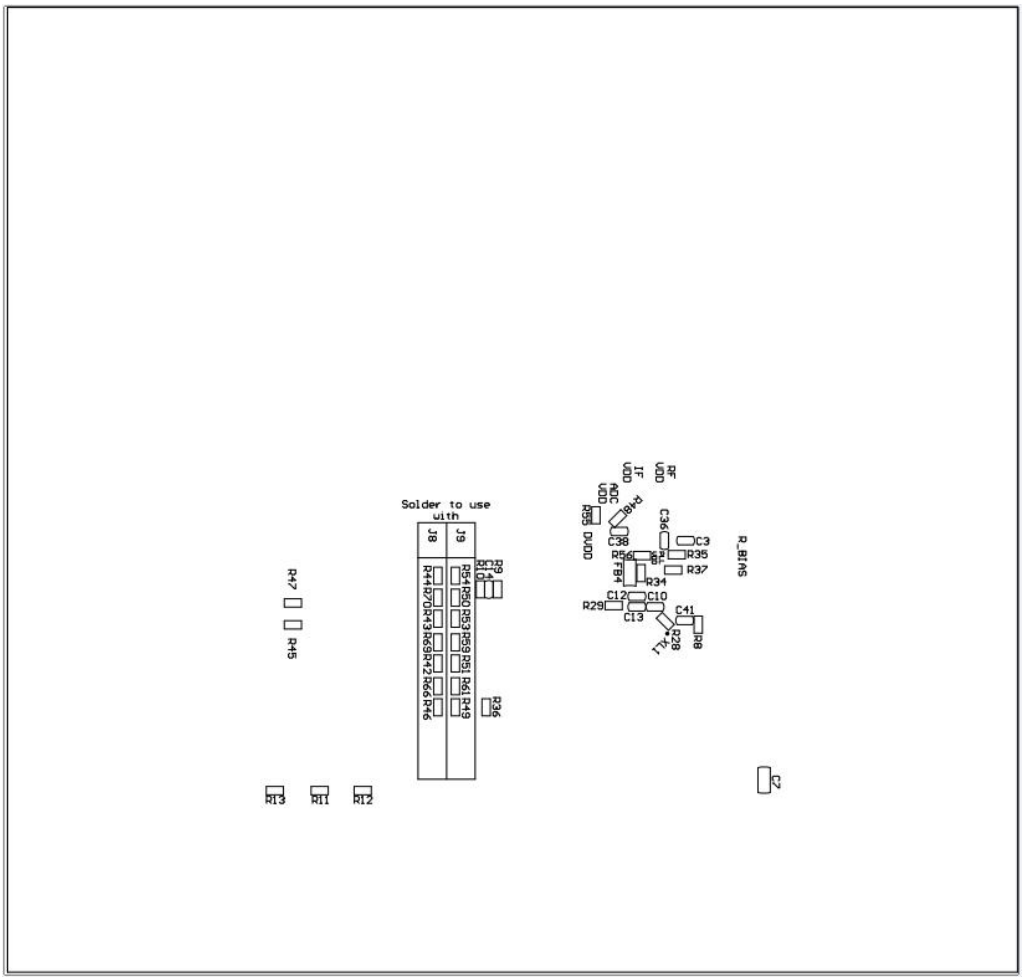


Figure 6 - PCB Layout: Bottom

7 Detailed Description

The EV9180 serves as an evaluation platform for the CMX918 (U4), a 40-lead VQFN device.

EV9180 functionality includes:

- RF input between 150 kHz and 108 MHz in 3 ‘bands’
- On-chip VCO and 16 / 24-bit Fractional-N PLL, providing the Local Oscillator
- Reference crystal at 38.4 MHz (XL1)
- USB Interface via a PE0004 Controller to a CML PC GUI, allowing device control, graphical output of the IQ data and capture of output data

7.1 Hardware Description

Full details of the device functionality are contained in the CMX918 datasheet. The EV9180 is assembled on a 115 x 112 mm, 1.6 mm thick 4-layer PCB (PCB reference PCB779D), using an FR4 / VT481 2116 dielectric.

The layout has been optimised for low ground impedance and short RF tracking for operation at high frequencies. Datasheet, user manual, Gerber files and a Bill of Materials can be downloaded from the CML website (Home | CML Micro) on the CMX918 product page.

The RF input is automatically selected via the CMX918 Fc registers; inputs J1 (HF bands, 2 to 40 MHz) and J2 (VHF, 40 to 180 MHz) are nominal 50 Ω impedance. Each input can be considered as a PI network with a 0 Ω through connection as default and a dc block. The input circuits may then be modified to become filters or attenuators to suit the user.

RF input J11 provides a low impedance input to the balanced high impedance LF/MF band (150 kHz to 2000 kHz) CMX918 inputs via transformer TR1 (Coilcraft 36:1 ratio transformer, part number WB36-1SL) and dc blocking capacitors C24 and C25. Removing these capacitors provides direct access to the high impedance inputs via J15, which also allows connection to the on-chip tuning capacitor bank. An area free of ground is provided along the bottom edge of the board, along with a strip of holes, where the user may mount a ferrite rod antenna for use with the LF/MF input.

A test output from the LF/MF LNA stage can be enabled to output at J7 / JP13 if necessary.

The CMX918 contains a 16- or 24-bit Fractional-N PLL synthesiser used with the on-chip VCO to provide the receiver local oscillator. A configurable loop filter is internal to the IC. Optionally, an external LO input may be applied to J4 / JP4.

XL1 is a low phase noise 38.4 MHz crystal, part number **MP10435**, supplied by Techpoint Golledge (www.golledge.com). This is used as a reference source for the PLL within the CMX918 and as the master ADC and Digital Processing Block clock source. Capacitors internal to the CMX918 provide fine adjustment of the crystal oscillator frequency. A higher stability or accuracy 38.4 MHz reference may be required for demanding applications and may be applied via J5 after circuit modifications (see Table 8). Note that other reference frequencies are not supported.

SPI/C-BUS control of the CMX918 registers is by default via connector J8 (the host port). The streaming digital IQ baseband outputs are available via I2S data, clock and frame signals. By default, these are also routed to the host connector J8. These are intended for use by the PE0004 host controller. Alternatively, all these signals may be connected by rearrangement of links to J9 to a different host and demodulation platform.

An IRQ interrupt indicator is provided by D1 (the red LED ON indicates IRQn is low) and a hardware reset can be activated by pressing the push button SW1. This pulls the RESETN pin low with the parallel capacitor charge time providing a suitable delay.

7.2 Power Supplies

The input to the PCB is nominally 5.0 V applied to J3 or alternatively J6 (PE0004 power supply) via selection link JP1. Reverse polarity protection is provided by D3. On-board regulators are provided to generate the 3.3 V analogue and 3.3 V IO (optionally 1.8 V supply via resistor changes on U5) supplies used by the CMX918. A green LED on the digital supply (D2) confirms that power is correctly applied.

7.3 Adjustments and Controls

The only user hardware controls on the board are the ability to:

- Selection of the on-board voltage regulator supplies via JP3 and JP2 or JP11. These allow for current monitoring in place of the jumper links
- Application of an external higher stability 38.4 MHz frequency reference (via J5 and fitting associated components), disabling the on-board crystal oscillator (XL1, see Table 8 below)
- Alternative routing of control and data outputs between J9 (default DNF) and J8 connectors via link resistors (refer to schematic)
- LF/MF inputs - by removing C24 and C25, the high impedance inputs of the CMX918 may be accessed, along with the on-chip tuning capacitor bank, via J15. This connector may be used with a ferrite rod antenna rather than the 50 Ω input at J11 (refer to CMX918 datasheet)

All other control is via SPI/C-BUS control of the CMX918 and the ES9180 GUI described in the next section.

Table 8 - Reference source configuration

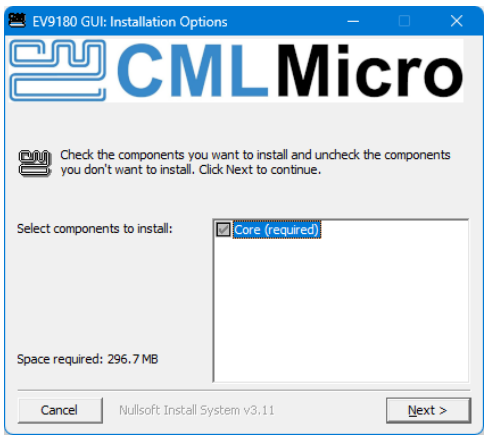
Reference	XL1	C12	R28
XL1 (Default)	Fit	DNF	DNF
External Via J5	DNF	Fit 1nF	Fit 0R

7.4 Software Description - ES9180 Graphical User Interface

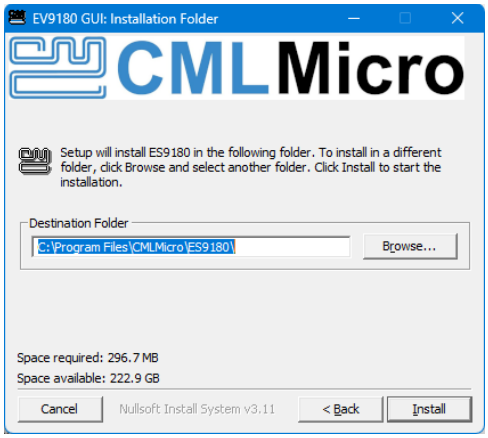
7.4.1 GUI Installation

When the ES9180xx.exe installer is run, verification warnings may appear. Click ‘Run’ / ‘Yes’.

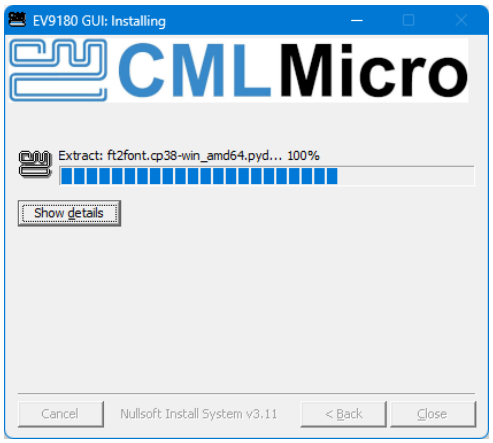
The GUI installation options window will then appear. Check the space required, then click ‘Next’.



Choose the required installation folder, then click ‘Install’.



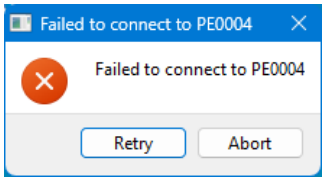
If a previous version has been installed, a prompt asks if you wish to uninstall that version ('No' exits installation). A bar then display the installation progress, with an option to show details.



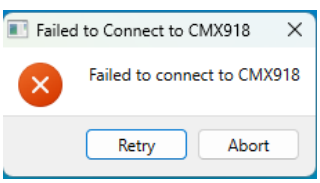
Once this shows 'Completed', click 'Close'. Prompts will first ask for permission to create a desktop shortcut, then if you want to run the program now. This will then start the GUI software, running ES9180xx.exe.

7.4.2 GUI Introduction

The GUI is started by running ES9180xx.exe. A blue box will appear briefly during initialisation followed by the main GUI window. If power is not applied to the PE0004, or its USB is not connected, the following warning will appear.



There is also a warning presented to the user if the PE0004 is powered and connected to the system, but the CMX918 is not detected.



Located top left of the main GUI window, a drop-down ‘File’ menu button allows for setting states to be stored and re-loaded, with a choice of file name. An ‘Options’ button allows for control of the SPI/C-BUS speed, and ‘Help’ will show the version of the ES9180 software in use.

Control of the CMX918 is split across tabs in the GUI for ease of use, grouping related functions. Two tabs, Time and FFT, allow visual analysis of the data and export to other applications.

At the bottom of the window, buttons allow options to write or read all registers, to Auto Write value changes and Poll Enabled (reads back registers continually). There is also a soft reset button.

7.4.3 The General Tab

This tab contains the essential configuration fields for operation of the device, for example standby /operational modes, operating frequency, IF and bandwidth selection. It includes basic controls and indicators for the PLL and a read back of the Received Signal Strength Indicator (RSSI) as a decimal value and converted to dBm.

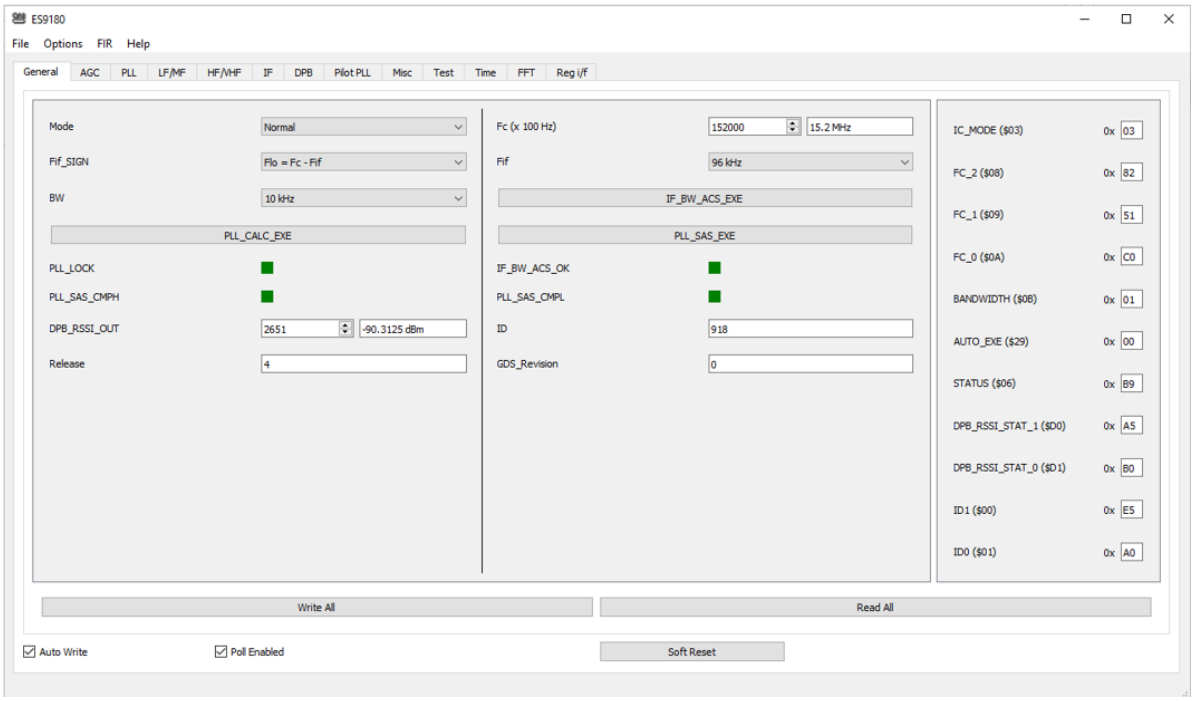


Figure 7 - General Tab

7.4.4 The AGC Tab

This tab contains the Automatic Gain Control (AGC) configuration fields for operation of the device. Specific controls for AGC in a particular band are covered in other tabs.

7.4.5 The PLL Tab

This tab contains configuration controls for the PLL, including the reference mode and crystal capacitor bank adjustment. The results of auto calculation from the frequency entry are shown, along with fields for manual entry of the PLL N, F, R and LDIV values. Indicators are shown for PLL Lock, as well as visual status of the VCO Sub-band Auto Select (SAS) comparators.

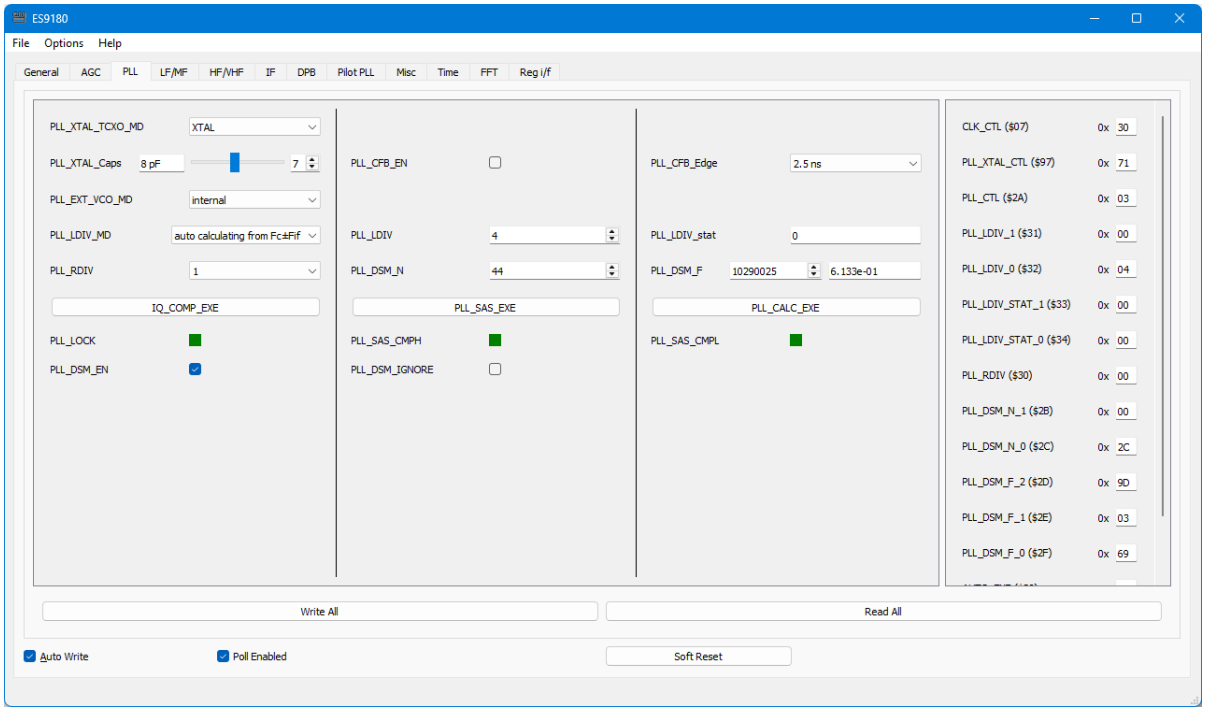


Figure 8 - PLL Tab

7.4.6 The LF/MF Tab

The LF/MF tab incorporates controls and status information on the LF/MF input 150 kHz to 2000 kHz signal path, its gains and AGC system, as well as the capacitor bank value intended for tuning a ferrite rod antenna.

7.4.7 The HF/VHF Tab

The HF/VHF tab incorporates controls and status information on the HF (2 - 40 MHz) and VHF (40 – 108 MHz) input signal paths, its gains and AGC system.

7.4.8 The IF Tab

The IF tab incorporates controls and status information on both the I and Q channel Intermediate Frequency signal paths, their gains and AGC system, as well as a function for calibrating the IF filters.

7.4.9 The DPB Tab

The Digital Processing Block (DPB) tab incorporates controls and status information for the gains, IQ corrections and output data format selections.

7.4.10 The Pilot PLL Tab

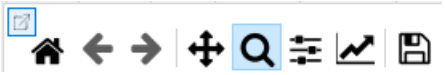
This tab controls a secondary integer-N PLL which may be used to generate internal test (‘Pilot’) signals for calibration of the I and Q channels to maximise image rejection within the Digital Processing Block. Use of this function however is optional as an in-built routine within the CMX918 can adjust the I and Q amplitude and phase balance continuously and automatically. Refer to the CMX918 datasheet for further details.

7.4.11 The Misc Tab

The Miscellaneous tab contains controls for the IRQ mask and slew rate of the I2S and SPI/C-BUS output signals from the CMX918. The use of the slew rate control on these signals can reduce the effects of harmonics, impairing RF reception.

7.4.12 The Time Tab

The Time tab can be used to continuously display the output data in a time domain format. Both I and/or Q data can be displayed, and the X and Y scales, view etc can be adjusted using the controls top left.



From left to right, these controls can be used to:

- Pop Out – moves the tab out to a separate sub-plot window. This can then be used to see how adjustment of other controls affects the received signal. Once in a separate window, the Pop In button can be used to return the display to the tabs
- Home – Resets the original view
- Left Arrow – Return to previous view
- Right Arrow –Forward to next view
- Crossed Arrows – Left button pans, right button zooms, X/Y fixes the axis, CTRL fixes the display aspect.
- Magnifying Glass – Zoom to rectangle, X/Y fixes axis
- Horizontal Sliders – Configures sub-plots
- Graph Arrow – Edits Axis, curve and image parameters
- Save – Pops up a file browser window, allowing image capture of the graph to a file location with a choice of file formats. Note that this applies for the graph only, and to save peripheral data like markers, cursor position, etc. a screenshot should be used

The data can also be saved as either .csv or .wav formats. A value can be entered for the number of samples to be saved. Clicking 'Select file' displays a dialogue box enabling the file location, name and type to be selected, after which 'Save' saves the file. The default storage location is the folder into which ES9180 has been installed.

If storing as a .wav file, a sufficiently large number of samples should be captured if further signal processing is contemplated. At an export rate of 96 ks/s for example, 25600 samples is only 0.26 seconds.

7.4.13 The FFT Tab

The FFT tab can be used to continuously display the output data in a frequency domain format. Both I and/or Q data can be displayed, and the X and Y scales, view, etc can be popped out, adjusted, etc. using the controls top left as per the Time tab. The image can also be saved, as described in the Time tab. To also save data like the marker table, a screenshot should be used. Trace averaging can be selected (bottom right) with an adjustable count to a maximum value of 100. Markers can be applied, including peak search and delta marker functions.

To add a marker, click the 'Add Marker' button; this will create marker M0. A frequency for the marker can be added in the X value field, or peak search clicked to find the peak value. To add a delta marker, click 'Add Marker'; this will be M1. The mode can be changed by double clicking in the 'Mode' box of the marker table and selecting 'Delta' from the drop-down selection. The reference for delta mode can be selected by double clicking in the 'Ref' box and selecting M0 from the drop-down menu. The offset frequency can then be set in the X field of the marker table, the Step Up/Down buttons. or again a peak / next peak Left /Right search used. The frequency and amplitude offsets between M0 and M1 are then displayed in the marker table.

Markers

	X	Y	Trace	Label	Mode	Ref
0	1.945 k	−30.626	I	M0	Normal	
1	Δ 1.500 k	Δ −59.407	I	M1	Delta	M0
2	3.900 k	−86.087	I	M2	Normal	

Figure 9 - Example FFT marker table

Markers can also be moved along the X axis using the Step Down and Step Up buttons, with a configurable step size above.

7.4.14 The Reg i/f Tab

This Register Interface tab can be used to read or write data to the CMX918 registers. Consult the CMX918 register description for detailed information on the register map and its operation.

7.5 Application Information

7.5.1 Typical Performance

Using the FFT and time domain output on the ES9180 graphic user interface the following data was obtained. Typically averaging has been applied and a value of 10 used.

- MF Performance

CW Input Frequency – 1000 kHz + 2kHz, results in 2 kHz output tone
Input Signal level - -90 dBm
Channel BW – 10 kHz
Output CNR ~ 64 dB
Output relative to full scale ~ -12 dBFS
Sample value ~ +/- 7000 pp

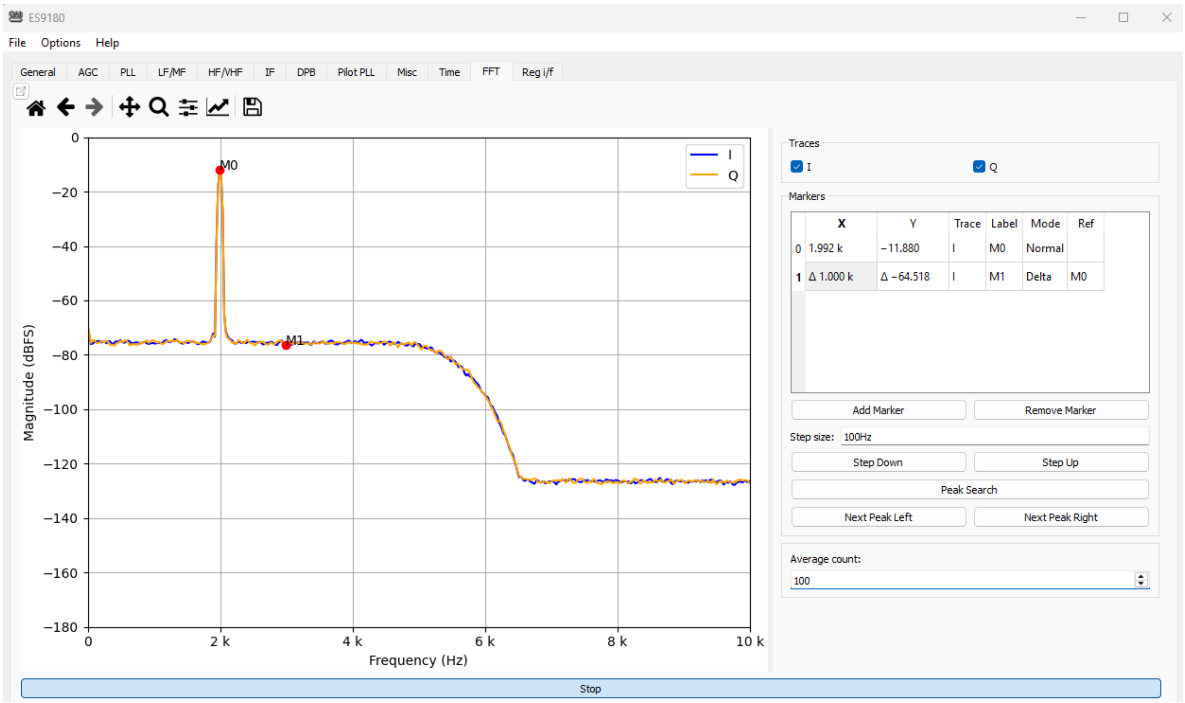


Figure 10 - MF Typical Performance at 1000 kHz (offset + 2 kHz), -90 dBm CW input, FFT Output. Delta marker shows Carrier to Noise Ratio (CNR). Average count = 100.

Note that the MF output is higher than the HF output (below) for the same input signal level due to the MF IC input being high impedance and the voltage magnification of the step-up transformer TR1.

- HF Performance

CW Input Frequency – 15.200 MHz + 2kHz, results in 2 kHz output tone
Input Signal level - -90 dBm
Channel BW – 10 kHz
Output CNR ~ 59 dB
Output relative to full scale ~ -29 dBFS
Sample value ~ +/- 1000 pp

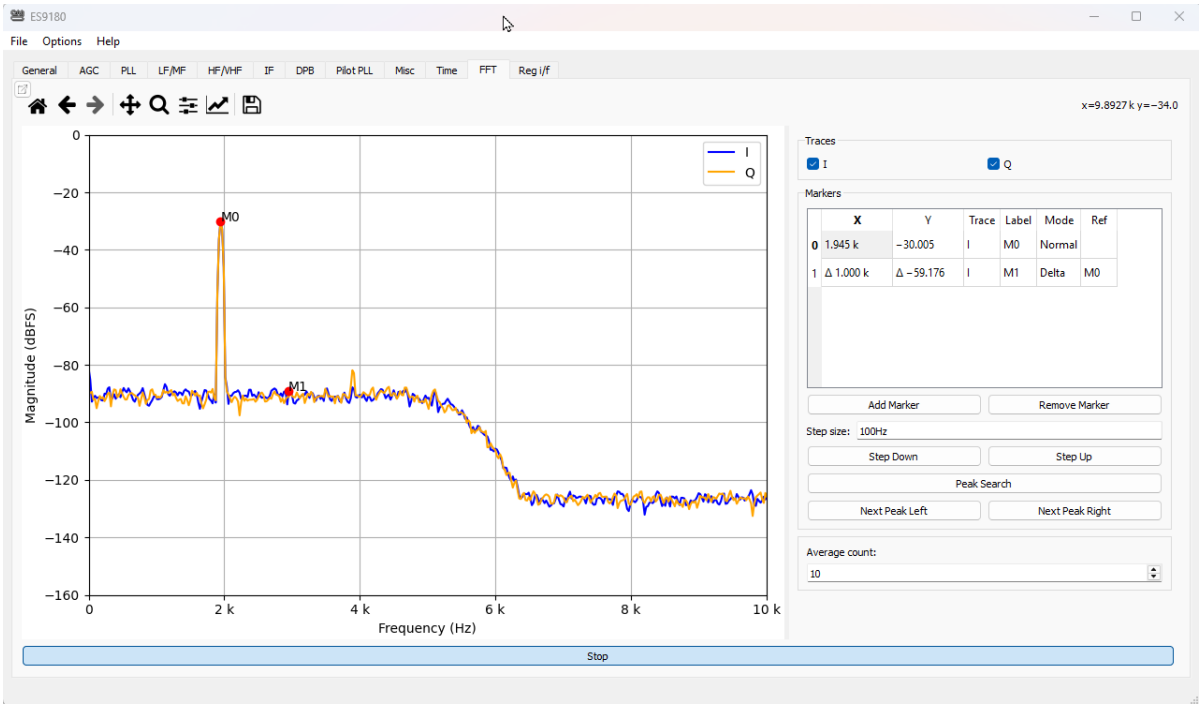


Figure 11 - HF Typical Performance at 15.200 MHz (offset + 2 kHz), -90 dBm CW input, FFT Output

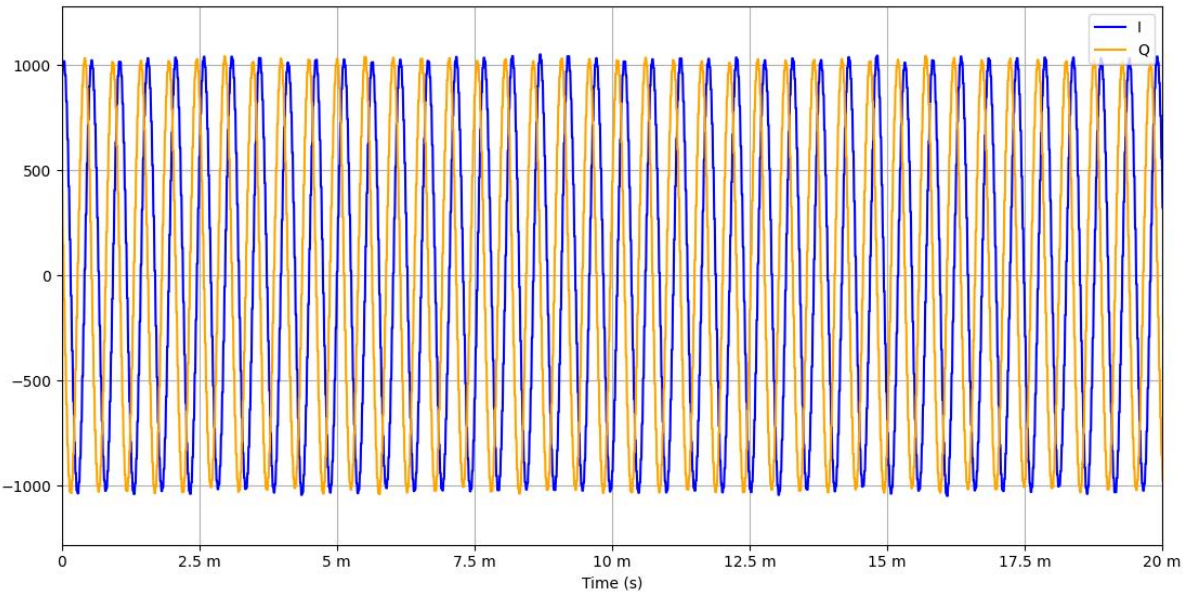


Figure 12 - HF Typical Performance at 15.200 MHz (offset + 2 kHz), -90 dBm CW input, Time domain IQ Output

- VHF Performance

  CW Input Frequency – 98.500 MHz + 10 kHz, results in 10 kHz output tone
  Input Signal level - -90 dBm
  Channel BW – 100 kHz
  Output CNR ~ 42 dB
  Output relative to full scale ~ -29 dBFS

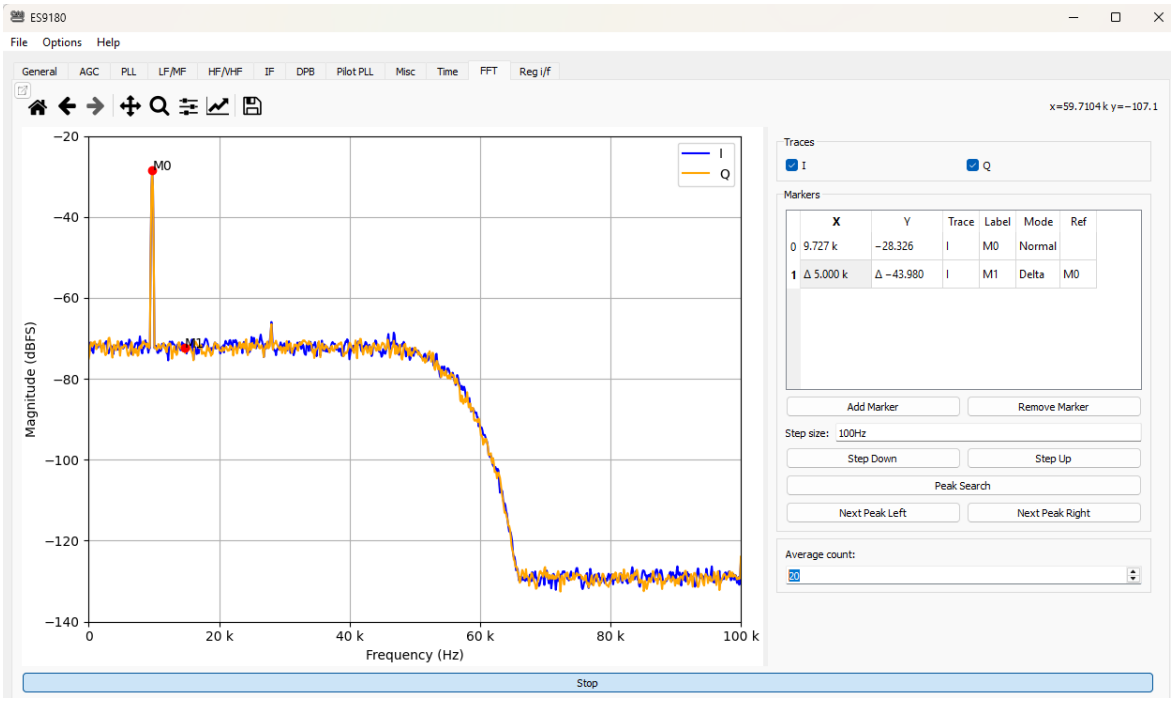


Figure 13 - VHF Typical Performance at 98.50 MHz (offset + 10 kHz), -90 dBm CW input, FFT Output

7.6 Troubleshooting

The CMX918 is a complex RF and baseband system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the CMX918 datasheet, register description, this user manual and the associated schematics and layout drawings carefully when troubleshooting.

This section provides some suggestions to help users resolve application issues they might encounter.

Error Observed	Possible Cause	Remedy
ES9180xx.exe software fails to run correctly	PE0004 / EV9180 not powered up at start up	Ensure +5.0 V supply is provided to both the PE0004 and EV9180 with the appropriate current limit
	Incorrect software for the PE0004	Contact techsupport@cmlmicro.com
	Incorrect connection	Ensure that EV9180 J8 is connected to the PE0004 HOST port J6 (not the C-BUS-1 or -2 connectors).
PLL fails to lock	Reference not applied	Check power is applied and that the control interface is functional. Check the crystal operation mode has been enabled. If an external reference has been selected, check the signal path has been modified (fitting C12 and R28 as Table 8) and the level at CMX918 pin 12.
Signals not observed at the output (Time or FFT tabs)	Break in the signal path	Check that the signal is of sufficient level and is applied to the correct SMA input on the EV9180.
	Incorrect input signal frequency	Check that the CMX918 is tuned to the correct frequency for the input signal, that PLL_CALC_EXE has been actioned, and that the PLL is locked. Ensure that a small frequency offset is applied (e.g. 2 kHz) to the Rx input signal. Ensure that EV9180 J8 is connected to the PE0004 HOST port J6.

Table 9 - Possible Errors

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (V_{IN} - V_{SS})	+3.5	+6.0	V
Current into or out of V_{IN} and V_{SS} pins	0	1.0	A
Current into or out of any other connector pin	-20	+20	mA
Maximum RF Input Level		+10	dBm

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Min.	Typ.	Max.	Units
Supply (V_{IN} - V_{SS})	4.8	5.0	6.0	V
Xtal/External Clock Frequency		38.4		MHz
Ambient Operating Temperature	+10		+40	degs C

8.1.3 Operating Characteristics

Example conditions:

For the following conditions unless otherwise specified:
Xtal Frequency = 38.4 MHz, V_{IN} = 5.0 V, T_{AMB} = +25 °C.
Normal Mode.

	Notes	Min.	Typ.	Max.	Units
MF Performance @ 1000 kHz, -90 dBm IP					
Output Level			-12		dBFS
Output CNR			64		dB
HF Performance @ 15.200 MHz, -90 dBm IP					
Output Level			-29		dBFS
Output CNR			59		dB
VHF Performance @ 98.5 MHz, -90 dBm IP					
Output Level			-29		dBFS
Output CNR			42		dB

Contact information

For further information please contact your local CML sales representative.
Contact details can be found at www.cmlmicro.com