CMX918
Low Power SDR Tuner

Low Power Software Defined Radio (SDR) Tuner

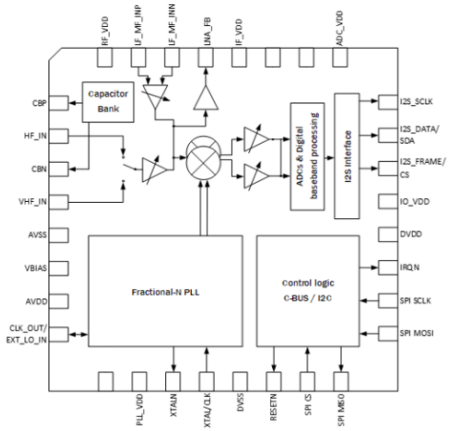
D/918/2.0 January 2026 **DATASHEET** Provisional

Features

- **Low power multi-mode SDR Tuner**
- **Tuning Range 150 kHz to 108 MHz**
- **LF/MF/HF/VHF band optimised RF inputs**
- **High spurious free dynamic range tuner**
- **Analogue and Digital Modulation support**
- **Software configurable autonomous AGC**
- **Integrated VCO with low phase noise and fast lock**
- **Low-IF architecture**
- **Selectable optimised IF bandwidths**
- **Standard digital interfaces (SPI, I2C, I2S)**
- **5 x 5mm VQFN32 package for low-cost PCB design**
- **2.9 V to 3.6 V supply**

Applications

- **Battery-powered SDR receivers**
- **IF processor for professional receivers**
- **Smartphone accessories**
- **In-car entertainment**



1 Brief Description

The CMX918 is a flexible RF Front-End Processor designed for small form factor, low-power software-defined radio (SDR) receiver solutions. Supporting a very wide frequency range from LF through to VHF Band II, the device is suitable for a diverse range of analogue and digital communication applications.

The processor offers general coverage operation from 150 kHz to 108 MHz, featuring frequency-optimised front-end inputs and a highly configurable receive path. Key features include variable gain settings, adjustable IF bandwidths, and programmable IF centre frequencies. This level of configuration allows the device to be precisely tailored to various air interfaces and challenging RF environments. External component requirements are kept to a minimum. Support for Ferrite rod antennas is provided for the LF and MF bands.

The CMX918 is designed to provide robust 'real-world' signal reception. The device's digital output is ready for further processing by a suitable DSP or FPGA platform, which implements the specific demodulation, protocol decoding, and audio processing functions required by the application. This architecture is ideal for SDR implementation, allowing for reception modes such as AM, FM, DRM, DRM+, as well as specialised protocols like SSB, NAVDAT, and others, to be implemented purely in software. A compact, versatile, high-performance, low-power receiver with extended battery life can therefore be realised at low cost.

Programmable power management is included to allow unused circuit blocks to be power saved when not in use, effectively minimizing overall current consumption for extended battery life. The CMX918 is controlled and programmed via a serial port which can be operated as either the industry-standard I^2C or SPI/C-BUS. The device operates from a single supply of 2.9 to 3.6 V and is supplied in a 32-pin VQFN package with a central ground tab.

Contact CML Sales (cmlmicro.com) for access to additional documentation describing the device register settings.

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Version	Changes	Date
1.0	First full release – Provisional Information	December 2023
2.0	Updated for product launch	January 2026

2 Recommended External Components

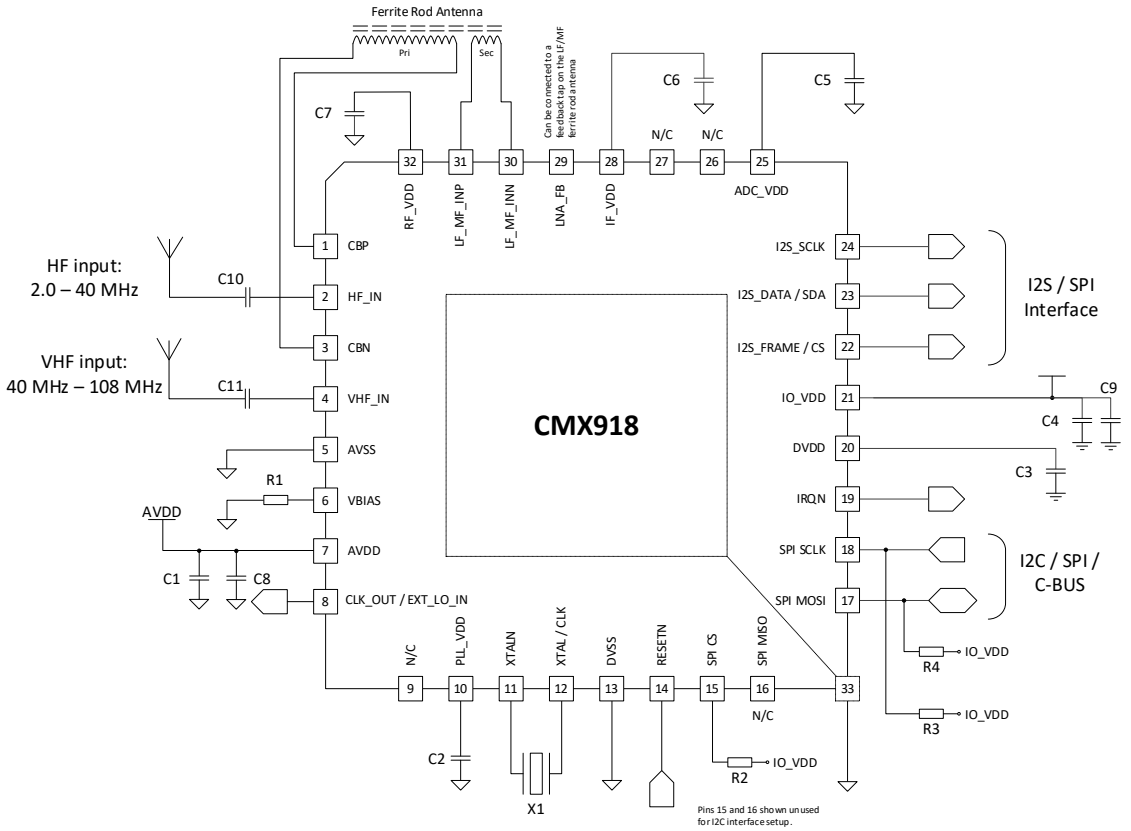


Figure 1 - CMX918 Recommended External Components

Table 1 - Recommended External Components (typical example)

Component	Value	Tolerance	Notes
C1	10 nF >10 V X7R	±10 %	AVDD Supply voltage filter capacitor
C8	1 µF >10 V X5R	±10 %	AVDD Supply voltage filter capacitor
C2	1 µF >10 V X5R	±10 %	PLL_VDD LDO regulator filter capacitor
C3	1 µF >10 V X5R	±10 %	DVDD LDO regulator filter capacitor
C4	10 nF >10 V X7R	±10 %	IO_VDD Supply voltage filter capacitor
C9	1 µF >10 V X5R	±10 %	IO_VDD Supply voltage filter capacitor
C5	1 µF >10 V X5R	±10 %	ADC_VDD LDO regulator filter capacitor
C6	1 µF >10 V X5R	±10 %	IF_VDD LDO regulator filter capacitor
C7	1 µF >10 V X5R	±10 %	RF_VDD LDO regulator filter capacitor
X1	38.4 MHz	±20 ppm *	38.4 MHz GSX-223/X SM Crystal 6 pF MP10435
R1	61.9 kOhm	± 1 %	Reference resistor
R2	47 kOhm	± 1 %	Pull-up resistor
R3-R4	4.7 kOhm	± 1 %	Pull-up resistor
C10	100 nF >16 V X7R	± 10 %	HF input dc blocking capacitor
C11	22 nF >16 V X7R	± 10 %	VHF input dc blocking capacitor

Notes (applicable to Figure 1 / Table 1):

1. X1 can be a crystal or an external clock source (e.g. TCXO); this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, operation with a 38.4 MHz crystal is selected.
2. Crystal oscillator tolerance depends on demodulator requirements
3. The above shows connections for I2C control mode. For SPI / C-BUS operation, omit R2, R3 and R4. Pins 15 & 16 are then also included in the control interface.
4. Nominal values of pull up resistors R3-R4 depend on the total capacitance on the bus and operating frequency.
5. Recommended R & C component size is 0402 (Imperial).
6. For the parallel combinations of C1/C8 (AVDD) and C4/C9 (IO_VDD), the smaller value should be located closest to the IC pin. It is recommended that a larger bulk decoupler (>10 µF) is also implemented on each of these supplies (i.e. at the output of a voltage regulator).
   Pins 5 and 33 (Centre tab, AVSS) must both be connected to analogue ground in the PCB layout. They are not connected together within the CMX918.

3 Pin and Signal List

Pin No.	Signal Name	Type	DC level (V)	Description
1	CBP	AO	-	Capacitor bank positive output
2	HF_IN	AI	0.8	HF band amplifier input
3	CBN	AO	-	Capacitor bank negative output
4	VHF_IN	AI	0.8	VHF band amplifier input
5	AVSS	G	0	The negative supply rail (ground) for the analogue on-chip circuits
6	VBIAS	AO	1.2	External reference resistor connection for generating reference currents for internal blocks
7	AVDD	P	3.3	The positive 3.3 V supply rail for the analogue on-chip circuits. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
8	CLK_OUT /EXT_LO_IN	AIO	-	Clock frequency output (19.2 MHz) / Input for external LO or VCO
9	N/C			Not connected
10	PLL_VDD	P	1.8	Fractional-N PLL LDO output voltage to external filtering capacitor
11	XTALN	AIO	0.7	The output of the on-chip crystal oscillator inverter.
12	XTALP/CLK	AIO	0.7	The input to the oscillator inverter from the crystal circuit or external clock source.
13	DVSS	G	0	The negative supply rail (ground) for the digital on-chip circuits.
14	RESETN	DI	-	Chip reset to default state (pull low for > 1µs to 'reset') Requires external pull-up to IO_VDD
15	SPI CS	DI	-	SPI chip select (active low), used to enable an SPI data read or write operation on the chip. Pull high at start-up for I2C port operation
16	SPI MISO	DO	-	SPI serial data 3-state output to host
17	SPI MOSI	DIO	-	SPI serial data input from the host / I2C data input / output.
18	SPI SCLK	DI	-	SPI clock input from the host / I2C clock input.
19	IRQN	DO	-	Interrupt Request (active low). This is driven high internally to IO_VDD.
20	DVDD	P	1.8	Digital circuits LDO output voltage to external filtering capacitor
21	IO_VDD	P	1.8 – 3.3	Supply to SPI / C-BUS / I2C digital interface circuits

Pin No.	Signal Name	Type	DC level (V)	Description
22	I2S_FRAME / CS	DO	-	Data Interface: I^2S frame output / SPI master chip select output
23	I2S_DATA / SDA	DO	-	Data Interface: I^2S data output / SPI master data output
24	I2S_SCLK	DO	-	Data Interface: I^2S clock output / SPI master clock output
25	ADC_VDD	P	1.8	ADC LDO output voltage to external filtering capacitor
26	N/C			Not connected
27	N/C			Not connected
28	IF_VDD	P	2.7	IFA LDO output voltage to external filtering capacitor
29	LNA_FB	AO	1.5[1]	LF / MF amplifier feedback
30	LF_MF_INN	AI	1.5	LF / MF band amplifier input – negative
31	LF_MF_INP	AI	1.5	LF / MF band amplifier input – positive
32	RF_VDD	P	2.5	LNA & Mixer LDO output voltage to external filtering capacitor
33 (central metal pad)	AVSS	G	0	Analogue ground

Key: AI – analogue input; AO – analogue output; AIO – analogue input/output; DI – digital input; DO – digital push/pull output; DIO – digital input/output; D/AO – digital/analogue output; P – power; G – ground.

[1] If RF_LNA_FB_EN = “1” and RF_LNA_FB_MUX= “0”

4 Functional Description

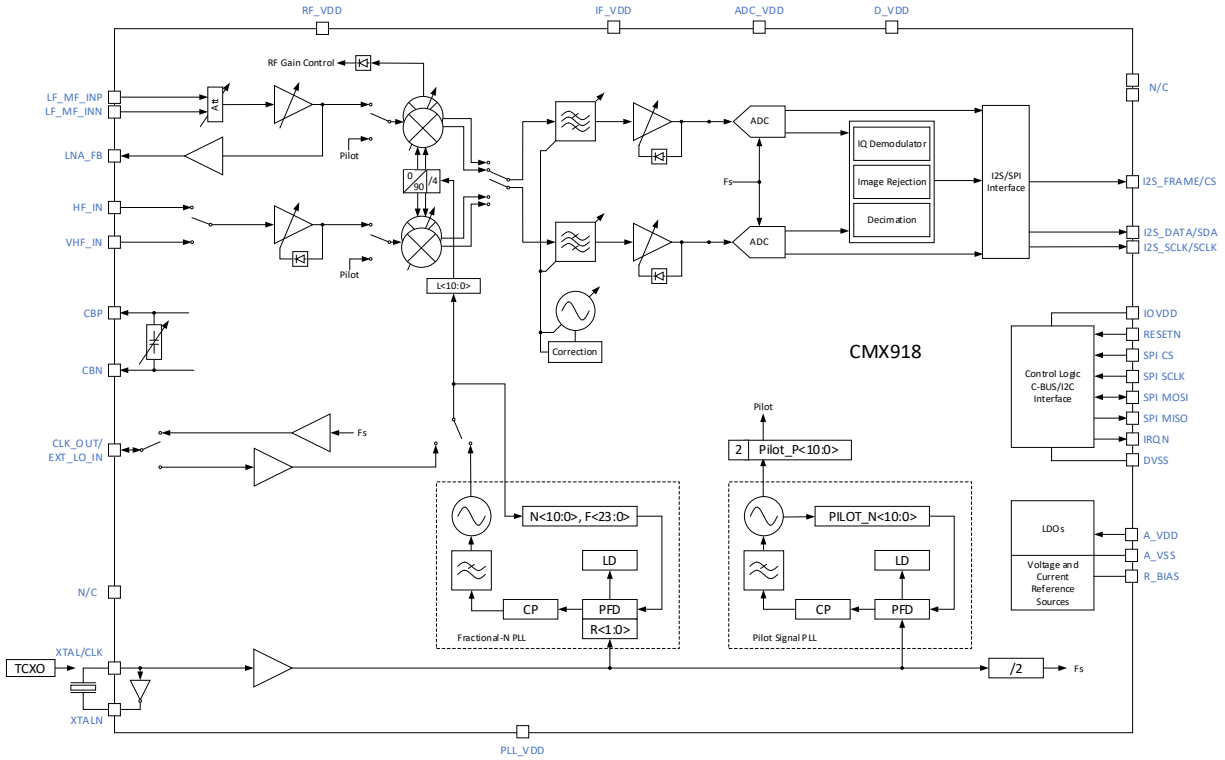


Figure 2 - Block Diagram

The CMX918 tuner IC includes the following functional blocks: -

Separate signal inputs with configurable gain settings / AGC for

- LF/MF (150 kHz to 2 MHz) operation (high impedance)
- HF (2 to 40 MHz)
- VHF (40 to 108 MHz)

Frequency mixers convert the signal to a low-IF (96 or 120 kHz) as I/Q channels.

The RF, IF and mixer stages again have configurable gain settings / AGC and filtering.

The IQ channels are then sampled by ADCs after which there is further channel filtering and signal processing within in the Digital Processing Block (DPB). The DPB provides a number of features such as RSSI and IQ image rejection optimisation. The signal is converted to digital baseband (zero IF) IQ outputs for further processing and demodulation by an external processor. The digital baseband signal data interface is configurable, further information on this interface can be found in section 4.8.2.

An on chip, flexible fractional-N PLL and VCO provide the receive local oscillator including automatic calibration and spur avoidance functions. A separate integer-N 'Pilot' PLL may be used to generate test signals.

A reference input supports either crystal (default) or TCXO operation.

On-chip voltage regulators are provided for each system block for low noise operation and minimising external component count.

The IC is highly configurable via the control logic block, providing multiple control and monitoring functions via the extensive register functions. Basic operation however requires few register writes.

4.1 Modulation Modes

The CMX918 supports multi-mode operation, including AM and all the modes of DRM30, via its digital baseband output. In addition, WBFM (including Stereo-WBFM, RDS etc.) and DRM+ are supported at VHF.

The receiver RF front ends (LNA + IQ Mixer) are followed by low-IF filters and programmable gain amplifiers (IFPGA) centred on either 96 kHz or 120 kHz. Suggested options are:

Table 2 - IF Modes

Mode	IF Frequency (kHz)	Filter bandwidth (kHz)
AM / DRM30	96	5/10/20
AM / DRM30	120	5/10/20
FM / DRM+	96	100
FM / DRM+	120	100
Analogue WBFM	120	200

When used in DRM30 and DRM+ broadcasting applications, a choice of different bandwidths are available:

- LF/MF 4.5 kHz – Allows a simulcast with the lower-sideband of a 9 kHz raster channel used for AM, with a 4.5 kHz DRM signal occupying the area traditionally taken by the upper-sideband
- LF/MF 5 kHz - Allows a simulcast with the lower-sideband of a 10 kHz raster channel used for AM, with a 5.0 kHz DRM signal occupying the area traditionally taken by the upper-sideband
- LF/MF 9 kHz – DRM uses a standard bandwidth of an ITU region 1 or 3 broadcast channel, may be used as digital only or with an analogue simulcast
- LF/MF 10 kHz- DRM uses a standard bandwidth of an ITU region 2 broadcast channel, may be used as digital only or with an analogue simulcast
- HF 10kHz DRM uses a full worldwide broadcast channel on a 5kHz channel raster
- LF/MF 18 kHz - a double bandwidth region 1 or 3 channel, offers highest audio quality (for DRM30) and multichannel broadcast ability
- LF/MF 20 kHz - a double bandwidth region 2 channel, offers highest audio quality (for DRM30) and multichannel broadcast ability
- VHF 100 kHz for DRM+ allows four multiplexed audio channels or one low-definition video channel
- VHF 200 kHz - analogue FM. The channel is capable of supporting Stereo WBFM, RDS and any other sub-carrier information systems deployed in legacy broadcasting systems on VHF around the world.

The CMX918 supports 5, 10, 20, 100 and 200 kHz bandwidths. 4.5, 9 and 18 kHz channels require additional digital filtering to be implemented in the external DSP or baseband demodulation system.

4.2 RF Path

The RF path is intended to receive signals at LF, MF, HF and VHF bands using three inputs:

- A differential, high impedance input for the LF/MF bands (LF_MF_INP, LF_MF_INN inputs)
- An HF band input (HF_IN)
- A VHF band input (VHF_IN).

The HF and VHF bands share the same LNA and mixer but have switched RF inputs. The correct input is selected automatically from entry of the wanted receive frequency, though this can also be manually controlled. The subsequent IF path is then common regardless of operating frequency.

4.2.1 LF / MF Path

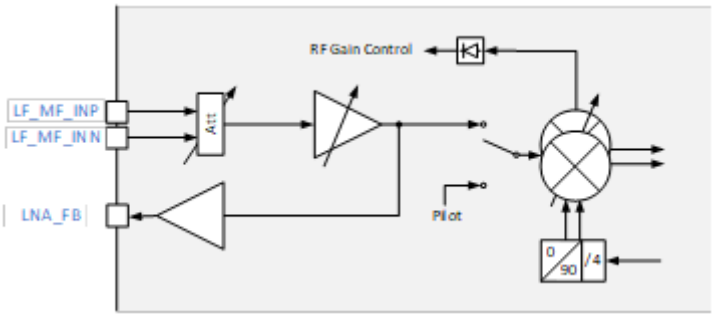


Figure 3 - LF/MF Input Path

The LF/MF RF path consists of following sections:

- LF/MF band LNA attenuator
- LF/MF band LNA
- LF/MF band LNA feedback follower
- LF/MF band quadrature Mixer
- LF/MF band AGC detector
- LF/MF band LO quadrature formers and LO buffers

Each stage in the LF/MF path has switchable gains, as a result there are wide opportunities for optimising the gain/noise/linearity. An attenuator is available at the input of LNA which extends gain control range in the low gain region. An integrated AGC loop can be widely configured in both the amplitude and time domain. Each block can be individually set to automatic or manual control mode (refer to the register description).

An embedded tuneable capacitor bank is intended to tune an external resonant ferrite rod antenna, as an alternative to using the broadband feedback winding configuration. This capacitance is connected between outputs CBP and CBN. The LF/MF LNA is designed with a high input impedance.

4.2.2 HF / VHF Path

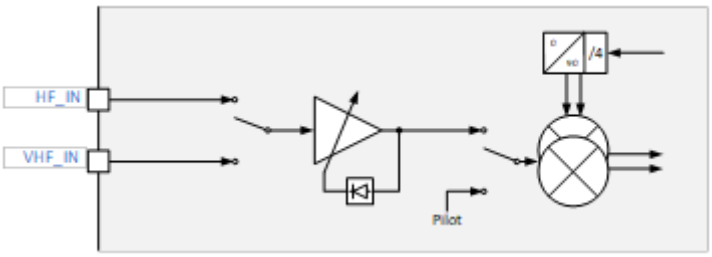


Figure 4 - HF/ VHF input path

The HF/VHF RF path consists of following sections:

- Separate HF/ VHF inputs to allow filter selection
- HF/VHF band LNA
- HF/VHF band quadrature mixer
- HF/VHF band LNA AGC detector
- HF/VHF band LO quadrature former and LO buffers

The HF/VHF LNA has programmable gain, with the mixer having a fixed gain setting. A HF/VHF band dedicated mixer is used to increase system linearity. The AGC loop is constructed around the LNA only. The detection point of the AGC is at the output of the LNA. The AGC can be widely configured in both amplitude and time domain and can be set to automatic or

manual gain control modes. There is an input multiplexer integrated into the LNA gain switching scheme, which is intended to select the input to the LNA: HF_IN or VHF_IN. The inputs are designed for a nominal 50 Ohm input impedance, although use with 75 Ohm antenna system will result in minimal loss.

The outputs of the LF/MF and HF/VHF mixers are multiplexed according to the selected operating band. A large tuneable capacitor bank at output of the mixers creates a first order pole to filter out of band noise and interference. The Quadrature LO signal is also multiplexed to the corresponding mixer input in accordance with the selected frequency band.

The RF section contains a dedicated LDO regulator and bias current source.

4.3 IF path description

The Intermediate frequency (IF) path is intended to amplify the down converted differential signals from the IQ mixer and to filter out-of-band components. The IF path has two channels, an 'I' channel and a 'Q' channel; each channel consists of two stages of programmable gain amplifier (PGA) each with a tuneable upper cut-off frequency, an amplitude detector, and a DC offset compensation block. See register description document and 6.1.3 Operating Characteristics for filter details.

The voltage gain in the respective channel is regulated in the range from -1.6 to 29.3 dB in 1 dB steps.

The DC offset compensation (DCOC) system is an analogue RC high-pass filter and is intended to eliminate flicker noise in the I and Q channels. The analogue DCOC system works continuously, and it is recommended that this it is always enabled.

The IF section contains a dedicated LDO regulator and bias current source.

4.4 Gain Control

Gain control is provided to optimise the dynamic range of the system and prevent over-ranging of the ADC at the output of the analogue stages. Two modes are available: manual gain via the SPI/I2C control interface and automatic mode. In automatic mode there is a two-control loop automatic gain control system (AGC).

- For the LF/MF input, loop one has an attenuator, low-noise amplifier (LNA) and mixer AGC system with a detector connected to the mixer output, in order to monitor the peak amplitude of the mixer output voltage. The LNA and mixer gain is then adjusted to achieve the required mixer output voltage amplitude peak threshold. In this case the AGC is intended to prevent IF stage overload.
- For the HF/VHF input, loop one has a low-noise amplifier (LNA) wideband AGC system with a detector connected to the LNA output / mixer input in order to monitor the peak amplitude of the LNA output voltage. The LNA gain is then adjusted to achieve the required LNA output voltage amplitude peak threshold. LNA AGC is intended to prevent mixer overload.
- Loop two is a pair of intermediate frequency, programmable gain amplifiers (IFPGA) in an AGC system with a detector connected to each IFPGA output / ADC input to monitor amplitude of each IFPGA output voltage (one for the I path, the other for the Q path). The two have essentially identical characteristics but can be controlled independently. The IFPGA gain settings are then adjusted to achieve the required IFPGA output voltage amplitude peak threshold. IFPGA AGC is intended to prevent ADC overload.

Each AGC loop has a temperature compensated diode detector with a typical characteristic as follows; if the output detector level is higher than the high threshold, the gain is reduced. If the output detector level is lower than the low threshold, the gain is increased. This continues until the signal remains between the thresholds. The thresholds should be set with a suitably wide separation to avoid any amplitude modulation content changing the gain yet remaining within the linear range of the detectors. Below a certain input level, the gain will be at maximum, and the low threshold will be exceeded.

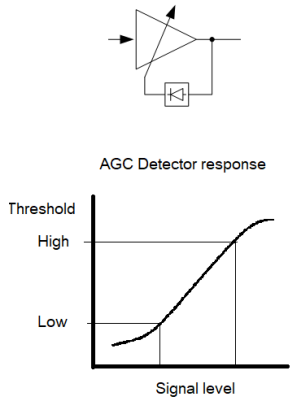


Figure 5 - AGC Response

For most users, the AGC system can be left in its default automatic mode. The default thresholds however may require adjustment dependent on the modulation mode/type being received, the out of band conditions of the system and specifications trying to be met. A typical characteristic for the reported AGC gain status for HF / VHF operation is shown below, with the RF and IF gains reducing at high RF input levels.

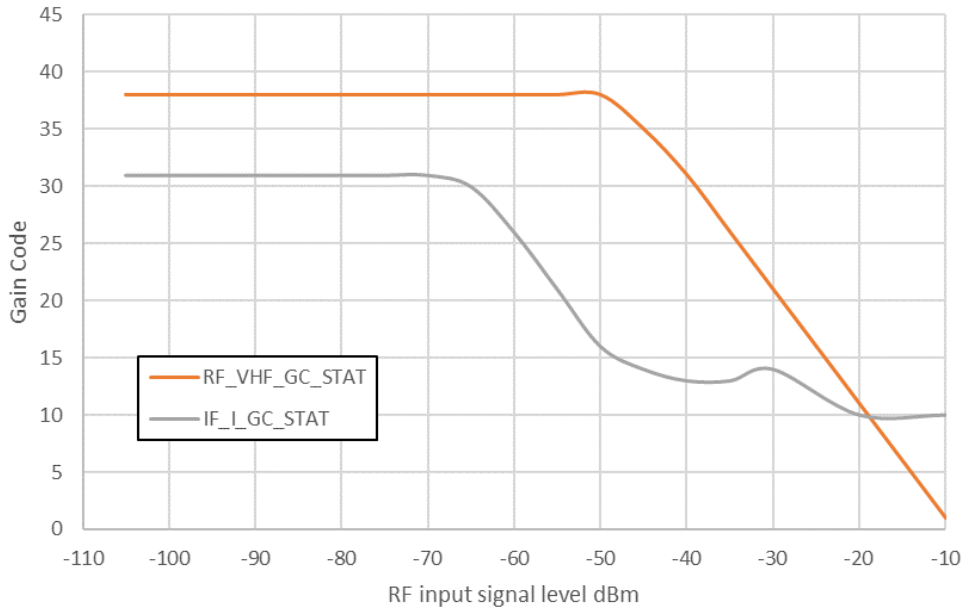


Figure 6 - Typical HF AGC gain variation with signal level

Note: The $1E - IF_Q_GC_STAT response will be similar to that of the I channel.

In manual mode the gains of both the LNA output and IFPGA AGC peak thresholds are programmable via the SPI/I2C control interface. The triggering of the upper or lower threshold for each loop is indicated by separate status bits in the AGC status register. The AGC detector levels can be read directly if required.

The AGC loops are widely configurable (for details refer to the register description).

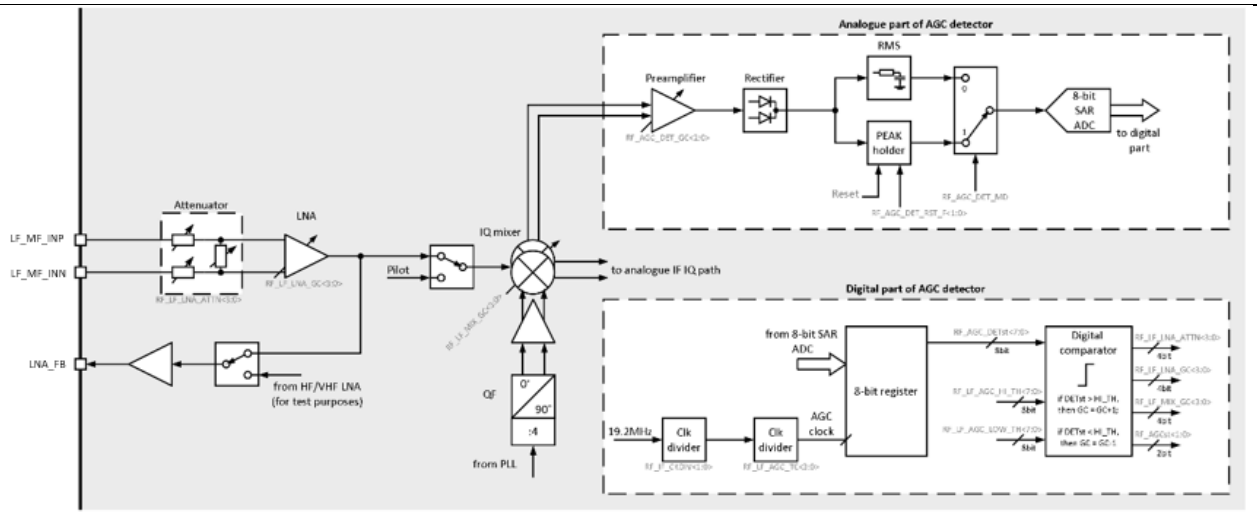


Figure 7 - LF/MF AGC System

The following settings and statuses are available for the LF/MF signal path:

- Automatic or manual gain control mode (register $0C – RF_GC_CTL provides separate control bits for attenuator, LNA and mixer; by default this is set to automatic mode for the LNA and mixer, and manual mode for the attenuator). If a block is in manual mode, then the AGC skips it during operation.
- The order of gain switching stages (register $3C – RF_LF_AGC_CTL)
- Each stage has its min/max gain code selection limits in automatic mode (registers $3D – RF_LF_ATTN for the attenuator, $3E – RF_LF_LNA_GTH for the LNA and $3F – RF_LF_MIX_GTH for the mixer). The gain of the block is changed only after the preceding block has reached GMIN or GMAX. Only one block is being regulated at the time.
- Programmable high and low thresholds (registers $11 – RF_LF_AGC_HI_TH and $12 – RF_LF_AGC_LOW_TH)
- Programmable detector type (register $3C – RF_LF_AGC_CTL, peak or RMS) and gain (register $41 – RF_AGC_DET_GC)
- Peak detector reset time and reset force (register $A1 – RF_AGC_DET_CTL)
- Detector value status (register $3B – RF_DET_STAT) – the value compared to the selected thresholds.
- AGC status (register $19 – RF_AGC_STAT) indicates whether a signal is between thresholds / gain to be decreased / gain to be increased / AGC threshold fault.
- AGC clock frequency (register $40 – RF_LF_AGC_TC for time constant adjustment and $45 for clock division ratio)
- Status of gain selected by AGC (registers $17 – RF_LF_ATTN_STAT for attenuator, $18 – RF_LF_GC_STAT for LNA and mixer)
- Pause mode (register $0C – RF_GC_CTL). Detector output is being updated, but the gain control codes are frozen in the last state.
- In manual gain control mode the AGC detector can be disabled for power saving (register $9F – RF_ AGC_CTL_1)
- Gain control in manual mode (registers $16 – LF_ATTN_GC for attenuator gain, $13 – RF_LF_GC for LNA gain, $0C – RF_GC_CTL for mixer gain).

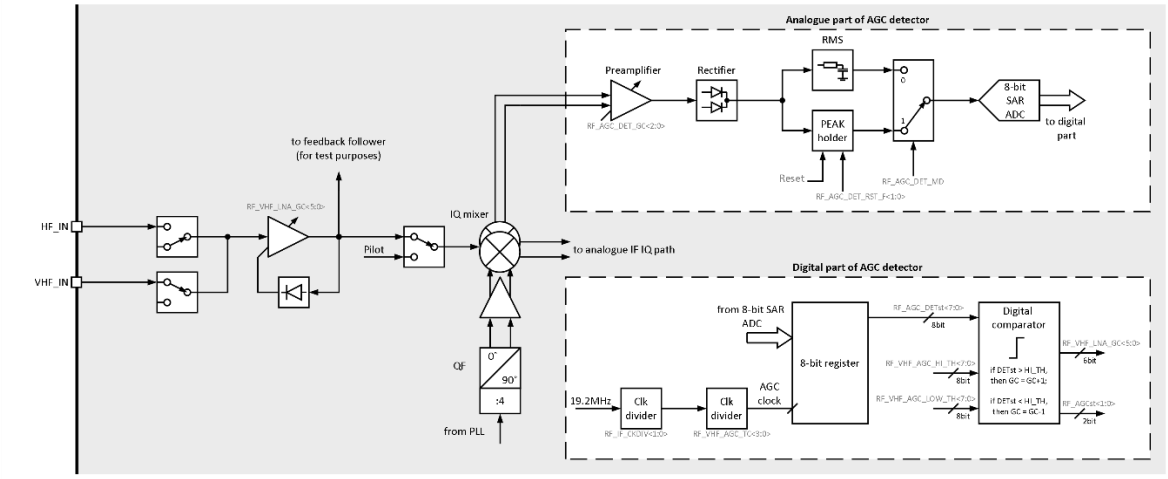


Figure 8 - HF/VHF AGC System

The following settings and statuses are available for the HF/VHF signal path:

- Automatic or manual gain control mode (register $0C – RF_GC_CTL, LNA only)
- Min/max gain code selection limits in automatic mode (registers $37 – RF_VHF_LNA_GMAX and $38 – RF_VHF_LNA_GMIN)
- Programmable high and low thresholds (registers $0D – RF_VHF_AGC_HI_TH and $0E – RF_VHF_AGC_LOW_TH)
- Programmable detector type (register $3C – RF_LF_AGC_CTL, peak or RMS) and gain (register $41 – RF_AGC_DET_GC)
- Peak detector reset time and reset force (register $A1 – RF_AGC_DET_CTL)
- Detector value status (register $3B – RF_DET_STAT) – the value compared to selected thresholds.
- AGC status (register $19 – RF_AGC_STAT) indicates whether signal is between thresholds / gain to be decreased / gain to be increased / AGC threshold fault.
- AGC clock frequency (register $39 – RF_VHF_AGC_TC for time constant adjustment and $45 for clock division ratio)
- Status of gain selected by AGC (register $10 – RF_VHF_GC_STAT)
- Pause mode (register $0C – RF_GC_CTL). The detector output continues to be updated, but the gain control code is frozen in the last state.
- In manual gain control mode, the AGC detector can be disabled for power saving (register $9F – RF_ AGC_CTL_1).
- Gain control in manual mode (register $0F – RF_VHF_LNA_GC).

The following settings and statuses are available for the IFPGA stages:

- Automatic or manual gain control mode (register $1A – IF_GC_CTL)
- Min/max gain code selection limits in automatic mode (registers $43 – IF_AGC_GMAX and $44 – IF_AGC_GMIN)
- Programmable high and low thresholds (registers $1B – IF_AGC_HI_TH and $1C – IF_AGC_LOW_TH)
- Programmable detector type (register $42 – IF_AGC_CTL, peak or RMS)
- Peak detector reset time and reset force (register $ A8 – IF_AGC_DET_CTL)
- Detector value status (registers $46 – IF_I_DET_STAT and $47 – IF_Q_DET_STAT) – the value compared to selected thresholds.
- AGC mode (register $42 – IF_AGC_CTL). By default, both I and Q channels are tracked and the minimum result for gain control is applied for both channels. It is also possible to select one channel to be tracked, while the result will be applied for both channels, or to regulate gain independently for I and Q channels.
- AGC status (register $1F – IF_AGC_STAT) indicates whether a signal is between thresholds / gain to be decreased / gain to be increased / AGC threshold fault.
- AGC clock frequency (register $45 – IF_AGC_TC for clock division ratio and time constant adjustment).
- Status of gain selected by AGC (registers $1D – IF_I_GC_STAT and $1E – IF_Q_GC_STAT)

- Pause mode (register $1A – IF_GC_CTL). Detector output is being updated, but the gain control codes are frozen in the last state.
- In manual gain control mode, the AGC detector can be disabled for power saving (register $A6 – IF_AGC_CTL_1)
- Gain control in manual mode (registers $20 – IF_I_GC and $21 – IF_Q_GC)

4.5 ADC description

The CMX918 contains a quadrature IF path, with a dual channel (I and Q) sigma-delta ADC. ADC sampling occurs at 19.2 MHz frequency with a 38.4 MHz reference.

The ADC section contains a dedicated LDO and bias current source.

4.6 Local Oscillator / Synthesizer

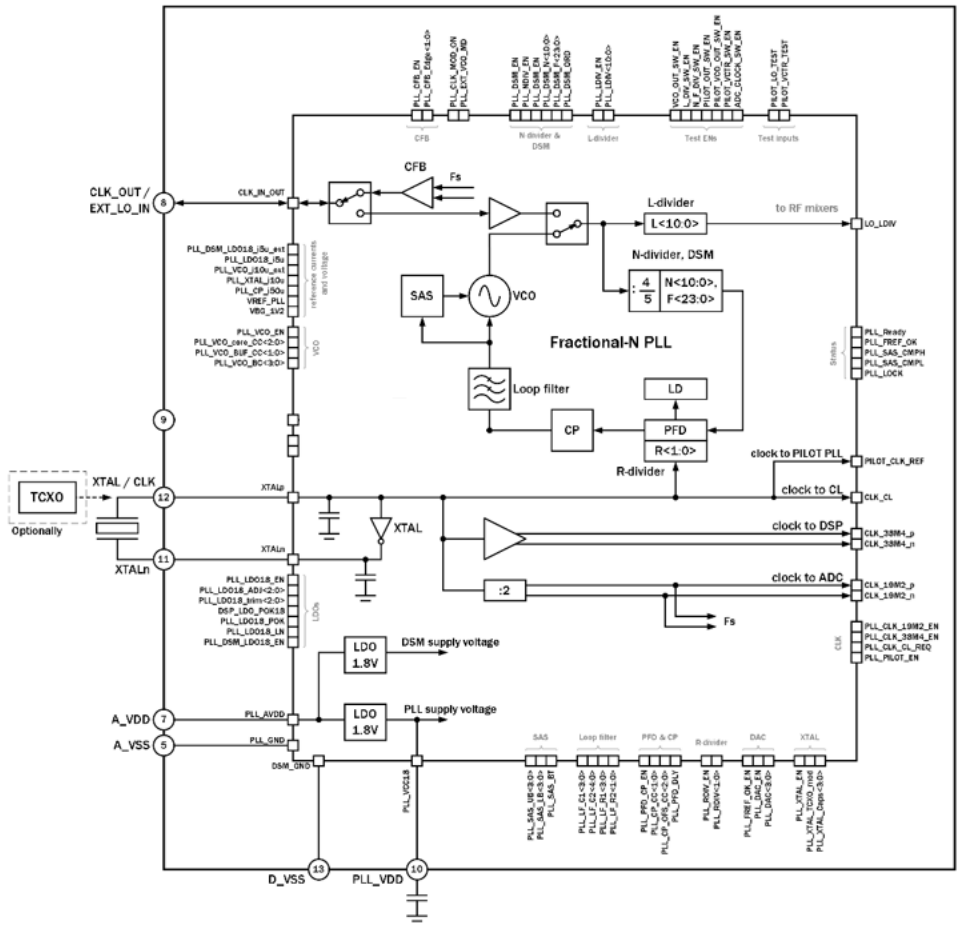


Figure 9 - Synthesizer PLL block diagram

The local oscillator for the mixer is provided by a Fractional-N phase-locked loop frequency synthesizer (PLL). This includes a fully integrated 1.5 – 1.9 GHz Voltage Controlled Oscillator with low tuning gain and good phase noise performance. Optionally, an external LO source can be applied. The PLL operates with a reference frequency of 38.4 MHz, provided from a crystal (with an internal amplifier and tuneable feedback capacitors for frequency adjustment), or an external TCXO source.

The PLL comparison frequency is derived from the reference, dividing by 1, 2, 3 or 4. The feedback N-divider from the VCO to the phase / frequency detector has an integer range of 16 to 2047 and can work in integer mode or in 24-bit fractional mode (fractional range defined as 0-1).

The VCO output is then routed to the quadrature mixer via the L-divider, with a range of 4 to 2047. The mixer has an in-built division by 4 to obtain accurate quadrature outputs (the Quadrature Former). The phase-frequency detector has a built-in digital lock detector circuit. The charge pump has adjustable output current and offset current. There is an

integrated 3rd order loop filter, with a nominal loop bandwidth of 200 kHz; adjustable values of resistance and capacitance are available to optimize the loop phase-noise response.

The PLL block consists of:

- A dedicated PLL 1.8 V LDO
- A separate 1.8 V LDO for DSM
- Programmable XTAL oscillator / TCXO input
- Reference-divider (RDIV)
- Reference frequency indicator (FREF_OK)
- Voltage-controlled oscillator (VCO)
- N-divider (including prescaler) and Fractional Delta-Sigma Modulator (NDIV + DSM)
- Phase-Frequency Detector, charge pump and lock detector (PFD + CP + LD)
- Loop filter
- L-divider (LDIV)
- Voltage detector for SAS (VCO Sub-band Auto-selection System)
- CLK_BUF – Clock buffers to other circuit blocks
- Clock frequency buffer (CFB)

The default settings of the CMX918 PLL system are sufficient for the majority of users and many parameters can be configured automatically. All that is required is to program all PLL parameters is to enter the receive frequency into the Fc registers and execute the PLL_CALC function. Full access to the more detailed PLL parameters is available via the registers for more advanced users (for details refer to the user manual).

4.6.1 PLL programming

To reconfigure the PLL, the following procedure is recommended:

- Select normal operation mode: $03 – IC_MODE, Mode<2:0> = “3”
- Select the IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = “0” or Fif_SIGN = “1” to the IC registers
- Write the IF frequency value (Fif, 96 kHz or 120 kHz) to the IC registers: $08 – Fc_2<6>, Fif = “0” or Fif = “1”
- Write the Carrier frequency (Fc, value in 0.1 kHz) to the IC registers: Fc 2, Fc 1 and Fc 0 <20:0>
- Execute the LO PLL tuning procedure: set PLL_CALC_EXE = “1” in register $29 – AUTO_EXE, ($29 – AUTO_EXE<1> PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to "0".

All the advanced features of the PLL are then automatically calculated and configured (e.g. the N, fractional F and L divider values, along with VCO calibration). The resulting N, F and L values can be read back if required via the applicable registers (for details refer to the user manual).

Note that the LO must be operated above the wanted frequency (Fif_SIGN = 1) for 150 - 281 kHz reception.

To reconfigure PLL in manual mode the following procedure is recommended:

- Select normal operation mode: $03 – IC_MODE, Mode<2:0> = “3”.
- Select the IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = “0” or Fif_SIGN = “1” to the IC registers
- Write the IF frequency value (Fif, 96kHz or 120kHz) to the IC registers: $08 – Fc_2<6>, Fif =“0” or Fif = “1”
- Write the Receive Carrier frequency (Fc, value in 0.1 kHz) to the registers: Fc 2, Fc 1 and Fc 0 <20:0>
- Calculate the values of N, F, L and R coefficients according to the formula:

$$Flo = Fc \pm Fif1 = (Fref*(N+F/2^{24}))/(4*L*R)$$

Where:

Fref = Reference frequency (38.4 MHz)
R = Reference divider (RDIV) value
L = L divider value
N,F = Integer and fractional parts of the overall feedback divider value.

The /4 term is fixed and denotes the action of the Quadrature Former in the mixer.

- Write $2A – PLL_CTRL<1>, PLL_LDIV_MD = “0”.
- Disable the DSM if F divider value = 0: write $2A – PLL_CTRL<0>, PLL_DSM_EN = “0”.

The values of N, F, L and R can then be written to the IC registers: $2B/2C (PLL_DSM_N<10:0>), $2D/2E/2F (PLL_DSM_F<23:0>),$31/32 (PLL_LDIV_reg<10:0>), $30 (PLL_RDIV<1:0>).

4.6.2 VCO Tuning

The integrated VCO has a tuning range of 1500 to 1900 MHz and is coarse tuned to one of 16 bands (SAS - Sub-band Auto-select System) via a switched fixed capacitor bank. Fine PLL adjustment over a sub-band uses a built-in varactor diode.

Table 3 - Frequency Synthesizer Tuning in all Frequency Bands

VCO frequency (MHz)	Quadrature former (mixer) division ratio	L divider division ratio	Local oscillator frequency (MHz)
1530 - 1848	4	920 - 2040	0.19 - 0.5
1512 - 1892	4	180 - 760	0.5 - 2.30
1520 - 1872	4	10 - 167	2.3 - 43
1504 - 1880	4	4 - 10	40 -108.07

A voltage detector within the SAS compares the VCO control voltage with upper and lower thresholds and generates status flags if out of range. The type of threshold is selected by the PLL_SAS_BT bit. The voltages of the upper and lower thresholds are selected by PLL_SAS_UB<3:0> and PLL_SAS_LB<3:0> respectively. If Vctrl is higher than the upper threshold PLL_SAS_CMPH = “1”. If Vctrl is lower than the lower threshold PLL_SAS_CMPL = “1”. The PLL_SAS_EXE routine can then be reactivated, or the sub-band selection can then be manually incremented appropriately. The purpose of this is to reduce VCO phase noise and to compensate for temperature drift in the VCO.

4.6.3 Clock / Crystal Oscillator

The input reference frequency is 38.4 MHz, chosen to be above the LF/MF/HF bands, but also avoiding harmonics within the VHF broadcast band. Use of other input reference frequencies is not supported. The crystal oscillator uses a Pierce architecture optimized for low power consumption. It also can operate as a buffer for an external TCXO input.

The crystal oscillator has integrated adjustable feedback capacitors to optimise performance. The Reference frequency indicator (PLL_FREF_OK) returns “0” when reference signal frequency is too low or is absent. The recommended crystal is a 38.4MHz GSX-223/X SM Crystal 6pF (Techpoint Golledge MP10435). Alternatively, a recommended TCXO is a 38.4 MHz, 1.8 V GTXO-203 (Techpoint Golledge MP07688). Use of a TCXO gives improved close-in phase noise performance. This TCXO can be supplied from the on-chip 1.8 V regulator output (PLL_VDD).

The CLK_BUF block provides reference clocks for other IC functions such as the ADC, DPB (digital processing block) and CFB (clock frequency buffer). Reference frequencies are:

- $F_{DPB} = F_{REF}$ (38.4 MHz)
- $F_{ADC} = F_{REF/2}$ (19.2 MHz)
- $F_{CFB} = F_{REF/2}$ (19.2 MHz)

Dividing the reference frequency by 2 provides the clock for ADC delta-sigma data sampling at 19.2 Ms/s (Million samples per second). The 16-bit post-decimated sample rate is 19.2 Ms/s ÷ 2n.

The Clock frequency buffer (CFB) is a block which optionally provides an output clock which may be used by the demodulator IC. The output clock frequency is $F_{CFB} = F_{REF/2}$. The clock output type is CMOS to the AVDD supply and PLL_CFB_edge<1:0> controls the clock output edge speed.

4.6.4 PFD, charge pump, lock detector

The Phase-frequency detector (PFD) and Charge pump (CP) together with the loop filter form a control loop for VCO tuning. The PFD has a built-in digital lock detector.

4.6.5 Integer boundary spur avoidance

An internal routine ($29 – AUTO_EXE<0>, PLL_CALC_EXE) calculates the appropriate PLL values, including the L divider, automatically from entry of the wanted receive frequency. Within this, if an integer boundary is within 300 kHz of the calculated VCO frequency, the original value of L is changed to L + 1 and N and F recalculated. The values of L are also chosen in such a way as to prevent $F_{VCO} = F_{LO}$ x 4 x (L + 1) being out of the VCO range 1500-1900 MHz.

As $F_{VCO} = \frac{F_{REF} \times (N + F/2^{24})}{R}$ and $F_{VCO} = F_{LO} \times 4 \times L$, for some combinations of FLO and L the result is a small fractional value F that can lead to boundary spurs.

For the chosen FLO and L, a spur offset frequency can be calculated:
$F_{spur} = F_{REF} \times F/2^{24}$.

For $F_{LO} > 52\text{MHz}$ however, the flexibility to change the L divide value is unavailable while remaining within the VCO frequency range. The automatic spur avoidance calculation is therefore not applied in this instance.

For operation at VHF, changing between high and low side mixing (IF_SIGN bit) is an effective method of boundary spur avoidance. This can be implemented by reading the calculated PLL fractional value and checking if this is sufficiently close to zero or one. If it is, the IF_SIGN can be changed and the PLL values recalculated.

4.7 Signal filtering and down conversion

The wanted signal (Fw) is down converted to the first intermediate frequency (IF = 96 kHz or 120 kHz) and is then filtered by analogue filter blocks. The IF path provides pre-filtering and ADC anti-alias frequency suppression.

The output lower cut-off frequency (Fl) is determined by the DC offset compensation time constant (~6 dB/octave).

The output upper cut-off frequency (Fh) is determined by three RC adjustable poles: one after the mixer and two in the IFPGA (~6 dB/octave each pole). The ADC passband is approximately 220 kHz.

Table 4 - Pre ADC Analogue 'roofing' Filter Operating Configurations when used in DRM applications

Configuration	Low F_{cut} max (kHz)	IF_{centre} (kHz)	High F_{cut} max (kHz)	Channel Bandwidth (kHz)
AM and DRM modes A,B,C,D for LF/MF/HF	86	96	106	5, 10, 20
AM and DRM modes A,B,C,D for LF/MF/HF	110	120	130	5, 10, 20
DRM mode E for VHF	46	96	146	100
DRM mode E for VHF	70	120	170	100
Stereo WBFM for VHF	20	120	220	200

4.8 Digital Processing Block

The DPB (digital processing block) implements further decimation and signal filtering from the delta-sigma IQ ADC output. The input is two-channel (I and Q), each channel having a signed bitstream.

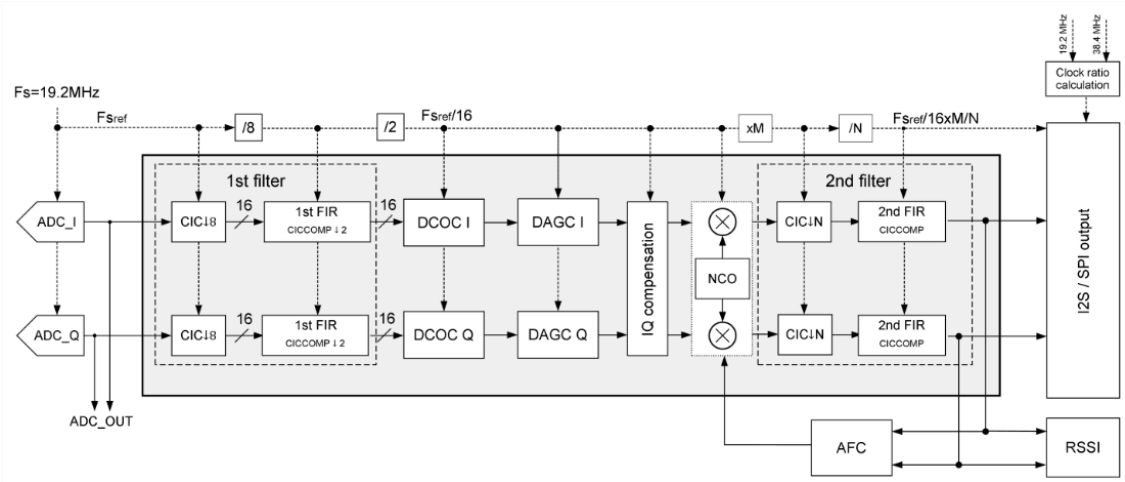


Figure 10 - Digital Processing Block Diagram

The digital IF filter bandwidth is programmable to 5, 10, 20, 100 or 200 kHz. The image frequency F_{Image} is suppressed in the digital domain. The wanted signal is down converted to a zero intermediate frequency (Fif2 = 0 Hz). This is presented as a composite IQ data stream at the I2S/SPI data interface.

All necessary clock signals are formed from the sampling clock Fs of 19.2MHz. The ADC output signal is filtered and decimated by 8 allowing further processing. The signal then passes through a filter, DC Offset Compensation (DCOC) system and digital automatic gain control amplifier (DAGC).

The first digital filter is implemented as a cascade connection of the filter-decimator (CIC) with a decimation factor of 8 and the FIR filter-compensator (CICCOMP) with a decimation factor of 2.

The DC offset is automatically compensated in the DCOC block. The DPB_DCOC_ON register ($BA – DPB_CTL_1<1>) is used to enable the DCOC system (enabled by default). DPB_DCOC_MAN ($C2 - DPB_DCOC_CTL<1>) is used to select manual control mode. In manual control mode correction coefficients should be written to DPB_DCOC_MAN_OFS_I<15:0> ($C3, $C4) and DPB_DCOC_MAN_OFS_Q<15:0> ($C5, $C6).

Gain control, as a part of the DPB (DAGC) block, is enabled by DPB_AGC_ON ($BA – DPB_CTL_1<0>) and operates in automatic or manual mode (DPB_AGC_GC_MD). DAGC precision and speed are programmable (DPB_AGC_GC_PREC<1:0> and DPB_AGC_GC_GSCL<2:0>). In manual control mode the gain at the input of I and Q channels of the demodulator is set by the $BC & $BD - DPB_AGC_MAN_G_I<10:0> and $BE & $BF DPB_AGC_MAN_G_Q<10:0> registers respectively. Manual mode with 0 dB gain is recommended and is the default mode of operation.

After IQ compensation, the signal is then down converted to the second intermediate frequency (FIF2=0). A second filter after digital down conversion is determined by the pair of filter-decimators (CIC) with programmable decimation factor (N) and FIR filter-compensator (CICCOMP). Further adjustment of the output rate is given by the upsample factor (M) which is applied by repeating sample values into the second stage filter. The final signal is then output as 16-bit words via the data port to the host processor for further filtering and demodulation.

The coefficients for the first and second FIR filters are reprogrammable using $D7 - DPB_FIR_MEM_ADDR<5:0> (index pointer), $D8 - DPB_FIR_MEM_DATA_1<7:0> (coefficient MSB) and $D9 - DPB_FIR_MEM_DATA_0<7:0> (coefficient LSB). Coefficients are loaded as signed 16-bit values and the internal memory for each coefficient is updated when the LSB is written. They can be accessed in any order and can also be read back, but the index pointer does not increment automatically so must be explicitly written for every access.

Both filters must have symmetrical impulse responses, with further restrictions as given below. Only the first half of each set of coefficients should be loaded and they are then mirrored internally to form the complete sets. The first FIR has a polyphase architecture and requires its coefficients to be de-interleaved into two phases for loading.

- First FIR: 31 coefficients
  - Load first 16 only in polyphase order using $D7 - DPB_FIR_MEM_ADDR = 0 to 7 (1st phase) and 8 to 15 (2nd phase)
  - To obtain 0 dB DC gain, scaling should be such that the sum of the full set (31 coefficients) = 2^{15}

- Second FIR: 80 coefficients
  - Load first 40 only in conventional form using $D7 - DPB_FIR_MEM_ADDR = 16 to 55
  - Absolute values of the first 20 coefficients must be less than 2^{12}
  - Absolute values of the second 20 coefficients must be less than 2^{14}
  - To obtain 0 dB DC gain, scaling should be such that the sum of the full set (80 coefficients) = 2^{16}

The default FIR coefficients can be reloaded from the table below.

Table 5 - Default FIR coefficients

A[56] =	-13,	-137,	-56,	573,	-60,	-1824,	1284,	8378,
	-61,	-173,	249,	562,	-1113,	-1190,	4998,	9744,
	28,	44,	54,	38,	-11,	-82,	-146,	-163,
	-107,	16,	157,	244,	211,	43,	-201,	-402,
	-435,	-236,	142,	531,	716,	545,	28,	-629,
	-1092,	-1057,	-424,	602,	1551,	1876,	1229,	-310,
	-2162,	-3410,	-3145,	-870,	3214,	8185,	12674,	15332

4.8.1 Digital processing operating modes

Table 6 - Output Data Rate Configuration

Bandwidth (kHz)	N	M	Over sampling	Sample rate (ks/s)	Clock rate	Data and clock rate (kb/s)	Frame rate (ks/s)
5	50	1	4.8	24	2 (decreased)	1920	48
					4 (normal)	3840	96
					10 (increased)	9600	240
			2.4	12	4 (decreased)	1920	48
					8 (normal)	3840	96
					20 (increased)	9600	240
10	25	1	4.8	48	1 (decreased)	1920	48
					2 (normal)	3840	96
					5 (increased)	9600	240
			2.4	24	2 (decreased)	1920	48
					4 (normal)	3840	96
					10 (increased)	9600	240

Bandwidth (kHz)	N	M	Over sampling	Sample rate (ks/s)	Clock rate	Data and clock rate (kb/s)	Frame rate (ks/s)
20	25	2	4.8	96	0.5 (decreased)	1920	48
					1 (normal)	3840	96
					5 (increased)	19200	480
			2.4	48	1 (decreased)	1920	48
					2 (normal)	3840	96
					5 (increased)	9600	240
100	5	2	4.8	480	0.5 (decreased)	9600	240
					1 (normal)	19200	480
			2.4	240	0.5 (decreased)	4800	120
					1 (normal)	9600	240
200	5	4	4.8	960	0.5 (decreased)	19200	480
					1 (normal)	38400	960
			2.4	480	0.5 (decreased)	9600	240
					1 (normal)	19200	480

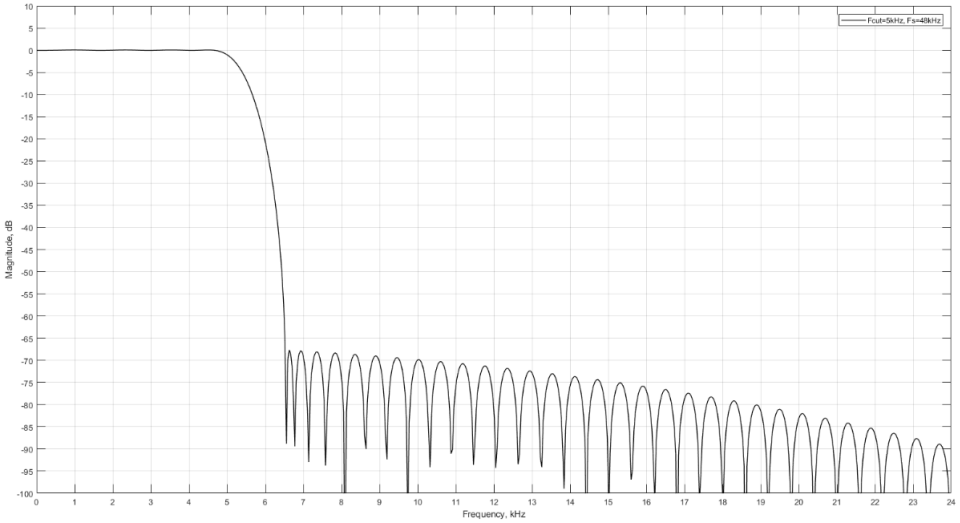


Figure 11 - DPB Channel Filter response @ BW=10 kHz

Table 7 - Filter frequency response

Bandwidth (kHz)	Target rejection (dB)	Frequency point (kHz)
5	-1	2.5
	-50	3.22
10	-1	5
	-50	6.44
20	-1	10
	-50	12.88
100	-1	50
	-50	64.4
200	-1	100
	-50	128.8

The source of the input data for the RSSI (Received Signal Strength Indicator) system is the output signal of the decimation filter stage; the power measurement is therefore carried out within the output filter band. The measured value of the signal power is presented in “dB” in the DPB_RSSI_STAT_1(0) registers $D0/D1 A correction offset can be added for the HF/VHF bands in DPB_RSSI_REF_HF_1(0) in registers $CE/CF and for the LF/MF bands in DPB_RSSI_REF_LF_1(0) in registers $DD/DE.

The AFC system is enabled by DPB_AFC_ON. The AFC structure is based on a CORDIC-based frequency discriminator and an integral loop filter in the feedback path. The output of the last FIR is used as input to the AFC system. Correction is done by adding the loop filter output to the frequency controlling word of the digital mixer. Its correction range and precision / speed can be adjusted in the registers.

4.8.2 Output data interface

The DRM Tuner IC outputs 16-bit I and Q data using the I2S (master) or SPI (master) interfaces. I and Q data may be allocated to either channel ($28:b6).

- I2S standard data interface is optimized for streaming PCM data and requires 3 serial bus lines:
  - WS: word select (0=left channel, 1=right channel);
  - SD: serial interface output data, two time-multiplexed data channels;
  - SCK: serial interface clock.
- Standard Serial Peripheral Interface requires 3 serial bus lines:
  - CS: serial interface chip select signal with programmable polarity;
  - SDA: serial interface output data, two time-multiplexed data channels;
  - SCLK: serial interface clock.

Table 8 - Output data interface pins

Pin #	I2S	SPI
22	WS	CS
23	SD	SDA
24	SCK	SCLK

I2S

Data word length	16 bits data + 4 fixed (pause) bits
Polarity of WS	Left channel WS = 0 = I data Right channel WS = 1 = Q data
Delay	First CK falling edge after WS transition is valid data
Data format	Two's complement, MSB sent first
Transition	SD and WS change on the falling edge of CLK SD valid on the rising edge of CLK
Data transfer	On the falling edge of SCK
Data reception	On the rising edge of SCK

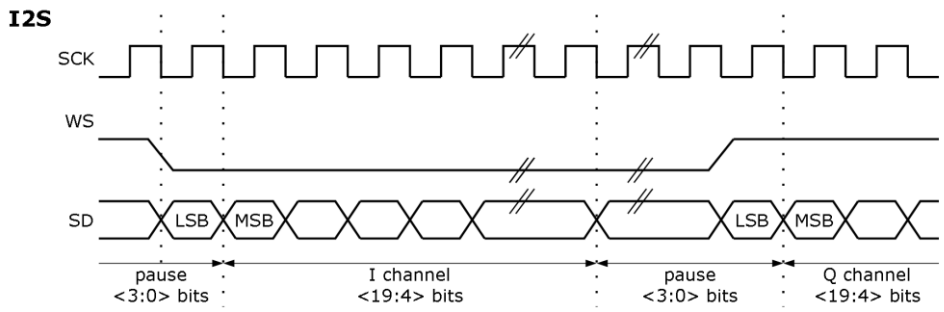


Figure 12 - I2S Data Format

SPI

Data word length	16 bits
CS polarity	Programmable (low or high active level)
Data sequence	I channel data first, then - Q channel data
Data format	Two's complement, MS byte sent first
Transition	SDA change on the falling edge of CLK SDA valid on the rising edge of CLK
Data transfer	On the falling edge of SCLK
Data reception	On the rising edge of SCLK

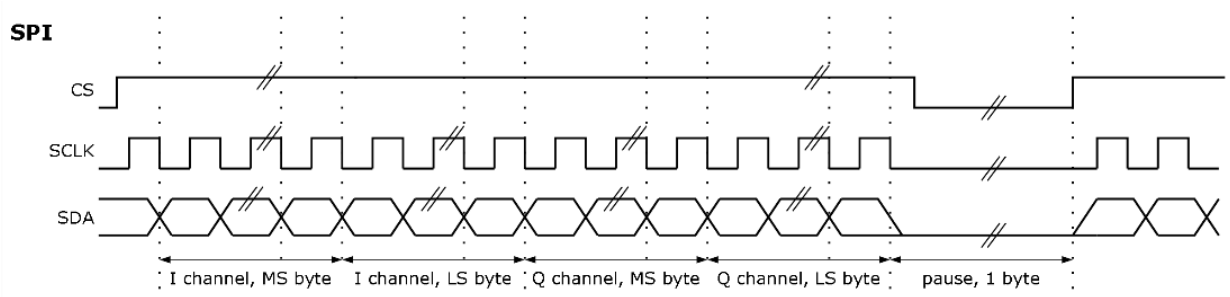


Figure 13 - SPI Data Format

4.8.3 IQ Calibration

The amplitude and phase balance of the I/Q mixer system requires calibration in order to achieve optimum image rejection.

- Select normal, ECO or boost mode using $03 – IC_Mode, Mode<2:0> setting
- Write Carrier frequency (Fc, value in 0.1 kHz) to the IC registers: Fc_2, Fc_1 & Fc_0, Fc<20:0>
- Write IF frequency value (Fif1, 96 kHz or 120 kHz) to the IC registers: $08 – Fc_2<6>, Fif = "0" or Fif = "1"
- Select IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = "0" or Fif_SIGN = "1" to the IC registers
- Select channel bandwidth $0B – BANDWIDTH (BW<2:0>)
- Execute IF filter bandwidth calibration procedure: $29 – AUTO_EXE<2>, IF_BW_ACS_EXE="1". Wait until IF_BW_ACS_EXE is reset to "0".
- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE="1", $29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE. Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to "0".
- Write DPB_CTRLS<2>="1" to enable improved "running" mode and DPB_CTRLS<6:4>="110" to enhance accuracy. IQ calibration will be continuously running until the pause command is written or "running" mode is turned off.
- "Running" mode can be set to pause (write DPB_CTRLS<3> = "1" to set pause and DPB_CTRLS<3> = "0" to end pause).
- Write DPB_CTRLS<2> = "0" to disable "running" mode.
- No calibration coefficients are available in this mode (DPB_IQ_COMP_CORR_I_VAL<15:0>, DPB_IQ_COMP_CORR_Q_VAL<15:0>).

Alternative methods are available, see section 5.9.2

4.9 IF Filter bandwidth calibration

The IF filter bandwidth calibration procedure is intended to compensate for process variation and temperature dependence on the filter characteristics.

The initial bandwidth code ($4D – IF_BW_ACS_IN <4:0>dec = “20” for Fif = 96 kHz and BW = 100kHz by default) is used to control an RC-oscillator and its oscillation frequency is compared to the expected cut-off frequency (159.7 kHz by default). This RC-oscillator is built on the same components used in the IF filter design, which allows correlation between oscillation frequency and IF filter cut-off frequency to be achieved.

This code is then adjusted by a state machine (step polarity is programmable, BW_ACS_STEP_PLR) until the oscillation frequency and expected frequency have the minimum error.

The lower the cut-off frequency, the longer the calibration time. For the lowest cut-off frequency, IF_BW calibration may take up to 520 us (310 us typical). The calibration time for higher cut-off frequencies however is faster, typically around 50 us.

The obtained BW code is used as calibration output and is applied to the IF analogue bandwidth controls in separate registers ($4E – RF_MIX_BW, $4F – IF_I_BW and $50 – IF_Q_BW) and can be read by the controller.
If the calibration procedure is not executed, BW control registers (RF_MIX_BW, IF_I_BW and IF_Q_BW) should be configured manually. $0B – BANDWIDTH must be also written.

The bandwidth calibration procedure must be executed (BW_ACS_EXE = “1” in $29 – AUTO_EXE) after device activation and if the Fif ($08 – Fc_2, b6) or $0B – BANDWIDTH settings are changed.

Bit 4 in the $05 – IRQ_MASK and $06 – STATUS registers (IF_BW_ACS_OK) indicates whether the bandwidth calibration completed successfully or with error/was not executed.

Application of an input signal does not affect IF_BW calibration.

5 Operational Guidelines

5.1 Initial settings

After power-on and once out of reset, the CMX918 is in standby mode: the reference voltage and currents sources and internal regulators (for RF, IF, PLL, ADC and DPB) and XTAL will be enabled.

The receive carrier frequency can be set from 150 kHz to 108 MHz with 100 Hz step size using Fc<20:0> bits (registers $08 to $0A). All 21-bits should be rewritten when Fc is changed. Writing the 8 least significant bits implements the change in value (but does not execute PLL changes). The default carrier frequency is 94.9 MHz.

The Intermediate frequency (Fif) can be set to 96 kHz (Fif = "0", default) or 120 kHz (Fif = "1") via bit6 of register $08 FC_2. The default IF frequency polarity corresponds to Flo-Fc=Fif conversion (Fif_SIGN = "0") and can be changed to low-side mixing by writing Fif_SIGN = "1" (Fc-Flo= Fif). This is bit 7 of register $08 FC_2.

The channel bandwidth can be set to 5 kHz, 10 kHz, 20 kHz, 100 kHz (default) or 200 kHz using $0B – BANDWIDTH BW<2:0> setting.

If the default settings of Fc, Fif and BW are acceptable and IQ calibration is not required, a simplified start-up procedure is as described below:

- Select Normal mode: $03 – IC_Mode, Mode<2:0> = "3"
- Execute IF filter bandwidth calibration procedure: $29 – AUTO_EXE<2>, IF_BW_ACS_EXE = "1"
- Wait until IF_BW_ACS_EXE is reset to "0"
- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = "1" ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE have completed and are reset to "0"

These EXE commands are accessed via the AUTO_EXE register $29 (for details refer to the register description).

The following procedure is recommended if Fc, Fif and BW need to be changed:

- Select Normal mode in register: $03 – IC_Mode, Mode<2:0> = "3"
- Select the Carrier frequency (Fc, value in 0.1 kHz) Fc_2, Fc_1 & Fc_0, Fc<20:0>, select the IF frequency value (Fif1, 96 kHz or 120 kHz) : $08 – Fc_2<6>, Fif = "0" or Fif = "1" and select the IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = "0" or Fif_SIGN = "1"
- Select the channel bandwidth $0B – BANDWIDTH (BW<2:0>)
- Execute the IF filter bandwidth calibration procedure: $29 – AUTO_EXE<2>, IF_BW_ACS_EXE= "1". Wait until IF_BW_ACS_EXE is reset to "0"
- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = "1", $29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE. Wait until PLL_CALC_EXE and PLL_SAS_EXE have completed and are reset to "0". These can be run by writing 0x05 to AUTO_EXE register $29

5.2 Reference Frequency Configuration

The IC is preconfigured to operate a with 38.4 MHz reference frequency. The default reference frequency input source is an on-chip oscillator using a crystal connected across pins 11 and 12 (PLL_XTAL_TCXO_MD bit in $07 – CLK_CTL is set to "0"). Service register $97 – PLL_XTAL_CTL allows control of internal capacitors to tune the crystal oscillator frequency in XTAL mode.

As an option, the reference frequency input source can be switched to use a TCXO by writing PLL_XTAL_TCXO_MD = "1". In this case TCXO must be connected to pin 12, while pin 11 is then connected to ground. The TCXO power supply can be sourced from +1.8 V available at pin 10 (PLL_VDD).

The PLL comparison frequency is set by default to use the input 38.3 MHz reference frequency, however this can be divided by 2, 3, or 4, set using PLL_RDIV<1:0> (register $30 – PLL_RDIV). In this case the PLL must be reconfigured according to procedure described in section 5.3 PLL Reconfiguration. The PLL is preconfigured according to the default Fc and Fif settings.

5.3 PLL Reconfiguration

To reconfigure the PLL the following procedure is recommended:

- Select normal operation mode: $03 – IC_Mode, Mode<2:0> = “3”
- Select the Carrier frequency (Fc, value in 0.1 kHz) Fc_2, Fc_1 & Fc_0, Fc<20:0>, select the IF frequency value (Fif1, 96 kHz or 120 kHz): $08 – Fc_2<6>, Fif = “0” or Fif = “1” and select the IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = “0” or Fif_SIGN = “1”
- Write these values to the IC registers $08 to $0A (FC_2/1/0)
- Execute the LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = “1” ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE)

Wait until PLL_CALC_EXE and PLL_SAS_EXE have completed and are reset to “0”.

In automatic mode, when the user executes the PLL dividers ratio calculation by writing PLL_CALC_EXE = “1”, internal control logic will calculate and change values of PLL_DSM_N<7:0> (registers $2B/2C), PLL_DSM_F<23:0> (registers $2D-2F) and PLL_LDIV<7:0> (registers $31/32) appropriately. The values of the fractional N value PLL_DSM_F<23:0> will be changed simultaneously after calculation is finished.

To reconfigure the PLL in manual mode (for advanced users) the following procedure is recommended:

- Select normal operation mode: $03 – IC_Mode, Mode<2:0> = “3”
- Select the Carrier frequency (Fc, value in 0.1 kHz) Fc_2, Fc_1 & Fc_0, Fc<20:0>, select the IF frequency value (Fif1, 96 kHz or 120 kHz): $08 – Fc_2<6>, Fif = “0” or Fif = “1” and select the IF frequency sign: write $08 – Fc_2<7>, Fif_SIGN = “0” or Fif_SIGN = “1”
- Write these values to the IC registers $08 to $0A (FC_2/1/0)
- Calculate values of N, F, L and R coefficients according to the formula:
    - Flo = Fc±Fif1 = (Fref*(N+F/2^24))/(4*L*R)
- Write PLL_LDIV_MD = “0” (bit 1 of register $2A)
- Disable the DSM if F divider value = 0: write PLL_DSM_EN = “0” (bit 0 of register $2A)
- Write the values of N, F, L and R coefficients to the IC registers: PLL_DSM_N<10:0>, PLL_DSM_F<23:0>, PLL_LDIV_reg<10:0>, PLL_RDIV<1:0> (registers $2B to $30)

In manual mode, the values of $2C - PLL_DSM_N<7:0>, $2D & $2E PLL_DSM_F<23:0> and $32 - PLL_LDIV<7:0> are updated via the control interface separately by 8bit registers. They are always “applied” if the PLL is active, so intermediate values will be used while user rewrites them register by register.

A PLL lock indicator (PLL_LOCK) is available in register $06 – STATUS, bit 3. Crossing of the VCO voltage comparator lower threshold (PLL_SAS_CMPL) will be indicated by bit 1 of the $06 - STATUS register, crossing of upper threshold (PLL_SAS_CMPH) – by bit 2.

The IC includes an integrated 3rd order low-pass loop filter with adjustable values of resistance and capacitance for loop tuning with the aim of best phase-noise performance. The loop filter components can be tuned using $8F – PLL_LF_CTL_0, PLL_LF_R1<3:0>, $90 - PLL_LF_CTL_1, PLL_LF_R2<1:0>, $8F - PLL_LF_CTL_0, PLL_LF_C1<3:0> and $91 – PLL_LF_CTL_2, PLL_LF_C2<4:0> settings in service section of the registers map ($8F – PLL_LF_CTL_0 onwards).

If an external LO source is to be used with the device, PLL_EXT_VCO_MD must be set to “1” (b2 in $2A – PLL_CTL). Note that this input is before the PLL L divider.

5.4 Noise Figure Improvement

Changing the R-divider value allows improved noise figure performance over VHF frequency range. Recommended values are given in table overleaf.

Table 9 - R-divider recommended values

Fc (MHz)	Fref (MHz)	R-divider value	Fpfd (MHz)
2 - 86	38.4	1	38.4
86 - 92	38.4	3	12.8
92 - 100	38.4	2	19.2
100 - 110	38.4	3	12.8

If R=2 or 3 is selected and written (PLL_RDIV = “01” or “10” in register $30 – PLL_RDIV), execute the LO PLL tuning procedure: set $29 – AUTO_EXE<0>, PLL_CALC_EXE = “1”, ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to "0".

In addition to R-divider value changes, PLL loop filter adjustment can be applied for in-band phase noise reduction in trade off to out of band phase noise.

Table 10 - Loop filter recommended settings

R-divider value	PLL_LF_C1<3:0> (dec)	PLL_LF_C2<4:0> (dec)	PLL_LF_R1<3:0> (dec)	PLL_LF_R2<1:0> (dec)
1	15	31	4	3
2	9	20	5	3
3	7	17	6	3

5.5 DRM Operation Table

This section provides further details for using the CMX918 in a DRM application. The following diagrams are from ES 201 980 (DRM system specification) and illustrate the necessity for re-tuning the tuner local oscillator for 18/20 kHz modes (spectrum occupancy 4 and 5) to centre the signal within the IF passband. The re-tuning must be managed by the demodulating DSP as data signifying the transmission type is contained within the FAC cells.

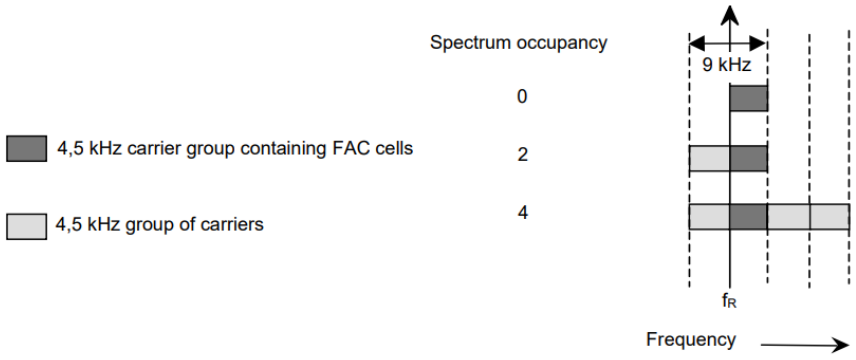


Figure 14 - Spectrum occupancy for 4.5 kHz modes

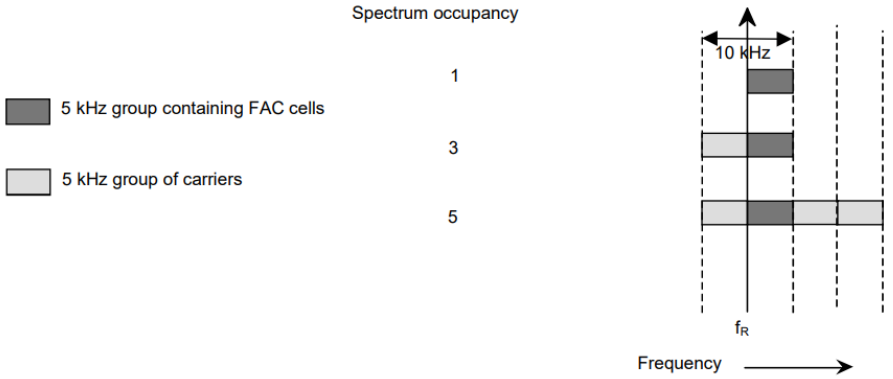


Figure 15 - Spectrum occupancy for 5 kHz modes

5.6 Worked examples for specific frequencies

These examples are after a power on reset and assume IQ calibration is not required.

909 kHz MF band

```
Write 0x03 to *IC MODE              ; normal mode
Write 0x01 to *BANDWIDTH            ; 10 kHz
Write 0x80 to *FC2                  ; Flo = Fc – Fif, 96 kHz IF
Write 0x23 to *FC1
Write 0x82 to *FC0                  ; 0x2382 = 9090 decimal, FC value is in 100 Hz.
Write 0x05 to *AUTO_EXE             ; Calibrates IF filter bandwidth, calculates and executes PLL / VCO routines.

Write 0x02 to *RF_LF_LNA_IN_CO      ; MF internal tuning capacitance for tuning a ferrite or air loop antenna.
Write 0x34 to *RF_LF_LNA_IN_C1      ; Value is typical and can be optimised on RSSI reading.

Write 0x61 to *PLL_XTAL_CTL         ; Tunes reference crystal to typical value.
```

The CMX918 is then tuned to 909 kHz with 10 kHz channel band width. The LF/MF front-end and antenna input has been automatically selected, and the IQ baseband data stream is available for demodulation at the outputs.

3965 kHz HF band (Radio France DRM test)

```
Write 0x03 to *IC MODE              ; normal mode
Write 0x01 to *BANDWIDTH            ; 10 kHz
Write 0x80 to *FC2                  ; Flo = Fc – Fif, 96 kHz IF
Write 0x9A to *FC1
Write 0xE2 to *FC0                  ; 0x9AE2 = 39650 decimal, FC value is in 100 Hz.
Write 0x05 to *AUTO_EXE             ; Calibrates IF filter bandwidth, calculates and executes PLL / VCO routines.
Write 0x61 to *PLL_XTAL_CTL         ; Tunes reference crystal to typical value.
```

A wider window of AGC thresholds is required due to the high peak to mean nature of DRM, compared to AM. Full details of recommended AGC settings are provided in section 5.8, with the values stated dependent upon the current mode.

```
Write 0xC8 to RF_VHF_AGC_HI_TH      ; Sets LNA AGC high threshold suitable for DRM mode
Write 0x6C to RF_VHF_AGC_LOW_TH     ; Sets LNA AGC high threshold suitable for DRM mode
Write 0x9C to IF_AGC_HI_TH          ; Sets IF AGC high threshold suitable for DRM mode
Write 0x50 to IF_AGC_LOW_TH         ; Sets IF AGC high threshold suitable for DRM mode
```

The CMX918 is then tuned to 3650 kHz with 10 kHz channel band width. The HF front-end and antenna input has been automatically selected, and the IQ baseband data stream is available for demodulation at the outputs.

95.5 MHz VHF band

```
Write 0x03 to *IC MODE          ; normal mode
Write 0x04 to *BANDWIDTH        ; 200 kHz
Write 0xCE to *FC2              ; Flo = Fc – Fif, 120 kHz IF
Write 0x92 to *FC1
Write 0x78 to *FC0              ; 0xE9278 = 955000 decimal, FC value is in 100 Hz.
Write 0x05 to *AUTO_EXE         ; Calibrates IF filter bandwidth, calculates and executes PLL / VCO routines.
Write 0x61 to *PLL_XTAL_CTL     ; Tunes reference crystal to typical value.
```

The CMX918 is then tuned to 95.500 MHz with 200 kHz channel band width. The VHF front-end and antenna input has been automatically selected, and the IQ baseband data stream is available for demodulation at the outputs.

The default output data format is SPI in all cases above.

5.7 LF/MF band Input and Antennas

The LF/MF inputs can be connected to low impedance antennas or signal sources via a suitable input transformer, e.g. Coilcraft WB36-1SL.

Recommended LF/MF band antenna configurations are as follows:

The inductance of a ferrite rod antenna connected across the LF_MF_INP/CBP and LF_MF_INN/CBN pins should have these values:

- MF 500 kHz to 1700 kHz: 450 µH
- LF 130 kHz to 300 kHz: 15 mH

The CMX918 includes a programmable capacitor bank on the CBP and CBN pins (see registers $14 – RF_LF_LNA_IN_C_1 and $15 – RF_LF_LNA_IN_C_0) which can be used to resonate a suitable ferrite rod antenna for the MF band (shown in Figure 16 - Ferrite Rod Antenna - Programmable Capacitor Bank). In this implementation the capacitor bank is connected in parallel with the inputs. It is expected that the capacitance value is adjusted either via a look-up table or for maximum signal via the host controller software.

A PCB design should minimise stray capacitance to these pins as any additional capacitance will affect the ability to resonate the ferrite antenna at the higher frequency end of the band.

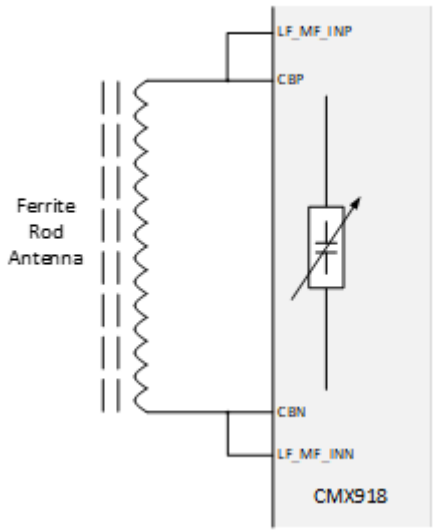


Figure 16 - Ferrite Rod Antenna - Programmable Capacitor Bank

A suitable ferrite rod antenna for MF is approximately 60 turns of 10 strand/ 0.04mm (overall diameter approximately 0.18mm) Litz wire on a 152 x 12.7 mm type 61 ferrite rod. Other rod shapes using other ferrite materials capable of

operating up to 2 MHz are acceptable, but the number of turns will need to be adjusted. **The exact number of turns, and the position of the coil on the rod, will need to be determined by measurement to achieve the 450 µH value**. Use of a shorter ferrite rod will reduce the receiver sensitivity.

An alternative arrangement is to resonate a ferrite rod antenna primary winding using the CBP/CBN pins but to feed the LF_MF_INP/LF_MF_INN pins from a separate, lower impedance secondary winding.

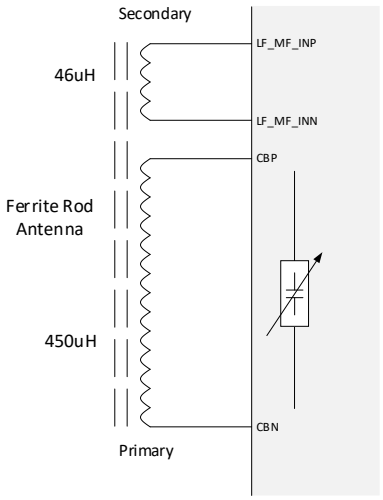


Figure 17 - Use of ferrite rod antenna with dual windings

Alternatively, an MF 'air loop' antenna of approximately 15 uH can also be used via an input transformer (Coilcraft type WB36-1SL recommended) – see Figure 18 - Typical Air Loop Antenna. The capacitor bank can also be used to resonate this if required.

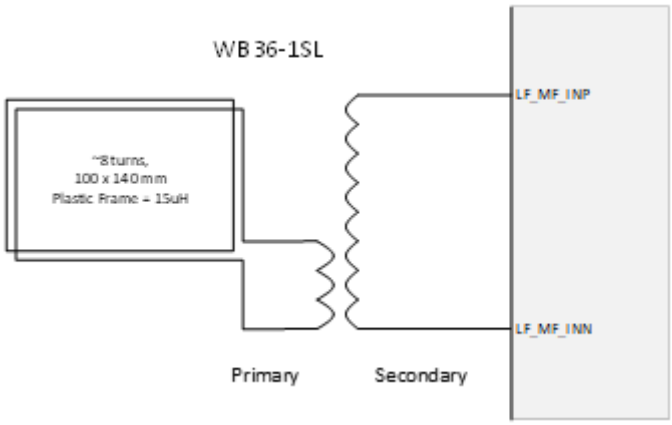


Figure 18 - Typical Air Loop Antenna

In most regions, LF reception is not required. However, if an LF antenna is required, a more complex coil structure may be needed, along with additional external parallel capacitance to resonate. Suitable band switching of the windings may also be needed if both MF and LF band reception is envisaged. This could be implemented via GPIO pins on the host controller. Advice from a specialist in ferrite antennas is recommended.

5.8 AGC and Bandwidth Settings

Recommended values for the AGC settings and analogue filter bandwidths, optimised for broadcast receiver use, are as follows. These changes are dependent on mode, with DRM having a higher peak to mean ratio than AM.

LF_MF AGC Settings

Description	Register $ (hex)	AM Value (hex)	DRM value (hex)
RF_LF_AGC_HI_TH	11	AA	AA
RF_LF_AGC_LOW_TH	12	3C	32
IF_AGC_HI_TH	1B	A0	C8
IF_AGC_LOW_TH	1C	46	50
RF_GC_CTL	0C	00	00
RF_AGC_DET_GC	41	04	00
RF_MIX_BW	4E	0A	08
IF_I_BW	4F	0A	00
IF_Q_BW	50	0A	00

HF AGC Settings

Description	Register $ (hex)	AM Value (hex)	DRM value (hex)
RF_VHF_AGC_HI_TH	0D	82	C8
RF_VHF_AGC_LOW_TH	0E	3c	6C
IF_AGC_HI_TH	1B	82	9C
IF_AGC_LOW_TH	1C	46	50
RF_GC_CTL	0C	00	00
RF_AGC_DET_GC	41	04	00
RF_MIX_BW	4E	0A	08
IF_I_BW	4F	0A	00
IF_Q_BW	50	0A	00

VHF AGC Settings

DRM uses a 100 kHz channel bandwidth whereas wideband broadcast FM uses 200 kHz. The settings are otherwise identical.

Description	Register $ (hex)	FM Value (hex)	DRM value (hex)
RF_VHF_AGC_HI_TH	0D	82	82
RF_VHF_AGC_LOW_TH	0E	3C	3C
IF_AGC_HI_TH	1B	82	82
IF_AGC_LOW_TH	1C	46	46
RF_GC_CTL	0C	00	00
RF_AGC_DET_GC	41	04	04
RF_MIX_BW	4E	1B	13
IF_I_BW	4F	1B	13
IF_Q_BW	50	1B	13

5.9 Other Features

5.9.1 Pilot PLL

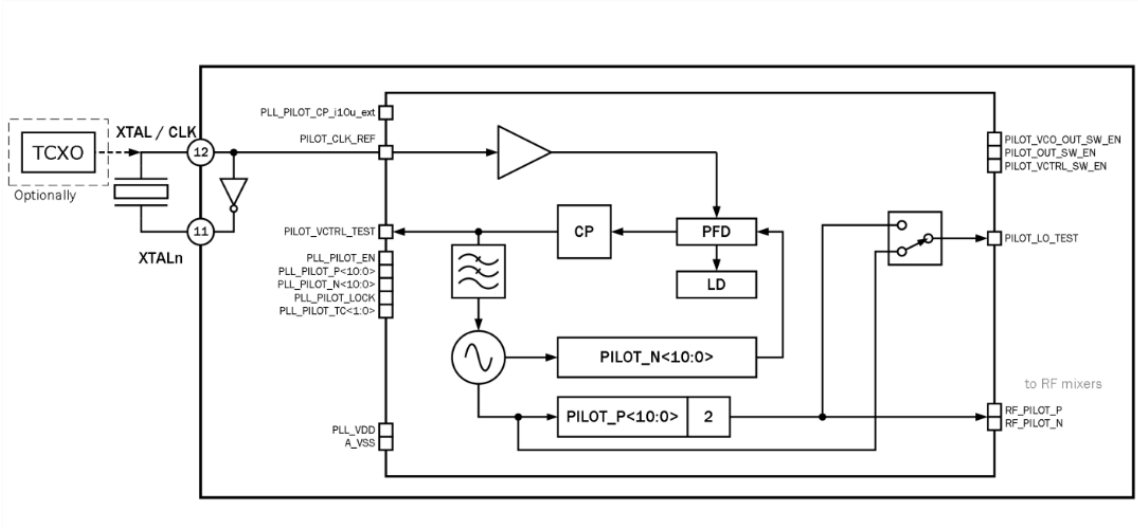


Figure 19 - Pilot PLL block diagram

A separate Pilot signal, generated using an integer N PLL synthesizer, provides a test signal source that can briefly be injected into the receiver (mixer input) to allow IQ calibration, with the aim of optimising image rejection. The phase and amplitude correction factors are then determined by a semi-automatic system (see IQ Calibration, 4.8.3) and are then applied to the CMX918 Digital Processing Block. The Pilot signal frequency is selected so that it falls in the 'image' channel for the wanted signal (Fc). The Pilot signal frequency is calculated according to the formula:

$$F\_pilot = (F\_ref \times PILOT\_N)/(2 \times PILOT\_P)$$

where F_{ref}= 38.4 MHz;
PILOT_N = 9, 10, … 19;
PILOT_P = 3, 4, … 2047.

Note the pilot PLL must be powered down during normal operation otherwise performance will be degraded/impaired.

5.9.2 I/Q Amplitude and Phase Compensation

The IQ compensation function can be performed continuously ("running" mode). This mode is recommended, however this section also describes manual control (if required).

To run IQ compensation in continuous running mode:

- Select normal, ECO or boost mode using $03 – IC_Mode, Mode<2:0> setting
- Write Carrier frequency (Fc, value in 0.1 kHz) to the IC registers: Fc_2, Fc_1 & Fc_0, Fc<20:0>
- Write IF frequency value (Fif1, 96 kHz or 120 kHz) to the IC registers: Fc_2<6> Fif = "0" or Fif = "1"
- Select IF frequency sign: write Fc_2<7>, Fif_SIGN = "0" or Fif_SIGN = "1" to the IC registers
- Select channel bandwidth $0B – BANDWIDTH, BW<2:0>
- Execute IF filter bandwidth calibration procedure: $29 – AUTO_EXE<2>, IF_BW_ACS_EXE = "1"; Wait until IF_BW_ACS_EXE is reset to "0"
- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = "1", $29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE. Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to "0"
- Write $B8 - DPB_CTRLS_0<2> = "1" to enable continuous IQ compensation "running" mode and $B8 - DPB_CTRLS_0<6:4> = "110" for enhanced accuracy
- "Running" mode can be set to pause (write $B8 - DPB_CTRLS_0<3> = "1" to set pause and write $B8 - DPB_CTRLS_0<3> = "0" to end pause). Write $B8 - DPB_CTRLS_0<2> = "0" to disable "running" mode

The IQ compensation precision can be adjusted for a specific application ($B8 - DPB_CTRLS_0, b6-4)

IQ compensation “running” mode is not recommended to be run in presence of very strong interferers at the image frequency, because the image rejection result can be degraded from 80 dB to 50 dB. Since the power ratio of the interferer and the image channel signal at any time is unknown, IQ compensation using pilot signals is recommended to be used in this case as the result of calibration does not then depend on the interferer signal power.

The clock system provides test signals that can be injected into the receiver path to allow IQ calibration (see Pilot PLL, section 5.9.1). The Pilot signal frequency is placed at the mixer IF image (‘mirror’) to the central frequency of each range from Table 11 - Pilot Signal Coefficients.

The test signal from the pilot synthesizer is injected into the analogue IQ mixer and is down converted to the 1st IF (96 kHz or 120 kHz), amplified and filtered in the IF paths of I and Q channels. During the IQ calibration procedure, the IF gain control system may be in manual or automatic mode; because the pilot signal amplitude is constant in time and AGC state, this will be stable. In manual control mode the gain must be selected correctly in order to prevent ADC overloading.

It is recommended to start in automatic gain control mode and then switch to manual mode, when gain adjustment is finished. After the IF stage, the test signal is digitized by the ADC and enters the DPB block. The IQ imbalance compensation system is part of the DPB block and calculates two correction factors: phase and amplitude imbalance.

Phase error is calculated in the I-channel, with the correction factor β used to adjust the phase and is interpreted as a signed 16-bit fixed point value. Phase correction is carried out in the range [-57 °; 57 °] ((DPB_IQ_COMP_CORR_I_VAL<15:0>/2^{15})*(180/pi), step 0.0017°).

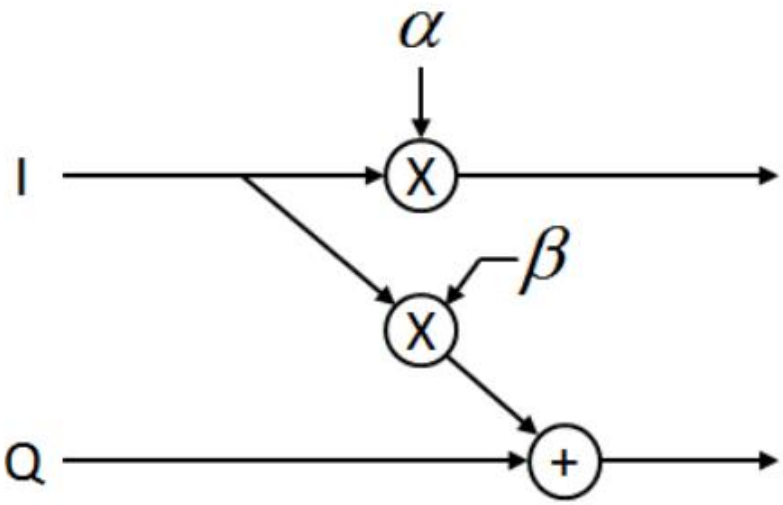


Figure 20 - **Calculation of Correction Factors**

Amplitude error is calculated in the Q-channel, with the correction factor α used to adjust the amplitude and is interpreted as a signed 16-bit fixed point value. The gain is adjusted in the range from 0 to 2, or approximately from -48 dB to +48 dB with step 0.0003dB:

$$\alpha = 10 \times \log10\left(\frac{1 + \text{DPB\_IQ\_COMP\_CORR\_Q\_VAL} < 15{:}0 > /2^{15}}{1 - \text{DPB\_IQ\_COMP\_CORR\_Q\_VAL} < 15{:}0 > /2^{15}}\right)$$

The time constant of the calibration is programmable ($51 – DPB_IQ_CFG, DPB_IQ_COMP_TC<2:0>). The IQ calibration can be repeated in iterative mode ($51 – DPB_IQ_CFG<7>, DPB_IQ_COMP_ITER = “1”) to use the previously calculated (in automatic mode) calibration values as the starting values for a new calibration round. In non-iterative mode ($51 – DPB_IQ_CFG<7>, DPB_IQ_COMP_ITER = “0”) each round is considered as a new one.

$51 – DPB_IQ_CFG - DPB_IQ_ROT<1:0> swaps upper sideband and lower sideband channels (image and wanted channels) at the compensation input and output.

The IQ imbalance compensation system can be used in automatic mode ($51 – DPB_IQ_CFG<1>, DPB_IQ_COMP_MD = “1”,) or manual mode ($51 – DPB_IQ_CFG<1>, DPB_IQ_COMP_MD=“0”), when user writes α and β values manually.

To run IQ calibration procedure in automatic mode (if Fif=96 kHz and IF sign="0" (Flo=Fc+Fif)) user should perform the following steps:

To run IQ Pilot mode calibration, the following sequence should be followed:

- Select normal, ECO or boost mode and write $03 – IC_Mode, Mode<2:0>
- Select channel bandwidth $0B – BANDWIDTH BW<2:0>
- Execute bandwidth calibration procedure: BW_ACS_EXE = "1"
- Make sure that the IQ imbalance compensation procedure in "running" mode is disabled: DPB_IQ_COMP_ON = "0" (bit 0, register $51) and DPB_CTRLS<1:0> = "0" (bit 1, register $B8).
- Select the Carrier frequency to be received and check which range it belongs to according to Table 11 - Pilot Signal Coefficients.
- Select the IF frequency value (Fif1 = 96 kHz) to the IC registers: Fif = "0"
- Select the IF frequency sign (Flo = Fc + Fif) to the IC registers: $08 – Fc_2<7>, Fif_SIGN = "0"
- Each range corresponds to pilot signal frequency (Fpilot in Table 11 - Pilot Signal Coefficients) calculated for Fif = 96 kHz and Flo = Fc + Fif, which is the image frequency of the Carrier frequency to be received, and to appropriate Fc value to be written to Fc_2, Fc_1 & Fc_0, Fc<20:0> registers

$$Fc = Fpilot - 2 \times Fif1 \text{ // if Fif\_SIGN = "0"}$$

- Write the Fc (value in 0.1 kHz) to Fc_2, Fc_1 & Fc_0, Fc<20:0>, with the selected IF and sign (registers $08 to $0A)
- Execute the LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = "1" ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to "0" (register $29 = 0x 05),
- Select calibration mode: write $03 – IC_Mode, Mode<2:0> = "5"
- Execute pilot signal generation procedure: PILOT_EXE = "1" in register $29 Wait until $29 – AUTO_EXE<3>, PILOT_EXE is reset to "0"
- Execute IQ calibration procedure: $29 AUTO_EXE, IQ_COMP_EXE = "1"

After calibration is completed, return to normal, ECO or boost mode (register $03).

Reception will then use the calculated calibration values automatically.

The calibration result is correct for the frequency range on which calibration was performed.

All other systems, including gain control systems, start working in automatic mode from this point, only the status registers / IRQ should be monitored.

Table 11 - Pilot Signal Coefficients

Band	Fc (MHz)	Fpilot (MHz)	PILOT_N	PILOT_P	Fc=Fpilot-2*96 kHz
VHF	> 102.4	108.8	17	3	108.608
	102.4 - 92.8	96	15	3	95.808
	92.8 - 83.2	89.6	14	3	89.408
	83.2 - 70.4	76.8	12	3	76.608
	70.4 - 60.8	65.28	17	5	65.088
	60.8 - 51.84	57.6	12	4	57.408
	51.84 - 40	46.08	12	5	45.888
HF	40 - 25.6	32	15	9	31.808

Band	Fc (MHz)	Fpilot (MHz)	PILOT_N	PILOT_P	Fc=Fpilot-2*96 kHz
	25.6 - 14.4	19.2	14	14	19.008
	14.4 - 6.4	9.6	14	28	9.408
	6.4 - 2.0	3.84	15	75	3.648
MF	2.0 - 1.33	1.8	15	160	1.608
	1.33 - 0.4	0.96	13	260	0.768
LF	0.4 - 0.256	0.5	15	576	0.308
	0.256>	0.39	13	640	0.198

- Each range corresponds to pilot signal frequency calculated for Fif=96 kHz and Flo = Fc + Fif, which is the image frequency of the Carrier frequency to be received, and to appropriate Fc value to be written to Fc_2, Fc_1 & Fc_0, Fc<20:0> registers

Fc = Fpilot – 2*Fif1 // if Fif_SIGN = “0”

Write the Carrier frequency (Fc, value in 0.1 kHz). to the IC registers: Fc_2, Fc_1 & Fc_0, Fc<20:0>

- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = “1” ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE have completed and are reset to "0"
- Select calibration mode: write $03 – IC_Mode, Mode<2:0> = “5”
- Execute pilot signal generation procedure: $29 – AUTO_EXE<3>, PILOT_EXE = “1”. Wait until PILOT_EXE is reset to “0”
- Execute IQ calibration procedure: $29 AUTO_EXE, IQ_COMP_EXE = “1”. Wait until IQ_COMP_EXE is reset to “0”
- After calibration is completed, return to normal, ECO or boost mode
- Calibration result is correct for frequency range on which calibration was performed

After the IQ calibration procedure is completed, calculated values of calibration coefficients are stored in the $56 & $57 DPB_IQ_COMP_CORR_I_VAL<15:0> and $58 & $59 DPB_IQ_COMP_CORR_Q_VAL<15:0> registers and are automatically used to correct the input data. Values from the registers may be read by the external host controller.

Advanced users may select manual mode ($51 – DPB_IQ_CFG<1> - DPB_IQ_COMP_MD = “0”). In this mode values of calibration coefficients must be written to $52 & $53 - DPB_IQ_COMP_MAN_CORR_I<15:0> and $54 & $55 DPB_IQ_COMP_MAN_CORR_Q<15:0> registers.

Note: Do not execute IQ calibration procedure ($29 AUTO_EXE, IQ_COMP_EXE) in manual mode.

The $D4 – DPB_STAT_2 - DPB_IQ_COMP_RDY signal is set to “1” at the end of the calibration.
If a restart of the calibration process is required, the $51 – DPB_IQ_CFG - DPB_IQ_COMP_ON control must be set to “0”, and when DPB_IQ_COMP_RDY is cleared, a new calibration cycle is activated by setting the DPB_IQ_COMP_ON control signal to “1”.

If Fif=120 kHz or/and IF sign = “1” (Flo=Fc-Fif), pilot signal frequency and also LO frequency values should be calculated according to the following procedure:

- Select normal, ECO or boost mode and write $03 – IC_Mode, Mode<2:0> value to the registers.
- Write IF frequency value (Fif1=96 kHz or 120 kHz) to the IC registers: Fif = “0” or “1”.
- Write IF sign (Flo = Fc + Fif or Flo = Fc - Fif) to the IC registers: $08 – Fc_2<7>, Fif_SIGN = “0” or “1”.
- Select channel bandwidth $0B – BANDWIDTH, BW<2:0>.

- Execute bandwidth calibration procedure: BW_ACS_EXE= “1”. Wait until IF_BW_ACS_EXE is reset to “0”.
- Make sure that IQ imbalance compensation procedure in “running” mode is disabled: DPB_IQ_COMP_ON = “0” and DPB_CTRLS<1:0> = “0”.
- Select Carrier frequency to be received and calculate pilot signal frequency, which is the image frequency of the Carrier frequency to be received, and pilot synthesizer integer coefficients ($99 & $9A PILOT_N and $9B & $9C PILOT_P):

  Fpilot = Fc + 2*Fif1= (Fref*PILOT_N)/(2*PILOT_P) // if Fif_SIGN = “0”
  Fpilot = Fc – 2*Fif1 = (Fref*PILOT_N)/(2*PILOT_P) // if Fif_SIGN = “1”

- After pilot synthesizer integer coefficients and Fpilot are known, calculate Fc to be written to Fc_2, Fc_1 & Fc_0, Fc<20:0> registers:

  Fc = Fpilot – 2*Fif1 // if Fif_SIGN = “0”
  Fc = Fpilot + 2*Fif1 // if Fif_SIGN = “1”

Write Fc (value in 0.1 kHz) to Fc_2, Fc_1 & Fc_0, Fc<20:0> registers.

- Execute LO PLL tuning procedure: $29 – AUTO_EXE<0>, PLL_CALC_EXE = “1” ($29 – AUTO_EXE<1>, PLL_SAS_EXE will be executed automatically along with PLL_CALC_EXE). Wait until PLL_CALC_EXE and PLL_SAS_EXE are reset to “0”.
- Select calibration mode: write $03 – IC_Mode, Mode<2:0> = “5”.
- Write calculated values of PILOT_N, PILOT_P coefficients to the IC registers: $99 & $9A PLL_PILOT_N<10:0>, $9B & $9C PLL_PILOT_P<10:0>.
- Execute IQ calibration procedure: $29 AUTO_EXE, IQ_COMP_EXE = “1”.
- After calibration is completed, return to normal, ECO or boost mode.
- Calibration result is correct for frequency range on which calibration was performed.

In continuous mode, IQ calibration will run in the usual way but does not stop when calibration coefficients are obtained. The routine continues to slowly adjust phase and amplitude.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings – Typical figures

Exceeding these maximum ratings can result in damage to the device.

ESD Warning: This high-performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

ESD ratings (HBM)	CBP and CBN:	500 V
	HF_IN, VHF_IN, LF_MF_INP, LF_MF_INN, LNA_FB,	500 V
	XTALn, XTAL/CLK, CLK_OUT/EXT_LO_IN;	500 V
	All other pins:	2000 V

	Min.	Max.	Units
Supply (AVDD – AVSS) or (IO_VDD – DVSS)	-0.3	+4.0	V
Voltage on any analogue pin to AGND pin	-0.3	TBD	V
Voltage on any digital pin to DGND pin	-0.3	TBD	V
Voltage between AGND and DGND pins	-50	+50	mV
Current into or out of DGND, VDDIO, VDDA, DVDD pins	-75	+75	mA
Current into or out of AGND (exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-20	+20	mA
RF Input level, HF_IN, VHF_IN, LF_MF_INP, LF_MF_INN pins	-	+10	dBm

Q5 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1820	mW
De-rating	–	18.2	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+90	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Analogue Supply (AVDD)	–	2.9	3.6	V
IO Supply (IO_VDD)	–	1.6	3.6	V
Operating Temperature	–	-20	+70	°C

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified: AVDD = IO_VDD = 3.3 V; AVSS = DVSS, T_{AMB} = +25°C.

DC parameters

DC Parameters	Notes	Min.	Typ.	Max.	Units
Power down mode (powersave)	–		30		µA
Operating Currents (Normal Mode)					
LF /MF mode	–		25.5		mA
HF mode	–		26.0		mA
VHF/FM mode	–		28.5		mA
Current from IO_VDD					
LF/MF mode	–		0.9		mA
HF mode	–		0.9		mA
VHF/FM mode	–		9.5		mA
Logic ‘1’ Input Level	–	70%			VDD_{IO}
Logic ‘0’ Input Level	–			30%	VDD_{IO}
Output Logic ‘1’ Level (I_{OH} = 0.6 mA)	–	80%			VDD_{IO}
Output Logic ‘0’ Level (I_{OL} = -1.0 mA)	–			+0.4	V

Main blocks operate in the following performance modes:

- Normal (typical parameters and current consumption);
- Boost (improvement of parameters by increasing current consumption);
- ECO (reducing current consumption when high performance is not needed).

AC parameters – LF Band System parameters

System parameters calculated according to “Minimum-Receiver-Requirements-MRR_v4.1” and for Normal operation mode unless otherwise specified.

Operation in the LF band (below 520 kHz) is inferred from MF testing and cannot be guaranteed.

Overall	Notes	Min.	Typ.	Max.	Units
LF band					
Input frequency	1	150		280	kHz
Sensitivity	2		4		dBuV EMF
Input impedance			>1		kΩ
Input signal dynamic range	2		107		dB
Adjacent channel selectivity	2				
at ±9 kHz offset			59.5		dB
at ±18 kHz offset			60.0		dB
at ±27 kHz offset			59.5		dB
at +64 kHz offset	3		60.0		dB
at ±36 - 400 kHz offset			60.0		dB
Far-off selectivity					
at ±400 kHz offset	2		72.0		dB
Blocking					
at ±100 kHz offset	2		62.3		dB
at ±400 kHz offset	2		60.5		dB
Intermodulation distortion immunity					
at -200 / -400 kHz offset	2		56.0		dB
at +200 / +400 kHz offset	2		55.0		dB
3rd order interception point					
at -200 /- 400 kHz offset	2		121.0		dBuV
at +200 / +400 kHz offset	2		119.4		dBuV

AC parameters – MF Band System parameters

Overall	Notes	Min.	Typ.	Max.	Units
MF band					
Input frequency	1	400		2000	kHz
Sensitivity	4		4		dBuV EMF
Input impedance			>1		kΩ
Input signal dynamic range	4		107		dB
Adjacent channel selectivity	4				
at ±9 kHz offset			59.5		dB
at ±18 kHz offset			60.0		dB
at ±27 kHz offset			59.5		dB
at +64 kHz offset	5		60.0		dB
at ±36 - 400 kHz offset			65.0		dB
Far-off selectivity					
at ±400 kHz offset	4		72.0		dB
Blocking					
at ±100 kHz offset	4		62.3		dB
at ±400 kHz offset	4		60.5		dB
Intermodulation distortion immunity					
at -200 / -400 kHz of interference frequency offset	4		56		dB
at +200 / +400 kHz of interference frequency offset	4		55		dB
3rd order interception point					
at -200 / -400 kHz offset	4		121.0		dBuV
at +200 / +400 kHz offset	4		119.4		dBuV

AC parameters – HF Band System parameters

Overall	Notes	Min.	Typ.	Max.	Units
HF band					
Input frequency	1	2.0		40	MHz
Sensitivity	6		-6.5		dBuV
Input impedance			50		Ω
Input signal dynamic range	6		116		dB
Adjacent channel selectivity	6				
at ±10 kHz offset			63.5		dB
at ±20 kHz offset			65.5		dB
at ±30 kHz offset			66.0		dB
at +64 kHz offset	7		64.0		dB
at ±40 - 400 kHz offset			68.1		dB
Far-off selectivity					
at ±400 kHz offset	6		69.5		dB
Blocking					
at ±100 kHz offset	6		65.8		dB
at ±400 kHz offset	6		69.5		dB
at ±4 MHz offset	6		72.0		dB
Intermodulation distortion immunity					
at - 200 / - 400 kHz offset	6		49.0		dB
at + 200 / + 400 kHz offset	6		49.0		dB
3rd order interception point					
at - 200 / - 400 kHz offset	6		109.8		dBuV
at + 200 / + 400 kHz offset	6		109.8		dBuV

AC parameters – VHF Band System parameters

Overall	Notes	Min.	Typ.	Max.	Units
VHF band					
Input frequency	1	40		108	MHz
Sensitivity	8		1		dBuV
Input impedance			50		Ω
Input signal dynamic range	8		110		dB
Adjacent channel selectivity	8				
at ±100 kHz offset			60.0		dB
at ±200 kHz offset			60.0		dB
at ±300 kHz offset			61.0		dB
at ±400 kHz offset			62.0		dB
Far-off selectivity	8, 9				
at ±800 kHz offset			64.0		dB
at ±400 kHz offset and 100 dBuV of interference level			62.5		dB
Blocking	8, 9				
at ±800 kHz offset			66		dB
at ±4 MHz offset and 100 dBuV of interference level			71		dB
Intermodulation distortion immunity	8				
at - 200 / - 400 kHz offset			51.0		dB
at +200 / + 400 kHz offset			51.0		dB
at – 400 / - 800 kHz offset			51.0		dB
at + 400 / + 800 kHz offset			52.0		dB
3rd order interception point	8				
at - 200 / - 400 kHz offset			106.1		dBuV
at + 200 / + 400 kHz offset			107.1		dBuV
at - 400 / - 800 kHz offset			106.6		dBuV
at + 400 / + 800 kHz offset			107.6		dBuV

Notes:

1. The IC can be tuned continuously between 150 kHz – 2 MHz for the LF/MF input, 2.0 – 40 MHz for HF and 40-108 MHz for VHF but is optimised for broadcast reception.
2. Demodulator requirements to SNR (AWGN channel model) according to "ETSI ES 201 980 Digital Radio Mondiale (DRM); System Specification": ≥ 14.9 dB in LF, MF and HF bands with 64-QAM modulation. ADC SINAD = 18 dB. Additional margins: 12 dB of Qn noise margin and AGC accuracy.
3. For Fif = 96 kHz.
4. Demodulator requirements to SNR (AWGN channel model) according to "ETSI ES 201 980 Digital Radio Mondiale (DRM); System Specification": ≥ 14.9 dB in LF, MF and HF bands with 64-QAM modulation. ADC SINAD = 18 dB. Additional margins: 12 dB of Qn noise margin and AGC accuracy.
5. For Fif = 96 kHz.
6. Demodulator requirements to SNR (AWGN channel model) according to "ETSI ES 201 980 Digital Radio Mondiale (DRM); System Specification": ≥ 14.9 dB in LF, MF and HF bands with 64-QAM modulation. ADC SINAD = 18 dB. Additional margins: 12 dB of Qn noise margin and AGC accuracy.
7. For Fif=96 kHz.
8. Demodulator requirements to SNR (AWGN channel model) according to "ETSI ES 201 980 Digital Radio Mondiale (DRM); System Specification": ≥ 7.9 dB for VHF band with 16-QAM modulation. ADC SINAD = 11 dB. Additional margins: 12 dB of Qn noise margin and AGC accuracy.
9. Peak factor 12dB.

AC parameters – FIR Filter

Receiver Selectivity post digital filter at baseband using default filter coefficients. These are specific to DRM and WBFM application, these filters are configurable by the user.

All bands

Bandwidth (kHz)	Rejection (dB)	Min. (kHz)	Typ. (kHz)	Max. (kHz)	Output Dividers M:N	Output Frame Rates (ks/s)	Mode	I2S Rate (ks/s)
5	-1	-	+/- 2.5	-	1 : 50	96	AM, DRM30	3840
	-50	-	+/- 3.22	-				
10	-1	-	+/- 5	-	1 : 25	96	AM, DRM30	3840
	-50	-	+/-6.44	-				
20	-1	-	+/- 10	-	2 : 25	96	AM, DRM30	3840
	-50	-	+/- 12.88	-				
100	-1	-	+/- 50	-	2 : 5	480	WBFM-Mono, DRM+	19200
	-50	-	+/-64.4	-				
200	-1	-	+/- 100	-	4 : 5	960	WBFM-Stereo, RDS	38400
	-50	-	+/- 128.8	-				

AC parameters – LF Path

First Stage Low Noise Amplifiers and IQ mixer	Notes	Min.	Typ.	Max.	Units
LF band					
Input frequency	–	150		280	kHz
Upper output cut-off frequency @ -1 dB					
Mode 1	10		112		kHz
Mode 2	11		137		kHz
Attenuation					
at 296 kHz, mode 1	10		4.4		dB
at 320 kHz, mode 2	11		3.8		dB
Input impedance (differential)	–		>1		kΩ
Maximum Input capacitor bank value	–		244		pF
Minimum Input capacitor bank value	–		3		pF
Capacitor bank resolution	–		12		bit
Capacitor bank LSB step size	-		65		fF
Capacitor bank tolerance				±15	%
Minimum voltage gain	–		-17.1		dBV
Maximum voltage gain	–		36.9		dBV
Gain step	–		1.2		dB
Intermodulation distortion					
Mode 1	10, 12		64.0		dB
Mode 1	10, 13		54.0		dB
3rd order intermodulation distortion					
Mode 1	10, 12		97.0		dBuV
Mode 1	10, 13		122.0		dBuV
Output differential signal	–		-	1	Vp-p

Notes:

10. Mode 1: AM and DRM signals; 96 kHz central frequency.
11. Mode 2: AM and DRM signals; 120 kHz central frequency.
12. At voltage gain 33 dB, Uin1=Uin2=65 dBuV, F1= ±200 kHz, F2= ±400 kHz.
13. At voltage gain 9 dB, Uin1=Uin2=95 dBuV, F1= ±9 kHz, F2 = ±18 kHz.

AC parameters – MF Band

First Stage Low Noise Amplifiers and IQ mixer	Notes	Min.	Typ.	Max.	Units
MF band					
Input frequency	–	0.4		2.0	MHz
Upper output cut-off frequency @ -1 dB					
Mode 1	14		112		kHz
Mode 2	15		137		kHz
Attenuation					
at 296 kHz, mode 1	14		4.4		dB
at 320 kHz, mode 2	15		3.8		dB
Input impedance (differential)	–		>1		kΩ
Maximum Input capacitor bank value	–		244		pF
Minimum Input capacitor bank value	–		3		pF
Capacitor bank resolution	–		12		bit
Capacitor bank LSB step size	-		65		fF
Capacitor bank tolerance				±15	%
Minimum voltage gain	–		-17.5		dBV
Maximum voltage gain	–		36.4		dBV
Gain step	–		1.25		dB
Intermodulation distortion					
Mode 1	14, 16		73.6		dB
Mode 1	14, 17		44		dB
Third order intermodulation distortion					
Mode 1	14, 16		102.8		dBuV
Mode 1	14, 17		123		dBuV
Output differential signal	–			1	Vp-p

Notes:

14. Mode 1: AM and DRM signals; 96 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
15. Mode 2: AM and DRM signals; 120 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
16. At voltage gain 32 dB, Uin1=Uin2=66 dBuV, F1= ±200 kHz, F2= ±400 kHz.
17. At voltage gain 3 dB, Uin1=Uin2=101 dBuV, F1= ±9 kHz, F2= ±18 kHz.

AC parameters – HF Band

First Stage Low Noise Amplifiers and IQ mixer	Notes	Min.	Typ.	Max.	Units
HF band					
Input frequency	–	2		40	MHz
Upper output cut-off frequency @ -1 dB					
Mode 1	18		112		kHz
Mode 2	19		137		kHz
Attenuation					
at 296 kHz, mode 1	18		4.4		dB
at 320 kHz, mode 2	19		3.8		dB
Input impedance	–		50		Ω
LNA Input switch isolation (HF)	-		43		dB
Minimum power gain	–		-21.5		dB
Maximum power gain	–		18.9		dB
Gain step	–		1		dB
Noise figure					
at 12 dB power gain	–		7		dB
at -5 dB power gain	–		23.3		dB
Intermodulation distortion					
Mode 1	18, 20		56.4		dB
Mode 1	18, 21		42.7		dB
Third order interception point					
Mode 1	18, 20		-11.8		dBm
Mode 1	18, 21		5.4		dBm
Output differential signal	–			1	Vp-p

Notes:

18. Mode 1: AM and DRM signals; 96 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
19. Mode 2: AM and DRM signals; 120 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
20. At power gain 11.9 dB, Pin1=Pin2= -40 dBm, F1= ±200 kHz, F2= ±400 kHz.
21. At power gain -6 dB, Pin1=Pin2= -16 dBm, F1= ±10 kHz, F2= ±20 kHz.

AC parameters – VHF Band

First Stage Low Noise Amplifiers and IQ mixer	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
VHF band					
Input frequency	–	40		108	MHz
Upper output cut-off frequency @ -1 dB					
Mode 3	22		154		kHz
Mode 4	23		179		kHz
Mode 5	24		231		kHz
Attenuation					
at 654 kHz, mode 3	22		7.3		dB
at 630 kHz, mode 4	23		6.4		dB
at 680 kHz, mode 5	24		4.9		dB
Input Impedance	–		50		Ω
LNA Input switch isolation (VHF)	-		33		dB
LNA Input switch isolation (VHF)	-		33		dB
Minimum power gain	–		-21.3		dB
Maximum power gain	–		19.9		dB
Gain step	–		1		dB
Noise Figure					
at 18 dB power gain	–		3.6		dB
at 2 dB power gain	–		16.5		dB
at -3 dB power gain	–		21.3		dB
Intermodulation distortion					
Mode 3	22, 25		56.9		dB
Mode 3	22, 26		41.6		dB
Third order interception point					
Mode 3	22, 25		-13.5		dBm
Mode 3	22, 26		1.8		dBm
Maximum output differential signal peak-to-peak voltage	–	1			Vp-p

Notes:

22. Mode 3: DRM mode ‘E’; 96 kHz central frequency, signal bandwidth 100 kHz.
23. Mode 4: DRM mode ‘E’; 120 kHz central frequency, signal bandwidth 100 kHz.
24. Mode 5: Analogue broadcast FM; 120 kHz central frequency, signal bandwidth 200 kHz.
25. At power gain 13.9 dB, Pin1=Pin2= -42 dBm, F1= ±200 kHz, F2= ±400 kHz.
26. At power gain -3 dB, Pin1=Pin2= -19 dBm, F1= ±100 kHz, F2= ±200 kHz.

AC parameters – IF Amplifier and Filter

IF amplifier and filter	Notes	Min.	Typ.	Max.	Units
Lower cut-off frequency @ -3 dB					
All modes	–		1.6		kHz
Upper cut-off frequency @ -2 dB					
Mode 1	27		112		kHz
Mode 2	28		137		kHz
Mode 3	29		154		kHz
Mode 4	30		179		kHz
Mode 5	31		231		kHz
Attenuation					
at 296 kHz, mode 1	27		7		dB
at 320 kHz, mode 2	28		5.5		dB
at 654 kHz, mode 3	29		12.4		dB
at 630 kHz, mode 4	30		9.5		dB
at 680 kHz, mode 5	31		8.3		dB
Minimum voltage gain	–		-1.6		dBV
Maximum voltage gain	–		29.4		dBV
Gain control range	–		31		dB
Gain step	–		1		dB
Noise figure					
at 29 dB voltage gain	–		10		dB
at 15.9 dB voltage gain	–		17.3		dB
at 9 dB voltage gain	–		21.9		dB
at 5 dB voltage gain	–		24.7		dB
at 0 dB voltage gain	–		28.1		dB
Input differential signal	32			1.2	Vp-p
Output differential signal	–			1.2	Vp-p
Output common mode voltage	–		0.9		V
Third order input intermodulation point					
Mode 1	27, 33		26.2		dBm
Mode 1	27, 34		-1.2		dBm
Mode 3	29, 35		20.9		dBm
Mode 3	29, 36		-5.5		dBm

Notes:

27. Mode 1: AM and DRM signals; 96 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
28. Mode 2: AM and DRM signals; 120 kHz central frequency, signal bandwidth 5, 10, 20 kHz.
29. Mode 3: DRM mode ‘E’; 96 kHz central frequency, signal bandwidth 100 kHz.
30. Mode 4: DRM mode ‘E’; 120 kHz central frequency, signal bandwidth 100 kHz.
31. Mode 5: Analogue broadcast FM; 120 kHz central frequency, signal bandwidth 200 kHz.
32. At voltage gain 0 dB.
33. At voltage gain 0 dB, Pin1=Pin2=-26.8 dBm, Um1=Um2=0.26 Vp-p, F1=296 kHz, F2=496 kHz.
34. At voltage gain 29.4 dB, Pin1=Pin2=-40 dBm, Um1=Um2=57 mVp-p, F1=296 kHz, F2=496 kHz.
35. At voltage gain 0 dB, Pin1=Pin2=-25 dBm, Um1=Um2=0.32 Vp-p, F1=296 kHz, F2=496 kHz
36. At voltage gain 30.1 dB, Pin1=Pin2=-43.5 dBm, Um1=Um2=38 mVp-p, F1=296 kHz, F2=496 kHz.

AC parameters – PLL

Fractional-N PLL	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
Clocks					
Reference frequency input (F_{REF})	37		38.4		MHz
Reference frequency input level (AC-coupled)	–	0.2		1.2	Vp-p
Internal crystal oscillator capacitance (pin to AVSS)	38		7		pF
Reference frequency input phase noise, crystal					
Fref = 38.4 MHz, 1 kHz offset	39		-127		dBc/Hz
Fref = 38.4 MHz, 10 kHz offset	39		-132.8		dBc/Hz
Reference frequency input phase noise, TCXO					
Fref = 38.4 MHz, 1 kHz offset	40		-135		dBc/Hz
Fref = 38.4 MHz, 10 kHz offset	40		-150		dBc/Hz
Synthesizer					
Quadrature local oscillator frequency range					
LF band	–	0.190		0.516	MHz
MF band	–	0.285		2.120	MHz
HF band	–	2.180		40.115	MHz
VHF band	–	39.93		108.07	MHz
Local oscillator phase noise					
LF band, 100 Hz offset	–		-150		dBc/Hz
LF band, 9 kHz offset	–		-169		dBc/Hz
LF band, 18 kHz offset	–		-169		dBc/Hz
LF band, 27 kHz offset	–		-168		dBc/Hz
LF band, 191 kHz offset	–		-169		dBc/Hz
LF band, 518 kHz offset	–		-182		dBc/Hz
MF band, 100 Hz offset	–		-136		dBc/Hz
MF band, 9 kHz offset	–		-155		dBc/Hz
MF band, 18 kHz offset	–		-155		dBc/Hz
MF band, 27 kHz offset	–		-154		dBc/Hz
MF band, 191 kHz offset	–		-155		dBc/Hz
MF band, 518 kHz offset	–		-167		dBc/Hz
HF band, 100 Hz offset	–		-112		dBc/Hz
HF band, 10 kHz offset	–		-131		dBc/Hz
HF band, 20 kHz offset	–		-131		dBc/Hz
HF band 30 kHz offset	–		-130		dBc/Hz
HF band, 190 kHz offset	–		-131		dBc/Hz
HF band, 10 MHz offset	–		-161		dBc/Hz
VHF band, 1 kHz offset	–		-120		dBc/Hz
VHF band, 100 kHz offset	–		-120		dBc/Hz
VHF band, 200 kHz offset	–		-122		dBc/Hz
VHF band, 500 kHz offset	–		-134		dBc/Hz
VHF band, 10 MHz offset	–		-151		dBc/Hz
Quadrature former (mixer) division ratio	–		4		–
VCO to QF frequency division ratio (L Divider)	–	3		2047	–
N-Divider (Integer mode)	-	16		2047	-
N-divider (Fractional mode)		20		2043	
Fractional divider resolution	-		24		Bit
Reference divider ratio (PLL_RDIV)	-	1		4	
PFD comparison frequency	-	9.6	38.4	38.4	MHz
External LO input level	41	-15	-10	-5	dBm
External LO frequency range	-	1500		1900	MHz

Notes:

37. Sinewave or clipped sinewave
38. The internal crystal oscillator capacitance is adjustable via register control, the absolute min/max will depend on device parasitics
39. GSX-223/X SM Crystal (Techpoint Golledge MP10435)
40. GTXO-203T/ES SM TCXO +1.8 V (Techpoint Golledge MP07688)
41. Assumed 50 Ohm source

AC parameters – Sigma Delta ADC

Sigma Delta ADC	Notes	Min.	Typ.	Max.	Unit
Delta sigma modulator sample rate	–		19.2		Ms/s
Input frequency range	–	20		220	kHz
Resolution (per LSB)	–		18.3		µV/bit
SINAD	42, 43				
BW = 10 kHz, ADC 2nd order mode	–		87.8		dB
BW = 10 kHz, ADC 4th order mode	–		109.0		dB
BW = 20 kHz, ADC 2nd order mode	–		85.3		dB
BW = 20 kHz, ADC 4th order mode	–		106.6		dB
BW = 100 kHz, ADC 2nd order mode	–		77.0		dB
BW = 100 kHz, ADC 4th order mode	–		98.0		dB
BW = 200 kHz, ADC 2nd order mode	–		71.4		dB
BW = 200 kHz, ADC 4th order mode	–		94.5		dB
SFDR	–		90		dB
Noise floor					
BW = 10 kHz, ADC 2nd order mode	–		-131.0		dBFS/Hz
BW = 10 kHz, ADC 4th order mode	–		-151.6		dBFS/Hz
BW = 20 kHz, ADC 2nd order mode	–		-131.3		dBFS/Hz
BW = 20 kHz, ADC 4th order mode	–		-149.9		dBFS/Hz
BW = 100 kHz, ADC 2nd order mode	–		-128.8		dBFS/Hz
BW = 100 kHz, ADC 4th order mode	–		-149.7		dBFS/Hz
BW = 200 kHz, ADC 2nd order mode	–		-126.4		dBFS/Hz
BW = 200 kHz, ADC 4th order mode	–		-149.6		dBFS/Hz
Common mode voltage	–		0.9		V
Maximum input voltage range	44			1	Vp-p
Current consumption					
IQ ADC 2nd order mode	–		2.4		mA
IQ ADC 4th order mode	–		3.6		mA

Notes:

42. The signal at the input to the ADC is at the maximum input signal level for the specified SINAD to apply. AVDD supply is stable.
43. ADC SC sample rate = 19.2 Ms/s.
44. Centred about AVDD/2 and measured at ADC input.

6.1.4 SPI/C-BUS/I2C Control Interface Description

The Serial Control interface (I2C or SPI/C-BUS) is used to read and change CMX918 data register information. It is intended for status monitoring, mode configuration and parameter adjustment. The device default interface type is I2C. The CMX918 SPI Slave only drives RDATA when transferring read data from a valid device address. This feature allows the CMX918 SPI/C-BUS pin connections to be potentially shared with other CML C-BUS slave devices.

To switch to SPI/C-BUS, a 'dummy' single byte command 'write' must be performed. At the start of the SPI/C-BUS data write, CSN should be asserted '0' and the data clock start. If 'CSN' is '0' and the data clock sends at least 8 clock '1' to '0' edges the device will switch to using the SPI/C-BUS control interface. The 'dummy' write data will be discarded. The SPI/C-BUS bus will be selected from this point until the next RESETN event. The bus will be 'active' to accept following command write events etc.

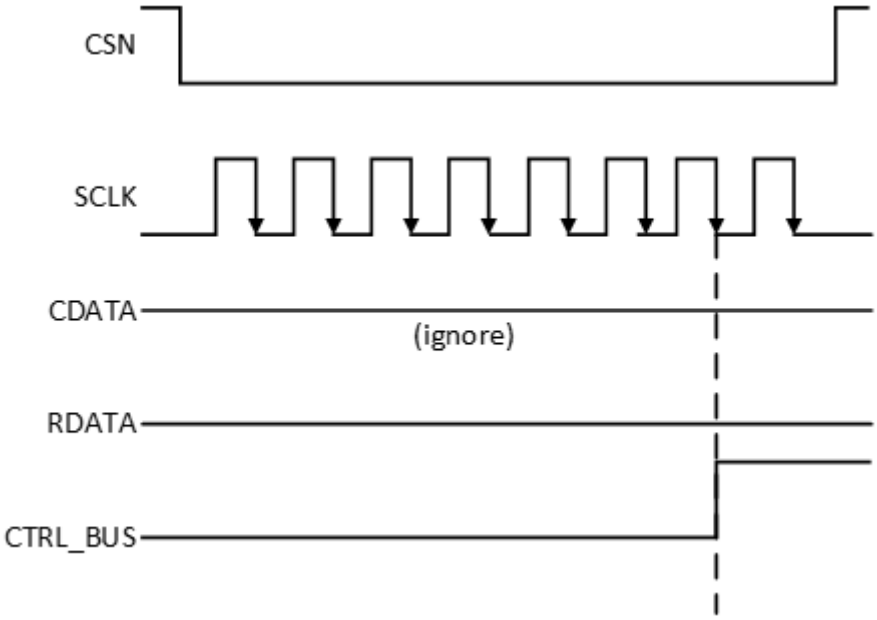


Figure 21 – SPI/C-BUS interface selection command

RESETN pin is pulled to 0 V to 'reset' the CMX918 device into a default state. Register $27 – PAD_SR_CTL<3:0> controls drive strength of interface output pads. The Register map has address REG_ADDR[7:0] in range from 0 to 255 (8 bit), which is treated differently depending on the selected interface. See further interfaces description for the details.

Status bits in the Register map are read-only and cannot be written. Non-defined bits in Register map are read as '0' and cannot be written.

6.2 I2C description

The CMX918 uses a 2-wire I2C-compatible serial slave interface consisting of a serial-data line (SDA) and a serial-clock line (SCK). The serial interface allows communication between CMX918 and the master at clock frequencies up to 400 kHz. The master initiates a data transfer on the bus and generates the SCK signal to permit data transfer. CMX918 behaves as slave device that transfers and receives data to and from the master. One bit is transferred during each SCK clock cycle. A minimum of nine clock cycles are required to transfer a byte in or out of the IC (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCK clock pulse. Changes in SDA while SCK is high and stable are considered as control signals. Both SDA and SCK remain high when the bus is not busy. Note that the I2C pins will not tolerate very slow rise/fall times, the timing parameters shown in Table 12 - I2C Timing (Fast mode) should be adhered to.

Slave does not perform clock-stretching and will not drive the SCL line.

6.2.1 Start and stop conditions

The master initiates a transmission with a START condition (S) which is a high-to-low transition on SDA while SCK is high. The master terminates a transmission with a STOP condition (P) which is a low-to-high transition on SDA while SCK is high.

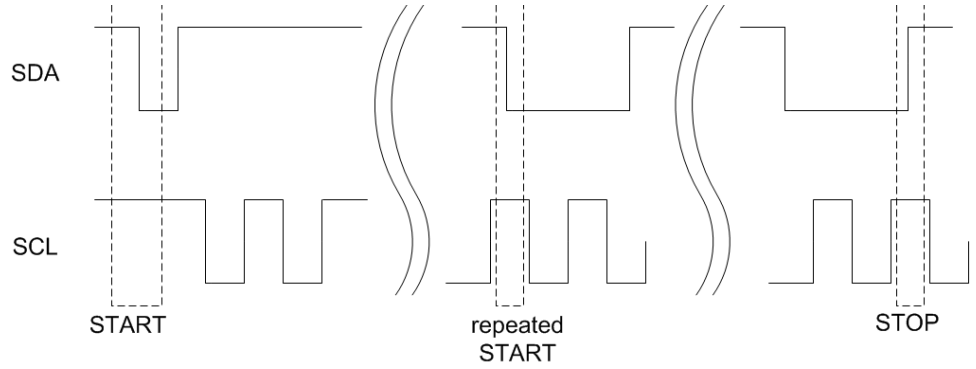


Figure 22 - I2C Start and Stop Conditions

6.2.2 ACK and NACK conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the IC (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows to capture unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

6.2.3 Slave address

The I2C address of the CMX918 is 0x55 (last 7 bits are “1010101” binary).
The eighth bit (R/W) following the 7-bit address determines whether a read or write operation will occur. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period; it is ready to accept or send data depending on the R/W bit (see the next “Command Format” section).
If the 7-bit Slave address does not match the defined value, device will remain idle until a new Start condition is generated.

6.2.4 Command format

Each transaction is initiated via Start condition followed by Slave address and R/W bit which indicates the direction of data transfer up to the next Stop condition (which terminates transfer) or Repeated Start condition.

Write register operation is a single-phase transaction indicated by '0' in R/W bit after Slave address. Next byte is a register address REG_ADDR[7:0], pointing at specific register in Register map. Register address is followed by register data to be written at selected address. Master controls further data transfer operation. Register address is internally incremented for each following byte received (up to 255), allowing multiple registers being written in a single transaction.

Read register operation is a two-phase transaction. First phase is indicated by '0' in R/W bit after Slave address. Next byte is a register address REG_ADDR[7:0], pointing at specific register in Register map. Second phase is initiated by a Repeated start condition (functionally identical to Start condition), Slave address and '1' in R/W bit, indicating that further data transfer direction is slave-to-master (excluding ACK/NACK). Following data byte is a register value at address set in the first phase of the transaction. Master indicates the end of the transaction by responding with NACK to a data byte, followed by Stop condition. Register address is internally incremented for each following byte received (up to 255), allowing multiple registers being read in a single transaction.

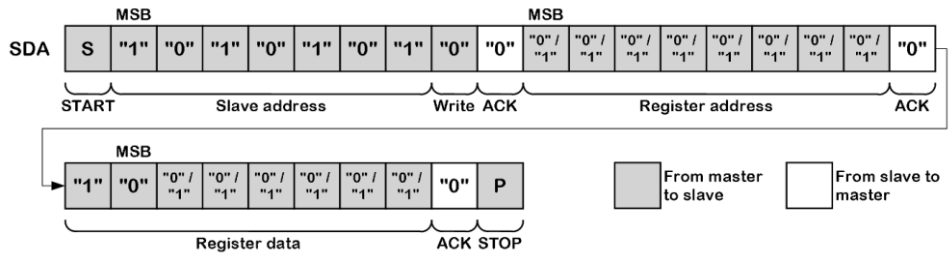


Figure 23 - Individual Registers Data Writing

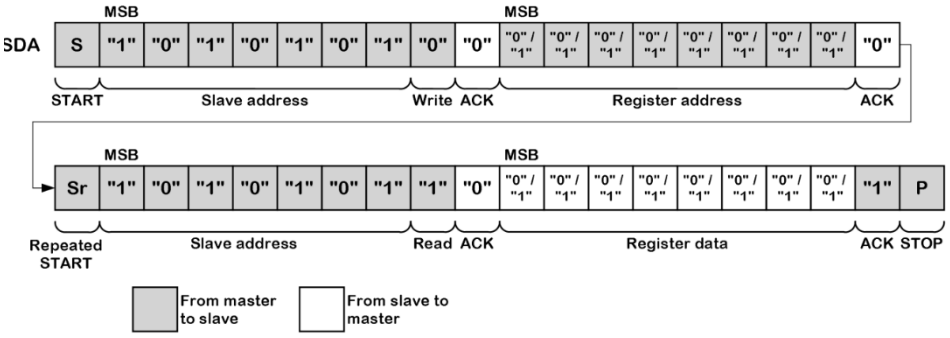


Figure 24 - Individual Register Data Reading

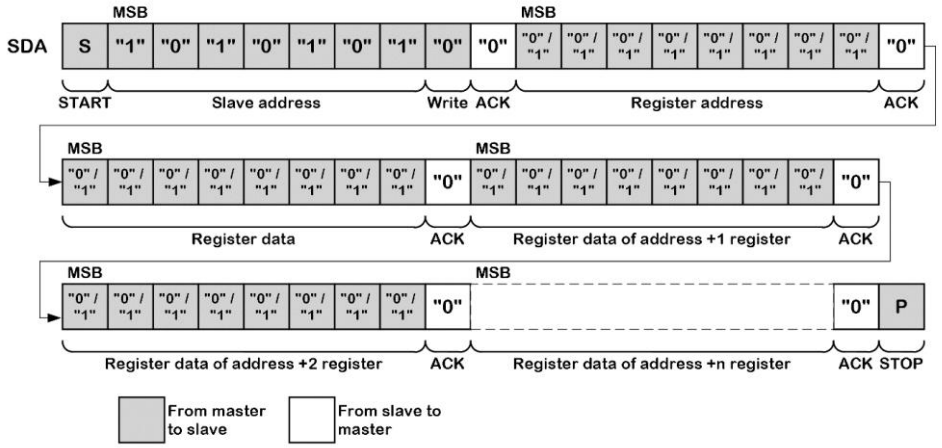


Figure 25 - Continuous Register Data Writing

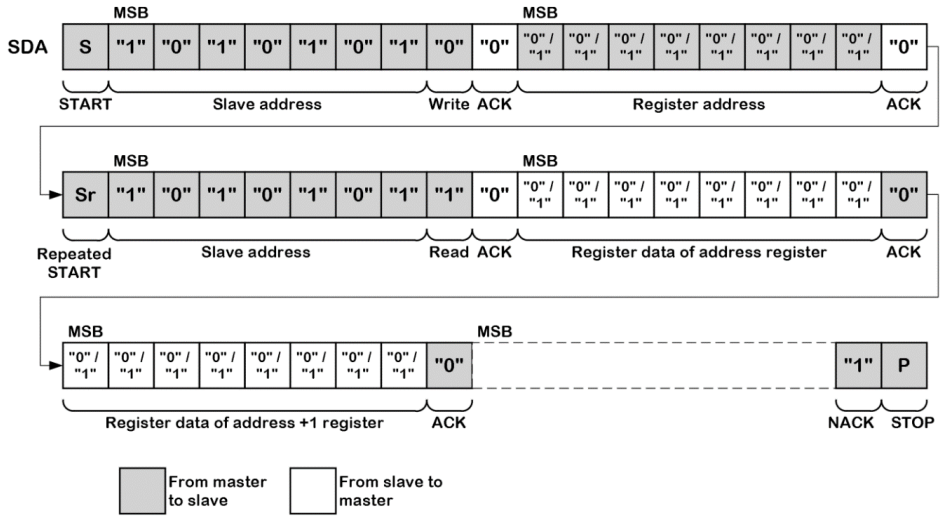


Figure 26 - Continuous Register Data Reading

6.2.5 Timing diagram

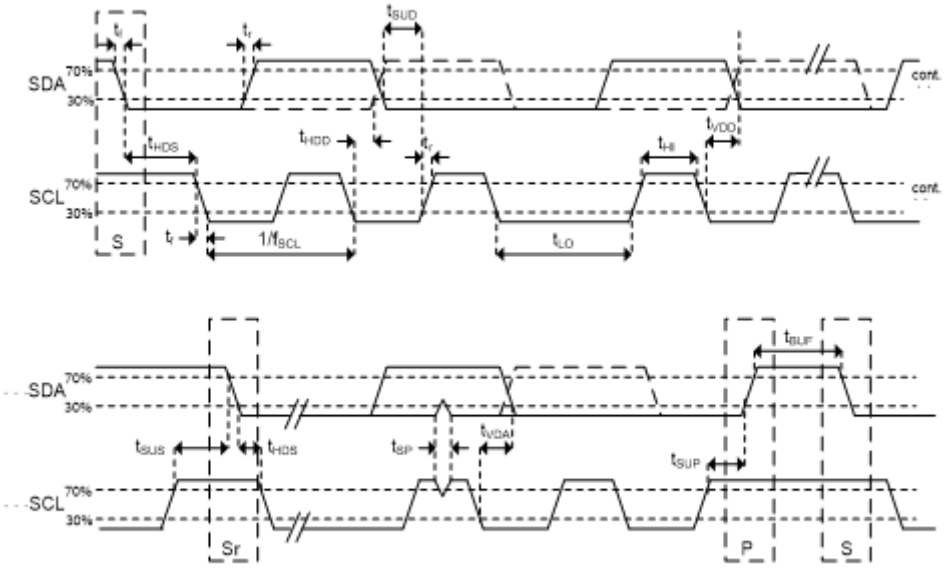


Figure 27 - I2C Timing Diagram

Table 12 - I2C Timing (Fast mode)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{HDS}	Hold time (repeated) START condition	0.6	-	-	µs
t_{LO}	Low period of SCL	1.3	-	-	µs
t_{HI}	High period of SCL	0.6	-	-	µs
t_{SUS}	Set-up time for repeated START condition	0.6	-	-	µs
t_{HDD}	Data hold time measured from falling edge of SCL	0	-	-	µs
t_{SUD}	Data set-up time measured from rising edge of SCL	0.1	-	-	µs
t_r	Rise time of SDA and SCL	-	-	0.3	µs
t_f	Fall time of SDA and SCL	-	-	0.3	µs
t_{SUP}	Set-up time for STOP condition	0.6	-	-	µs
t_{BUF}	Bus-free time between a STOP and START condition	1.3	-	-	µs
t_{VDD}	Data valid time	-	-	0.9	µs
t_{VDA}	Data valid acknowledge time	-	-	0.9	µs
t_{SP}	Pulse Width of Suppressed Spike	0	-	50	ns

6.3 SPI/C-BUS description

SPI/C-BUS - an SPI compatible serial bus, uses 4 pins for communication:

- CSN – serial interface enable chip select signal (low active)
- RDATA – serial interface output data
- CDATA – serial interface input data
- SCLK – serial interface clock (low when idle)

The serial interface allows communication between the IC and the master at clock frequencies up to 10 MHz. The master initiates a data transfer on the bus by driving CSN signal low and generates the SCLK signal to permit data transfer. The IC behaves as slave device that transfers and receives data to and from the master. One bit is transferred during each SCLK clock cycle. The RDATA output is disabled (high impedance) when the IC is not transmitting data.

A single transaction over SPI/C-BUS consists of two bytes, command/address and data. The command/address byte consists of a R/W bit that indicates the direction of data byte transfer and the 7-bit address C_ADDR[6:0].
In order to access register addresses greater than 127, bit 0 of the ADDRESS_PAGE register must be set to ‘1’.

REG_ADDR = ADDRESS_PAGE*128 + C_ADDR
ADDRESS_PAGE register can always be accessed by the interface with C_ADDR = 2.

6.3.1 Writing to register

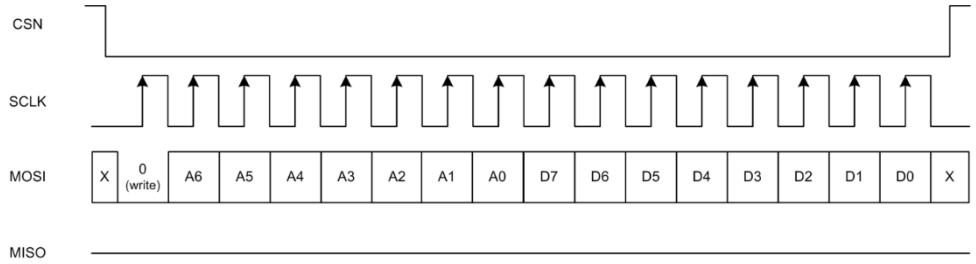


Figure 28 - Individual Register Writing

Single register write operation is shown in Figure 28 - Individual Register Writing. Communication is initialized by setting the Chip Select (CSN) pin low. Bytes are transmitted MSB first. Data bits are clocked into the IC, through the CDATA pin, on the rising edges of SCLK. The first bit of a command/address byte is a read/write attribute: read operation is defined by logic “1” and write operation is defined by logic “0”. Bits A6…A0 represent the page address C_ADDR. The second byte (D7…D0 bits) is data written to the given address register. After the 16th rising SCLK edge and turn-off CSN hold time, CSN goes high, disabling the interface.

6.3.2 Reading from register

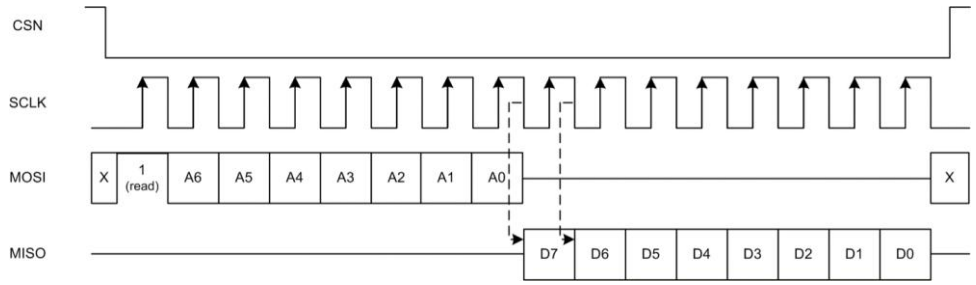


Figure 29 - Single Register Reading

Single register reading is similar to writing. The first byte is the command byte. Read attribute is logic “1” and A6–A0 bits specify the address of register to be read. Data is clocked out the IC, through the RDATA pin, on the falling edges of SCLK. Output data should be clocked on rising SCLK edges of the external SPI/C-BUS master. Bytes are transmitted MSB first. After sending the data byte, CSN goes high, disabling the interface.

6.3.3 Burst data transfer

The IC has a burst-mode data transfer. Unlike single data transfer, CSN continues to be “low” after the LSB of the data byte. The next bit after LSB is a write/read attribute. CSN goes high to stop the burst data transfer. The direction of data transfer can be changed an infinite number of times during burst data transfer. See examples below.

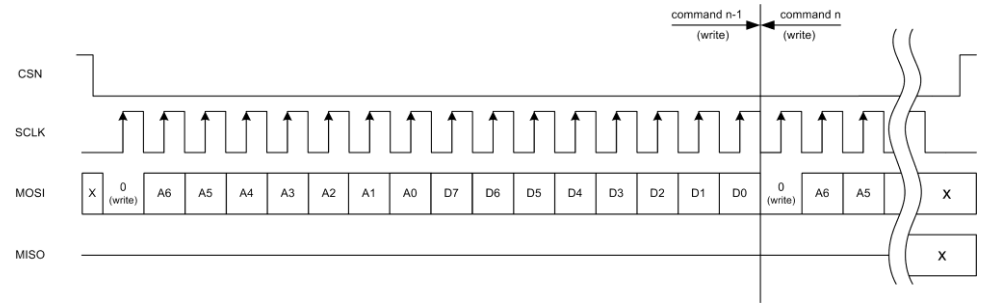


Figure 30 - Burst Data Writing

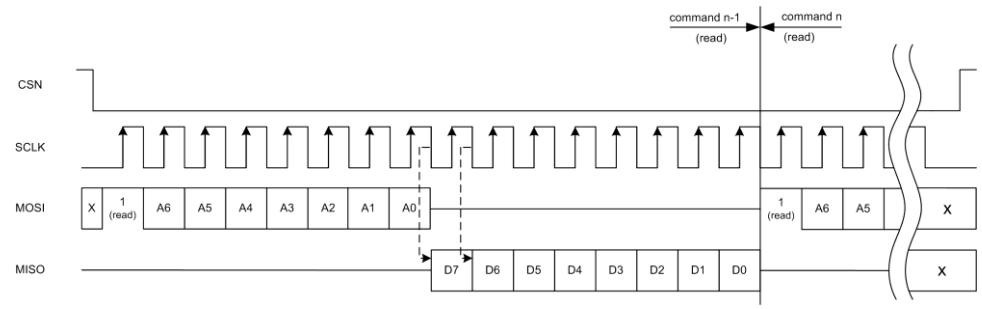


Figure 31 - Burst Data Reading

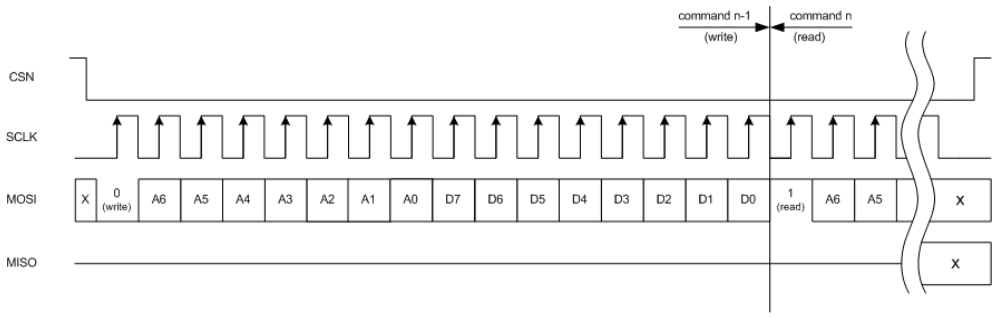


Figure 32 - Burst Data Writing and Reading

6.3.4 SPI/C-BUS Timing

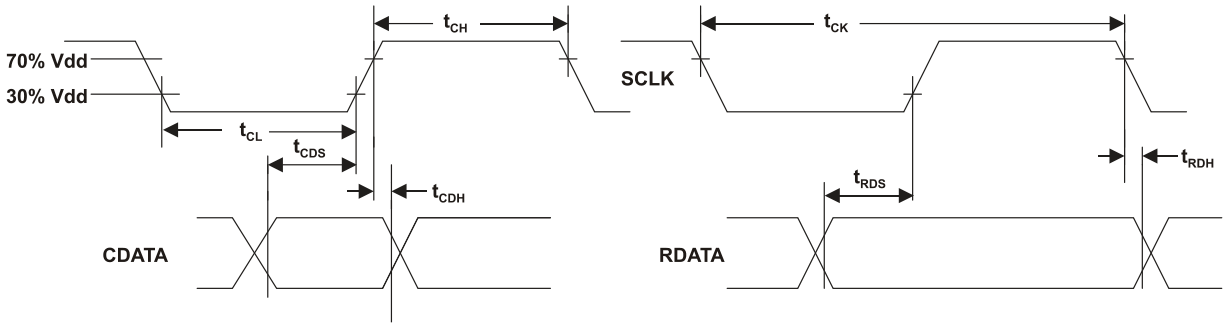


Figure 33 – SPI/C-BUS Timing

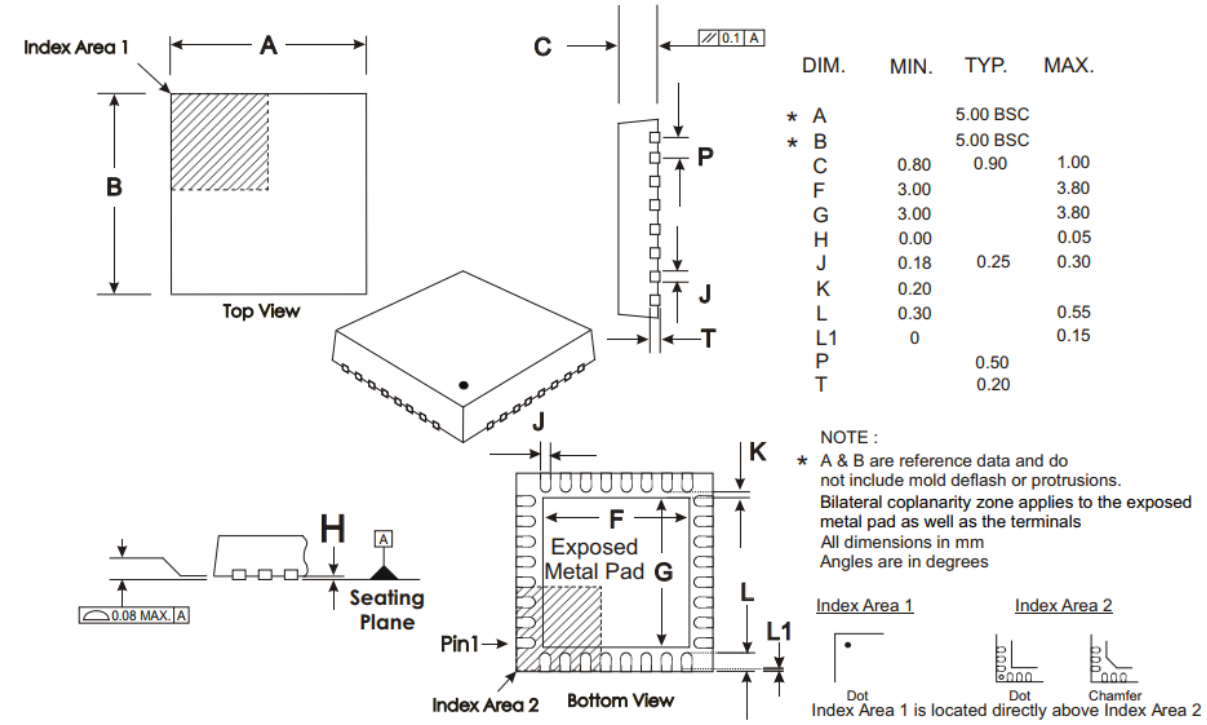
SPI/C-BUS Timings		Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time	100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time	100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time	0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time	–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions	1.0	–	–	µs
t_{NXT}	Inter-byte time	200	–	–	ns
t_{CK}	Clock-cycle time	200	–	100	ns
t_{CH}	Serial clock-high time	100	–	–	ns
t_{CL}	Serial clock-low time	100	–	–	ns
t_{CDS}	Command data set-up time	75.0	–	–	ns
t_{CDH}	Command data hold time	25.0	–	–	ns
t_{RDS}	Reply data set-up time	50.0	–	–	ns
t_{RDH}	Reply data hold time	0.0	–	–	ns

Notes:

1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. Unlike other C-BUS compatible ICs, SCLK must be low when inactive.
5. Maximum 30pF load on IRQN pin and each SPI/C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX918 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints

7 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 34 - Q5 Mechanical Outline

Order as part no. CMX918Q5

Handling precautions: This product includes input protection; however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed

Contact information

For further information please contact your local CML sales representative.

Contact details can be found at www.cmlmicro.com