Provisional Issue

CMX90A009 10W 136 – 1000 MHz Power Amplifier

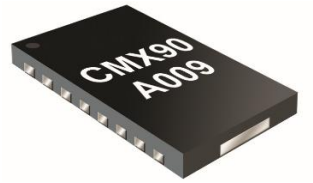
Description

The CMX90A009 is a high efficiency single-stage GaAs HBT power amplifier in thermally enhanced DFN package, delivering +40.0 dBm (10 W) of output power with >60 % efficiency at 435 MHz and 7.4 V.

CMX90A009 requires external matching at both input and output to optimize performance for each application and frequency band. The measured data presented in this document is based on the evaluation board (EV90A009).

The wide supply voltage range of 6 – 9.5 V makes the CMX90A009 suitable for dual-cell Lithium batteries and on-chip active bias maintains operation over temperature.

CMX90A009 is intended as the output stage in a high-power amplifier, combined with CMX90A007 driver to provide a complete line-up solution. Support for complex modulation such as π/4 DQPSK and QAM can be achieved with CMX998 Cartesian feedback loop IC.

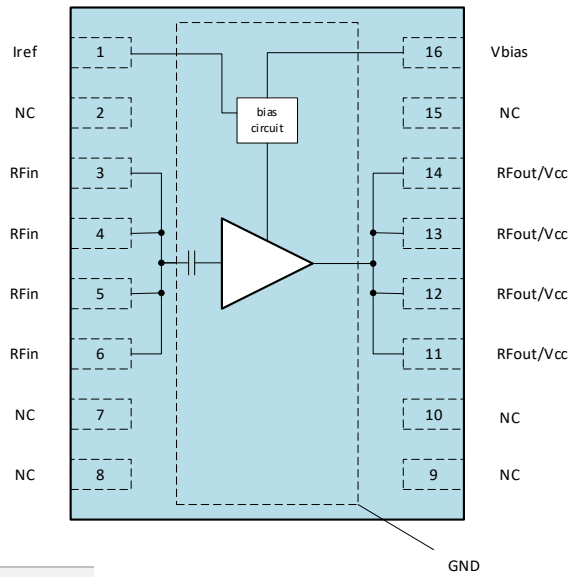


4x5mm VDFN-16L Package

Product Features

- Frequency range 136 – 1000 MHz
- Supply voltage 6 – 9.5 V
- P3dB +40 dBm @ 435 MHz, Vcc =7.4 V
- Small signal gain 17.5 dB
- High collector efficiency 60 % @ P3dB
- On-chip active bias circuit
- Saturated and linear operation
- OIP3 +45 dBm @ +33 dBm/tone at 435 MHz

Block Diagram



Applications

- Critical communications
- PMR / LMR hand-portable
- Two-way radio (analogue / digital)
- Public safety TETRA / P25
- Wireless data modem / network
- VHF / UHF / 915 MHz ISM band
- Marine radio / AIS

Ordering Information

Part Number	Description
CMX90A009QK-R710	7” Reel with 1,000 pieces
CMX90A009QK-R350	13” Reel with 5,000 pieces
EV90A009	Evaluation board (400 – 470 MHz)

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+33 dBm
Device Voltage (Vcc)	+10 V
Case Temperature (Tc)	-40 to +85 °C
Junction Temperature (Tjmax)	200 °C (MTTF = 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM > 250 V (Class 1A); CDM >1k V (Class C3)
MSL Level	Level 3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	6.05 °C/W at Tc = 85 °C

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	136		1000	MHz
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vcc)	6.0	7.4	9.5	V
Bias Voltage (Vbias)	6.0	7.4	9.5	V

The device will be tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A009 incorporates ESD protection circuitry. However, ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices and evaluation kits supplied by CML Micro are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances.

Electrical Specification

Measured results on the EV90A009 evaluation board including PCB losses. Matching optimised for specified operating band or frequency.

Vcc = Vbias = +7.4 V, Vref = +3.15V, Icq = Icc + Ibias, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Quiescent Current (Icq)	RF OFF	1		136		mA
Standby Current	Vcc current in standby mode, RF OFF			< 5		uA
Vbias Current	RF OFF			1.8		mA
Vref1, 2 (Standby)	PA placed into standby mode		0		1.5	V
Vref Current	See applications section for further details.			3.6		mA

Notes
1. Bias setting resistor as application circuit in application information section, R2 in Figure 50.

Operating Characteristics 400 - 470 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			400		470	MHz
P3dB				40		dBm
Psat				41.5		dBm
Small Signal Gain	Pin = -20 dBm			17.5		dB
Large Signal Gain	435 MHz, P3dB			14.5		dB
Collector Efficiency (η)	435 MHz, P3dB			60		%
OIP3	435 MHz, Pout = +33 dBm/tone			45		dBm
Current Consumption (Icc)	435 MHz, P3dB			2.1		A
Vbias Current	435 MHz, Pout = P3dB			35		mA
Input Return Loss	Pin = -20 dBm			20		dB
2nd Harmonic (2Fo)	400 MHz, P3dB			-30		dBc
3rd Harmonic (3Fo)	400 MHz, P3dB			-60		dBc
Output Load VSWR, Ruggedness	All phase angles, no damage	2		5:1		VSWR
Output Load VSWR, Stability	Spurious <-36dBm RBW – 100 kHz All phase angles	2		3:1		VSWR
Turn-On Time	Vref = 0 V to 4 V			TBD		ns
Turn-Off Time	Vref = 4 V to 0 V			TBD		ns

Notes
2. Common settings / parameters; Vcc = Vbias = 7.4 V, Pout = P3dB

Operating Characteristics 136 - 174 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			136		174	MHz
P3dB				39.8		dBm
Psat				40.6		dBm
Small Signal Gain	Pin = -20 dBm			18.8		dB
Large Signal Gain	155 MHz, P3dB			15.8		dB
Collector Efficiency (η)	155 MHz, P3dB			52		%
OIP3	155 MHz, Pout = +33 dBm/tone			45		dBm
Current Consumption (Icc)	155 MHz, P3dB			2.7		A
Vbias Current (Ibias)	155 MHz, P3dB			38		mA
Input Return Loss	155 MHz, Pin = -20 dBm			15		dB
2nd Harmonic (2Fo)	155 MHz, P3dB			-40		dBc
3rd Harmonic (3Fo)	155 MHz, P3dB			-60		dBc
Output Load VSWR, Ruggedness	P3dB, all phase angles, no damage	2		5:1		VSWR
Output Load VSWR, Stability	Spurious <-36dBm RBW – 100 kHz All phase angles	2		3.5:1		VSWR

Operating Characteristics 900 - 930 MHz

Zo = 50 Ω, Vcc = Vbias = +7.4 V, Vref = +3.15V, Ta = +25 °C (unless otherwise noted)

Parameter	Conditions	Notes	Min	Typ	Max	Units
Frequency			900		930	MHz
P3dB				39.5		dBm
Psat				40		dBm
Small Signal Gain	Pin = -20 dBm			15		dB
Large Signal Gain	915 MHz, P3dB			12		dB
Collector Efficiency (η)	915 MHz, P3dB			60		%
OIP3	915 MHz, Pout = +33 dBm/tone			43		dBm
Current Consumption (Icc)	915 MHz, P3dB			1.8		A
Vbias Current (Ibias)	915 MHz, P3dB			30		mA
Input Return Loss	Pin = -20 dBm			15		dB
2nd Harmonic (2Fo)	915 MHz, P3dB			-30		dBc
3rd Harmonic (3Fo)	915 MHz, P3dB			-58		dBc
Output Load VSWR, Ruggedness	P3dB, all phase angles, no damage	2		5:1		VSWR
Output Load VSWR, Stability	Spurious <-36dBm RBW – 100 kHz All phase angles	2		3:1		VSWR

Pin Assignments

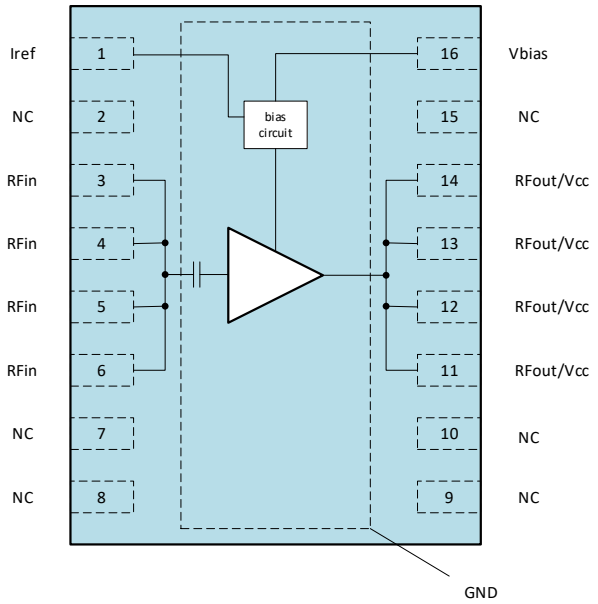


Figure 1 - Top View

Pin	Name	Description
1	Iref	Sets bias current. Regulated voltage and external series resistor required. Can also be used for on/off and power control.
2	NC	Connect to GND
3	RFin	RF input. An external input match to 50 Ω. Integrated DC blocking capacitor.
4	RFin	RF input. An external input match to 50 Ω. Integrated DC blocking capacitor.
5	RFin	RF input. An external input match to 50 Ω. Integrated DC blocking capacitor.
6	RFin	RF input. An external input match to 50 Ω. Integrated DC blocking capacitor.
7	NC	Connect to GND
8	NC	Connect to GND
9	NC	Connect to GND
10	NC	Connect to GND
11	RFout/Vcc	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc to be applied using external bias feed. Pin 11, 12, 13 & 14 to be connected on PCB.
12	RFout/Vcc	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc to be applied using external bias feed. Pin 11, 12, 13 & 14 to be connected on PCB.
13	RFout/Vcc	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc to be applied using external bias feed. Pin 11, 12, 13 & 14 to be connected on PCB.
14	RFout/Vcc	RF output. External matching to 50 Ω and DC-blocking capacitor required. Vcc to be applied using external bias feed. Pin 11, 12, 13 & 14 to be connected on PCB.
15	NC	Connect to GND
16	Vbias	Supplies current to bias circuit.
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

CML recommends that all no connect (NC) pins are connected to ground.

The bottom exposed die pad must be connected to the ground plane on the board, note guidance given in the application information section.

Typical Performance

The following plots show typical performance characteristics of CMX90A009 measured on the evaluation board (Part Number - EV90A009).

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

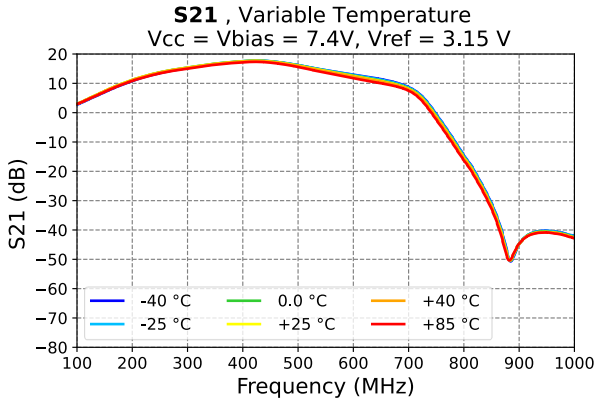


Figure 2 - Small Signal Gain (S21)

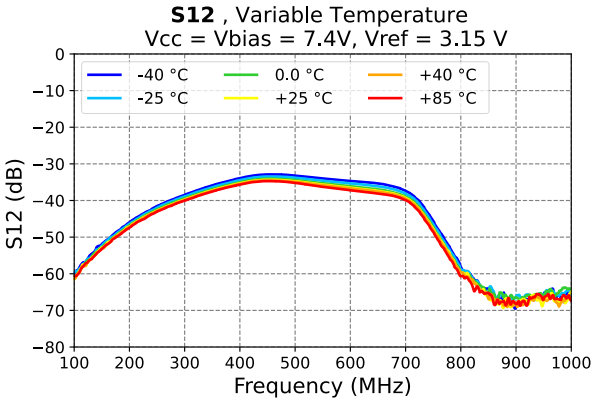


Figure 3 - Reverse Isolation (S12)

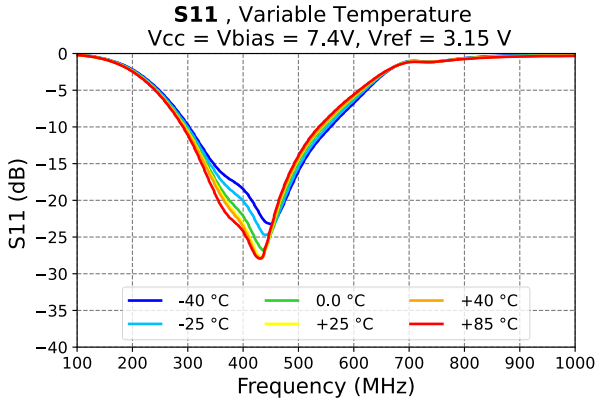


Figure 4 - Input Return Loss (S11)

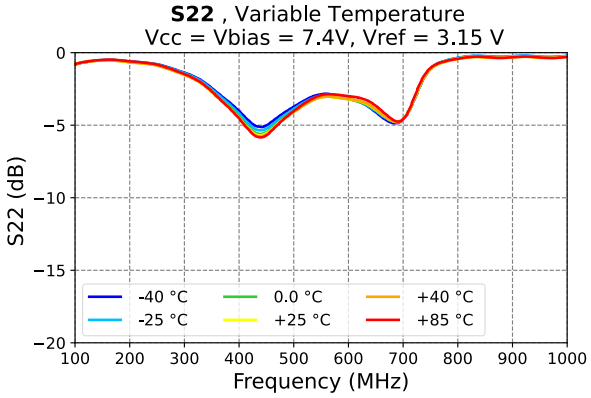


Figure 5 - Output Return Loss (S22)

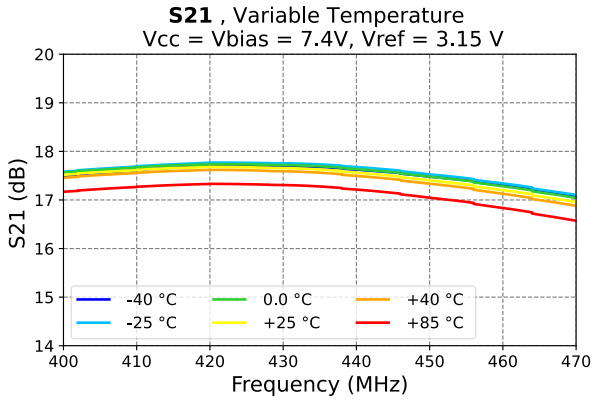


Figure 6 - Small Signal Gain (S21)

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

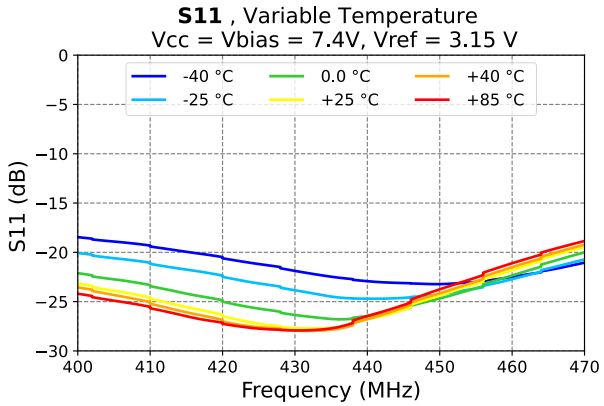


Figure 7 - Input Return Loss (S11)

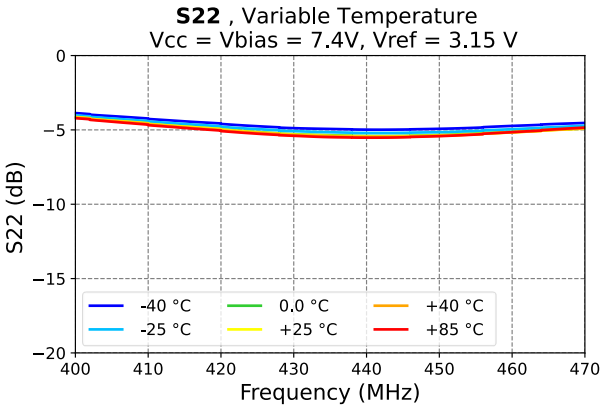


Figure 8 - Output Return Loss (S22)

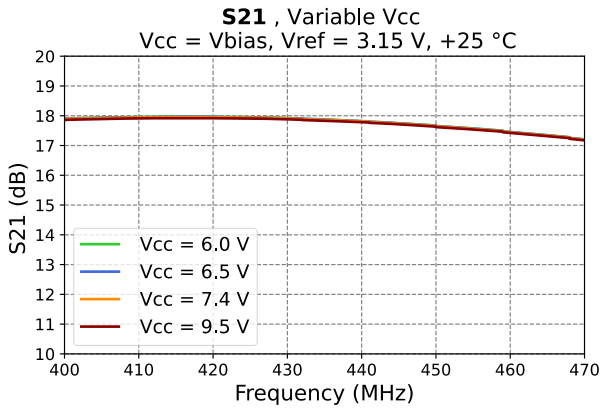


Figure 9 - Small Signal Gain vs. Vcc

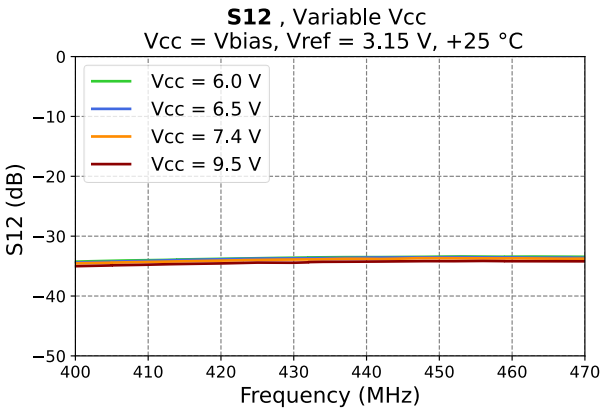


Figure 10 - Reverse Isolation vs. Vcc

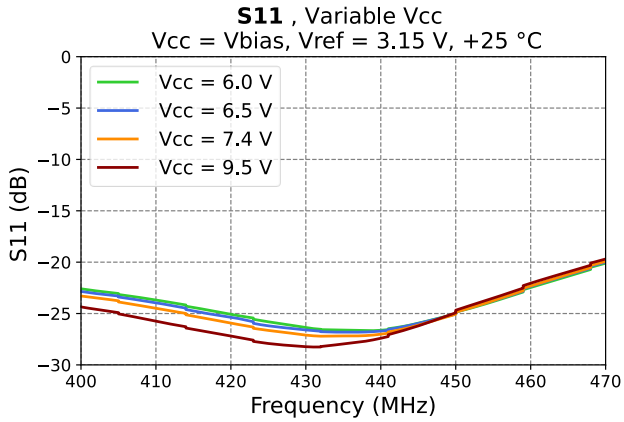


Figure 11 - Input Return Loss vs. Vcc

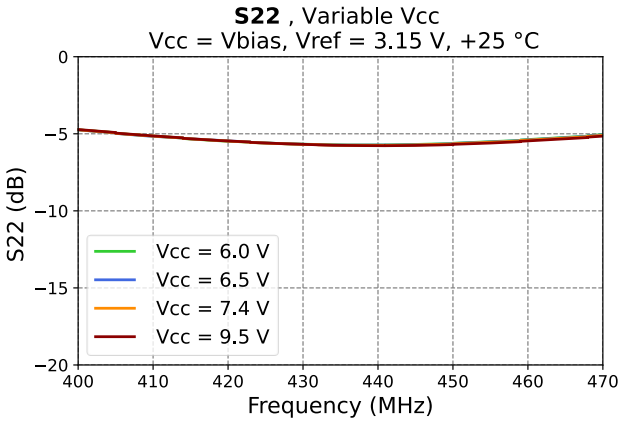


Figure 12 - Output Return Loss vs. Vcc

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

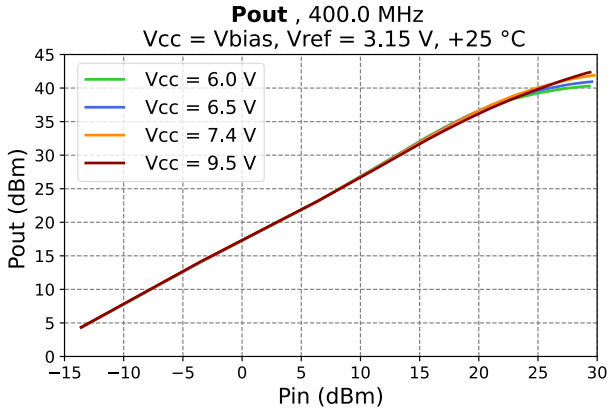


Figure 13 - Output Power vs. Input Power at 400 MHz

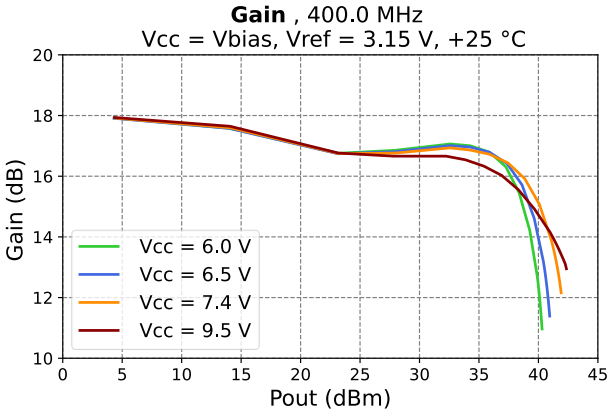


Figure 14 - Gain vs. Output Power at 400 MHz

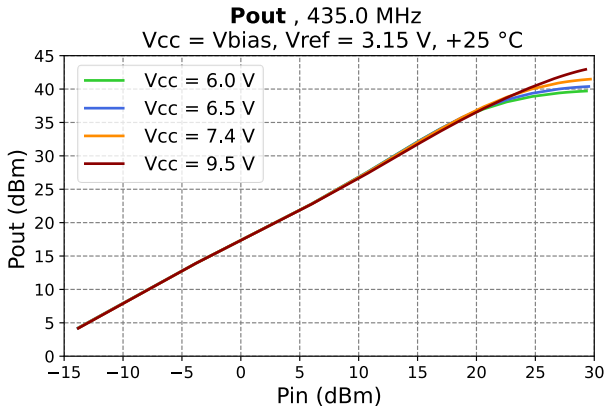


Figure 15 - Output Power vs. Input Power at 435 MHz

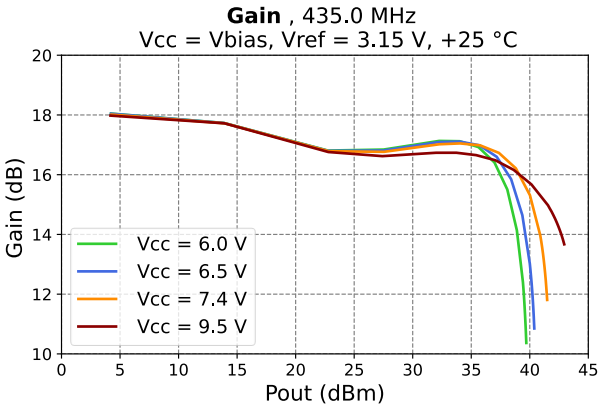


Figure 16 - Gain vs. Output Power at 435 MHz

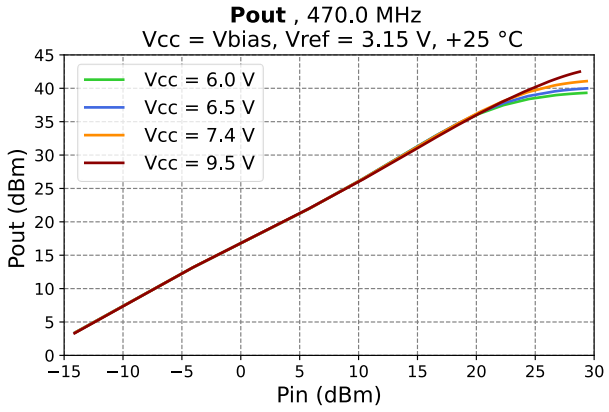


Figure 17 - Output Power vs. Input Power at 470 MHz

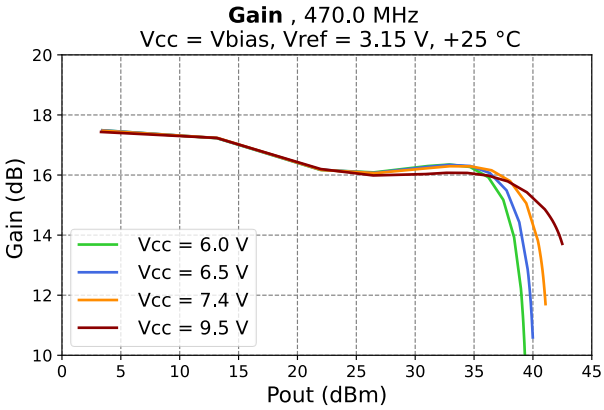


Figure 18 - Gain vs. Output Power at 470 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

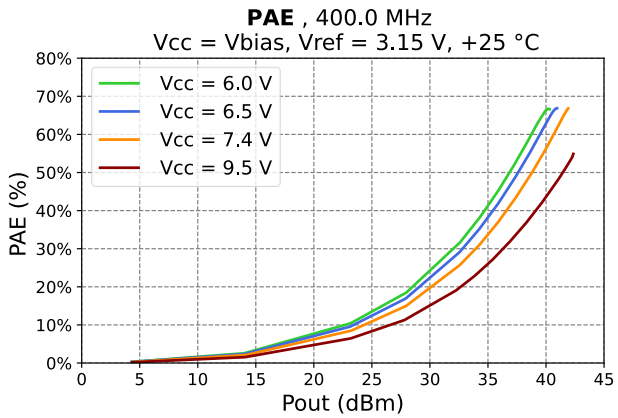


Figure 19 - PAE vs. Output Power at 400 MHz

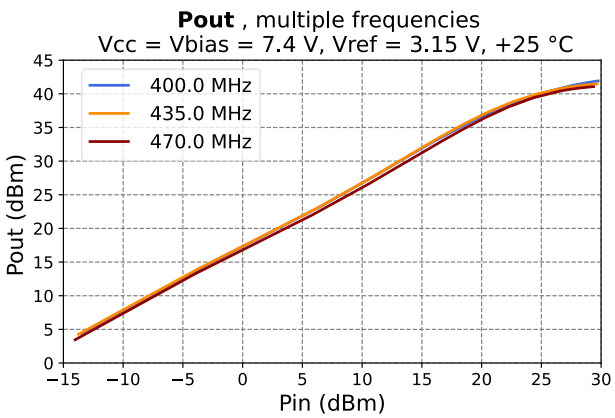


Figure 20 - Output Power vs. Input Power

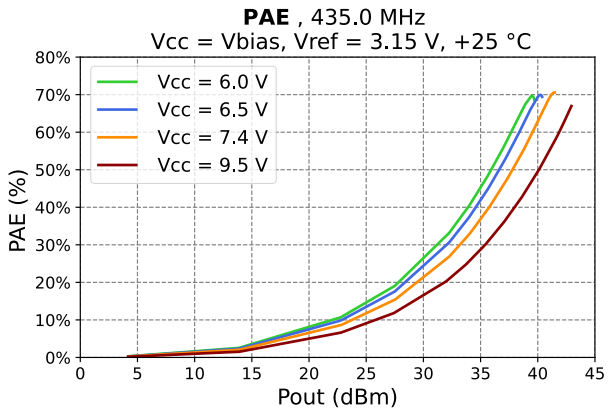


Figure 21 - PAE vs. Output Power at 435 MHz

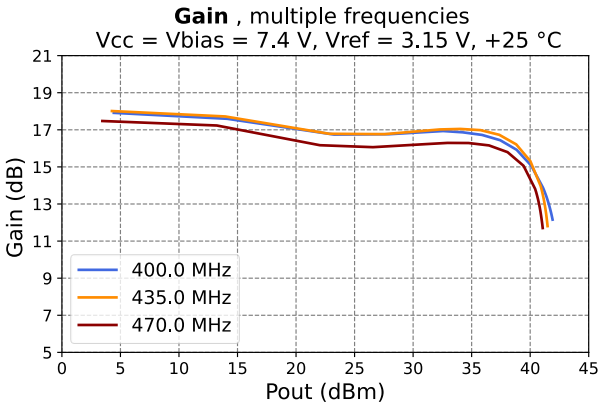


Figure 22 - Gain vs. Output Power

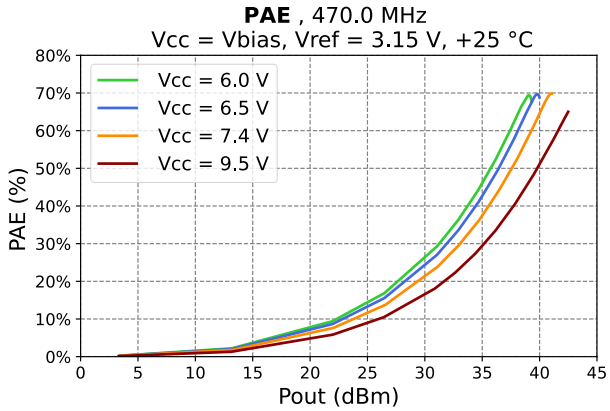


Figure 23 - PAE vs. Output Power at 470 MHz

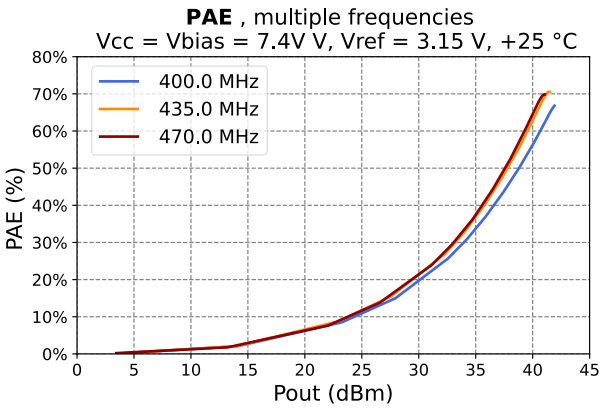


Figure 24 - PAE vs. Output Power

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

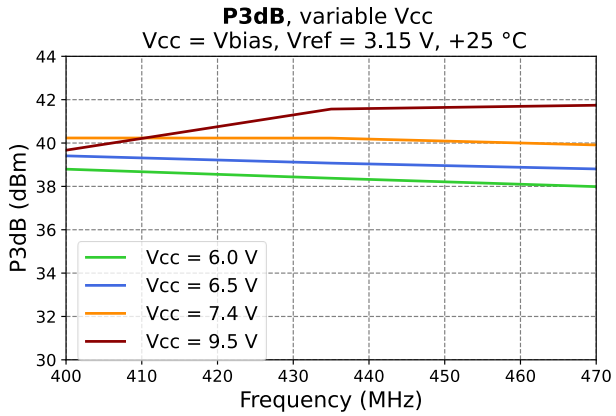


Figure 25 – P3dB vs. Frequency

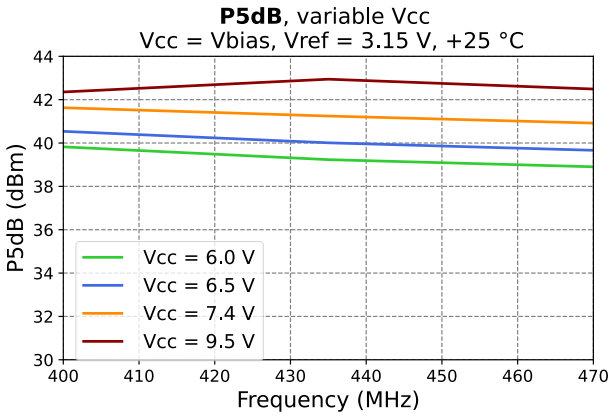


Figure 26 - Psat vs. Frequency

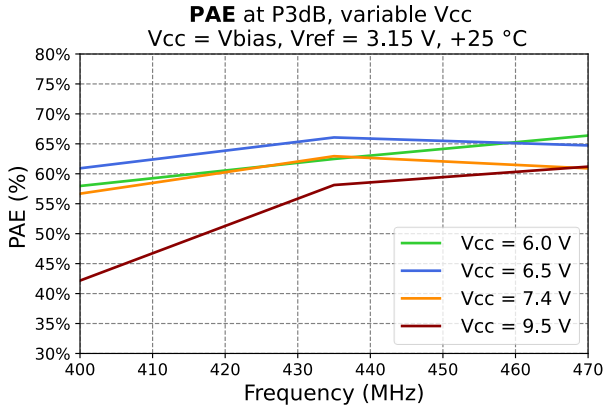


Figure 27 - PAE at P3dB

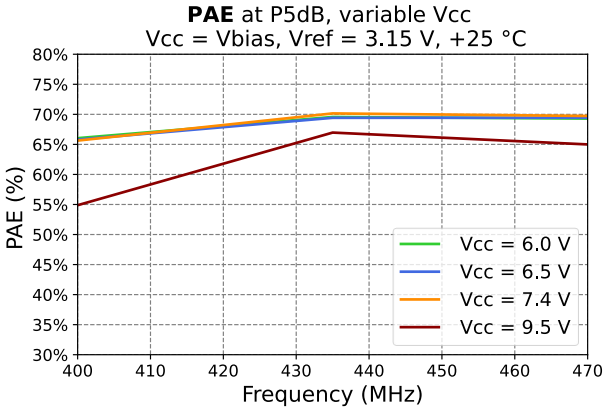


Figure 28 - PAE at Psat

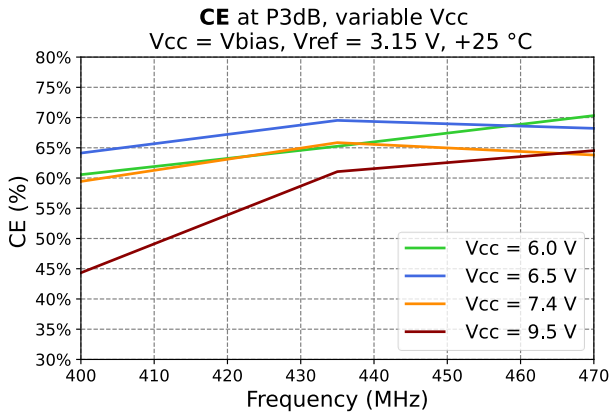


Figure 29 - Collector Efficiency at P3dB

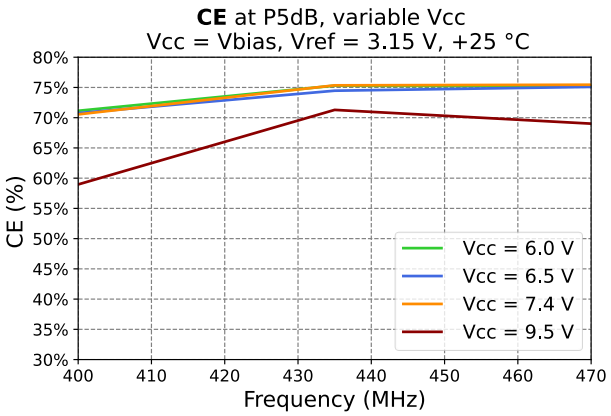


Figure 30 – Collector Efficiency at Psat

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

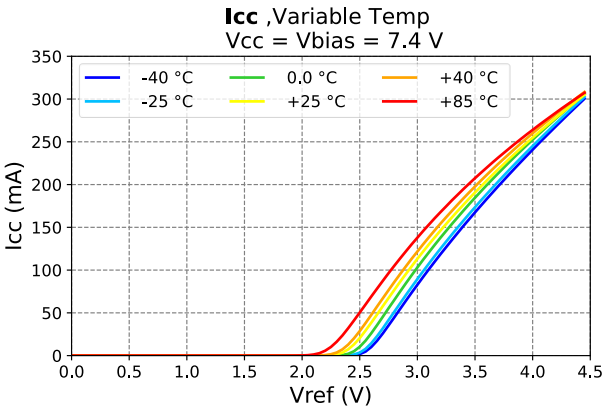


Figure 31 - Icc vs. Vref over Temp

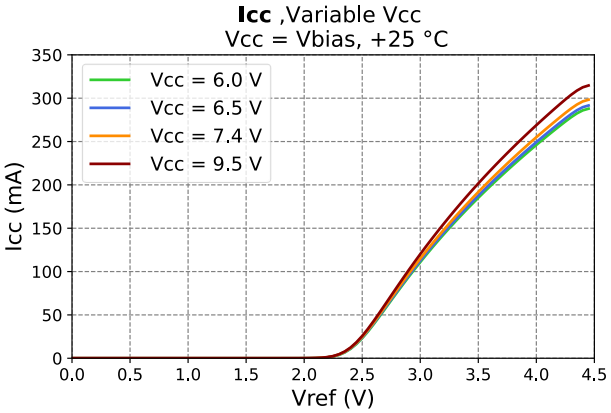


Figure 32 - Icc vs. Vref over Vcc

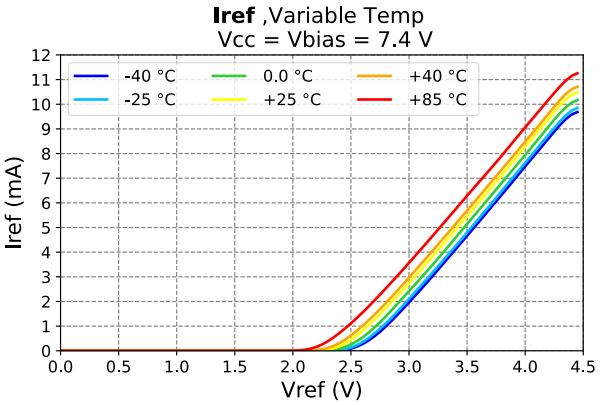


Figure 33 - Iref vs. Vref over Temp

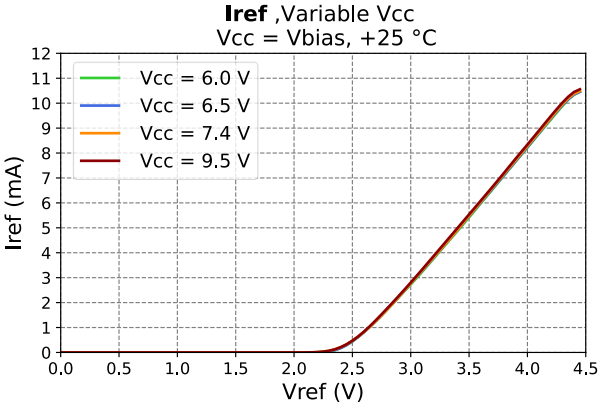


Figure 34 - Iref vs. Vref over Vcc

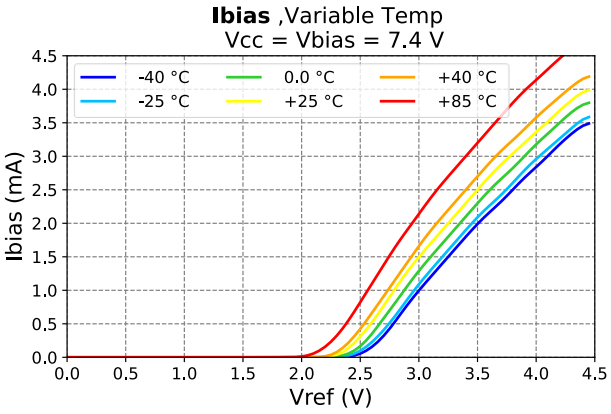


Figure 35 - Ibias vs. Vref over Temp

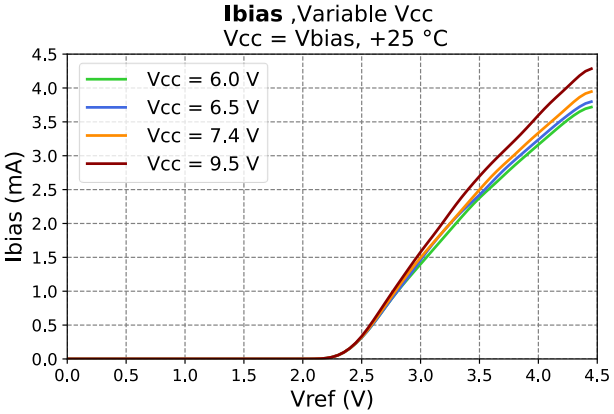


Figure 36 - Ibias vs. Vref over Vcc

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

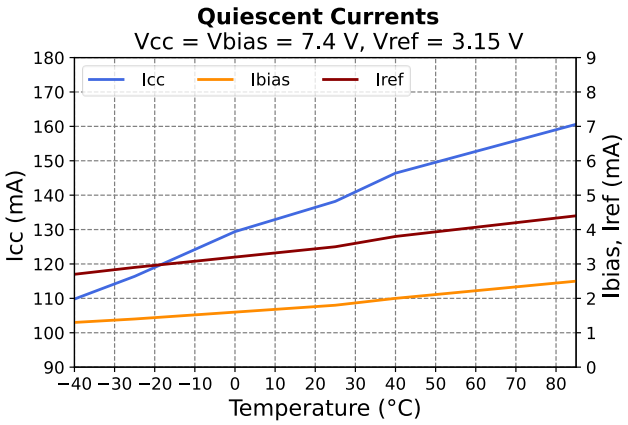


Figure 37 - Idle Currents vs. Temp

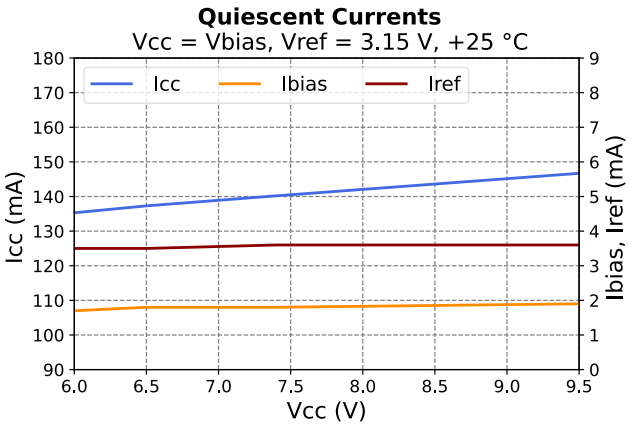


Figure 38 - Idle Currents vs. Vcc

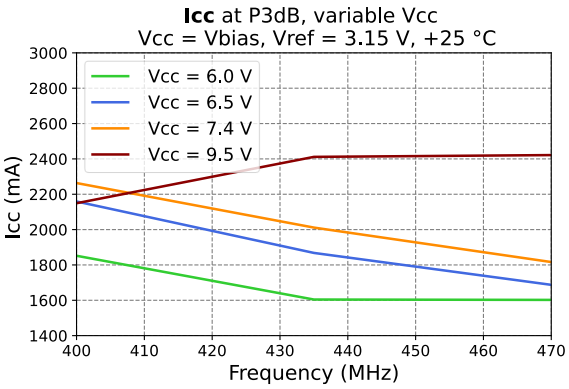


Figure 39 - Icc at P3dB

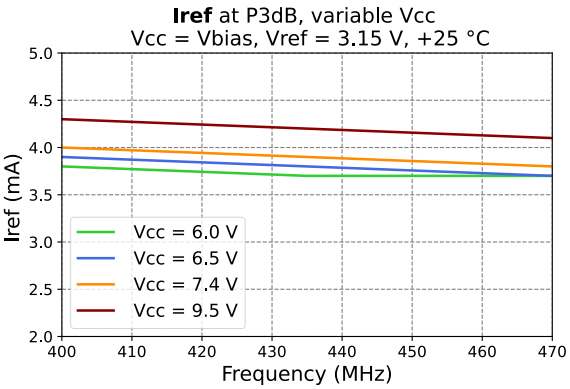


Figure 40 - Iref at P3dB

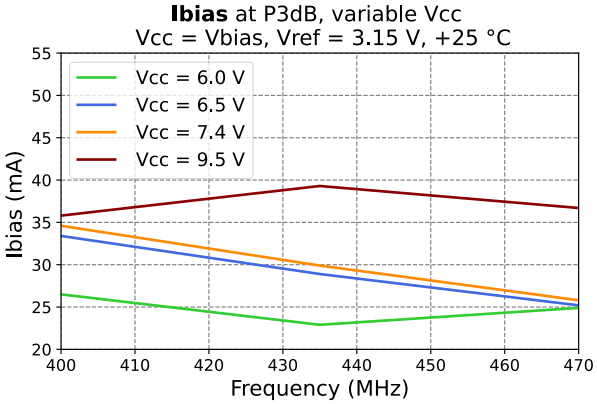


Figure 41 - Ibias at P3dB

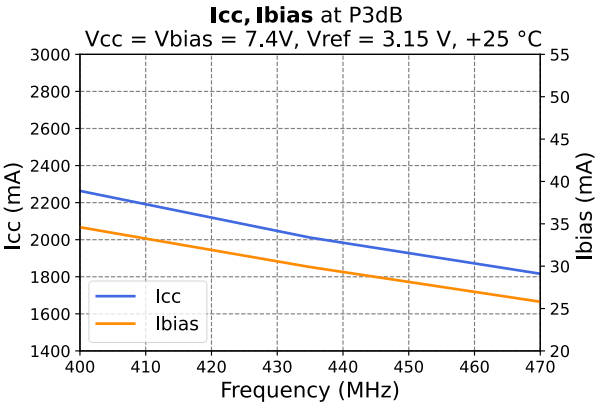


Figure 42 - Icc and Ibias at P3dB

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

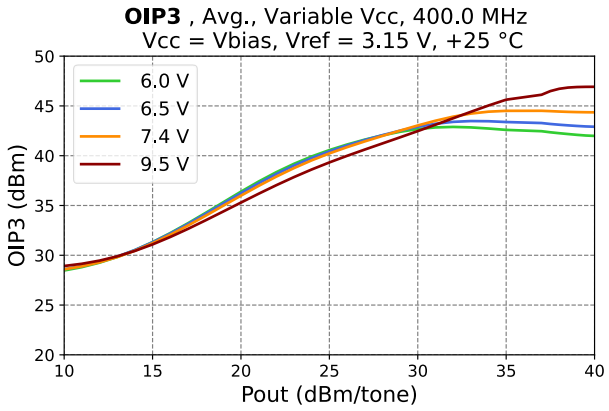


Figure 43 - OIP3 vs. Pout at 400 MHz

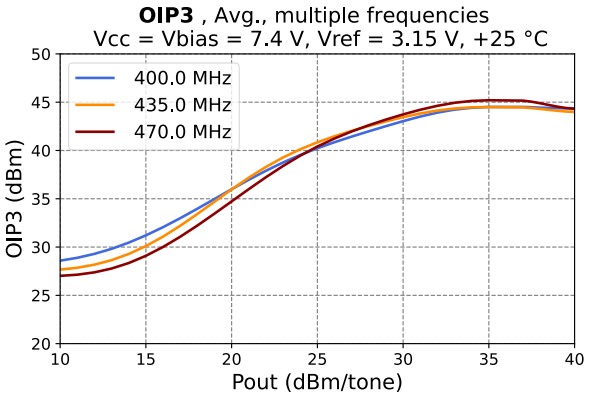


Figure 44 - OIP3 vs. Pout

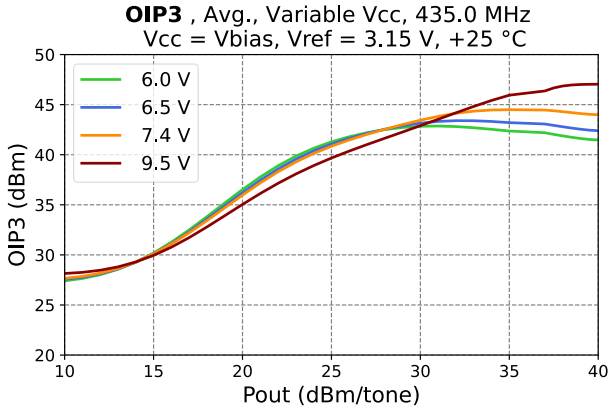


Figure 45 - OIP3 vs. Pout at 435 MHz

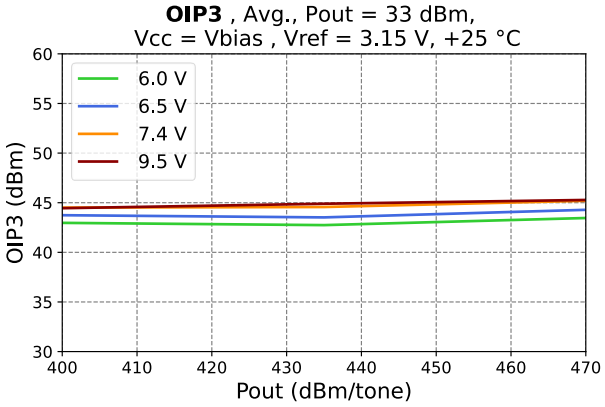


Figure 46 - OIP3 vs. Frequency at Pout = 33 dBm/tone

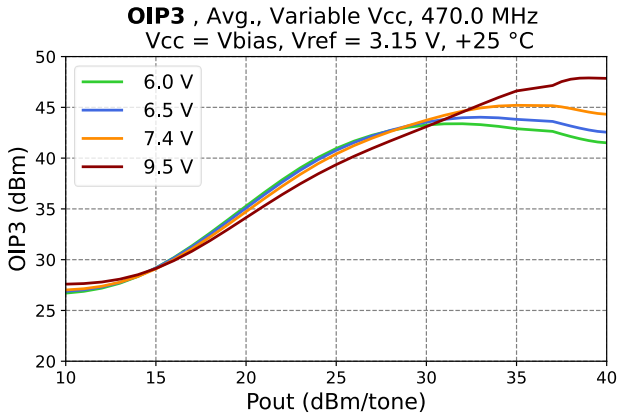


Figure 47 - OIP3 vs. Pout at 470 MHz

Test conditions unless otherwise noted:-
Vcc = Vbias = +7.4 V, Vref = +3.15 V, Ta = +25 °C, Zo = 50 Ω.

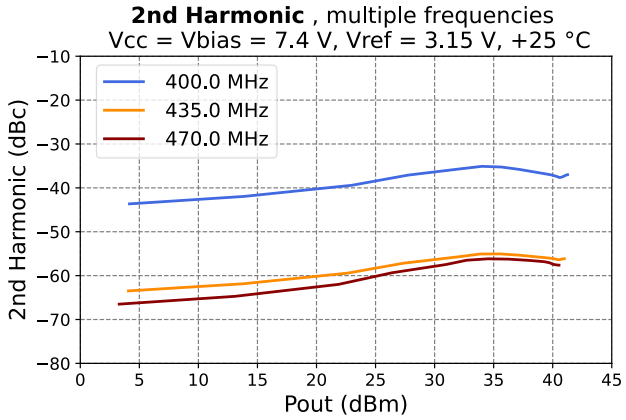


Figure 48 - Second Harmonic vs. Pout

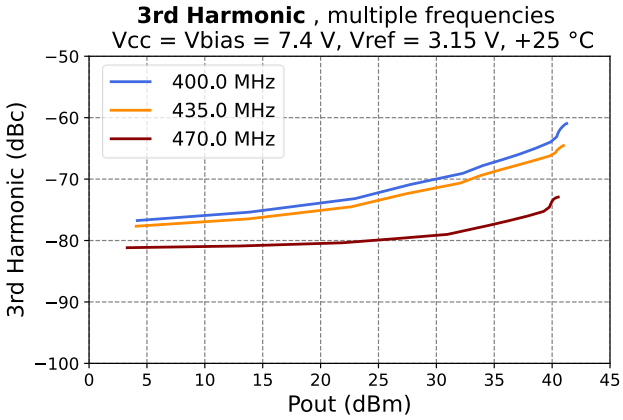


Figure 49 - Third Harmonic vs. Pout

Application Information

Evaluation Board Schematic

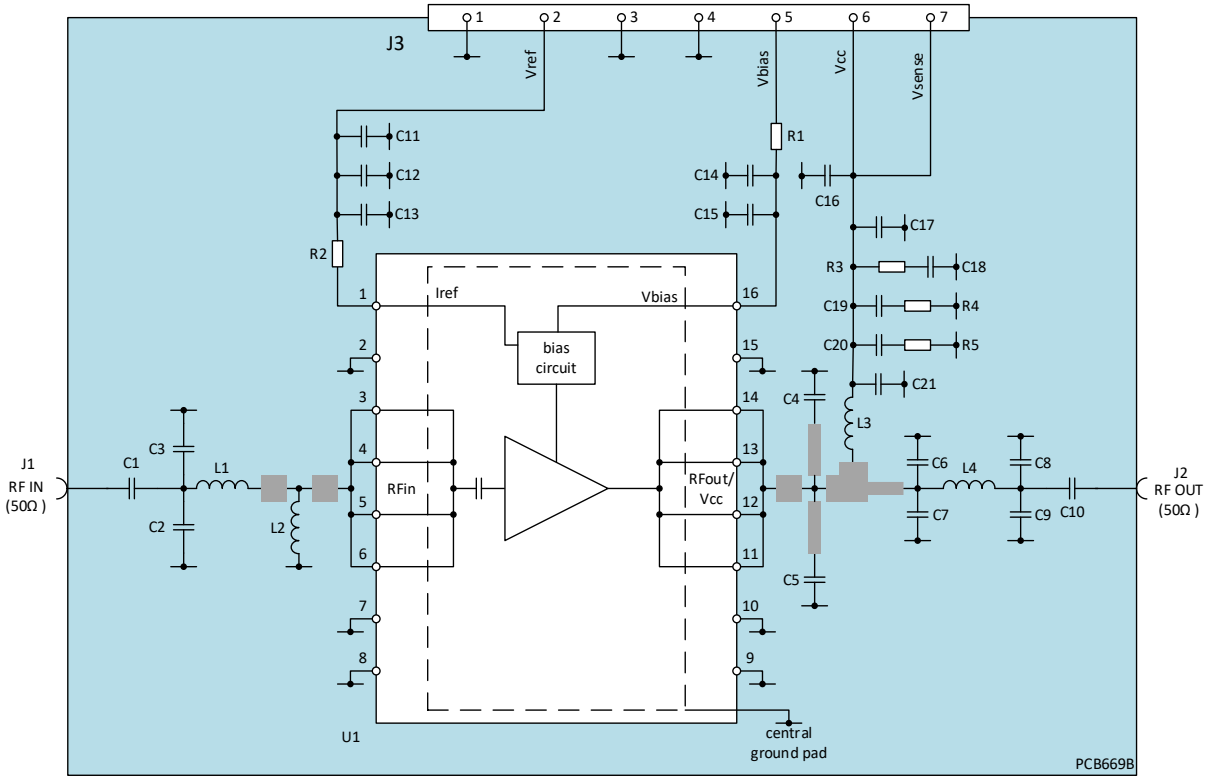


Figure 50 - EV90A009 Schematic

Bill Of Materials (BOM)

The following BOM is for the 400 to 470 MHz operating band, contact CML for BOM details for other operating bands.

Reference Designator	Value	Size	Description
C1, C7	22 pF	0603	ATC600S, NPO, 250 V, +/-1 %
C2	7.5 pF	0603	ATC600S, NPO, 250 V, +/-0.1 pF
C4, C5	20 pF	0603	ATC600S, NPO, 250 V, +/-1 %
C6, C10	24 pF	0603	ATC600S, NPO, 250 V, +/-1 %
C8	6.2 pF	0603	ATC600S, NPO, 250 V, +/-0.05 pF
C9	6.8 pF	0603	ATC600S, NPO, 250 V, +/-0.1 pF
C12, C18	0.1 uF	0805	X7R, 50 V, +/-10%
C13, C19	1 nF	0603	C0G, 50 V, +/-5%
C14	120 pF	0603	COG, 50 V, +/-1%
C15	30 pF	0603	COG, 50 V, +/-1%
C16	10 uF	2312	TANT (C), 25 V, +/-10%
C20	100 pF	0603	C0G, 50 V, +/-5%
C21	150 pF	0603	COG, 50 V, +/-1%
L1	9.1 nH	0603	Coilcraft: 0603DC-9N1, +/-2%
L2	5.1 nH	0603	Coilcraft: 0603DC-5N1, +/-2%
L3	27 nH	1111SQ	Coilcraft: 1111SQ-27N, +/-2%
L4	5.6 nH	0603	Coilcraft: 0603DC-5N6, +/-2%
R1	20 R	1206	0.75 W, +/-1%
R2	162 R	0603	0.1 W, +/-1%
R3, R4, R5	2.2 R	0402	0.1 W, +/-1%
C3, C11, C17	DNF		
U1	CMX90A009QK		
J3	7-way 0.1” pin header (TE 640456-7, mating 3-640440-7)		
J1, J2	Gigalane, PSF-S00-000		

Note:
DNF = Do Not Fit

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for stable RF and good thermal performance. The recommended layout, including the ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A009, PCB669B). See the following section for recommendations on best thermal and RF design.

The PCB consists of single layer FR-4 with a total thickness of 0.5 mm (Figure 51) and the EV90A009 PCB (Figure 52) is 41 mm x 41 mm. The microstrip RF input and output width is 1 mm.

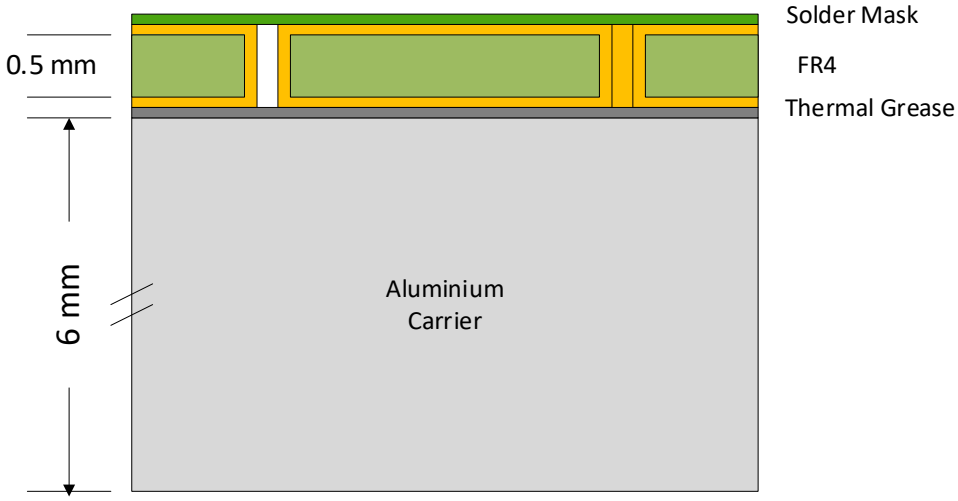


Figure 51 - EV90A009 PCB Layer Stack

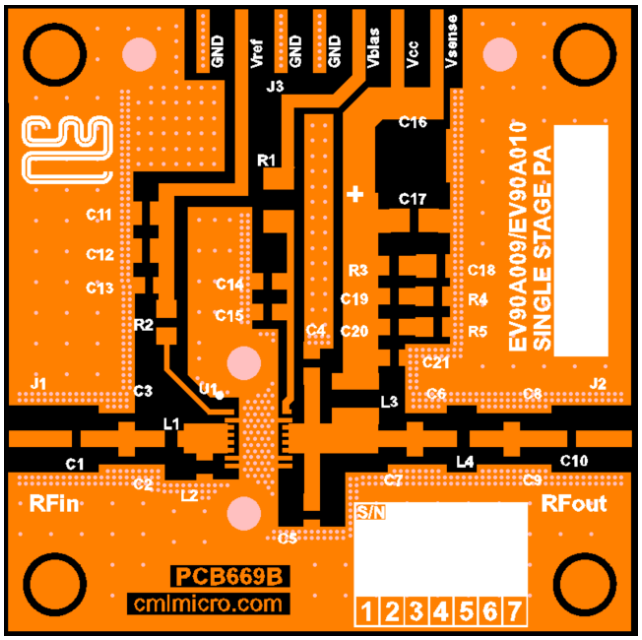


Figure 52 - EV90A009 PCB Top Layer View

Thermal and Stability Design

The primary RF/DC ground and thermal path is via the exposed die pad on the backside of the package, which must be connected to the PCB ground plane. A large array of plated through-hole ground vias directly underneath the CMX90A009 is essential to provide a low-inductance RF path and low-resistance thermal path to distribute heat away effectively. On the EV90A009, these 0.2mm, 25µm plated vias are resin filled, capped, over plated and planarised, for the above factors and to provide a flat PCB surface for good device placement.

A low inductance connection as described between the central ground pad and the board RF ground plane prevents unwanted gain peaking and instability due to internal ground path feedback.

The same via type is used for ground paths for the input and output matching networks and decoupling. Use of an alternative via style and pattern in either area may result in different performance from that published.

The bottom layer of the EV90A009 PCB is a solid ground plane, clear of solder resist to enable the board to be mounted to an appropriate carrier/heatsink to distribute heat and provide rigidity for the board.

The printed board is supplied mounted to an aluminium carrier using high performance thermal and electrically conductive grease. For effective evaluation, this carrier should be mounted on a heatsink using the four mounting holes (M3) positioned in the corners. It is recommended to use thermal grease to ensure good thermal contact between the carrier and the heatsink.

Device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin - Pout and Tc is the case temperature on the backside of the package (die pad) in contact with the PCB.

RFin Matching

The CMX90A009 RFin (pin 3, 4, 5 and 6) require external matching to 50 Ω. At 435 MHz, the target impedance to present to RFin is 7.33 + j10.41 Ω. The EV90A009 evaluation board uses three sections to achieve this. In the DC block section, C1 acts as a DC block to protect devices connected to J1 but also moves the impedance. The MS1 section (C2 shunt capacitor and L1 series inductor) transforms this impedance to an intermediate point on the real axis close to the geometric mean. Section MS2 (L2 shunt inductor) completes the impedance matching to present the target impedance to the CMX90A009 RFin. At these frequencies the interconnecting track and ground via paths need to be considered as part of any initial simulation. Some adjustment of values may be needed in a final layout.

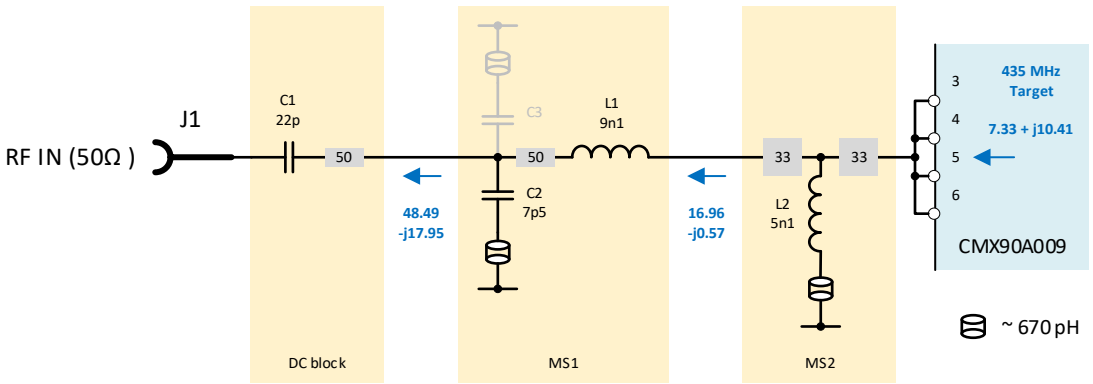


Figure 53 - Diagram of the EV90A009 Input Matching Network including inductance of vias and track impedances

RFout Matching

The Vcc & RFout pins (11, 12, 13 and 14) require matching to 50 ohms along with a suitable external inductor (L3) for the Vcc supply. This must be capable of carrying the DC current under all operating conditions and associated RF

decoupling on the supply side is required. At 435 MHz, 7.4V Vcc and operating at P3dB, the target impedance the matching circuit should present to the device to achieve the specified performance is approximately 2.41 -j0.21 Ω.

The matching network on EV90A009 consists of four sections that present this impedance to the device from 50 Ω. C10 acts as a DC block to protect devices connected to J2 but also moves the impedance. The MS1 section (C8/C9 shunt capacitors and L4 series inductor) transforms this impedance to an intermediate point on the real axis close to the geometric mean. Section MS2 (C6/C7 shunt capacitors and transmission lines) brings the impedance close to the target impedance for the CMX90A009 RFout. The Vcc feed inductor (L3) has a small effect on the matching. MS3 includes the 2nd harmonic shorts required for optimal efficiency and the transmission line to the four output pins. The two 2nd harmonic traps are capacitive at 435 MHz and, with the final transmission line, act as the final matching network to present the target impedance to the CMX90A009 RFout. At these frequencies and low impedances, the interconnecting track and ground via paths need to be carefully considered as part of any initial simulation. Some adjustment of values will likely be needed in a final layout to obtain optimal performance.

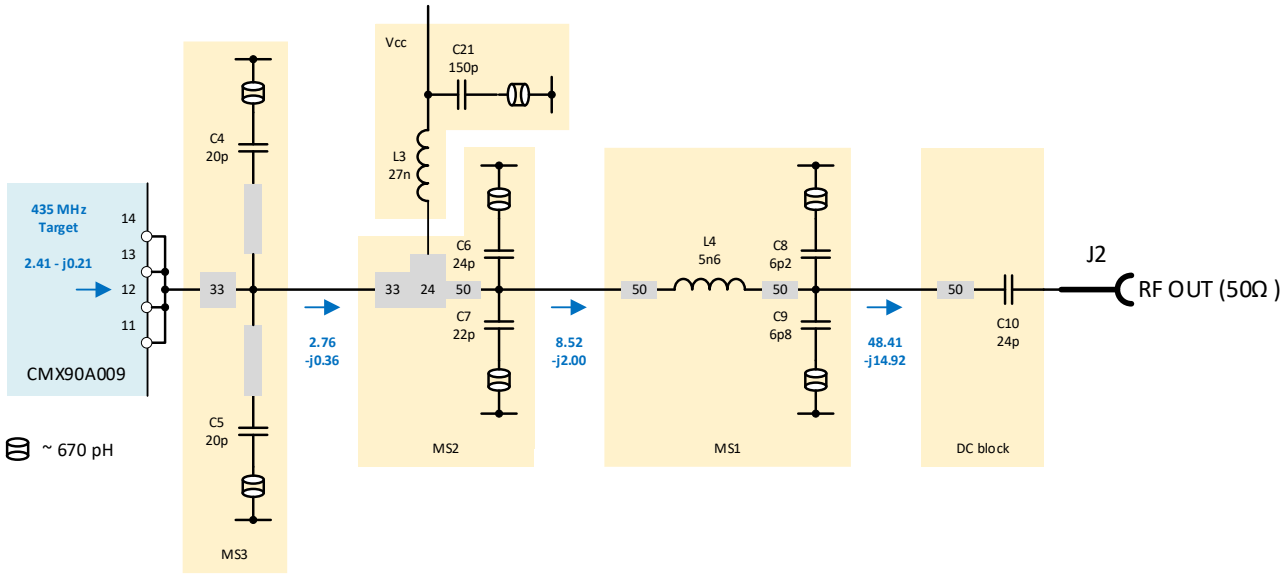


Figure 54 – Diagram of the EV90A009 Output Matching Network including inductance of vias and track impedances

Vbias Pin

The Vbias pin provides the supply to the internal bias circuit and the associated base current to the amplifier stage. To consolidate power supplies the Vbias pin can be connected to Vcc without affecting the performance of the device. This pin is protected by ESD diodes.

Iref Pin

The quiescent bias current is proportional to the current into the Iref pin. This current is set by a series resistor from the Vref regulated supply. The resistor is 162 Ω (R2, Figure 50) on the EV90A009, resulting in the following current with Vref = 3.15 V:

Iref = (Vref – (2 x Vbe)) / (R2 + Rint)

Current into Iref = (3.15 – (2 x 1.25)) / (162 + 18.5) = 3.6 mA, resulting in a typical Icq of 134 mA.

Icq (approx.) = (Iref x 134 / 3.6) – ((Iref – 3.6) * 12)

These bias points have been selected for optimum PA performance. It is possible to achieve these same currents from a higher or lower Vref supply by appropriate selection of the series resistor. To ensure correct bias circuit operation the current into Iref should not exceed 12 mA. This pin is protected by ESD diodes.

Ramping

Vref can also be used to ramp the CMX90A009 gain up or down to support burst signals and TDD systems. By varying Vref between 2 V and 3.15 V (typ.) the gain can be adjusted by 40 dB (Figure 55).

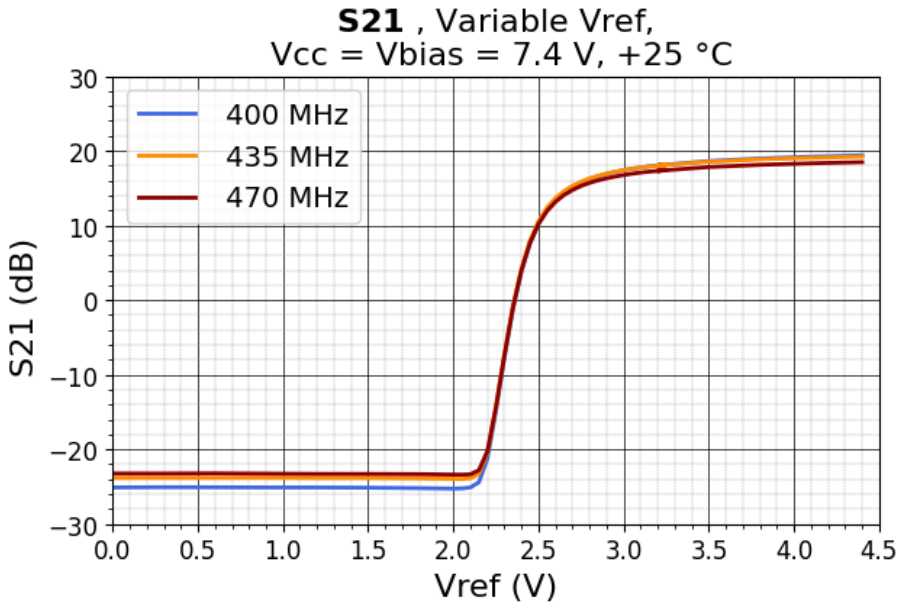


Figure 55 - Vref Gain Control

Evaluation Board and Bias Procedure

Ensure an adequately rated attenuator is placed between the output of the amplifier (RFout) and 50 Ω RF test equipment. The amplifier RFin should be connected to a signal source with the ability to turn off the drive to the CMX90A009. A dual power supply will be needed, with output of +7.4 V @ 3 A for the collector voltage (Vcc) and bias circuit (Vbias) and +3.15 V for the reference voltage (Vref). Use good quality cables for both supply and ground to minimise the voltage drop between the PSU and evaluation board. This may be significant at high output powers. A Vsense pin (7) is provided on the board to optionally enable feedback to a suitably equipped power supply to compensate for the cable voltage drop at high current. This is connected in parallel with Vcc and may alternatively be used as a second Vcc connection. Connect the power supply with the RF input drive off and ensure that the evaluation board consumes the correct quiescent current (Icq). Although it is good practice to enable the Vcc & Vbias supply before the Vref supply, in general, power supply sequencing is not necessary. If the quiescent current is correct, enable the RF signal with a low RF level, for example RFin = -30 dBm, to begin with to ensure the device is not overdriven. Ensure the test signal is within the recommended frequency range of the device and that the output signal measured on the test equipment complies with the expected small signal gain, before continuing with any further tests.

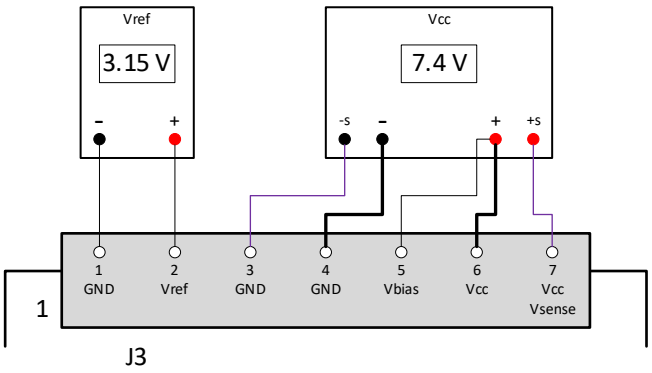


Figure 56 – EV90A009 Standard Power Supply Connections: common Vcc & Vbias PSU

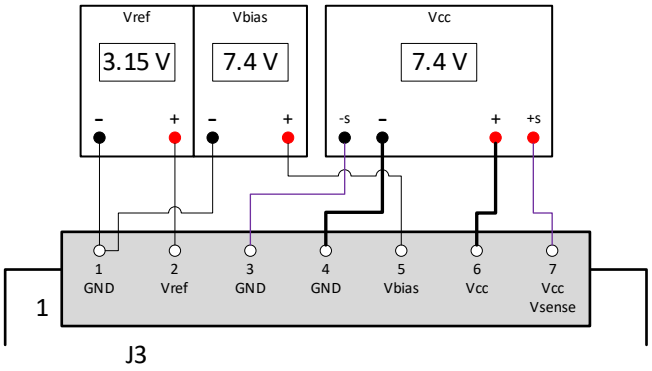


Figure 57 - Alternative EV90A009 Power Supply Connections: separate Vcc & Vbias PSUs

The user should be aware that noise from power supplies may modulate the amplified RF signal and introduce spurious products in the output spectrum. Ensure that the power supplies used are 'RF quiet'.

Ruggedness

To prevent possible damage to the device, care should be taken to ensure that the VSWR of the load that the CMX90A009 is working into does not exceed the limits in the Electrical Specification.

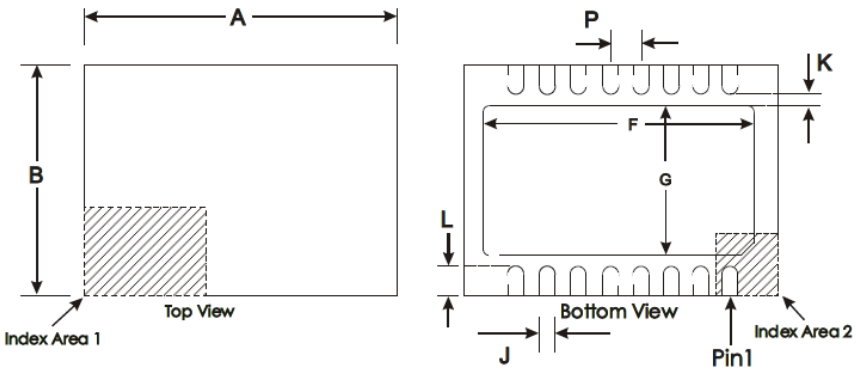
A typical transmit system will have couplers, filtering, transmit/receive switching and antenna matching between the PA and the antenna. These all need to be designed carefully to ensure a good 50 Ω match is presented to the PA that is above the minimum return loss limits over the whole operating frequency range.

External effects on the antenna impedance should also be considered. Proximity to other objects and surfaces can change the antenna impedance significantly, resulting in the return loss presented to the PA falling below the limit and therefore subsequent damage to the PA.

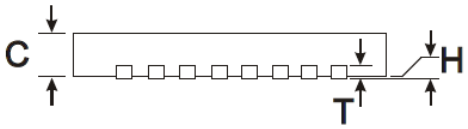
If there is an external antenna connector on the equipment, it should be assumed that the wrong antenna might get connected or that the transmitter may be operated with no antenna connected.

Package Outline

16-lead 4x5mm VDFN Package (QK)



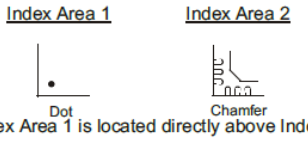
DIM.	MIN.	TYP.	MAX.
* A		5.00 BSC	
* B		4.00 BSC	
C	0.80	0.90	1.00
F	4.20	4.35	4.45
G	2.30	2.45	2.55
H	0.00	0.02	0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
P		0.50	
T		0.20	



NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees



Index Area 1 is located directly above Index Area 2

The underside of the package has an exposed metal pad which should be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.

Line 1: CMX90 SμRF series

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1.1	Added load output VSWR ruggedness and stability data Added ESD levels Minor editorial updates	26 September 2025
1.0	First approved release	21 March 2025

Contact Information

For further information please contact your local CML sales representative.

Contact details can be found at http:///www.cmlmicro.com