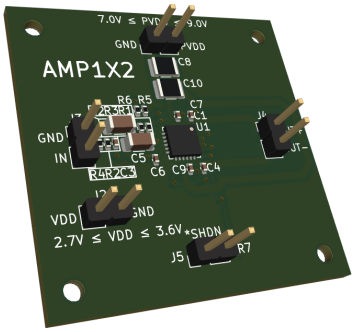


Data Sheet AMP1X2 Audio Amplifier Board

PUI Audio's AMP1X2 audio amplifier board features an Analog Device's MAX9768 Class D mono amplifier circuit for maximum signal fidelity. This amplifier delivers a minimum of 2.0W into 8Ω loads and 4.0W into 4Ω loads, both at <1% THD+N while using a 7V DC supply.

The board features a small size of 38.0mm x 38.0mm and header pins for easy design prototype development.

Features:

- 2.0W into 8Ω loads
- 4.0W into 4Ω loads
- Enhances System Performance that includes
  - Transient suppression when the supply voltage is applied
  - High 77dB PSRR (f_{IN} = 1kHz, V_{RIPPLE} = 200mV_{P-P})
- Low quiescent current
- Thermal overload protection
- Short-circuit protection
- Amplifier power supply range: 7.0V ≤ PV_{DD} ≤ 9.0V
- Subsystem power supply voltage range: 2.7V ≤ PV_{DD} ≤ 3.6V
- Logic power supply range:
- 7mA subsystem power supply current (V_{DD} = 3.3V)
- 4mA amplifier power supply current (PV_{DD} = 7.0V)
- P_{OUT} = 2.0W into 8Ω (THD < 1%, V_{DD} = 7.0V)
- P_{OUT} = 4.0W into 4Ω (THD < 1%, V_{DD} = 7.0V)
- External resistors adjust the amplifier gain
- 1.8V Logic-Compatible SHDN Input
- 100mil spaced header pins for input, output, shutdown, power supply, and ground connections

Absolute Maximum Rating

PV_{DD} with respect to GND ..... $-0.3V \le PV_{DD} \le 16V$
VDD with respect to GND ..... $-0.3V \le V_{DD} \le 4V$
SCLK, SDA/VOL, $\overline{SHDN}$ with respect to GND ..... $-0.3V \le V_{DD} \le 4V$
FB, SYNCOUT ..... $-0.3V \le (V_{DD} + 0.3V)$
BOOT+ with respect to OUT+, BOOT- with respect to OUT- ..... $-0.3V \le V_{DD} \le 4V$
OUT+ with respect to GND, OUT- with respect to GND ..... $-0.3V \le (V_{DD} + 0.3V)$
Continuous Current
- PV_{DD}, PGND, OUT-, OUT+ 2.2A
- Any other pin ..... ±20mA

OUT- and OUT+ Short-Circuit Duration ..... Continuous
Operating Temperature Range ..... $-40°C \le T_A \le 85°C$
Storage Temperature Range ..... $-65°C \le T_A \le 150°C$

Electrical Characteristics

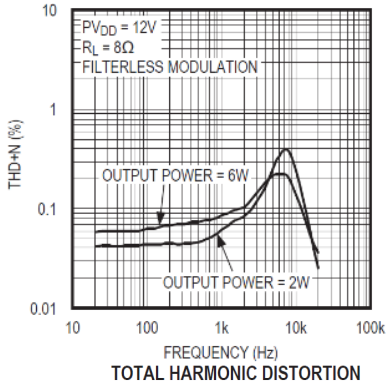
(PV_{DD} = 7.0V V_{DD} = 3.3V, V_{GND} = V_{PGND} = 0V, $\overline{SHDN}$ = V_{DD}, V_{MUTE} = GND, GAIN = V_{DD} (0dB), C_{BIAS} = C_{IN} = 2.2µF, C1 = C4 = 0.1µF, no load, R_{IN} = 20kΩ, R_F = 30kΩ, SSM mode, filterless modulation, T_A = $t_{MIN} \le t \le t_{MAX}$. Typical values are given at T_A = 25°C, unless otherwise noted.)

Parameter	Conditions		Minimum	Typical	Maximum	Unit
Amplifier Power Supply Voltage Range	Guaranteed by the PSRR test		7.0		12.0	V
Subsystem Power Supply Voltage			2.7		3.6	V
Output Power	PV_{DD} = 7V, 1% THD+N	R_L = 8Ω + 68µH		2.0		W
		R_L = 4Ω + 33µH		4.0		
Total Harmonic Distortion + Noise	f_{IN} = 1kHz, R_L = 8Ω, P_{OUT} = 2W BW = 22Hz ≤ f ≤ 22kHz	Filterless modulation		0.09		%
Signal-to-Noise Ratio	A-weighted, V_{DD} = 7V, P_{OUT} = 2W, R_L = 8Ω + 33mH, Input-referred			97		dB
Over-Current Protection Threshold				2		A
Thermal Protection Threshold				150		°C
Thermal Protection Hysteresis				15		°C
Under-Voltage Lockout	V_{DD}			2.5		V
	PV_{DD}			4.0		
Quiescent Power Supply Current	I_{VDD}			7		mA
	I_{PVDD}			4		
Shutdown Active Power Supply Current	$\overline{SHDN}$ = 0V, I_{SHDN} = I_{PVDD} + I_{DD}			0.5		µA
Turn-On Time				220		ms
Output Offset Voltage	Inputs AC-coupled to GND			±2		mV
Output Turn-On Transient Magnitude	R_L = 8Ω, 32 samples per second, A-weighted	Into Shutdown		-52.6		dBV
		Into Mute		-67		
		Out of Shutdown		-48		
		Out of Mute		47		
Power-Supply Rejection Ratio	V_{DD} = 2.7V ≤ V_{DC} ≤ 3.6V			68		dB
	PV_{DD} = 7V ≤ V_{DC} ≤ 9.0V			84		
	f = 1kHz	V_{RIPPLE} = 200mV_{P-P} on PV_{DD}		77		
		V_{RIPPLE} = 100mV_{P-P} on V_{DD}		60		

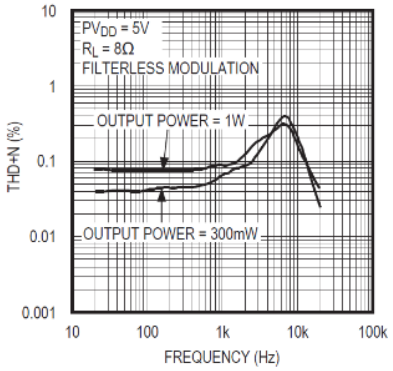
Typical Performance Characteristics

(V_{DD} = 3.7V, V_{GND} = 0V, $\overline{SHDN}$ = V_{DD}, GAIN = GND (R_F = R_{IN} = 10kΩ), C_{BIAS} = 0.1µF, C_{IN} = 1µF, no load, unless otherwise noted.)

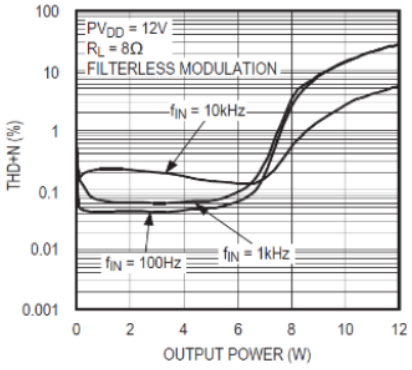
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



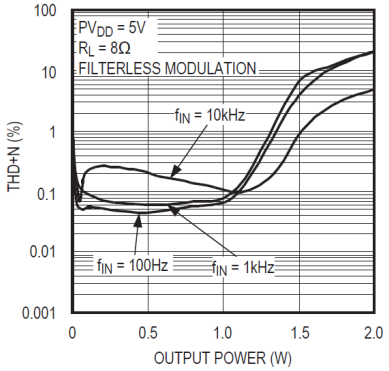
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



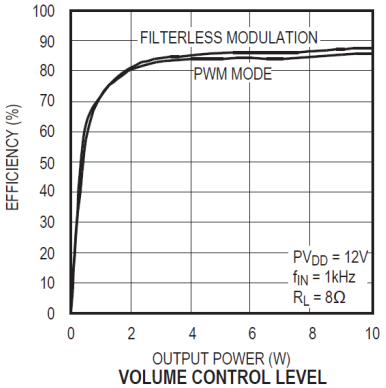
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



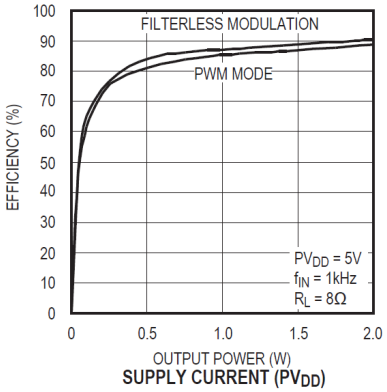
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



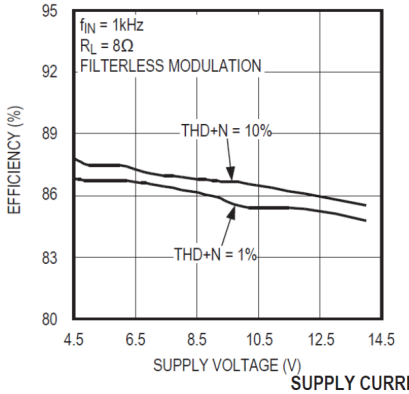
EFFICIENCY vs. OUTPUT POWER



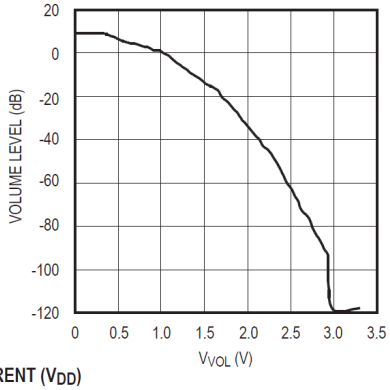
EFFICIENCY vs. OUTPUT POWER



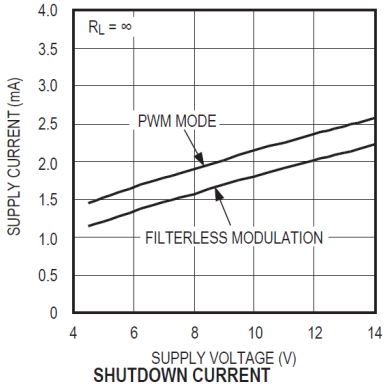
EFFICIENCY vs. SUPPLY VOLTAGE



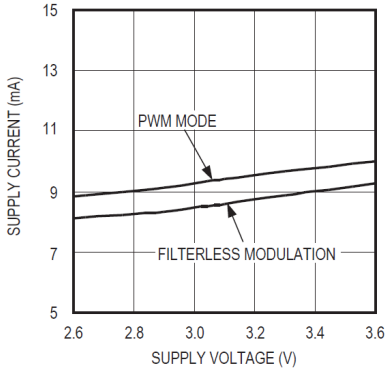
VOLUME CONTROL LEVEL vs. VOLUME CONTROL VOLTAGE



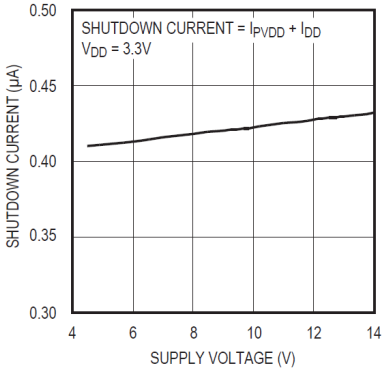
SUPPLY CURRENT (PV_{DD}) vs. SUPPLY VOLTAGE



SUPPLY CURRENT (V_{DD}) vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



Detailed Description

The AMP1X2 audio amplifier board uses the MAX9768 mono Class D audio amplifier. This amplifier offers low IPV_{DD} = 1.8mA (typical, PV_{DD} = $7V_{DC}$) and IV_{DD} = 8.8mA (typical, V_{DD} = $3.3V_{DC}$) quiescent power supply current, an excellent 94dB (typical) SNR, and high linearity exemplified by its 0.08% THD+N. The amplifier features circuitry that produces high suppression of output transients when the power supply voltage is applied. Additionally, the amplifier's power supply rejection ratio (PSRR) is an outstanding 68dB (V_{DD}) and 84dB (PV_{DD}).

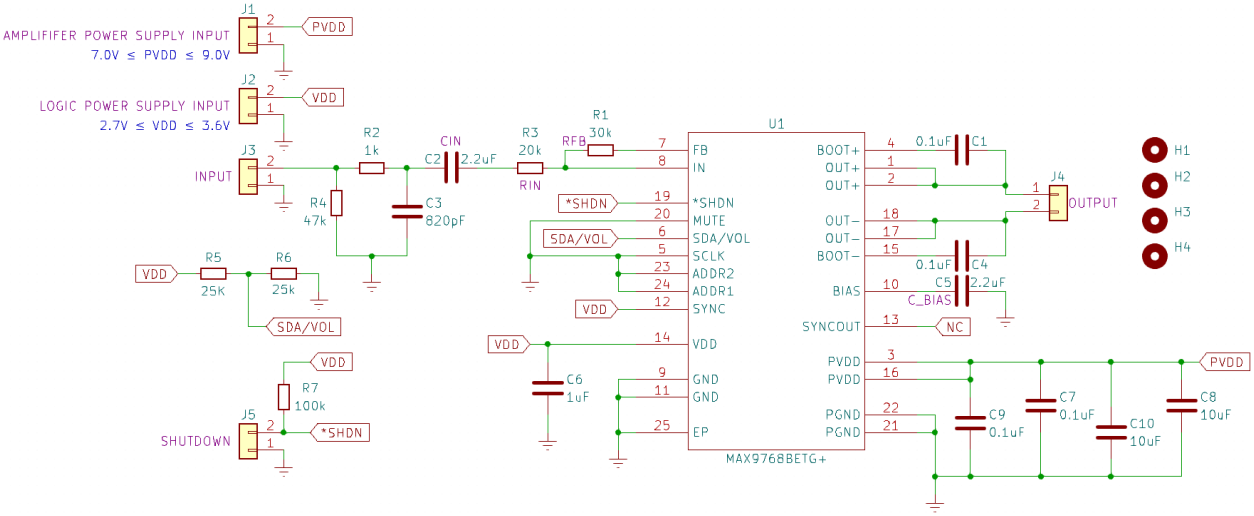


Figure 1. AMP1X2 schematic.

Bias

The AMP1X2's amplifier operates with a single 7.0V to 12.0V power supply voltage. It uses internal circuitry to generate the $V_{DD}/2$, ground-referenced common-mode bias voltage. The BIAS circuitry's output is available on the BIAS pin so that an external capacitor can be connected between this pin and GND, allowing for the connection of a decoupling capacitor. The value of this capacitor is chosen based on the recommendations detailed in the BIAS Capacitor section below.

Soft Current Limit

When the output current exceeds the typical 2A soft current limit, the MAX9768 enters a cycle-by-cycle current-limit mode. In soft current-limit mode, the output is clipped at 2A. When the output decreases so the output current falls below 2A, normal operation resumes. The effect of soft current limiting is a slight increase in distortion. Most applications will not enter soft current-limit mode unless the speaker or filter creates impedance nulls below 8Ω.

Hard Current Limit

When the output current exceeds the typical 2.5A hard current limit, the MAX9768 disables the outputs and initiates a startup sequence. This startup sequence takes 220ms for the MAX9768. The shutdown and startup sequence is

repeated until the output fault is removed. During hard current limit, the output may produce a small amplitude transient voltage change at the amplifier output, that may be heard on speakers driven by the amplifier as a soft click. The average supply current is relatively low, as the duty cycle of the output short is brief. Most applications will not enter hard current-limit mode unless the output is short circuited or incorrectly connected.

BTL Amplifier Output

The AMP1X2's amplifier is designed to differentially drive loads connected between the OUT+ and OUT- pins. This is a bridge-tied-load (BTL). This configuration has advantages over a single-ended, ground referenced load. Differential output drive doubles the output voltage across the load when compared by the drive voltage across a single-ended load.

Doubling the voltage applied across a load quadruples the power dissipated by the load. The peak-to-peak voltage swing across a single-ended load is expressed by Eq. 1. The peak-to-peak voltage swing across a BTL-connected load is expressed by Eq. 2. The power dissipated by a single-ended-connected load is expressed by Eq. 3. The power dissipated by a BTL-connected load is expressed by Eq. 4.

$$V_{RMS\_SE} = \frac{V_{OUTp-p}}{2\sqrt{2}} \quad \text{Eq. 1}$$

$$V_{RMS\_BTL} = \frac{2V_{OUTp-p}}{2\sqrt{2}} \quad \text{Eq. 2}$$

$$P_{OUT\_SE} = \frac{{V_{RMS\_SE}}^2}{R_L} \quad \text{Eq. 3}$$

$$P_{OUT\_BTL} = \frac{2{V_{RMS\_SE}}^2}{R_L} = \frac{V_{RMS\_BTL}}{R_L} \quad \text{Eq. 4}$$

For a 5Vp-p output voltage swing, the dissipation in an 8Ω load is 0.391W.

When the load is applied across two identical amplifiers whose outputs are 180degress out-of-phase, the output voltage swing is 10Vp-p. This results in a dissipation across the same 8 Ω load that is 1.56W, or four times that dissipated by a single-ended load.

Even though each amplifier is biased to one-half of the power supply voltage, since the voltage with respect to ground is the same on each output, there is no net differential DC voltage applied across the load. There is, therefore, no need to use any DC-blocking capacitors in series between the amplifier's outputs and the load. This is unlike a single-ended amplifier, which must have a DC-blocking capacitor when the single-ended output and the ground terminated load. DC-blocking capacitors used with single-ended amplifiers and very low resistances will typically have high values, large size, and can degrade low-frequency response and performance.

Adjustable Gain

The AMP1X2's amplifier uses external resistors to set the desired closed loop gain. The output stage has an internal 20dB gain in addition to the externally set gain. The MAX9768's gain is set using Eq. 5.

$$A_V = -10\frac{R_F}{R_{IN}} \quad \text{Eq. 5}$$

Referring to Figure 1 with R_{IN} = 20kΩ and R_F = 30kΩ, the gain is -15V/V or 23.5dB.

R_F is best chosen in the range of 10kΩ and 50kΩ. The final gain is a function of the volume setting. In the AMP1X2's case with a fixed voltage applied to the SDA/VOL input, the maximum gain is 7.1dB. If adjustable gain or adjustable volume is desired, the fixed value resistors R5 and R6 can be replaced by a potentiometer.

Input Filter

The AMP1X2 uses AC-coupling capacitor, C_{IN}, in series with amplifier's single-ended input. This capacitor allows the MAX9768's input to bias to the optimum DC level. Assuming a zero-source impedance, the combination of the input resistor, R_{IN}, and coupling capacitor C_{IN}, forms a high-pass filter that has a cutoff frequency as defined by Eq. 4.

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{Eq. 4}$$

Setting the f_{-3dB} frequency is set too high can compromise the low frequency performance. This frequency is dependent on the frequency bandwidth design targets for the system in which the AMP1X2 is used.

Capacitor chemistry recommendations include selecting devices with low voltage coefficients such as film capacitors or NPO or X7R ceramic devices. It is best to use high voltage ratings beyond 20V.

BIAS Capacitor

The BIAS pin is internally connected to the circuitry that generates the $V_{DD}/2$ bias voltage. This connection allows connecting a capacitor between the internal bias voltage generator and ground. This capacitor reduces power supply and other source noise present at the common-mode node, maximizing the PSRR and THD+N performance. This capacitor is also used by the bias generator circuitry to produce a controlled slew rate bias voltage waveform that ensures transient suppression at the amplifier outputs. This recommended capacitor's value is 2.2µF to maximize PSRR. To ensure proper amplifier operations, do not connect any load to the BIAS pin. Doing so will compromise the amplifier's overall operation.

Power Supply Bypassing

The AMP1X2 uses proper supply capacitive bypassing to ensure low-noise, low-distortion audio performance. The suggested bypass device is a 1µF ceramic capacitor connected between the V_{DD} pin and GND. The AMP1X2 uses an additional 10µF bulk capacitance in parallel with a 0.1µF capacitor connected between PV_{DD} and GND. The bypass capacitor is best placed as close as possible to the respective V_{DD} and PV_{DD} pins.

Shutdown Mode

The AMP1X2 features a low-power shutdown mode that, when activated, reduces the board's power supply current to a nominal 100μA. When shutdown mode is active (a logic-low is applied to the $\overline{SHDN}$ pin by shorting JP6), the amplifier's internal bias circuitry is disabled, the amplifier's outputs change to a high impedance state, the SYNCOUT is set to a logic high, and the BIAS pin output and the common-mode input voltages decay to GND.

Suppressing Amplifier Output Transients

The AMP1X2's MAX9768 features a leading-edge transient suppression circuit that ensures that output transients' magnitude the occur when the power supply voltage is applied to the amplifier are minimized. This is a result of controlling the slew rate of the bias circuitry's output voltage's magnitude changes to $V_{DD}/2$. Conversely, when shutdown is activated, the impedance of amplifier's outputs is set to a high impedance. Both functions work together to ensure that transient energy in the audio bandwidth is suppressed and minimized.

Undervoltage Lockout (UVLO)

The AMP1X2 features undervoltage lockout protection that shuts down the amplifier if either of the supplies (V_{DD} and PV_{DD}) fall below at preset threshold. The amplifier will shut down if V_{DD} is less than 2.5V (V_{DD} UVLO = 2.5V) or if PV_{DD} is less than 4V (PV_{DD} UVLO = 4V).

Thermal Shutdown

When the amplifier's die temperature exceeds the nominal 150°C thermal shutdown threshold, the AMP1X2 outputs are disabled. When the die temperature falls below a nominal 135°C, normal operation resumes. The thermal shutdown turns off the output signal for approximately 3s. Most applications should not activate thermal shutdown. Some of the possible causes of thermal shutdown are a load impedance that is too low, high ambient temperature, poor PCB layout and assembly, or excessive output overdrive.

AMP1X2 Controls, Input, Outputs, and Settings

The AMP1X2 features the following controls, input, output, and settings.

Jumper J1 is the AMP1X2's amplifier power supply voltage (PV_{DD}) input. Apply a DC voltage in the range of $7V_{DC}$ to $9V_{DC}$ to achieve a clean, undistorted 2W output for an 8Ω load or a 4W output for a 4Ω load. Apply the positive voltage to the V_{DD} pin (pin 2) and apply ground to the GND pin (pin 1).

Jumper J2 is the AMP1X2's logic subsystem power supply voltage input. Apply a DC voltage in the range of $2.7V_{DC}$ to $3.6V_{DC}$. Apply the positive voltage to the V_{DD} pin (pin 2) and apply ground to the GND pin (pin 1).

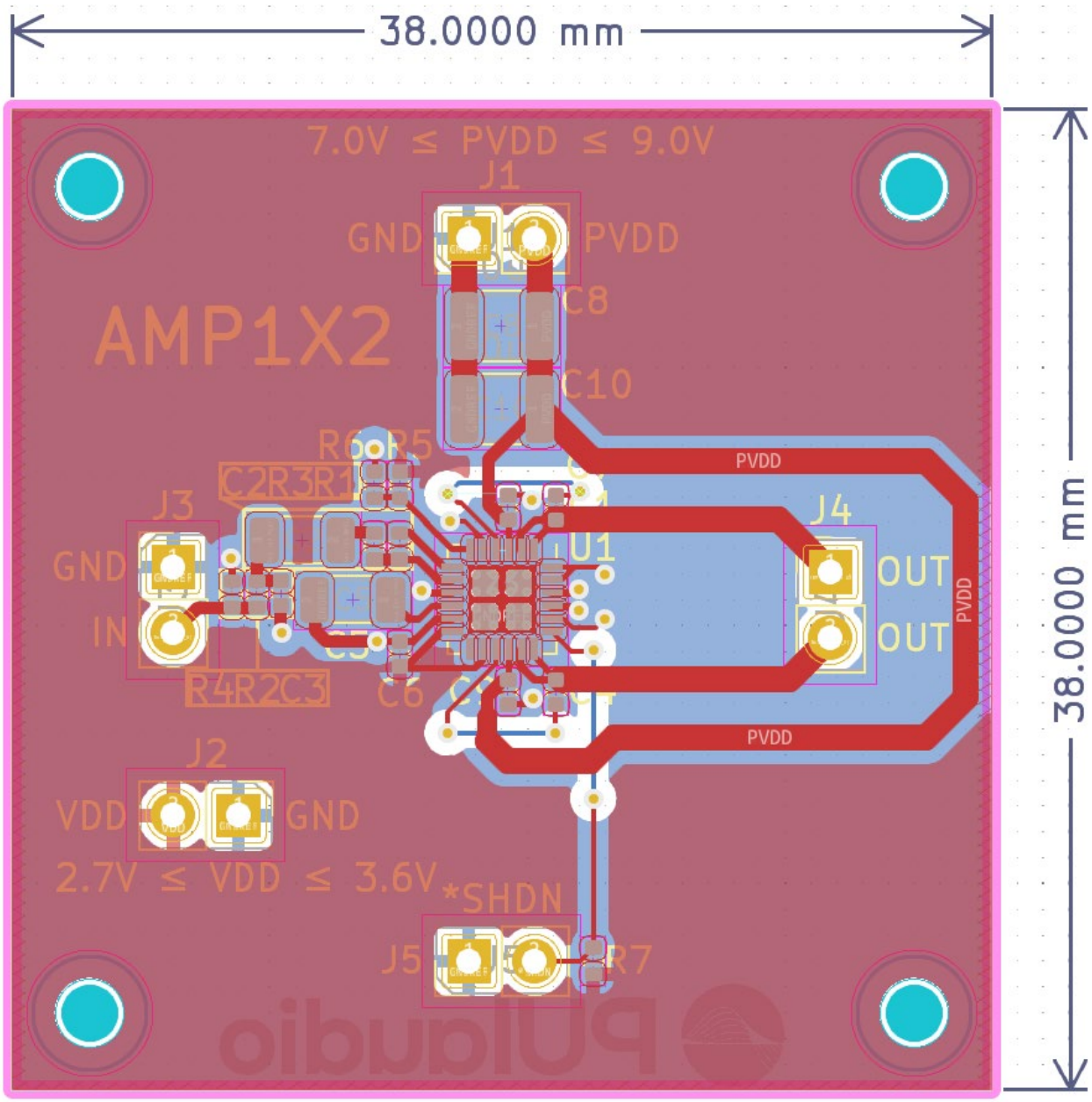
Jumper J3 provides the connection node for the single-ended audio signal input. The audio signal is applied to V_{IN} pin (pin 2) and the input signal's ground reference is applied to GND (pin 1).

The input signal's voltage magnitude is predicated on the power supply voltage and the closed-loop gain set by resistors R1/R3. As configured, the AMP1X2 has a 15x (23.5dB) closed-loop gain. For example, when using a 7V power supply voltage, the output voltage is nominally $4.47V_{RMS}$ when driving an 8Ω loads and $3.16V_{RMS}$ when driving 4Ω loads. With the AMP1X2's 23.5dB (15x) nominal gain, the RMS input voltage levels are, respectively, $0.298V_{RMS}$ and $0.211V_{RMS}$. At these levels, the THD will typically not exceed 1%.

Jumper J4 is the MAX9768's BTL amplifier output. Connect a load across the jumper's pin 1 and pin 2. Pin 1 is the non-inverting output, whereas pin 2 is the inverting output.

Jumper J5 controls the amplifier's shutdown function. The default setting is the jumper is open, pulling the active-low $\overline{\text{SHDN}}$ input to a logic high, allowing full operation. When shutdown is desired, place a short between pin 1 and pin 2. When shutdown is active, the amplifier output's change to a high-impedance state, and the power supply current drops to a nominal 2μA.

Dimensions



Packaging

One box that features one single-channel, 2W amplifier board and through-hole headers contained within an ESD-protective bag.

Specifications Revisions

Revision	Description	Date	Approved
A	Preliminary datasheet released from Engineering	05/22/2025	KH

Note:

1. Unless otherwise specified:
   A. All dimensions are in millimeters.
   B. Default tolerances are ±0.5mm and angles are ±3°, unless otherwise specified.
2. Specifications subject to change or withdrawal without notice.