DATA SHEET

Si827x 4 Amp ISOdriver with High Transient (dV/dt) Immunity

The Si827x isolators are ideal for driving power switches used in a wide variety of power supply, inverter, and motor control applications. The Si827x isolated gate drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 2.5 kV_{RMS} withstand voltage per UL1577. This technology enables industry leading common-mode transient immunity (CMTI), tight timing specifications, reduced variation with temperature and age, better part-to-part matching, and extremely high reliability. It also offers unique features, such as separate pull-up/pull-down outputs, driver shutdown on UVLO fault, and precise dead-time programmability. The Si827x series offers longer service life and dramatically higher reliability compared to optocoupled gate drivers.

The Si827x drivers utilize Skyworks' proprietary silicon isolation technology, which provides up to 2.5 kV_{RMS} withstand voltage per UL1577 and fast 60 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8271/2/3/5) or PWM input (Si8274) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si827x family ideal for a wide range of isolated MOSFET/IGBT and SiC or GaN FET gate drive applications.

Automotive Grade products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- Switch-mode Power Supplies
- Solar Power Inverters
- Motor controls and drives
- Uninterruptible Power Supplies
- High-Power Class D Amplifiers

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid Electric Vehicles
- Battery Electric Vehicles

Safety Regulatory Approvals

- UL recognized
  - 1577 (2500 V_{RMS} for one minute)
- CSA certification conformity
  - 62368-1 (basic insulation)
- VDE certification conformity
  - 60747-17 (basic insulation)
- CQC certification approval
  - GB4943.1 (basic insulation)

Key Features

- Single, dual, or high-side/low-side drivers
- Single PWM or dual digital inputs
- High dV/dt immunity:
  - 200 kV/µs CMTI
  - 400 kV/µs Latch-up
- Separate pull-up/pull-down outputs for slew rate control
- Wide supply range:
  - Input supply: 2.5 to 5.5 V
  - Driver supply: 4.2 to 30 V
- Very low jitter of 200 ps p-p
- 60 ns propagation delay (max)
- Dedicated enable pin
- Skyworks' high-performance isolation technology:
  - Industry leading noise immunity
  - High-speed, low latency and skew
  - Best reliability available
- Compact packages:
  - 8-pin SOIC
  - 16-pin SOIC
  - LGA-13 packages
- Wide temperature range:
  - –40 to 125 °C
  - –55 to 125 °C (OPNs with "-ZS" suffix, refer to 8. "Ordering Guide")
- AEC-Q100 Qualified (all other OPNs)
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

1. Pin Descriptions

1.1. Si8271 Pin Descriptions

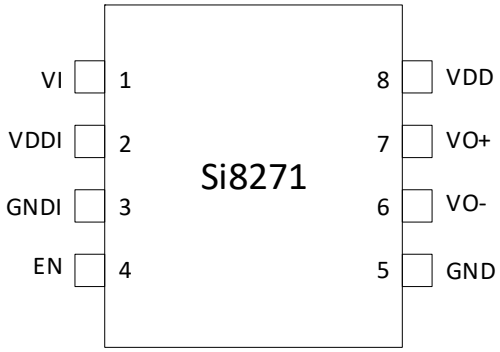


Figure 1. Pin Assignments Si8271

Table 1. Si8271 Pin Descriptions

Pin	Name	Description
1	VI	Digital driver control signal
2	VDDI	Input side power supply
3	GNDI	Input side ground
4	EN	Enable
5	GND	Driver side ground
6	VO–	Gate drive pull low
7	VO+	Gate drive pull high
8	VDD	Driver side power supply

1.2. Si8273/75 Pin Descriptions

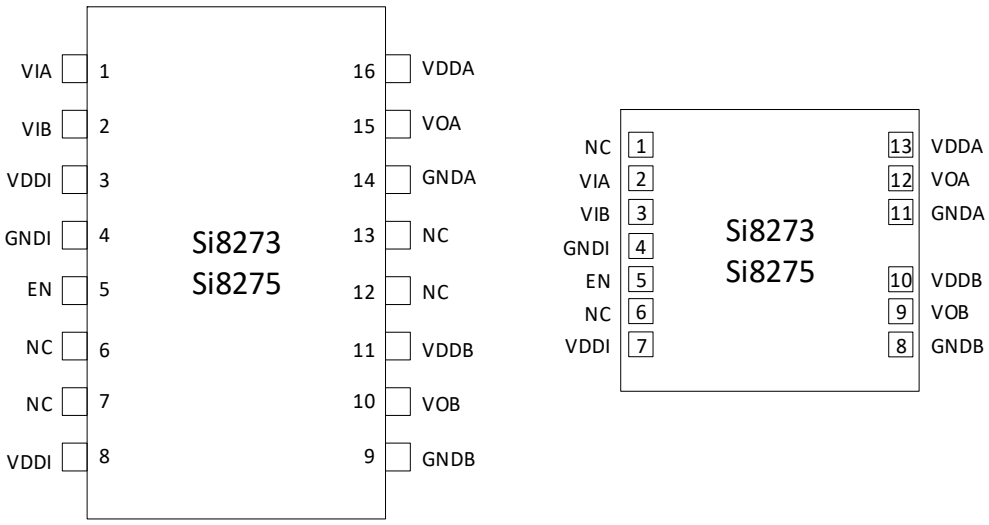


Figure 2. Pin Assignments Si8273/5

Table 2. Si8273/5 Pin Descriptions

NB SOIC-16 Pin #	LGA-13 Pin #	Name	Description
1	2	VIA	Digital driver control signal for “A” driver
2	3	VIB	Digital driver control signal for “B” driver
3,8	7	VDDI	Input side power supply
4	4	GNDI	Input side ground
5	5	EN	Enable
6, 7, 12, 13	1, 6	NC	No Connect
9	8	GNDB	Driver side power supply for “B” driver
10	9	VOB	Gate drive output for “B” driver
11	10	VDDB	Driver side power supply for “B” driver
14	11	GNDA	Driver side power supply for “A” driver
15	12	VOA	Gate drive output for “A” driver
16	13	VDDA	Driver side power supply for “A” driver

1.3. Si8274 Pin Descriptions

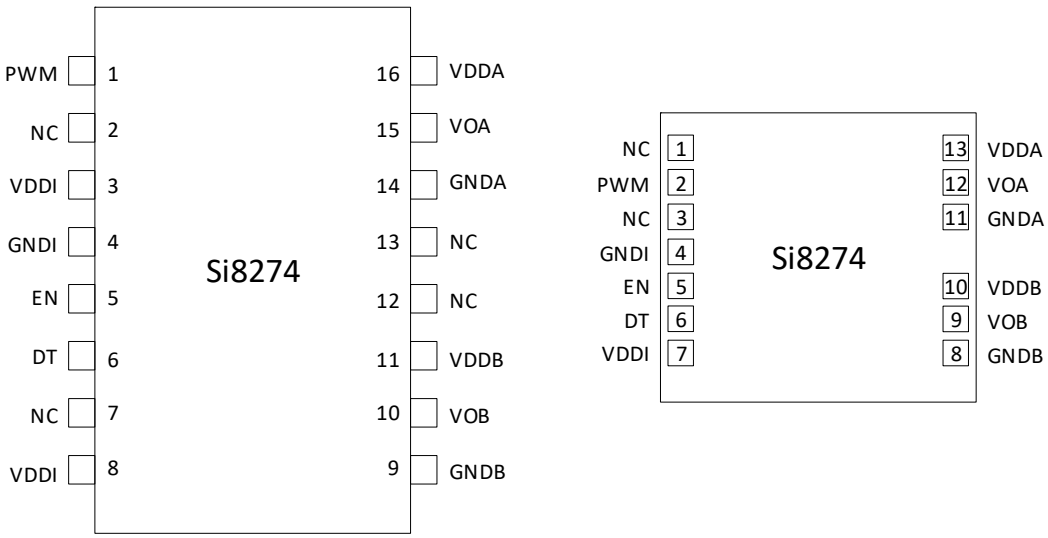


Figure 3. Pin Assignments Si8274

Table 3. Si8274 Pin Descriptions

NB SOIC-16 Pin #	LGA-13 Pin #	Name	Description
1	2	PWM	Pulse width modulated driver control signal
2, 7, 12, 13	1, 3	NC	No Connect
3, 8	7	VDDI	Input side power supply
4	4	GNDI	Input side ground
5	5	EN	Enable
6	6	DT	Dead-time control
9	8	GNDB	Driver side power supply for “B” driver
10	9	VOB	Gate drive output for “B” driver
11	10	VDDB	Driver side power supply for “B” driver
14	11	GNDA	Driver side power supply for “A” driver
15	12	VOA	Gate drive output for “A” driver
16	13	VDDA	Driver side power supply for “A” driver

2. System Overview

2.1. Top Level Block Diagrams

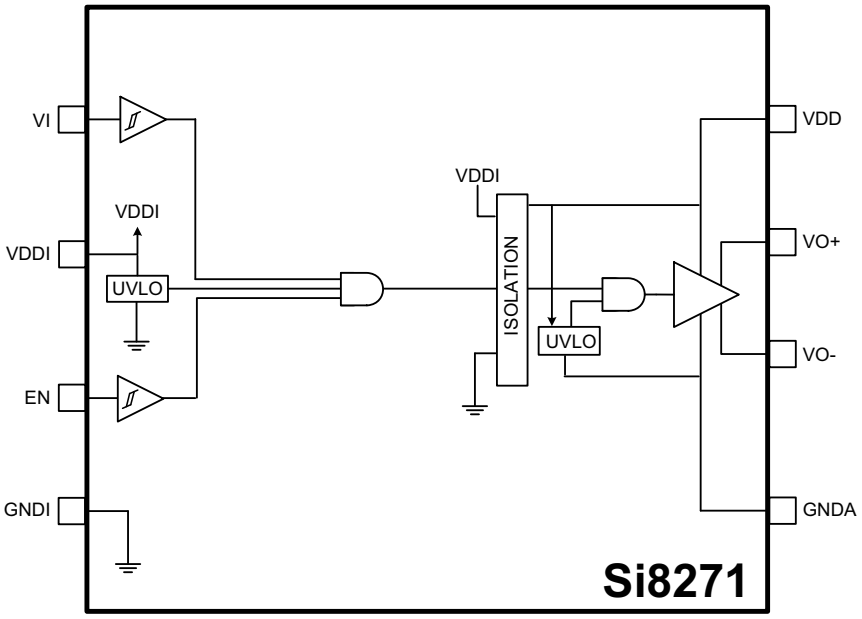


Figure 4. Si8271 Block Diagram

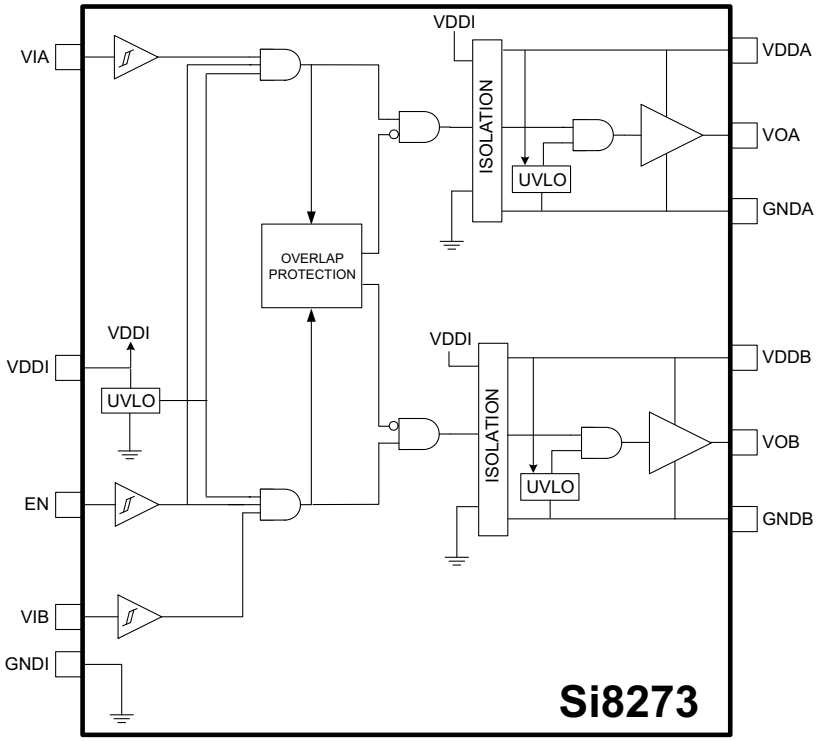


Figure 5. Si8273 Block Diagram

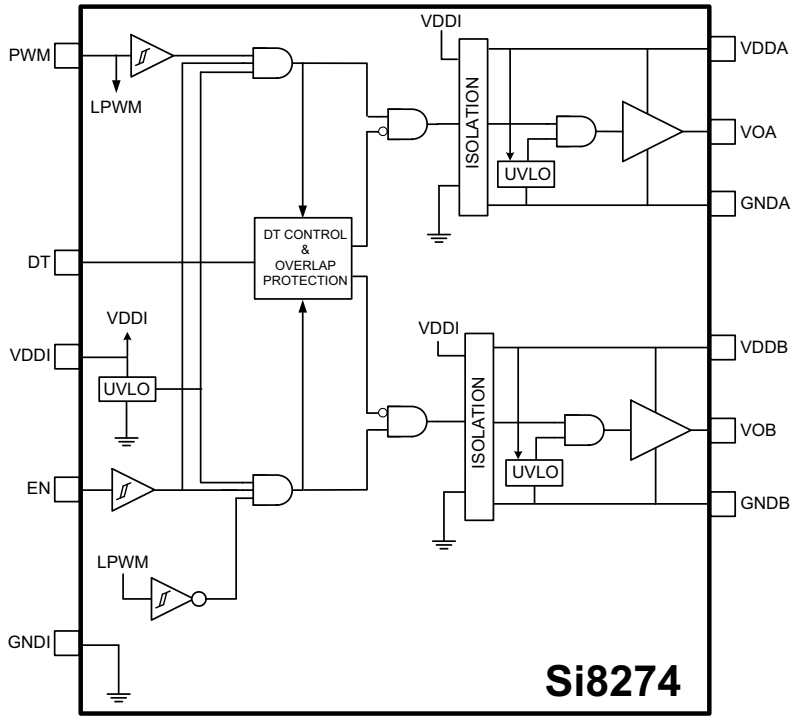


Figure 6. Si8274 Block Diagram

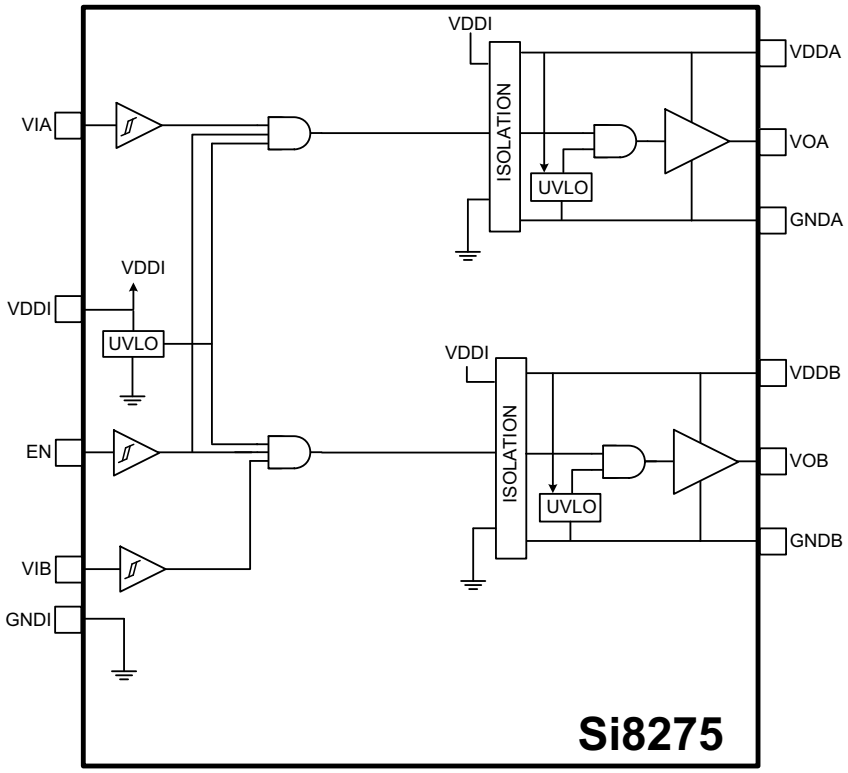


Figure 7. Si8275 Block Diagram

2.2. Functional Description

The operation of an Si827x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si827x channel is shown in the figure below.

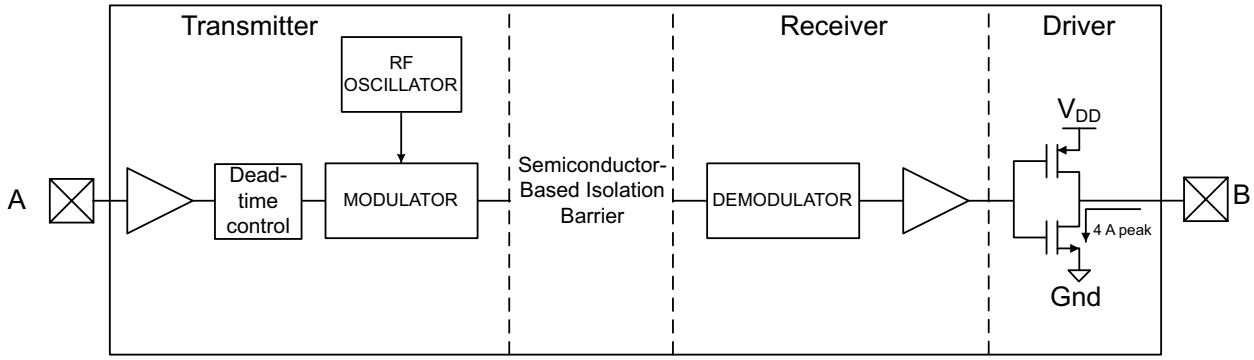


Figure 8. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 9 for more details.

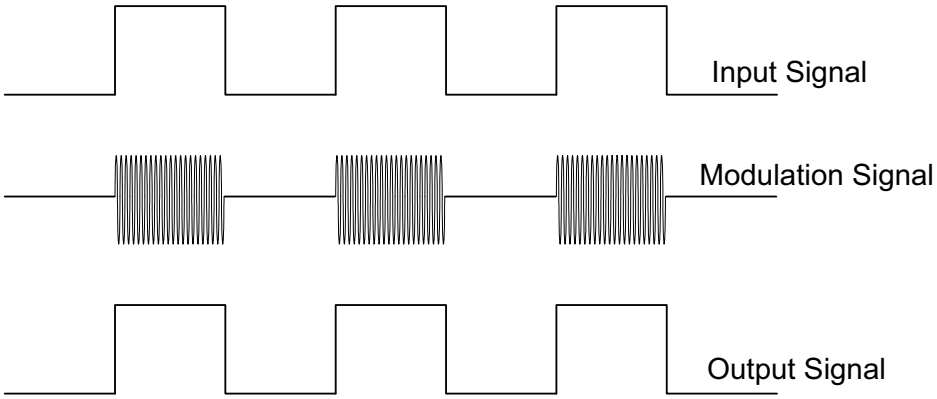


Figure 9. Modulation Scheme

2.3. Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to Table 8, “Electrical Characteristics,” on page 21 for actual specification limits.

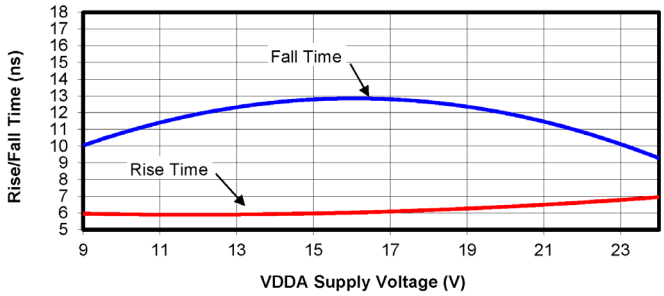


Figure 10. Rise/Fall Time vs. Supply Voltage

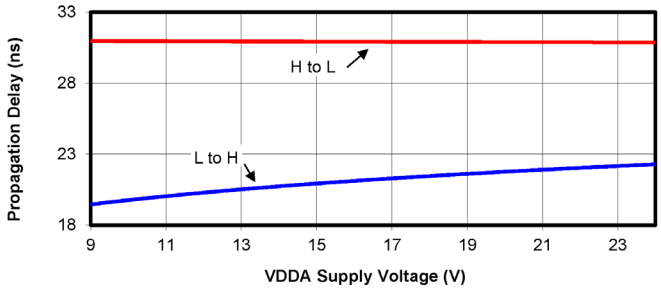


Figure 11. Propagation Delay vs. Supply Voltage

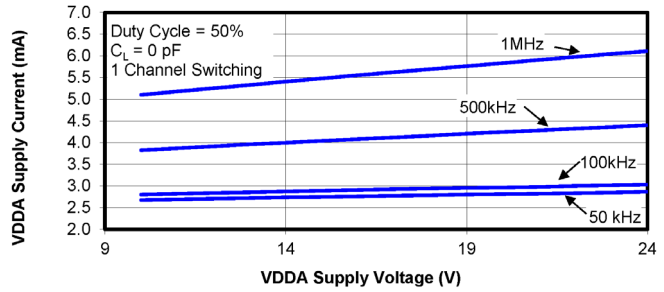


Figure 12. Supply Current vs. Supply Voltage

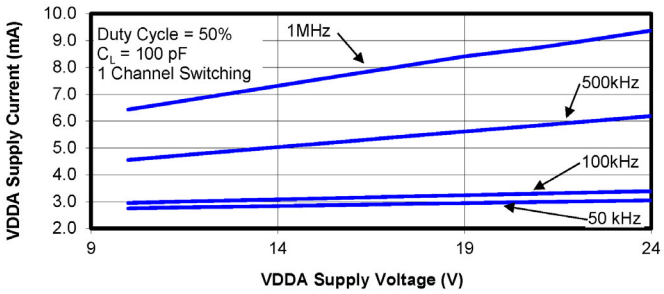


Figure 13. Supply Current vs. Supply Voltage

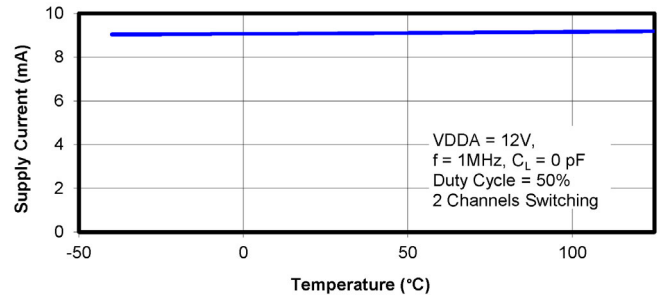


Figure 14. Supply Current vs. Temperature

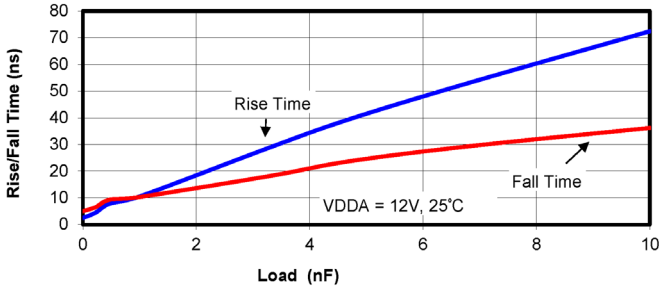


Figure 15. Rise/Fall Time vs. Load

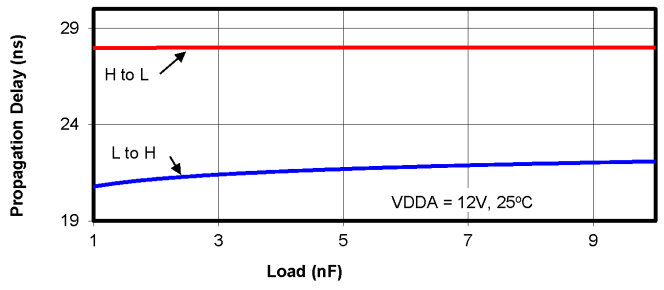


Figure 16. Propagation Delay vs. Load

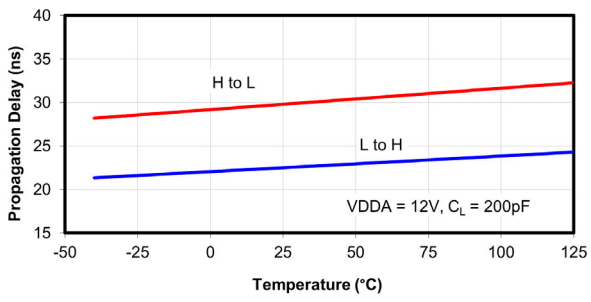


Figure 17. Propagation Delay vs. Temperature

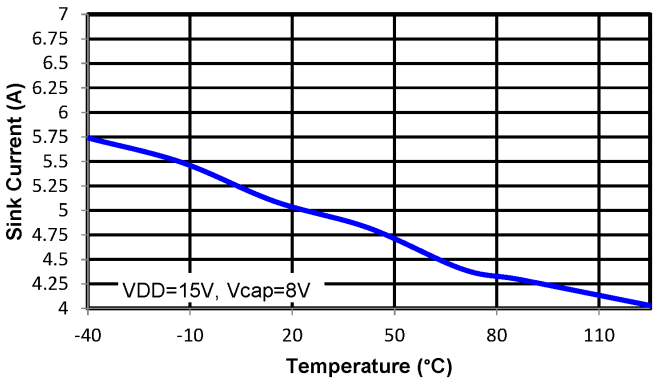


Figure 18. Output Sink Current vs. Temperature

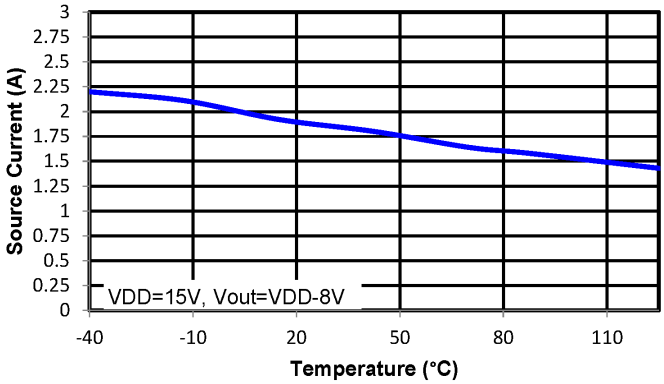


Figure 19. Output Source Current vs. Temperature

2.4. Family Overview and Logic Operation During Startup

The Si827x family of isolated drivers consists of single, high-side/low-side, and dual driver configurations.

2.4.1. Products

The following table shows the configuration and functional overview for each product in this family.

Table 4. Si827x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8271	Single Driver	—	—	VI	4.0
Si8273	High-Side/Low-Side	Y	—	VIA, VIB	4.0
Si8274	PWM	Y	Y	PWM	4.0
Si8275	Dual Driver	—	—	VIA, VIB	4.0

2.4.2. Device Behavior

The following table consists of truth tables for the Si8271, Si8273, Si8274, and Si8275 families.

Table 5. Si827x Family Truth Table[1]

Si8271 (Single Driver) Truth Table					
Inputs	VDDI State	Enable	Output		Notes
VI			VO+	VO–	
L	Powered	H	Hi–Z	L	
H	Powered	H	H	Hi–Z	
X[2]	Unpowered	X	Hi–Z	L	
X	Powered	L	Hi–Z	L	

Si8273 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
L	H	Powered	H	L	H	
H	L	Powered	H	H	L	
H	H	Powered	H	L	L	Invalid state
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration
X	X	Powered	L	L	L	Device is disabled

Si8274 (PWM Input High-Side/Low-Side) Truth Table					
PWM Input	VDDI State	Enable	Output		Notes
			VOA	VOB	
H	Powered	H	H	L	
L	Powered	H	L	H	
X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	Powered	L	L	L	Device is disabled.

Si8275 (Dual Driver) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
L	H	Powered	H	L	H	
H	L	Powered	H	H	L	
H	H	Powered	H	H	H	

Table 5. Si827x Family Truth Table[1] (Continued)

Si8271 (Single Driver) Truth Table					
Inputs	VDDI State	Enable	Output		Notes
VI			VO+	VO–	
L	Powered	H	Hi–Z	L	
H	Powered	H	H	Hi–Z	
X[2]	Unpowered	X	Hi–Z	L	
X	Powered	L	Hi–Z	L	

Si8273 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
L	H	Powered	H	L	H	
H	L	Powered	H	H	L	
H	H	Powered	H	L	L	Invalid state
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration
X	X	Powered	L	L	L	Device is disabled

Si8274 (PWM Input High-Side/Low-Side) Truth Table					
PWM Input	VDDI State	Enable	Output		Notes
			VOA	VOB	
H	Powered	H	H	L	
L	Powered	H	L	H	
X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	Powered	L	L	L	Device is disabled.

Si8275 (Dual Driver) Truth Table						
Inputs		VDDI State	Enable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	H	L	L	
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	L	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.5.2. "Undervoltage Lockout" for more information.
2. An input can power the input die through an internal diode if its source has adequate current.

2.5. Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 20, “Device Behavior during Normal Operation and Shutdown,” on page 14, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively.

It is important to note that the driver outputs (VO) will default to a low output state when the input side power supply (VDDI) is not present, but the output side power supply (VDDx) is present.

2.5.1. Device Startup

Driver outputs (VO) are held low during power-up until the device power supplies are above the UVLO threshold for time period t_{START}. Following this, the outputs follow the state of device inputs (VI).

2.5.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when the device power supplies are below their specified operating circuits range. The input (control) side, and each driver on the output side, have their own undervoltage lockout monitors.

The Si827x input side enters UVLO when VDDI < $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver output (VO) remains low when the input side of the Si827x is in UVLO and VDDx is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

The UVLO circuit unconditionally drives VO low when VDDx is below the lockout threshold. Upon power up, the Si827x is maintained in UVLO until VDDx rises above $VDDx_{UV+}$. During power down, the Si827x enters UVLO when VDDx falls below $VDDx_{UV-}$. Please refer to spec tables for UVLO values.

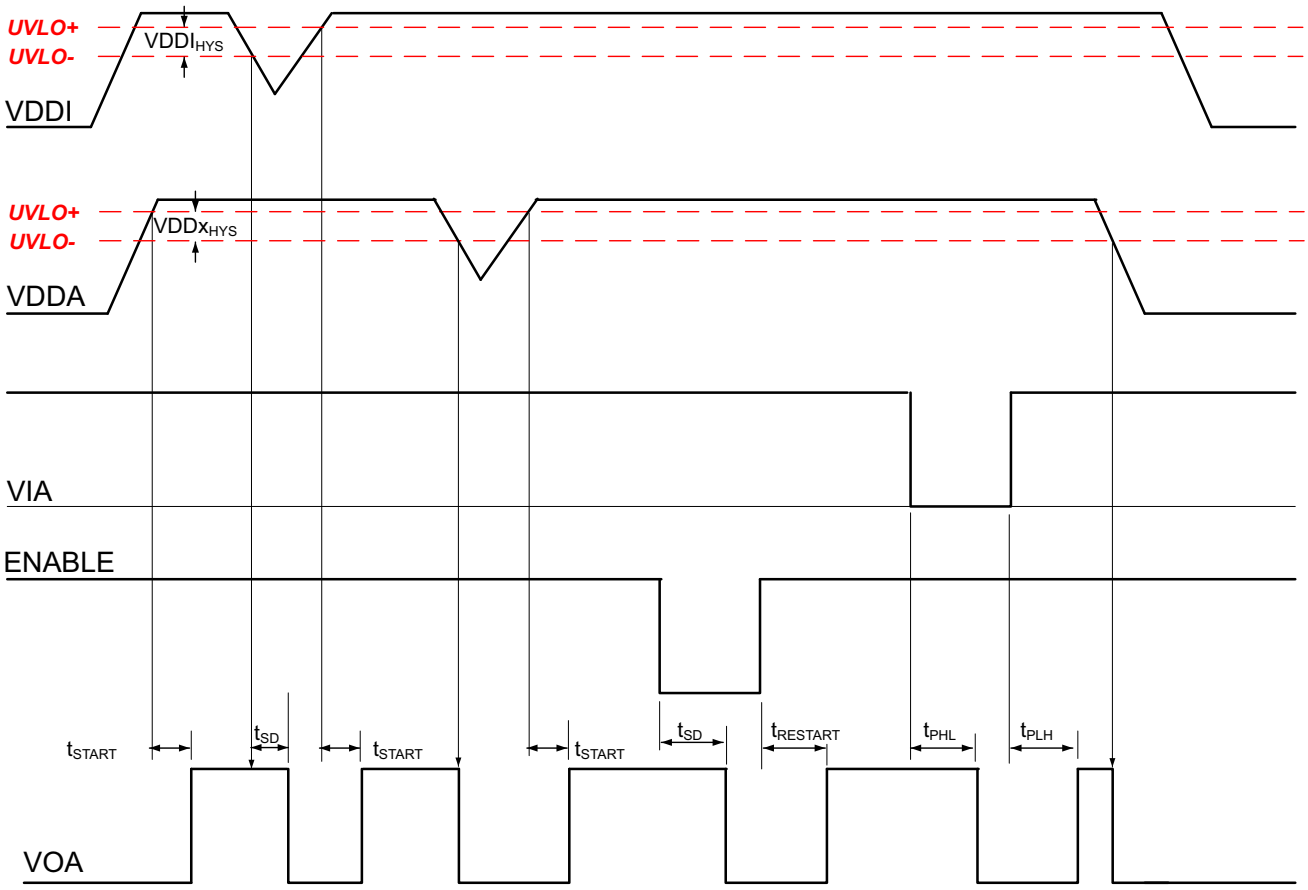


Figure 20. Device Behavior during Normal Operation and Shutdown

2.5.3. Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8274), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.5.4. Enable Input

When brought low, the ENABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within t_{SD} after ENABLE = V_{IL} and resumes within $t_{RESTART}$ after ENABLE = V_{IH}. The ENABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

2.6. Programmable Dead Time and Overlap Protection

Overlap protection prevents the two driver outputs from both going high at the same time. Programmable dead time control sets the amount of time between one output going low and the other output going high.

All drivers configured as high-side/low-side pairs with separate inputs (Si8273x) have overlap protection. See Figure 21 and Table 6. Drivers controlled with a single input (Si8274x) have inherit overlap protection by virtue of one driver being active high and the other being active low with respect to the PWM input.

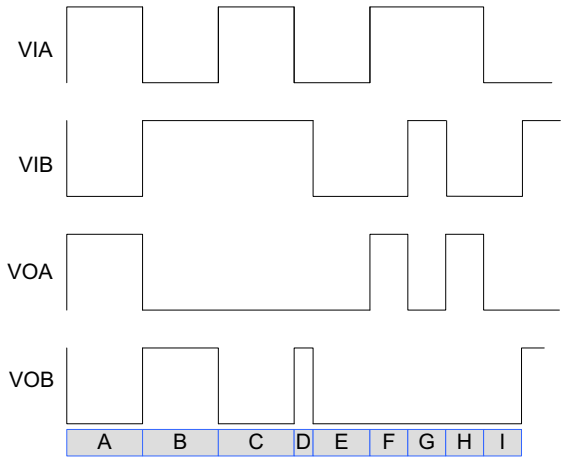


Figure 21. Input and Output Waveforms for Si8273x Drivers

Table 6. Description of Input and Output Waveforms for Si8273x Drivers

Reference	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

All high-side/low-side drivers with a single PWM input (Si8274x) include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions. The amount of dead time delay (DT) is programmed by a single resistor (R_{DT}) connected from the DT input to ground per the equation below. Note that the dead time pin should be connected to GNDI through a resistor between the values of 6 kΩ and 100 kΩ. To aid in noise immunity, place a 0.1 µF ceramic capacitor in parallel with R_{DT}. The capacitor should be placed as close to the DT pin as possible. See Figure 22 below.

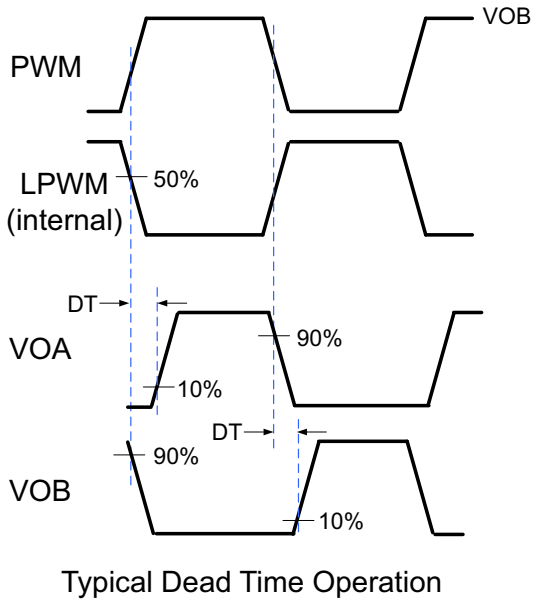
$$DT = 2.02 \times RDT + 7.77 \text{ (for 10-200 ns range)}$$
$$DT = 6.06 \times RDT + 3.84 \text{ (for 20-700 ns range)}$$

where:

DT is the dead time (ns)

RDT is the dead time programming resistor (kΩ)

Equation 1.



Typical Dead Time Operation

Figure 22. Dead-Time Waveforms for Si8274x Drivers

2.7. Deglitch Feature

A deglitch feature is provided on some options, as defined in the 8. "Ordering Guide". The internal deglitch circuit provides an internal time delay of 15 ns typical, during which any noise is ignored and will not pass through the IC. For these product options, the propagation delay will be extended by 15 ns, as specified in the spec table.

3. Application Information

The device is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate configuration must be selected and its circuit carefully designed.

3.1. Recommended Application Circuits

The following examples illustrate typical circuit configurations using the Si827x.

3.1.1. High-Side/Low-Side Driver

In Figure 23, side A shows the Si8273 controlled using the VIA and VIB input signals, and side B shows the Si8274 controlled by a single PWM signal.

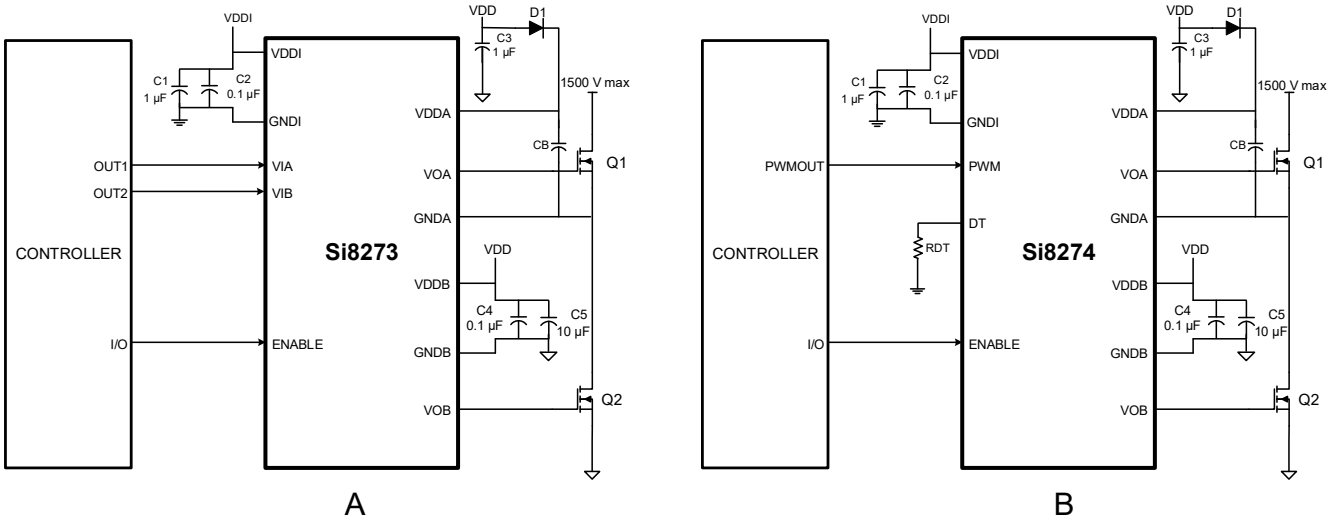


Figure 23. Si827x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si827x requires VDDI in the range of 2.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 4.2 V and 30 V with respect to their respective grounds. The boot-strap start up time will depend on the CB capacitor chosen. VDD is usually the same as VDDB. Also, note that the bypass capacitors on the Si827x should be located as close to the chip as possible. Moreover, it is recommended that bypass capacitors be used (as shown in the figures above for input and driver side) to reduce high frequency noise and maximize performance. The outputs VOA and VOB can be used interchangeably as high-side or low-side drivers.

3.1.2. Dual Driver

Figure 24 shows the Si827x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.

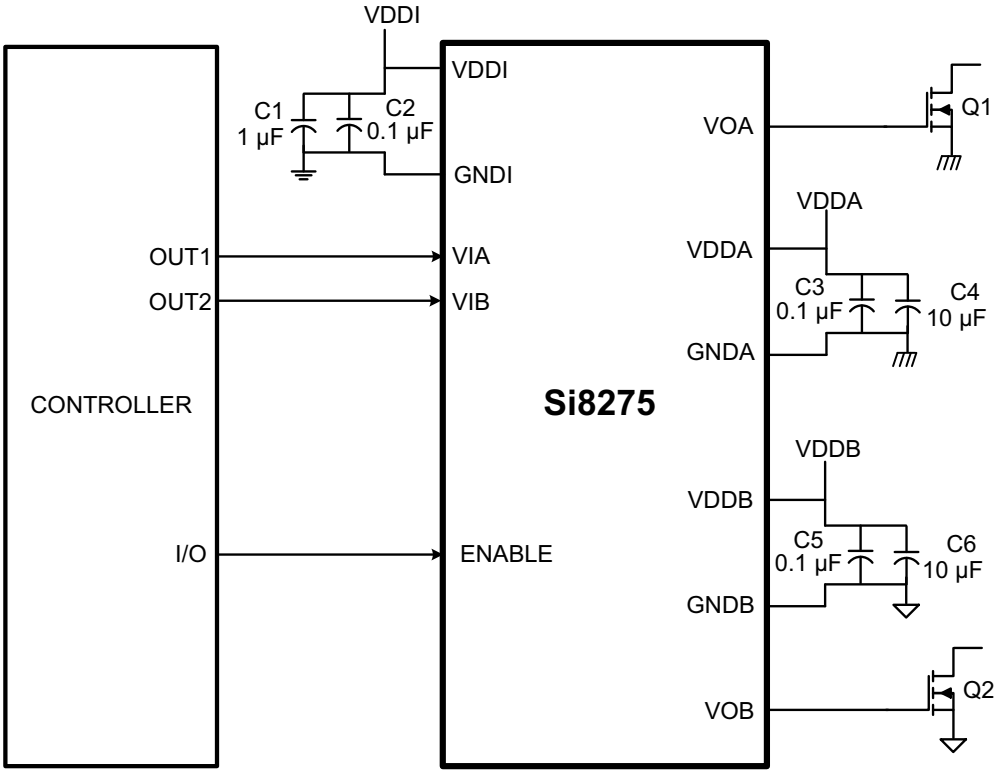


Figure 24. Si827x in a Dual Driver Application

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. That is, the voltage at VOA can be higher or lower than that of VOB by VDD without damaging the driver. Therefore, a dual driver in a high-side/low-side drive application can use either VOA or VOB as the high-side driver. Similarly, a dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

3.2. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si827x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it.
Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

3.3. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Please refer to "3.1. Recommended Application Circuits" on page 17 for specific parts referenced.

3.3.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between gate drivers A and B on the gate driver side is usually not required. If the system needs safety isolation between gate drivers A and B, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between gate drivers A and B is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si827x device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si827x device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si827x device to avoid unwanted noise coupling.

3.3.2. Logic Input Considerations

- Place resistor R_{DT} close to the device's dead time (DT) pin.
- If the application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the device should be kept from any noisy signals in the system.

3.3.3. Gate Driver Considerations

- It is recommended to use ≥20 mil trace width for the VOA/B gate driver traces and their return path.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, use ≥20 mil trace width for the power supply connections.
- If the design utilizes Y2 capacitors between the logic input and gate drivers, the Y2 capacitors across the isolation barrier should be placed as close as possible to the sides of the device without pins.

3.4. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of AN1339 to easily estimate the device's power dissipation and silicon junction temperature.

4. Specifications

4.1. Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Units
Storage temperature	T_{STG}	–65	+150	°C
Operating temperature (OPNs with "-ZS" suffix)	T_A	–55	+125	°C
Operating temperature (all other OPNs)	T_A	–40	+125	°C
Junction temperature	T_J	—	+150	°C
Logic input supply voltage	VDDI	–0.6	6.0	V
Gate driver supply voltage	VDD, VDDA, VDDB	–0.6	36	V
Voltage on any pin with respect to ground	V_{IO}	–0.5	V_{DD} + 0.5	V
Output voltage to GND, repeat spike of –1.2 V for 200 ns, 200 kHz	VO+, VO–, VOA, VOB	–1.2	V_{DD} + 0.5	V
Lead solder temperature (10 s)		—	260	°C
Latch-up immunity		—	400	kV/µs
ESD per AEC-Q100				
Human body model	HBM	—	3.5	kV
Charged device model	CDM	—	2000	V

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

4.2. Electrical Characteristics

Table 8. Electrical Characteristics

VDDI = 2.5 to 5.5 V; VDDx – GNDx = 4.2 to 30 V; T_A = –40 to +125 °C (T_A = –55 to +125 °C for OPNs with "-ZS" suffix).
Typical specifications at VDDI = 5 V; VDDx – GNDx = 15 V; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input supply voltage	VDDI	VDDI – GNDI	2.5	—	5.5	V
Driver supply voltage	VDDx[1]	VDDx – GNDx	4.2	—	30	V
Input supply quiescent current	IDD_Q		—	7.9	10.0	mA
Input supply active current	IDDI	f = 500 kHz	—	8.0	10.0	mA
Output supply quiescent current	$IDDx_Q$[2]		—	2.5	4.0	mA
Output supply active current	IDDx[2]	f = 500 kHz (no load)	—	10.0	11.0	mA
Gate Driver						
High output transistor RDS (ON)	R_{OH}		—	2.7	—	Ω
Low output transistor RDS (ON)	R_{OL}		—	1.0	—	Ω
High-level peak output current	I_{OH}	VDDx = 15 V, See Figure 26 for Si827xG, VDDx = 4.2 V, t_{PW_IOH} < 250 ns	—	1.8	—	A
Low-level peak output current	I_{OL}	VDDx = 15 V, See Figure 25 for Si827xG, VDDx = 4.2 V, t_{PW_IOL} < 250 ns	—	4.0	—	A
UVLO						
VDDI UVLO threshold +	$VDDI_{UV+}$		1.85	2.2	2.45	V
VDDI UVLO threshold –	$VDDI_{UV–}$		1.75	2.1	2.35	V
VDDI hysteresis	$VDDI_{HYS}$		—	100	—	mV
UVLO threshold + (Driver Side)						
3 V threshold	$VDDx_{UV+}$[1]		2.7	3.5	4.0	V
5 V threshold			4.9	5.5	6.3	V
8 V threshold			7.2	8.3	9.5	V
12 V threshold			11	12.2	13.5	V
UVLO threshold – (Driver Side)						
3 V threshold	$VDDx_{UV–}$[1]		2.5	3.0	3.8	V
5 V threshold			4.6	5.2	5.9	V
8 V threshold			6.7	7.8	8.9	V
12 V threshold			9.6	10.8	12.1	V

Table 8. Electrical Characteristics (Continued)

VDDI = 2.5 to 5.5 V; VDDx – GNDx = 4.2 to 30 V; T_A = –40 to +125 °C (T_A = –55 to +125 °C for OPNs with "-ZS" suffix).
Typical specifications at VDDI = 5 V; VDDx – GNDx = 15 V; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
UVLO Lockout Hysteresis						
3 V threshold	$VDDx_{HYS}$		—	500	—	mV
5 V threshold			—	300	—	mV
8 V threshold			—	500	—	mV
12 V threshold			—	1400	—	mV
Digital						
Logic high input threshold	V_{IH}		2.0	—	—	V
Logic low input threshold	V_{IL}		—	—	0.8	V
Input hysteresis	V_{HYST}		350	400	—	mV
Logic high output voltage	V_{OH}	I_O = –1 mA	VDDx – 0.04	—	—	V
Logic low output voltage	V_{OL}	I_O = 1 mA	—	—	0.04	V
AC Switching Parameters						
Minimum pulse width			—	30	—	ns
Propagation delay Si8271/3/5 with low jitter	t_{PLH}, t_{PHL}	C_L = 200 pF	20	30	60	ns
Propagation delay Si8271/3/5 with deglitch option	t_{PLH},t_{PHL}	C_L = 200 pF	30	45	75	ns
Propagation delay Si8274 with low jitter	t_{PHL}	C_L = 200 pF	20	30	60	ns
Propagation delay Si8274 with deglitch option	t_{PHL}	C_L = 200 pF	30	45	75	ns
Propagation delay Si8274 with low jitter	t_{PLH}	C_L = 200 pF	30	45	75	ns
Propagation delay Si8274 with deglitch option	t_{PLH}	C_L = 200 pF	65	85	105	ns
Pulse width distortion Si8271/3/5 all options	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	3.6	8	ns
Pulse width distortion Si8274 with low jitter	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	14	19	ns
Pulse width distortion Si8274 with deglitch option	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	38	47	ns
Peak-to-peak jitter Si827x with low jitter	$t_{JIT(PK)}$		—	200	—	ps
Programmed dead time (DT) for products with 10 to 200 ns DT range	DT	R_{DT} = 6 kΩ	10	20	30	ns
		R_{DT} = 15 kΩ	26	38	50	
		R_{DT} = 100 kΩ	150	210	260	
Programmed dead time (DT) for products with 20 to 700 ns DT range	DT	R_{DT} = 6 kΩ	23	40	57	ns
		R_{DT} = 15 kΩ	60	95	130	
		R_{DT} = 100 kΩ	450	610	770	
Rise time	t_R	CL = 200 pF	4	10.5	16	ns

Table 8. Electrical Characteristics (Continued)

VDDI = 2.5 to 5.5 V; VDDx – GNDx = 4.2 to 30 V; T_A = –40 to +125 °C (T_A = –55 to +125 °C for OPNs with "-ZS" suffix).
Typical specifications at VDDI = 5 V; VDDx – GNDx = 15 V; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Fall time	t_F	CL = 200 pF	5.5	13.3	18	ns
Shutdown time from Enable False	t_{SD}		—	—	60	ns
Restart time from Enable True	$t_{RESTART}$		—	—	60	ns
Device startup time	t_{START}		—	16	30	µs
Common-mode transient immunity Si827x with deglitch option	CMTI	See Figure 27. VCM = 1500 V	200	350	400	kV/µs
Common-mode transient immunity Si827x with low jitter option	CMTI	See Figure 27. VCM = 1500 V	150	300	400	kV/µs
Input capacitance[3]	C_I	f = 100 kHz	—	3.0	—	pF

1. The symbols VDD, VDDA, and VDDB all refer to the driver supply voltage but reflect the different pin names used for the supply on different product options. Specifications that apply to the driver supply voltage are also referred to as VDDx in this data sheet.
2. The symbols IDD, IDDA, and IDDB all refer to the driver supply current, but reflect the different pin names used for the supply on different product options. Specifications that apply to the driver supply current are also referred to as IDDx in this data sheet.
3. Measured from input to ground.

4.3. Test Circuits

The following figures depict sink current, source current, and common-mode transient immunity test circuits.

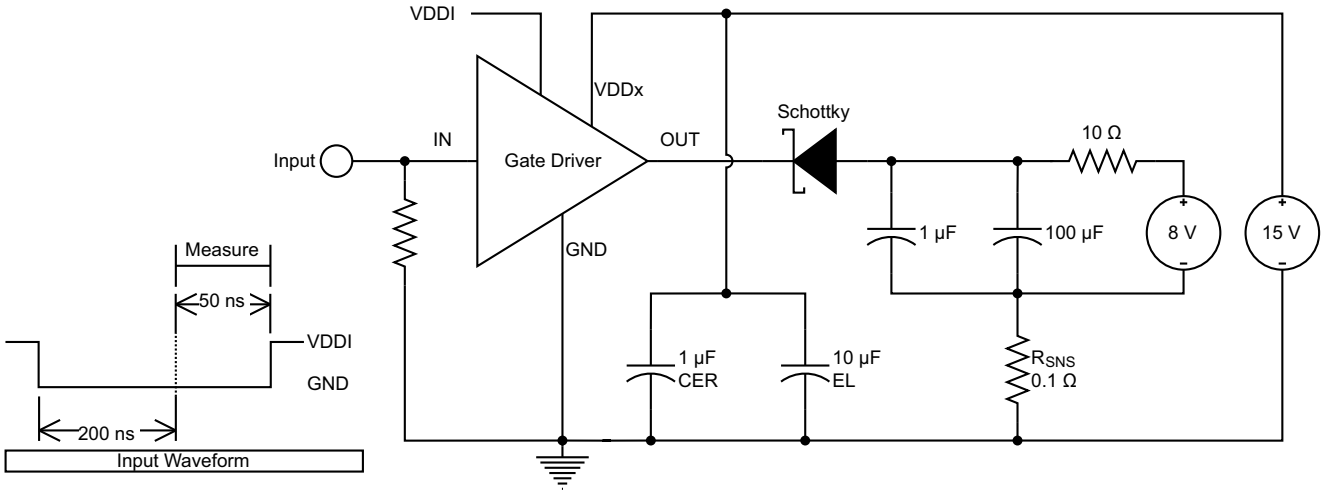


Figure 25. IOL Sink Current Test Circuit

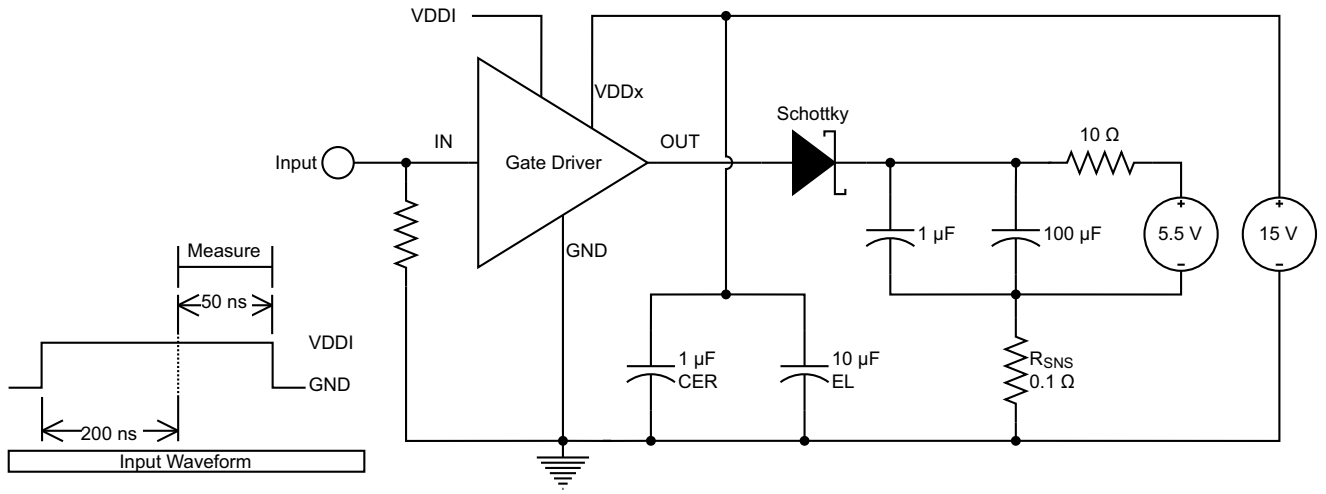


Figure 26. IOH Source Current Test Circuit

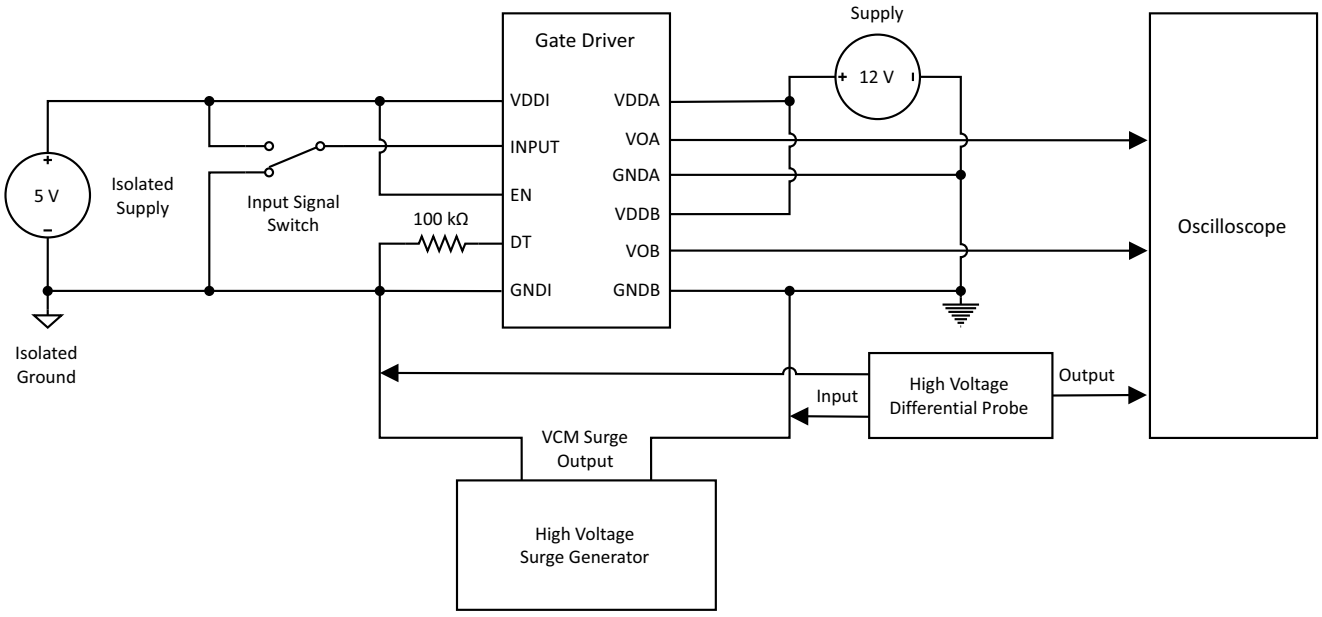


Figure 27. Common-Mode Transient Immunity Test Circuit

4.4. Thermal Characteristics

Table 9. Thermal Characteristics

Parameter	Symbol	SOIC-8	NB SOIC-16	LGA-13	Unit
IC junction-to-air thermal resistance	θ_{JA}	115	104	109	°C/W

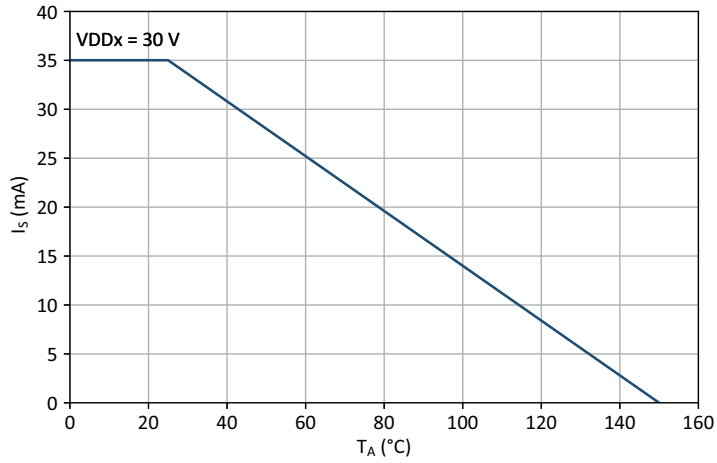


Figure 28. NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

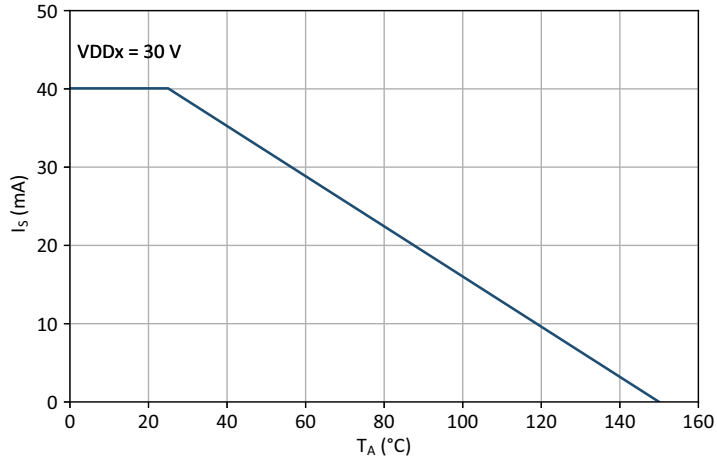


Figure 29. NB SOIC-16 Safety Current vs. Ambient Temperature Derating Curve

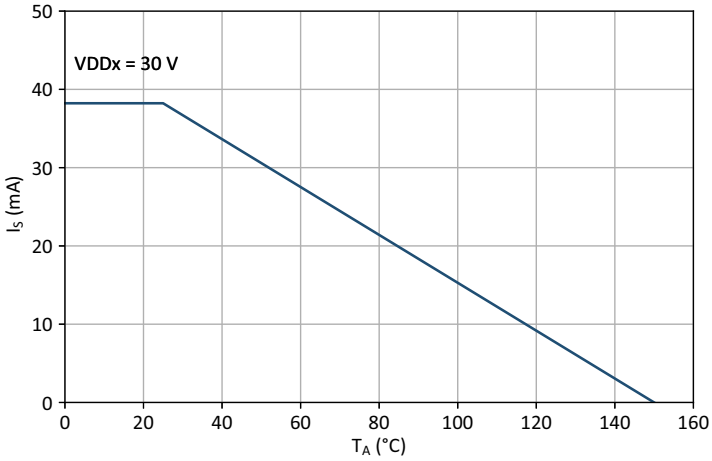


Figure 30. LGA-13 Safety Current vs. Ambient Temperature Derating Curve

4.5. Safety Certifications and Specifications

Table 10. Regulatory Information[1]

CSA
The Si827x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Rated up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si827x is certified under VDE. For more details, see File 5028467.
60747-17: Rated up to 630 V_{PEAK} for basic insulation working voltage.
UL
The Si827x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2.5 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si827x is certified under GB4943.1.
Rated up to 250 V_{RMS} basic insulation working voltage at 5000 meters tropical climate.

1. For more information, see "8. Ordering Guide" on page 41.

Table 11. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			SOIC-8	NB SOIC-16	LGA-13	
Nominal external air gap (clearance)[1,2,3]	CLR		3.9	3.9	3.5	mm
Nominal external tracking (creepage)[1,2,3]	CRP		3.9	3.9	3.5	mm
Minimum internal gap (internal clearance)	DTI		0.008	0.008	0.008	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	600	V_{RMS}

1. CSA certifies the clearance and creepage limits listed in this table.
2. UL does not impose a clearance and creepage minimum for component-level certifications.
3. VDE certifies the clearance and creepage limits as: SOIC-8 $\geq$ 4.7 mm, NB SOIC-16 $\geq$ 4.7 mm, and LGA-13 $\geq$ 3.5 mm.

Table 12. IEC60664-1 Ratings

Parameter	Test Conditions	Specification		
		SOIC-8	NB SOIC-16	LGA-13
Material group		I	I	I
Overvoltage category	Rated mains voltage ≤ 100 V_{RMS}	I-IV	I-IV	I-IV
	Rated mains voltage ≤ 150 V_{RMS}	I-III	I-III	I-III
	Rated mains voltage ≤ 300 V_{RMS}	I-II	I-II	I-II
	Rated mains voltage ≤ 600 V_{RMS}	I	I	I

Table 13. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			SOIC-8	NB SOIC-16	LGA-13	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	445	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	630	630	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.5 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	≤ 5	≤ 5	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	3535	3535	3535	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with ≥1.3 x V_{IMP} and 1.2 µs/50 µs profile (qualification)	4000	4000	4000	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	3077	3077	3077	V_{PEAK}
Capacitance (input-output)[2]	C_{IO}	f = 1 MHz	0.5	0.5	0.5	pF
Isolation resistance[2]	R_{IO}	T_A = 25 °C, V_{IO} = 500 V	$>10^{12}$	$>10^{12}$	$>10^{12}$	Ω
		T_A = 125 °C, V_{IO} = 500 V	$>10^{11}$	$>10^{11}$	$>10^{11}$	Ω
	R_{IO_S}	T_A = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	2	
Climatic category			40/125/21	40/125/21	40/125/21	

1. This coupler is suitable for “basic insulation” only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.
2. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 14. IEC60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			SOIC-8	NB SOIC-16	LGA-13	
Safety temperature	T_S		150	150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in Table 9 on page 26. VDDI = 5.5 V, VDDx = 30 V, T_J = 150 °C, T_A = 25 °C.	35.0	40.0	38.0	mA
Safety input, output, or total power	P_S	Refer to θ_{JA} in Table 9 on page 26. T_J = 150 °C, T_A = 25 °C.	1.10	1.20	1.15	W

1. Maximum value allowed in the event of a failure; Refer to Figure 28, Figure 29, and Figure 30 for thermal derating curves.

Table 15. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Max			Unit
			SOIC-8	NB SOIC-16	LGA-13	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	2500	2500	2500	V_{RMS}
Primary-side current rating		VDDI = 5.5 V, VDDx = 30 V, T_A = 25 °C, (qualification)	10	10	10	mA
Primary-side power rating			60	60	60	mW
Secondary-side current rating			19	38	40	mA
Secondary-side power rating			570	1140	1200	mW

5. Package Outlines

5.1. Package Outline: 16-Pin Narrow-Body SOIC

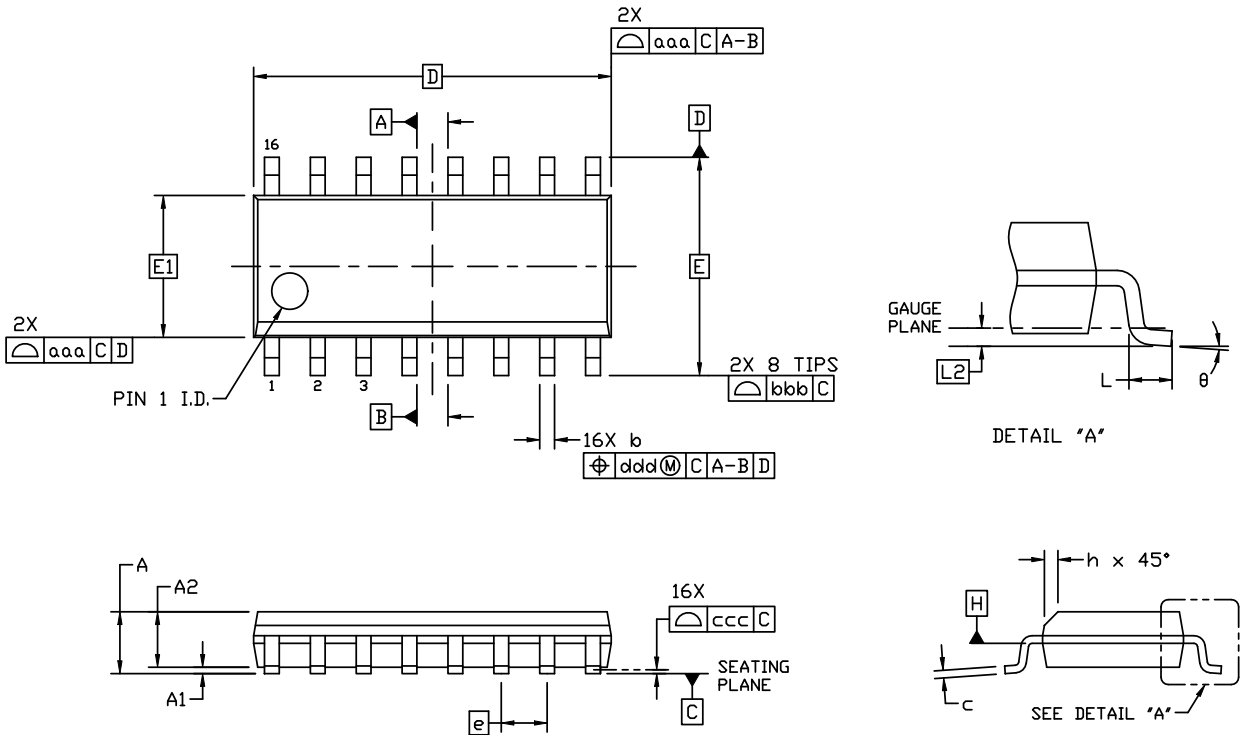


Figure 31. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 16. Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max		Dimension	Min	Max
A	—	1.75		L	0.40	1.27
A1	0.10	0.25		L2	0.25 BSC	
A2	1.25	—		h	0.25	0.50
b	0.31	0.51		θ	0°	8°
c	0.17	0.25		aaa	0.10	
D	9.90 BSC			bbb	0.20	
E	6.00 BSC			ccc	0.10	
E1	3.90 BSC			ddd	0.25	
e	1.27 BSC					

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2. Package Outline: 8-Pin Narrow Body SOIC

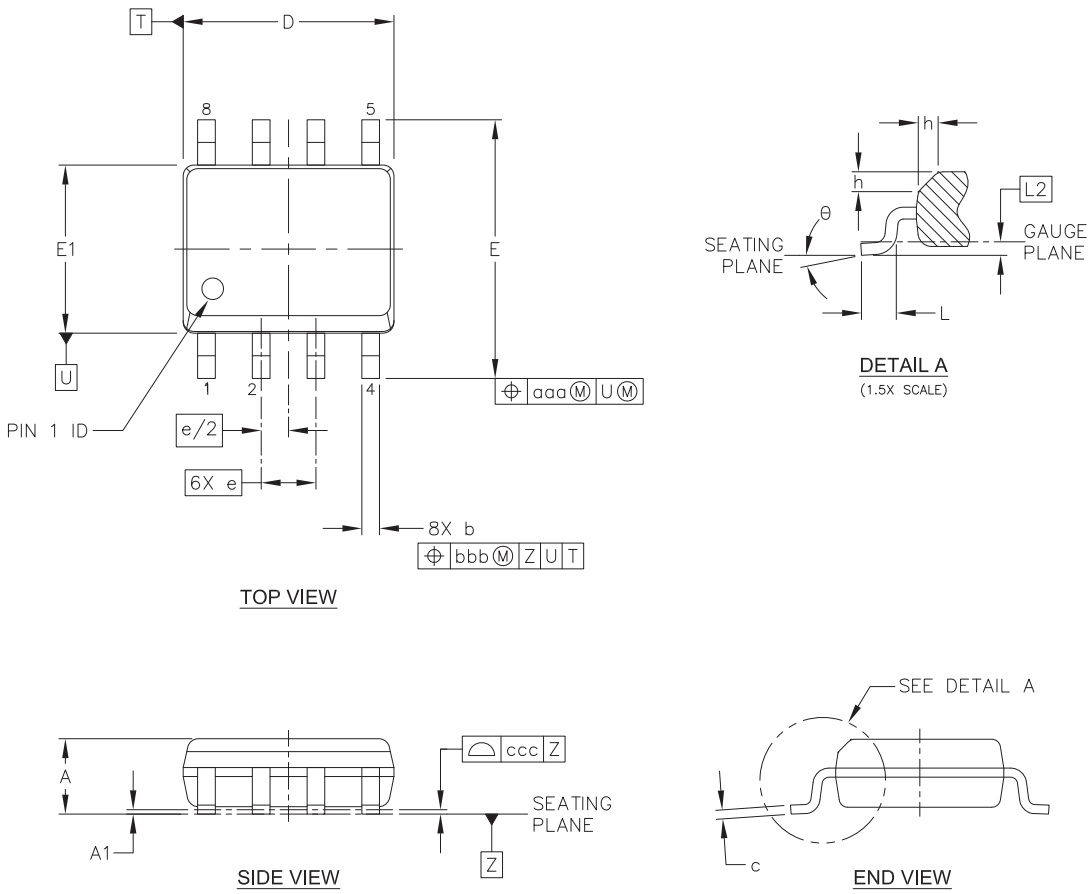


Figure 32. 8-Pin Narrow Body SOIC Package

Table 17. 8-Pin Narrow Body SOIC Package Diagram Dimensions[1,2,3,4,5]

Dimension	Symbol	Min	Max
Overall height	A	—	1.75
Stand off	A1	0.10	0.25
Lead width	b	0.33	0.51
L/F thickness	c	0.19	0.25
Body size	D	4.80	5.00
	E	5.80	6.20
	E1	3.80	4.00
Lead pitch	e	1.27 BSC	
Lead length	L	0.40	1.27
Gauge plane	L2	0.25 BSC	
Corner chamfer	h	0.25	0.50
Foot angle	θ	0°	8°

Table 17. 8-Pin Narrow Body SOIC Package Diagram Dimensions[1,2,3,4,5]

Dimension	Symbol	Min	Max
Lead edge tolerance	aaa		0.10
Lead offset	bbb		0.20
Coplanarity	ccc		0.10

1. All linear dimensions are in millimeters.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   BSC: Basic dimension. Theoretically exact shown without tolerance.
   REF: Reference dimension. Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end.
   Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

5.3. Package Outline: LGA-13

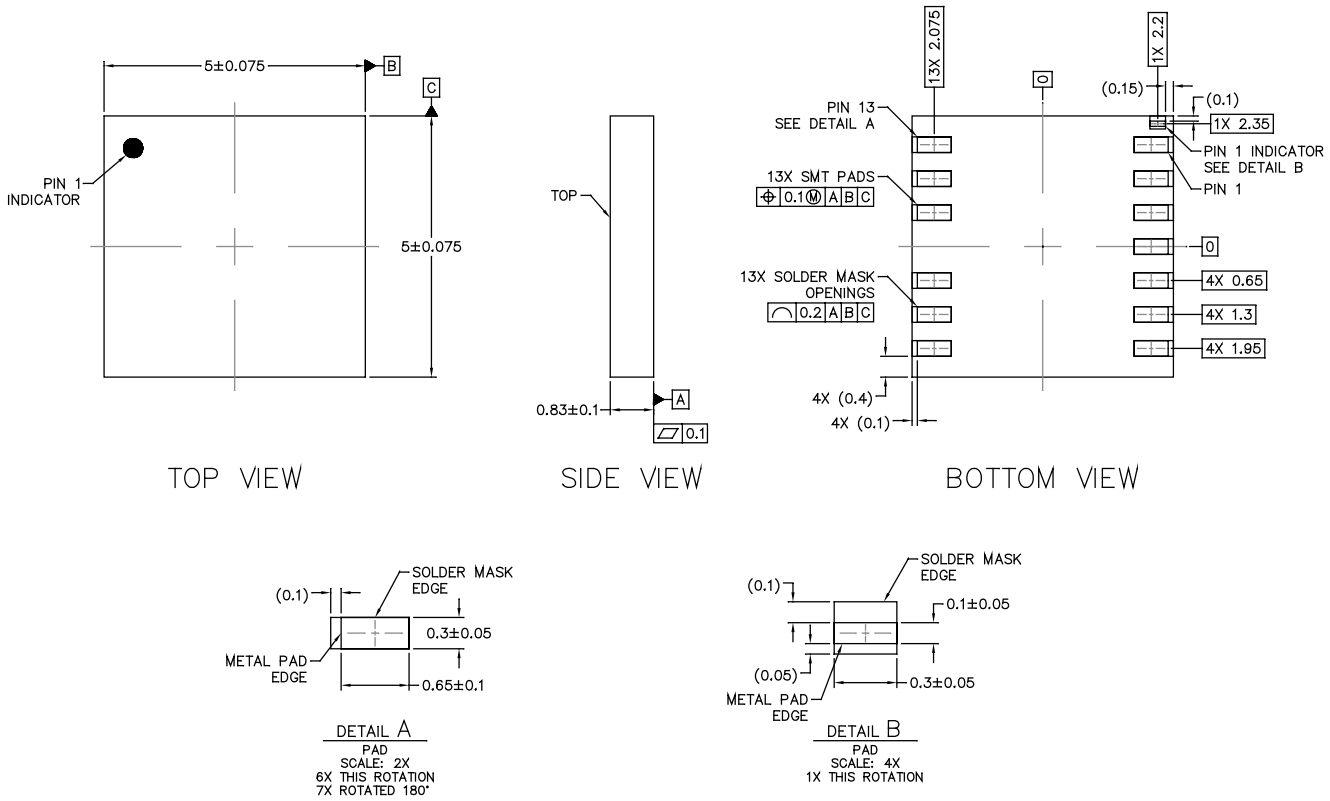


Figure 33. Si827x LGA-13 Outline

6. Land Patterns

6.1. Land Pattern: 16-Pin Narrow Body SOIC

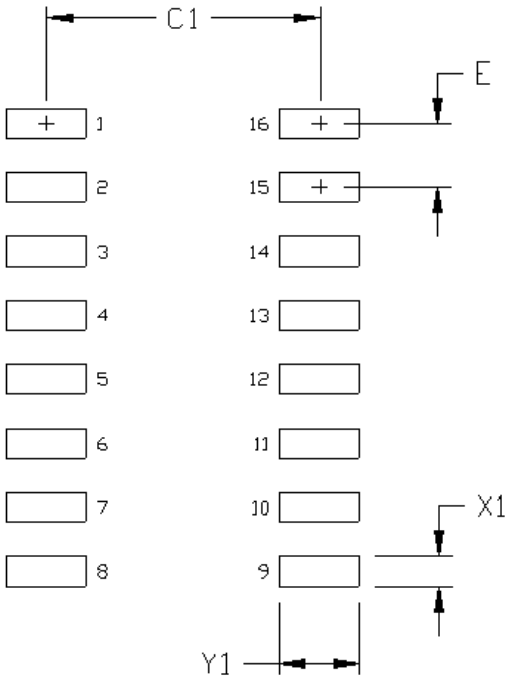


Figure 34. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 18. 16-Pin Narrow Body SOIC Land Pattern Dimensions[1,2]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.2. Land Pattern: 8-Pin Narrow Body SOIC

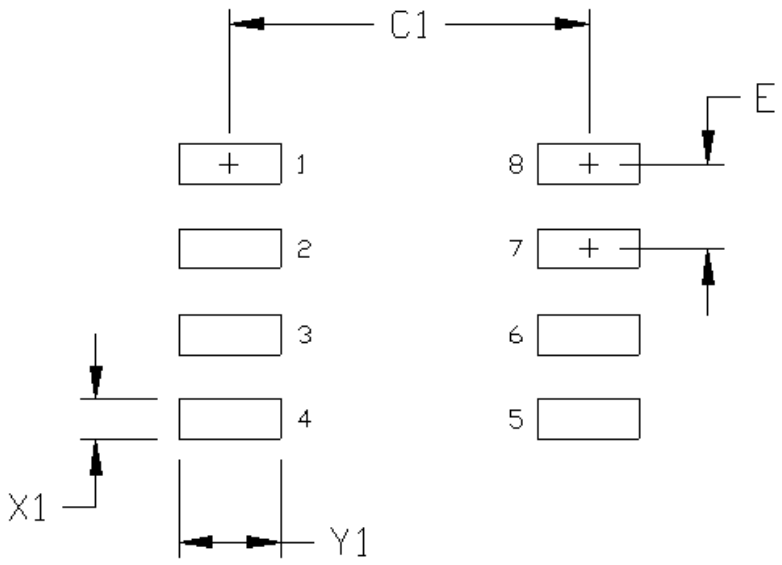


Figure 35. 8-Pin Narrow Body SOIC Land Pattern

Table 19. 8-Pin Narrow Body SOIC Land Pattern Dimensions[1,2]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.3. Land Pattern: LGA-13

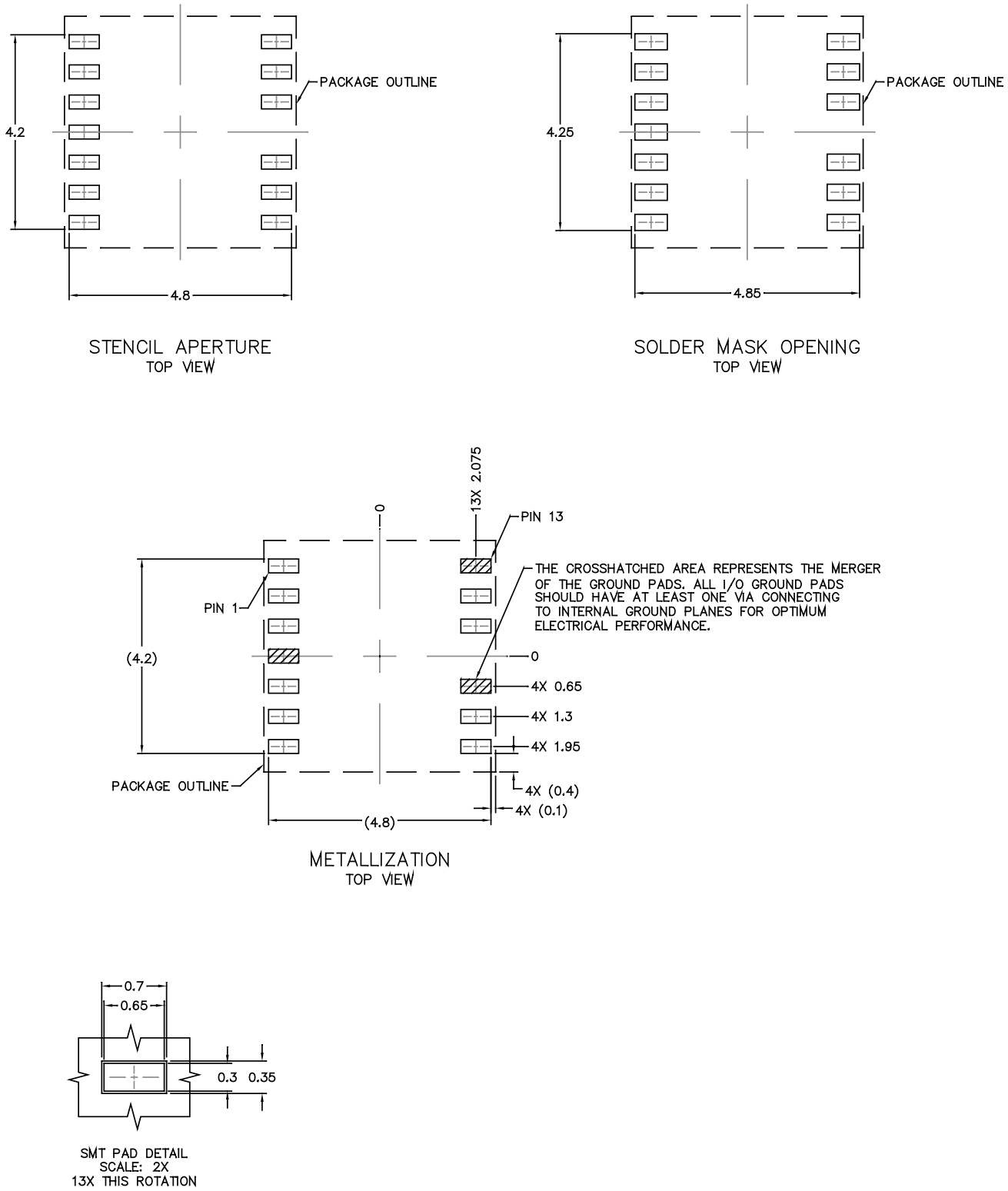


Figure 36. LGA-13 Land Pattern

7. Top Markings

7.1. Si827x Top Marking (16-Pin Narrow Body SOIC)

Figure 37. Si827x Top Marking (16-Pin Narrow Body SOIC)

Table 20. Top Marking Explanation (16-Pin Narrow Body SOIC)[1]

Line 1 Marking:	Base Part Number Ordering Options See 8. "Ordering Guide" for more information.	Si827 = ISOdriver product series Y = Configuration 3 = High-side/Low-side (HS/LS) 4 = PWM HS/LS 5 = Dual driver U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating B = 2.5 kV W = Dead-time setting range none = not included 1= 10–200 ns 4 = 20–700 ns X = Integrated deglitch circuit none = not included D = integrated
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form. The Manufacturing Code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate Automotive-Grade.

1. Characters W and/or X are optional and may be missing from the marking line. When missing, the remaining characters are right-justified on the marking line.

7.2. Si8271 Top Marking (8-Pin Narrow Body SOIC)

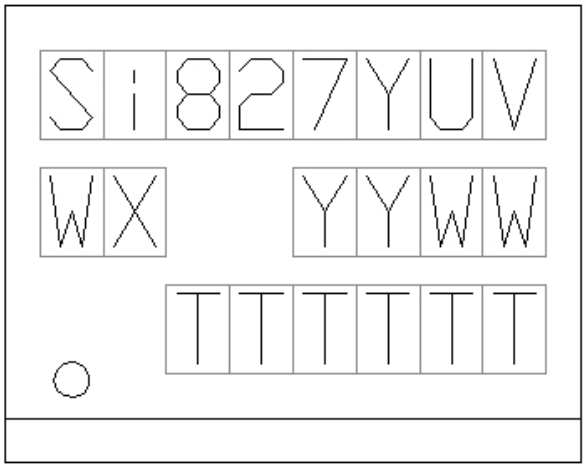


Figure 38. Si8271 Top Marking (8-Pin Narrow Body SOIC)

Table 21. Top Marking Explanation (Narrow Body SOIC)[1]

Line 1 Marking:	Customer Part Number	Si827 = ISOdriver product series Y = Configuration 1 = Single driver U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating A = 1 kV_{RMS} B = 2.5 kV_{RMS}
Line 2 Marking:	WX = Ordering options	W = Dead-time setting range none = not included 1= 10–200 ns 4 = 20–700 ns X = Integrated deglitch circuit none = not included D = integrated
	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form. The Manufacturing Code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate Automotive-Grade.

1. Characters W and/or X are optional and may be missing from the marking line. When missing, the remaining characters are right-justified on the marking line.

7.3. Si827x Top Marking (LGA-13)

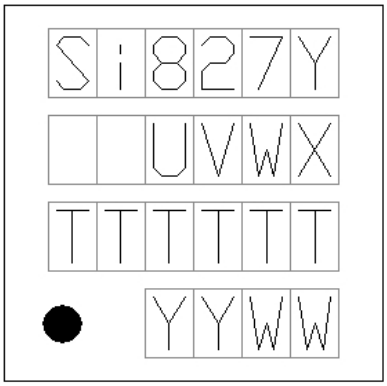


Figure 39. Si827x Top Marking (LGA-13)

Table 22. Top Marking Explanation (LGA-13)[1]

Line 1 Marking:	Base Part Number Ordering Options See 8. "Ordering Guide" for more information.	Si827 = ISOdriver product series Y = configuration 3 = High-side/Low-side (HS/LS) 4 = PWM HS/LS 5 = Dual driver
Line 2 Marking:	Ordering options	U = UVLO level G = 3 V A = 5 V B = 8 V D = 12 V V = Isolation rating A = 1 kV_{RMS} B = 2.5 kV_{RMS} W = Dead-time setting range none = not included 1= 10–200 ns 4 = 20–700 ns X = Integrated deglitch circuit none = not included D = integrated
Line 3 Marking:	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form. The Manufacturing Code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate Automotive-Grade.
Line 4 Marking:	Circle = 1.5 mm diameter YYWW	Pin 1 identifier. Manufacturing date code.

1. Characters W and/or X are optional and may be missing from the marking line. When missing, the remaining characters are right-justified on the marking line.

8. Ordering Guide

8.1. Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is employed throughout definition, design, evaluation, qualification, and mass production steps.

Table 23. Si827x Ordering Guide [1,2,3]

Ordering Part Number	Automotive OPN[4,5]	Inputs	Driver Configuration[6]	Output UVLO (V)	Integrated Deglitcher	Dead-Time Range (ns)	Low Jitter	Package	Isolation Rating
2.5 kV_{RMS} Isolation Options									
Si8271AB-IS	Si8271AB-AS	VI	Single	5	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
Si8271BB-IS	Si8271BB-AS	VI	Single	8	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
Si8271ABD-IS	Si8271ABD-AS	VI	Single	5	Y	N/A	N	SOIC-8 NB	2.5 kV_{RMS}
Si8271BBD-IS	Si8271BBD-AS	VI	Single	8	Y	N/A	N	SOIC-8 NB	2.5 kV_{RMS}
Si8271DB-IS	Si8271DB-AS	VI	Single	12	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
Si8271DBD-IS	Si8271DBD-AS	VI	Single	12	Y	N/A	N	SOIC-8 NB	2.5 kV_{RMS}
Si8271GB-IS	Si8271GB-AS	VI	Single	3	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
Si8271GB-ZS[7]	—	VI	Single	3	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
Si8271GBD-IS	Si8271GBD-AS	VI	Single	3	Y	N/A	N	SOIC-8 NB	2.5 kV_{RMS}
Si8273AB-IS1	Si8273AB-AS1	VIA/VIB	HS/LS	5	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8273ABD-IS1	Si8273ABD-AS1	VIA/VIB	HS/LS	5	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8273BB-IS1	Si8273BB-AS1	VIA/VIB	HS/LS	8	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8273BBD-IS1	Si8273BBD-AS1	VIA/VIB	HS/LS	8	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8273DB-IS1	Si8273DB-AS1	VIA/VIB	HS/LS	12	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8273DBD-IS1	Si8273DBD-AS1	VIA/VIB	HS/LS	12	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8273GB-IS1	Si8273GB-AS1	VIA/VIB	HS/LS	3	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8273GBD-IS1	Si8273GBD-AS1	VIA/VIB	HS/LS	3	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8274AB1-IS1	Si8274AB1-AS1	PWM	HS/LS	5	N	10-200	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8274AB4D-IS1	Si8274AB4D-AS1	PWM	HS/LS	5	Y	20-700	N	SOIC-16 NB	2.5 kV_{RMS}
Si8274BB1-IS1	Si8274BB1-AS1	PWM	HS/LS	8	N	10-200	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8274BB4D-IS1	Si8274BB4D-AS1	PWM	HS/LS	8	Y	20-700	N	SOIC-16 NB	2.5 kV_{RMS}

Table 23. Si827x Ordering Guide [1,2,3](Continued)

Ordering Part Number	Automotive OPN[4,5]	Inputs	Driver Configuration[6]	Output UVLO (V)	Integrated Deglitcher	Dead-Time Range (ns)	Low Jitter	Package	Isolation Rating
Si8274DB1-IS1	Si8274DB1-AS1	PWM	HS/LS	12	N	10-200	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8274DB4D-IS1	Si8274DB4D-AS1	PWM	HS/LS	12	Y	20-700	N	SOIC-16 NB	2.5 kV_{RMS}
Si8274GB1-IS1	Si8274GB1-AS1	PWM	HS/LS	3	N	10-200	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8274GB4D-IS1	Si8274GB4D-AS1	PWM	HS/LS	3	Y	20-700	N	SOIC-16 NB	2.5 kV_{RMS}
Si8275AB-IS1	Si8275AB-AS1	VIA/VIB	Dual	5	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8275ABD-IS1	Si8275ABD-AS1	VIA/VIB	Dual	5	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8275BB-IS1	Si8275BB-AS1	VIA/VIB	Dual	8	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8275BBD-IS1	Si8275BBD-AS1	VIA/VIB	Dual	8	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8275DB-IS1	Si8275DB-AS1	VIA/VIB	Dual	12	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8275DBD-IS1	Si8275DBD-AS1	VIA/VIB	Dual	12	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8275GB-IS1	Si8275GB-AS1	VIA/VIB	Dual	3	N	N/A	Y	SOIC-16 NB	2.5 kV_{RMS}
Si8275GBD-IS1	Si8275GBD-AS1	VIA/VIB	Dual	3	Y	N/A	N	SOIC-16 NB	2.5 kV_{RMS}
Si8273AB-IM3	Si8273AB-AM3	VIA/VIB	HS/LS	5	N	N/A	Y	LGA-13	2.5 kV_{RMS}
Si8273ABD-IM3	Si8273ABD-AM3	VIA/VIB	HS/LS	5	Y	N/A	N	LGA-13	2.5 kV_{RMS}
Si8273GB-IM3	Si8273GB-AM3	VIA/VIB	HS/LS	3	N	N/A	Y	LGA-13	2.5 kV_{RMS}
Si8274AB1-IM3	Si8274AB1-AM3	PWM	HS/LS	5	N	10-200	Y	LGA-13	2.5 kV_{RMS}
Si8274AB4D-IM3	Si8274AB4D-AM3	PWM	HS/LS	5	Y	20-700	N	LGA-13	2.5 kV_{RMS}
Si8274GB1-IM3	Si8274GB1-AM3	PWM	HS/LS	3	N	10-200	Y	LGA-13	2.5 kV_{RMS}
Si8274GB4D-IM3	Si8274GB4D-AM3	PWM	HS/LS	3	Y	20-700	N	LGA-13	2.5 kV_{RMS}
Si8275AB-IM3	Si8275AB-AM3	VIA/VIB	Dual	5	N	N/A	Y	LGA-13	2.5 kV_{RMS}
Si8275ABD-IM3	Si8275ABD-AM3	VIA/VIB	Dual	5	Y	N/A	N	LGA-13	2.5 kV_{RMS}
Si8275BB-IM3	Si8275BB-AM3	VIA/VIB	Dual	8	N	N/A	Y	LGA-13	2.5 kV_{RMS}
Si8275BBD-IM3	Si8275BBD-AM3	VIA/VIB	Dual	8	Y	N/A	N	LGA-13	2.5 kV_{RMS}
Si8275DBD-IM3	Si8275DBD-AM3	VIA/VIB	Dual	12	Y	N/A	N	LGA-13	2.5 kV_{RMS}
Si8275GB-IM3	Si8275GB-AM3	VIA/VIB	Dual	3	N	N/A	Y	LGA-13	2.5 kV_{RMS}
Si8275GBD-IM3	Si8275GBD-AM3	VIA/VIB	Dual	3	Y	N/A	N	LGA-13	2.5 kV_{RMS}
1 kV_{RMS} Isolation Options									
Si8271GA-IS	Si8271GA-AS	VI	Single	3	N	N/A	Y	SOIC-8 NB	1 kV_{RMS}
Si8271GAD-IS	Si8271GAD-AS	VI	Single	3	Y	N/A	N	SOIC-8 NB	1 kV_{RMS}

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the Ordering Part Number indicates tape and reel option.
4. Automotive-Grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial- Grade (with an “-I” suffix) version counterpart. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
5. In Top Markings, the Manufacturing Code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate Automotive-Grade.
6. All HS/LS drivers have built-in overlap protection while the single and dual drivers do not.
7. “-ZS” OPNs indicate an operating ambient temperature rating of –55 °C to +125 °C. 100% tested for UVLO, input and output hysteresis, source and sink current at min and max VDD conditions of 3.3 V (VDDI) and 5 V (VDD).

9. Revision History

Revision	Date	Description
C	November, 2025	• Updated Table 13. "IEC60747-17 Insulation Characteristics" per certification. • Updated order of data sheet elements.
B	April, 2025	• Replaced package option “IM1” with “IM3” in Ordering Guide. • Added “-ZS” suffix OPN information for –55 to +125 °C temperature ratings. • Replaced references to IM1 with IM3 throughout the document. • Replaced package outline and land pattern drawings and dimensions with IM3 details.
A	July, 2022	Added Agile data sheet revision in footer.
1.06	April, 2021	• Added automotive-grade ordering part numbers to Ordering Guide.
1.05	September, 2020	• Added Si8271GB-AS to Ordering Guide.
1.04	May, 2020	• Adjusted industrial Ordering Guide to group by isolation rating. • Added 8 new OPNs rated at 1 kV_{RMS} to the Table 1.1 on page 2. • Added Si8273GB-IM1 to Table 1.1 on page 2. • Added footnotes section to Table 1.1 on page 2 and appropriate footnotes. • Removed duplicate Si8273BB-IS1 line in the Table 1.1 on page 2. • The QFN package was renamed to DFN throughout the document and pin count naming was unified with SOIC packages. • Updated and unified style and naming conventions throughout the document. • Edited CQC basic working voltage rating from 600 V to 250 V and removed the reinforced working voltage rating in Table 4.2 on page 25. • Edited Table 4.8 on page 30 and clarified negative transient tolerance specification. • Edited the Top Marking Explanation tables in 8. Top Markings and added a footnote clarifying how optional characters are represented. • Removed “component notice 5A” from CSA certification descriptions in Table 4.2 on page 25. • Added “-2011” to CQC certification descriptions in Table 4.2 on page 25. • Corrected Dead-Time Adjustable Range on Si8274DB1-AS1 to 10-100 ns in Table 1.1 on page 2. • Updated diagrams in 2. System Overview to improve readability. • Updated application diagrams in 3. Applications to improve readability and to follow updated naming conventions. • Corrected IC Junction-to-Air Thermal Resistance (θ_{JA}) specifications for all packages in Table 4.7 on page 28. • Clarified Figure 4.1 on page 24, Figure 4.2 on page 24, and Figure 4.3 on page 25. • Updated thermal derating curves, power dissipation example, and safety input current specifications and test conditions for all packages based on new Ã˜JA specifications. • Added a new thermal derating curve for the DFN-14 package (Figure 4.6 on page 29) based on the new θ_{JA} specification. • Clarified, reorganized, and updated the 2.4 Power Dissipation Considerations section. • Figure 6.3 on page 38 and Table 6.3 on page 38 were edited and clarified. • Footnote 3 was removed from Table 6.3 on page 38. • Removed the single driver option from Line 1 Marking row in Table 8.3 on page 44 • Reorganized and clarified 2.7 Overlap Protection and Programmable Dead Time • Clarified conditions for typical specifications in Table 4.1 Electrical Characteristics on page 21.
1.03	October, 2019	• Added Si8275BB-AS1 and Si8275GB-AS1 to Ordering Guide for Automotive Grade OPNs.
1.02	June, 2019	• Updated Table 1.1 Si827x Ordering Guide1, 2, 3 on page 2.
1.01	April, 2019	• Added Si8271AB-AS and Si8274BB4D-AS1 to Ordering Guide for Automotive Grade OPNs.
1.0	May, 2018	• Replaced references and descriptions of LGA package with QFN package throughout the data sheet. • Updated OPNs with LGA package denoted by “-IM” suffix to QFN packages denoted by “-IM1” suffix in the Ordering Guide. • Added Si8274DB1-AS1 OPN to Ordering Guide for Automotive Grade OPNs. • Added Note 6 to Ordering Guide for Automotive Grade OPNs referring to top markings for Automotive Grade parts. • Updated Equation 3 and the chart generated by Equation 3 in Figure 2.17 Max Load vs. Switching Frequency on page 15. • Corrected power dissipation example calculations in Power Dissipation Considerations. • Updated Package Outline: 14 LD QFN with new QFN package outline drawing and updated Table 6.3 Package Diagram Dimensions with QFN package dimensions. • Updated Table 4.2 Regulatory Information on page 25 with certification information. • Updated Table 4.3 Insulation and Safety-Related Specifications on page 26 symbols and clarified parameters. • Added Surge Voltage specification to Table 4.5 VDE 0884 Insulation Characteristics on page 27. • Updated description of Figure 4.5 NB SOIC-16, QFN-14 Thermal Derating Curve on page 28 and Figure 4.4 NB SOIC-8 Thermal Derating Curve on page 28.

Revision	Date	Description
0.6	December, 2017	• Updated Figure 2.12. Rise/Fall Time vs. Load on page 10. • Updated Table 4.1. Electrical Characteristics on page 21. - Added "(no load)" under IDDx specification test condition. - Added t_{SD} and $t_{RESTART}$ specs. • Corrected storage temp and power dissipation for SOIC-8 package in Table 4.6. IEC Safety Limiting Values on page 27. • Added footnote about VO+ and VOA/VOB voltages with respect to ground in Table 4.8. Absolute Maximum Ratings on page 30 with improvement from other pins. • Added new table to Ordering Guide for Automotive-Grade OPN options.
0.5	February, 2016	Initial release.