VSC8228-01

Dual Signal Conditional and Retimer

Datasheet

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Revision 4.1
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Confidential

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.1

Revision 4.1 of this datasheet was published in January 2009. In revision 4.1 of the document, information about controlling modes of operation was added. When controlling modes of operation, it is necessary to power up the VSC8228-01 device in pin programming mode, then to switch to either SPI mode or two-wire serial mode as desired. For more information about the switching procedure, see "Controlling the PIO[6:0] and Multiplexer Mode Settings," page 15.

Revision 4.0

Revision 4.0 of this datasheet was published in January 2007. This was the first production-level publication of the document.

1 Product Overview

1.1 General Description

The VSC8228-01 device is a dual repeater or retimer for Fibre Channel, gigabit Ethernet, and Infiniband applications. The VSC8228-01 contains dual FibreTimer clock recovery units (CRU) for bidirectional signal conditioning in system interconnect and serial backplane applications. The device supports rates from 125 Mbps up to 4.25 Gbps. Using a single reference clock for acquisition, the VSC8228-01 retransmits the incoming serial data synchronously to the reference clock in retimer mode or to the incoming data in repeater mode. In retimer mode, add and drop elasticity buffers insert or delete Fibre Channel fill words to compensate for timing differences between the incoming data and the local reference clock.

An analog signal detect function is integrated into both channels. In the retimer and repeater modes, the device monitors the incoming data for run-length violations and K28.5– symbols. The inputs on both the transmit and receive channels can be looped back to the outputs of the opposite channels for diagnostic purposes. The device provides a built-in pattern generator and checker. The receive channel output includes an optional half-rate clock for SGMII applications.

A high degree of signal integrity is maintained by differential I/O, on-chip input and output terminations, input equalization, and output de-emphasis. The programmable input equalization circuit compensates for long printed circuit board (PCB) traces, backplanes, connectors, and cables. Equalization, de-emphasis, output drive levels, data rate, and other features are configured through industry standard serial interfaces (two-wire or SPI).

The device's core and high-speed I/O can be powered from a single 1.2-V power supply, single 1.8-V power supply, or both 1.2-V and 1.8-V power supply. The 1.8-V power supply is required to meet the LVPECL output swing levels. For compatibility with legacy controllers and ASICs, the TTL control and status I/O can be powered with a 1.2-V, 1.8-V, 2.5-V, or 3.3-V power supply. The device has current-mode logic (CML) inputs and outputs that can be AC-coupled for LVPECL and LVDS compatibility. Typical power dissipation for a 1.2-V supply is 360 mW.

1.2 Features

The features for the VSC8228-01 device are:

- Dual clock and data recovery architecture for gigabit Ethernet and Fibre Channel applications
- FibreTimer™ configurable clock recovery unit (CRU): repeater, retimer, or bypassed
- Programmable input signal equalization, output de-emphasis, and output drive levels
- Analog signal detect and protocol monitor indicators
- SPI or two-wire serial interface
- Optional half-rate SGMII clock and repeated reference clock output

- Single 1.2-V power supply, single 1.8-V power supply, or both 1.2-V and 1.8-V power supplies
- 10 mm × 10 mm, 64-pin TQFP package
- 360-mW typical power dissipation
- –10 °C ambient to 105 °C case temperature

1.3 Applications

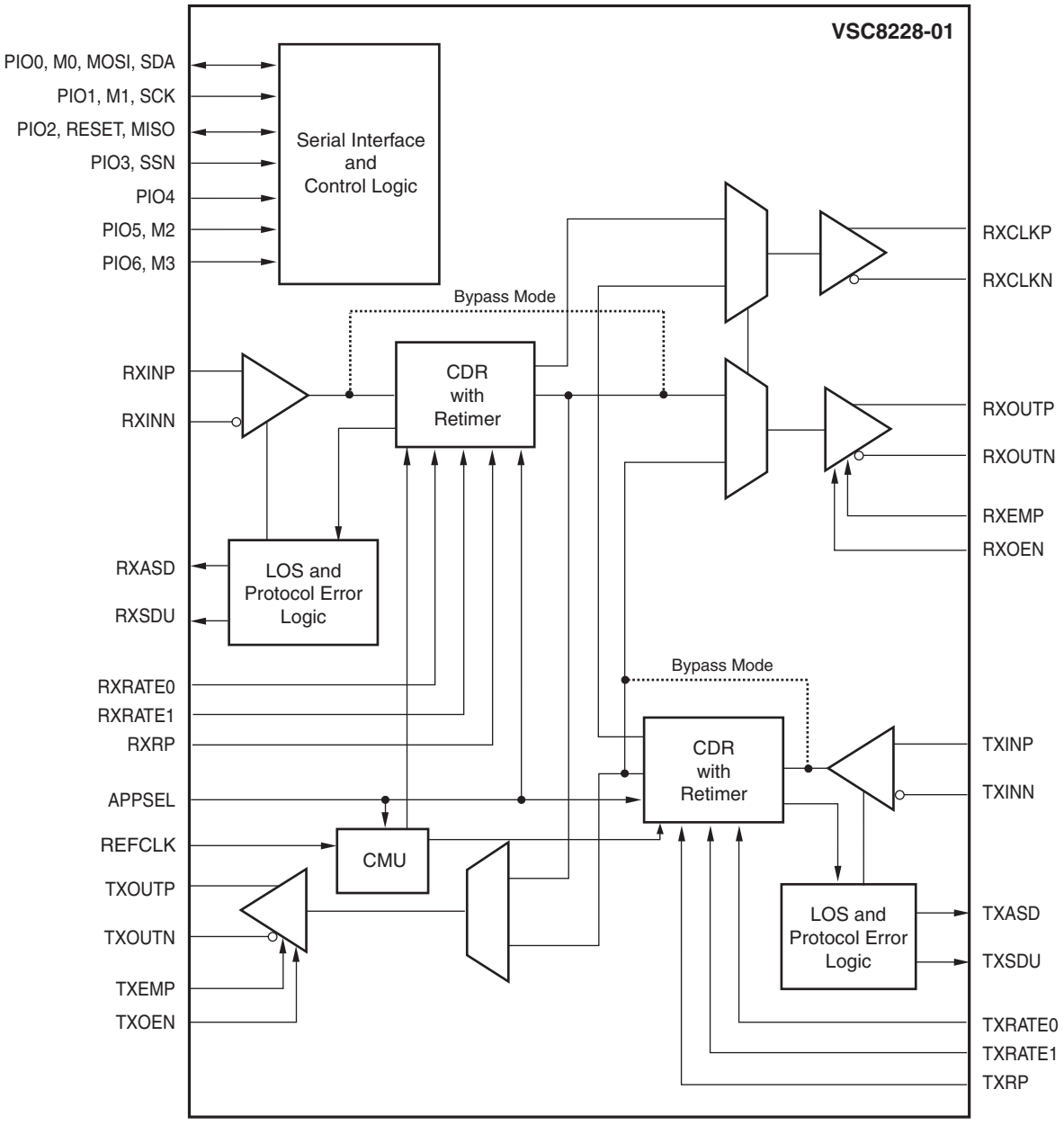
Some of the applications for the VSC8228-01 device are:

- Ethernet: 125 Mbps and 1.25 Gbps
- Fibre Channel: 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps
- In both retimer mode and repeater mode, the CRU also covers the following speeds: 155.52 Mbps, 622.08 Mbps, and 2488.32 Mbps
- Infiniband™: 2.5 Gbps
- ESCON/SBCON: 200 Mbps
- Fibre Channel switches, disk arrays, RAID subsystems, and host bus adapters
- iSCSI SAN host bus adapters and switches
- SFP/SFP signal clean-up
- Serial backplane

1.4 Block Diagram

The block diagram for the VSC8228-01 device is shown in the following figure.

Figure 1. Block Diagram



2 Functional Descriptions

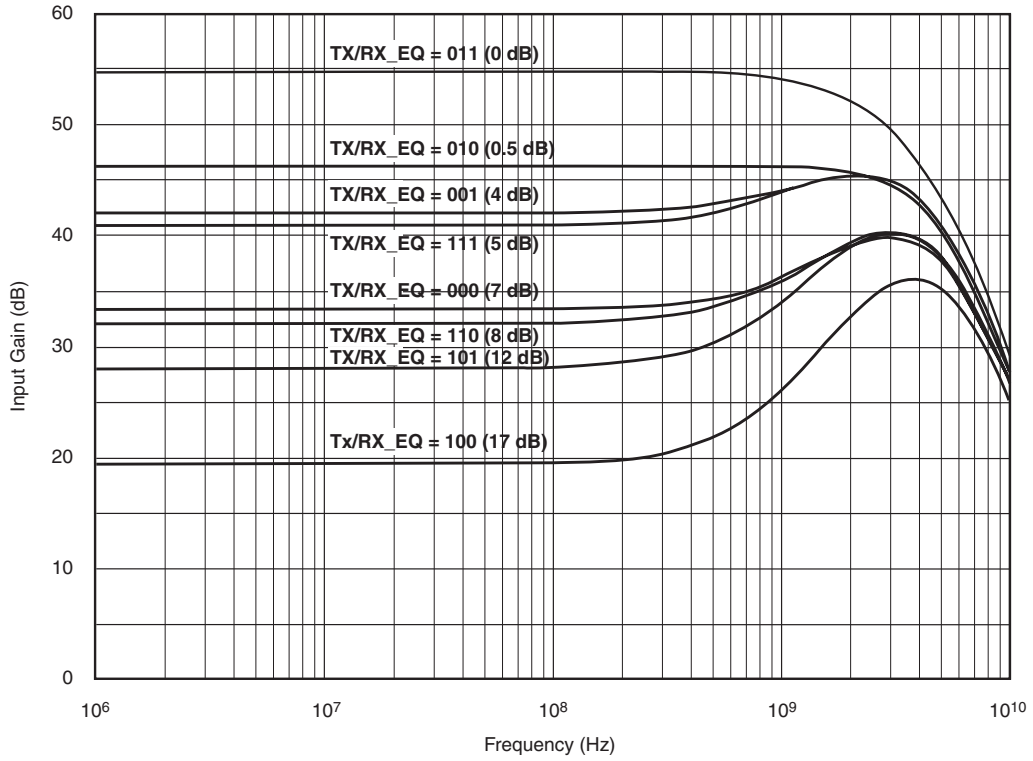
The VSC8228-01 device is divided into four main sections: receive channel (Rx), transmit channel (Tx), pattern generator and checker, and serial interface port. Both the Rx and Tx channels are identical except the Rx channel has an optional half-rate clock for SGMII applications. Both channels contain an input buffer, FibreTimer clock recovery unit (CRU), provisions for loopback, and programmable output drivers. Each channel is controlled independently with separate control and status I/O.

2.1 Input Buffers

2.1.1 Equalization and Termination

Each high-speed differential input contains an eight-level equalization circuit that attenuates low-frequency signals to compensate for the high-frequency loss that is characteristic of copper cables and traces. The amount of cable equalization can be programmed for each channel for optimal signal quality. The three TX/RX_EQ[2:0] bits of the RXIN_CTRL and TXIN_CTRL registers select one of eight values of equalization. The following graph shows the simulated correlation between input buffer gain and the setting of TX/RX_EQ[2:0].

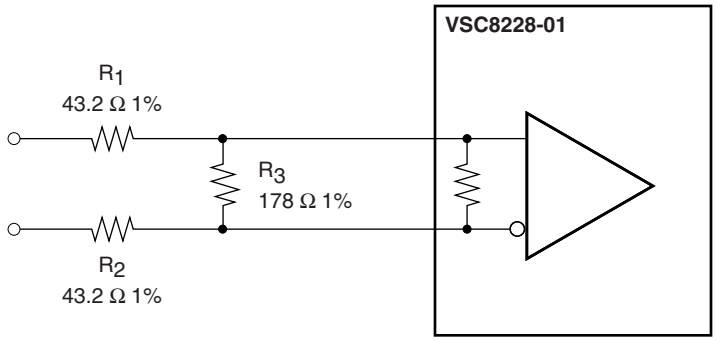
Figure 2. Input Gain, Frequency, and Equalization Settings Comparison



As trace lengths increase, high-frequency attenuation causes deterministic jitter, or Inter-Symbol Interference (ISI), which increases jitter. Low-frequency components of the signal remain relatively unattenuated, so low-frequency gain is not as important. The VSC8228-01 equalization circuit reduces low-frequency gain, but increases the ratio of high-frequency gain relative to low-frequency gain to reduce the affects of ISI.

The current industry standards for 4.25-Gbps drives include support for only 100-Ω media. For applications requiring 150-Ω differential impedances, external resistors must be added to match the 150-Ω impedance of the media to the 100-Ω impedance of the VSC8228-01. The following figure shows an example of a simple external circuit that provides this impedance matching function. The impedance looking into the VSC8228-01 is ~150 Ω. The impedance looking out of the VSC8228-01 is ~100 Ω.

Figure 3. Accommodating 150-Ω Applications



Position the external resistors as closely as possible to the VSC8228-01 device. Because this circuit attenuates the signal by approximately 3.95 dB (~64.3% of output swing), it is necessary to ensure the output signal of the VSC8228-01 has adequate amplitude so that the differential swing meets the minimum output swing specification.

2.1.2 Analog Signal Detect

Integrated into the input receivers are independent programmable Analog Signal Detect (ASD) circuits that monitor peak-to-peak signal amplitude as well as signal transitions. The signal is compared to one of four programmable levels. The default value is 100 mV. For more information about the programmable levels, see Table 1, page 14.

If the signal amplitude is below the programmed level or if there are less than 32 transitions within a period of approximately 700 ns, the signal is considered invalid. In the absence of a valid input signal, the condition is flagged by setting the respective ASD pin LOW and the ASD register bit to 0 (RXASD for the Rx Channel or TXASD for the Tx Channel). The device can be configured to squelch the data on a per-channel basis when the data is invalid.

The ASD pin sets itself automatically provided that the input signal is greater than the programmed analog threshold and that there are at least 32 transitions within a

700-ns period. The minimum pulse width of the ASD signal is 700 ns. The invalid signal bit (RXASDERR or TXASDERR) is only cleared after a read to that register.

Table 1. Receiver Loss of Signal Detect Threshold Values

	Loss of Signal Threshold Values			
RX/TX_LTH[1:0]	**Low**	**Undefined**	**High**	**Unit**
00	<71	71 - 166	>166	mV
01	<116	116 - 200	>200	mV
10	<168	168 - 266	>266	mV
11	<177	177 - 298	>298	mV

2.2 FibreTimer Clock Recovery Units (CRU)

The FibreTimer clock recovery units (CRU) can recover data, and repeat or retime the data. A 100 nF external loop filter capacitor must be connected from pin CMU_FILT to GND. The device requires a single reference clock (REFCLK) for signal acquisition and lock. Table 5, page 19 describes the supported data rates, reference clock requirements for those rates, and internal register settings for each rate. The REFCLK input need not be phase-locked to the incoming data but must have a frequency within 200 ppm of the divided down recovered data PLL frequency.

Because a single REFCLK is used for both Rx and Tx data, the Rx and Tx recovered frequencies can differ by as much as 200 ppm. The device accepts single-ended or differential reference clock inputs that are LVPECL-, LVTTL-, or HSTL-compatible and meet the requirements listed in Table 52, page 59.

2.2.1 Repeater Mode

The term repeater is used for a CDR function where the recovered serial data is retransmitted synchronously to the recovered clock. Unlike standard PLL-based CDRs, this circuit is all digital, resulting in good jitter tolerance, excellent jitter transfer, and low latency in a circuit that performs identically across process, voltage, and temperature.

In repeater mode, serial data enters the CDR where the clock is extracted from the data and the data is resynchronized to the recovered clock. The resynchronized output of the CDR contains serial data with improved signal quality due to amplification of the signal and attenuation of input jitter. In repeater mode, not all of the jitter at the input is eliminated from the recovered data. However, any jitter that passes through the repeater is low-frequency and therefore is benign to downstream devices.

Repeater mode for the receiver and transmitter channel is selected using either the serial interface or by setting the RXRP or TXRP pin HIGH for their respective channels. When RXRP or TXRP are LOW, the retimer mode is selected. In both the repeater and retimer modes, the data is checked for Run Length Limit (RLL) violations and K28.5 violations. The RXSDU and TXSDU outputs can be programmed to indicate the various violations.

2.2.2 Retimer Mode

The term retimer is used for a CDR that retransmits the recovered serial data synchronously to the locally generated internal bit clock. This complex CDR function eliminates jitter transfer at the expense of latency. Due to the potential mismatch between the bit rate of the incoming data and the local reference clock (±200 ppm), an add or drop elasticity buffer is needed to insert or delete special Fibre Channel ordered sets, called fill words, to accommodate this rate difference. The rules for adding and dropping fill words are delineated in documents generated by the T11 committee. By eliminating jitter transfer, compliance to signal quality standards is ensured.

In Retimer mode, serial data enters the CDR where the clock is extracted from the data and the data is resynchronized to the recovered clock. This data is then input to a 5-word deep add and drop FIFO. Data is removed from the FIFO and retransmitted from the CDR synchronously to the CMU's bit rate clock derived from REFCLK. Because the retransmitted data is synchronized with the bit clock and not the recovered clock, jitter does not pass through the retimer. The output of the retimer is compliant with all Fibre Channel signal quality specifications.

Retimer mode is most useful when the output of the CDR is exiting a system that must meet the Fibre Channel signal quality standards. Because the latency of the retimer is quite high, repeaters are preferable in situations where full Fibre Channel jitter compliance is not required.

Retimer mode for the receiver and transmitter channel is selected using either the serial interface or by setting the RXRP or TXRP pin LOW for their respective channels. When Rxrp or TXRP are HIGH, the Repeater mode is selected. In both the Repeater and Retimer modes, the data is checked for run length limit (RLL) violations and K28.5 violations. The RXSDU and TXSDU outputs can be programmed to indicate the various violations.

2.2.3 Bypass Mode

For system debugging, a bypass mode is provided where the CDR can be bypassed. Using bypassing mode means that the input buffer is directly connected to the output buffer without retiming. The de-emphasis does not work in this mode.

2.2.4 Controlling the PIO[6:0] and Multiplexer Mode Settings

The VSC8228-01 has multiple modes of operation for loopback, bypass, retiming or repeating, and pattern generation and checking. The PIOx pins provide an interface for either the serial peripheral interface (SPI), two-wire serial interface, or a pin programming mode compatible with the VSC7142 dual repeater and retimer.

Power up the VSC8228-01 device in pin programming mode (PIO4 = 1, PIO3 = 0), then switch to either two-wire serial mode or SPI mode, as follows:

- For two-wire serial mode, change the setting of the PIO3 pin to 1. The setting of the PIO4 pin remains 1.
- For SPI mode, change the setting of the PIO4 pin to 0. The setting of the PIO3 pin remains 0. After SPI mode is enabled, the PIO3 pin can be used as the (SSN) pin.

Alternatively, if the VSC8228-01 device is the only slave on the bus, power up the VSC8228-01 device in two-wire serial mode directly, and then send 11 STOP symbols from the two-wire serial master to the VSC8228-01, to put the two-wire serial engine of the device into IDLE state. At this point, normal communication resumes.

To power up the VSC8228-01 device in SPI mode directly, keep the SSN signal at low, and do not activate the SSN signal until power is stabilized.

To emulate the VSC7142 functions, set PIO4 = 1, PIO3 = 0. In this mode, the PIO6, PIO5, PIO1, and PIO0 (respectively) perform the same function as the M3, M2, M1, and M0 pins, for most settings. SPI does not support bus addressing. The SPI for each of the VSC8228-01 devices requires a separate SPI port to communicate with. The following table describes the settings for the PIO[6:0] pins.

Table 2. PIOx and Multiplexer Mode Selection

PIO6/M3	PIO5/M2	PIO4(1)	PIO3(1)	PIO2	PIO1/M1	PIO0/M0	Function/Mode
X	X	0	SSN	MISO	SCK	MOSI	SPI(2)
A2	A1	1	1	A0	SCK	SDA	Two-wire serial interface
M3	M2	1	0	RESET	M1	M0	Pin programming mode

1. When changing from pin programming mode to SPI or two-wire serial interface modes, PIO3 and PIO4 must be set to at least 500 ns before attempting to communicate by using serial interfaces.
2. SPI does not support bus addressing.

The following table provides the pin programming mode selection.

Table 3. Pin Programming Mode Selection

#	Operation Mode	PIO6 /M3	PIO5 /M2	PIO2	PIO1 /M1	PIO0 /M0	RxOut(1)	TxOut(1)	Checker Input(2)	VSC7142 Equivalent Setting
0	Receiver bypass	0	0	Reset	0	0	RxIn Byp	TxIn		Invalid
1	line-side generator and checker (3)	0	0	Reset	0	1		PG(4)	RxIn	Invalid
2	Bypass	0	0	Reset	1	0	RxIn Byp	TxIn Byp		Removed
3	Test mode (Rx)	0	0	Reset	1	1				Removed
4	Test mode (Tx)	0	1	Reset	0	0				Invalid
5	Line broadcast(5)	0	1	Reset	0	1	RxIn	RxIn		Same
6	Transmitter loopback bypass	0	1	Reset	1	0	TxIn	TxIn Byp		Same
7	Transmitter bypass	0	1	Reset	1	1	RxIn	TxIn Byp		Same
8	Split loopback, RxCLK on	1	0	Reset	0	0	TxIn	TxIn		Invalid
9	Normal, RxCLK on	1	0	Reset	0	1	RxIn	TxIn		Invalid
10	Receiver loopback bypass	1	0	Reset	1	0	RxIn Byp	RxIn		Removed
11	Host broadcast(5)	1	0	Reset	1	1	TxIn	TxIn		Same

Table 3. Pin Programming Mode Selection *(continued)*

#	Operation Mode	PIO6 /M3	PIO5 /M2	PIO2	PIO1 /M1	PIO0 /M0	RxOut(1)	TxOut(1)	Checker Input(2)	VSC7142 Equivalent Setting
12	Host-side generator and checker(6)	1	1	Reset	0	0	PG		TxIn	Invalid
13	Split loopback	1	1	Reset	0	1	TxIn	RxIn		Invalid: transmitter retimed twice
14	Internal generator and checker	1	1	Reset	1	0			PG	Invalid: transmitter retimed twice
15	Normal	1	1	Reset	1	1	RxIn	TxIn		Same

1. Indicates the source of the data for that output.
2. Indicates the source of the data for the pattern checker.
3. In line-side generator and checker mode, TX_FIFO_CTRL must be set to 20'h.
4. PG indicates pattern generator.
5. In line broadcast and host broadcast modes, the Rx and Tx channels must be configured so that both Rx and Tx are both in the repeater mode. If one channel is in repeater mode and the other in retimer mode, the data will be corrupted.
6. In Host-side generator and checker mode, RX_FIFO_CTRL must be set to 20'h.

2.2.5 Considerations for Non-Fibre Channel Applications

The FibreTimer blocks of the VSC8228-01 are designed for use in Fibre Channel systems. The add or drop entities required for speed matching are not compatible with gigabit Ethernet, SONET/SDH, or other applications. If the VSC8228-01 is used in non-Fibre Channel applications, it must be configured for repeater or bypass mode.

2.2.6 Fibre Channel Protocol Detection

In the retimer and repeater mode, the incoming data is examined for run-length violations and K28.5– symbols. These signals can be optionally combined with RXASDERR or TXASDERR to confirm if there is incoming data and if it is valid Fibre Channel data.

The SDUSEL pin selects one of two different modes: single-window (LOW) or multiple-window (HIGH) error mode. When controlled by the serial interface, the RXSDUSEL and TXSDUSEL bits control this mode when enabled by setting RXSDUSEL_SRC or TXSDUSEL_SRC HIGH.

By default, single-window detection is enabled. Single-window error mode allows the user to develop their own algorithm for monitoring data and enabling control of the multiplexor mode settings. In multiple-window error mode, RXSDU or TXSDU is asserted LOW after four consecutive 32,768-bit windows containing ASD, RLL, or K28.5– errors. RXSDU or TXSDU remains asserted until four consecutive 32,768-bit windows occur error free.

2.2.7 Run-Length Limit (RLL) Detection

The retimer run-length limit (RLL) detection scheme uses 32,768-bit windows. If a run of six or more consecutive zeros or a run of six or more consecutive ones begins in the 32,768-bit window, that window is considered to have an RLL error. Otherwise, that window is considered to be RLL-clean. For a run-length limit error, the RXRLLERR or TXRLLERR bit is set HIGH. This bit is only cleared after a read to that register.

2.2.8 K28.5– Detection

The K28.5– character detection uses 32,768-bit windows. If at least one K28.5– character begins in the 32,768-bit window, that window is considered to have a K28.5– character within it. Otherwise, K28.5– characters are considered to be absent and in error.

In normal Fibre Channel traffic, an interframe gap with a minimum of two idle characters containing two K28.5– characters occurs every 21,000 bits. Therefore, in normal traffic, the detection scheme always declares the detection of K28.5– characters. For a K28.5– error, the RXK28ERR or TXK28ERR bit is set HIGH. This bit is only cleared after a read from the RXK28ERR or TXK28ERR register.

2.2.9 Protocol Error Signaling

The VSC8228-01 provides a programmable output signal that indicates protocol errors in the retimer and repeater modes. The RXSDU, TXSDU, RXASD, and TXASD signals can be programmed to indicate loss of signal, RLL violations, or K28.5 violations. The user selects which errors to monitor. If any of these errors occur, the respective RXSDU, TXSDU, RXASD, or TXASD output is set LOW.

By default, all of the following signals must indicate normal operation for RXSDU and TXSDU to be set HIGH: transition detector, peak-to-peak amplitude monitor, run-length limit detector, and K28.5– monitor. By default, the RXASD and TXASD signals are set HIGH when the transition detector and peak-to-peak amplitude monitor indicate normal operation.

2.2.10 Reference Clock

The VSC8228-01 derives all internal clock signals from an external reference clock on the REFCLKP/REFCLKN input pins. These inputs support a variety of oscillator output configurations as identified in Table 4, page 18. For optimized signal quality and minimal jitter, a differential AC-coupled LVPECL oscillator is recommended. Differential LVPECL and HSTL reference clocks require a 100-Ω external termination across the REFCLKP/REFCLKN inputs. Single-ended LVPECL and HSTL reference clocks require a 50-Ω external termination to ground.

Table 4. Reference Clock Configuration Support

Reference Clock Type	DC-Coupled		AC-Coupled	
	Single-Ended(1)	Differential	Single-Ended(1)	Differential
HSTL	Yes(2)	Yes	Yes	Yes
LVTTL	Yes(3)	No	NA	NA

Table 4. Reference Clock Configuration Support *(continued)*

Reference Clock Type	DC-Coupled		AC-Coupled	
	Single-Ended[1]	Differential	Single-Ended[1]	Differential
LVPECL[4]	See note[5]	See note[5]	Yes	Yes

1. For the unused REFCLKN, a 0.1 µF capacitor to ground should be added to suppress noise.
2. REFCLKP driven with REFCLKN biased from 0.68 V to 0.9 V.
3. Requires a modified V_{IL} maximum of 0.5 V.
4. A minimum swing of 250 mV single-ended or 350 mV differential is required.
5. DC-coupled operation for LVPECL REFCLK+/– is allowed only if the LVPECL driver meets the modified common-mode signal level specified in Table 16, page 51.

2.2.11 Data Rate Selection

The VSC8228-01 supports the data rates and reference clocks listed in the following table. The data rate is configured through the RXRATE0/1 and TXRATE0/1 pins or through the programming interface. The channels can be programmed independently for multiples of a given service (Fibre Channel, Ethernet). For example, if one channel is programmed for 1 Gbps Fibre Channel (1 GFC), the other can be programmed for 2 GFC or 4 GFC but not gigabit Ethernet. If one channel is set to Infiniband or PCI Express™, the other can be set to gigabit Ethernet. The default register settings for a 125-MHz reference clock are for gigabit Ethernet for both channels.

Table 5. Reference Clock Rates by Application

Application	Data Rate (Gbps)	Service Setting for Both Channels (CMU_DIV_SEL[1:0])	Rate Multiplier Setting for Each Channel (RX_DIVK/ TX_DIVK[2:0])	REFCLK Frequency (MHz)	
				RCK_SEL = 0	RCK_SEL = 1
ESCON/SBCON	0.200	01	001	125	62.5
Fast Ethernet	0.125	01	000	125	62.5
Gigabit Ethernet	1.2500	11	101	125	62.5
1× Fibre Channel	1.0625	11 10	101 101	106.25 125	53.125 62.5
2× Fibre Channel	2.1250	11 10	110 110	106.25 125	53.125 62.5
4× Fibre Channel	4.2500	11 10	111 111	106.25 125	53.125 62.5
2.5 InfiniBand or PCI Express	2.5000	11	110	125	62.5
STS-3/STM-1	0.15552	01	000	155.52	77.76
STS-12/STM-4	0.62208	01	100	155.52	77.76
STS-48/STM-16	2.48832	01	110	155.52	77.76

To provide fast rate-change response, two pins are provided to directly select the data rate. The user programs the rate multiplier for each of the four combinations for the RXRATE0/1 and TXRATE0/1 pins. When enabled, the device selects the programmed rate multiplier based on the state of the RXRATE0/1 and TXRATE0/1 pins. The pins settings for RXRATE0/1 and TXRATE0/1 are listed in the following table. Note that the Ethernet reference clock (125 MHz) can be used to support Fibre Channel, Ethernet,

and ESCON/SBCON with a single reference clock. Using the Fibre Channel reference clock setting requires a 100-MHz clock to support ESCON/SBCON.

Table 6. Hardware Control of Data Rate

TXRATE1/ RXRATE1	TXRATE0/ RXRATE0	APPSEL	REFCLK Frequency (MHz)	Application	Data Rate (Gbps)
0	0	0	106.25	1× Fibre Channel	1.0625
		0	125	Gigabit Ethernet	1.25
		1	125	1× Fibre Channel	1.0625
0	1	0	106.25	2× Fibre Channel	2.125
		0	125	Infiniband	2.50
		1	125	2× Fibre Channel	2.125
1	0	0	100	ESCON	0.200
		1	125	ESCON	0.200
1	1	0	106.25	4× Fibre Channel	4.25
		1	125	4× Fibre Channel	4.25

2.3 Output Drivers

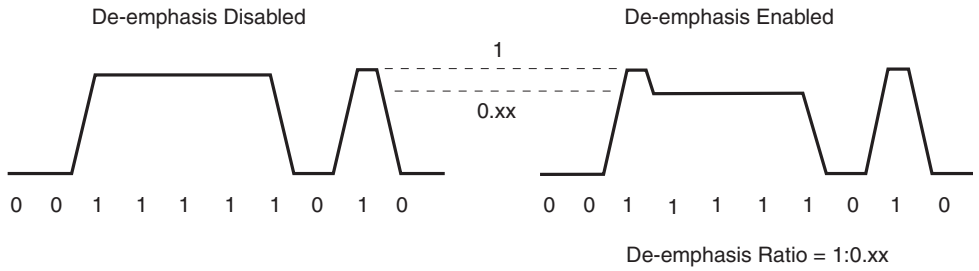
The output swing is user-programmable on a per-channel basis. When operating with a single 1.2-V power supply, the output levels are compatible with AC-coupled LVDS. When operating with a single 1.8-V power supply, the outputs can be programmed to one of three different levels. The outputs have 50-Ω back-termination resistors and should be AC-coupled.

2.3.1 De-Emphasis

All high-speed differential outputs contain a nine-level de-emphasis circuit, which is controlled by the RX/TX_ED[3:0] bits in the RX/TXOUT_CTRL register that can attenuate lower frequency signals in a transmitted data stream. Alternately, the RX/TXEMP pin can be used to set the de-emphasis to maximum (HIGH) or disable the de-emphasis (LOW).

The following figure shows with de-emphasis enabled that the initial amplitude of the signal after a transition is the same as when de-emphasis is disabled. However, after approximately a 1-bit delay, the amplitude of the signal drops by a programmable amount. By combining the amplitude control determined by the RX/TX_HIV[1:0] bits in the RX/TXOUT_CTRL register with the de-emphasis feature, the user has extremely flexible control of output amplitude. This feature can compensate for the loss of signal amplitude and the effect on the data eye opening, because of long cables or trace length runs. A maximum de-emphasis ratio of 1:0.5 produces more open data eyes at the end of a long cable or trace length run.

Figure 4. Output De-Emphasis



The following table shows the relative amplitude of the output as related to the output level controls, which are set by the RX/TX_HIV[1:0] bits in the RX/TXOUT_CTRL register and the de-emphasis controls, which are set by the RX/TX_ED[1:0] bits in the RX/TXOUT_CTRL register. The de-emphasis ratio is the non-de-emphasized signal (normalized to 1) compared to the de-emphasized signal. For a de-emphasized setting of 1:0.5, the reduced amplitude signal is one-half of the maximum signal.

Table 7. De-Emphasis Values for Typical Conditions

RX_ED[3:0]	De-Emphasis Ratio
0000	1:1.00 (no emphasis)
1001	1:0.94
0001	1:0.88
1010	1:0.81
0010	1:0.75
1011	1:0.68
0011	1:0.62
1100	1:0.55
0100	1:0.50 (maximum emphasis)
All other values are reserved for future use. If the RX/TX_SLE bit is set, these inputs are ignored, and the de-emphasis ratio is 1:1.	

The following table shows how the RX/TX_SLE bit of the RX/TXOUT_CTRL register controls the output slew rate. This feature is used to adjust the output slew rate to match the operating speed of the channel.

Table 8. Output Slew Rate Values

RX/TX_SLE	Output Slew Rate
0	Fastest
1	Slower by ~25%

The following table lists the output voltage swing levels of the channel. The values listed in the table are for 1.0625 Gbps and 2.125 Gbps operation measured per FC-PI-2, Section 9.3.1. The minimum values are inside the data eye, and maximum values are outside the data eye with the emphasis disabled for both.

Table 9. Output Swing Levels

	Output Swing $V_{DDIORX/TX}$ = 1.2 V			Output Swing $V_{DDIORX/TX}$ = 1.8 V		
RX_HIV[1:0]	Minimum	Typical	Maximum	Minimum	Typical	Maximum
00	770	970	1200	850	1050	1300
01		Reserved		950	1200	1700
10		Reserved		1050	1400	1800
11		Reserved			Reserved	

For 4.25-Gbps operation, the output is measured per FC-PI-2, session 9.3.3. With de-emphasis enabled, the measurement at both near-end and far-end after transmitter compliance transfer function (TCTF) is between 1600 mV and 310 mV differential respectively. The TCTF used is more stringent than the one defined by FC-PI-2. The attenuation frequencies are:

- 425 MHz: –3.1 dB
- 1.0625 GHz: –6.5 dB
- 2.125 GHz: –10.0 dB
- 4.25 GHz: –16.7 dB

2.3.2 SGMII Clock Output

The VSC8228-01 device provides an SGMII output clock on the host-side of the device for gigabit Ethernet applications. This output is disabled unless enabled by the serial interface port. For more information about the timing for this clock, see Figure 10, page 59. This clock runs at half the selected data rate (625 MHz for gigabit Ethernet) and complies with SGMII levels. The clock is supported only at the gigabit Ethernet rate. When disabled, the RXCLKN and RXCLKP outputs float HIGH. The SGMII clock output should be terminated by a 50-Ω resistor to ground for AC coupling and should be terminated with 50-Ω resistor to 1.2-V power supply for DC coupling.

2.4 TTL Inputs and Outputs

The VSC8228-01 includes adjustable TTL I/O levels. By providing 1.2 V, 1.8 V, 2.5 V, and 3.3 V to the VDDTTL pins, the TTL inputs and outputs match the levels for the respective VDDTTL voltage provided in Table 14, page 47. All TTL inputs have internal pull-ups. For PIO0 and PIO2, external 1 KΩ pull-up resistors to VDDTTL are required when these pins are used for outputs.

2.5 Pattern Generation, Pattern Checking, and Loopback Modes

A programmable pattern generator and pattern checker, as well as loopback features are provided to aid with system test and diagnostics. The device can generate and detect an unframed 2^7, 2^{23}, and 2^{31} pseudo-random bit stream (PRBS), a user-defined pattern of exactly 40 bits or 64 bits, and the Fibre Channel CRPAT, CJTPAT, and CSPAT patterns. The pattern generator and pattern checker are independent.

The device supports various host-side and line-side loopback, as well as pattern generation and pattern checking modes. These modes can be accessed by using the serial port or using the PIO[6:0] pins as described in Table 2, page 16. For line-side pattern generation and pattern checker modes, TX_FIFO_CTRL must be set to 20'h. For host-side pattern generation and pattern checker modes, RX_FIFO_CTRL must be set to 20'h. For both line-side generator and checker (mode 1) and host-side generator and checker (mode 12), the VSC8228-01 device must be set to a retimer mode.

2.6 Serial Interface Port

Communication to and from the device occurs through either pin control or by using a programmable serial interface port that supports SPI or two-wire serial and is accessible by programmable I/O pins PIO[6:0]. Control inputs and status outputs can be written to and read from the device using the serial port. The port can be configured either as two-wire serial interface or SPI, or it can be disabled so that the user can control the more important features of the device directly through input pins. For more information about LVTTL input pins PIO[6:0], see Table 2, page 16. The serial port does not require an external reference clock.

When the serial interfaces (SPI or two-wire) are disabled, the PIO[6:0] pins determine the mode of the device (loopback, normal, pattern generation, checking, and so forth) and whether the clock output is enabled.

The device has a power-on reset circuit that puts the device in the default state. The device also has a hardware RESET signal assigned to pin PIO2 in the non-serial state defined by PIO[3:2] = 01, as shown in Table 2, page 16. Setting RESET to a 1 places the device in the default state.

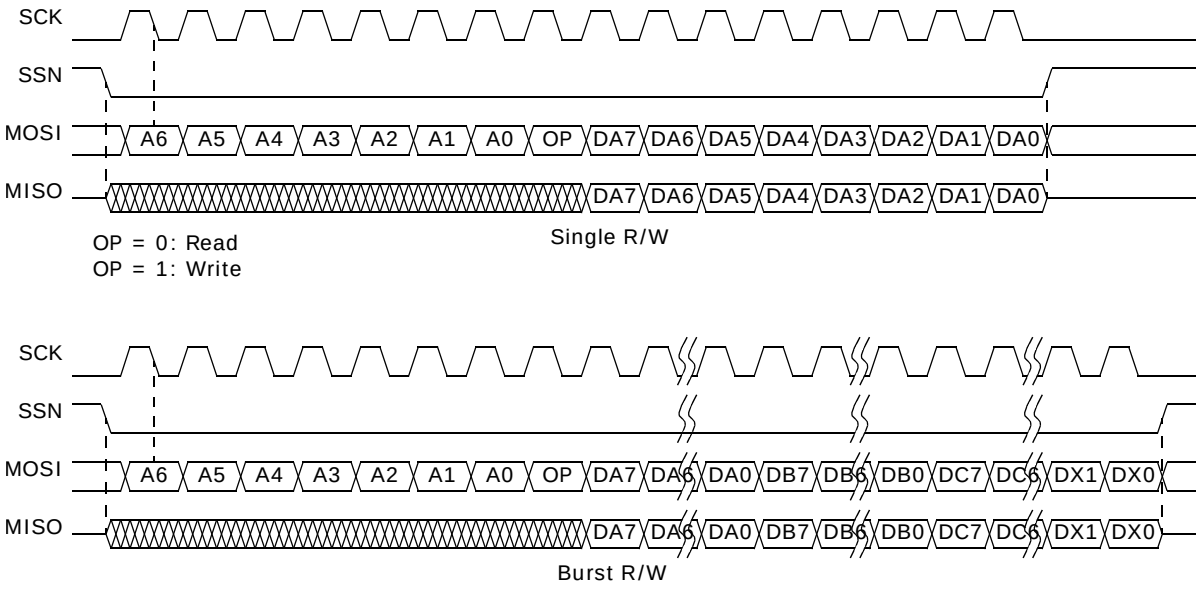
2.6.1 SPI Interface

The SPI protocol is described in the timing diagram of the following figure. Signal SSN is the active LOW serial select signal that must be LOW to activate the SPI port. Data is input into the device on signal MOSI (Master Out, Slave In), sampled on the falling edge of clock signal SCK. Data is output on signal MISO (Master In, Slave Out), synchronous with the rising edge of SCK. A 7-bit address is transferred first, followed by an OPCODE bit, which specifies whether a read (OP = 0) or write (OP = 1) operation is to take place, and then the data. Two read/write (R/W) modes are possible with the SPI protocol: single and burst. For more information about both modes, see Figure 5, page 24.

In single R/W mode, a single 8-bit word is transferred. After the 8 bits are transferred, the SSN line is brought HIGH, designating the end of the data transfer procedure. In burst mode, data bits transferred beyond the initial 8 bits are written to sequential

addresses until the SSN line is brought HIGH. If the SSN is brought HIGH before all 8 bits in a given word are transferred, none of the 8 bits in that word are transferred. All I/O levels are programmed based on the VDDTTL voltage. Internal pull-up resistors are weak on all PIO pins; therefore, external pull-up resistors should be added. SPI port does not support bus addressing, and the SPI of each the VSC8228 requires a separate SPI port to communicate with.

Figure 5. SPI Timing



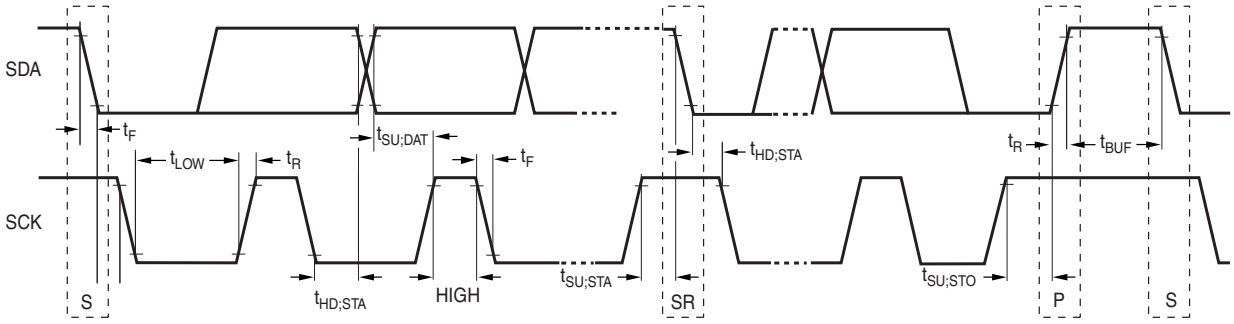
2.6.2 Two-Wire Serial Interface

The VSC8228-01 supports a slave mode, two-wire serial interface, where an external master device controls the VSC8228-01 device. The slave two-wire serial interface operates in both standard mode (up to 100 kbps) and fast mode (up to 400 kbps) data transfer rates.

To enable two-wire serial mode, it is recommended that the VSC8228-01 device first be powered up in pin programming mode. For information about configuring the device for two-wire serial mode, see "Controlling the PIO[6:0] and Multiplexer Mode Settings," page 15.

A valid START condition is generated by a master device by transitioning SDA HIGH to LOW while SCK is HIGH. Data is then transferred on the SDA line, most significant bit (MSB) first, with the SCK line clocking data. Data transitions during SCK LOW periods and is valid (read) or latched (write) when SCK pulses HIGH then LOW. Data transfers are acknowledged (ACK) by the receiving device (VSC8228-01) for data writes and by the master for data reads. An acknowledge is signaled by holding the SDA signal LOW while pulsing SCK HIGH then LOW. The master terminates data transfer by generating a STOP condition by transitioning SDA LOW to HIGH while SCK is HIGH. For a detailed timing diagram, see the following figure.

Figure 6. Two-Wire Serial Interface Timing



The interface supports eight different 7-bit slave addresses within the 8-bit device address. The slave address is programmed by using the PIO pins as indicated in the following table. All I/O levels are programmed based on the VDDTTL voltage. Pull-up resistors are provided on all PIO pins. Because the read and write (R/W) bit is the LSB of the 8-bit device address, the device address changes from a read to a write as shown in the following table. The slave address is compared to bits 7:1 of the device address byte, which is the first byte transmitted to the device after a START condition. The 8-bit of the device address byte is set LOW to indicate a write or HIGH to indicate a read.

Table 10. Two-Wire Serial Interface 7-Bit Slave Addresses

							Device Address (Read)			Device Address (Write)		
PIO6 /A2	PIO5 /A1	PIO 4	PIO 3	PIO 2/ A0	PIO 1	PIO 0	Byte Value	Slave Address Bits	R/W Bit	Byte Value	Slave Address Bits	R/W Bit
0	0	1	1	0	SCK	SDA	81'h	1000 000	1	80'h	1000 000	0
0	0	1	1	1	SCK	SDA	83'h	1000 001	1	82'h	1000 001	0
0	1	1	1	0	SCK	SDA	85'h	1000 010	1	84'h	1000 010	0
0	1	1	1	1	SCK	SDA	87'h	1000 011	1	86'h	1000 011	0
1	0	1	1	0	SCK	SDA	89'h	1000 100	1	88'h	1000 100	0
1	0	1	1	1	SCK	SDA	8B'h	1000 101	1	8A'h	1000 101	0
1	1	1	1	0	SCK	SDA	8D'h	1000 110	1	8C'h	1000 110	0
1	1	1	1	1	SCK	SDA	8F'h	1000 111	1	8E'h	1000 111	0

Note Because of the pull-up resistors on all PIO pins, the default serial address is 8F'h for read, 8E'h for write.

The first byte transferred is always the device address. Write accesses require a 3-byte transfer. The first byte is the device address with a write operation indicated. This is the 7-bit slave address followed by a HIGH R/W bit. The second byte contains the register address, and the third byte is the write data.

Read accesses require a 4-byte transfer. First a dummy write operation is sent, which is composed of two bytes: the device address with read operation indicated and the register address. Next, a START condition is sent. The third byte is a repeated device address with the R/W bit HIGH, and the fourth byte is the read data.

For write operations, the data is latched into the appropriate register during the acknowledge of the third byte. All transactions to or from the device are completed

during the acknowledge of the third byte, allowing the user to immediately initiate another transfer to the device or terminate transfers.

Multibyte read or write transactions are allowed and are extensions of the above protocol with additional data bytes added to the end of the transaction. All multibyte transactions cause the internal address to increment by one, regardless of the register address. For multibyte read transactions, the master terminates the data transfer by generating a not acknowledged (NACK) condition, holding SDA HIGH while pulsing SCK HIGH, then LOW, and then generating a STOP condition. See Figure 7, page 27 for illustrations of single-byte and multibyte R/W operations.

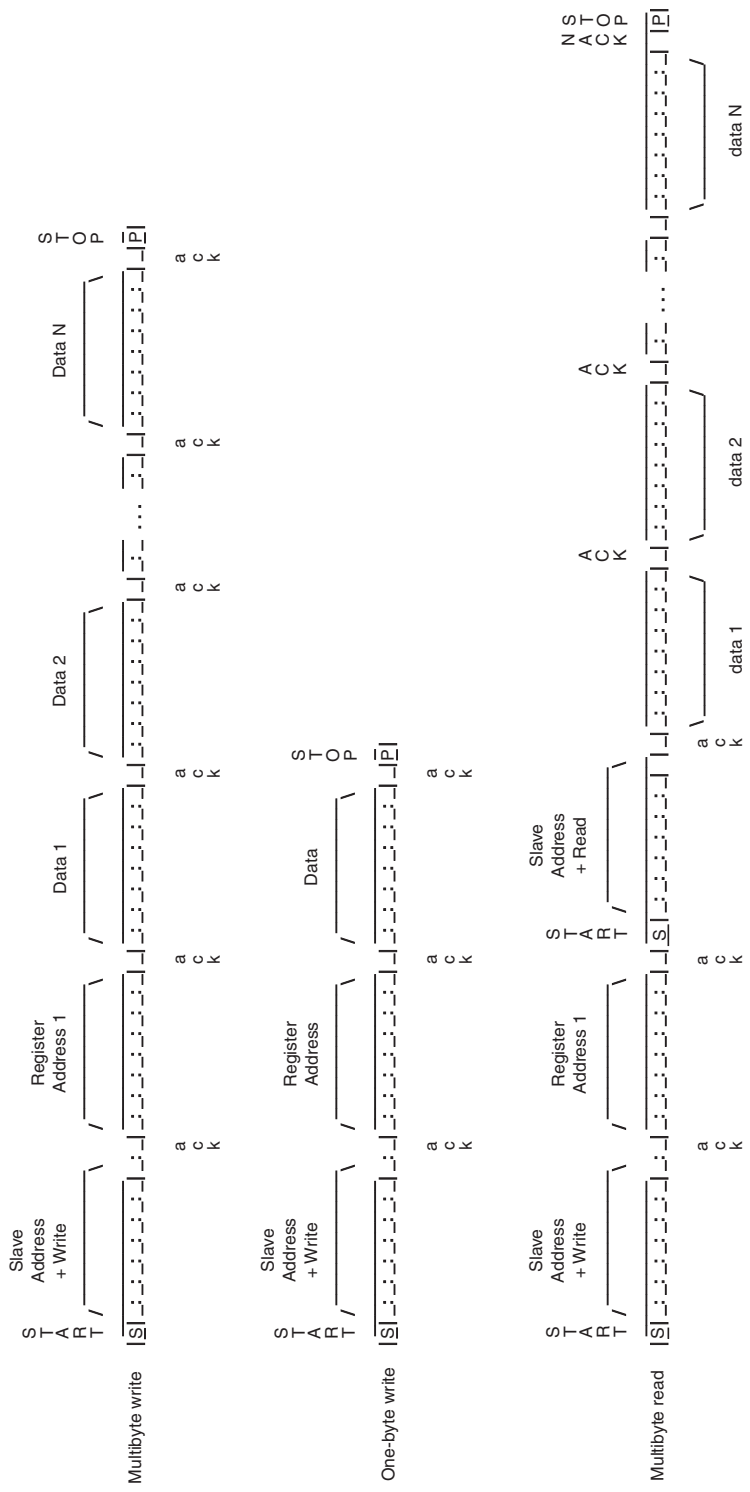
The following table shows a two-wire serial interface transaction example using slave address: 1000 111'b. The conventions used in the table are:

- [UPPERCASE] denotes a master's action.
- [lowercase] denotes a slave's action.
- [S] denotes a START: The master signals a start by transitioning SDA HIGH to LOW while SCK is HIGH.
- [P] denotes a STOP: The master signals a stop by transitioning SDA LOW to HIGH while SCK is HIGH.
- [A] denotes a master's ACK: The master signals an acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.
- [N] denotes a master's NACK: The master signals an reverse acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.
- [a] denotes a slave's ACK: The slave signals an acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.

Table 11. Two-Wire Serial Interface Transaction Example Using Slave Address

Transaction	Sequence
1 byte write	[S] [0x8E] [a] [REGISTER ADDRESS] [a] [DATA] [a] [P]
N byte write	[S] [0x8E] [a] [REGISTER ADDRESS 1] [a] [DATA 1][a] [DATA 2] [a] ... [DATA N-1] [a] [DATA N] [a] [P]
1 byte read	[S] [0x8E] [a] [REGISTER ADDRESS] [a] [S] [0x8F] [a] [data] [N] [P]
N byte read	[S] [0x8E] [a] [REGISTER ADDRESS 1] [a] [S] [0x8F] [a] [data 1] [A] [data 2] [A] ... [data n-1] [A] [data n] [N] [P]

Figure 7. Two-Wire Serial Interface Operation



Notes:
[UPPERCASE] denotes a master's action.
[lowercase] denotes a slave's action.
[S] denotes a START: The master signals a start by transitioning SDA HIGH to LOW while SCK is HIGH.
[P] denotes a STOP: The master signals a stop by transitioning SDA LOW to HIGH while SCK is HIGH.
[A] denotes a master's ACK: The master signals an acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.
[N] denotes a master's NACK: The master signals an reverse acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.
[a] denotes a slave's ACK: The slave signals an acknowledge by holding the SDA signal LOW while pulsing SCK HIGH then LOW.

2.7 Power Supply Filtering

The VSC8228-01 power supplies can be configured in one of three ways: 1.2-V power supply only, 1.8-V power supply only, or both 1.2-V and 1.8-V power supplies. For the HIGH output swing setting, VDDIORX and VDDIOTX must be connected to a 1.8-V pull-up inductor or else a ferrite bead must be connected from each high-speed output to a 1.2-V power supply to restore the DC common-mode of the output.

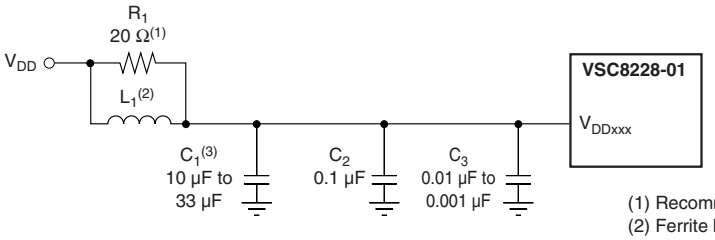
Contact your local Vitesse sales representative for more information on using a ferrite bead for DC restoration with a 1.2-V power supply. The following table lists each of the power supply connection groups for the VSC8228-01. Each group should be separately filtered using the filter depicted in the following figure to reduce crosstalk, jitter, and noise. If VDDTTL is set to 1.8 V, it can be connected to the VDDB18 filter.

Table 12. Power Supply Connection Groups by Configuration

Configuration	Power Supply Pin Name	Group Description	Connection
1.2 V only	VDDA12, VDDA18	CMU power supply	1.2 V
	VDDTX18, VDDTX12, VDDIOTX	Transmitter power supply	1.2 V
	VDDRX18, VDDRX12, VDDIORX	Receiver power supply	1.2 V
	VDDB12, VDDB18	Serial interface and digital logic	1.2 V
	VDDTTL	TTL power supply	1.2 V, 1.8 V, 2.5 V, or 3.3 V
1.8 V only	VDDA18	CMU power supply	1.8 V
	VDDTX18, VDDIOTX	Transmitter power supply	1.8 V
	VDDRX18, VDDIORX	Receiver power supply	1.8 V
	VDDB18	Serial interface and digital logic	1.8 V
	VDDTX12, VDDRX12, VDDB12, VDDA12	1.2-V regulated power supply	Bypass capacitors(1)
	VDDTTL	TTL power supply	1.2 V, 1.8 V, 2.5 V, or 3.3 V
1.2 V and 1.8 V	VDDA12, VDDA18	CMU power supply	1.2 V
	VDDIOTX	Transmitter I/O power supply	1.8 V
	VDDIORX	Receiver I/O power supply	1.8 V
	VDDTX12, VDDTX18	Transmitter power supply	1.2 V
	VDDRX12, VDDRX18	Receiver power supply	1.2 V
	VDDB12, VDDB18	Serial interface and digital logic	1.2 V
	VDDTTL	TTL power supply	1.2 V, 1.8 V, 2.5 V, or 3.3 V

1. When using only a 1.8-V power supply, bypass the 1.2-V connections with 1-µF and 0.001 µF capacitors.

Figure 8. Power Supply Filter



(1) Recommended for resonance damping.
(2) Ferrite bead with high impedance at high frequencies and a DC resistance of ~0.5 Ω.
(3) Ceramic recommended.

3 Registers

This section contains the register memory map and detailed descriptions of the bits in each register.

3.1 Register Map

This section provides a map of the serial interface port registers. The register width is 8 bits and the soft reset is to write FF'h to address 7F'h.

Table 13. Register Memory Map

Address	Bit	Register Name	Description	Access	Reset Value
00'h	7:0	CMU_STATUS	CMU loss-of-lock status register	R	00'h
01'h	7:0	RX_STATUS	Receiver channel status register	R	00'h
02'h	7:0	TX_STATUS	Transmitter channel status register	R	00'h
08'h	7:0	FIFO_STATUS	FIFO status	R	00'h
10'h	7:0	RX_SDU_CTRL	Receiver channel signal detect unit control	R/W	60'h
11'h	7:0	RX_ASD_CTRL	Receiver channel analog signal detect unit control	R/W	80'h
12'h	7:0	TX_SDU_CTRL	Transmitter channel signal detect unit control	R/W	60'h
13'h	7:0	TX_ASD_CTRL	Transmitter channel analog signal detect unit control	R/W	80'h
17'h	7:0	MODE_CTRL_0	Chip mode select	R/W	F0'h
1D'h	7:0	RX_FIFO_CTRL	Receiver FIFO control	R/W	D0'h
1E'h	7:0	TX_FIFO_CTRL	Transmitter FIFO control	R/W	D0'h
1F'h	7:0	RX_FT_MODE	Receiver channel retimer mode control	R/W	80'h
20'h	7:0	TX_FT_MODE	Transmitter channel retimer mode control	R/W	80'h
21'h	7:0	RX_DATA_CTRL	Receiver data path control	R/W	80'h
22'h	7:0	TX_DATA_CTRL	Transmitter data path control	R/W	80'h
23'h	7:0	CMU_RATE_CTRL	CMU rate control	R/W	C0'h
24'h	7:0	RX_RATE_CTRL	Receiver channel divider control	R/W	00'h
25'h	7:0	TX_RATE_CTRL	Transmitter channel divider control	R/W	00'h
26'h	7:0	REFCLK_CTRL	Reference clock frequency select	R/W	00'h
28'h	7:0	RXIN_CTRL	Receiver channel input control	R/W	04'h
29'h	7:0	RX_OUT_CTRL	Receiver channel output control	R/W	00'h
2A'h	7:0	TXIN_CTRL	Transmitter channel input control	R/W	04'h
2B'h	7:0	TX_OUT_CTRL	Transmitter channel output control	R/W	00'h
2C'h	7:0	RXCLK_CTRL	Receiver clock control	R/W	00'h
3A'h-41'h	8 × 7:0	PATCHK_UD7-0	User-defined checker pattern	R/W	00'h

Table 13. Register Memory Map *(continued)*

Address	Bit	Register Name	Description	Access	Reset Value
42'h-46'h	5 × 7:0	PATCHK_TIMER_SET4-0	Pattern checker timer set	R/W	00'h
47'h-4B'h	5 × 7:0	PATCHK_TIMER_READBACK4-0	Pattern checker timer readback	R	00'h
4E'h-51'h	4 × 7:0	ERRCNT3-0	Error counter	R	00'h
52'h	7:0	PATCHK_CTRL	Pattern checker control	R/W	20'h
54'h	7:0	PATCHK_STATUS	Pattern checker status	R	00'h
5A'h-61'h	8 × 7:0	PATGEN_UD7-0	User-defined generator pattern	R/W	00'h
62'h	7:0	PATGEN_CTRL	Pattern generator control	R/W	00'h
74'h-75'h	7:0	CHIP_ID	Chip identifier	R/W	00B0'h
7F'h	7:0	RESET	Device reset	W	00'h

3.2 CMU Status

Name: CMU_STATUS

Address: 00'h

Description: CMU lock status flag.

Table 14. CMU Status

Bit	Bit Label	Description	Access	Reset Value
7	CMU_LOL	CMU loss-of-lock status: 0: CMU is in lock. 1: CMU is or was out of lock. (This bit is cleared only after a read to this register.)	R	0
6:0		Unused.	R	0000000

3.3 Rx Status

Name: RX_STATUS

Address: 01'h

Description: Receiver channel status flags.

Table 15. Rx Status

Bit	Bit Label	Description	Access	Reset Value
7	RXASDERR	Receiver channel analog signal detect error: 0: Receiver channel signal detected. 1: Receiver channel signal not detected. (This bit is cleared only after a read to this register.)	R	0
6	RXRLLERR	Receiver channel run-length limit error: 0: Receiver channel run-length limit valid. 1: Receiver channel run-length limit violation. (This bit is cleared only after a read to this register.)	R	0
5	RXK28ERR	Receiver channel K28.5– error: 0: Receiver channel K28.5 valid. 1: Receiver channel K28.5 violation. (This bit is cleared only after a read to this register.)	R	0
4	RXSDU	RXSDU pin status: 0: RXSDU pin is LOW. 1: RXSDU pin is HIGH.	R	0
3	RXASD	RXASD pin status: 0: RXASD pin is LOW. 1: RXASD pin is HIGH.	R	0
2:0		Unused.	R	000

3.4 Tx Status

Name: TX_STATUS

Address: 02'h

Description: Transmitter channel status flags.

Table 16. Tx Status

Bit	Bit Label	Description	Access	Reset Value
7	TXASDERR	Transmitter channel analog signal detect error: 0: Transmitter channel signal not detected. 1: Transmitter channel signal detected. (This bit is cleared only after a read to this register.)	R	0

Table 16. Tx Status *(continued)*

Bit	Bit Label	Description	Access	Reset Value
6	TXRLLERR	Transmitter channel run-length limit error: 0: Transmitter channel run-length limit valid. 1: Transmitter channel run-length limit violation. (This bit is cleared only after a read to this register.)	R	0
5	TXK28ERR	Transmitter channel K28.5– error: 0: Transmitter channel K28.5 valid. 1: Transmitter channel K28.5 violation. (This bit is cleared only after a read to this register.)	R	0
4	TXSDU	TXSDU pin status: 0: TXSDU pin is LOW. 1: TXSDU pin is HIGH.	R	0
3	TXASD	TXASD pin status: 0: TXASD pin is LOW. 1: TXASD pin is HIGH.	R	0
2:0		Unused.	R	000

3.5 FIFO Status

Name: FIFO_STATUS

Address: 08'h

Description: FIFO status.

Table 17. FIFO Status

Bit	Bit Label	Description	Access	Reset Value
7	RXFIFO_OVERFL	RXFIFO overflow status: 0: RXFIFO normal. 1: RXFIFO overflow. (This bit is cleared only after a read to this register.)	R	0
6	TXFIFO_OVERFL	TXFIFO overflow status: 0: TXFIFO normal. 1: TXFIFO overflow. (This bit is cleared only after a read to this register.)	R	0
5:0		Unused.	R	0

3.6 Rx Signal Detect Control

Name: RX_SDU_CTRL

Address: 10'h

Description: Receiver channel signal detect control. This register programs the RXSDU pin.

Table 18. Rx Signal Detect Control

Bit	Bit Label	Description	Access	Reset Value
7	RXSDU_ASDERR_EN	Receiver channel analog signal detect error enable: If RXSDU_ASDERR_EN_SRC = 0, this bit is ignored and control reverts to the external ASD_DIS pin. 0: If RXSDU_ASDERR_EN_SRC = 1, RXSDU pin state does not depend on analog signal detect. 1: If RXSDU_ASDERR_EN_SRC = 1, RXSDU pin set HIGH if analog signal is detected.	R/W	0
6	RXSDU_K28ERR_EN	Receiver channel K28.5– error detect enable: 0: RXSDU pin state does not depend on K28.5– error detection. 1: RXSDU pin set HIGH if there are no K28.5- errors.	R/W	1
5	RXSDU_RLLERR_EN	Receiver channel run-length limit error detect enable: 0: RXSDU pin state does not depend on run-length limit error detection. 1: RXSDU pin set HIGH if there are no run-length limit errors.	R/W	1
4	RXSDUSEL	Receiver channel frame mode. If RXSDUSEL_SRC = 0, this bit is ignored and control reverts to the external SDUSEL pin: 0: If RXSDUSEL_SRC = 1, Fibre Timer uses single frame error mode. 1: If RXSDUSEL_SRC = 1, Fibre Timer uses multiple frame error mode.	R/W	0
3	RXSDUSEL_SRC	Receiver channel frame mode source: 0: External pin controls receiver channel analog signal detect enable. 1: RXSDUSEL_ASD_EN bit controls receiver channel analog signal detect enable.	R/W	0
2	RXSDUSEL_ASDERR_EN_SRC	Receiver channel analog signal detect enable source: 0: External pin controls receiver channel analog signal detect enable. 1: RXSDUSEL_ASDERR_EN bit controls receiver channel analog signal detect enable.	R/W	0
1:0		Unused.	R	00

3.7 Rx Analog Signal Detect Control

Name: RX_ASD_CTRL

Address: 11'h

Description: Receiver channel analog signal detect control. This register programs the RXASD pin.

Table 19. Rx Analog Signal Detect Control

Bit	Bit Label	Description	Access	Reset Value
7	RXASD_ASDERR_EN	Receiver channel analog signal detect error enable: 0: RXASD pin state does not depend on analog signal detect. 1: RXASD pin set HIGH if analog signal is detected.	R/W	1
6	RXASD_K28ERR_EN	Receiver channel K28.5– error detect enable: 0: RXASD pin state does not depend on K28.5– errors detect. 1: RXASD pin set HIGH if there are no K28.5– errors.	R/W	0
5	RXASD_RLLERR_EN	Receiver channel run-length limit error detect enable: 0: RXASD pin state does not depend on the run-length limit error detection. 1: RXASD pin set HIGH if there are no run-length limit errors.	R/W	0
4:0		Unused.	R	00000

3.8 Tx Signal Detect Control

Name: TX_SDU_CTRL

Address: 12'h

Description: Transmitter channel signal detect control. This register programs the TXSDU pin.

Table 20. Tx Signal Detect Control

Bit	Bit Label	Description	Access	Reset Value
7	TXSDU_ASDERR_EN	Transmitter channel analog signal detect error enable: If TXSDU_ASDERR_EN_SRC = 0, this bit is ignored and control reverts to the external ASD_DIS pin. 0: If TXSDU_ASDERR_EN_SRC = 1, TXSDU pin state does not depend on analog signal detection. 1: If TXSDU_ASDERR_EN_SRC = 1, TXSDU pin set HIGH if analog signal is detected.	R/W	0

Table 20. Tx Signal Detect Control *(continued)*

Bit	Bit Label	Description	Access	Reset Value
6	TXSDU_K28ERR_EN	Transmitter channel K28.5– error detect enable: 0: TXSDU pin state does not depend on K28.5– error detection. 1: TXSDU pin set HIGH if there are no K28.5– errors.	R/W	1
5	TXSDU_RLLERR_EN	Transmitter channel run-length limit detect error enable: 0: TXSDU pin state does not depend on the run-length limit error detection. 1: TXSDU pin set HIGH if there are no run-length limit errors.	R/W	1
4	TXSDUSEL	Transmitter channel frame mode: If TXSDUSEL_SRC = 0, this bit is ignored and control reverts to the external SDUSEL pin. 0: If TXSDUSEL_SRC = 1, Fibre Timer uses single frame error mode. 0: If TXSDUSEL_SRC = 1, Fibre Timer uses multiple frame error mode.	R/W	0
3	TXSDUSEL_SRC	Transmitter channel frame mode source: 0: External pin controls transmitter channel analog signal detect enable. 1: TXSDUSEL_ASDERR_EN bit controls transmitter channel analog signal detect enable.	R/W	0
2	TXSDUSEL_ASDERR_EN_SRC	Transmitter channel analog signal detect enable source: 0: External pin controls transmitter channel analog signal detect enable. 1: TXSDUSEL_ASDERR_EN bit controls transmitter channel analog signal detect enable.	R/W	0
1:0		Unused.	R	00

3.9 Tx Analog Signal Detect Control

Name: TX_ASD_CTRL

Address: 13'h

Description: Transmitter channel analog signal detect control. This register programs the TXASD pin.

Table 21. Tx Analog Signal Detect Control

Bit	Bit Label	Description	Access	Reset Value
7	TXASD_ASDERR_EN	Transmitter channel analog signal detect error enable: 0: TXASD pin state does not depend on analog signal detect. 1: TXASD pin set HIGH if analog signal is detected.	R/W	1
6	TXASD_K28ERR_EN	Transmitter channel K28.5– error detect enable: 0: TXASD pin state does not depend on K28.5– error detection. 1: TXASD pin set HIGH if there are no K28.5– errors.	R/W	0
5	TXASD_RLLERR_EN	Transmitter channel run-length limit error detect enable: 0: TXASD pin state does not depend on the run-length limit error detection. 1: TXASD pin set HIGH if there are no run-length limit errors.	R/W	0
4:0		Unused.	R	00000

3.10 Chip Mode Select

Name: MODE_CTRL_0

Address: 17'h

Description: Chip mode select.

Table 22. Chip Mode Select

Bit	Bit Label	Description	Access	Reset Value
7:4	MODESEL[3:0]	Chip mode select. If MODESEL_SRC = 0, this register is ignored and the M0/1/2/3 pins control the chip mode. If MODESEL_SRC = 1, the MODESEL pins correspond to M0/1/2/3. See Table 3, page 16. MODESEL[0] = M0. MODESEL[1] = M1. MODESEL[2] = M2. MODESEL[3] = M3.	R/W	1111

Table 22. Chip Mode Select *(continued)*

Bit	Bit Label	Description	Access	Reset Value
3	MODESEL_SRC	Mode control source. 0: Mode is controlled by the M0, M1, M2, and M3 pins. 1: Mode is controlled by the MODESEL[3:0] bits.	R/W	0
2:0		Unused.	R	000

3.11 Receiver Channel FIFO Control

Name: RX_FIFO_CTRL

Address: 1D'h

Description: Transmitter channel FIFO control

Table 23. Receiver Channel FIFO Control

Bit	Bit Name	Description	Access	Reset Value
7	RXADEN	Receiver channel add/drop FIFO enable: 0: If RXADAL_SRC = 1, the receiver channel FIFO add/drop is disabled. 1: If RXADAL_SRC = 1, the receiver channel FIFO add/drop is enabled.	R/W	1
6	RXALGEN	Receiver channel FIFO alignment enable: 0: If RXADAL_SRC = 1, the receiver channel FIFO alignment is disabled. 1: If RXADAL_SRC = 1, the receiver channel FIFO alignment is enabled.	R/W	1
5	RXADAL_SRC	Receiver channel FIFO control source: 0: Receiver FIFO add/drop enable and alignment controlled by the external M1/2/3/4 pins or MODSEL[3:0]. 1: Receiver FIFO add/drop enable and alignment controlled by the RXADEN and RXALGEN bits of this register.	R/W	0
4	RXOVERN	Receiver channel overflow and underflow control: 0: Disabled. 1: If the receiver FIFO overflow and underflow, the CDR automatically switches to repeater mode to avoid loss of data.	R/W	1
3:0		Unused.	R	0000

3.12 Transmitter Channel FIFO Control

Name: TX_FIFO_CTRL

Address: 1E'h

Description: Transmitter channel FIFO control

Table 24. Transmitter Channel FIFO Control

Bit	Bit Name	Description	Access	Reset Value
7	TXADEN	Transmitter channel add/drop FIFO enable: 0: If TXADAL_SRC = 1, the transmitter channel FIFO add/drop is disabled. 1: If TXADAL_SRC = 1, the transmitter channel FIFO add/drop is enabled.	R/W	1
6	TXALGEN	Transmitter channel FIFO alignment enable: 0: If TXADAL_SRC = 1, the transmitter channel FIFO alignment is disabled. 1: If TXADAL_SRC = 1, the transmitter channel FIFO alignment is enabled.	R/W	1
5	TXADAL_SRC	Transmitter channel FIFO control source: 0: Transmitter FIFO add/drop enable and alignment controlled by the external M1/2/3/4 pins or MODSEL[3:0]. 1: Transmitter FIFO add/drop enable and alignment controlled by the TXADEN and TXALGEN bits of this register.	R/W	0
4	TXOVERN	Transmitter channel overflow and underflow control: 0: Disabled. 1: If the transmitter FIFO overflows and under-flows, the CDR automatically switches to repeater mode to avoid loss of data.	R/W	1
3:0		Unused.	R	0000

3.13 Rx Fibre Timer Control

Name: RX_FT_MODE

Address: 1F'h

Description: Receiver Fibre timer mode.

Table 25. Rx Fibre Timer Control

Bit	Bit Label	Description	Access	Reset Value
7	RXRP	Receiver channel repeater enable (retimer disable). If RXRP_SRC = 0, this register is ignored and the external RXRP pin controls the mode. 0: If RXRP_SRC = 1, retimer mode. 1: If RXRP_SRC = 1, repeater mode.	R/W	0
6	RXRP_SRC	Receiver channel repeater enable source. 0: RXRP pin controls the repeater and retimer modes. 1: RXRP bit controls the repeater and retimer modes.	R/W	0
5:0		Unused.	R	000000

3.14 Tx Fibre Timer Control

Name: TX_FT_MODE

Address: 20'h

Description: Transmitter Fibre timer mode.

Table 26. Tx Fibre Timer Control

Bit	Bit Label	Description	Access	Reset Value
7	TXRP	Transmitter channel repeater enable (retimer disable). If TXRP_SRC = 0, this register is ignored and the external TXRP pin controls the mode. 0: If TXRP_SRC = 1, retimer mode. 1: If TXRP_SRC = 1, repeater mode.	R/W	1
6	TXRP_SRC	Transmitter channel repeater enable source. 0: TXRP pin controls the repeater and retimer modes. 1: TXRP bit controls the repeater and retimer modes.	R/W	0
5:0		Unused.	R	000000

3.15 Rx Channel Data Control

Name: RX_DATA_CTRL

Address: 21'h

Description: Receiver data control.

Table 27. Rx Channel Data Control

Bit	Bit Label	Description	Access	Reset Value
7	RXOEN	Receiver channel output enable. If RXOEN_SRC = 0, this register is ignored and the external RXOEN pin controls the mode. 0: If RXOEN_SRC = 1, RXOUT channel output is disabled. 1: If RXOEN_SRC = 1, RXOUT channel output is enabled.	R/W	1
6	RXOBITFLP	Receiver channel output bit flip: 0: Receiver channel output polarity is normal. 1: Receiver channel output polarity is inverted.	R/W	0
5	RXIBITFLP	Receiver channel input bit flip: 0: Receiver channel input polarity is normal. 1: Receiver channel input polarity is inverted.	R/W	0
4	RX_DTA(1)	Receiver channel auto data squelch enable: 0: Receiver channel output is normal. 1: Receiver channel output squelch on RXASDERR.	R/W	0
3	RXOEN_SRC	Receiver channel output enable source: 0: Receiver channel output enable controlled by the RXOEN pin. 1: Receiver channel output enable controlled by the RXOEN bit.	R/W	0
2:0		Unused.	R	000

1. RXASDERR refers to the internal signal output of the loss of signal circuit. When RX_DTA is high, output data is squelched if there is a loss of signal condition. When the signal is restored, the output data is also restored. For more information about programmable threshold values, see Table 1, page 14.

3.16 Tx Channel Data Control

Name: TX_DATA_CTRL

Address: 22'h

Description: Transmitter data control.

Table 28. Tx Channel Data Control

Bit	Bit Label	Description	Access	Reset Value
7	TXOEN	Transmitter channel output enable: If TXOEN_SRC = 0, this register is ignored and the external TXOEN pin controls the mode. 0: If TXOEN_SRC = 1, TXOUT channel output is disabled. 1: If TXOEN_SRC = 1, TXOUT channel output is enabled.	R/W	1
6	TXOBITFLP	Transmitter channel output bit flip: 0: Transmitter channel output polarity is normal. 1: Transmitter channel output polarity is inverted.	R/W	0
5	TXIBITFLP	Transmitter channel input bit flip: 0: Transmitter channel input polarity is normal. 1: Transmitter channel input polarity is inverted.	R/W	0
4	TX_DTA(1)	Transmitter channel auto data squelch enable: 0: Transmitter channel output is normal. 1: Transmitter channel output squelch on TXASDERR.	R/W	0
3	TXOEN_SRC	Transmitter channel output enable source: 0: Transmitter channel output enable controlled by the TXOEN pin. 1: Transmitter channel output enable controlled by the TXOEN bit.	R/W	0
2:0		Unused.	R	000

1. TXASDERR refers to the internal signal output of the loss of signal circuit. When TX_DTA is high, output data is squelched if there is a loss of signal condition. When the signal is restored, the output data is also restored. For more information about programmable threshold values, see Table 1, page 14.

3.17 CMU Rate Control

Name: CMU_RATE_CTRL

Address: 23'h

Description: CMU rate control.

Table 29. CMU Rate Control

Bit	Bit Label	Description	Access	Reset Value
7:6	CMU_DIV_SEL[1:0]	Service selection: If CMU_DIV_SEL_SRC = 0, these bits are ignored and the CMU rate is set by the external rate pins. 00: CMU Divider = 10. 01: CMU Divider = 16. 10: CMU Divider = 17. 11: CMU Divider = 20.	R/W	11
5	RATE_SEL_SRC	CMU_DIV_SEL source. 0: Rate controlled by external TXRATE0/1 and RXRATE0/1. 1: Rate controlled by CMU rate control, Rx clock divider, and Tx clock divider registers.	R/W	0
4:0		Unused.	R	00000

3.18 Rx Clock Divider

Name: RX_RATE_CTRL

Address: 24'h

Description: Receiver clock divider.

Table 30. Rx Clock Divider

Bit	Bit Label	Description	Access	Reset Value
7:5	RX_DIVK[2:0]	Receiver channel rate divider. If CMU_DIV_SEL_SRC = 0, these bits are ignored and the CMU rate is set by the external rate pins. 000: Divide by 32. 001: Divide by 20. 010: Divide by 16. 011: Divide by 10. 100: Divide by 8. 101: Divide by 4. 110: Divide by 2. 111: Divide by 1.	R/W	000
4:0		Unused.	R	00000

3.19 Tx Clock Divider

Name: TX_RATE_CTRL

Address: 25'h

Description: Transmitter clock divider.

Table 31. Tx Clock Divider

Bit	Bit Label	Description	Access	Reset Value
7:5	TX_DIVK[2:0]	Transmitter channel rate divider: If CMU_DIV_SEL_SRC = 0, these bits are ignored and the CMU rate is set by the external rate pins. 000: Divide by 32. 001: Divide by 20. 010: Divide by 16. 011: Divide by 10. 100: Divide by 8. 101: Divide by 4. 110: Divide by 2. 111: Divide by 1.	R/W	000
4:0		Unused.	R	00000

3.20 Reference Clock Control

Name: REFCLK_CTRL

Address: 26'h

Description: Reference clock control. For more information, see Table 5, page 19.

Table 32. Reference Clock Control

Bit	Bit Label	Description	Access	Reset Value
7	RCK_SEL	CMU reference clock frequency select: 0: Fast reference clock (125 MHz, 106.25 MHz,155.52 MHz) 1: Slow reference clock (62.5 MHz, 53.125 MHz, 77.76 MHz)	R/W	0
6:0		Unused	R/W	0000000

3.21 RX Channel Input Control

Name: RXIN_CTRL

Address: 28'h

Description: Receiver channel input control.

Table 33. RX Channel Input Control

Bit	Bit Label	Description	Access	Reset Value
7:5	RX_EQ[2:0]	Receiver input equalization: 000: 7.0 dB 001: 4.0 dB 010: 0.5 dB 011: 0.0 dB 100: 17.0 dB 101: 12.0 dB 110: 8.0 dB 111: 5.0 dB	R/W	000
4:2	RX_LMD[2:0]	Receiver input signal detection mode: 000: Loss-of-signal disabled (no signal detection) 001: Loss-of-signal and transition detection enabled 010: Reserved 011: Reserved 100: Reset 101: Reset 110: Reset 111: Reset	R/W	001
1:0	RX_LTH[1:0]	Receiver input loss of signal threshold setting (differential voltages): Low High 00: < 71 mV > 166 mV 01: < 116 mV > 200 mV 10: < 168 mV > 266 mV 11: < 177 mV > 298 mV	R/W	00

3.22 RX Channel Output Control

Name: RXOUT_CTRL

Address: 29'h

Description: Receiver channel output control.

Table 34. RX Channel Output Control

Bit	Bit Label	Description	Access	Reset Value
7:4	RX_ED[3:0]	Receiver output de-emphasis setting: 0000: 1:1.00 (no emphasis) 1001: 1:0.94 0001: 1:0.88 1010: 1:0.81 0010: 1:0.75 1011: 1:0.68 0011: 1:0.62 1100: 1:0.55 0100: 1:0.50 (maximum emphasis)	R/W	0000
3	RX_SLE	Receiver output slow edge-rate setting: 0: Fast edge rate 1: Slow edge rate	R/W	0
2:1	RX_HIV[1:0]	Receiver output swing setting: 00: Normal (for 1.2-V or 1.8-V VDDIO) 01: 25% swing amplitude (for 1.8-V VDDIO only) 10: 50% swing amplitude (for 1.8-V VDDIO only) 11: Reserved	R/W	00
0	RX_ED_SRC	Receiver de-emphasis setting source: 0: Receiver channel de-emphasis controlled by the RXEMP pin. 1: Receiver channel de-emphasis controlled by the RXOUT_CTRL register.	R/W	0

3.23 TX Channel Input Control

Name: TXIN_CTRL

Address: 2A'h

Description: Transmitter channel input control.

Table 35. TX Channel Input Control

Bit	Bit Label	Description	Access	Reset Value
7:5	TX_EQ[2:0]	Transmitter input equalization: 000: 7.0 dB 001: 4.0 dB 010: 0.5 dB 011: 0.0 dB 100: 17.0 dB 101: 12.0 dB 110: 8.0 dB 111: 5.0 dB	R/W	000
4:2	TX_LMD[2:0]	Transmitter input signal detection mode: 000: Loss-of-signal disabled (no signal detection) 001: Loss-of-signal and transition detection enabled 010: Reserved 011: Reserved 100: Reset 101: Reset 110: Reset 111: Reset	R/W	001
1:0	TX_LTH[1:0]	Transmitter input loss of signal threshold setting (differential voltages): Low High 00: < 71 mV > 166 mV 01: < 116 mV > 200 mV 10: < 168 mV > 266 mV 11: < 177 mV > 298 mV	R/W	00

3.24 Tx Channel Output Control

Name: TXOUT_CTRL

Address: 2B'h

Description: Transmitter channel output control.

Table 36. Tx Channel Output Control

Bit	Bit Label	Description	Access	Reset Value
7:4	TX_ED[3:0]	Transmitter output de-emphasis setting: 0000: 1:1.00 (no emphasis) 1001: 1:0.94 0001: 1:0.88 1010: 1:0.81 0010: 1:0.75 1011: 1:0.68 0011: 1:0.62 1100: 1:0.55 0100: 1:0.50 (maximum emphasis)	R/W	0000
3	TX_SLE	Transmitter output slow edge-rate setting: 0: Fast edge rate. 1: Slow edge rate.	R/W	0
2:1	TX_HIV[1:0]	Transmitter output swing setting: 00: Normal (1.2-V or 1.8-V VDDIO). 01: 25% swing amplitude (for 1.8-V VDDIO only). 10: 50% swing amplitude (for 1.8-V VDDIO only). 11: Reserved.	R/W	00
0	TX_ED_SRC	Transmitter de-emphasis setting source: 0: Transmitter channel de-emphasis controlled by the TXEMP pin. 1: Transmitter channel de-emphasis controlled by the TXOUT_CTRL register.	R/W	0

3.25 Rx Clock Control

Name: RXCLK_CTRL

Address: 2C'h

Description: Receiver clock enable register (SGMII).

Table 37. Rx Clock Control

Bit	Bit Label	Description	Access	Reset Value
7	CKOUT_EN	RXCLK output enable: 0: Receiver output clock disabled. 1: Receiver output clock enabled.	R/W	0

Table 37. Rx Clock Control *(continued)*

Bit	Bit Label	Description	Access	Reset Value
6	CKOUT_EN_SRC	CKOUT_EN source: 0: Receiver output clock controlled by the PIO[6:0] mode setting. 1: Receiver output clock controlled by the CKOUT_EN bit.	R/W	0
5:0		Unused.	R/W	000000

3.26 Pattern Checker

Name: PATCHK_UD_7-0

Address: 3A'h-41'h

Description: User-defined pattern checker.

Table 38. Pattern Checker

Bit	Bit Label	Description	Access	Reset Value
7:0	UDCHK[63:56]	User-defined checker pattern, bits 63:56	R/W	00'h
7:0	UDCHK[55:48]	User-defined checker pattern, bits 55:48	R/W	00'h
7:0	UDCHK[47:40]	User-defined checker pattern, bits 47:40	R/W	00'h
7:0	UDCHK[39:32]	User-defined checker pattern, bits 39:32	R/W	00'h
7:0	UDCHK[31:24]	User-defined checker pattern, bits 31:24	R/W	00'h
7:0	UDCHK[23:16]	User-defined checker pattern, bits 23:16	R/W	00'h
7:0	UDCHK[15:8]	User-defined checker pattern, bits 15:8	R/W	00'h
7:0	UDCHK[7:0]	User-defined checker pattern, bits 7:0	R/W	00'h

3.27 Pattern Checker Timer Setting

Name: PATCHK_TIMER_SET4-0

Address: 42'h-46'h

Description: 40-bit pattern checker timer set. The timer updates at a rate of 1/16th the data rate.

Table 39. Pattern Checker Timer Setting

Bit	Bit Label	Description	Access	Reset Value
7:0	TIMER_SET[39:32]	Pattern checker timer setting, bits 39:32	R/W	00'h
7:0	TIMER_SET[31:24]	Pattern checker timer setting, bits 31:24	R/W	00'h
7:0	TIMER_SET[23:16]	Pattern checker timer setting, bits 23:16	R/W	00'h
7:0	TIMER_SET[15:8]	Pattern checker timer setting, bits 15:8	R/W	00'h

Table 39. Pattern Checker Timer Setting *(continued)*

Bit	Bit Label	Description	Access	Reset Value
7:0	TIMER_SET[7:0]	Pattern checker timer setting, bits 7:0	R/W	00'h

3.28 Pattern Checker Timer Readback

Name: PATCHK_TIMER_READBACK4-0

Address: 47'h-4B'h

Description: 40-bit pattern checker timer set. The timer updates at a rate of 1/16th the data rate.

Table 40. Pattern Checker Timer Readback

Bit	Bit Label	Description	Access	Reset Value
7:0	TIMER_READBACK[39:32]	Pattern checker timer setting, bits 39:32	R/W	00'h
7:0	TIMER_READBACK[31:24]	Pattern checker timer setting, bits 31:24	R/W	00'h
7:0	TIMER_READBACK[23:16]	Pattern checker timer setting, bits 23:16	R/W	00'h
7:0	TIMER_READBACK[15:8]	Pattern checker timer setting, bits 15:8	R/W	00'h
7:0	TIMER_READBACK[7:0]	Pattern checker timer setting, bits 7:0	R/W	00'h

3.29 Pattern Checker Error Counter

Name: ERRCNT3-0

Address: 4E'h-51'h

Description: Error counter for pattern checker.

Table 41. Pattern Checker Error Counter

Bit	Bit Label	Description	Access	Reset Value
7:0	ERRCNT[31:24]	Error counter, bits 31:24	R	00'h
7:0	ERRCNT[23:16]	Error counter, bits 23:16	R	00'h
7:0	ERRCNT[15:8]	Error counter, bits 15:8	R	00'h
7:0	ERRCNT[7:0]	Error counter, bits 7:0	R	00'h

3.30 Pattern Checker Control

Name: PATCHK_CTRL

Address: 52'h

Description: Controls the pattern checker.

Table 42. Pattern Checker Control

Bit	Bit Label	Description	Access	Reset Value
7	ERRMASKEN	Error mask enable (self-clearing): 0: Error mask disabled. 1: Error mask enabled.	R/W	0
6	FRUN	Free run mode enable: 0: Checker stops counting errors when timer reaches 0. 1: Checker continues counting errors, regardless of timer state.	R/W	0
5	HOLDCNT	Hold error count enable: 0: Reset error count between test. 1: Hold error count between test.	R/W	0
4	PATCHK_START	Starts checker: 0: Checker is stopped, holding error count. 1: Set HIGH to start checker and reset error count, stays HIGH while checking errors.(1)	R/W	0
3:0	PATCHK_SEL[2:0]	Pattern checker select: 0000: PRBS7.(2) 0001: PRBS23.(2) 0010: PRBS31.(2) 0011: User-defined 64-bit pattern. 0100: User-defined 40-bit pattern. 0101: Fibre Channel CJTPAT. 0110: Fibre Channel CRPAT. 0111: Fibre Channel CSPAT.	R/W	0010

1. To ensure that the checker starts cleanly, first write this register to desired state, with PATCHK_START bit = 0. Then write this register again, with PATCHK_START bit = 1.
2. The polarity of the PRBS pattern is different from the popular BERT used in the lab. To match the corresponding PRBS pattern of the external BERT, bit 5 of RX_DATA_CTRL and TX_DATA_CTRL can be set to flip the polarity.

3.31 Pattern Checker Status

Name: PATCHK_STATUS

Address: 54'h

Description: Status of pattern checker. Bits 0 through 5 are cleared only upon start or restart of the checker. The BUSY bit is asserted at the start of the test and is cleared only if the checker is stopped, the error counter is full, or the timer reaches zero.

Table 43. Pattern Checker Status

Bit	Bit Label	Description	Access	Reset Value
7:6		Undefined	R	00
5	FWERR	Fill-word error: 0: Fill word count is normal 1: Fill word count	R	0
4	SYNC	Pattern synchronization: 0: Synchronization not established 1: Synchronization is established	R	0
3	FAIL	Pattern checker fail: 0: No errors detected 1: Error detected	R	0
2	ECF	Error counter overflow: 0: Error counter normal 1: Error counter overflow	R	0
1	SYNCERR	Synchronization error: 0: Synchronization normal 1: Error Synchronizing	R	0
0	BUSY	Pattern checker status: 0: Not checking pattern 1: Checking pattern	R	0

3.32 Pattern Generator Pattern

Name: PATGEN_UD7-0

Address: 5A'h-61'h

Description: User-defined generator pattern. For 64-bit patterns, all eight registers are used and the MSB is bit 7 of 0x5A. For 40-bit patterns, only the lower five registers are used and the MSB is bit 7 of 0x5D. These registers alternatively hold the user-defined 40-bit idle word (0x5D - 0x61) and count (0x5C.2:0) when the IDLE_EN bit is set HIGH.

Table 44. Pattern Generator Pattern

Bit	Bit Label	Description	Access	Reset Value
7:0	UDGEN[63:56]	User-defined generator pattern, bits 63:56	R/W	00'h
7:0	UDGEN[55:48]	User-defined generator pattern, bits 55:48	R/W	00'h
7:0	UDGEN[47:40]	User-defined generator pattern, bits 47:40	R/W	00'h

Table 44. Pattern Generator Pattern *(continued)*

Bit	Bit Label	Description	Access	Reset Value
7:0	UDGEN[39:32]	User-defined generator pattern, bits 39:32	R/W	00'h
7:0	UDGEN[31:24	User-defined generator pattern, bits 31:24	R/W	00'h
7:0	UDGEN[23:16]	User-defined generator pattern, bits 23:16	R/W	00'h
7:0	UDGEN[15:8]	User-defined generator pattern, bits 15:8	R/W	00'h
7:0	UDGEN[7:0]	User-defined generator pattern, bits 7:0	R/W	00'h

3.33 Pattern Generator Control

Name: PATGEN_CTRL

Address: 62'h

Description: Control of pattern generator.

Table 45. Pattern Generator Control

Bit	Bit Label	Description	Access	Reset Value
7:6		Undefined	R/W	00
5	IDLE_EN	Custom idle enable (custom idle sequence and idle count is entered into lower 40 bits of PATGEN_UD registers): 0: Custom idle disabled 1: Custom idle enabled	R/W	0
4	PATGEN_EN	Pattern generator enable: 0: Pattern generator disabled 1: Pattern generator enabled	R/W	0
3:0	PATGEN_SEL[2:0]	Pattern generator select 0000: PRBS7.(1) 0001: PRBS23.(1) 0010: PRBS31.(1) 0011: User-defined 64-bit pattern 0100: User-defined 40-bit pattern 0101: Fibre Channel CJTPAT 0110: Fibre Channel CRPAT 0111: Fibre Channel CSPAT	R/W	0010

1. The polarity of the PRBS pattern is different from the popular BERT used in the lab. To match the corresponding PRBS pattern of the external BERT, bit 5 and bit 6 of RX_DATA_CTRL and TX_DATA_CTRL can be set to flip the polarity.

3.34 Chip Revision

Name: CHIP_REV[7:0]

Address: 74'h

Description: ASCII chip revision.

Table 46. Chip Revision

Bit	Bit Label	Description	Access	Reset Value
7:0	CHIP_REV[7:0]	Chip revision	R	07'h

3.35 Chip Identification

Name: CHIP_ID[7:0]

Address: 75'h

Description: ASCII chip identification.

Table 47. Chip Identification

Bit	Bit Label	Description	Access	Reset Value
7:0	CHIP_ID[7:0]	Chip identifier	R	B0'h

3.36 Register Reset

Name: RESET

Address: 7F'h

Description: Reset.

Table 48. Register Reset

Bit	Bit Label	Description	Access	Reset Value
7	REGRST	Resets all registers to the default state. It is a one-shot reset and writing a one into it resets the registers. It is self clearing.	W	0
6	MRST	Master reset. Resets registers and data path. It is an edge-triggered reset and writing a one to it resets the registers and data paths. However, another write of zero is needed for it to be set back to low.	W	0
5:0		Unused.	W	000000

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, stress ratings, and power sequencing for the VSC8228-01 device. The following characteristics are guaranteed for 1.8-V external power supplies. An internal power supply regulator is employed to generate the internal 1.2-V supplies.

4.1 DC Characteristics

The following table shows the DC characteristics for the VSC8228-01 device. The specifications listed in the following table are guaranteed over the recommended operating conditions shown in Table 55, page 63.

Table 49. DC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input HIGH voltage (LVTTL)	V_{IH}	0.7		V_{DDTTL}	V	V_{DDTTL} = 1.2 V.
		1.3		V_{DDTTL}	V	V_{DDTTL} = 1.8 V.
		1.7		V_{DDTTL}	V	V_{DDTTL} = 2.5 V.
		2.0		V_{DDTTL}	V	V_{DDTTL} = 3.3 V.
Input LOW voltage (LVTTL)	V_{IL}	–0.3		0.4	V	V_{DDTTL} = 1.2 V.
		–0.3		0.6	V	V_{DDTTL} = 1.8 V.
		–0.3		0.8	V	V_{DDTTL} = 2.5 V.
		–0.3		0.8	V	V_{DDTTL} = 3.3 V.
Input HIGH current (LVTTL)	I_{IH}	–500		500	µA	V_{IN} = 2.0 V V_{DDTTL} = 3.3 V.
Input LOW current (LVTTL)	I_{IL}	–50		50	µA	V_{IN} = 0.5 V V_{DDTTL} = 3.3 V.
Output HIGH voltage (LVTTL)	V_{OH_TTL}	0.9		V_{DDTTL}	V	V_{DDTTL} = 1.2 V. I_{OH} = 0.2 mA.
		1.4		V_{DDTTL}	V	V_{DDTTL} = 1.8 V. I_{OH} = 0.2 mA.
		1.8		V_{DDTTL}	V	V_{DDTTL} = 2.5 V. I_{OH} = 0.4 mA.
		2.4		V_{DDTTL}	V	V_{DDTTL} = 3.3 V. I_{OH} = 0.4 mA.
Output HIGH voltage (open-drain)	V_{OH_OD}	0.9		V_{DDTTL}	V	V_{DDTTL} = 1.2 V. I_{OH} = 0.2 mA. 1 kΩ to VDDTTL.
		1.4		V_{DDTTL}	V	V_{DDTTL} = 1.8 V. I_{OH} = 0.2 mA. 1 kΩ to VDDTTL.
		1.8		V_{DDTTL}	V	V_{DDTTL} = 2.5 V. I_{OH} = 0.4 mA. 1 kΩ to VDDTTL.
		2.4		V_{DDTTL}	V	V_{DDTTL} = 3.3 V. I_{OH} = 0.4 mA. 1 kΩ to VDDTTL.

Table 49. DC Characteristics *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Output LOW voltage (LVTTL, open-drain)	V_{OL}	0		0.2	V	V_{DDTTL} = 1.2 V. I_{OL} = 0.2 mA.
		0		0.4	V	V_{DDTTL} = 1.8 V. I_{OL} = 0.2 mA.
		0		0.5	V	V_{DDTTL} = 2.5 V. I_{OL} = 0.4 mA.
		0		0.5	V	V_{DDTTL} = 3.3 V. I_{OL} = 0.4 mA.
Power supply voltage	V_{DD18}	1.62	1.8	1.98	V	VDD = 1.8 V ±10%.
Power supply voltage (optional)	V_{DD12}	1.14	1.2	1.26	V	VDD = 1.2 V ±5%.
Power supply current	I_{DD}		300	400	mA	
Power dissipation for 1.2-V power supply	P_{D12}		360	540	mW	Outputs open. All supplies connected to 1.2-V power supply. RXCLK disabled.
Power dissipation for 1.8-V power supply	P_{D18}		520	790	mW	Outputs open. All supplies connected to 1.8-V power supply. RXCLK disabled.

4.2 AC Characteristics

This section contains the AC characteristics. The specifications listed in the following table are guaranteed over the recommended operating conditions shown in Table 55, page 63.

Table 50. AC Characteristics for 1 Gbps and 2 Gbps

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Latency from data input to data output (repeater mode)	t_{LRP}	5		10	UI	RXIN to RXOUT and TXIN to TXOUT; repeater mode.
Latency from data input to data output (retimer mode)	t_{LRT}		120	260	UI	RXIN to RXOUT and TXIN to TXOUT; retimer mode.
Differential data output rise time and fall time	t_R, t_F		70	85	ps	RXOUT, TXOUT; 20% to 80%, 4.25-Gbps rate only.
–3 dB roll of point of the jitter transfer curve	J_{TNFR}, –3 dB	75		150	kHz	Rx/Tx in to Rx/Tx out.
Peaking of the jitter transfer curve	J_{TNFR}, pk			0.75	dB	Rx/Tx in to Rx/Tx out.
Total data output jitter	$t_{J(RTMR)}$			0.25	UI	Jitter generation, RCK_SEL= 0.

Table 50. AC Characteristics for 1 Gbps and 2 Gbps *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial data output deterministic jitter peak-to-peak	$t_{DJ(RTMR)}$			0.10	UI	Jitter generation, RCK_SEL= 0.
Total jitter tolerance (Fibre Channel)	t_{JTOL_FC}			0.76	UI	Maximum eye closure, RCK_SEL= 0.
Total jitter tolerance (SONET)	t_{JTOL_SONET}	1.5x			SONET mask	1 MHz < f < 5 MHz, 2.48832 GHz. See Figure 9, page 59.
SGMII output rise time and fall time	t_R, t_F			200	ps	RXCLK, 20% to 80%, 1-GbE rate only.
SGMII clock to Q	$t_{CLOCK2Q}$	250		550	ps	RXCLK, 1-GbE rate only.
CML differential input swing	ΔV_{IN}	150		1600	mVp-p	AC-coupled.
CML differential output swing(1)	ΔV_{OUTD}	850	1050	1500	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. TX_HIV/ RX_HIV[1:0] = 00.
		950	1200	1700	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. TX_HIV/ RX_HIV[1:0] = 01.
		1050	1400	2000	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. TX_HIV/ RX_HIV[1:0] = 10.
		680		1300	mVp-p	50 Ω, V_{DDIO} = 1.2 V without pull-up inductors. TX_HIV/ RX_HIV[1:0] = 00.
SGMII differential output swing (SGMII clock)	ΔV_{OUTCLK}	150		400	mVp-p	50 Ω, 1-GbE rate only.

1. The following UI measurement widths were used for each data rate:
   4.25 Gbps = 0 UI
   2.125 Gbps = 0.32 UI
   1.0625 Gbps = 0.35 UI
   0.2 Gbps = 0.35 UI

Table 51. AC Characteristics for 4 Gbps

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Latency from data input to data output (repeater mode)	t_{LRP}	5		10	UI	RXIN to RXOUT and TXIN to TXOUT; repeater mode.
Latency from data input to data output (retimer mode)	t_{LRT}		120	260	UI	RXIN to RXOUT and TXIN to TXOUT; retimer mode.
Differential data output rise time and fall time	t_R, t_F		70	85	ps	RXOUT, TXOUT; 20% to 80%, 4.25-Gbps rate only.

Table 51. AC Characteristics for 4 Gbps *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
–3 dB roll of point of the jitter transfer curve	J_{TNFR}, –3 dB	75		150	kHz	Rx/Tx in to Rx/Tx out.
Peaking of the jitter transfer curve	J_{TNFR}, pk			0.75	kHz	Rx/Tx in to Rx/Tx out.
Total data output jitter	$T_{J(RTMR)}$			0.15	UI	Jitter generation, RCK_SEL=0 Operating speed at 1.0625 Gbps and 2.125 Gbps, per FC-PI-2 Section 9 and MJS.
				0.31	UI	Jitter generation, RCK_SEL=0 Operating speed at 4.25 Gbps, measured at near end of TCTF per FC-PI-2 Section 9 and MJS. Maximum de-emphasis and output swing set at +25% level.
				0.36	UI	Jitter generation, RCK_SEL=0. Operating speed at 4.25 Gbps, measured at far-end of TCTF per FC-PI-2 Section 9 and MJS. Maximum de-emphasis and output swing set at +25% level.
Serial data output deterministic jitter, p-p	$t_{DJ(RTMR)}$			0.06	UI	Jitter generation, RCK_SEL = 0 Operating speed at 1.0625 Gbps and 2.125 Gbps, per FC-PI-2 Section 9 and MJS.
				0.10	UI	Jitter generation, RCK_SEL=0. Operating speed at 4.25Gbps, measured at near-end of TCTF per FC-PI-2 Section 9 and MJS. Maximum de-emphasis and output swing set at +25% level.
				0.14	UI	Jitter generation, RCK_SEL = 0. Operating speed at 4.25 Gbps, measured at far-end of TCTF per FC-PI-2 Section 9 and MJS. Maximum de-emphasis and output swing set at +25% level.
Total jitter tolerance	T_{JTOL}			0.76	UI	Maximum eye closure, RCK_SEL = 0, per FC-PI-2 Section 9 and MJS.
SGMII output rise time and fall time	t_R, t_F			200	ps	RXCLK, 20% to 80%, 1-GbE rate only.
SGMII clock to Q	$t_{CLOCK2Q}$	250		550	ps	RXCLK, 1-GbE rate only.

Table 51. AC Characteristics for 4 Gbps *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
CML differential input swing	ΔV_{IN}	150		2400	mVp-p	AC-coupled.
CML differential output swing (1) at 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps	V_{OUTD}	850	1050	1550	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. Tx_HIV/RX_HIV[1:0] = 00
		950	1200	1800	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. Tx_HIV/RX_HIV[1:0]=01
		1050	1400	2050	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. Tx_HIV/RX_HIV[1:0] = 10
		680		1300	mVp-p	50 Ω, V_{DDIO} = 1.2 V without pull-up inductors. Tx_HIV/RX_HIV[1:0] = 00
CML differential output swing (1) at 4.25 Gbps, at near end of TCTF	V_{OUTD}	550		1600	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. Tx_HIV/RX_HIV[1:0]=01 Maximum de-emphasis level and +25% level. Measured at near-end of the TCTF per FC-PI-2, Section 9. TCTF characteristics are: 425 MHz: -3.1 dB 1.0625 GHz: -6.5 dB 2.125 GHz: -10.0 dB 4.25 GHz: -16.7 dB
CML differential output swing (1) at 4.25 Gbps, at the far end of TCTF	V_{OUTD}	310		1600	mVp-p	50 Ω, V_{DDIO} = 1.8 V or V_{DDIO} = 1.2 V with pull-up inductors. Tx_HIV/RX_HIV[1:0]=01 Maximum de-emphasis level and +25% level. Measured at far-end of the TCTF per FC-PI-2, Section 9. TCTF characteristics are: 425 MHz: –3.1 dB 1.0625 GHz: –6.5 dB 2.125 GHz: –10.0 dB 4.25 GHz: –16.7 dB
SGMII differential output swing (SGMII clock)	ΔV_{OUTCLK}	150		400	mVp-p	50 Ω, 1-GbE rate only.

Figure 9. STS-48 SONET Jitter Tolerance Mask

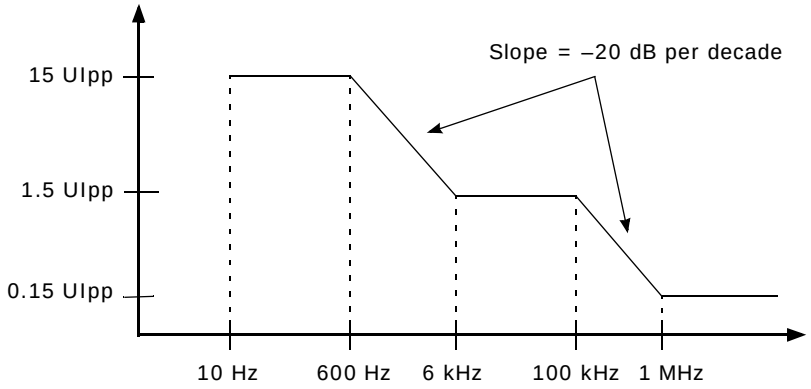
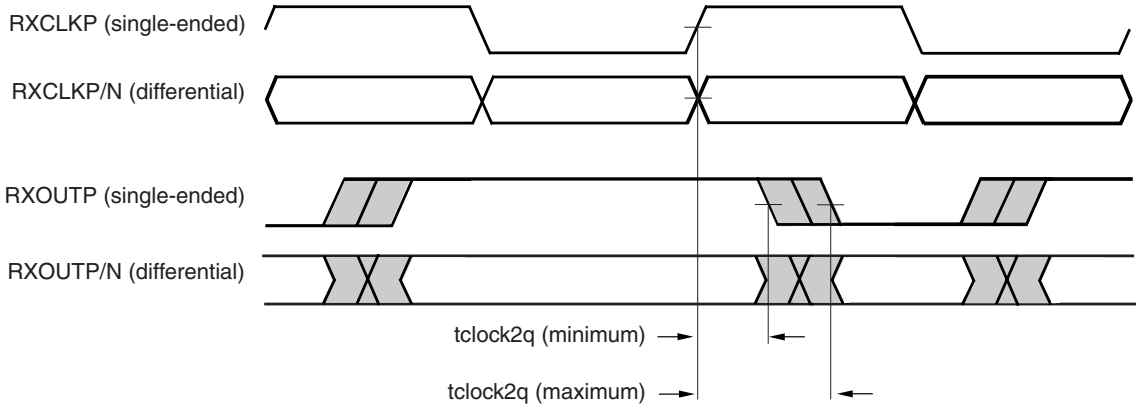


Figure 10. SGMII Clock Timing



The following table lists the reference clock parameters and values.

Table 52. Reference Clock

Parameter	Symbol	Minimum	Maximum	Unit	Condition
REFCLK input rise time and fall time	T_T		2.0	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
Frequency offset between incoming data and REFCLK	F_O	–200	200	ppm	Reference clock frequency must be within 100 ppm of the frequency stated in Table 5, page 19.
REFCLK duty cycle	DCC	40	60	%	
Input HIGH voltage (LVTTL)	V_{IH}	2.0	3.9	V	LVTTL reference clock input. V_{DDTTL} = 3.3 V.
Input LOW voltage (LVTTL)	V_{IL}	–0.3	0.5	V	LVTTL reference clock input. V_{DDTTL} = 3.3 V.
Input HIGH current (LVTTL)	I_{IH}	–200	200	µA	LVTTL reference clock input. V_{IN} = 2.0 V.
Input HIGH voltage (HSTL)	V_{IH}	V_X + 0.1	1.6	V	HSTL reference clock input.

Table 52. Reference Clock *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input LOW voltage (HSTL)	V_{IL}	–0.3	V_X – 0.1	V	HSTL reference clock input.
Input HIGH current (HSTL)	I_{IH}	–200	200	µA	HSTL reference clock input. V_{IN} = 2.0 V.
REFCLKN externally applied bias voltage (HSTL)	V_X	0.68	0.9	V	For HSTL, when driving REFCLKP, the REFCLKN input must be biased to this level.
Common-mode voltage (LVPECL)	V_{CM}	0.65	1.0	V	DC-coupled LVPECL inputs.
Single-ended input REFCLKP/N swing (LVPECL/CML)	ΔV_{IN_SE}	250	1200	mVp-p	CML, LVPECL reference clock input.
Differential input REFCLKP/N swing (LVPECL/CML)	ΔV_{IN_DIFF}	350	2400	mVp-p	CML, LVPECL reference clock input.

4.2.1 Two-Wire Serial Interface

The following table and illustration show the AC signal characteristics for the two-wire serial interface.

Table 53. Two-Wire Serial Interface AC Signal Characteristics

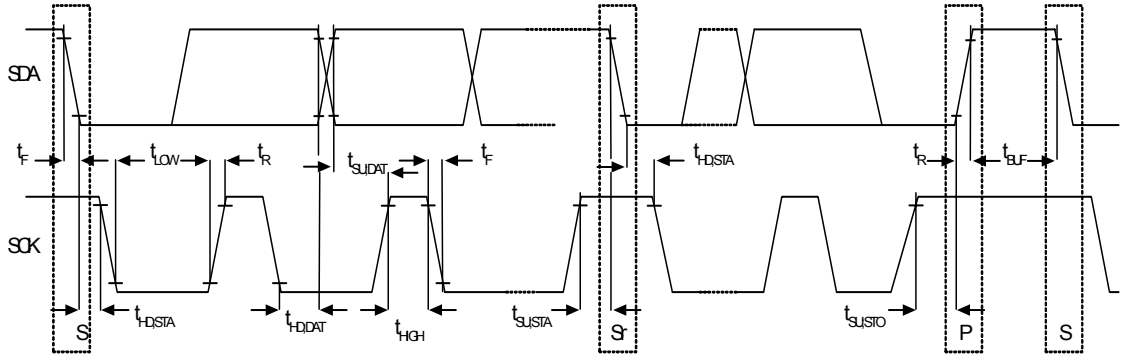
		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Serial clock frequency	F_{SCK}		100		400	kHz
Hold time START condition after this period, the first CLK pulse is generated	$t_{HD:STA}$	4.0		0.6		µs
Low period of SCK	t_{LOW}	4.7		1.3		µs
High period of SCK	t_{HIGH}	4.0		0.6		µs
Data hold time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data setup time	$t_{SU:DAT}$	250		100		ns
Rise time for SDA and SCK	t_R		1000		300	ns
Fall time for SDA and SCK	t_F		300		300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0		0.6		µs
Bus free time between a STOP and START	t_{BUF}	4.7		1.3		µs

Table 53. Two-Wire Serial Interface AC Signal Characteristics *(continued)*

		Standard		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Capacitive load for SCK and SDA bus line	C_B		400		330	pF
External pull-up resistor(1)	R_P	900	8×10^{-7} / CB	900	3×10^{-7} / CB	Ω

1. Minimum value determined from I_{OL} and internal reliability requirements. Maximum value determined by load capacitance. In general, 10 KΩ is recommended for the typical applications where capacitance loads are below the specified minimums

Figure 11. Two-Wire Serial Interface Timing



S=START, P=STOP, and Sr=repeated START.

4.2.2 Serial Peripheral Interface

The following table and illustration show the AC signal characteristics for the serial peripheral interface.

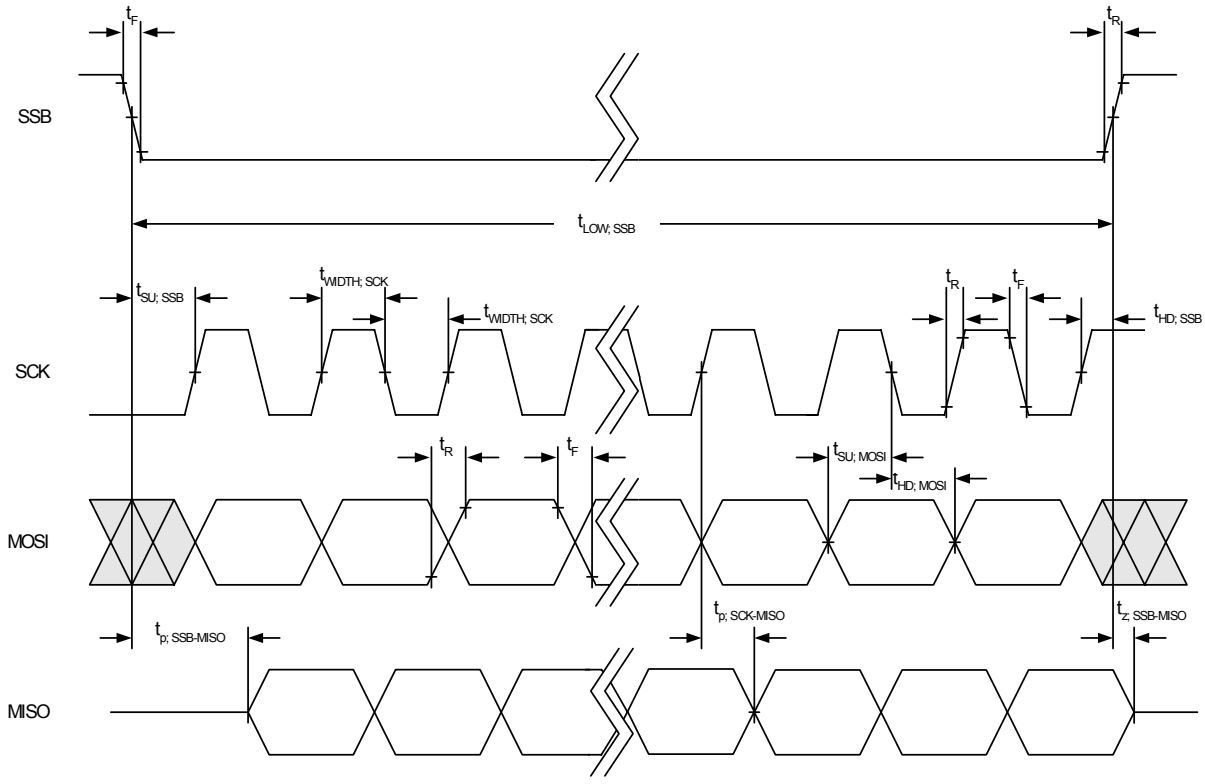
Table 54. Serial Peripheral Interface AC Signal Characteristics

Parameter	**Symbol**	**Minimum**	**Maximum**	**Unit**	**Condition**
Serial clock frequency	F_{SCK}		10	MHz	
Serial clock minimum pulse width	$t_{WIDTH:SCK}$	5		ns	
MOSI setup time to falling edge of SCK	$t_{SU:MOSI}$	3		ns	
MOSI hold time from falling edge of SCK	$t_{HD:MOSI}$	1		ns	
SSB setup time to rising edge of SCK	$t_{SU:SSB}$	1		ns	
SSB hold time from rising edge of SCK	$t_{HD:SSB}$	3		ns	

Table 54. Serial Peripheral Interface AC Signal Characteristics *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
SSB minimum pulse width	$T_{LOW:SSB}$	5		ns	
Rising edge of SCK to MISO propagation delay	$t_{P:SCK-MISO}$	1		ns	
Falling edge of SSB to active condition of MISO propagation delay	$t_{P:SSB-MISO}$	2		ns	
Rising edge of SSB to tri-state condition of MISO	$t_{Z:SSB-MISO}$		2	ns	
Rise time of all SPI input signals	t_R		5	ns	20% to 80%
Fall time of all SPI input signals	t_F		5	ns	20% to 80%
Capacitive load for each bus line	C_B		400	pF	

Figure 12. Serial Peripheral Interface Timing



4.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC8228-01 device.

Table 55. Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
1.2-V power supply voltage(1)	V_{DDTX12}, V_{DDRX12}, V_{DDA12}, V_{DDB12}	1.14	1.26	V
1.8-V power supply voltage(2)	V_{DDTX18}, V_{DDRX18}, V_{DDA18}, V_{DDB18}	1.62	1.98	V
1.2-V power supply voltage(1)	V_{DDIOTX}, V_{DDIORX}	1.14	1.26	V
1.8-V power supply voltage(2)	V_{DDIOTX}, V_{DDIORX}	1.62	1.98	V
1.2-V power supply voltage	V_{DDTTL}	1.14	1.26	V
1.8-V power supply voltage	V_{DDTTL}	1.62	1.98	V
2.5-V power supply voltage	V_{DDTTL}	2.25	2.75	V
3.3-V power supply voltage	V_{DDTTL}	2.97	3.63	V
Operating temperature(3)	T	–10	105	°C

1. When using only the 1.2-V power supply, 1.8-V power supply connections must also be connected to 1.2 V. See Table 12, page 28.
2. When using only the 1.8-V power supply, do not connect the 1.2-V power supply connections. Connect only VDDTX18, VDDRX18, VDDA18, VDDB18, VDDIOTX, and VDDIORX. Connect 1.2-V connections to a bypass capacitor. See Table 12, page 28.
3. Lower limit of specification is ambient temperature, and upper limit is case temperature.

4.4 Stress Ratings

This section contains the stress ratings for the VSC8228-01 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 56. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
1.2-V power supply voltage(1)	V_{DDTX12}, V_{DDRX12}, V_{DDA12}, V_{DDB12}	–0.5	2.0	V
1.8-V power supply voltage(2)	V_{DDTX18}, V_{DDRX18}, V_{DDA18}, V_{DDB18}	–0.5	2.2	V
V_{DDTTL} voltage	V_{DDTTL}	–0.5	5.5	V
1.2-V or 1.8-V power supply voltage	V_{DDIOTX}, V_{DDIORX}	–0.5	2.2	V
CML DC input voltage		–0.5	V_{DD} + 0.5	V
LVTTL DC input voltage		–0.5	5.5	V
DC voltage applied to LVTTL outputs		–0.5	V_{DDTTL} + 0.5	V
Storage temperature	T_S	–65	150	°C

Table 56. Stress Ratings *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–750	750	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note(3)		V

1. When using only the 1.2 V-power supply, 1.8-V power supply connections must also be connected to 1.2 V. For more information, see Table 12, page 28.
2. When using only the 1.8-V power supply, do not connect the 1.2-V power supply connections. Connect only V_{DDTX18}, V_{DDRX18}, V_{DDA18}, V_{DDB18}, V_{DDIOTX}, and V_{DDIORX}. Also connect 1.2-V connections to a bypass capacitor. For more information, see Table 12, page 28.
3. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

4.5 Power Sequencing

Power sequencing is not required for the VSC8228-01 device. However, the time from the first power supply to the last power supply coming on line should be less than 500 ms.

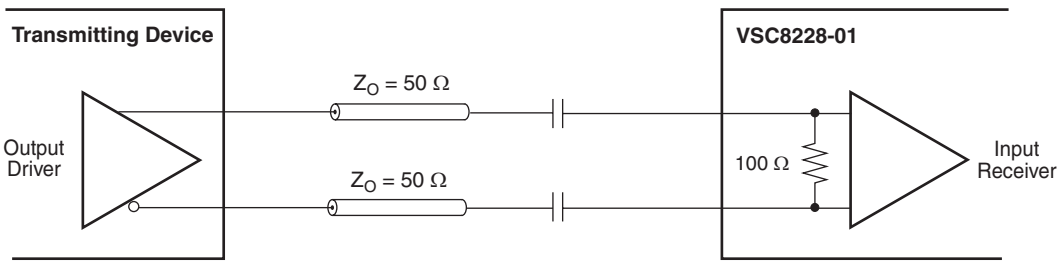
4.6 Termination for Input and Output

The following sections provide information and illustrations for input and output termination.

4.6.1 CML/LVDS Input

There is a 100-Ω resistor inside the input buffer for termination of the AC-coupled transmission lines. The DC biasing level of the input is set by the internal circuit of the device and no external resistor is needed.

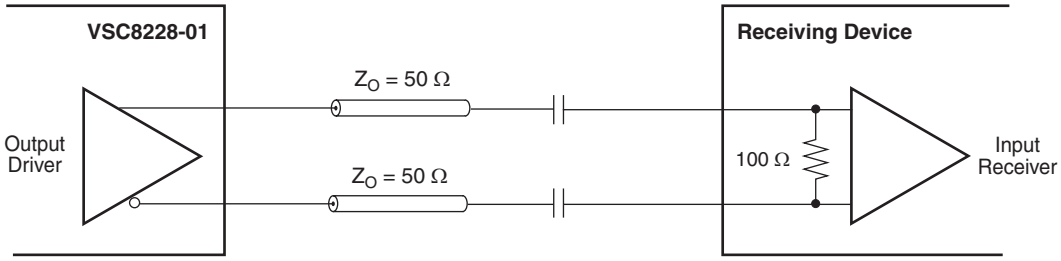
Figure 13. CML/LVDS Inputs Terminated by an Internal 100-Ohm Resistor



4.6.2 CML/LVDS Output

When V_{DDIO} = 1.8 V, no pull-up inductor is needed at the output. The output impedance is 50 Ω.

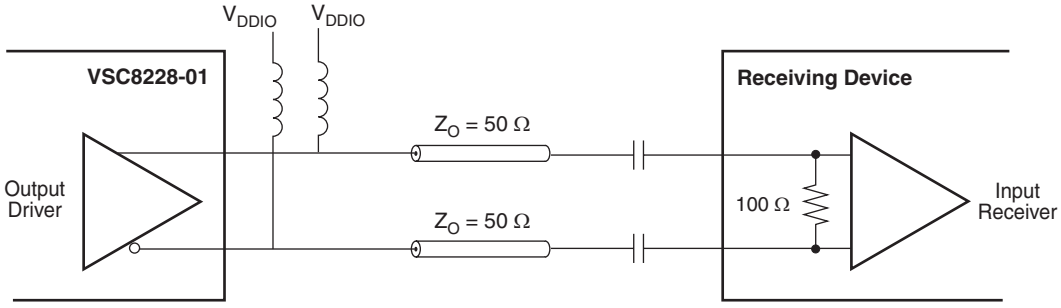
Figure 14. No Pull-Up Inductor Needed for 1.8-V CML/LVDS Output



Note: When the receiving device has no internal termination, a 100-Ω termination resistor must be inside the receiving device; however, when the receiving device has internal termination, do not add a termination resitor.

When V_{DDIO} = 1.2 V, an optional pull-up inductor at each of the differential output lines can be added to boost the output swing. These pull-up inductors should be placed close to the driver.

Figure 15. Optional Pull-Up Inductor for 1.2-V CML/LVDS Output



Note: When the receiving device has no internal termination, a 100-Ω termination resistor must be inside the receiving device; however, when the receiving device has internal termination, do not add a termination resitor.

4.6.3 REFCLK Input

The following illustrations show the LVPECL differential for DC-coupled and AC-coupled transmission lines.

Figure 16. LVPECL Differential - DC Coupled

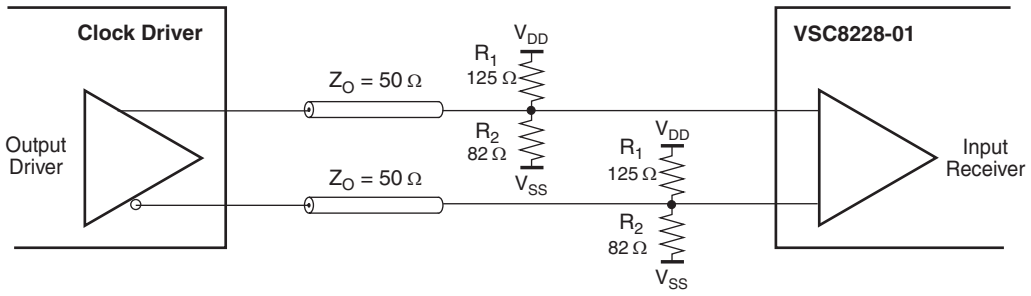
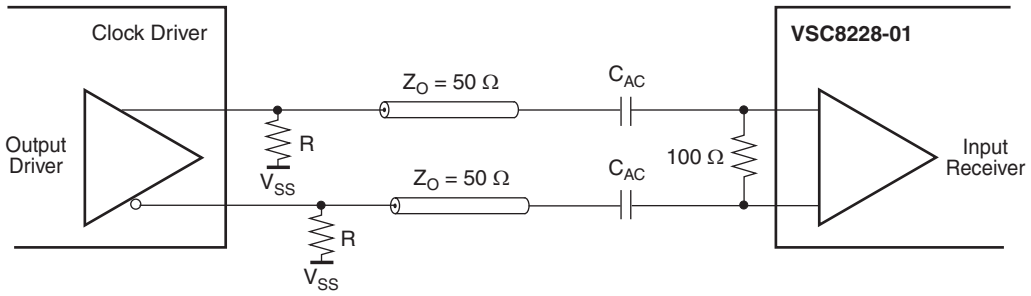


Figure 17. LVPECL Differential - AC Coupled



Note: Consult the clock driver specifications for the R value.

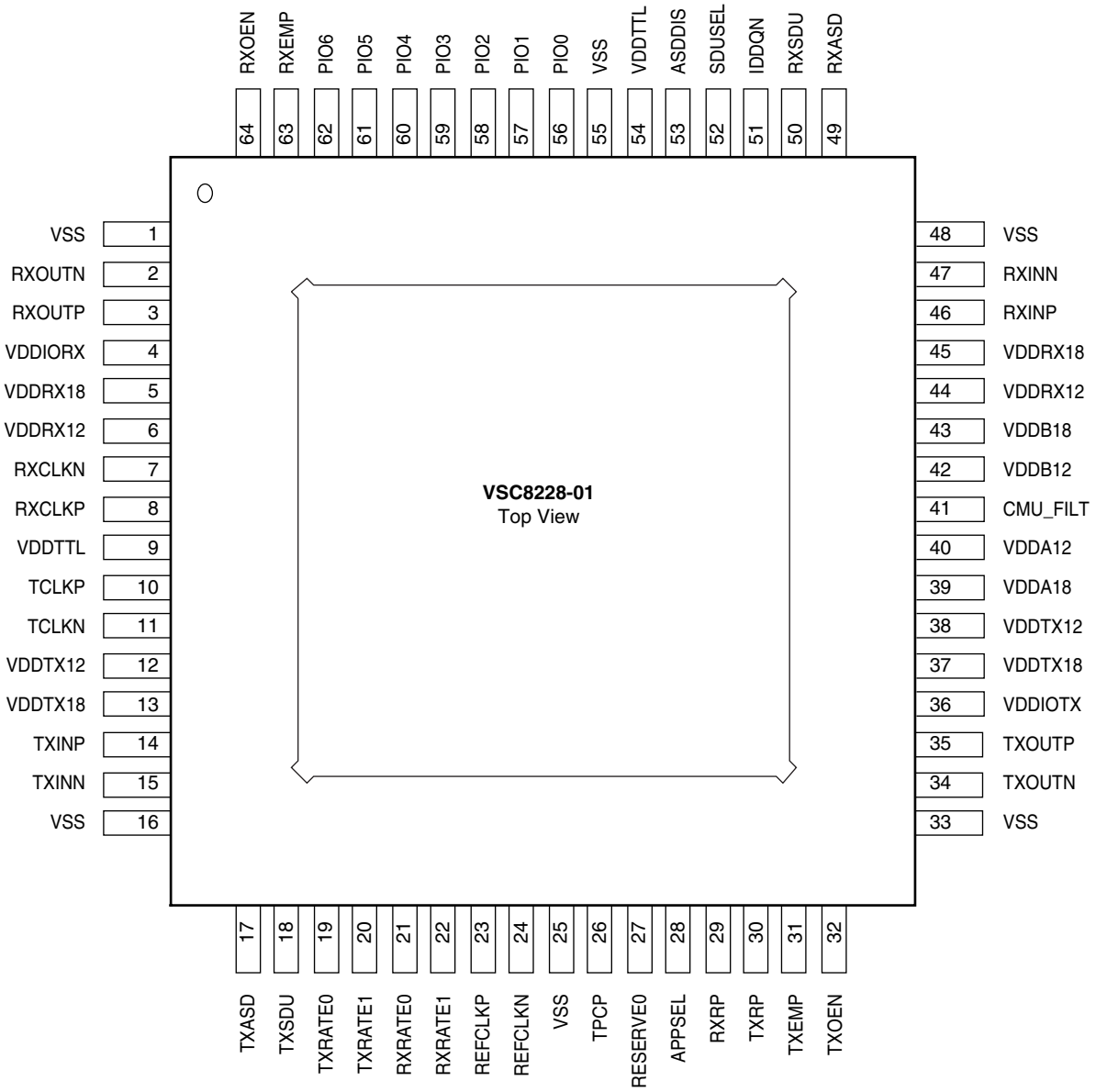
5 Pin Descriptions

This section provides the pin diagram and descriptions for the VSC8228-01 device.

5.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8228-01 device. Note that the electrical connection of the exposed paddle at the bottom of the device can be grounded or floated.

Figure 18. Pin Diagram



5.2 Pin Identifications

This section contains the pin descriptions for the VSC8228-01 device.

Table 57. Pin Identifications

Pin Number	Signal Name	I/O	Level	Description
1	VSS		Power	Ground.
2	RXOUTN	O	CML/LVDS	High-speed host-side receiver channel output, complement.
3	RXOUTP	O	CML/LVDS	High-speed host-side receiver channel output, true.
4	VDDIORX		Power	1.8 V or 1.2 V power supply voltage for receiver outputs.
5	VDDRX18		Power	1.8 V power supply voltage for receiver.
6	VDDRX12		Power	1.2 V power supply voltage for receiver.
7	RXCLKN	O	SGMII	Receiver clock output, complement.
8	RXCLKP	O	SGMII	Receiver clock output, true.
9	VDDTTL		Power	1.2 V, 1.8 V, 2.5 V, or 3.3 V power supply for TTL I/O.
10	TCLKP	O	CML/LVDS	Reserved. Leave unconnected.
11	TCLKN	O	CML/LVDS	Reserved. Leave unconnected.
12	VDDTX12		Power	1.2 V input power supply voltage for transmitter.
13	VDDTX18		Power	1.8 V input power supply voltage for transmitter.
14	TXINP	I	CML/LVDS	High-speed host-side transmitter channel input, true.
15	TXINN	I	CML/LVDS	High-speed host-side transmitter channel input, complement.
16	VSS		Power	Ground.
17	TXASD	O	LVTTL	Transmitter channel analog signal detect. HIGH indicates analog signal detected.
18	TXSDU	O	LVTTL	Transmitter protocol and analog signal detect. HIGH indicates analog signal detected and no protocol violation.
19	TXRATE0	I	LVTTL	Transmitter rate control 0.
20	TXRATE1	I	LVTTL	Transmitter rate control 1.
21	RXRATE0	I	LVTTL	Receiver rate control 0.
22	RXRATE1	I	LVTTL	Receiver rate control 1.
23	REFCLKP	I	LVTTL/LVPECL	Low-speed reference clock input, true.
24	REFCLKN	I	LVTTL/LVPECL	Low-speed reference clock input, complement.
25	VSS		Power	Ground.
26	TPCP	I	LVTTL	Vitesse use only. Leave unconnected.
27	RESERVE0			Reserved.
28	APPSEL	I	LVTTL	Application select. Application select. For information about setting the operating frequency from 106.25 MHz and 125 MHz, see Table 6, page 20.
29	RXRP	I	LVTTL	Receiver channel repeater select. HIGH selects repeater. LOW selects retimer.
30	TXRP	I	LVTTL	Transmitter channel repeater select. HIGH selects repeater. LOW selects retimer.

Table 57. Pin Identifications *(continued)*

Pin Number	Signal Name	I/O	Level	Description
31	TXEMP	I	LVTTL	Transmitter channel de-emphasis. LOW disables de-emphasis. HIGH enables de-emphasis.
32	TXOEN	I	LVTTL	Transmit channel output enable.
33	VSS		Power	Ground.
34	TXOUTN	O	CML/LVDS	High-speed line-side transmitter channel output, complement.
35	TXOUTP	O	CML/LVDS	High-speed line-side transmitter channel output, true.
36	VDDIOTX		Power	1.8 V or 1.2 V power supply voltage for transmitter outputs.
37	VDDTX18		Power	1.8 V power supply voltage for transmitter.
38	VDDTX12		Power	1.2 V power supply voltage for transmitter.
39	VDDA18		Power	1.8 V power supply voltage for CMU.
40	VDDA12		Power	1.2 V power supply voltage for CMU.
41	CMU_FILT		Analog	Connect to external CMU capacitor.
42	VDDB12		Power	1.2 V power supply voltage for serial interface and test block.
43	VDDB18		Power	1.8 V power supply voltage for serial interface and test block.
44	VDDRX12		Power	1.2 V power supply voltage for receiver.
45	VDDRX18		Power	1.8 V power supply voltage for receiver.
46	RXINP	I	CML/LVDS	High-speed line-side receiver channel input, true.
47	RXINN	I	CML/LVDS	High-speed line-side receiver channel input, complement.
48	VSS		Power	Ground.
49	RXASD	O	LVTTL	Receiver channel analog signal detect. HIGH indicates analog signal detected.
50	RXSDU	O	LVTTL	Receiver protocol and analog signal detect. HIGH indicates analog signal detected and no protocol violation.
51	IDDQN	I	LVTTL	Vitesse use only. Leave unconnected.
52	SDUSEL	I	LVTTL	Multiframe or single-frame error mode.
53	ASDDIS	I	LVTTL	Analog signal detect disable.
54	VDDTTL		Power	1.2 V, 1.8 V, 2.5 V, or 3.3 V power supply for TTL I/O.
55	VSS		Power	Ground.
56	PIO0	I/O	LVTTL input or open-drain output	Serial interface port, pin 0.
57	PIO1	I	LVTTL	Serial interface port, pin 1.
58	PIO2	I/O	LVTTL input or open-drain output	Serial interface port, pin 2.
59	PIO3	I	LVTTL	Serial interface port, pin 3.
60	PIO4	I	LVTTL	Serial interface port, pin 4.

Table 57. Pin Identifications *(continued)*

Pin Number	Signal Name	I/O	Level	Description
61	PIO5	I	LVTTL	Serial interface port, pin 5.
62	PIO6	I	LVTTL	Serial interface port, pin 6.
63	RXEMP	I	LVTTL	Receiver channel de-emphasis. LOW disables de-emphasis. HIGH enables de-emphasis.
64	RXOEN	I	LVTTL	Receiver channel output enable.

6 Package Information

The VSC8228-01 device is available in two package types. VSC8228RC-01 is a 64-pin, plastic thin quad flat package (TQFP) with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, 0.5 mm pitch, and 1.2 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8228XRC-01.

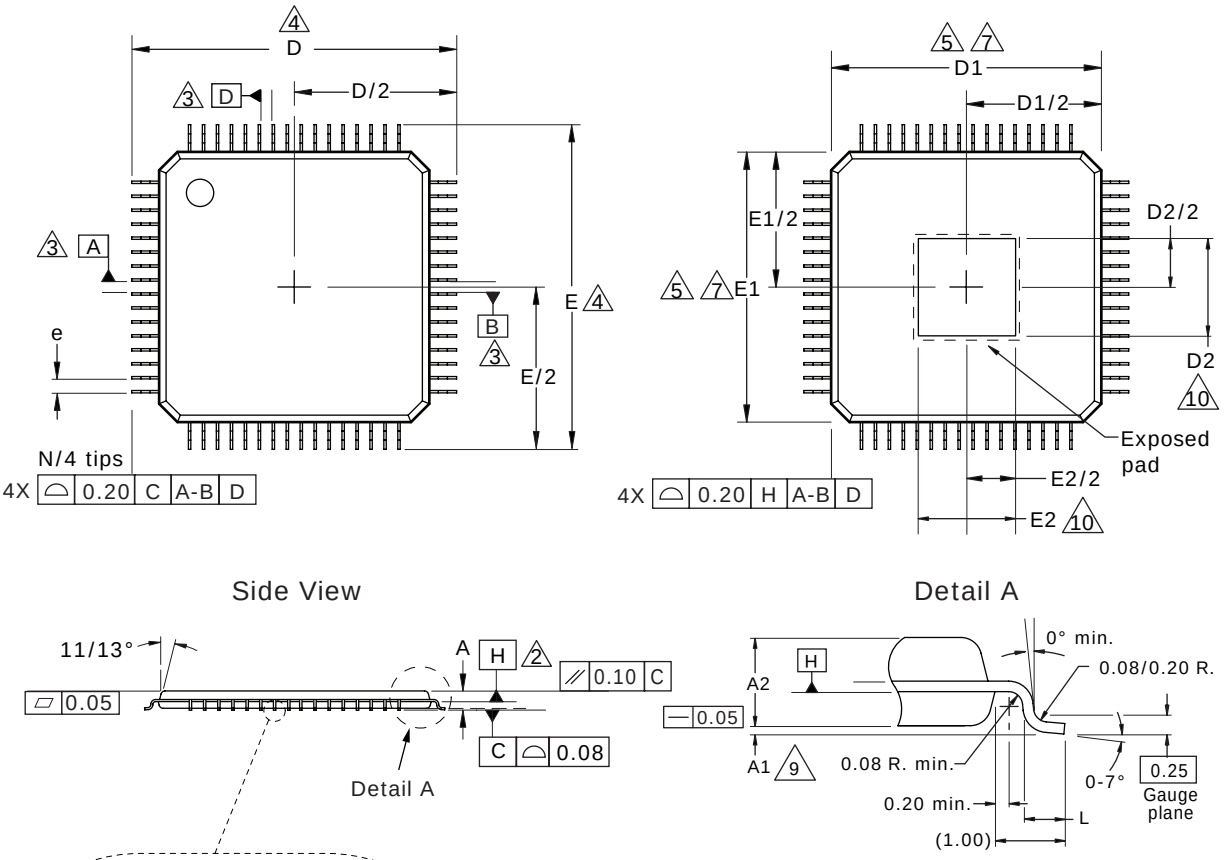
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8228-01 device.

6.1 Package Drawing

The following illustration shows the package drawing for the VSC8228-01 device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

Figure 19. Package Drawing



Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
L	0.45	0.60	0.75
N		64	
e		0.50	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23

Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Datum plane H is located at the mold parting line and is coincident with the lead, where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and D to be determined at the centerline between leads, where leads exit the plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
6. N is the total number of leads.
7. These dimensions to be determined at datum plane H.
8. This outline conforms to JEDEC publication 95 registration MS-026.
9. A1 is defined as the distance from the seating plane to the lowest point of the package body.
10. Dimensions D2 and E2 represent the size of the exposed pad, which is 2.93 mm × 2.93 mm typical.

6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 58. Thermal Resistances

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC8228RC-01	23.1(1) 4.5(2)	20.7	43.8	40.5	37.1
VSC8228XRC-01	23.1(1) 4.5(2)	20.7	43.8	40.5	37.1

1. Case temperature on the top of the mold compound with the exposed pad soldered to a ground pad on the PCB.
2. Case temperature on the exposed pad soldered to a ground pad on the PCB.

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

7 Ordering Information

The VSC8228-01 device is available in two package types. VSC8228RC-01 is a 64-pin, plastic thin quad flat package (TQFP) with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, 0.5 mm pitch, and 1.2 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8228XRC-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8228-01 device.

Table 59. Ordering Information

Part Order Number	Description
VSC8228RC-01	64-pin, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, 0.5 mm pitch, and 1.2 mm maximum height
VSC8228XRC-01	Lead(Pb)-free, 64-pin, plastic TQFP with an exposed pad, 10 mm × 10 mm body size, 1 mm body thickness, 0.5 mm pitch, and 1.2 mm maximum height