USB5807C

7-Port USB 3.2 Gen 1 SmartHub™ IC

Highlights

- USB Hub with 7 USB 3.1 Gen 1 / USB 2.0 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- **FlexConnect:** Downstream port able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- (TID 1595) USB-IF certified, supporting latest Engineering Change Notices for compliance with USB-IF logo testing for new USB Type-C® industry initiative (Revision C or newer only)
  - Header Packet Timer (TD7.9, TD7.11, TD7.26)
  - Power Management Timer (TD7.18, TD7.20, TD7.23)
  - Unacknowledged Connect and Remote Wake Test Failure (TD10.25)
- Available in 100-pin (12mm x 12mm) VQFN RoHS compliant package
- Commercial and industrial grade temperature support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.2 Gen 1 Peripherals

Key Benefits

- USB 3.2 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
  - 5V tolerant USB 2.0 pins
  - 1.32V tolerant USB 3.2 Gen 1 pins
  - Integrated termination and pull-up/down resistors
- Supports battery charging of most popular battery powered devices on all ports
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - European Union universal mobile charger support
  - Support for Microchip UCS100x family of battery charging controllers
  - Supports additional portable devices
- Smart port controller operation
  - Firmware handling of companion port power controllers
- On-chip microcontroller
  - manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One-Time-Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **FlexConnect**
  - Reversible upstream and downstream Port 1 roles on command
- **PortSwap**
  - Configurable USB 2.0 differential pair signal swap
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
  - USB 2.0 Hi-Speed disconnect threshold adjust (Revision C or newer only)
- **VariSense™**
  - Programmable USB receive sensitivity
- **Port Split**
  - USB2.0 and USB3.1 Gen1 port operation can be split for custom applications using embedded USB3.x devices in parallel with USB2.0 devices.
- Compatible with Microsoft Windows 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
  - 100-pin VQFN (12mm x 12mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Revision 3.2 Specification*, http://www.usb.org/developers/docs/
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5807C hub is a low-power, OEM configurable, USB 3.2 Gen 1 hub controller with 7 downstream ports and advanced features for embedded USB applications. The USB5807C is fully compliant with the Universal Serial Bus Revision 3.1 Specification and USB 2.0 Link Power Management Addendum. The USB5807C supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5807C supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of five generations of Microchip hub controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 hub controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB5807C enables OEMs to configure their system using “Configuration Straps.” These straps simplify the configuration process, assigning default values to USB 3.2 Gen 1 ports and GPIOs. OEMs can disable ports, enable battery charging, and define GPIO functions as default assignments on power-up, removing the need for OTP or external SPI ROM.

The USB5807C supports downstream battery charging via the integrated battery charger detection circuitry, which supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5807C provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

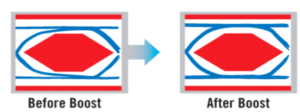
- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

Additionally, the USB5807C includes many powerful and unique features such as:

FlexConnect, which provides flexible connectivity options. One of the USB5807C’s downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



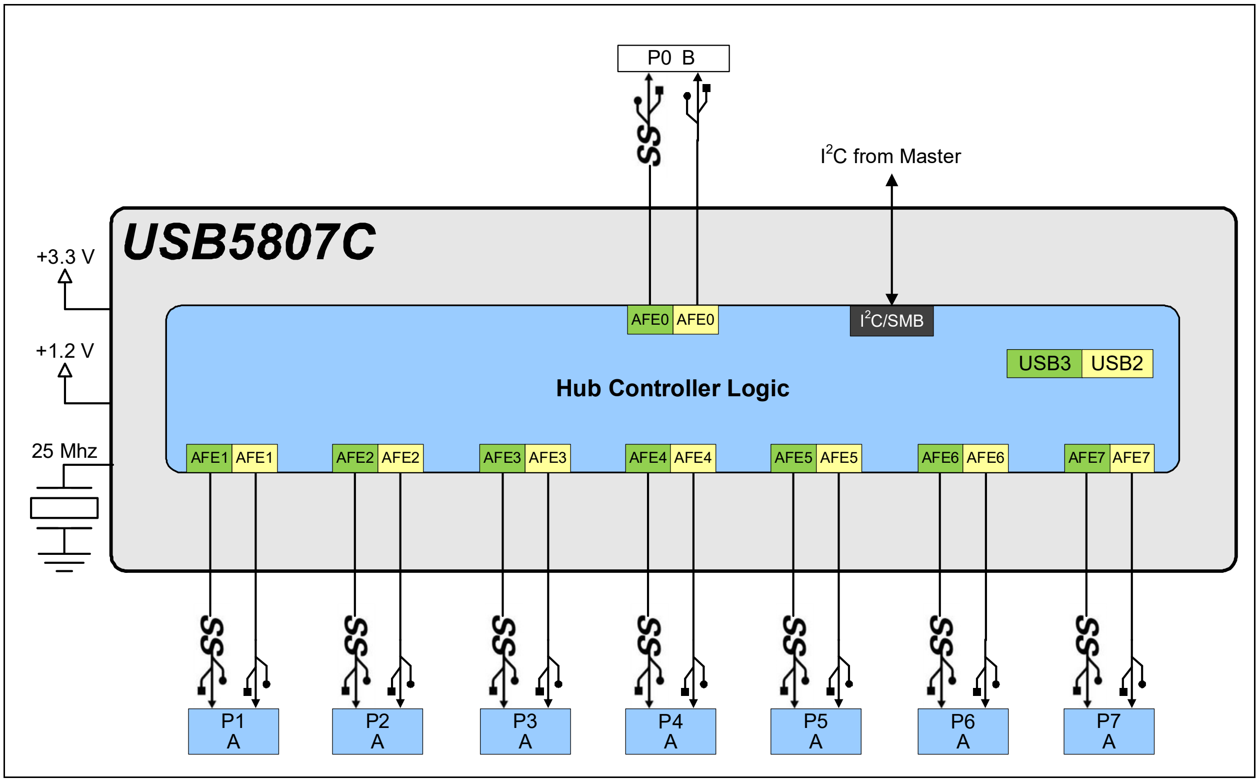
VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

Port Split, which allows for the USB3.1 Gen1 and USB2.0 portions of downstream ports 5 and 6 to operate independently and enumerate two separate devices in parallel in special applications.

The USB5807C can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5807C is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB5807C is shown in Figure 2-1.

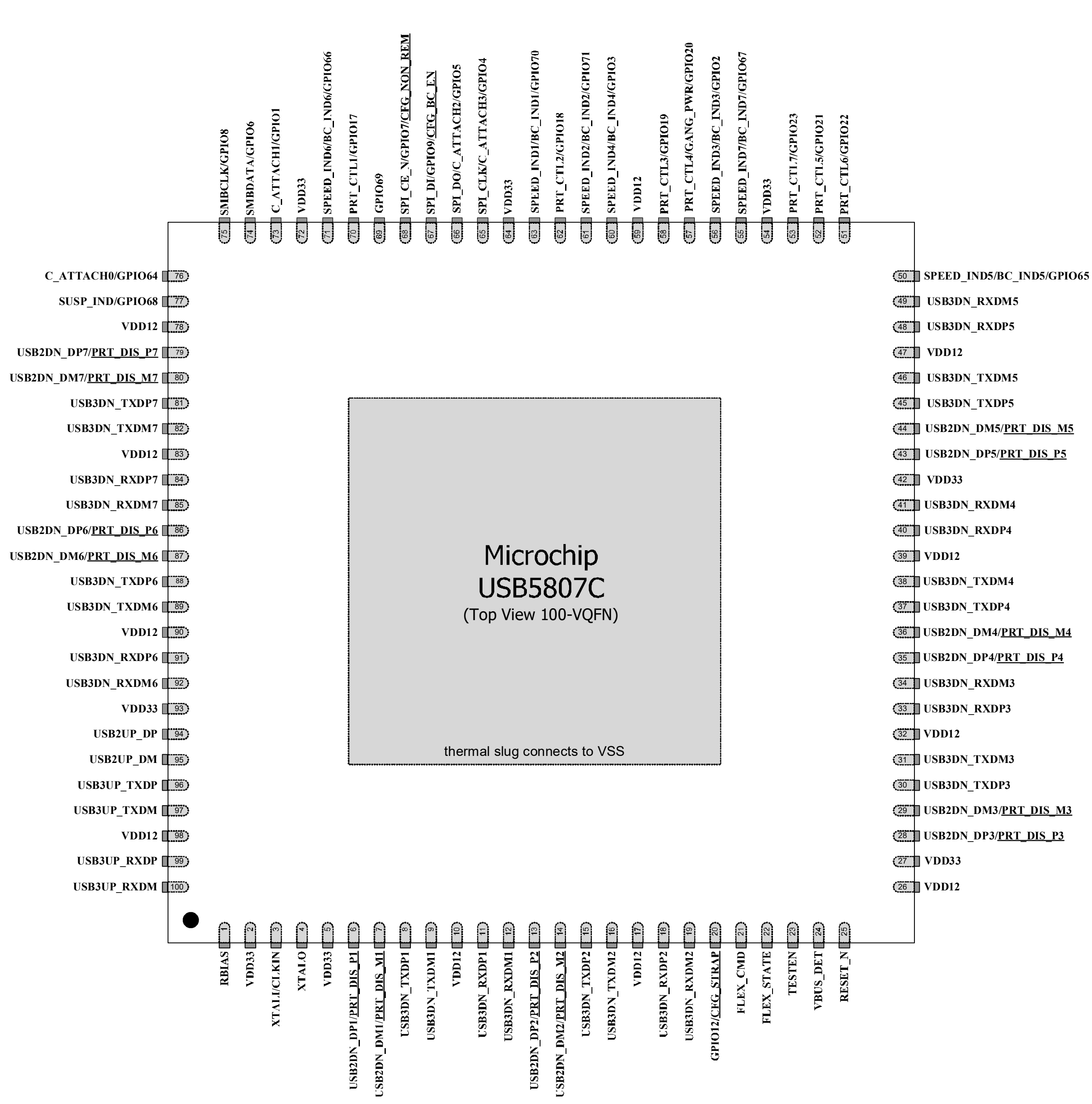
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS

3.1 Pin Diagram

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.5, Configuration Straps and Programmable Functions

3.2 Pin Symbols

Pin Num.	Pin Name	Reset	Pin Num.	Pin Name	Reset
1	RBIAS	A/P	51	PRT_CTL6/GPIO22	PD-50k
2	VDD33	A/P	52	PRT_CTL5/GPIO21	PD-50k
3	XTALI/CLKIN	A/P	53	PRT_CTL7/GPIO23	PD-50k
4	XTALO	A/P	54	VDD33	A/P
5	VDD33	A/P	55	SPEED_IND7/BC_IND7/GPIO67	Z
6	USB2DN_DP1/PRT_DIS_P1	PD-15k	56	SPEED_IND3/BC_IND3/GPIO2	Z
7	USB2DN_DM1/PRT_DIS_M1	PD-15k	57	PRT_CTL4/GANG_PWR/GPIO20	PD-50k
8	USB3DN_TXDP1	Z	58	PRT_CTL3/GPIO19	PD-50k
9	USB3DN_TXDM1	Z	59	VDD12	A/P
10	VDD12	A/P	60	SPEED_IND4/BC_IND4/GPIO3	Z
11	USB3DN_RXDP1	Z	61	SPEED_IND2/BC_IND2/GPIO71	Z
12	USB3DN_RXDM1	Z	62	PRT_CTL2/GPIO18	PD-50k
13	USB2DN_DP2/PRT_DIS_P2	PD-15k	63	SPEED_IND1/BC_IND1/GPIO70	Z
14	USB2DN_DM2/PRT_DIS_M2	PD-15k	64	VDD33	A/P
15	USB3DN_TXDP2	Z	65	SPI_CLK/C_ATTACH3/GPIO4	Z
16	USB3DN_TXDM2	Z	66	SPI_DO/C_ATTACH2/GPIO5	PD-50k
17	VDD12	A/P	67	SPI_DI/GPIO9/CFG_BC_EN	Z
18	USB3DN_RXDP2	Z	68	SPI_CE_N/GPIO7/CFG_NON_REM	PU-50k
19	USB3DN_RXDM2	Z	69	GPIO69	Z
20	GPIO12/CFG_STRAP	Z	70	PRT_CTL1/GPIO17	PD-50k
21	FLEX_CMD	Z	71	SPEED_IND6/BC_IND6/GPIO66	Z
22	FLEX_STATE	Z	72	VDD33	A/P
23	TESTEN	Z	73	C_ATTACH1/GPIO1	Z
24	VBUS_DET	Z	74	SMBDATA/GPIO6	Z
25	RESET_N	R	75	SMBCLK/GPIO8	Z
26	VDD12	A/P	76	C_ATTACH0/GPIO64	Z
27	VDD33	A/P	77	SUSP_IND/GPIO68	Z
28	USB2DN_DP3/PRT_DIS_P3	PD-15k	78	VDD12	A/P
29	USB2DN_DM3/PRT_DIS_M3	PD-15k	79	USB2DN_DP7/PRT_DIS_P7	PD-15k
30	USB3DN_TXDP3	Z	80	USB2DN_DM7/PRT_DIS_M7	PD-15k
31	USB3DN_TXDM3	Z	81	USB3DN_TXDP7	Z
32	VDD12	A/P	82	USB3DN_TXDM7	Z
33	USB3DN_RXDP3	Z	83	VDD12	A/P
34	USB3DN_RXDM3	Z	84	USB3DN_RXDP7	Z
35	USB2DN_DP4/PRT_DIS_P4	PD-15k	85	USB3DN_RXDM7	Z
36	USB2DN_DM4/PRT_DIS_M4	PD-15k	86	USB2DN_DP6/PRT_DIS_P6	PD-15k
37	USB3DN_TXDP4	Z	87	USB2DN_DM6/PRT_DIS_M6	PD-15k
38	USB3DN_TXDM4	Z	88	USB3DN_TXDP6	Z
39	VDD12	A/P	89	USB3DN_TXDM6	Z
40	USB3DN_RXDP4	Z	90	VDD12	A/P
41	USB3DN_RXDM4	Z	91	USB3DN_RXDP6	Z
42	VDD33	A/P	92	USB3DN_RXDM6	Z
43	USB2DN_DP5/PRT_DIS_P5	PD-15k	93	VDD33	A/P
44	USB2DN_DM5/PRT_DIS_M5	PD-15k	94	USB2UP_DP	PD-1M
45	USB3DN_TXDP5	Z	95	USB2UP_DM	PD-1M
46	USB3DN_TXDM5	Z	96	USB3UP_TXDP	Z
47	VDD12	A/P	97	USB3UP_TXDM	Z
48	USB3DN_RXDP5	Z	98	VDD12	A/P
49	USB3DN_RXDM5	Z	99	USB3UP_RXDP	Z
50	SPEED_IND5/BC_IND5/GPIO65	Z	100	USB3UP_RXDM	Z

The pin reset state definitions are detailed in Table 3-1.

TABLE 3-1: PIN RESET STATE LEGEND

Symbol	Description
A/P	Analog/Power Input
R	Reset Control Input
Z	Hardware disables output driver (high impedance)
PU-50k	Hardware enables internal 50kΩ pull-up
PD-50k	Hardware enables internal 50kΩ pull-down
PD-15k	Hardware enables internal 15kΩ pull-down
PD-1M	Hardware enables internal 1M pull-down

3.3 USB5926C Pin Descriptions

This section contains descriptions of the various USB5807 pins. The pin descriptions have been broken into functional groups as follows:

- USB 3.2 Gen 1 Pin Descriptions
- USB 2.0 Pin Descriptions
- Port Control Pin Descriptions
- SPI Interface
- USB Type-C Connector Controls
- Miscellaneous Pin Descriptions
- Configuration Strap Pin Descriptions
- Power and Ground Pin Descriptions

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-2: USB 3.2 GEN 1 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.2 Gen 1 Upstream D+ TX	USB3UP_TXDP	I/O-U	Upstream USB 3.2 Gen 1 Transmit Data Plus
USB 3.2 Gen 1 Upstream D- TX	USB3UP_TXDM	I/O-U	Upstream USB 3.2 Gen 1 Transmit Data Minus
USB 3.2 Gen 1 Upstream D+ RX	USB3UP_RXDP	I/O-U	Upstream USB 3.2 Gen 1 Receive Data Plus
USB 3.2 Gen 1 Upstream D- RX	USB3UP_RXDM	I/O-U	Upstream USB 3.2 Gen 1 Receive Data Minus

TABLE 3-2: USB 3.2 GEN 1 PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB 3.2 Gen 1 Ports 7-1 D+ TX	**USB3DN_TXDP[7:1]**	I/O-U	Downstream Super Speed Transmit Data Plus, ports 7 through 1.
USB 3.2 Gen 1 Ports 7-1 D- TX	**USB3DN_TXDM[7:1]**	I/O-U	Downstream Super Speed Transmit Data Minus, ports 7 through 1.
USB 3.2 Gen 1 Ports 7-1 D+ RX	**USB3DN_RXDP[7:1]**	I/O-U	Downstream Super Speed Receive Data Plus, ports 7 through 1.
USB 3.2 Gen 1 Ports 7-1 D- RX	**USB3DN_RXDM[7:1]**	I/O-U	Downstream Super Speed Receive Data Minus, ports 7 through 1.

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 2.0 Upstream D+	**USB2UP_DP**	I/O-U	Upstream USB 2.0 Data Plus (D+)
USB 2.0 Upstream D-	**USB2UP_DM**	I/O-U	Upstream USB 2.0 Data Minus (D-)
USB 2.0 Ports 7 D+	**USB2DN_DP[7:1]**	I/O-U	Downstream USB 2.0 Ports 7-1 Data Plus (D+)
USB 2.0 Ports 7 D-	**USB2DN_DM[7:1]**	I/O-U	Downstream USB 2.0 Ports 7-1 Data Minus (D-)
VBUS Detect	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Port 7 Power Enable / Overcurrent Sense	**PRT_CTL7**	I/OD12 (PU)	Port 7 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 7. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 6 Power Enable / Overcurrent Sense	**PRT_CTL6**	I/OD12 (PU)	Port 6 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 6. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 5 Power Enable / Overcurrent Sense	**PRT_CTL5**	I/OD12 (PU)	Port 5 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 4 Power Enable / Overcurrent Sense	**PRT_CTL4**	I/OD12 (PU)	Port 4 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 3 Power Enable / Overcurrent Sense	**PRT_CTL3**	I/OD12 (PU)	Port 3 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 2 Power Enable / Overcurrent Sense	**PRT_CTL2**	I/OD12 (PU)	Port 2 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 1 Power Enable / Overcurrent Sense	**PRT_CTL1**	I/OD12 (PU)	Port 1 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Gang Power	**GANG_PWR**	I	**GANG_PWR** becomes the port control (PRTCTL) pin for all downstream ports when the hub is configured for ganged port power control mode. All port power controllers should be controlled from this pin when the hub is configured for ganged port power mode.
FlexConnect Control	**FLEX_CMD**	I	FlexConnect control input. When low, the hub will operate in its default state. Port 0 is the upstream port and port 1 is a downstream port. When high, the hub will operate in its flexed state. Port 0 is a downstream port and port 1 is an upstream port.
FlexConnect Indicator	**FLEX_STATE**	O12	FlexConnect indicator output. Reflects the current state of FlexConnect. 0 = Hub is in default mode of operation 1 = Hub is in flexed mode of operation.

TABLE 3-5: SPI INTERFACE

Name	Symbol	Buffer Type	Description
SPI Chip Enable	**SPI_CE_N**	I/O12	This is the active low SPI chip enable output. If the SPI interface is enabled, this pin must be driven high in power-down states.
SPI Clock	**SPI_CLK**	I/O-U	This is the SPI clock out to the serial ROM. If the SPI interface is disabled, by setting the SPI_DIS-ABLE bit in the UTIL_CONFIG1 register, this pin becomes **GPIO4**. If the SPI interface is enabled this pin must be driven low during reset.
SPI Data Output	**SPI_DO**	I/O-U	SPI data output, when configured for SPI operation.
SPI Data Input	**SPI_DI**	I/O-U	SPI data input, when configured for SPI operation.

Note: If SPI memory device is not used, these pins may not be simply floated. These pins must be handled per their respective alternate pin functions descriptions (C_ATTACH2, C_ATTACH3, CFG_BC_EN, CFG_NON_REM).

TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS

Name	Symbol	Buffer Type	Description
USB Type-C Attach Control Input 0-3	**C_ATTACH[0:3]**	I (PD)	USB Type-C attach control input. This pin indicates to the hub when a valid USB Type-C attach has been detected. This pin is used by the hub to enable the USB 3.2 Gen 1 PHY when a Type-C connection is present. When there is no USB Type-C connection present, the USB 3.2 Gen 1 PHY is disabled to reduce power consumption. This pin behaves as follows: - 1: USB Type-C attach detected, turn respective USB 3.2 Gen 1 PHY on. - 0: No USB Type-C attach detected, turn respective USB 3.2 Gen 1 PHY off. When using legacy USB Type-A and Type-B connectors, pull these pins to 3.3V to permanently enable all USB 3.2 PHYs.

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
SMBus/I^{2}C Clock	**SMBCLK**	I/O12	SMBus/I^{2}C Clock The SMBus/I^{2}C interface acts as SMBus slave. For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.
SMBus/I^{2}C Data	**SMBDATA**	I/O12	SMBus/I^{2}C Data The SMBus/I^{2}C interface acts as SMBus slave. For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.
USB Port 7-1 Speed Indicator	**SPEED_IND[7:1]**	O12	USB Port Speed Indicator Indicates the connection speed of the respective port. Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.2 Gen 1
USB Port 7-1 Battery Charging Indicator	**BC_IND[7:1]**	O12	USB Battery Charging Indicator Indicates the connection speed of the respective port. Tri-state: Battery Charging not enabled 0: Battery Charging enabled and successful BC handshake has occurred. 1: Battery Charging enabled, but no BC handshake has occurred.
General Purpose I/O	**GPIO[1:9], GPIO12, GPIO[17:23], GPIO[64:71]**	I/O12 (PU/PD)	General Purpose Inputs/Outputs Refer to Section 3.5.5, General Purpose input/Output Configuration (GPIOx) for details.
USB 2.0 Suspend State Indicator	**SUSP_IND**	O12	USB 2.0 Suspend State Indicator **SUSP_IND** can be used as a sideband remote wakeup signal for the host when in USB 2.0 suspend.
Reset Control Input	**RESET_N**	IS	Reset Control Input This pin places the hub into Reset Mode when pulled low.
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close to the device as possible with a dedicated, low impedance connection to the GND plane.
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
External 25 MHz Reference Clock Input	**CLKIN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output
Test	**TESTEN**	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.

TABLE 3-8: CONFIGURATION STRAP PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Device Mode Configuration Strap	**CFG_STRAP**	I	Device Mode Configuration Strap. This configuration strap is used to set the device mode. Refer to Section 3.5.1, CFG_STRAP Configuration for details. See Note 2
Port 7-1 D+ Disable Configuration Strap	**PRT_DIS_P[7:1]**	I	Port 7-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[7:1]** straps to disable the related port (7-1). Refer to Section Section 3.5.2, Port Disable Configuration (PRT_DIS_P[7:1] / PRT_DIS_M[7:1]) for more information. See Note 2
Port 7-1 D- Disable Configuration Strap	**PRT_DIS_M[7:1]**	I	Port 7-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[7:1]** straps to disable the related port (7-1). Refer to Section 3.5.2, Port Disable Configuration (PRT_DIS_P[7:1] / PRT_DIS_M[7:1]) for more information. See Note 2
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Configuration strap to control number of reported non-removal ports. See Section 3.5.3, Non-Removable Port Configuration (CFG_NON_REM) See Note 2

TABLE 3-8: CONFIGURATION STRAP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Battery Charging Configuration Strap	CFG_BC_EN	I	Configuration strap to control number of BC 1.2 enabled downstream ports. See Section 3.5.4, Battery Charging Configuration (CFG_BC_EN) See Note 2

Note 2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.5, Configuration Straps and Programmable Functions for additional information.

TABLE 3-9: POWER AND GROUND PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
+3.3V Power Supply Input	VDD33	P	+3.3 V power and internal regulator input Refer to Section 4.1, Power Connections for power connection information
+1.2V Core Power Supply Input	VDD12	P	+1.2 V core power Refer to Section 4.1, Power Connections for power connection information.
Ground	GND	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.4 Buffer Type Descriptions

TABLE 3-10: USB5807 BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.

Note: Refer to Section 10.5, DC Specifications for individual buffer DC electrical characteristics.

3.5 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note:	The system designer must guarantee that configuration straps meet the timing requirements specified in Section 10.6.2, Power-On and Configuration Strap Timing and Section 10.6.3, Reset and Configuration Strap Timing. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.5.1 CFG_STRAP CONFIGURATION

The **CFG_STRAP** pin is used to place the hub into preset modes of operation. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up as shown in Table 3-11.

TABLE 3-11: CFG_STRAP RESISTOR ENCODING

CFG_STRAP Resistor Value	Config	Setting
200 kΩ Pull-Down	CONFIG1	**Speed Indicator Mode + SMBus Interface Disabled** The SMBus interface will be disabled. The following programmable pins will be re-purposed as USB Speed Indicator outputs: Pin 63: **SPEED_IND1** Pin 61: **SPEED_IND2** Pin 56: **SPEED_IND3** Pin 60: **SPEED_IND4** Pin 50: **SPEED_IND5** Pin 71: **SPEED_IND6** Pin 55: **SPEED_IND7** The **SPEED_INDx** pins operate in the following manner: Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.2 Gen 1

TABLE 3-11: CFG_STRAP RESISTOR ENCODING (CONTINUED)

CFG_STRAP Resistor Value	Config	Setting
200 kΩ Pull-Up	CONFIG2	**Speed Indicator Mode + SMBus Slave Mode** The SMBus interface will operate in Slave Mode for use with hub configuration. The following programmable pins will be re-purposed as USB Speed Indicator outputs: Pin 63: **SPEED_IND1** Pin 61: **SPEED_IND2** Pin 56: **SPEED_IND3** Pin 60: **SPEED_IND4** Pin 50: **SPEED_IND5** Pin 71: **SPEED_IND6** Pin 55: **SPEED_IND7** The **SPEED_INDx** pins operate in the following manner: Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.2 Gen 1
10 kΩ Pull-Down	CONFIG3	Unused, Reserved
10 kΩ Pull-Up	CONFIG4	Unused, Reserved
10 Ω Pull-Down	CONFIG5	**Battery Charging Indicator Mode** The following programmable pins will be re-purposed as USB Battery Charging Indicator outputs: Pin 63: **BC_IND1** Pin 61: **BC_IND2** Pin 56: **BC_IND3** Pin 60: **BC_IND4** Pin 50: **BC_IND5** Pin 71: **BC_IND6** Pin 55: **BC_IND7** The **BC_INDx** pins operate in the following manner: Tri-state: Battery Charging not enabled 0: Battery Charging enabled and successful BC handshake has occurred. 1: Battery Charging enabled, but no BC handshake has occurred.
10 Ω Pull-Up	CONFIG6	Unused, Reserved

3.5.2 PORT DISABLE CONFIGURATION (PRT_DIS_P[7:1] / PRT_DIS_M[7:1])

The **PRT_DIS_P[7:1]** and **PRT_DIS_M[7:1]** configuration straps are used in conjunction to disable the related port (7-1).

For **PRT_DIS_P*x*** (where *x* is the corresponding port 7-1):

- **0** = Port *x* D+ Enabled
- **1** = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 7-1):

- **0** = Port *x* D- Enabled
- **1** = Port *x* D- Disabled

Note:	Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where *x* is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.2 Gen 1 port.

3.5.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in Table 3-12.

TABLE 3-12: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable
10 kΩ Pull-Up	Port 1, 2, 3, non-removable
10 Ω Pull-Down	Port 1, 2, 3, 4 non-removable
10 Ω Pull-Up	Port 1, 2, 3, 4, 5, 6, 7 non-removable

3.5.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in Table 3-13.

TABLE 3-13: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3, battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging
10 Ω Pull-Up	Port 1, 2, 3, 4, 5, 6, 7 battery charging

3.5.5 GENERAL PURPOSE INPUT/OUTPUT CONFIGURATION (GPIO*x*)

General Purpose Inputs/Outputs may be used for application specific purposes. Any given GPIO may operate as an input or an output. Inputs can apply an internal 50kΩ pull-down or pull-up resistor. Outputs may drive low or drive high (3.3V). GPIOs may be configured and manipulated via SMBus.

3.5.5.1 SMBus configuration

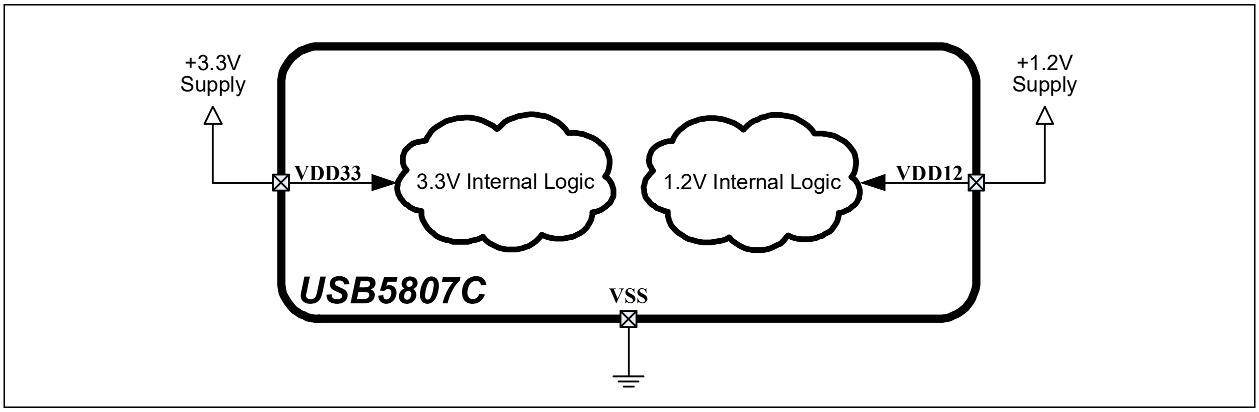
The SMBus slave interface may be used to write to internal registers that configure the state of the GPIO. Refer to the "Configuration Options for Microchip USB58xx and USB59xx Hubs" application note for additional details.

4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

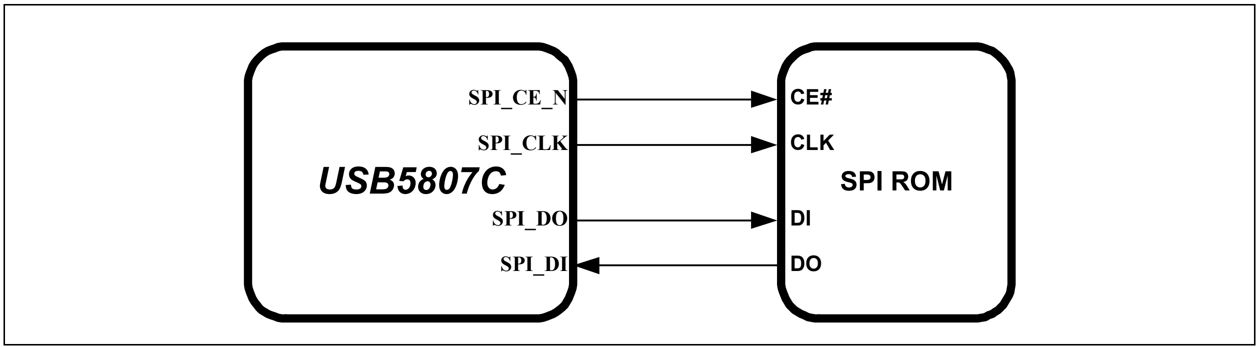
FIGURE 4-1: DEVICE POWER CONNECTIONS



4.2 SPI ROM Connections

Figure 4-2 illustrates the device SPI ROM connections. Refer to **Section 7.1 "SPI Master Interface"** for additional information on this device interface.

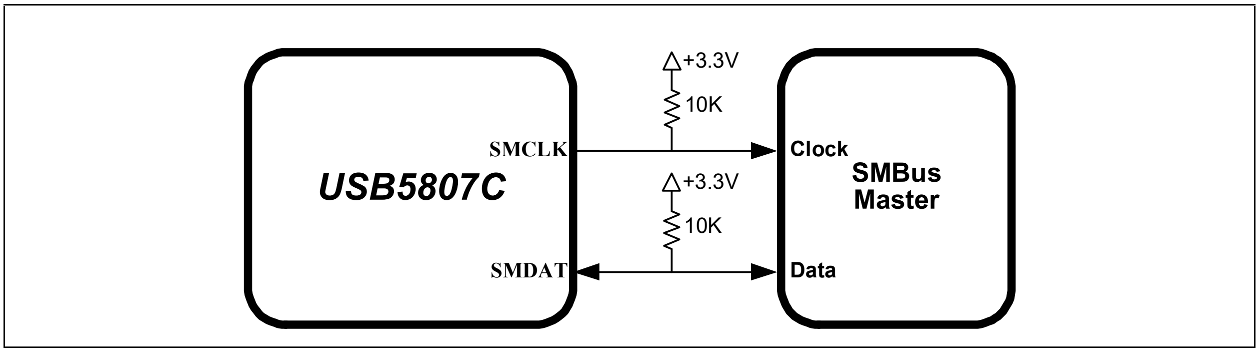
FIGURE 4-2: SPI ROM CONNECTIONS



4.3 SMBus Slave Connections

Figure 4-3 illustrates the device SMBus slave connections. Refer to **Section 7.2 "SMBus Slave Interface"** for additional information on this device interface.

FIGURE 4-3: SMBUS SLAVE CONNECTIONS



5.0 MODES OF OPERATION

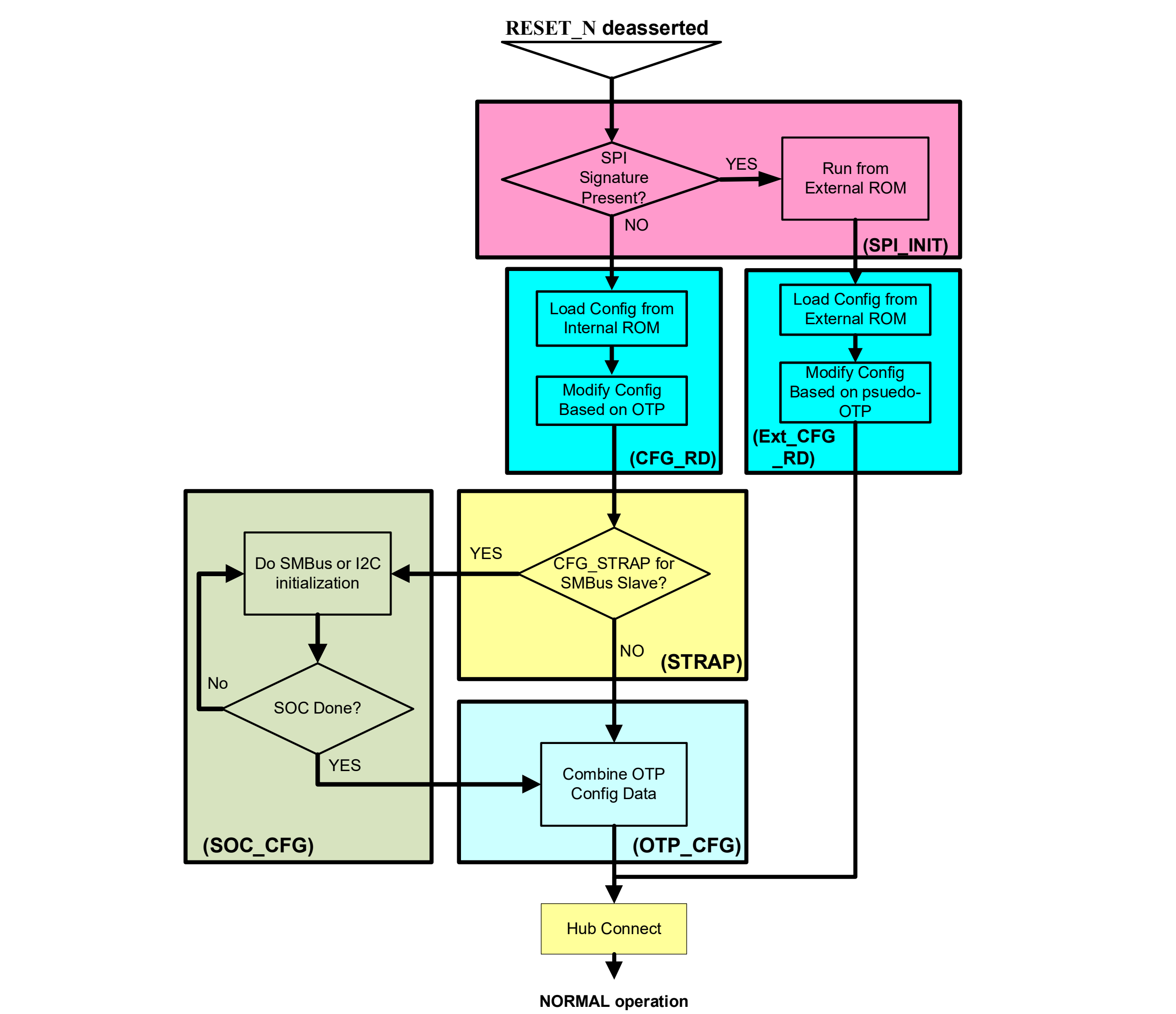
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the RESET_N pin, as shown in Table 5-1.

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	**Standby Mode**: This is the lowest power mode of the device. No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.4.2, External Chip Reset (RESET_N) for additional information on RESET_N.
1	**Hub (Normal) Mode**: The device operates as a configurable USB hub with battery charger detection. This mode has various sub-modes of operation, as detailed in Figure 5-1. Power consumption is based on the number of active ports, their speed, and amount of data transferred.

The flowchart in Figure 5-1 details the modes of operation and how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB BOOT FLOWCHART



5.1 Standby Mode

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.2 SPI Initialization Stage (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_RD stage).

When using an external SPI ROM, a 1 Mbit, 60 MHz or faster ROM must be used. Both 1- and 2-bit SPI operation are supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMs are also supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_RD stage).

5.3 Configuration Read Stage (CFG_RD)

In this stage, the internal firmware loads the default values from the internal ROM and then uses the configuration strapping options to override the default values. Refer to Section 3.5, Configuration Straps and Programmable Functions for information on usage of the various device configuration straps.

5.4 Strap Read Stage (STRAP)

In this stage, the firmware registers the configuration strap settings and checks the state of **CFG_STRAP**. If **CFG_STRAP** is set for CONFIG2, then the hub will check the state of the **SMBDATA** and **SMBCLK** pins. If 10k pull-up resistors are detected on both pins, the device will enter the SOC_CFG stage. If 10k pull-up resistors are not detected on both pins, the hub will transition to the OTP_CFG stage instead.

5.5 SOC Configuration Stage (SOC_CFG)

In this stage, the SOC can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors and port electrical settings.

There is no time limit on this mode. In this stage the firmware will wait indefinitely for the SMBus/I^{2}C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.6 OTP Configuration Stage (OTP_CFG)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and battery charging is enabled, the device will transition to the Battery Charger Detection Stage. If VBUS is present, and battery charging is not enabled, the device will transition to the Connect stage.

5.7 Hub Connect Stage (Hub.Connect)

Once the CHGDET stage is completed, the device enters the Hub Connect stage. USB connect can be initiated by asserting the VBUS pin function high. The device will remain in the Hub Connect stage indefinitely until the VBUS pin function is deasserted.

5.8 Normal Mode

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

Microchip provides a comprehensive software programming tool, Pro-Touch2, for configuring the USB5807C functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch2 programming tool. For additional information on the Pro-Touch2 programming tool, refer to Software Libraries within Microchip USB5807C product page at www.microchip.com/USB5807C.

Note:	Device configuration straps and programmable pins are detailed in Section 3.5, Configuration Straps and Programmable Functions. Refer to Section 7.0, Device Interfaces for detailed information on each device interface.

6.1 Customer Accessible Functions

The following functions are available to the customer via the Pro-Touch2 Programming Tool.

Note:	For additional programming details, refer to the Pro-Touch2 programming tool User's Guide.

6.1.1 USB ACCESSIBLE FUNCTIONS

6.1.1.1 SPI Access over USB

Access to an attached SPI device is performed as a pass-through operation from the USB Host. The device firmware has no knowledge of the operation of the attached SPI device. For more information, refer to the Microchip USB5807C product page and SDK at www.microchip.com/USB5807C.

Note:	Refer to Section 7.1, SPI Master Interface for additional information on the SPI.

6.1.1.2 OTP Access

The OTP ROM in the device is accessible via the USB bus during normal runtime operation or SMBus during the SOC_CFG stage. For more information, refer to the Microchip USB5807C product page or the Pro-Touch2 User's Guide.

6.1.1.3 Battery Charging Access over USB

The Battery charging behavior of the device can be dynamically changed by the USB Host when something other than the preprogrammed or OTP programmed behavior is desired. For more information, refer to the Microchip USB5807C product page or the Pro-Touch2 User's Guide.

6.1.2 SMBUS ACCESSIBLE FUNCTIONS

OTP access and configuration of specific device functions are possible via the USB5807C SMBus slave interface. All OTP parameters can be modified via the SMBus Host. For more information refer to the Microchip USB5807C product page.

7.0 DEVICE INTERFACES

The USB5807C provides multiple interfaces for configuration and external memory access. This section details the various device interfaces and their usage:

- SPI Master Interface
- SMBus Slave Interface

Note: For details on how to enable each interface, refer to Section 3.5, Configuration Straps and Programmable Functions.

For information on device connections, refer to Section 4.0, Device Connections. For information on device configuration, refer to Section 6.0, Device Configuration.

Microchip provides a comprehensive software programming tool, Pro-Touch2, for configuring the USB5807C functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch2 programming tool. For additional information on the Pro-Touch2 programming tool, refer to Software Libraries within Microchip USB5807C product page at www.microchip.com/USB5807C.

7.1 SPI Master Interface

The device is capable of code execution from an external SPI ROM. When configured for SPI Mode, on power up the firmware looks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM.

Note: For SPI timing information, refer to Section 10.6.7, SPI Timing.

7.2 SMBus Slave Interface

The device includes an integrated SMBus slave interface, which can be used to access internal device run time registers or program the internal OTP memory. SMBus slave detection is accomplished by setting the **CFG_STRAP** in the correct configuration followed by detection of pull-up resistors on both the **SMDAT** and **SMCLK** signals during the hub's boot-up sequence. Refer to Section 3.5.1, CFG_STRAP Configuration for additional information.

Note: All configuration is to be performed via the Pro-Touch2 programming tool. For additional information on the Pro-Touch2 programming tool, refer to Software Libraries within Microchip USB5807C product page at www.microchip.com/USB5807C.

8.0 FUNCTIONAL DESCRIPTIONS

This section details various USB5807C functions, including:

- Port SplitUSB Type-C Receptacle Support
- Battery Charging
- FlexConnect
- Resets
- Link Power Management (LPM)
- Remote Wakeup Indicator
- Port Control Interface

8.1 Port SplitUSB Type-C Receptacle Support

The USB5807C has built-in support for the USB Type-C receptacle.

8.1.1 EXTERNAL USB 3.2 GEN 1 MULTIPLEXER

C_ATTACH[0:3] pins are used to signal to the hub when a valid USB Type-C connection has been detected. This functionality requires an external USB Type-C controller such as a Microchip UTC2000 to monitor the USB Type-C receptacle for a valid attach. This signal is used to enable and disable clocking to the USB 3.2 Gen 1 PHY in order to reduce power consumption when there is no USB Type-C attach.

The **C_ATTACH[0:3]** pins are active high inputs. A high signal enables clocking to the PHY to enable a USB 3.2 Gen 1 connection. A low signal disables the PHY.

A diagram of a USB Type-C Downstream Facing Port with a USB5807C, Microchip UTC2000, and external multiplexer is shown in Figure 8-1.

A diagram of a USB Type-C Upstream Facing Port with a USB5807C, Microchip UTC2000, and external multiplexer is shown in Figure 8-2.

FIGURE 8-1: DFP TYPE-C PORT WITH MICROCHIP UTC2000 AND EXTERNAL MUX

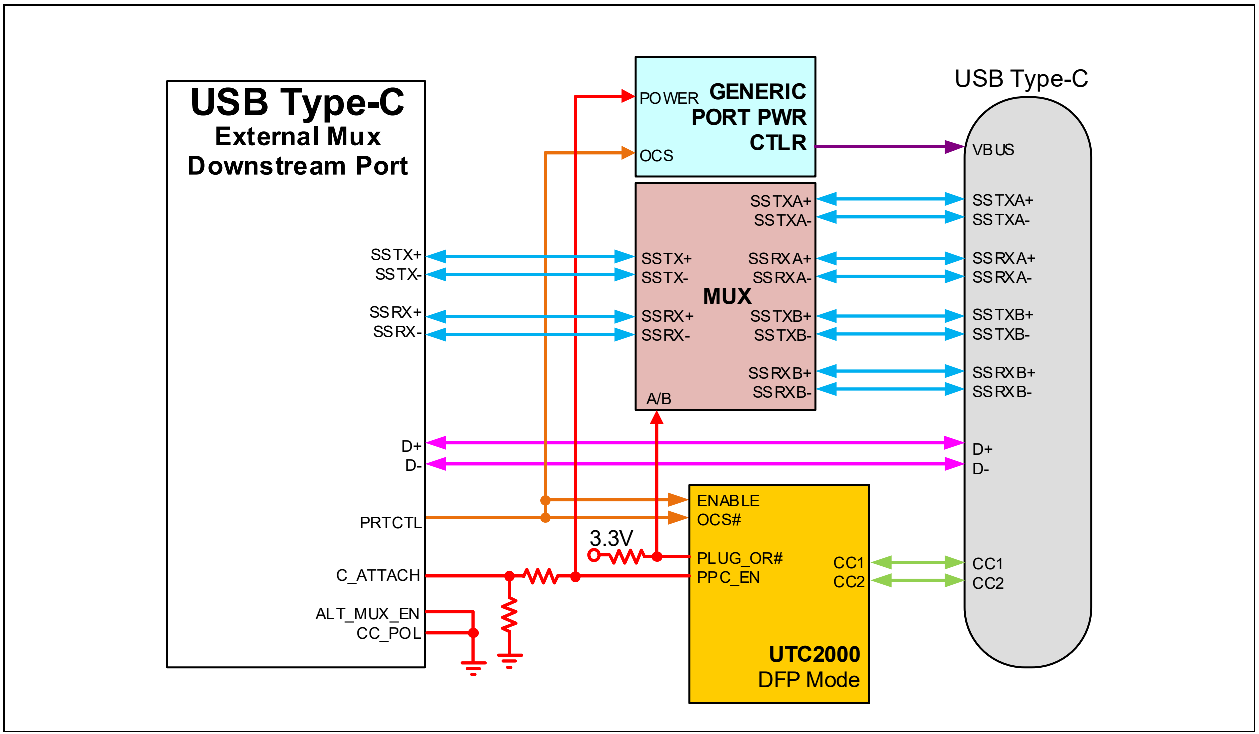
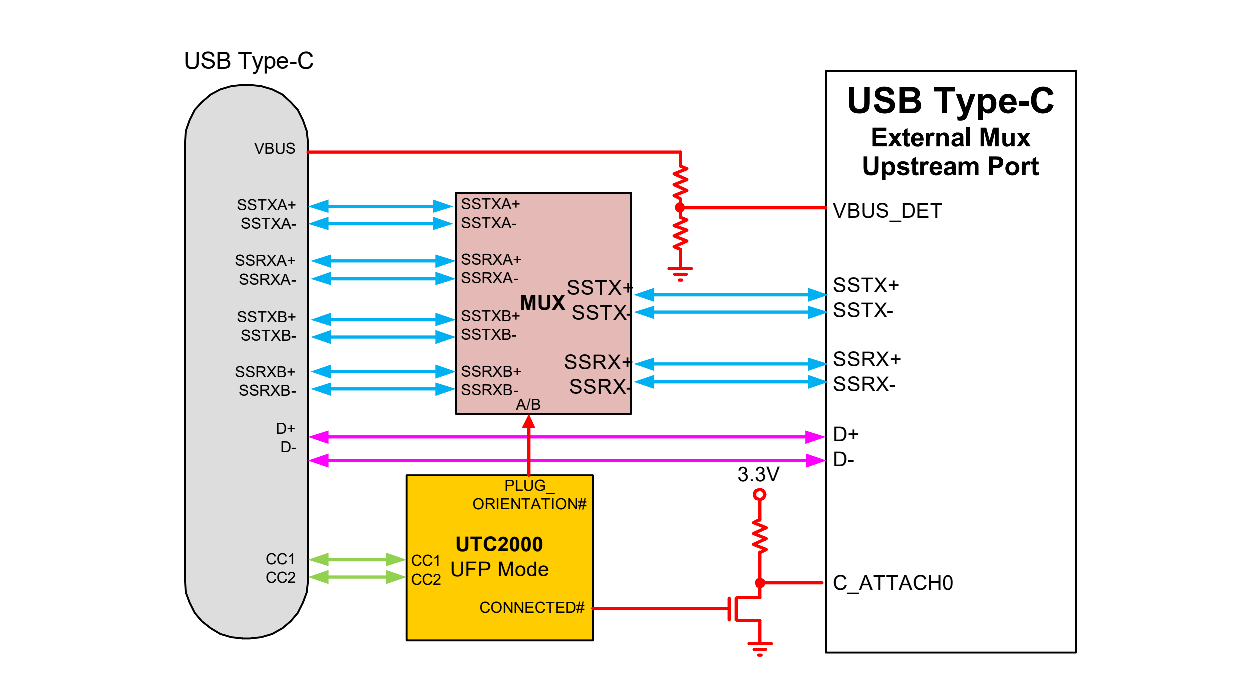


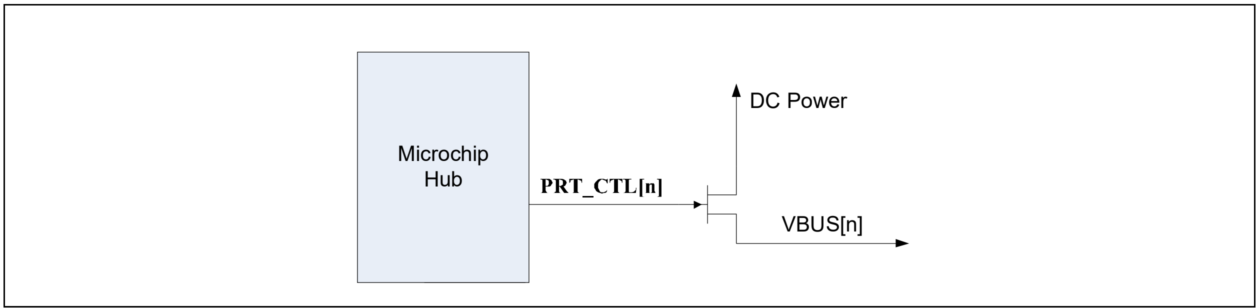
FIGURE 8-2: UFP TYPE-C PORT WITH MICROCHIP UTC2000 & EXTERNAL MUX



8.2 Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 8-3: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via the **PRT_CTL[7:1]** pins, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

For additional information, refer to the Microchip USB5807C Battery Charging application note on the Microchip.com USB5807C product page www.microchip.com/USB5807C.

8.3 FlexConnect

This feature allows the upstream port to be swapped with downstream physical port 1. Only downstream port 1 can be swapped physically. The default state is when port 0 is the upstream port. The 'flexed" state is when port 1 is the upstream port.

FlexConnect can be enabled/disabled in any of the following ways:

- SMBus Configuration
- Direct Pin Control

8.3.1 SMBUS CONFIGURATION

FlexConnect can be controlled via runtime configuration registers through the SMBus Slave Interface during hub run-time (after enumeration).

8.3.2 DIRECT PIN CONTROL

The **FLEX_CMD** control input can be used to control the FlexConnect state. When driven or pulled low, the hub will operate in it's default state. When driven or pull high, the hub will operate in it's "flexed" state.

The **FLEX_STATE** output displays the current state of FlexConnect. It operates in the same manner regardless of how FlexConnect is controlled (SMBus or Direct Pin Control). When low, the hub is currently in it's default state. When high, the hub is in its "flexed" state.

Note:	For additional information, refer to the Microchip USB58xx/USB59xx FlexConnect application note on the Microchip.com USB5807C product page.

8.4 Resets

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.4.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 10.6.2, Power-On and Configuration Strap Timing.

8.4.2 EXTERNAL CHIP RESET (**RESET_N**)

A valid hardware reset is defined as assertion of **RESET_N**, after all power supplies are within operating range, per the specifications in Section 10.6.3, Reset and Configuration Strap Timing. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of **RESET_N** causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note:	All power supplies must have reached the operating levels mandated in Section 10.2, Operating Conditions**, prior to (or coincident with) the assertion of **RESET_N**.

8.4.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

Note: The device does not propagate the upstream USB reset to downstream devices.

8.5 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8-1.

TABLE 8-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 us Exit: <50 us
L0	Fully Enabled (On)	-

8.6 Remote Wakeup Indicator

The remote wakeup indicator feature uses **SUSP_IND** as a side band signal to wake up the host when in USB 2.0 suspend. This feature is enabled and disabled via the HUB_RESUME_INHIBIT configuration bit in the hub configuration space register HUB_CFG_3. The only way to control the bit is by configuration EEPROM, SMBus or internal ROM default setting. The state is only modified during a power on reset, or hardware reset. No dynamic reconfiguring of this capability is possible.

When HUB_RESUME_INHIBIT = '0', Normal Resume Behavior per the USB 2.0 specification

When HUB_RESUME_INHIBIT = '1', Modified Resume Behavior is enabled

Note: The **SUSP_IND** signal only indicates the USB2.0 state.

8.7 Port Control Interface

Port power and over-current sense share the same pin (**PRT_CTLx**) for each port. These functions can be controlled directly from the USB hub, or via the processor. Additionally, smart port controllers can be controlled via the I^2C interface.

The device can be configured into one of the two following port control modes:

- **Ganged Mode** - A single **GANG_PWR** pin controls power and detects over-current events for all downstream ports.
- **Individual Mode** - Each port has an individual **PRT_CTLx** pin for independent port power control and over-current detection.

Port connection in various modes are detailed in the following subsections.

8.7.1 PORT CONNECTION IN GANGED MODE

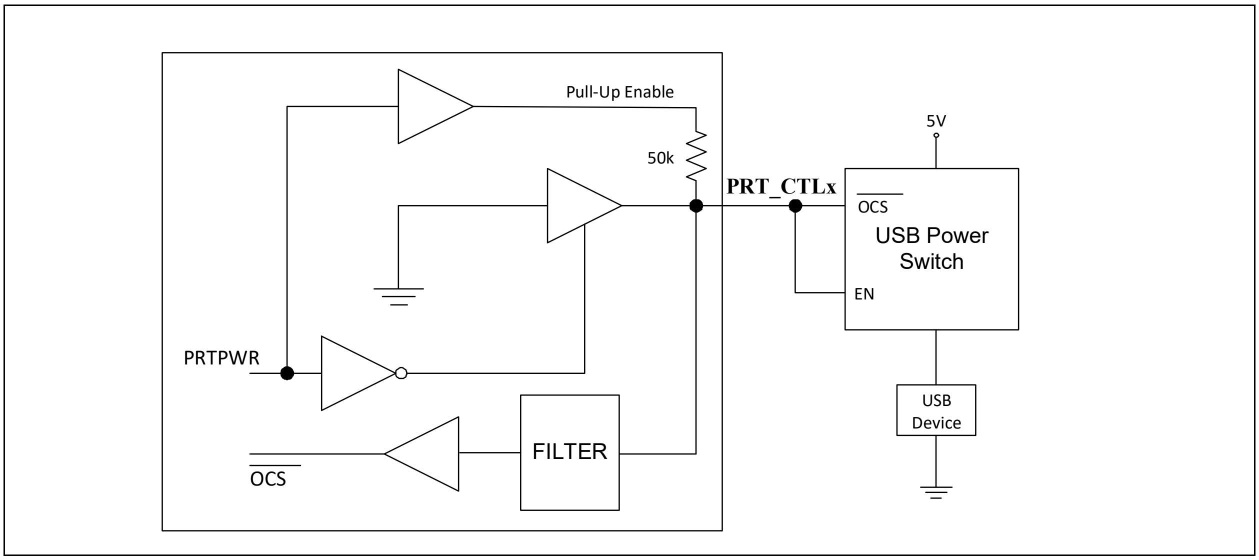
Ganged Mode is enabled via SMBus or OTP configuration. **GANG_PWR** becomes the port control (PRTCTL) pin for all downstream ports when the hub is configured for ganged port power control mode. All port power controllers should be controlled from this pin when the hub is configured for ganged port power mode. While in this mode of operation, an over-current event on any single downstream port will cause all downstream ports to be flagged for over-current.

8.7.2 PORT CONNECTION IN INDIVIDUAL MODE

8.7.2.1 Port Power Control using USB Power Switch

Individual mode is the default mode of operation. When operating in individual mode, the device will have one port power control and over-current sense pin for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the pull-up resistor will be disabled at that time. When port power is enabled, it will disable the output driver and enable the pull-up resistor, making it an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmidt trigger input will recognize that as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions such as low voltage while the device is powering up.

FIGURE 8-4: PORT POWER CONTROL WITH USB POWER SWITCH



When the port is enabled, the **PRT_CTLx** pin input is constantly sampled. Overcurrent events can be detected in one of two ways:

- Single, continuous low pulse (consecutive low samples over t_{ocs_single}), as shown in Figure 8-5.
- Two short low pulses within a rolling window (two groupings of 1 or more low samples over t_{ocs_double}), as shown in Figure 8-6.

FIGURE 8-5: SINGLE LOW PULSE OVERCURRENT DETECTION

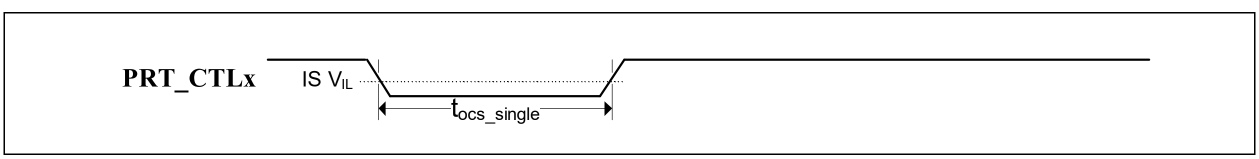
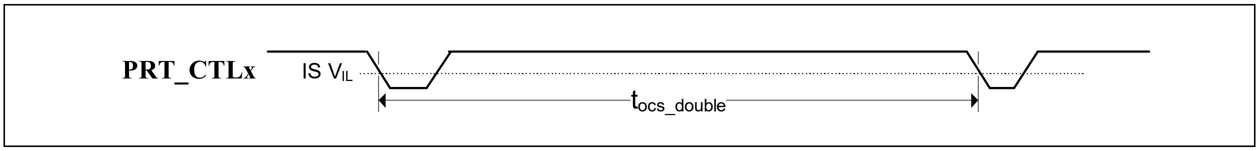


FIGURE 8-6: DOUBLE LOW PULSE OVERCURRENT DETECTION



To maximize compatibility with various port power control topologies, the parameters t_{ocs_single} and t_{ocs_double} are configurable via the Overcurrent Minimum Pulse Width Register and Overcurrent Inactive Timer Register.

The pin also has a turn-on “lockout” feature where the state of the pin is ignored for a configured amount of time immediately after port power is turned on. This prevents slow ramp times due to parasitic resistance/capacitance attached to the pin from triggering false overcurrent detections. This parameter is configurable via the Overcurrent Lockout Timer Register.

TABLE 8-2: OVERCURRENT MINIMUM PULSE WIDTH REGISTER

OCS_MIN_WIDTH (30EAh)			Overcurrent Detection Pulse Window
BIT	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:0	OCS_MIN_WIDTH	R/W	The minimum overcurrent detection pulse width (t_{ocs_single}) is configured in this register. The range can be configured in 1ms increments from 0ms to 5ms. 0000 - 0ms minimum overcurrent detection pulse width 0001 - 1ms minimum overcurrent detection pulse width 0010 - 2ms minimum overcurrent detection pulse width 0011 - 3ms minimum overcurrent detection pulse width 0100 - 4ms minimum overcurrent detection pulse width 0101 - 5ms minimum overcurrent detection pulse width [Default]

TABLE 8-3: OVERCURRENT INACTIVE TIMER REGISTER

OCS_INACTIVE_TIMER (30EBh)			Overcurrent Inactive Timer After First Overcurrent Detection
BIT	**Name**	**R/W**	**Description**
7:0	OCS_INACTIVE_TIMER	R/W	This register configures the timer within which a double low pulse triggers an overcurrent detection event (t_{ocs_double}). The timer can be incremented in 1ms steps. The default value is 20ms (14h). **Note:** This register should never be set to 00h.

TABLE 8-4: OVERCURRENT LOCKOUT TIMER REGISTER

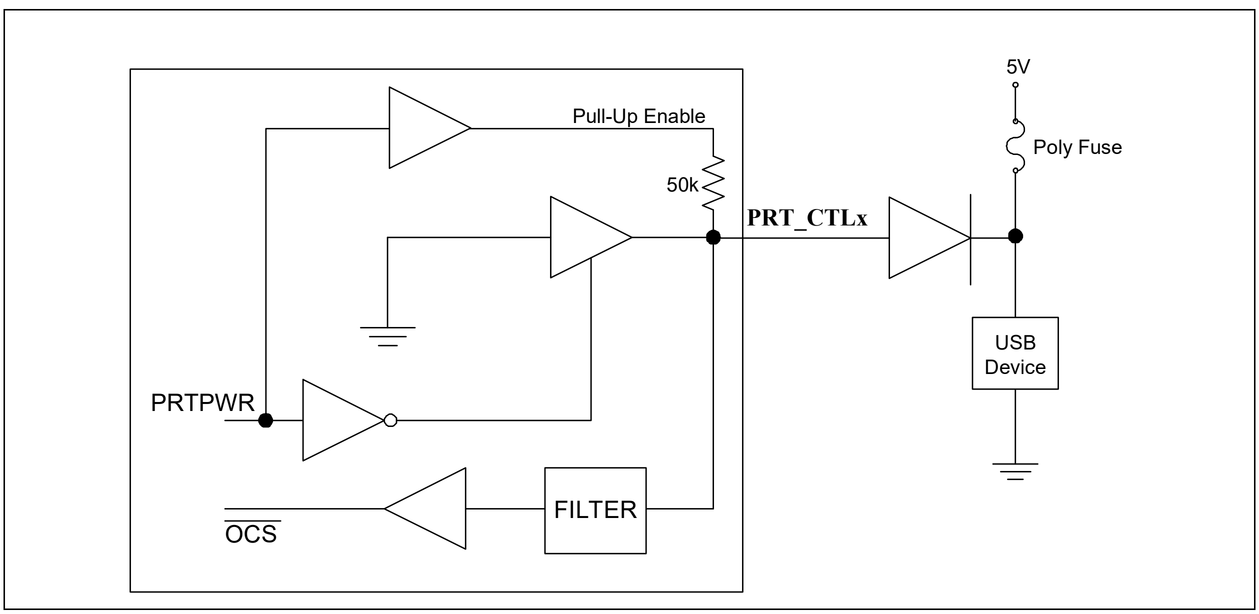
START_LOCKOUT_TIMER_REG (30E1h)			Start Lockout Timer Register
BIT	**Name**	**R/W**	**Description**
7:0	START_LOCKOUT_TIMER_REG	R/W	The “start lockout timer” blocks an overcurrent event from being detected immediately after port power is turned on. Any overcurrent event within this timer value is ignored. The timer can be incremented in 1ms steps. The default value is 10ms (0Ah). **Note:** This register should never be set to 00h.

8.7.2.2 Port Power Control using Poly Fuse

When using the device with a poly fuse, there is no need for an output power control. To maintain consistency, the same circuit will be used. A single port power control and over-current sense for each downstream port is still used from the Hub's perspective. When disabling port power, the driver will actively drive a '0'. This will have no effect as the external diode will isolate pin from the load. When port power is enabled, it will disable the output driver and enable the pull-up resistor. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volts, and the Schmidt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

> **Note:** The USB 2.0 and USB 3.2 Gen 1 bPwrOn2PwrGood descriptors must be set to 0 when using poly-fuse mode. Refer to the “Configuration Options for the USB58xx and USB59xx” Microchip application note for details on how to change these values.

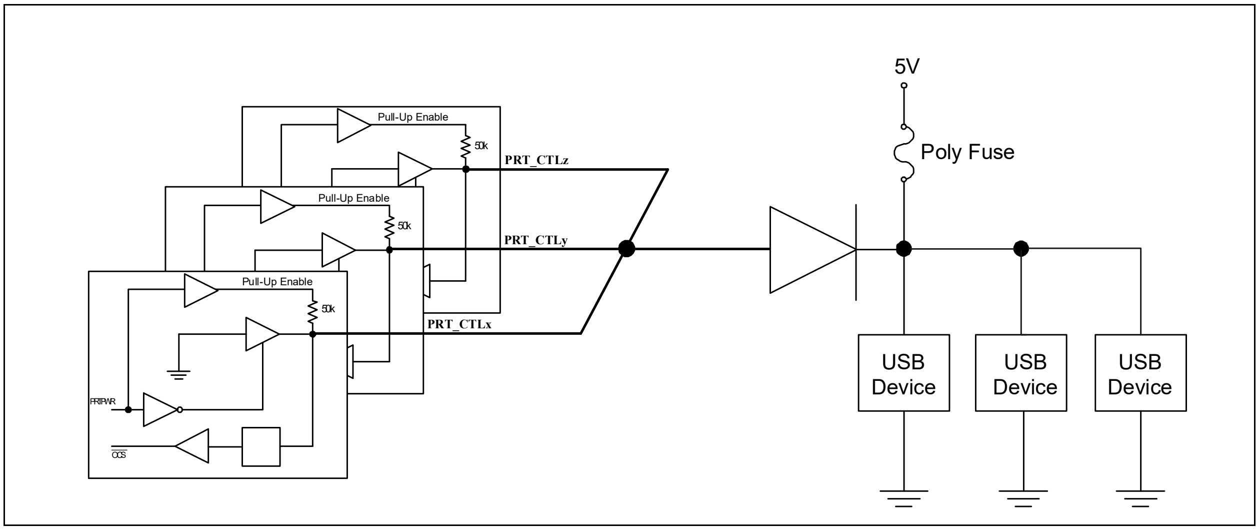
FIGURE 8-7: PORT POWER CONTROL USING A POLY FUSE



8.7.2.3 Port Power Control with Single Poly Fuse and Multiple Loads

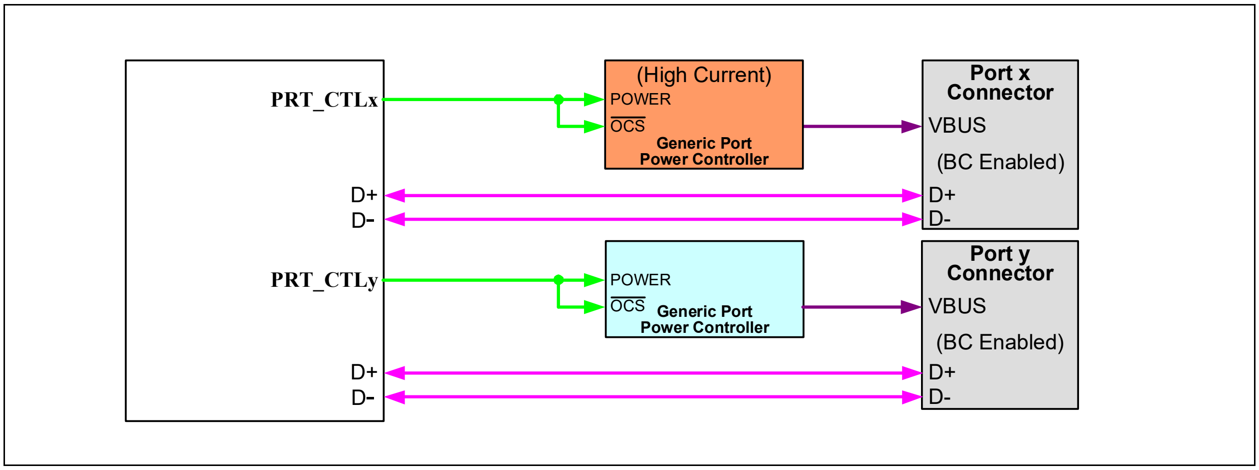
Many customers use a single poly fuse to power all their devices. For the ganged situation, all power control pins must be tied together.

FIGURE 8-8: PORT POWER CONTROL WITH GANGED CONTROL WITH POLY FUSE



8.7.3 PORT CONTROLLER CONNECTION EXAMPLE

FIGURE 8-9: GENERIC PORT POWER CONTROLLERS



Note: The **CFG_BC_EN** configuration strap must be properly configured to enable battery charging on the appropriate ports. For more information on the **CFG_BC_EN** configuration strap, refer to Section 3.5.4, Battery Charging Configuration (CFG_BC_EN).

8.8 Port Split

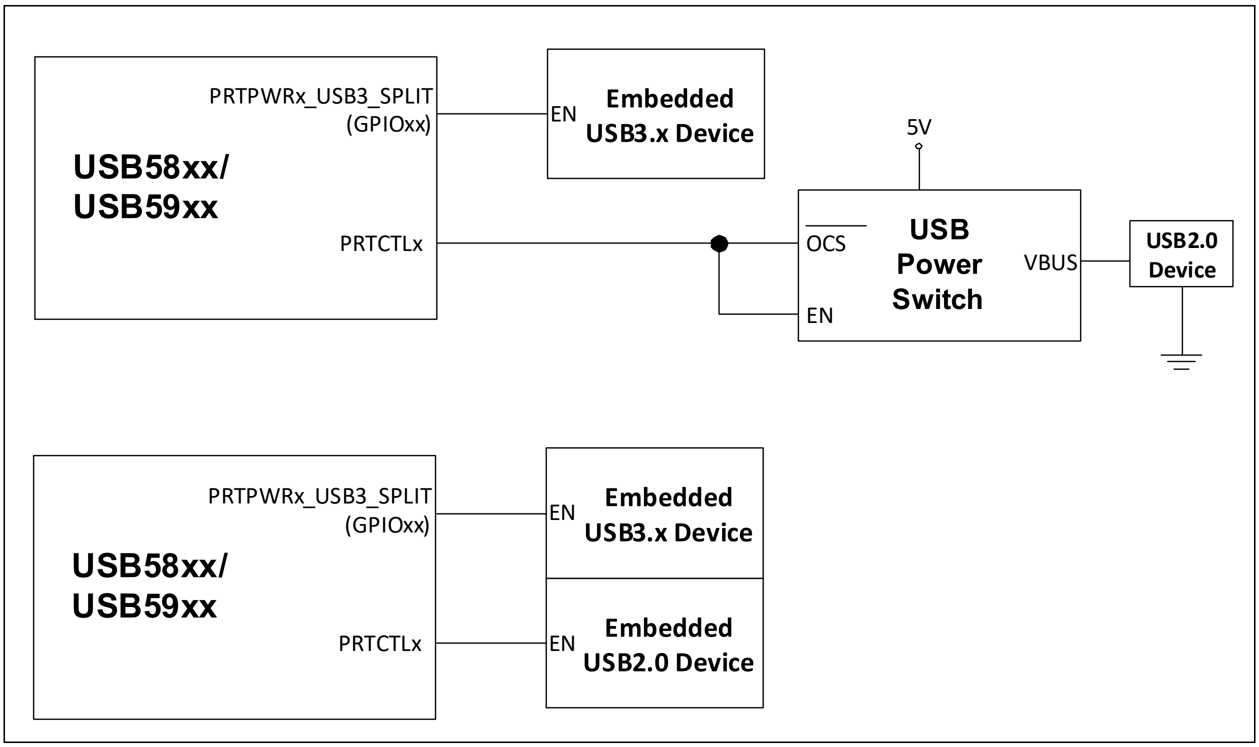
8.8.1 FEATURE OVERVIEW

This feature allows the USB 2.0 and USB 3.2 Gen 1 PHYs associated with any downstream port to be operationally separated. The intention of this feature is to allow a system designer to connect an embedded USB 3.x device to the USB 3.2 Gen 1 PHY, while allowing the USB 2.0 PHY to be used as either a standard USB 2.0 port or with a separate embedded USB 2.0 device.

This feature operates outside of the provisions of the USB specifications. Operation is intended for specialized applications only. Contact your local sales representative for additional information.

In order to maintain a positive end user experience, it is recommended that only permanently attached, embedded USB 3.x devices be connected to the USB 3.2 Gen 1 PHY when enabling the Port Split feature. This prevents end users from attempting to connect USB High-Speed, Full-Speed, or Low-Speed devices to an exposed USB port which only has USB 3.2 Gen 1 connections.

FIGURE 8-10: RECOMMENDED PORT SPLITTING CONFIGURATIONS



8.8.2 PORT SPLITTING CONFIGURATION

Downstream ports 5 and 6 may be configured for Port Splitting. Port Splitting is configured via register configuration through SMBus during the hub configuration stage (SOC_CFG) or via the hub's internal OTP memory.

When Port Splitting is enabled, the existing **PRT_CTLx** pin associated with that port will continue to control the USB 2.0 portion of the port in an identical matter. A new pin function assigned to a **GPIOx** pin will be activated and configured to control the USB 3.2 Gen 1 portion of the port. This new pin is named **PRTPWRx_USB3_SPLIT** where x indicates the respective port. Note that overcurrent detection is not supported on the **PRTPWRx_USB3_SPLIT** pin. These new pins are assigned as shown in Table 8-5.

TABLE 8-5: PORT SPLIT PRTPWRX_USB3_SPLIT PIN ASSIGNMENT

GPIOx Pin	Port Split Assignment
GPIO66	PRTPWR5_USB3_SPLIT Option A
GPIO6	PRTPWR6_USB3_SPLIT Option A
GPIO5	PRTPWR5_USB3_SPLIT Option B
GPIO4	PRTPWR6_USB3_SPLIT Option B

8.8.2.1 Enabling Port Splitting

In order to enable the Port Splitting feature on downstream ports 5 and/or6, the following configuration settings must be made.

Enabling Port Splitting on Port 5:

- Write 0x42 to register 0x416E to select **GPIO66** **for Option A**
- Write 0x05 to register 0x416E to select **GPIO5** **for Option B**
- Set bit 5 of the **USB3_PORT_SPLIT_EN** (0x3C48 = 0x20)
- Set bit 0 of the **PORTSPLITENABLEFLAG** (0x4141 = 0x01)

Enabling Port Splitting on Port 6:

- Write 0x06 to register 0x416F to select **GPIO6 for Option A**
- Write 0x04 to register 0x416F to select **GPIO4 for Option B**
- Set bit 6 of the **USB3_PORT_SPLIT_EN** (0x3C48 = 0x40)
- Set bit 0 of the **PORTSPLITENABLEFLAG** (0x4141 = 0x01)

TABLE 8-6: USB 3.0 PORT SPLIT ENABLE REGISTER

USB3_PORT_SPLIT_EN (0x3C48 - RESET = 0x00)			USB 3.0 Port Split Enable
BIT	Name	R/W	Description
7:1	PORT_SPLIT_EN[7:1]	R/W	0 = Port Splitting on the specified port is disabled 1 = Port Splitting on the specified port is enabled Bit [1] - Reserved [2] - Reserved [3] - Reserved [4] - Reserved [5] - Port 5 [6] - Port 6 [7] - Reserved
0	Reserved	R	Reserved

TABLE 8-7: GLOBAL PORT SPLIT ENABLE REGISTER

PORTSPLITENABLEFLAG (0x4141 - RESET = 0x00)			Global Port Split Enable
BIT	**Name**	**R/W**	**Description**
7:1	Reserved	R	Reserved
0	GLOBAL_PORT_SPLIT_EN	R/W	0 = Port Split feature global disable 1 = Port Split feature global enable

8.8.2.2 Link Timeout Reset

Port Splitting is intended for use with embedded USB 3.x devices only. When Port Splitting is enabled, the hub constantly monitors the USB 3.2 Gen 1 Link to see if a valid USB 3.2 Gen 1 Link is established. If there is no valid USB 3.2 Gen 1 Link for a configured amount of time (see below), then the hub will toggle assertion of the associated "**PRTPWRx-_USB3_SPLIT**" pin in an attempt to reset the embedded USB 3.2 Gen 1 device and re-establish the USB 3.2 Gen 1 Link. The timer is always reset and restarted whenever the timeout occurs.

A valid USB 3.2 Gen 1 link is qualified by the LTSSM_STATE register status for the port. A normal Link will actively switch through many Link states.

If the hub detects that the Link is staying in one of the following Link states the entire duration of the timeout timer, then the Link is stuck in an invalid state and **PRTPWRx_USB3_SPLIT** will be toggled in order to attempt to re-establish the Link.

- SIS.Disabled(0x4)
- Rx.Detect(0x5)
- SS.Inactive(0x6)
- Polling(0x7)
- Recovery(0x8)
- HotReset (0x9)

The Link Timeout Reset value is configured via register 0x4171 and can be overridden by OTP. The default value is 0x05, which selects a Timeout value of 1 second. Setting the register to 0x00 will disable the Link Timeout Reset feature.

The duration of the Link reset (time which **PRTPWRx_USB3_SPLIT** signal stays low) can be configured in register 0x4176. The default duration is 400ms with a configurable range of 350ms to 2.9s.

9.0 COMPLIANCE UPDATE

In order to be USB-IF certified (TID 1595), silicon revision C and newer of the USB5807C supports the USB 3.2 Engineering Change Notices (ECNs) included in the *Universal Serial Bus Revision 3.2 Specification*. This allows the latest revision of the USB5807C to be certified in compliance with USB-IF logo testing for the new USB Type-C® industry initiative. The following compliance updates are supported:

- Pending Header Packet (HP) Timer (TD7.9, TD7.11, TD7.26)
- Power Management (PM) Timer (TD7.18, TD7.20, TD7.23)
- Unacknowledged Connect and Remote Wake Test Failure (TD10.25)

These USB 3.2 ECNs can be found as part of the *Universal Serial Bus Revision 3.2 Specification* zip file, which can be downloaded from the USB developers website (http://www.usb.org/developers/docs/).

9.1 Pending Header Packet (HP) Timer (TD7.9, TD7.11, TD7.26)

A turn around time is defined between the communication of a Host and Device (Link Partners) for an acknowledgment of a USB connection. The time is budgeted between a number of steps (Transmit/Receive data path of the initiator, the delay in the cable, and the response time of the responder). If the time is exceeded, no USB communication is initiated.

The ECN calls to relax the timing from 3us to 10us at the link and PHY layers to allow for an extended propagation delay to account for the usage of active cables and retimers in new SuperSpeed Plus designs.

Impact to Legacy Systems:

- A new host with a retimer connected to an active cable AND a legacy device
- A legacy host connected to an active cable and a new device with or without a retimer

9.2 Power Management (PM) Timer (TD7.18, TD7.20, TD7.23)

There are three timers for link power management: PM_LC_TIMER, PM_ENTRY_TIMER, and Ux_EXIT_TIMER. The PM_LC_TIMER is used for a port initiating an entry request to a low power link state. The PM_ENTRY_TIMER is used for a port accepting the entry request to a low power link state. Ux_EXIT_TIMER is used for a port to initiate the exit from U1 or U2 to a low power state.

The ECN calls to increase the maximum timeout values to accommodate for the new connectivity models with retimers and active cables beyond the standard USB-IF transmission lengths.

Impact to Legacy Systems:

- No impact to USB 3.0 or early USB 3.2 ecosystems

9.3 Unacknowledged Connect and Remote Wake Test Failure (TD10.25)

If a USB3 port with a connected device is placed into Suspend and RemoteWake is set but the RemoteWake mask (C_PORT_CONNECTION bit) has not been cleared, the USB3 hub will automatically issue a wake up signal to the host.

In legacy systems, if a USB3 port with a connected device was placed into Suspend and RemoteWake is set without the mask bit being cleared, the USB3 hub would NOT issue a wake up signal to the host.

Impact to Legacy Systems:

- No impact – with the new implementation, a remote wake is automatically initiated if the mask bit is not set. In older systems the remote wake may or may not have been executed.

10.0 OPERATIONAL CHARACTERISTICS

10.1 Absolute Maximum Ratings*

+1.2 V Supply Voltage (**VDD12**) (Note 1) . . . . . -0.5 V to +1.32 V

+3.3 V Supply Voltage (**VDD33**) (Note 1) . . . . . -0.5 V to +4.6 V

Positive voltage on input signal pins, with respect to ground (Note 2) . . . . . +4.6 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Positive voltage on **XTALI/CLKIN**, with respect to ground . . . . . +3.63 V

Positive voltage on USB DP/DM signal pins, with respect to ground . . . . . +6.0 V

Positive voltage on USB 3.2 Gen 1 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** signal pins, with respect to ground . . . . . 1.32 V

Storage Temperature . . . . . -55°C to +150°C

Junction Temperature . . . . . +125°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . 2.5 kV

Note 1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 2: This rating does not apply to the following pins: All USB DM/DP pins, **XTAL1/CLKIN**, and **XTALO**

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 10.2, Operating Conditions**, Section 10.5, DC Specifications, or any other applicable section of this specification is not implied.

10.2 Operating Conditions**

+1.2 V Supply Voltage (**VDD12**) . . . . . +1.08 V to +1.32 V

+3.3 V Supply Voltage (**VDD33**) . . . . . +3.0 V to +3.6 V

Input Signal Pins Voltage (Note 2) . . . . . -0.3 V to +3.6 V

XTALI/CLKIN Voltage . . . . . -0.3 V to +3.6 V

USB 2.0 DP/DM Signal Pins Voltage . . . . . -0.3 V to +5.5 V

USB 3.2 Gen 1 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** Signal Pins Voltage . . . . . -0.3 V to +1.32 V

Ambient Operating Temperature in Still Air (T_A) . . . . . Note 3

+1.2 V Supply Voltage Rise Time (T_{RT} in Figure 10-1) . . . . . 400 µs

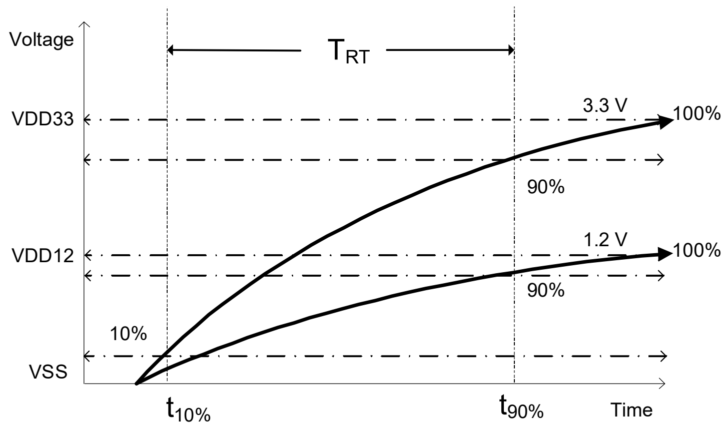
+3.3 V Supply Voltage Rise Time (T_{RT} in Figure 10-1) . . . . . 400 µs

Note 3: 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note:	Do not drive input signals without power supplied to the device.

FIGURE 10-1: SUPPLY RISE TIME MODEL



Note:	The rise time for the 3.3 V supply can be extended to 100ms max if **RESET_N** is actively driven low, typically by another IC, until 1 µs after all supplies are within operating range.

10.3 Package Thermal Specifications

TABLE 10-1: PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	19	0
	16	1
Ψ_{JT}	0.1	0
	0.1	1
Θ_{JC}	1.4	0
	1.4	1

Note:	Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51. For industrial applications, the USB5807C requires a multi-layer 2S4P PCB power dissipation.

TABLE 10-2: MAXIMUM POWER DISSIPATION

Parameter	Value	Units
PD(max)	2.3	W

10.4 Power Consumption

The values shown below represent typical power consumption as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

The following measurements were taken with **VDD33** equal to 3.3V, **VDD12** equal to 1.2V, at an ambient temperature of 25°C.

Note: A USB 3.x hub operates both the USB 3.x and USB 2.0 interfaces in parallel on it's upstream port connection. A port operating under the SS/HS condition indicates that a USB 3.x hub was connected to it.

TABLE 10-3: DEVICE POWER CONSUMPTION

	Typical (mA)		Typical Power
	VDD33	VDD12	(mW)
Reset	1.0	10.5	16
No VBUS	4.0	8.0	23
Global Suspend	4.0	8.0	23
7 FS Ports	42	246	433
7 HS Ports	105	259	657
7 SS Ports	84	1,008	1,487
7 SS/HS Ports	154	1,022	1,735

Note: Actual power consumption will vary depending on the capabilities of the USB host, the devices connected, data type, and data bus utilization. The published data represents typical power consumption of the hub at nominal ambient temperature and supply voltage while large file transfers are active between USB host and USB Mass Storage class devices on all downstream ports.

Typical power consumption for specific use cases can be estimated using the formulas below:

$I_{VDD33}(mA) = 35 + (N_{PORTSFS})(1)^* + (N_{PORTSHS})(10) + (N_{PORTSSS})(7)$
$I_{VDD12}(mA) = 245 + (N_{PORTSFS})(0.1)^* + (N_{PORTSHS})(2) + (N_{PORTSSS})(109)$
$P_{TOTAL}(mW) = 409.5 + (N_{PORTSFS})(3.42)^* + (N_{PORTSHS})(35.4) + (N_{PORTSSS})(153.9)$

10.5 DC Specifications

TABLE 10-4: I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
I Type Input Buffer						
Low Input Level	V_{IL}			0.9	V	
High Input Level	V_{IH}	2.1			V	
IS Type Input Buffer						
Low Input Level	V_{IL}			0.9	V	
High Input Level	V_{IH}	1.9			V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	9	20	40	mV	
O6 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -6 mA

TABLE 10-4: I/O DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	Typical	Max	Units	Notes
O12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -12 mA
OD12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
ICLK Type Input Buffer (XTALI Input)						Note 4
Low Input Level	V_{IL}			0.50	V	
High Input Level	V_{IH}	0.85		**VDD33**	V	
IO-U Type Buffer (See Note 5)						Note 5

Note 4: **XTALI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

Note 5: Refer to the USB 3.2 Gen 1 Specification for USB DC electrical characteristics.

10.6 AC Specifications

This section details the various AC timing specifications of the device.

10.6.1 POWER SUPPLY AND RESET_N SEQUENCE TIMING

Figure 10-2 illustrates the recommended power supply sequencing and timing for the device. **VDD33** should rise after or at the same rate as **VDD12**. Similarly, **RESET_N** and/or **VBUS_DET** should rise after or at the same rate as **VDD33**. **VBUS_DET** and **RESET_N** do not have any other timing dependencies.

FIGURE 10-2: POWER SUPPLY AND RESET_N SEQUENCE TIMING

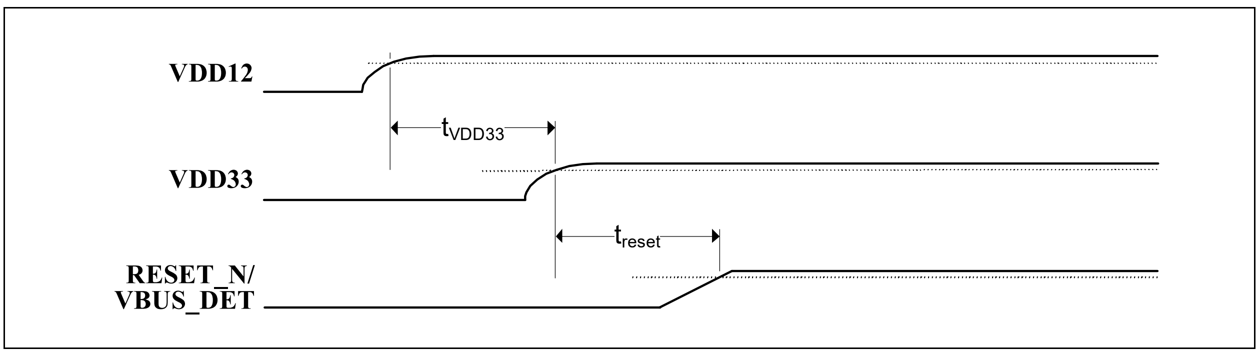


TABLE 10-5: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{VDD33}	**VDD12** to **VDD33** rise time	0			ms
t_{reset}	**VDD33** to **RESET_N/VBUS_DET** rise time	0			ms

10.6.2 POWER-ON AND CONFIGURATION STRAP TIMING

Figure 10-3 illustrates the configuration strap valid timing requirements in relation to power-on, for applications where RESET_N is not used at power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 10.2, Operating Conditions**.

FIGURE 10-3: POWER-ON CONFIGURATION STRAP VALID TIMING

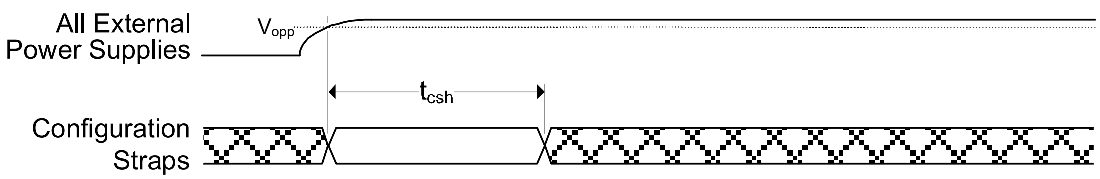


TABLE 10-6: POWER-ON CONFIGURATION STRAP LATCHING TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supplies at operational levels	1			ms

Device configuration straps are also latched as a result of RESET_N assertion. Refer to Section 10.6.3, Reset and Configuration Strap Timing for additional details.

10.6.3 RESET AND CONFIGURATION STRAP TIMING

Figure 10-4 illustrates the RESET_N pin timing requirements and its relation to the configuration strap pins. Assertion of RESET_N is not a requirement. However, if used, it must be asserted for the minimum period specified. Refer to Section 8.4, Resets for additional information on resets. Refer to Section 3.5, Configuration Straps and Programmable Functions for additional information on configuration straps.

FIGURE 10-4: RESET_N CONFIGURATION STRAP TIMING

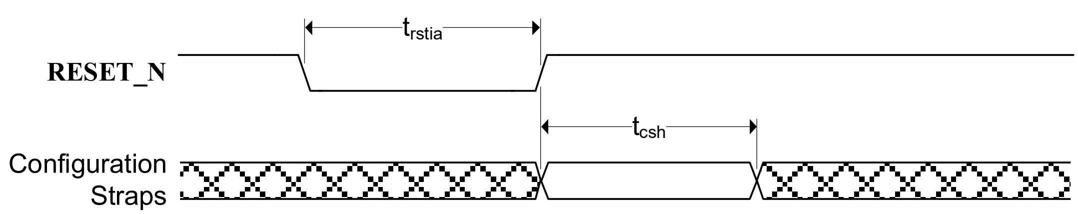


TABLE 10-7: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	RESET_N input assertion time	5			µs
t_{csh}	Configuration strap pins hold after RESET_N deassertion	1			ms

Note: The clock input must be stable prior to RESET_N deassertion.

Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 10.6.2, Power-On and Configuration Strap Timing apply.

10.6.4 USB TIMING

All device USB signals confirm to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Revision 3.1 Specification*, available at http://www.usb.org/developers/docs.

10.6.5 I^2C TIMING

All device I^2C signals confirm to the 100KHz Standard Mode (Sm) voltage, power, and timing characteristics/specifications as set forth in the *I^2C-Bus Specification*. Please refer to the *I^2C-Bus Specification*, available at http://www.nxp.com/documents/user_manual/UM10204.pdf.

10.6.6 SMBUS TIMING

All device SMBus signals confirm to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification.* Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

10.6.7 SPI TIMING

This section specifies the SPI timing requirements for the device.

FIGURE 10-5: SPI TIMING

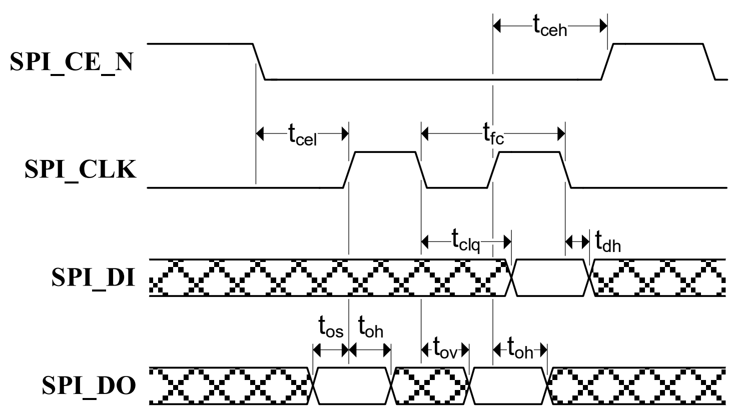


TABLE 10-8: SPI TIMING (30 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			30	MHz
t_{ceh}	Chip enable (SPI_CE_EN) high time	100			ns
t_{clq}	Clock to input data			13	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (SPI_CE_EN) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (SPI_CE_EN) high	12			ns

TABLE 10-9: SPI TIMING (60 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			60	MHz

TABLE 10-9: SPI TIMING (60 MHZ OPERATION)

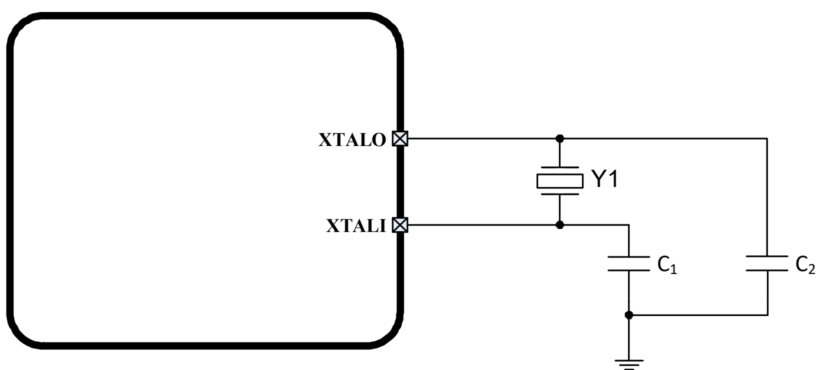
Symbol	Description	Min	Typ	Max	Units
t_{ceh}	Chip enable (**SPI_CE_EN**) high time	50			ns
t_{clq}	Clock to input data			9	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_EN**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_EN**) high	12			ns

10.7 Clock Specifications

The device can accept either a 25MHz crystal or a 25MHz single-ended clock oscillator (±50ppm) input. If the single-ended clock oscillator method is implemented, **XTALO** should be left unconnected and **XTALI/CLKIN** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). The following circuit design (Figure 10-6) and specifications (Table 10-10) are required to ensure proper operation.

FIGURE 10-6: 25MHZ CRYSTAL CIRCUIT



10.7.1 CRYSTAL SPECIFICATIONS

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). Refer to Table 10-10 for the recommended crystal specifications.

TABLE 10-10: CRYSTAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	±50	PPM	
Frequency Stability Over Temp	F_{temp}	-	-	±50	PPM	
Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	PPM	Note 6
Total Allowable PPM Budget		-	-	±100	PPM	Note 7
Shunt Capacitance	C_O	-	7 typ	-	pF	

TABLE 10-10: CRYSTAL SPECIFICATIONS (CONTINUED)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	100	-	-	uW	
Equivalent Series Resistance	R_1	-	-	60	Ω	
Operating Temperature Range		Note 7	-	Note 8	^oC	
XTALI/CLKIN Pin Capacitance		-	3 typ	-	pF	Note 9
XTALO Pin Capacitance		-	3 typ	-	pF	Note 9

Note 6: Frequency Deviation Over Time is also referred to as Aging.

Note 7: 0 °C for commercial version, -40 °C for industrial version.

Note 8: +70 °C for commercial version, +85 °C for industrial version.

Note 9: This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTALI/CLKIN** pin, **XTALO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

10.7.2 EXTERNAL REFERENCE CLOCK (**CLKIN**)

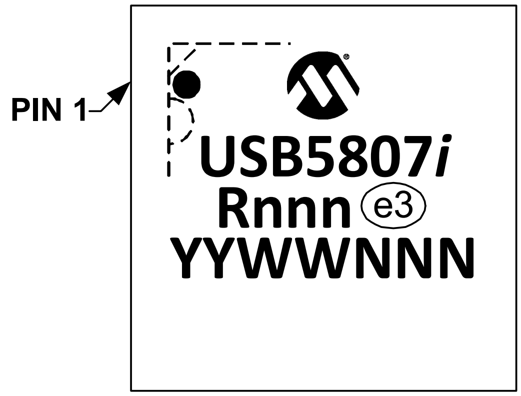
When using an external reference clock, the following input clock specifications are suggested:

- 25 MHz
- 50% duty cycle ±10%, ±100 ppm
- Jitter < 100 ps RMS

11.0 PACKAGE INFORMATION

11.1 Package Marking Information

100-VQFN (12x12 mm)



Legend:		
	i	Temperature range designator (Blank = commercial, *i* = industrial)
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

11.2 Package Drawings

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 11-1: 100-VQFN PACKAGE (DRAWING)

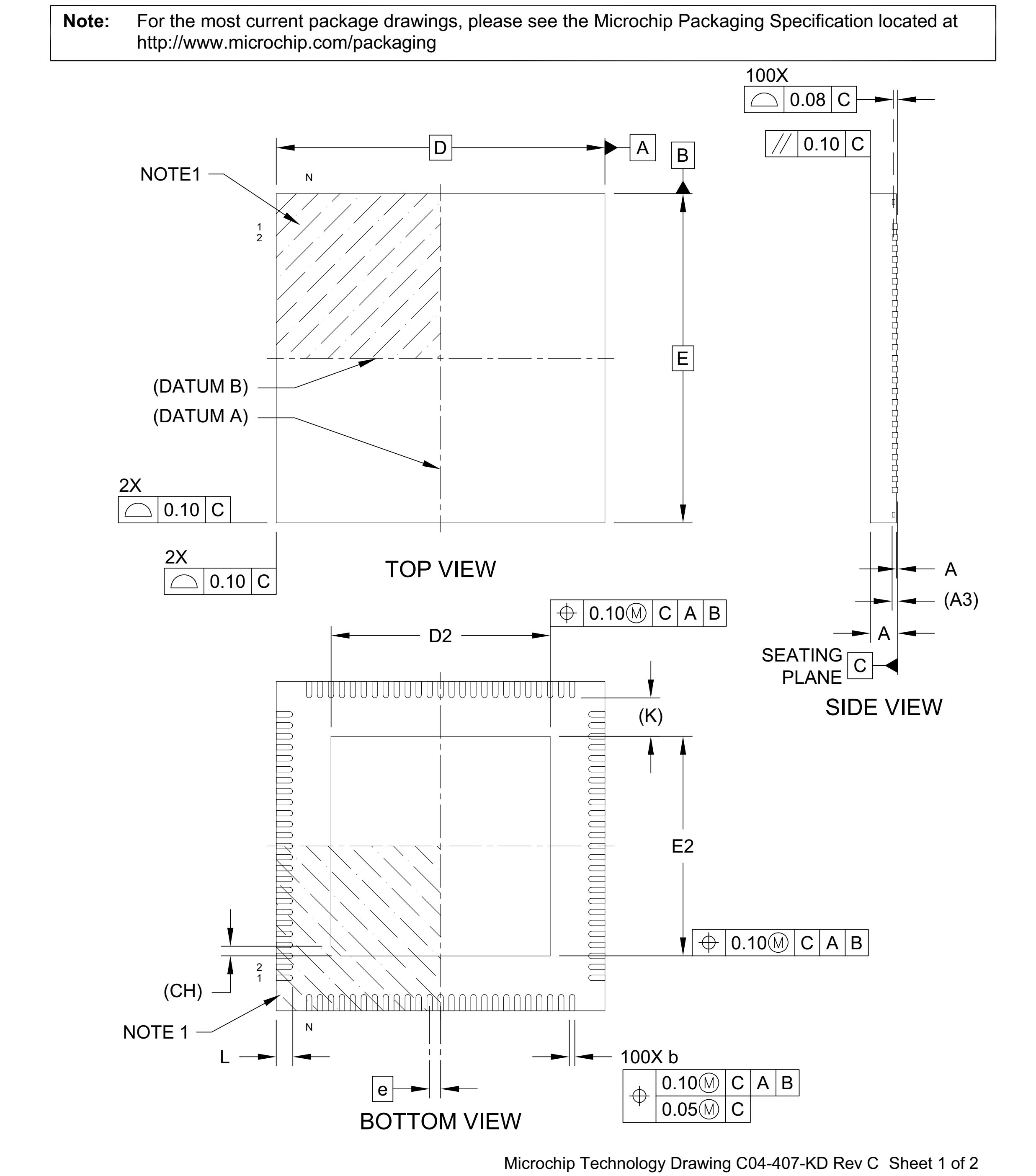
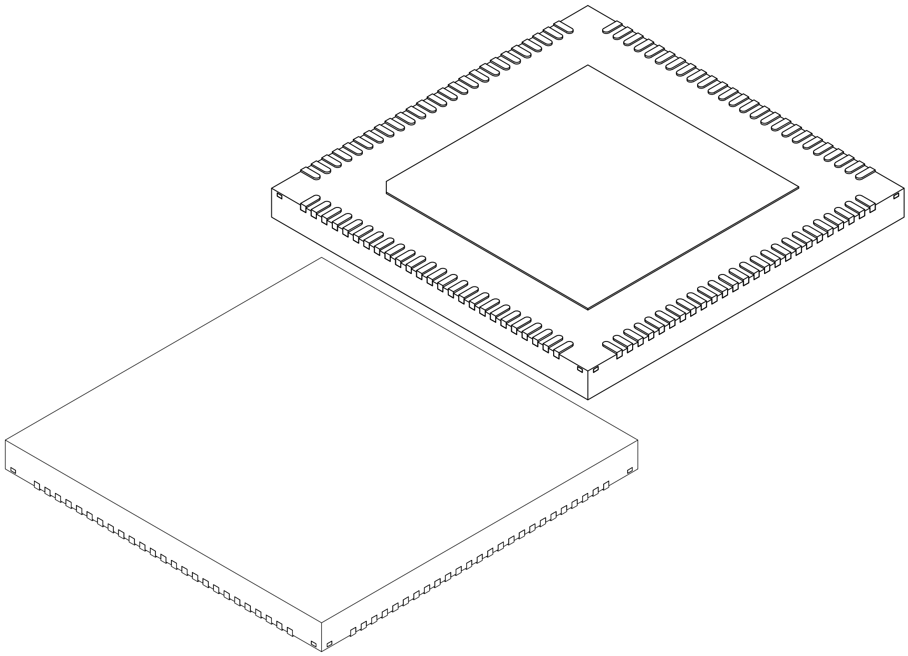


FIGURE 11-2: 100-VQFN PACKAGE (DIMENSIONS)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		12.00 BSC	
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E		12.00 BSC	
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K		1.40 REF	
Exposed Pad Corner Chamfer	CH		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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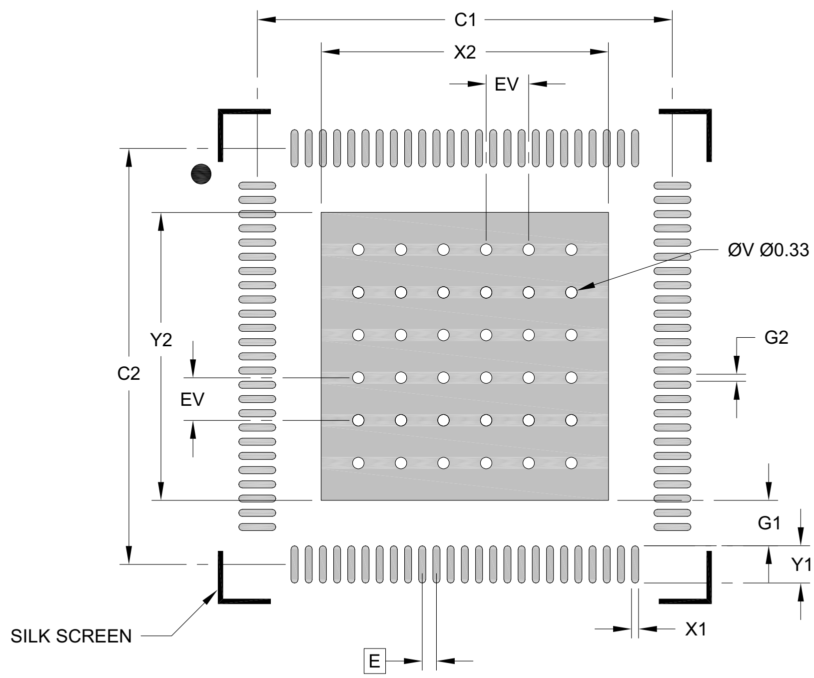
FIGURE 11-3: 100-VQFN PACKAGE (LAND PATTERN)

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			8.10
Center Pad Length	Y2			8.10
Contact Pad Spacing	C1		11.70	
Contact Pad Spacing	C2		11.70	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.05
Contact Pad to Center Pad (X100)	G1	1.28		
Contact Pad to Contact Pad (X96)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003182C (03-17-22)	Figure 11-1, Figure 11-2, Figure 11-3	Updated package drawings
DS00003182B (08-20-21)	Updated title	Added “SmartHub™ IC
	Figure 8-1	- Updated figure
		- Updated USB 3.1 to USB 3.2 throughout the document
DS00003182A (08-16-19)		Initial Release

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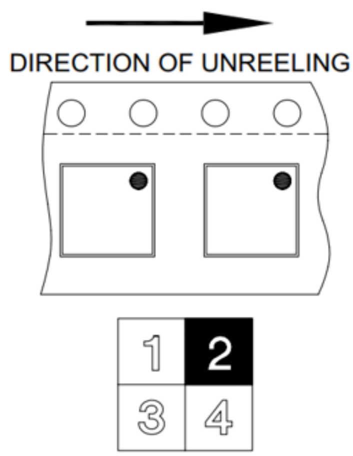
PART NO.	[X][(1)]	[-X]	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	USB5807C	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel[(1)]
Temperature Range:	Blank I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial)
Package:	KD	= 100-pin VQFN



Examples:

a) USB5807C/KD
Tray, Commercial temp., 100-pin VQFN

b) USB5807C-I/KD
Tray, Industrial temp., 100-pin VQFN

c) USB5807CT/KD
Tape & reel, Commercial temp., 100-pin VQFN

d) USB5807CT-I/KD
Tape & reel, Industrial temp., 100-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 2: Devices prior to silicon revision C do not include the upgrades described in Section 9.0, Compliance Update.

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