

## DC – 20 GHz Programmable 1, 2, 4, and 8 Binary Prescaler

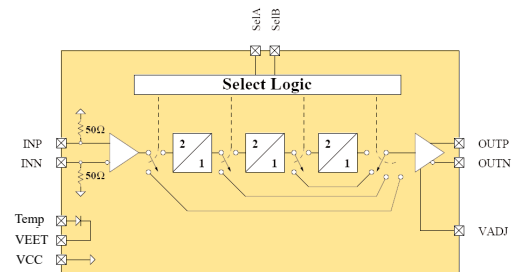
### Product Overview

The UXD20P is a low-noise DC-to-20 GHz Programmable Prescaler featuring either divide-by-1, divide-by-2, divide-by-4, or divide-by-8 division ratios. In the divide-by-1 mode, the UXD20P is also a limit amplifier. The device features differential inputs and outputs, adjustable output swing, and high input sensitivity. The control inputs are CMOS- and LVTTTL-compatible. UXD20P is a 24-pin, 4 mm × 4 mm plastic QFN package. The product is also available as a die.

#### Key Features

- **Wide operating range: DC – 20 GHz**
- **Low SSB phase noise: -153 dBc @ 10 kHz**
- **Large output swings: 750 mV pp/ side**
- **Single-ended and/or differential operation**
- **Low power consumption: 430 mW**
- **3 Dividers in one with pass through**
- **DC – 7 GHz limiting amp**

#### UXD20P Functional Block Diagram



#### Applications

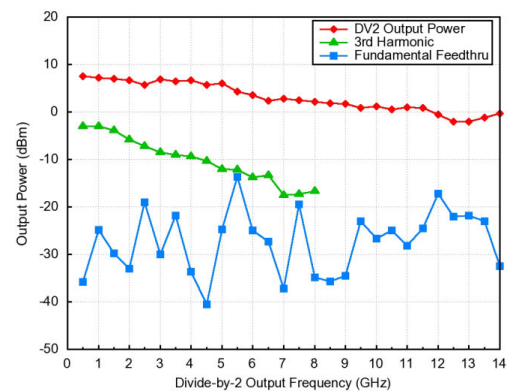
The UXD20P can be used as a general purpose, fixed modulus prescaler in high-frequency PLLs. The low phase noise of the divider makes it ideal for generating low-jitter synchronous clocks in telecom applications.

**Table 1. Performance Overview**

Parameter	Typ.	Units
Input frequency	DC – 20	GHz
Output power	+ 3	dBm
SSB phase noise at 10 kHz offset	-153	dBc/Hz

**Export Classification: EAR99**

#### Binary Divide-by-2 Output Power, 3rd Harmonic & Input Feedthru



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## 1. Electrical Performances

### 1.1 Typical Electrical Performance

**Table 1-1. Typical Electrical Performance at +25 °C, – 3.3V/130 mA, and 50 Ω Termination (Unless Otherwise Specified)**

Parameter	Min	Typ	Max	Units
Input frequency	DC		20	GHz
Input power	–10	0	+ 10	dBm
Output power	–5	3		dB
SSB phase noise at 10 kHz offset		–153		dBc/Hz
Supply voltage		–3.3		V
Supply current (divide-by-8)		130		mA

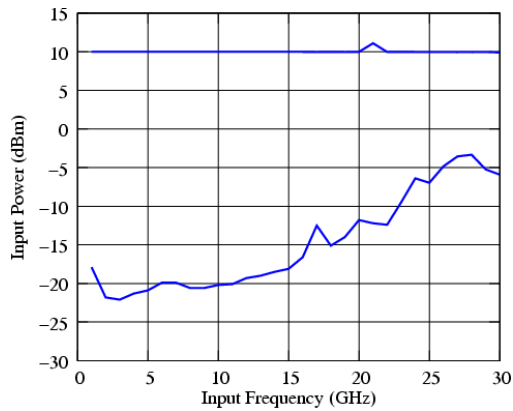
### 1.2 Typical Performance Curves

The following graphs show the typical performance curves of the UXD20P at +25 °C and – 3.3V unless otherwise indicated.

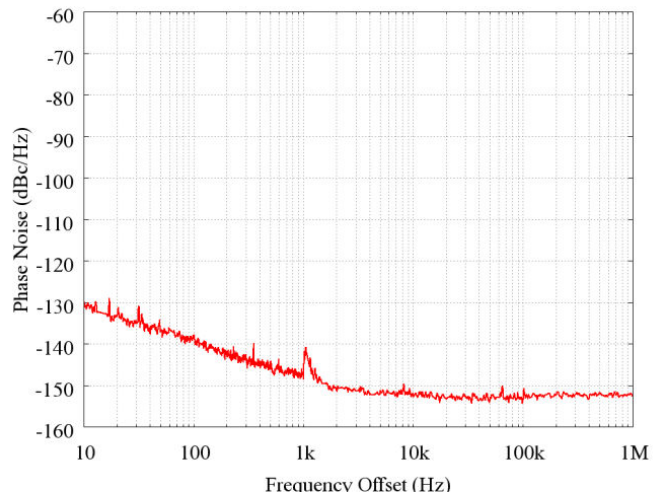
#### 1.2.1 Frequency Divider Application

The following graphs show the typical performance curves of the UXD20P device when used as a frequency divider at +25 °C, –3.3V (unless otherwise indicated).

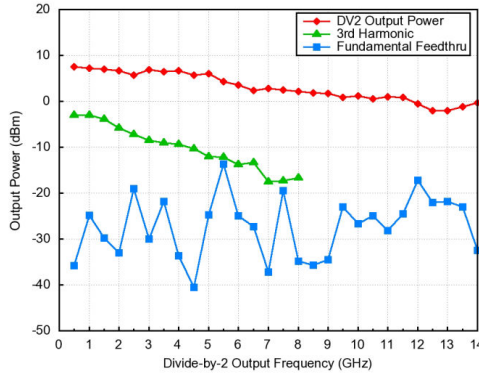
**Figure 1-1. Input Sensitivity Window (Single-Ended)**



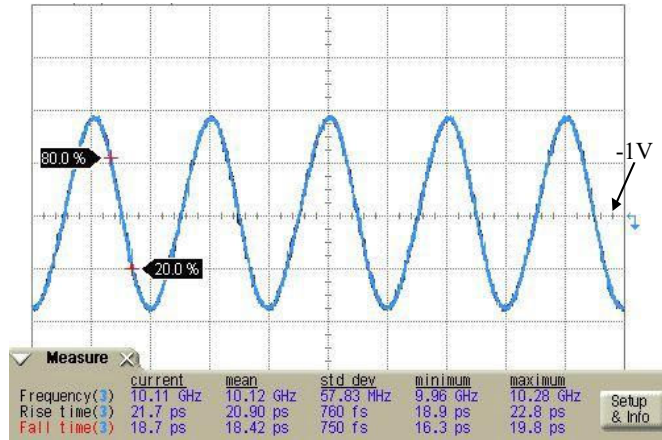
**Figure 1-2. SSB Phase Noise @ 7.8 GHz (Divide-by-8)**



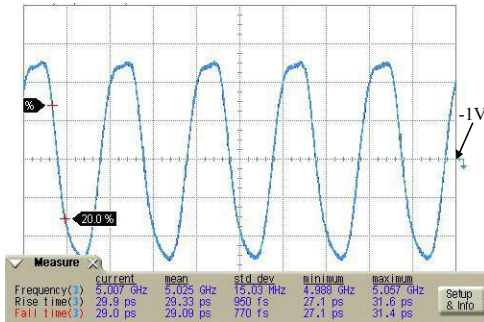
**Figure 1-3. Divide-by-2 Output Power, 3rd Harmonic & Input Feedthru**



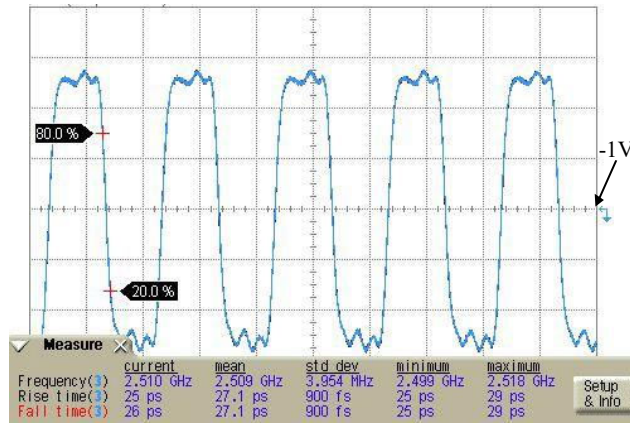
**Figure 1-4. Binary Divide-by-2 Configuration at 20 GHz Input Freq. (150 mV/div)**



**Figure 1-5. Binary Divide-by-4 Configuration at 20 GHz Input Freq. (150 mV/div)**



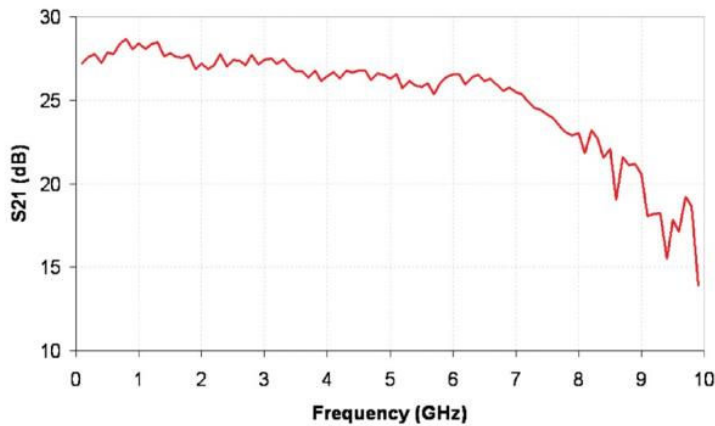
**Figure 1-6. Binary Divide-by-8 Configuration at 20 GHz Input Freq. (150 mV/div)**



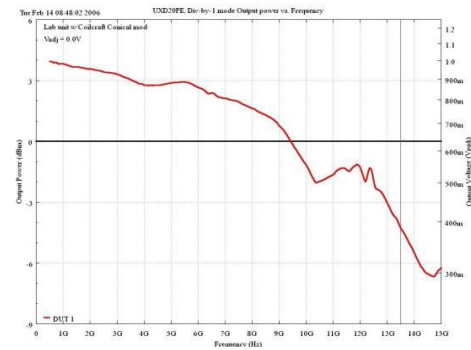
### 1.2.2 Limiting Amplifier Applications

The following graphs show the typical performance curves of the UXD20P device when used as a Limiting Amplifier at +25 °C, -3.3V and 130 mA (Unless otherwise indicated).

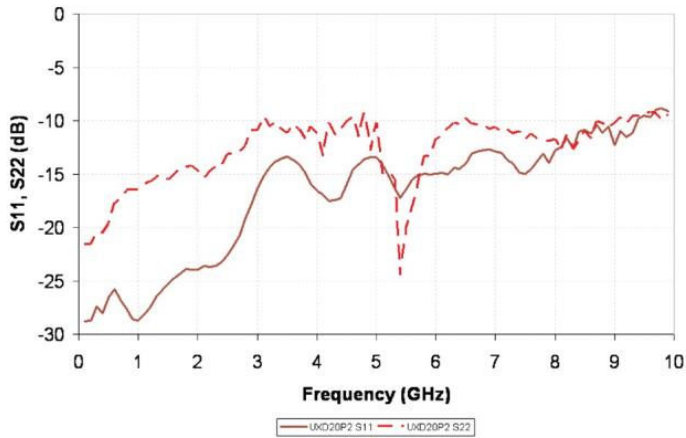
**Figure 1-7. S21 (Divide-by-1, Single-Ended)**



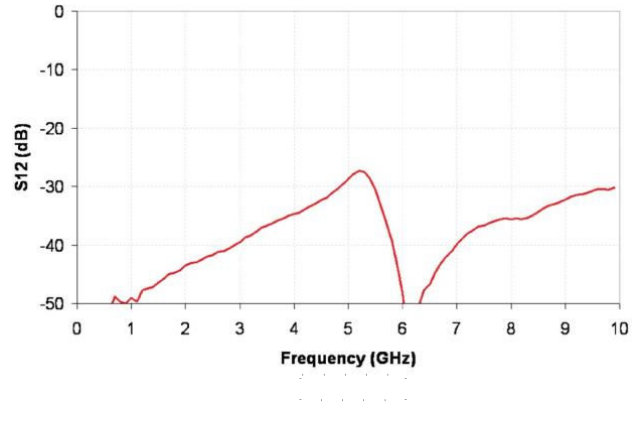
**Figure 1-8. Pout vs. Frequency (Divide-by 1, Single-Ended)**



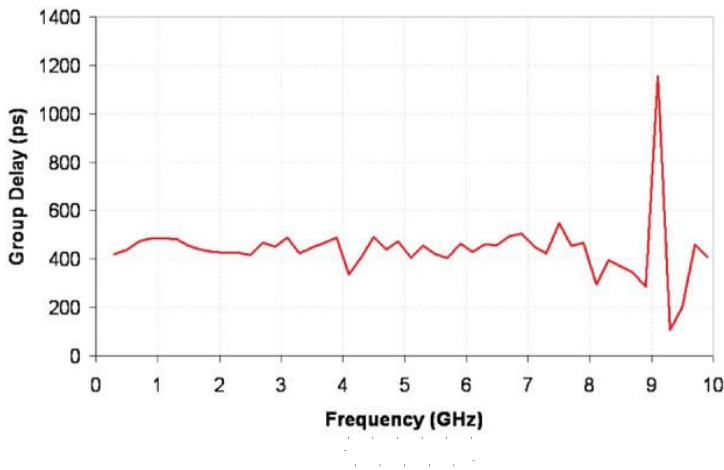
**Figure 1-9. Input & Output RL (Divide-by-1, Single-Ended)**



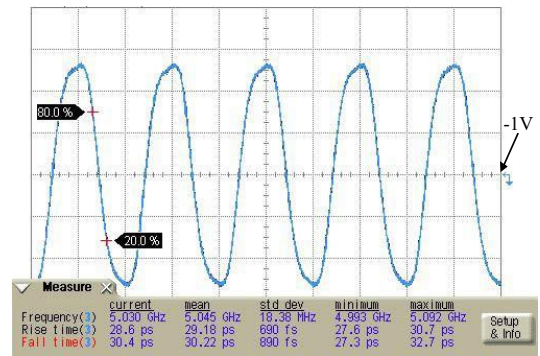
**Figure 1-10. S12 (Divide-by-1, Single-Ended)**



**Figure 1-11. Group Delay vs. Frequency (Divide-by-1, Single-Ended)**



**Figure 1-12. Binary Divide-by-1 Configuration at 5 GHz Input Freq. (150 mV/div)**



### 1.3 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the UXD20P device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

**Table 1-2. Absolute Maximum Ratings**

Parameter	Rating
Supply voltage (VCC – VEE)	4V
RF input power (INP, INN)	+10 dBm
Operating temperature	–40 °C to +85 °C
Junction temperature	+125 °C
Junction-case thermal resistance	32 °C/W
Storage temperature	–85 °C to +125 °C
Peak reflow temperature	260 °C
Time at peak reflow temperature	40 secs

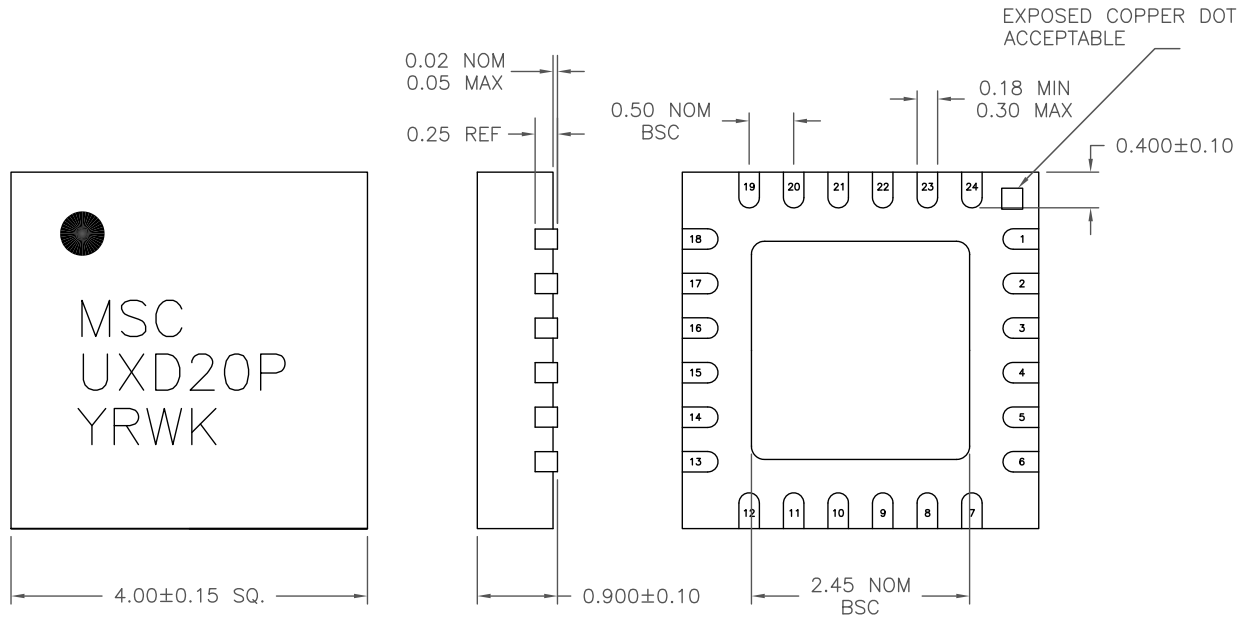


ESD Sensitive Device

## 2. Die Specifications

For additional packaging information, contact your Microchip sales representative.

**Figure 2-1. Package Outline Drawing**



4 mm × 4mm, 24L Plastic QFN Package

**Table 2-1. Package Information**

Parameter	Specification
Lead frame material	Cu (C194)
Plating	Ni/Pd/Au
Package body material	RoHS-compliant, low-stress injection molded plastic

**Table 2-2. I/O Pad Description**

PIN Number	PIN Label	PIN Description	Notes
2 & 4	INP/INN	Prescaler differential RF input, positive/negative terminal	CML signal levels
16 & 18	OUTP/OUTN	Prescaler differential RF outputs, positive/negative terminal	Requires DC return path to VCC
1, 3, 5, 6, 7, 13, 15, 17, 19, 20	VCC	Positive supply voltage	All VCC pads are connected together within the package.
23, 24	VEE	Negative supply voltage	All VCC pads are connected together within the package.
22 & 21	SelA & SelB	Divider mode	Divider Select Line, Refer to <a href="#">Table 2-3</a> , defaults to logic 0
14	VADJ	Output amplitude control	Tie to VCC via resistor for max swing.
8	Temp	Temperature diode	IC Surface Temperature, refer to corresponding App. Note
9	VEET	Negative supply voltage for temperature diode	Connect to VEE

.....continued

PIN Number	PIN Label	PIN Description	Notes
10, 11, 12	N/C	Not connected	

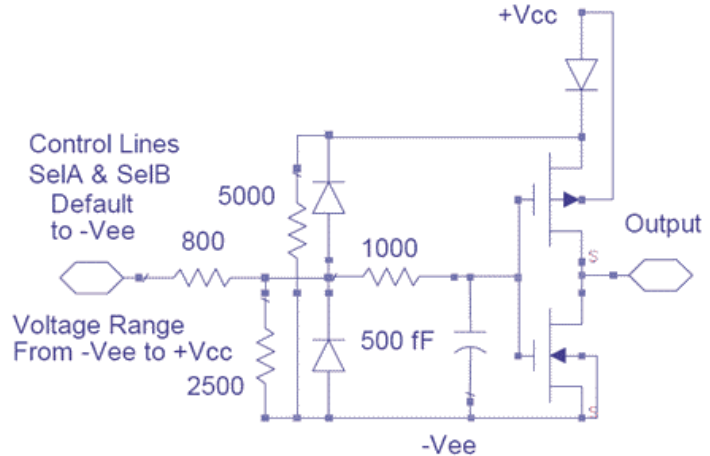
**Table 2-3. Divider Mode Slect Logic**

SeIA	SeIB	Mode	DC Current
0	0	Divide-by-1	105 mA
1	0	Divide-by-8	130 mA
0	1	Divide-by-4	125 mA
1	1	Divide-by-2	120 mA

**Table 2-4. Control Voltages**

State	Bias Conditions	Comment
Low (logic 0)	VEE @ 0 mA	Default condition (internally pulled low)
High (logic 1)	VCC @ 1 mA	

**Figure 2-2. Simplified Control Logic Schematic**



### 3. Application Notes

Contact Microchip Technology for further information.

#### 3.1 Divider Mode

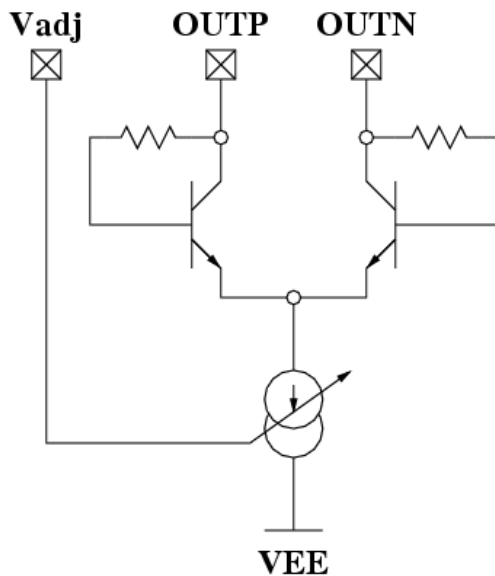
The UXD20P supports four division ratios controlled by two select lines which are compatible with CMOS/LVTTL signaling levels. [Table 2-3](#) lists the four states for the given logic levels on the SelA and SelB select lines. For any of the four modes, circuitry which is not used is automatically powered down to reduce power consumption.

#### 3.2 Divider Outputs

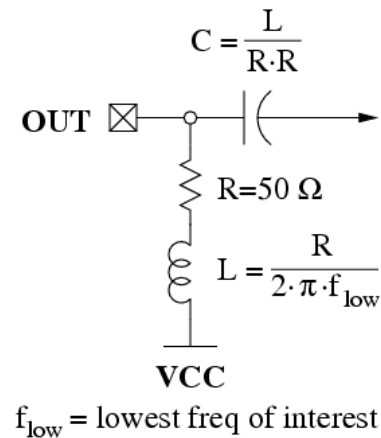
The equivalent circuit of the divider outputs is shown below. The outputs require a DC return path capable of handling ~35 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be ~50 Ω (or less) to VCC to prevent excessive common mode voltage from saturating the Prescaler outputs. If AC coupling is used, the perfect embodiment is shown in [Figure 3-2](#). The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

The output amplitude can be adjusted over a 1.5:1 range by one of the two methods. The Vadj pin voltage can be set to VCC for maximum amplitude or VCC-1.3 V for an amplitude ~2/3 the max swing. Voltages between these two values will produce a linear change in output swing. Alternatively, users can use a 1k potentiometer or fixed resistor tied between Vadj and VCC. Resistor values approaching 0 ohms will lead to the maximum swing, while values approaching 1k will lead to the minimum output swing. Users who only need/want the maximum swing should simply tie Vadj to VCC.

**Figure 3-1. Equivalent Circuit of the Output Buffer**



**Figure 3-2. Recommended Circuit for AC Coupled Outputs**



#### 3.3 Low-Frequency Operation

Low-frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

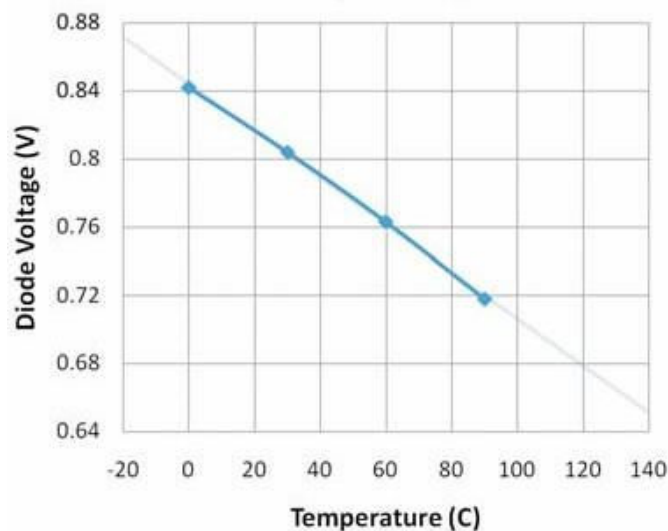
The values of the coupling capacitors for the high-speed inputs and outputs (I/Os) are determined by the lowest frequency the IC will be operated at  $C > > \frac{1}{2\pi \cdot 50 \cdot f}$ . For example, to use the device below 30 kHz, coupling capacitors should be larger than 0.1  $\mu$ F.

### 3.4 Temperature Diode

An optional on-chip temperature diode is provided for users interested in evaluating the IC's temperature. A single resistor to VCC establishes a nominal current through the diode. The voltage developed across the temperature pin (pin 8) referenced to VEE (pin 9) can then be used to indicate the surface temperature of the IC. The plot below was obtained by forcing a fixed current of 120  $\mu$ A through the diode for an unbiased device at multiple temperatures and fitting a line to the data to allow extrapolation over a range of temperatures.

**Figure 3-3. Diode Voltage vs Temp**

$$T = (0.84 - V_d) / 0.00133$$

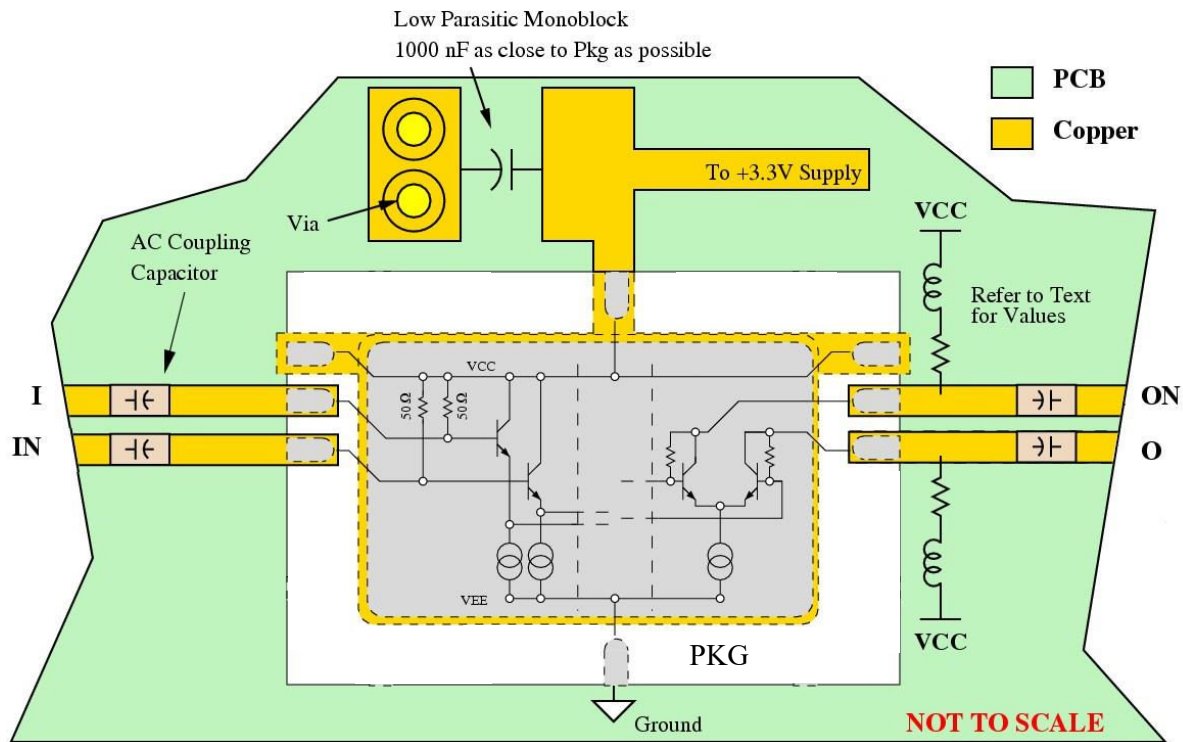


### 3.5 IC Assembly

The device is designed to operate with either single-ended or differential inputs. [Figure 3-4](#), [Figure 3-5](#) and [Figure 3-6](#) show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

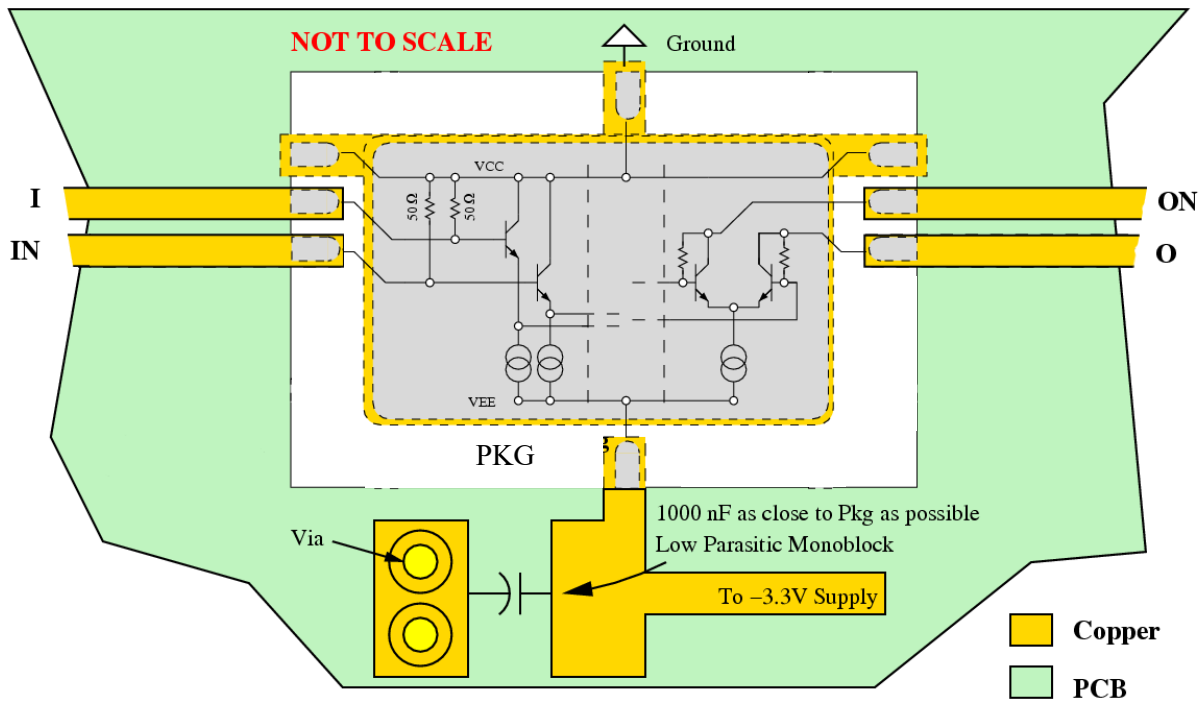
All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when VCC is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

Figure 3-4. Positive Supply (AC Coupled)



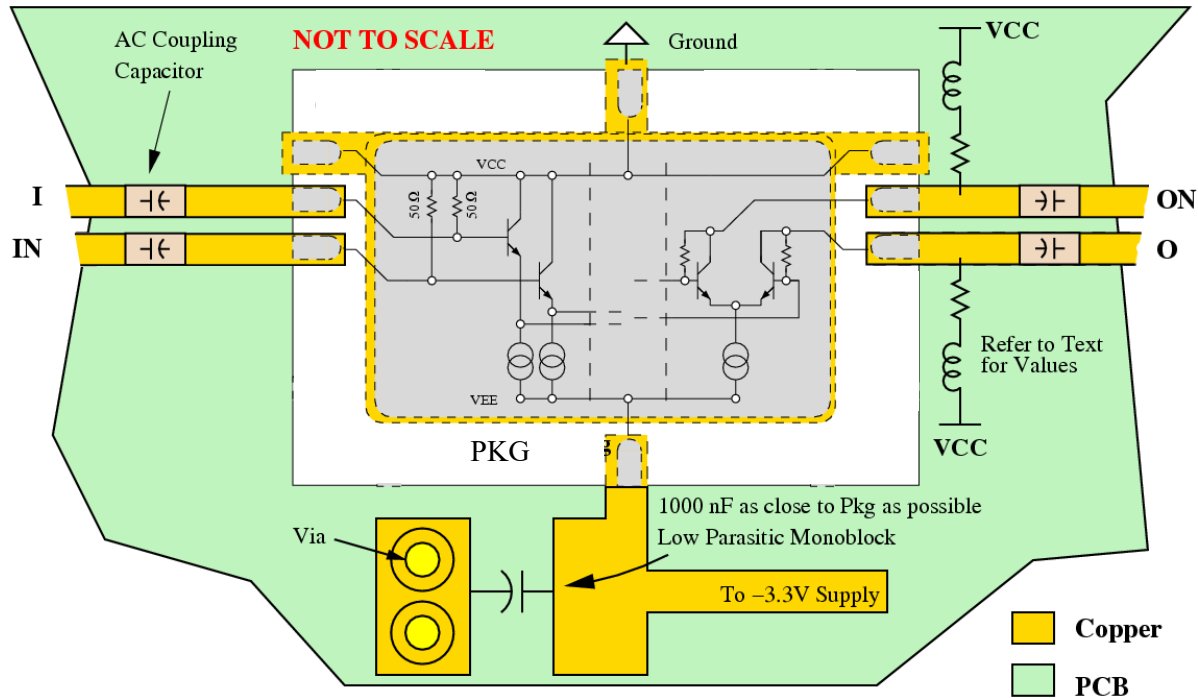
Biasing recommendations for positive supply with AC coupling applications

Figure 3-5. Negative Supply (DC Coupled)



Biasing recommendations for negative supply with DC coupling applications

Figure 3-6. Negative Supply (AC Coupled)



Biasing recommendations for negative supply with AC coupling applications

### 3.6 CML Logic Levels for DC Coupling (T = 25 °C)

Assuming 50 Ω terminations at inputs and outputs.

Parameter			Minimum	Typical	Maximum
Input	Differential	Logic input <sub>high</sub>	V <sub>cc</sub>	V <sub>cc</sub>	V <sub>cc</sub>
		Logic input <sub>low</sub>	V <sub>cc</sub> - 0.05V	V <sub>cc</sub> - 0.3V	V <sub>cc</sub> - 1V
	Single	Logic input <sub>high</sub>	V <sub>cc</sub> + 0.05V	V <sub>cc</sub> + 0.3V	V <sub>cc</sub> + 1V
		Logic input <sub>low</sub>	V <sub>cc</sub> - 0.05V	V <sub>cc</sub> - 0.3V	V <sub>cc</sub> - 1V
Output	Differential and single	Logic input <sub>high</sub>	V <sub>cc</sub> - 0.9V	V <sub>cc</sub> - 0.6V	V <sub>cc</sub> - 0.5V
		Logic input <sub>low</sub>	V <sub>cc</sub> - 1.3V	V <sub>cc</sub> - 1.6V	V <sub>cc</sub> - 1.7V

### 3.7 Differential vs. Single-Ended

The UXD20P is fully differential to maximize signal-to-noise ratios for high-speed operation. High speed inputs are terminated to VCC with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to V<sub>max</sub> to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$|V_{dm}/2 + V_{cm}| < V_{cc} \leq V_{max}$$

where V<sub>dm</sub> is the differential input signal and V<sub>cm</sub> is the common-mode voltage.

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to VCC for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest.

Use the positive terminals for single-ended operation while terminating the negative terminal to VCC.

Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Tying unused inputs directly to VCC shorts out the internal 50  $\Omega$  bias resistor, imposing a DC offset sufficient to prevent oscillations. Driving the differential inputs with DC blocks, or driving the single-ended inputs without terminating unused inputs, is not recommended without taking additional steps to eliminate the potential oscillation issues.

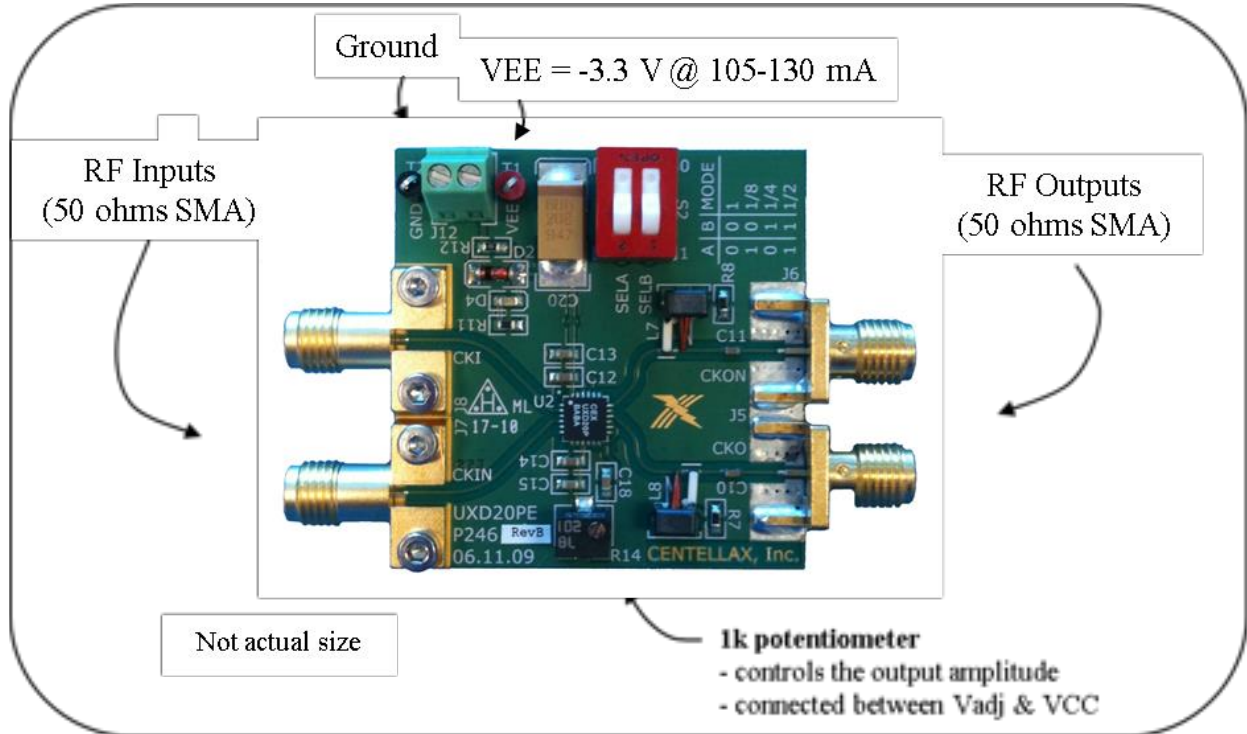
### 3.8 Die Heatsink

The Package backside provides the primary heat conduction path and should be attached to a good heatsink on the PC board to maximize performance. User PC boards should maximize the contact area to the package paddle and contain an array of vias to aid thermal conduction to either a backside heatsink or internal copper planes.

## 4. Evaluation PCB

UXD20PE is an evaluation board for the UXD20P DC-20 GHz Programmable 1,2,4,8 Binary Prescaler.

**Figure 4-1. UXD20P Evaluation PCB (Negative supply)**



### Notes

1. If RF inputs/outputs are used in single-ended configuration, terminate unused inputs/outputs with 50 ohm loads.
2. Use on-board switches to control the divide ratios according to [Table 4-1](#)
3. Refer to UXD20P Datasheet for performance specifications.
4. Contact Microchip for further assistance

**Table 4-1. Divider Mode Select Logic**

Switch Settings		Division Ratio Output
A	B	
0	0	1
1	0	1/8
0	1	1/4
1	1	1/2

## 5. Ordering, Shipping and Handling

### 5.1 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

### 5.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Note
UXD20P	4 mm × 4 mm, 24L Plastic QFN	
UXD20PE	UXD20P Eval PCB	
UXD20C	Bare Die	Refer to corresponding UXD20C Datasheet

### 5.3 Packing Information

Part Number	Description
MMFEB21PP5/TR	Tape and Reel

**Note:** Contact your Microchip sales representative for the minimum quantity order

## 6. Revision History

Table 6-1. Revision History

Revision	Date	Description
A	04/2022	Document created.

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