SAM9X60 System-in-Package (SiP) MPU with up to 1-Gbit DDR2 SDRAM and up to 64-Mbit SDR SDRAM

SAM9X60 SiP Data Sheet

Product Page Links

Scope

This document is an overview of the main features of the SAM9X60 SiP microprocessor. The sole reference documents for product information on the SAM9X60 and the DDR2/SDR SDRAM memories are listed in Reference Documents.

Introduction

The SAM9X60 SiP integrates the ARM926EJ-S™ Arm® Thumb® processor-based SAM9X60 MPU with up to 1-Gbit DDR2 SDRAM or 64-Mbit SDR SDRAM in a single package.

By combining the SAM9X60 with DDR2/SDR SDRAM in a single package, PCB routing complexity, area and number of layers are reduced in the majority of cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

DDR2 SDRAM memory sizes and package options available:

- 512-Mbit and 1-Gbit DDR2 SDRAM, TFBGA233

SDR SDRAM memory sizes and package options available:

- 64-Mbit SDRAM, TFBGA196

While the smallest option targets applications with a small OS or bare metal, the larger options are suitable for applications using Linux®.

Reference Documents

Type	Document Title	Available	Literature No.
Data sheet	SAM9X60	www.microchip.com	DS60001579
Errata sheet	SAM9X60 Device Silicon Errata and Data Sheet Clarification	www.microchip.com	DS80000846
Data sheet	8 Mwords × 4 Banks × 16 bits DDR2 SDRAM (512 Mbits)	www.winbond.com	W9751G6KB
Data sheet	8 Mwords × 8 Banks × 16 bits DDR2 SDRAM (1 Gbit)	www.winbond.com	W971GG6SB
Data sheet	1 Mword x 4 Banks x 16 bits SDR SDRAM (64 Mbits)	www.winbond.com	W9864G6KH

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1. Features

- CPU
  - ARM926EJ-S Arm Thumb processor running up to 600 MHz
  - 32-Kbyte data cache, 32-Kbyte instruction cache, Memory Management Unit (MMU)
- Memories
  - One 160-Kbyte internal ROM
    - 64-Kbyte internal ROM embedding a secure bootloader program supporting boot on NAND Flash, SD card, SPI or QSPI Flash. Bootloader features selectable by OTP bits.
    - 96-Kbyte ROM for NAND Flash BCH ECC table
  - DDR2 SDRAM memory up to 1-Gbit or 64-Mbit SDR SDRAM memory, 16-bit data bus
  - One 64-Kbyte internal SRAM (SRAM0), single-cycle access at system speed
  - High Bandwidth Multi-port DDR2/LPDDR Controller (MPDDRC)
  - 8-bit External Bus Interface (EBI) supporting 8-bit NAND Flash connected on D16-D23
  - NAND Flash Controller, with up to 24-bit Programmable Multi-bit Error Correcting Code (PMECC)
  - One 11-Kbyte OTP memory for secure key storage with Emulation mode (OTP bits are emulated by a 4-Kbyte SRAM (SRAM1))
- System Running up to 200 MHz
  - Power-on Reset cells, Reset Controller, Shutdown Controller, Periodic Interval Timer, Watchdog Timer running on internal low-power 32-kHz RC and Real Time Clock running on external crystal
  - Two internal trimmed RC oscillators: 32 kHz (low-power) and 12 MHz
  - Two selectable crystal oscillators: 32.768 kHz (low-power) and 8 to 50 MHz
  - One PLL for the system and one PLL optimized for USB high-speed operation (480 MHz)
  - One dual-port 16-channel DMA Controller (XDMAC)
  - Advanced Interrupt Controller (AIC) and Debug Unit (DBGU)
  - JTAG port with disable bit in OTP memory
  - Two programmable external clock signals
- Low Power Modes
  - Backup mode with RTC, eight 32-bit general purpose backup registers, and Shutdown Controller to control the external power supply
  - Clock Generator and Power Management Controller
  - Software-programmable Ultra-Low Power modes: Very Slow Clock Operating Mode (ULP0), and No-Clock Operating Mode (ULP1) with fast wake-up capabilities
  - Software programmable power optimization capabilities
- Peripherals
  - LCD Controller with overlay, alpha-blending, rotation, scaling and color conversion. Up to 1024 x 768 resolution
  - 2D Graphics Controller supporting Fill BLT, Copy BLT, Transparent BLT, Blend/Alpha BLT, ROP4 BLT (Raster Operations) and Command Ring Buffer
  - ITU-R BT. 601/656, up to 12-bit Image Sensor Interface (ISI)
  - One USB Device High Speed, three USB Host High Speed with dedicated On-Chip Transceivers

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  - Two 10/100 Mbps Ethernet Mac Controller
  - Two 4-bit Secure Digital MultiMedia Card Controller (SDMMC)
  - Two CAN Controllers
  - One Quad I/O SPI Controller
  - Two three-channel 32-bit Timer/Counters
  - One high resolution (64-bit) Periodic Interval Timer
  - One Synchronous Serial Controller
  - One Inter-IC Sound (I^2S) Multi-Channel Controller (I2SMCC) with TDM support
  - One Audio Class D Controller with Single-Ended (SE) or Bridge Tied Load (BTL) connection to power stage
  - One four-channel 16-bit PWM Controller
  - Thirteen FLEXCOMs (USART, SPI and TWI)
  - One 12-channel 12-bit Analog-to-Digital Converter with 4/5 wires resistive touchscreen support
- Hardware Cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512): compliant with FIPS PUB 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197
  - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
- I/O Ports
  - Four 32-bit Parallel Input/Output Controllers
  - Up to 112 programmable I/O Lines multiplexed with up to three peripheral I/Os
  - Input change interrupt capability on each I/O line, optional Schmitt trigger input
  - Individually programmable open-drain, pull-up and pull-down resistor, synchronous output
  - General-purpose analog and digital inputs tolerant to positive and negative current injection
- Package
  - DDR2 SDRAM variant: 233-ball BGA, 14x14 mm^2, 0.8 mm pitch, optimized for standard class PCB layout (down to 2 layers)
  - SDR SDRAM variant: 196-ball BGA, 11x11 mm^2, 0.65 mm pitch, optimized for standard class PCB layout (down to 4 layers)
- Design for Low Electromagnetic Interference (EMI)
  - Slew rate controlled I/Os
  - DDR/SDR Phy with impedance-calibrated drivers
  - Spread spectrum PLLs
  - Careful BGA power/ground ball assignment to provide optimum decoupling capacitors placement
- Operating Conditions
  - Ambient temperature range (T_A): -40°C to +85°C
  - Junction temperature range (T_J) : -40°C to +125°C

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2. DDR2 SDRAM Features

- Part Numbers:
  - 1-Gbit DDR2 SDRAM device (SAM9X60D1G-I): Winbond W971G16SG2-5I
  - 512-Mbit DDR2 SDRAM device (SAM9X60D5M-I): Winbond W975116KG2-5I
- Power Supply: DDRM_VDD = 1.8V ±0.1V
- Double Data Rate Architecture: Two Data Transfers per Clock Cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-Directional, Differential Data Strobes (DQS and DQSN) are Transmitted/Received with Data
- Edge-Aligned with Read Data and Center-Aligned with Write Data
- DLL Aligns DQ and DQS Transitions with Clock
- Differential Clock Inputs (CLK and CLKN)
- Data Masks (DM) for Write Data
- Commands Entered on Each Positive CLK Edge, Data and Data Mask are Referenced to Both Edges of DQS
- Auto-Refresh and Self-Refresh Modes
- Precharged Power-Down and Active Power-Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

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3. SDR SDRAM Features

- Part Number:
  - 64-Mbit SDR SDRAM device (SAM9X60D6K-I): Winbond W986416KG-5I
- Power Supply: DDRM_VDD = 3.3V ±0.3V
- 1,048,576 Words x 4 Banks x 16 Bits Organization
- Self-Refresh Current: Standard and Low-Power
- CAS Latency: 2 and 3
- Burst Length: 1
- Sequential Burst
- Byte Data Controlled by LDQM, UDQM
- Controlled Precharge
- Burst Read Operation
- 4K Refresh Cycles/16 ms

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4. Configuration Summary

Feature	SAM9X60D5M	SAM9X60D1G	SAM9X60D6K
Package	TFBGA233, 14x14 mm², 0.80-mm pitch		TFBGA196, 11x11 mm², 0.65-mm pitch
Embedded SDRAM	512-Mbit DDR2 SDRAM	1-Gbit DDR2 SDRAM	64-Mbit SDR SDRAM
DRAM Data Bus	16 bits		
Core	ARM926EJ @ 600MHz		
SRAM0 + SRAM1	64 Kbytes + 4 Kbytes		
L1 Cache (I + D)	32 Kbytes + 32 Kbytes		
External Bus I/F	NAND Flash connected on D16-D23		
Camera I/F (ISI)	1x 12-bit		
EMAC 10/100	1x MII / RMII + 1x RMII		
USB	3x HS Transceivers 2x Host + 1x (H or D)		
CAN	2x		
LCD / GFX2D	24-bit RGB Up to 1024 x 768 @ 60 fps		
SDIO / SD card / e.MMC	2x (4-bit / up to 52 MHz)		
ADC	1x 12-bit ADC		
Serial I/F	13x FLEXCOM		
DDR QSPI	1x		
Audio Peripherals SSC / I2S /CLASSD	1 / 1 / 1		
Security	TDES / AES / SHA + Secure Bootloader		

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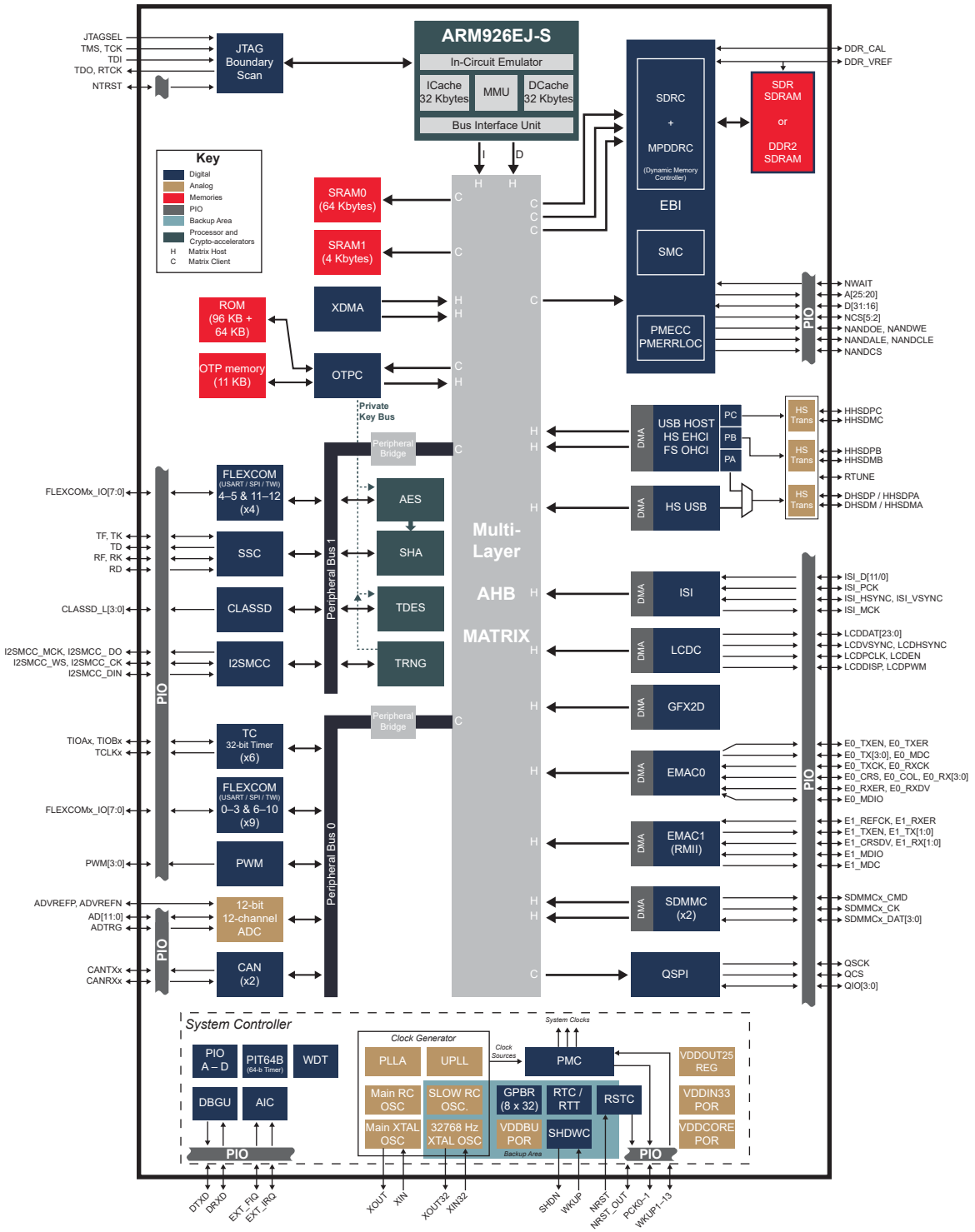
5. Block Diagram

Figure 5-1. SAM9X60 SiP Series Block Diagram



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6. Chip Identifier

Table 6-1. SAM9X60 SiP Chip ID Registers

Chip Name	Memory Type	Memory Size	DBGU_CIDR	DBGU_EXID
SAM9X60D5M	DDR2 SDRAM	512 Mbits	0x819B35A1 or 0x819B35A2	0x00000001
SAM9X60D5M-SL1				0x000000C8
SAM9X60D5M-SL2				0x000000C9
SAM9X60D5M-SL3				0x000000CA
SAM9X60D1G		1 Gbit		0x00000010
SAM9X60D1G-SL1				0x000000CC
SAM9X60D1G-SL2				0x000000CD
SAM9X60D1G-SL3				0x000000CE
SAM9X60D6K	SDR SDRAM	64 Mbits		0x00000011
SAM9X60D6K-SL1				0x000000C0
SAM9X60D6K-SL2				0x000000C1
SAM9X60D6K-SL3				0x000000C2

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7. Packages and Ballout

7.1. Packages

The SAM9X60 SiP is available in the packages listed in the following table.

Table 7-1. SAM9X60 SiP Packages

Package Name	Ball Count	Ball Pitch	Package Size	Memory Type
TFBGA233	233	0.80 mm	14 x 14 mm²	DDR2
TFBGA196	196	0.65 mm	11 x 11 mm²	SDRAM

For further details, see Mechanical Characteristics.

7.2. Ballout

Figure 7-1. BGA233 Ballout

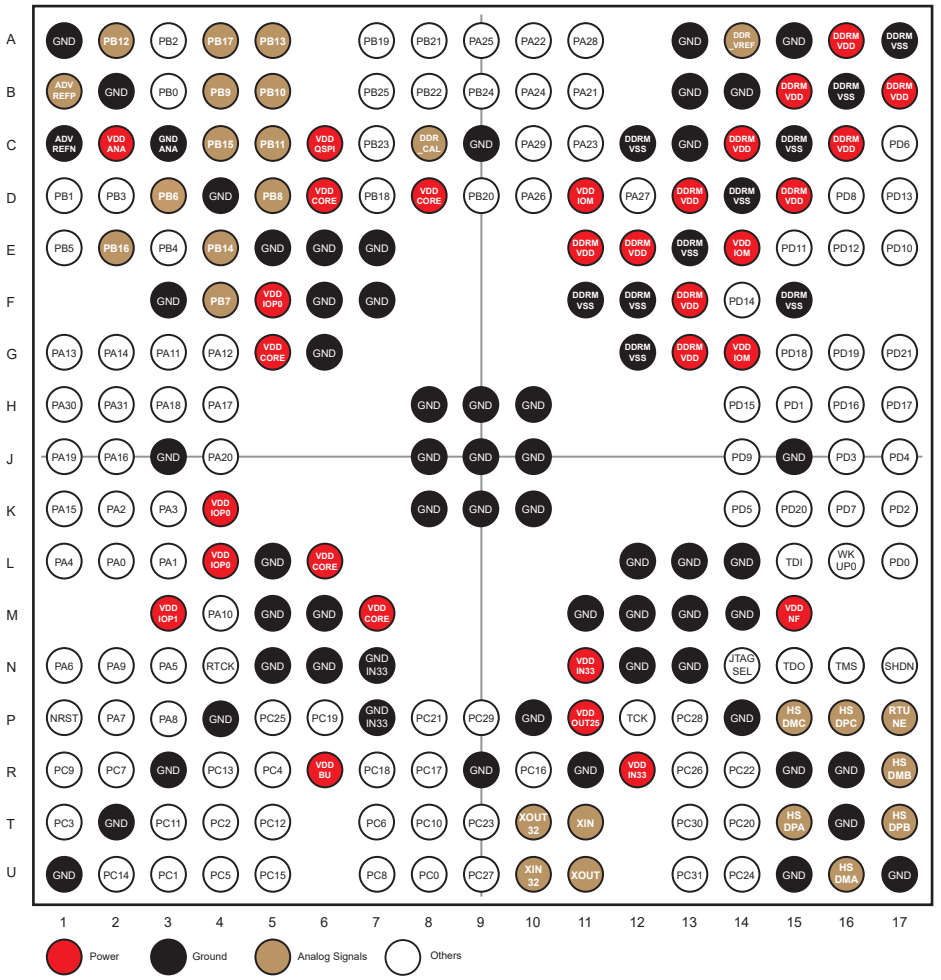

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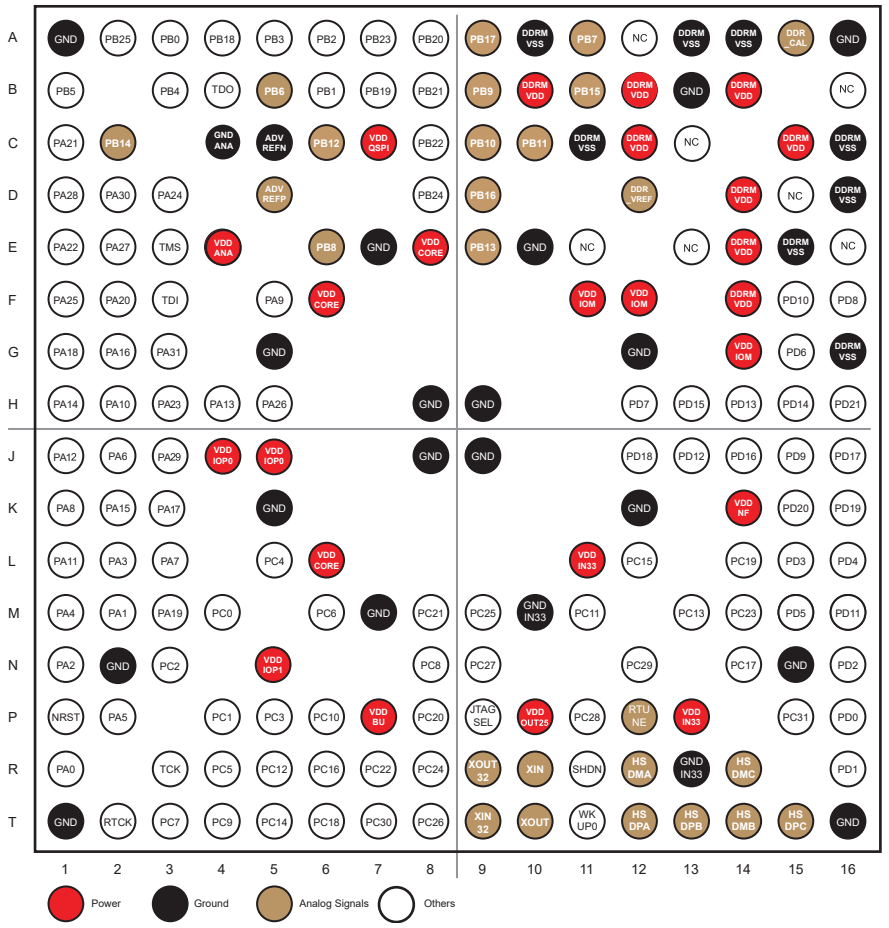
Figure 7-2. BGA196 Ballout



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7.3. Ball Description

Table 7-2. Ball Description

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
R1	L2	VDDIOP0	GPIO	PA0	I/O	–	–	A	FLEXCOM0_IO0	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO4	O	
								C	FLEXCOM4_IO4	O	
M2	L3	VDDIOP0	GPIO	PA1	I/O	–	–	A	FLEXCOM0_IO1	I/O	PIO, I, PU, ST
								B	FLEXCOM4_IO5	O	
N1	K2	VDDIOP0	GPIO	PA2	I/O	WKUP1	–	A	FLEXCOM0_IO4	O	PIO, I, PU, ST
								B	SDMMC1_DAT1	I/O	
								C	E0_TX0	O	
L2	K3	VDDIOP0	GPIO	PA3	I/O	–	–	A	FLEXCOM0_IO3	I/O	PIO, I, PU, ST
								B	SDMMC1_DAT2	I/O	
								C	E0_TX1	O	
M1	L1	VDDIOP0	GPIO	PA4	I/O	–	–	A	FLEXCOM0_IO2	I/O	PIO, I, PU, ST
								B	SDMMC1_DAT3	I/O	
								C	E0_TXER	O	
P2	N3	VDDIOP0	GPIO	PA5	I/O	–	–	A	FLEXCOM1_IO0	I/O	PIO, I, PU, ST
								B	CANTX1	O	
J2	N1	VDDIOP0	GPIO	PA6	I/O	–	–	A	FLEXCOM1_IO1	I/O	PIO, I, PU, ST
								B	CANRX1	I	
L3	P2	VDDIOP0	GPIO	PA7	I/O	–	–	A	FLEXCOM2_IO0	I/O	PIO, I, PU, ST
								B	FLEXCOM4_IO4	O	
								C	FLEXCOM5_IO4	O	
K1	P3	VDDIOP0	GPIO	PA8	I/O	–	–	A	FLEXCOM2_IO1	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO3	I/O	
								C	FLEXCOM4_IO5	O	
F5	N2	VDDIOP0	GPIO	PA9	I/O	WKUP2	–	A	DRXD	I	PIO, I, PU, ST
								B	CANRX0	I	
H2	M4	VDDIOP0	GPIO	PA10	I/O	WKUP3	–	A	DTXD	O	PIO, I, PU, ST
								B	CANTX0	O	
L1	G3	VDDIOP0	GPIO	PA11	I/O	–	–	A	FLEXCOM4_IO1	I/O	PIO, I, PU, ST
								B	SDMMC1_DAT0	I/O	
J1	G4	VDDIOP0	GPIO	PA12	I/O	–	–	A	FLEXCOM4_IO0	I/O	PIO, I, PU, ST
								B	SDMMC1_CMD	I/O	
H4	G1	VDDIOP0	GPIO	PA13	I/O	–	–	A	FLEXCOM4_IO2	I/O	PIO, I, PU, ST
								B	SDMMC1_CK	I/O	
H1	G2	VDDIOP0	GPIO	PA14	I/O	–	–	A	FLEXCOM4_IO3	I/O	PIO, I, PU, ST
K2	K1	VDDIOP0	GPIO	PA15	I/O	–	–	A	SDMMC0_DAT0	I/O	PIO, I, PU, ST

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
G2	J2	VDDIOP0	GPIO	PA16	I/O	–	–	A	SDMMC0_CMD	I/O	PIO, I, PU, ST
K3	H4	VDDIOP0	GPIO	PA17	I/O	–	–	A	SDMMC0_CK	I/O	PIO, I, PU, ST
G1	H3	VDDIOP0	GPIO	PA18	I/O	–	–	A	SDMMC0_DAT1	I/O	PIO, I, PU, ST
M3	J1	VDDIOP0	GPIO	PA19	I/O	–	–	A	SDMMC0_DAT2	I/O	PIO, I, PU, ST
F2	J4	VDDIOP0	GPIO	PA20	I/O	–	–	A	SDMMC0_DAT3	I/O	PIO, I, PU, ST
C1	B11	VDDIOP0	GPIO	PA21	I/O	–	–	A	TIOA0	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO1	I/O	
E1	A10	VDDIOP0	GPIO	PA22	I/O	–	–	A	TIOA1	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO0	I/O	
H3	C11	VDDIOP0	GPIO	PA23	I/O	–	–	A	TIOA2	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO2	I/O	
D3	B10	VDDIOP0	GPIO	PA24	I/O	–	–	A	TCLK0	I	PIO, I, PU, ST
								B	TK	I/O	
								C	CLASSD_L0	O	
F1	A9	VDDIOP0	GPIO	PA25	I/O	–	–	A	TCLK1	I	PIO, I, PU, ST
								B	TF	I/O	
								C	CLASSD_L1	O	
H5	D10	VDDIOP0	GPIO	PA26	I/O	–	–	A	TCLK2	I	PIO, I, PU, ST
								B	TD	O	
								C	CLASSD_L2	O	
E2	D12	VDDIOP0	GPIO	PA27	I/O	–	–	A	TIOB0	I/O	PIO, I, PU, ST
								B	RD	I	
								C	CLASSD_L3	O	
D1	A11	VDDIOP0	GPIO	PA28	I/O	WKUP4	–	A	TIOB1	I/O	PIO, I, PU, ST
								B	RK	I/O	
J3	C10	VDDIOP0	GPIO	PA29	I/O	–	–	A	TIOB2	I/O	PIO, I, PU, ST
								B	RF	I/O	
								C	FLEXCOM2_IO7	I	
D2	H1	VDDIOP0	GPIO	PA30	I/O	–	–	A	FLEXCOM6_IO0	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO6	O	
								C	E0_MDC	O	
G3	H2	VDDIOP0	GPIO	PA31	I/O	–	–	A	FLEXCOM6_IO1	I/O	PIO, I, PU, ST
								B	FLEXCOM5_IO5	O	
								C	E0_TXEN	O	
A3	B3	VDDANA	GPIO	PB0	I/O	WKUP5	–	A	E0_RX0	I	PIO, I, PU, ST
								B	FLEXCOM2_IO4	O	
B6	D1	VDDANA	GPIO	PB1	I/O	–	–	A	E0_RX1	I	PIO, I, PU, ST
								B	FLEXCOM2_IO3	I/O	

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
A6	A3	VDDANA	GPIO	PB2	I/O	–	–	A	E0_RXER	I	PIO, I, PU, ST
								B	FLEXCOM2_IO2	I/O	
A5	D2	VDDANA	GPIO	PB3	I/O	WKUP6	–	A	E0_RXDV	I	PIO, I, PU, ST
								B	FLEXCOM4_IO6	O	
B3	E3	VDDANA	GPIO	PB4	I/O	–	–	A	E0_TXCK	I/O	PIO, I, PU, ST
								B	FLEXCOM8_IO0	I/O	
B1	E1	VDDANA	GPIO	PB5	I/O	–	–	A	E0_MDIO	I/O	PIO, I, PU, ST
								B	FLEXCOM8_IO1	I/O	
B5	D3	VDDANA	GPIO	PB6	I/O	AD7	–	A	E0_MDC	O	PIO, I, PU, ST
								B	FLEXCOM0_IO7		
A11	F4	VDDANA	GPIO	PB7	I/O	AD8	–	A	E0_TXEN	O	PIO, I, PU, ST
E6	D5	VDDANA	GPIO	PB8	I/O	AD9	–	A	E0_TXER	O	PIO, I, PU, ST
B9	B4	VDDANA	GPIO	PB9	I/O	AD10	–	A	E0_TX0	O	PIO, I, PU, ST
								B	PCK1	O	
C9	B5	VDDANA	GPIO	PB10	I/O	AD11	–	A	E0_TX1	O	PIO, I, PU, ST
								B	PCK0	O	
C10	C5	VDDANA	GPIO	PB11	I/O	AD0	–	A	E0_TX2	O	PIO, I, PU, ST
								B	PWM0	O	
C6	A2	VDDANA	GPIO	PB12	I/O	AD1	–	A	E0_TX3	O	PIO, I, PU, ST
								B	PWM1	O	
E9	A5	VDDANA	GPIO	PB13	I/O	AD2	–	A	E0_RX2	I	PIO, I, PU, ST
								B	PWM2	O	
C2	E4	VDDANA	GPIO	PB14	I/O	AD3	–	A	E0_RX3	I	PIO, I, PU, ST
								B	PWM3	O	
B11	C4	VDDANA	GPIO	PB15	I/O	AD4	–	A	E0_RXCK	I	PIO, I, PU, ST
D9	E2	VDDANA	GPIO	PB16	I/O	AD5	–	A	E0_CRS	I	PIO, I, PU, ST
A9	A4	VDDANA	GPIO	PB17	I/O	AD6	–	A	E0_COL	I	PIO, I, PU, ST
A4	D7	VDDANA	GPIO	PB18	I/O	WKUP7	–	A	IRQ	I	PIO, I, PU, ST
								B	ADTRG	I	
B7	A7	VDDQSPI	GPIO	PB19	I/O	–	–	A	QSCK	O	PIO, I, PU, ST
								B	I2SMCC_CK	I/O	
								C	FLEXCOM11_IO0	I/O	
A8	D9	VDDQSPI	GPIO	PB20	I/O	–	–	A	QCS	O	PIO, I, PU, ST
								B	I2SMCC_WS	I/O	
								C	FLEXCOM11_IO1	I/O	
B8	A8	VDDQSPI	GPIO	PB21	I/O	–	–	A	QIO0	I/O	PIO, I, PU, ST
								B	I2SMCC_DIN0	I	
								C	FLEXCOM12_IO0	I/O	

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
C8	B8	VDDQSPI	GPIO	PB22	I/O	–	–	A	QIO1	I/O	PIO, I, PU, ST
								B	I2SMCC_DOUT0	O	
								C	FLEXCOM12_IO1	I/O	
A7	C7	VDDQSPI	GPIO	PB23	I/O	–	–	A	QIO2	I/O	PIO, I, PU, ST
								B	I2SMCC_MCK	O	
D8	B9	VDDQSPI	GPIO	PB24	I/O	–	–	A	QIO3	I/O	PIO, I, PU, ST
A2	B7	VDDIOP0	GPIO	PB25	I/O	WKUP8	–	A	NRST_OUT	O	NRST_OUT, O, PD
								B	NTRST	I	
M4	U8	VDDIOP1	GPIO	PC0	I/O	–	–	A	LCDDAT0	O	PIO, I, PU, ST
								B	ISI_D0	I	
								C	FLEXCOM7_IO0	I/O	
P4	U3	VDDIOP1	GPIO	PC1	I/O	–	–	A	LCDDAT1	O	PIO, I, PU, ST
								B	ISI_D1	I	
								C	FLEXCOM7_IO1	I/O	
N3	T4	VDDIOP1	GPIO	PC2	I/O	–	–	A	LCDDAT2	O	PIO, I, PU, ST
								B	ISI_D2	I	
								C	TIOA3	I/O	
P5	T1	VDDIOP1	GPIO	PC3	I/O	–	–	A	LCDDAT3	O	PIO, I, PU, ST
								B	ISI_D3	I	
								C	TIOB3	I/O	
L5	R5	VDDIOP1	GPIO	PC4	I/O	–	–	A	LCDDAT4	O	PIO, I, PU, ST
								B	ISI_D4	I	
								C	TCLK3	I	
R4	U4	VDDIOP1	GPIO	PC5	I/O	–	–	A	LCDDAT5	O	PIO, I, PU, ST
								B	ISI_D5	I	
								C	TIOA4	I/O	
M6	T7	VDDIOP1	GPIO	PC6	I/O	–	–	A	LCDDAT6	O	PIO, I, PU, ST
								B	ISI_D6	I	
								C	TIOB4	I/O	
T3	R2	VDDIOP1	GPIO	PC7	I/O	–	–	A	LCDDAT7	O	PIO, I, PU, ST
								B	ISI_D7	I	
								C	TCLK4	I	
N8	U7	VDDIOP1	GPIO	PC8	I/O	–	–	A	LCDDAT8	O	PIO, I, PU, ST
								B	ISI_D8	I	
								C	FLEXCOM9_IO0	I/O	
T4	R1	VDDIOP1	GPIO	PC9	I/O	–	–	A	LCDDAT9	O	PIO, I, PU, ST
								B	ISI_D9	I	
								C	FLEXCOM9_IO1	I/O	

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
P6	T8	VDDIOP1	GPIO	PC10	I/O	–	–	A	LCDDAT10	O	PIO, I, PU, ST
								B	ISI_D10	I	
								C	PWM0	O	
M11	T3	VDDIOP1	GPIO	PC11	I/O	–	–	A	LCDDAT11	O	PIO, I, PU, ST
								B	ISI_D11	I	
								C	PWM1	O	
R5	T5	VDDIOP1	GPIO	PC12	I/O	–	–	A	LCDDAT12	O	PIO, I, PU, ST
								B	ISI_PCK	I	
								C	TIOA5	I/O	
M13	R4	VDDIOP1	GPIO	PC13	I/O	–	–	A	LCDDAT13	O	PIO, I, PU, ST
								B	ISI_VSYNC	I	
								C	TIOB5	I/O	
T5	U2	VDDIOP1	GPIO	PC14	I/O	–	–	A	LCDDAT14	O	PIO, I, PU, ST
								B	ISI_HSYNC	I	
								C	TCLK5	I	
L12	U5	VDDIOP1	GPIO	PC15	I/O	–	–	A	LCDDAT15	O	PIO, I, PU, ST
								B	ISI_MCK	O	
								C	PCK0	O	
R6	R10	VDDIOP1	GPIO	PC16	I/O	–	–	A	LCDDAT16	O	PIO, I, PU, ST
								B	E1_RXER	I	
								C	FLEXCOM10_IO0	I/O	
N14	R8	VDDIOP1	GPIO	PC17	I/O	–	–	A	LCDDAT17	O	PIO, I, PU, ST
								B	FLEXCOM1_IO7	I	
								C	FLEXCOM10_IO1	I/O	
T6	R7	VDDIOP1	GPIO	PC18	I/O	–	–	A	LCDDAT18	O	PIO, I, PU, ST
								B	E1_TX0	O	
								C	PWM0	O	
L14	P6	VDDIOP1	GPIO	PC19	I/O	–	–	A	LCDDAT19	O	PIO, I, PU, ST
								B	E1_TX1	O	
								C	PWM1	O	
P8	T14	VDDIOP1	GPIO	PC20	I/O	–	–	A	LCDDAT20	O	PIO, I, PU, ST
								B	E1_RX0	I	
								C	PWM2	O	
M8	P8	VDDIOP1	GPIO	PC21	I/O	–	–	A	LCDDAT21	O	PIO, I, PU, ST
								B	E1_RX1	I	
								C	PWM3	O	
R7	R14	VDDIOP1	GPIO	PC22	I/O	–	–	A	LCDDAT22	O	PIO, I, PU, ST
								B	FLEXCOM3_IO0	I/O	

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
M14	T9	VDDIOP1	GPIO	PC23	I/O	–	–	A	LCDDAT23	O	PIO, I, PU, ST
								B	FLEXCOM3_IO1	I/O	
R8	U14	VDDIOP1	GPIO	PC24	I/O	WKUP9	–	A	LCDDISP	O	PIO, I, PU, ST
								B	FLEXCOM3_IO4	O	
M9	P5	VDDIOP1	GPIO	PC25	I/O	WKUP10	–	A	–	–	PIO, I, PU, ST
								B	FLEXCOM3_IO3	I/O	
T8	R13	VDDIOP1	GPIO	PC26	I/O	–	–	A	LCDPWM	O	PIO, I, PU, ST
								B	FLEXCOM3_IO2	I/O	
N9	U9	VDDIOP1	GPIO	PC27	I/O	–	–	A	LCDVSYNC	O	PIO, I, PU, ST
								B	E1_TXEN	O	
								C	FLEXCOM1_IO4	O	
P11	P13	VDDIOP1	GPIO	PC28	I/O	–	–	A	LCDHSYNC	O	PIO, I, PU, ST
								B	E1_CRSDV	I	
								C	FLEXCOM1_IO3	I/O	
N12	P9	VDDIOP1	GPIO	PC29	I/O	–	–	A	LCDDEN	O	PIO, I, PU, ST
								B	E1_TXCK	I/O	
								C	FLEXCOM1_IO2	I/O	
T7	T13	VDDIOP1	GPIO	PC30	I/O	–	–	A	LCDPCK	O	PIO, I, PU, ST
								B	E1_MDC	O	
								C	FLEXCOM3_IO7	I	
P15	U13	VDDIOP1	GPIO	PC31	I/O	WKUP11	–	A	FIQ	I	PIO, I, PU, ST
								B	E1_MDIO	I/O	
								C	PCK1	O	
P16	L17	VDDNF	GPIO	PD0	I/O	–	–	A	NANDOE	O	PIO, I, PU, ST
R16	H15	VDDNF	GPIO	PD1	I/O	–	–	A	NANDWE	O	PIO, I, PU, ST
N16	K17	VDDNF	GPIO	PD2	I/O	–	–	A	A21/NANDALE	O	A21,O, PD, ST
L15	J16	VDDNF	GPIO	PD3	I/O	–	–	A	A22/NANDCLE	O	A22,O, PD
L16	J17	VDDNF	GPIO	PD4	I/O	–	–	A	NCS3/NANDCS	O	PIO, I, PU, ST
M15	K14	VDDNF	GPIO	PD5	I/O	–	–	A	NWAIT	I	PIO, I, PU, ST
G15	C17	VDDNF	GPIO	PD6	I/O	–	–	A	D16	I/O	PIO, I, PU, ST
H12	K16	VDDNF	GPIO	PD7	I/O	–	–	A	D17	I/O	PIO, I, PU, ST
F16	D16	VDDNF	GPIO	PD8	I/O	–	–	A	D18	I/O	PIO, I, PU, ST
J15	J14	VDDNF	GPIO	PD9	I/O	–	–	A	D19	I/O	PIO, I, PU, ST
F15	E17	VDDNF	GPIO	PD10	I/O	–	–	A	D20	I/O	PIO, I, PU, ST
M16	E15	VDDNF	GPIO	PD11	I/O	–	–	A	D21	I/O	PIO, I, PU, ST
J13	E16	VDDNF	GPIO	PD12	I/O	–	–	A	D22	I/O	PIO, I, PU, ST
H14	D17	VDDNF	GPIO	PD13	I/O	–	–	A	D23	I/O	PIO, I, PU, ST
H15	F14	VDDNF	GPIO	PD14	I/O	–	–	A	D24	I/O	PIO, I, PU, ST

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
H13	H14	VDDNF	GPIO	PD15	I/O	–	–	A	D25	I/O	A20, O, PD
								B	A20	O	
J14	H16	VDDNF	GPIO	PD16	I/O	–	–	A	D26	I/O	A23, O, PD
								B	A23	O	
J16	H17	VDDNF	GPIO	PD17	I/O	WKUP12	–	A	D27	I/O	A24, O, PD
								B	A24	O	
J12	G15	VDDNF	GPIO	PD18	I/O	WKUP13	–	A	D28	I/O	A25, O, PD
								B	A25	O	
K16	G16	VDDNF	GPIO	PD19	I/O	–	–	A	D29	I/O	PIO, I, PU, ST
								B	NCS2	O	
K15	K15	VDDNF	GPIO	PD20	I/O	–	–	A	D30	I/O	PIO, I, PU, ST
								B	NCS4	O	
H16	G17	VDDNF	GPIO	PD21	I/O	–	–	A	D31	I/O	PIO, I, PU, ST
								B	NCS5	O	
A15	C8	VDDIOM	–	DDR_CAL	I/O	–	–	–	–	–	I
D12	A14	VDDIOM	–	DDR_VREF	I/O	–	–	–	–	–	I
D5	B1	VDDANA	–	ADVREFP	I	–	–	–	–	–	I
C5	C1	VDDANA	–	ADVREFN	I	–	–	–	–	–	I
P12	P17	VDDIN33	–	RTUNE	I/O	–	–	–	–	–	I
T12	T15	VDDIN33	–	HHSDPA	I/O	DHSDP	–	–	–	–	O, PD
R12	U16	VDDIN33	–	HHSDMA	I/O	DHSDM	–	–	–	–	O, PD
T13	T17	VDDIN33	–	HHSDPB	I/O	–	–	–	–	–	O, PD
T14	R17	VDDIN33	–	HHSDMB	I/O	–	–	–	–	–	O, PD
T15	P16	VDDIN33	–	HHSDPC	I/O	–	–	–	–	–	O, PD
R14	P15	VDDIN33	–	HHSDMC	I/O	–	–	–	–	–	O, PD
T11	L16	VDDBU	–	WKUP0	I	–	–	–	–	–	I, ST
R11	N17	VDDBU	–	SHDN	O	–	–	–	–	–	O, PD
P9	N14	VDDBU	–	JTAGSEL	I	–	–	–	–	–	I, PD
R3	P12	VDDIOP0	–	TCK	I	–	–	–	–	–	I, ST
F3	L15	VDDIOP0	–	TDI	I	–	–	–	–	–	I, ST
B4	N15	VDDIOP0	–	TDO	O	–	–	–	–	–	O
E3	N16	VDDIOP0	–	TMS	I	–	–	–	–	–	I, ST
T2	N4	VDDIOP0	–	RTCK	O	–	–	–	–	–	O
P1	P1	VDDIOP0	–	NRST	I	–	–	–	–	–	I, PU, ST
T9	U10	VDDBU	–	XIN32	I	–	–	–	–	–	I
R9	T10	VDDBU	–	XOUT32	I/O	–	–	–	–	–	O
R10	T11	VDDIN33	–	XIN	I	–	–	–	–	–	I
T10	U11	VDDIN33	–	XOUT	I/O	–	–	–	–	–	O

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
F11, F12, G14	D11, E14, G14	VDDIOM	Power	–	–	–	–	–	–	–	–
A1, T1, N2, G5, K5, E7, M7, H8, J8, H9, J9, E10, G12, K12, B13, N15, A16, T16	A1, U1, B2, T2, F3, J3, R3, D4, P4, E5, L5, M5, N5, E6, F6, G6, M6, N6, E7, F7, H8, J8, K8, C9, H9, J9, K9, R9, H10, J10, K10, P10, M11, R11, L12, M12, N12, A13, B13, C13, L13, M13, N13, B14, L14, M14, P14, A15, J15, R15, U15, R16, T16, U17	GND	Ground	–	–	–	–	–	–	–	–
K14	M15	VDDNF	Power	–	–	–	–	–	–	–	–
J4, J5	K4, L4, F5	VDDIOP0	Power	–	–	–	–	–	–	–	–
N5	M3	VDDIOP1	Power	–	–	–	–	–	–	–	–
P7	R6	VDDBU	Power	–	–	–	–	–	–	–	–
E4	C2	VDDANA	Power	–	–	–	–	–	–	–	–
C4	C3	GNDANA	Ground	–	–	–	–	–	–	–	–
P10	P11	VDDOUT25	Output	–	–	–	–	–	–	–	–
L11, P13	R12, N11	VDDIN33	Power	–	–	–	–	–	–	–	–
M10, R13	P7, N7	GNDIN33	Ground	–	–	–	–	–	–	–	–
E8, F6, L6	G5, D6, L6, M7, D8	VDDCORE	Power	–	–	–	–	–	–	–	–
C7	C6	VDDQSPI	Power	–	–	–	–	–	–	–	–

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Table 7-2. Ball Description (continued)

196-ball BGA	233-ball BGA	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral			Reset State[1]
				Signal	Dir	Signal	Dir	Func	Signal	Dir	
B10, B12, B14, C12, C15, D14, E14, F14	D15, C16, B17, E11, E12, D13, F13, G13, C14, B15, A16	DDRM_VDD	Power	–	–	–	–	–	–	–	–
A10, A13, A14, C11, C16, D16, E15, G16	F15, F11, C12, F12, G12, E13, D14, C15, B16, A17	DDRM_VSS	Ground	–	–	–	–	–	–	–	–
E11, C13, E13, D15, B16, E16, A12	–	–	NC	–	–	–	–	–	–	–	–

Note:

1. PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger

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8. Memories

The SAM9X60 SiP is available with up to 1 Gbit of DDR2 SDRAM memory, and with up to 64 Mbits of SDR SDRAM memory. For the features of these memories, see DDR2 SDRAM Features and SDR SDRAM Features.

For power consumption, electrical characteristics and timings of these memories, refer to the data sheets referenced below on the manufacturer's website.

Table 8-1. Memory Data Sheet References

Memory Type	Density	Manufacturer Packaged PN	Data Sheet Literature Number
DDR2 SDRAM	512 Mbits	Winbond W9751G6KB25I	W9751G6KB
	1 Gbit	Winbond W971GG6SB25I	W971GG6SB
SDR SDRAM	64 Mbits	Winbond W9864G6KH	W9864G6KH (Speed Grade 5I)

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9. Electrical Characteristics

9.1. Decoupling

100 nF (min) decoupling capacitors must be added on each power supply pin, as close as possible to the device.

9.2. Power Sequences

The DDRM_VDD power rail must be connected to VDDIOM (1.8V or 3.3V) on the PCB. Refer to the section “Recommended Power Supply Sequencing” in the SAM9X60 data sheet (see Reference Documents).

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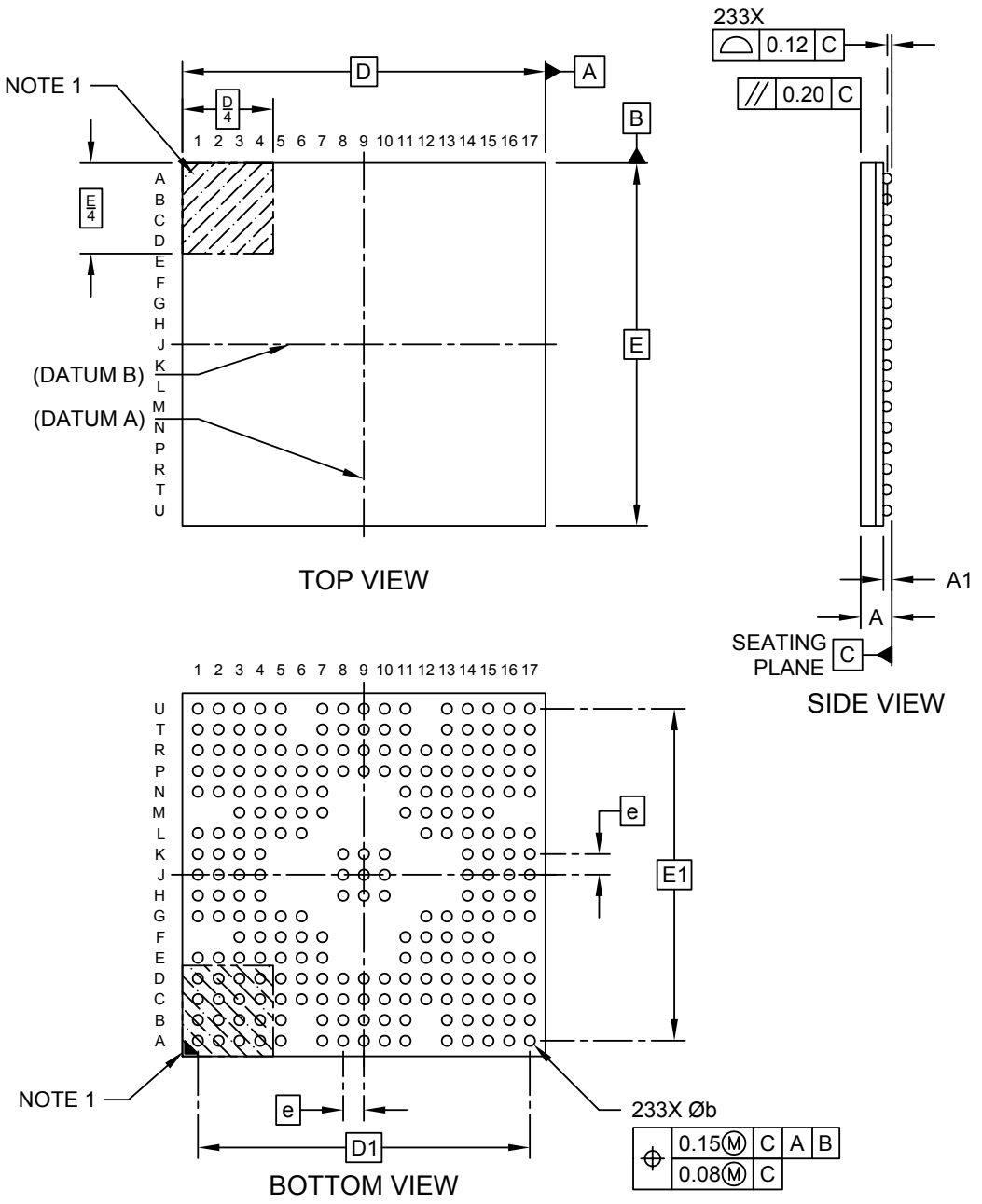
10. Mechanical Characteristics

10.1. 233-Ball TFBGA

233-Ball Thin Fine Pitch Ball Grid Array (4FB) - 14x14 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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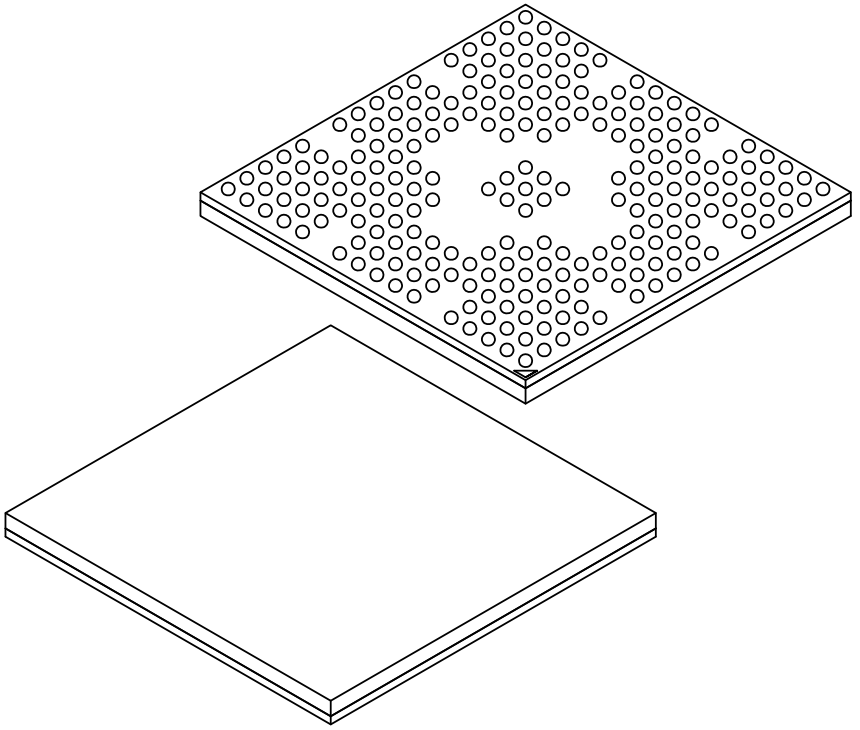
233-Ball Thin Fine Pitch Ball Grid Array (4FB) - 14x14 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		233	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.27	0.32	0.37
Overall Length	D		14.00 BSC	
Overall Ball Pitch	D1		12.80 BSC	
Overall Width	E		14.00 BSC	
Overall Ball Pitch	E1		12.80 BSC	
Terminal Width	b	0.38	0.40	0.48

Notes:

1. Terminal A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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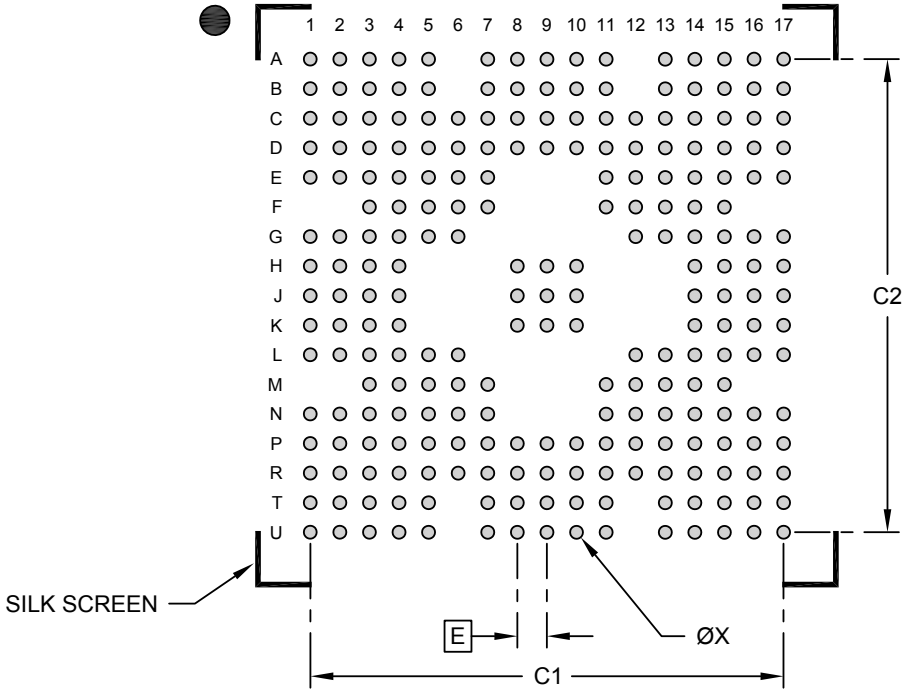
233-Ball Thin Fine Pitch Ball Grid Array (4FB) - 14x14 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		12.80	
Contact Pad Spacing	C2		12.80	
Contact Pad Width (Xnn)	X1			0.35

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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Table 10-1. 233-Ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 10-2. Device and 233-Ball TFBGA Package Weight

Device	Weight (mg)
SAM9X60D5M	394
SAM9X60D1G	399

Table 10-3. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

Table 10-4. 233-Ball TFBGA Package Information

Ball Land	0.45 ± 0.05 mm
Nominal Ball Diameter	0.4 mm
Solder Mask Opening	0.35 ± 0.03 mm
Solder Mask Definition	SMD
Solder	SAC105

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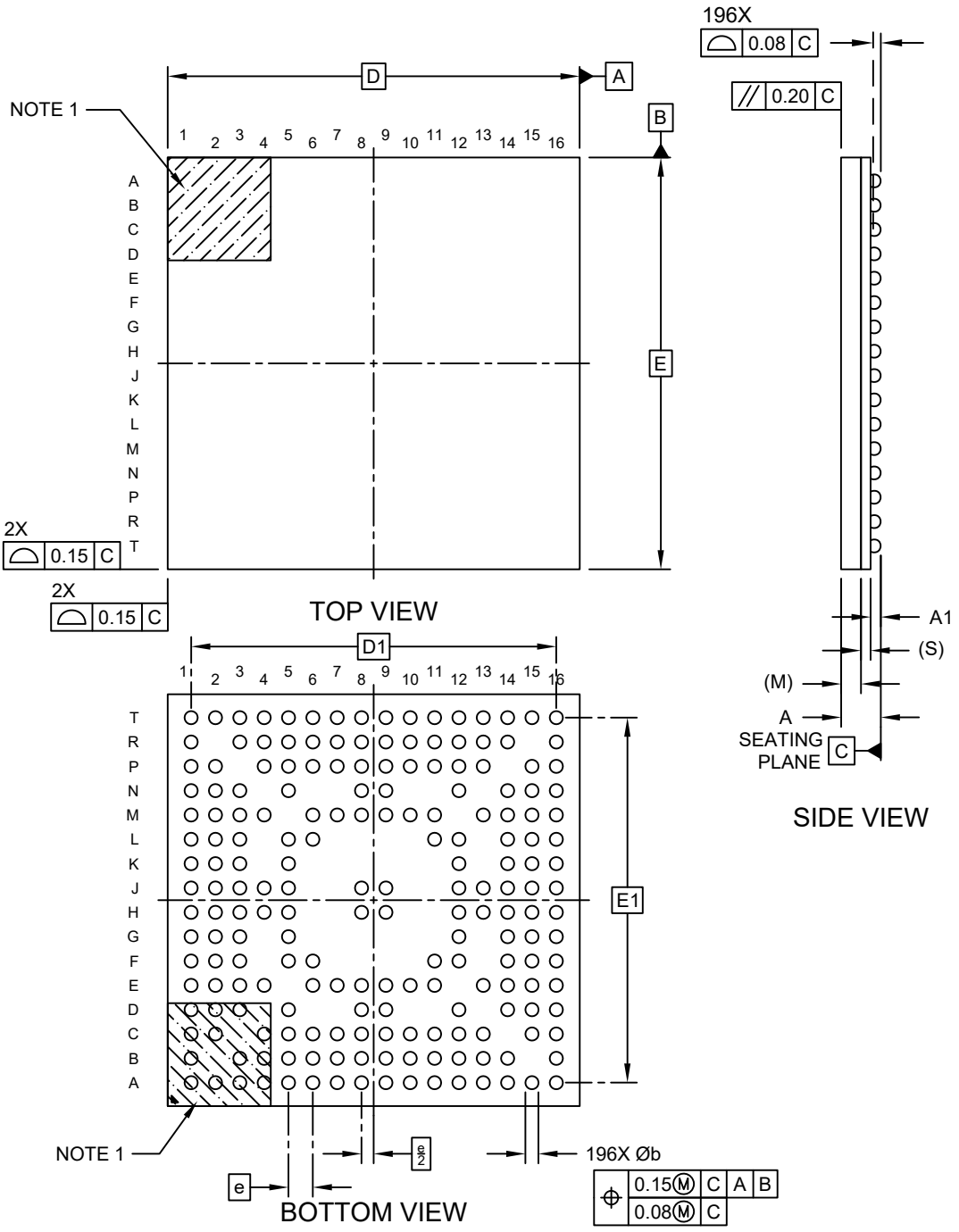
10.2. 196-Ball TFBGA

196-Lead Thin Fine Pitch Ball Grid Array (4GB) - 11x11x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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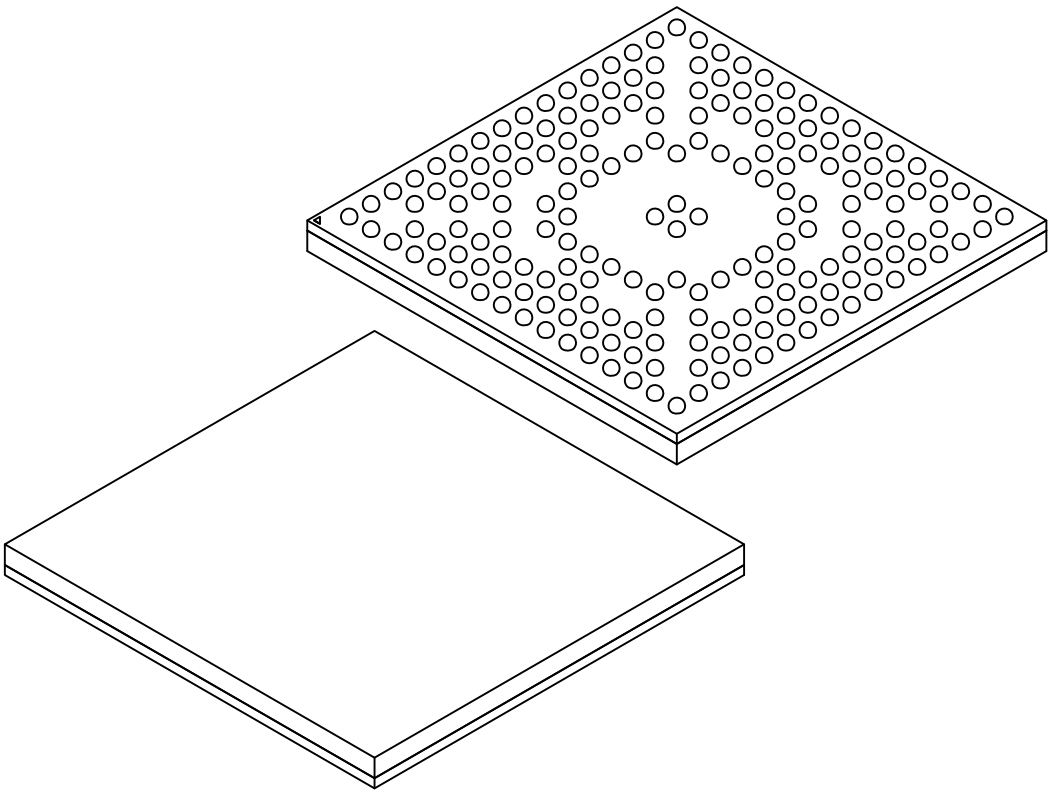
196-Lead Thin Fine Pitch Ball Grid Array (4GB) - 11x11x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		196	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.22	-	0.32
Substraight Thickness	S		0.26 REF	
Mold Cap Height	M		0.53 REF	
Overall Length	D		11.00 BSC	
Overall Terminal Pitch	D1		9.75 BSC	
Overall Width	E		11.00 BSC	
Overall Terminal Pitch	E1		9.75 BSC	
Terminal Diameter	b	0.32	-	0.42

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only, displayed in parentheses.

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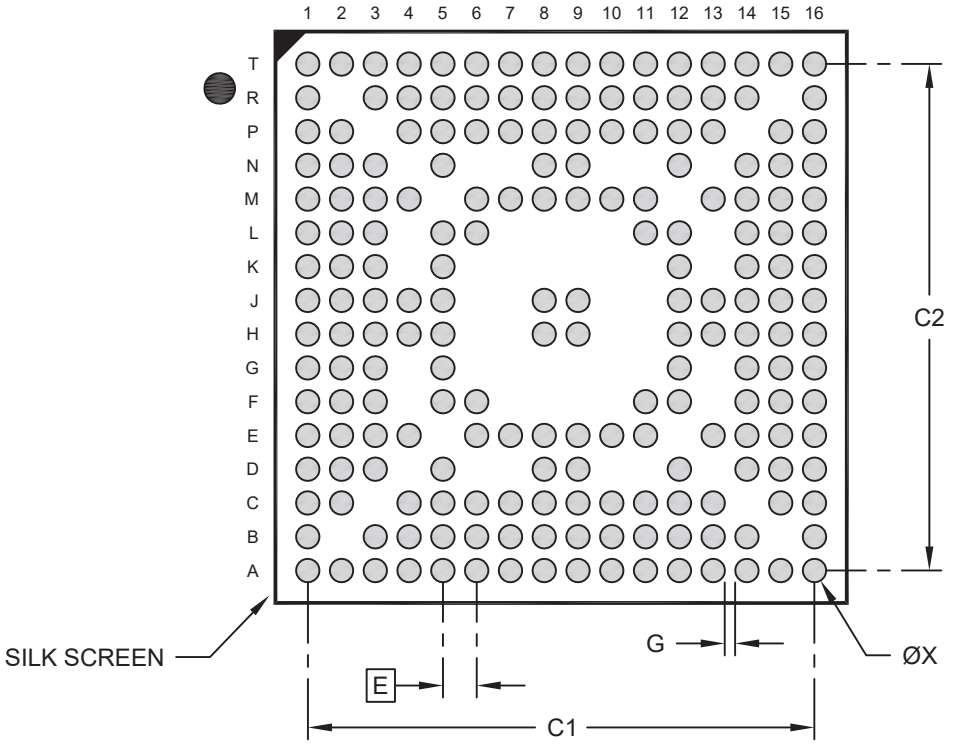
196-Lead Thin Fine Pitch Ball Grid Array (4GB) - 11x11x1.2 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		9.75	
Contact Pad Spacing	C2		9.75	
Contact Pad Width (X196)	X			0.45
Space Between Contact Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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Table 10-5. 196-Ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 10-6. Device and 196-Ball TFBGA Package Weight

Device	Weight (mg)
SAM9X60D6K	251

Table 10-7. Package Reference

JEDEC Drawing Reference	NA
J-STD-609 Classification	e8

Table 10-8. 196-Ball TFBGA Package Information

Ball Land	0.4 ± 0.05 mm
Nominal Ball Diameter	0.35 mm
Solder Mask Opening	0.30 ± 0.03 mm
Solder Mask Definition	SMD
Solder	SAC105

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11. Ordering Information

Table 11-1. Ordering Information

Ordering Code	Memory Type	Memory Size	Package	Operating Temperature Range
SAM9X60D5M(T)-I/4FB(-SLx)	DDR2 SDRAM	512 Mbits	TFBGA233	-40°C to +85°C
SAM9X60D1G(T)-I/4FB(-SLx)		1 Gbit		
SAM9X60D6K(T)-I/4GB(-SLx)	SDR SDRAM	64 Mbits	TFBGA196	

Notes:

1. For details on ordering codes, see Product Identification System.
2. For SL1, SL2 and SL3 device availability, contact a Microchip Sales representative.

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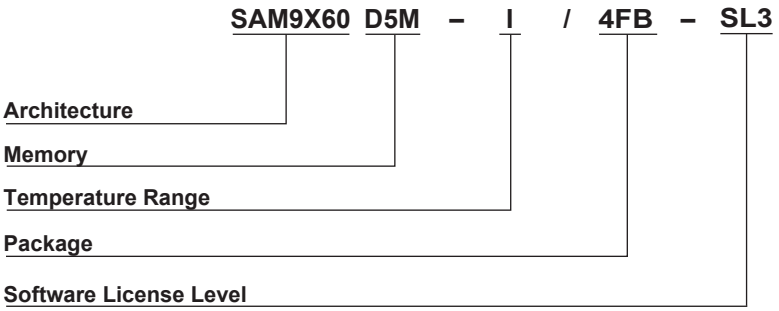
12. Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.



Architecture:	SAM9X60	= ARM926EJ-S Arm Thumb CPU
Memory Type and Size:	D5M	= 512-Mbit DDR2 SDRAM
	D1G	= 1-Gbit DDR2 SDRAM
	D6K	= 64-Mbit SDR SDRAM
Carrier Type:	Blank	= Standard packaging (tray)
	T	= Tape and Reel
Temperature Range:	I	= -40°C to +85°C (industrial)
Package:	4FB	= TFBGA233
	4GB	= TFBGA196
Software License Level:	Blank	= Standard
	SL1	= Level 1
	SL2	= Level 2
	SL3	= Level 3

Example:

- SAM9X60D5M-I/4FB-SL3: ARM926EJ-S Arm Thumb CPU, 512-Mbit DDR2 SDRAM, standard packaging, industrial temperature, 233-ball, TFBGA package, software license level 3

Note: The Tape and Reel identifier and the Software License Level identifier only appear in the catalog part number description. These identifiers are used for ordering purposes and are not printed on the device package. Check with your Microchip Sales Office for package availability.

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13. Revision History

13.1. DS60001580D - 11/2025

Section	Changes
Throughout the document	Introduced SL1, SL2, SL3 (monetization) content
Block Diagram	Updated Figure 5-1
Mechanical Characteristics	Updated package drawings in 196-Ball TFBGA

13.2. DS60001580C - 09/2021

Section	Changes
Chip Identifier	Updated table SAM9X60 SIP Chip ID Registers with additional chip ID value (0x819B35A2)

13.3. DS60001580B - 02/2020

Section	Changes
Reference Documents	Corrected hyperlink to SAM9X60 data sheet
DDR2 SDRAM Features	Added memory part numbers
SDR SDRAM Features	Added memory part number Updated Burst Length feature
Block Diagram	Updated Figure 5-1

13.4. DS60001580A - 10/2019

Changes
First issue.

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Product Page Links

SAM9X60D5M, SAM9X60D1G, SAM9X60D6K

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