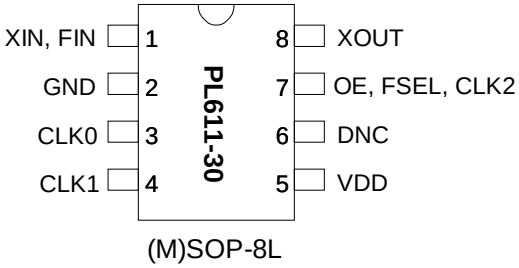
# PL611-30

## Programmable Clock

### FEATURES

- Advanced programmable PLL design
- Very low Jitter and Phase Noise (< 40ps Pk-Pk typ.)
- Supports complementary LVCMOS outputs to drive LVPECL and LVDS inputs.
- Output Frequencies:
  - ≤ 400MHz at 3.3V
  - ≤ 350MHz at 2.5V
- Input Frequencies:
  - Fundamental Crystal: 10MHz - 30MHz
  - 3RD overtone Crystal: Up to 75MHz
  - Reference Input: Up to 200MHz
- Accepts <1.0V reference signal input voltage
- One programmable I/O pin can be configured as Output Enable (OE) input, Frequency Selection (FSEL) input or Reference Clock (CLK2) output.
- Single 2.5V or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 8-pin MSOP/SOP Green/RoHS compliant packages.

### PIN CONFIGURATION

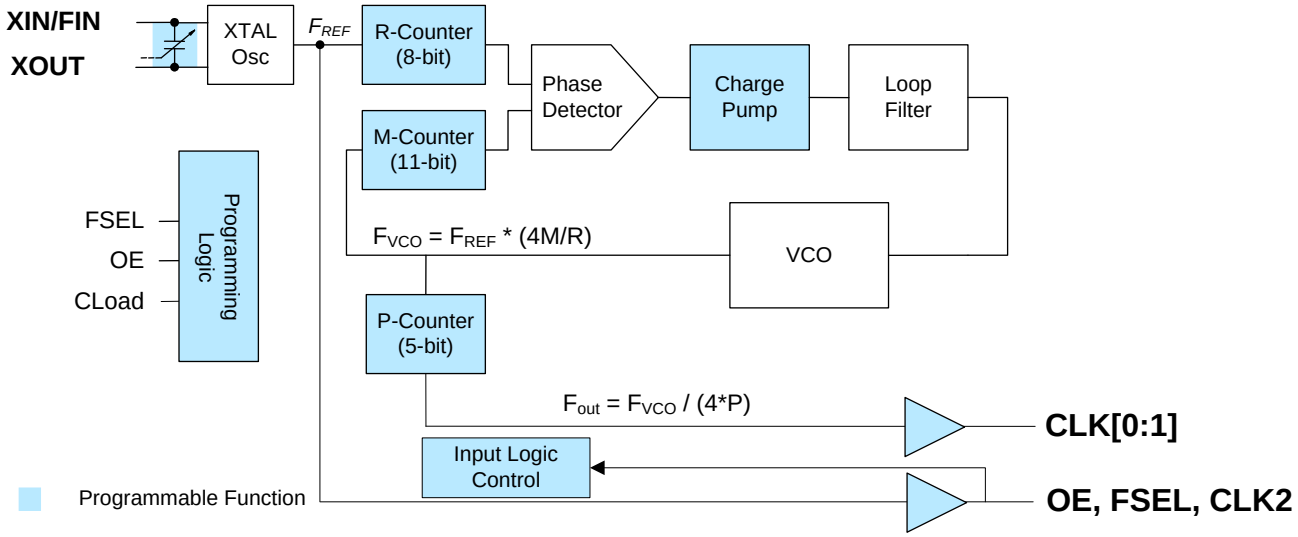



(M)SOP-8L

### DESCRIPTION

The PL611-30 is a low-cost general purpose frequency synthesizer and a member of Programmable Clock family. PL611-30 product family can generate any output frequency up to 400MHz from fundamental crystal input between 10MHz - 30MHz, a 3rd overtone crystal of up to 75MHz (3.3V Only) or a Reference Clock from 1MHz to 200MHz. The PL611-30 produces complementary LVCMOS outputs to support LVPECL, LVDS, and LVCMOS inputs.

### BLOCK DIAGRAM



## KEY PROGRAMMING PARAMETERS

| CLK[0:2] Output Frequency | Output Drive Strength | Crystal Load | Programmable Input/Output (pin #7) | # of Register Banks | Charge-Pump Current |
|---|---|---|---|---|---|
| $F_{OUT} = F_{IN} * M / (R * P)$<br>where M= 11 bit<br>R= 8 bit<br>P= 5 bit<br>1. CLK[0:1]= $F_{VCO} / (4 * P)$ or $F_{VCO}/2$<br>2. CLK[2]= $F_{REF}$ | Std: 10mA (default)<br><br>High: 24mA | ± 200ppm tuning. | One output pin can be configured as<br>1. CLK2 - output<br>2. FSEL - input<br>3. OE - input | 2 | 8 levels of charge-pump current setting |

## PIN DESCRIPTION

| Name | Pin # (M)SOP-8L | Type | Description |
|---|---|---|---|
| XIN, FIN | 1 | I | Crystal or Reference input pin |
| GND | 2 | P | GND connection |
| CLK[0:1] | 3,4 | O | Programmable Clock Output [note:CLK0=~CLK1] |
| VDD | 5 | P | VDD connection |
| DNC | 6 | - | Do No Connect |
| OE, FSEL, CLK2 | 7 | B | This programmable I/O pin can be configured as Output Enable (OE) input, Frequency Select (FSEL) input or CLK2 ($F_{REF}$) output. This pin has an internal 60KΩ pull up resistor when used as OE or FSEL. |
| XOUT | 8 | O | Crystal output pin. Do Not Connect when using $F_{IN}$ |

| State | OE | FSEL |
|---|---|---|
| 0 | Tristate CLK[0:1] | Select Bank '0' |
| 1 (default) | Normal mode | Select Bank '1' |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | -0.5 | 4.6 | V |
| Input Voltage Range | $V_I$ | -0.5 | $V_{DD}$+0.5 | V |
| Output Voltage Range | $V_O$ | -0.5 | $V_{DD}$+0.5 | V |
| Data Retention @ 85° C | | 10 | | Years |
| Soldering Temperature | | | 240 | °C |
| Storage Temperature | $T_S$ | -65 | 150 | °C |
| Ambient Operating Temperature* | | -40 | +85 | °C |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

## AC SPECIFICATIONS

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Crystal Input Frequency | Fundamental Crystal | 10 | | 30 | MHz |
| | 3rd Overtone Crystal (3.3V Operation Only) | | | 75 | |
| Input ($F_{IN}$) Frequency | | | | 200 | MHz |
| Input ($F_{IN}$) Signal Amplitude | Internally AC coupled | 0.9 | | $V_{DD}$ | Vpp |
| Output Frequency | At 3.3V $V_{DD}$, 15pF Load | 3 | | 400 | MHz |
| | At 2.5V $V_{DD}$, 15pF Load | 3 | | 350 | |
| OE Enable Time | OE Function; Ta=25° C, 15pF Load. Add one clock period to this measurement for a usable clock output. | | | 10 | ns |
| Settling Time | At power-up ($V_{DD} \geq$ 2.25V) | | | 10 | ms |
| VDD Sensitivity | Frequency vs. $V_{DD}$+/-10% | -2 | | 2 | ppm |
| Output Rise Time | 15pF Load, 10/90%$V_{DD}$, Standard Drive | | 2.5 | 3.5 | ns |
| | 15pF Load, 10/90%$V_{DD}$, High Drive | | 1.0 | 1.5 | |
| Output Fall Time | 15pF Load, 90/10%$V_{DD}$, Standard Drive | | 2.5 | 3.5 | ns |
| | 15pF Load, 90/10%$V_{DD}$, High Drive | | 1.0 | 1.5 | |
| Duty Cycle | At $V_{DD}$/2 | 45 | 50 | 55 | % |
| Max. output skew between same frequency clocks | Equal loading (15pF). Equal frequency & drive strength | | | 500 | ps |
| Period Jitter, peak-to-peak* (10,000 samples measured) | With capacitive decoupling between $V_{DD}$ and GND. Operating only CLK[0:1] outputs. | | 40 | | ps |

* Note: Jitter performance depends on the programming parameters.

## DC SPECIFICATIONS

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Supply Current, Dynamic, with Loaded Outputs | $I_{DD}$ | At 10MHz, load=15pF | | | 15 | mA |
| Operating Voltage | $V_{DD}$ | | 2.25 | | 3.63 | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = +4mA (Standard Drive) | | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4mA (Standard Drive) | $V_{DD}$-0.4 | | | V |
| Output Current | $I_{OSD}$ | $V_{OL}$ = 0.4V, $V_{OH}$ = 2.4V (Standard Drive) | 10 | | | mA |
| | $I_{OHD}$ | $V_{OL}$ = 0.4V, $V_{OH}$ = 2.4V (High Drive) | 24 | | | mA |

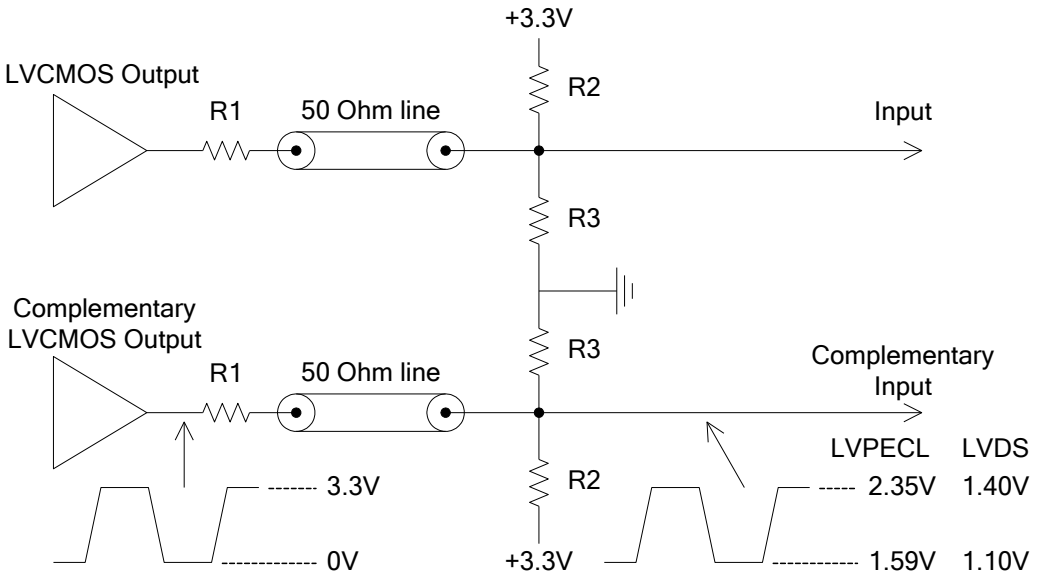
## CRYSTAL SPECIFICATIONS

| PARAMETERS | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Fundamental Crystal Resonator Frequency | $F_{XIN}$ | 10 | | 30 | MHz |
| 3rd Overtone Crystal Resonator Frequency (3.3V Only) | $F_{XIN}$ | | | 75 | MHz |
| Crystal Loading Rating<br>(The IC can be programmed for any value in this range.) | $C_{L\ (xtal)}$ | 5 | | 20 | pF |
| Maximum Sustainable Drive Level | | | | 500 | µW |
| Operating Drive Level | | | 100 | | µW |
| Crystal Shunt Capacitance | C0 | | | 6 | pF |
| Effective Series Resistance, Fundamental, 10MHz - 30MHz | ESR | | | 30 | Ω |
| Effective Series Resistance, 3rd Overtone, 30MHz - 50MHz [CO< 4pF, $C_L$=5pF/8pF] | ESR | | | 100/70 | Ω |
| Effective Series Resistance, 3rd Overtone, 50MHz - 65MHz, [CO< 4pF, $C_L$=5pF/8pF] | ESR | | | 60/40 | Ω |
| Effective Series Resistance, 3rd Overtone, 65MHz - 75MHz [CO< 4pF, $C_L$=5pF/8pF] | ESR | | | 45/30 | Ω |

## TERMINATING COMPLEMENTARY LVCMOS OUTPUTS

Figure 1 below describes how to terminate the complementary LVCMOS outputs of PL611-30 Programmable Clock for use with LVPECL or LVDS inputs.

The unique feature of complementary LVCMOS outputs allows great flexibility for board designers. By standardizing on one termination scheme you can use the PL611-30 for all your LVDS and LVPECL clock requirements up to 400MHz.




| Component selection | |
|---|---|
| For LVPECL input | For LVDS input |
| R1 = 130 Ohm<br>R2 = 82 Ohm<br>R3 = 130 Ohm | R1 = 360 Ohm<br>R2 = 130 Ohm<br>R3 = 82 Ohm |

Notes:
Place R1 as close to the LVCMOS outputs as possible.

Place R2 and R3 as close to the LVPECL/LVDS inputs as possible.

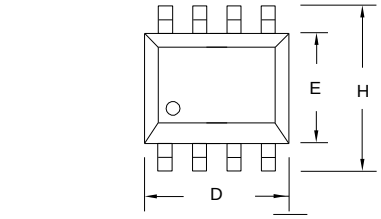
Figure 1

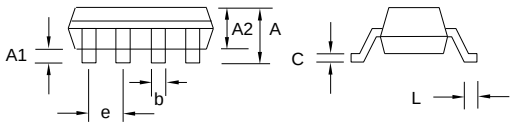
The above layout allows the PL611-30 to drive either LVPECL or LVDS inputs by simply changing the value of R1.

## PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

### MSOP-8L

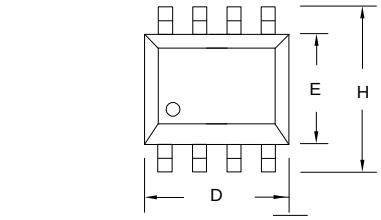
| Symbol | Dimension in MM | |
|---|---|---|
| | Min. | Max. |
| A | --- | 1.10 |
| A1 | 0.05 | 0.15 |
| A2 | 0.81 | 0.91 |
| B | 0.25 | 0.40 |
| C | 0.13 | 0.23 |
| D | 2.90 | 3.10 |
| E | 2.90 | 3.10 |
| H | 4.90 BSC | |
| L | 0.445 | 0.648 |
| e | 0.65 BSC | |

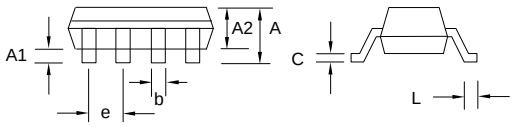



### SOP-8L

| Symbol | Dimension in MM | |
|---|---|---|
| | Min. | Max. |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.25 | 1.50 |
| B | 0.33 | 0.53 |
| C | 0.19 | 0.27 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| H | 5.80 | 6.20 |
| L | 0.40 | 0.89 |
| e | 1.27 BSC | |

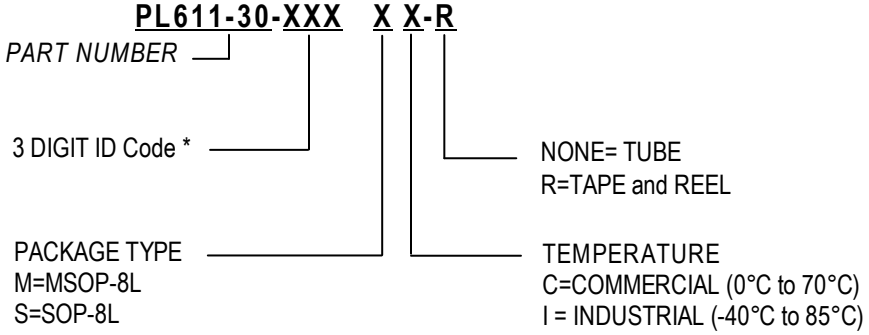


## ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

***For part ordering, please contact our Sales Department:***
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

***PART NUMBER***
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range




* Micrel will assign a unique 3-digit ID code for each approved programmed part number.

| Part / Order Number | Marking | Part / Order Number | Marking | Package Option |
|---|---|---|---|---|
| PL611-30-XXXMC | C3XXX LLL | PL611-30-XXXMI | C3XXX LLLI | 8-Pin MSOP (Tube) |
| PL611-30-XXXMC-R | | PL611-30-XXXMI-R | | 8-Pin MSOP (Tape and Reel) |
| PL611-30-XXXSC | P611-30 XXX LLLLL | PL611-30-XXXSI | P611-30 XXXI LLLLL | 8-Pin SOP (Tube) |
| PL611-30-XXXSC-R | | PL611-30-XXXSI-R | | 8-Pin SOP (Tape and Reel) |

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