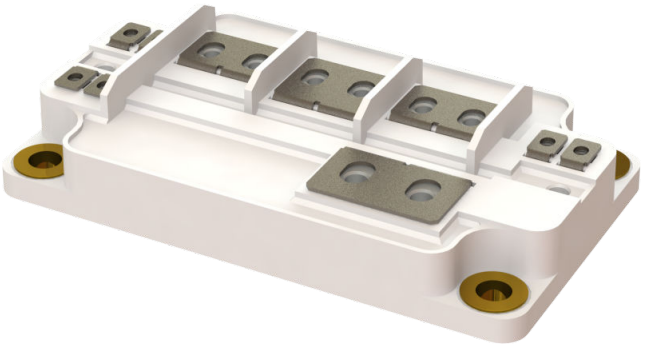
Evaluation Board for SP6LI mSiC™ MOSFET Module and Gate Driver

MSCDR-SP6LIEVB-001

Introduction

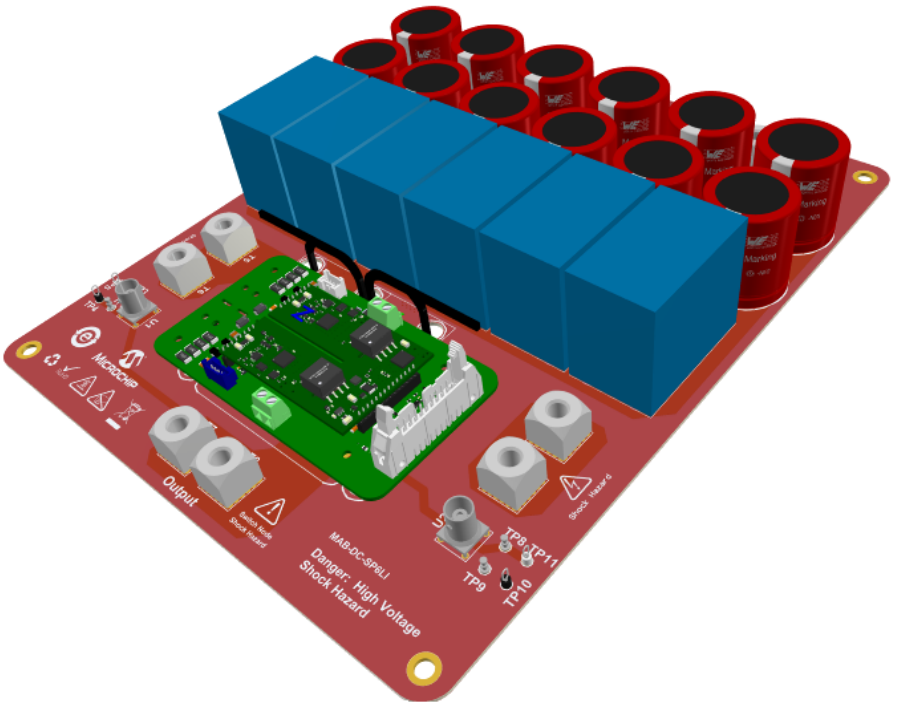
This user guide provides details on an evaluation board for Microchip mSiC MOSFET modules in the SP6LI package and mSiC gate drivers. For example, MSCSM120AM02CT6LING.

Figure 1. Microchip SP6LI SiC Power Module



The SP6LI evaluation board is designed to be a one-stop development platform for SP6LI low inductance SiC module testing with top mount digital gate driver solution.

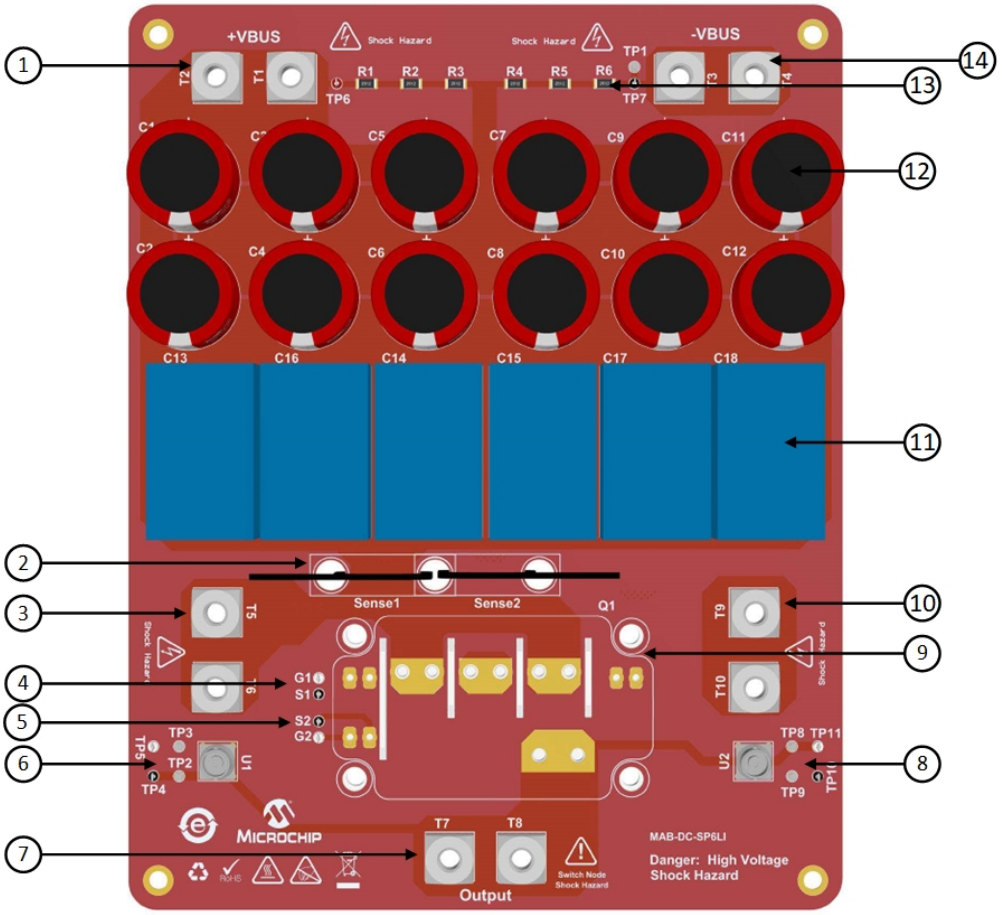
Figure 2. SP6LI Evaluation Board and Digital Gate Driver—3D Model



Features

The following figures show the key hardware features and components of the evaluation board.

Figure 3. SP6LI Evaluation Board—Top View



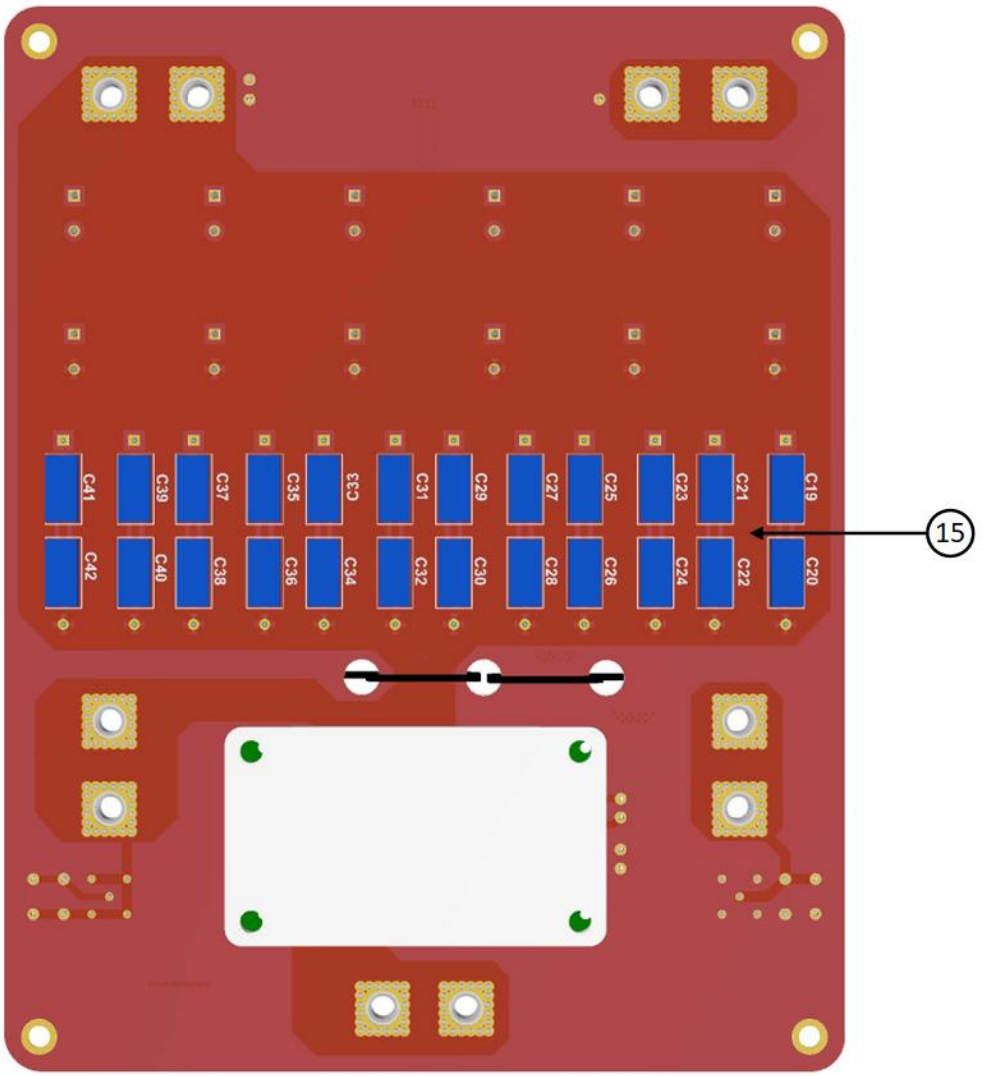
The following table lists the key features and hardware components available on the top of the evaluation board.

Table 1. Hardware Features and Components of the Evaluation Board—Top View

Number	Key Hardware Features and Components
1	Terminal block connector for providing +VBUS voltage up to 900 V_{DC} with respect to −VBUS
2	Rogowski coil provision for current measurement at the drain and source sides
3	Terminal block connector for connecting the inductor (load) while doing double-pulse testing for the low-side switch. This terminal is also connected to +VBUS.
4	Test point for sensing the high-side gate signal (V_{GS})
5	Test point for sensing the low-side gate signal (V_{GS})
6	Test point for measuring the V_{DS} voltage across high-side switch
7	Terminal block connector for output of module (connected device) as well as for connecting the inductor (load) while doing double-pulse testing
8	Test point for measuring the V_{DS} voltage across low-side switch
9	Placement of the SP6LI SiC module from the bottom side
10	Terminal block for connecting the inductor (load) while doing double-pulse testing for low-side switch. This terminal is also connected to −VBUS.

.....continued	
Number	**Key Hardware Features and Components**
11	Film capacitors of 132 µF
12	Bulk capacitor of 2 mF eqivalent in total
13	Bleeder resistor for capacitor discharge
14	Terminal block for connecting –VBUS

Figure 4. SP6LI Evaluation Board—Bottom View



The following table lists the key features and hardware components available on the bottom of the evaluation board.

Table 2. Hardware Features and Components of the Evaluation Board—Bottom View

Number	Key Hardware Features and Components
15	High frequency capacitors of equivalent 0.6 µF

Table of Contents

1. Evaluation Board

This section describes the evaluation board pinout, schematics, circuit, and Printed Circuit Board (PCB) layout.

1.1 Pinout

The following tables list the pinout and electrical parameter details for the terminal block and connectors, respectively.

Table 1-1. Pinout and Electrical Parameters for Terminal Block

Designator	Function/Description	Remark
T1, T2	+VBUS	T2 Unmounted
T3, T4	–VBUS	T4 Unmounted
T5, T6	+VBUS	T6 Unmounted
T7, T8	OUTPUT	T8 Unmounted
T9, T10	–VBUS	T10 Unmounted

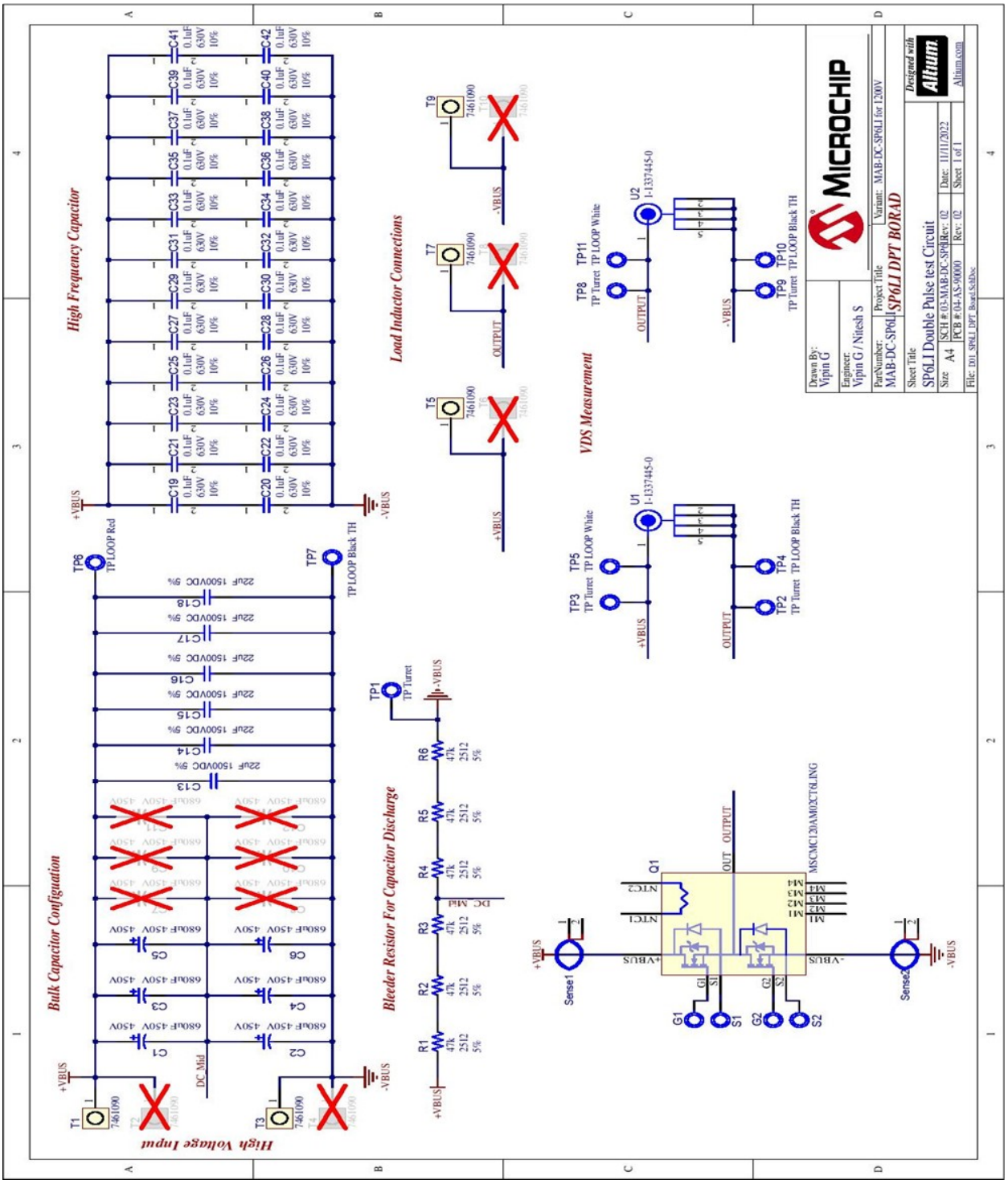
Table 1-2. Pinout and Electrical Parameters for Connectors

Designator	Pin Number	Function/Description	Remark
U1	1	+VBUS	When measuring with these connectors, use a oscilloscope with isolated channels.
	2, 3, 4, 5	OUTPUT	
U2	1	OUTPUT	
	2, 3, 4, 5	–VBUS	

1.2 Evaluation Board Schematic

The following figure shows the schematic for the SP6LI evaluation board.

Figure 1-1. SP6LI Evaluation Board Schematic



1.3 Evaluation Board PCB Layout

The SP6LI evaluation board is a four-layer FR4, 2 mm, and Plated-Through-Hole (PTH) PCB construction. The following figures show the PCB layers.

Figure 1-2. SP6LI Evaluation Board Top Overlay (Silk-Screen) Layer

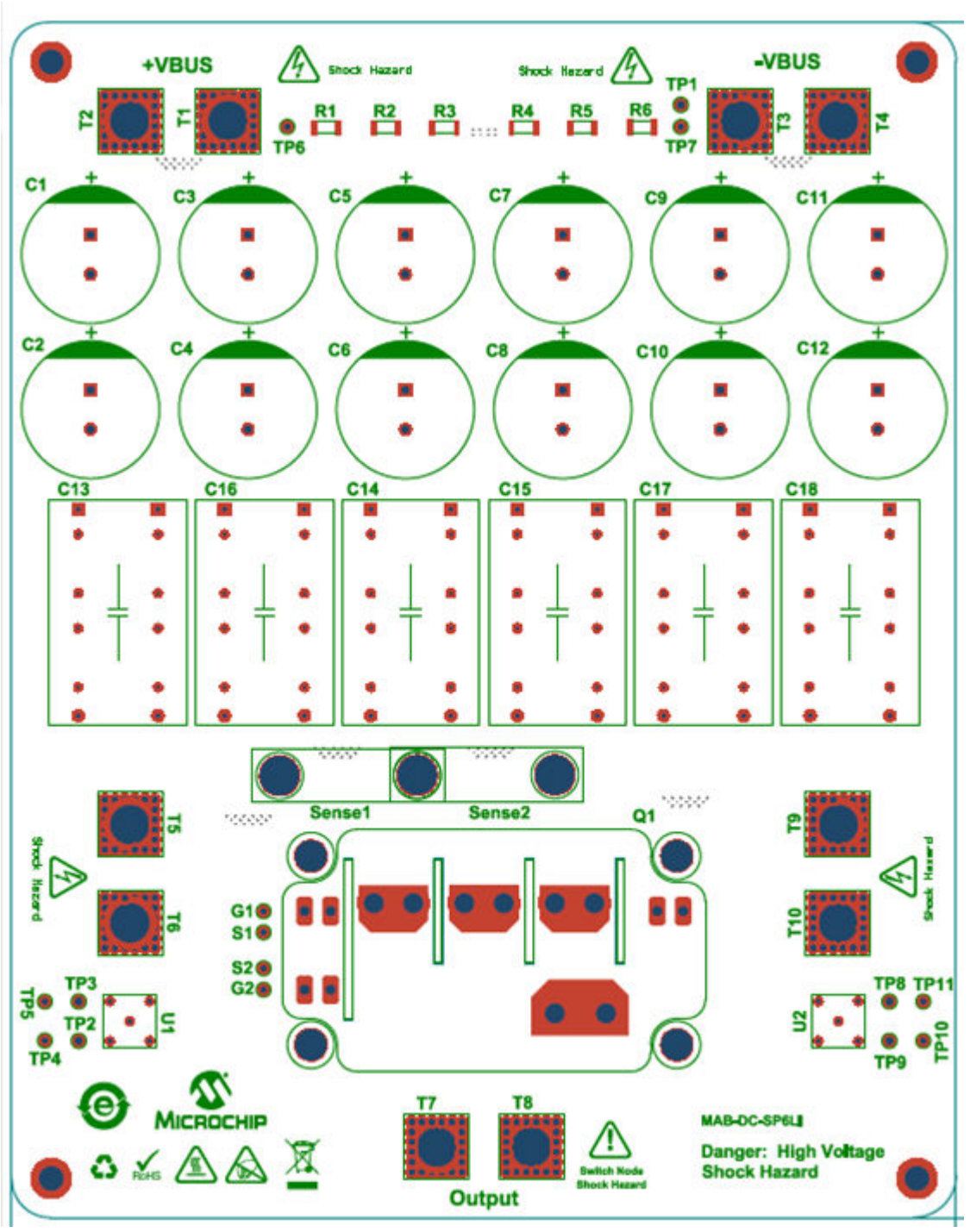


Figure 1-3. SP6LI Evaluation Board Top Layer

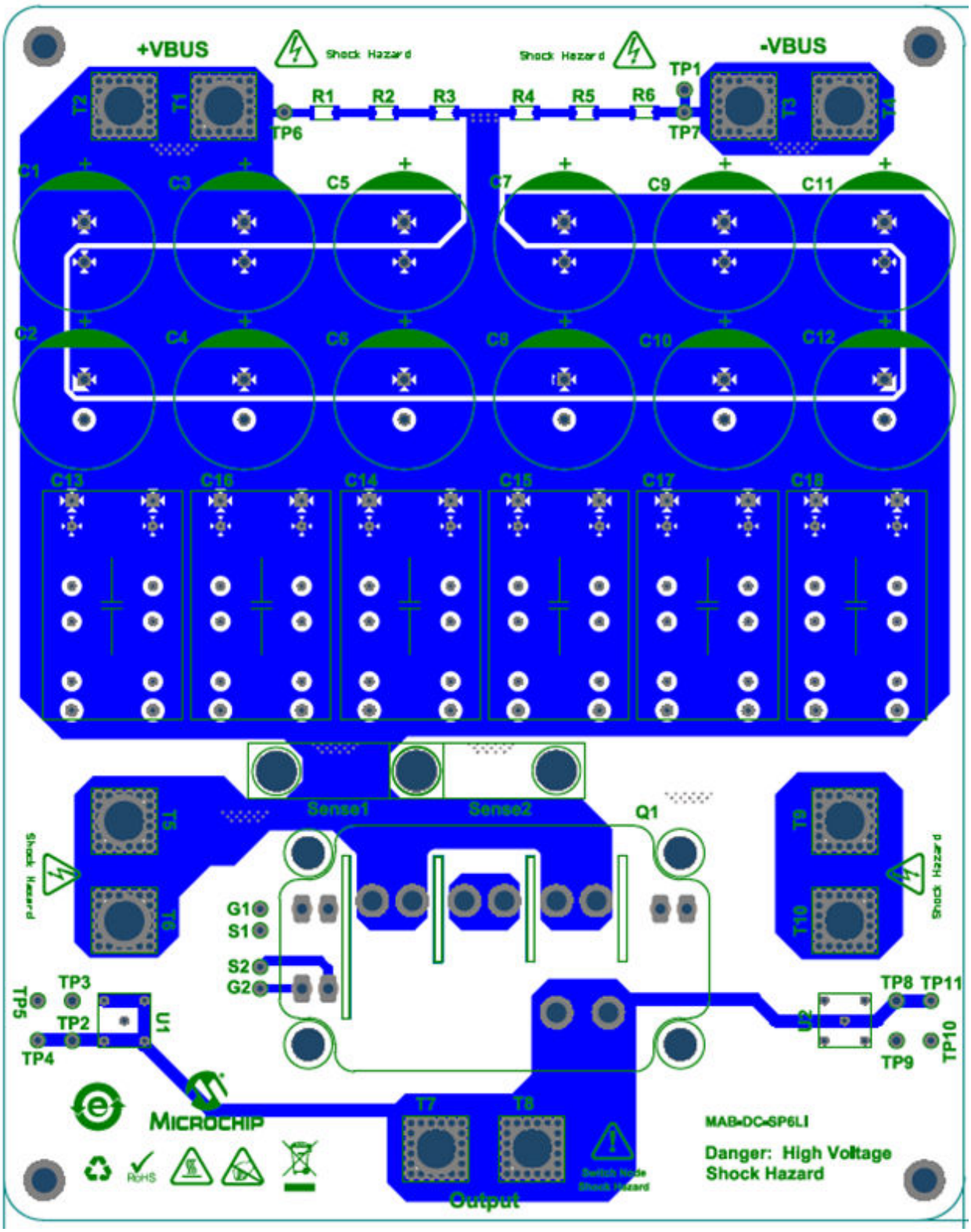


Figure 1-4. SP6LI Evaluation Board Inner Layer 1

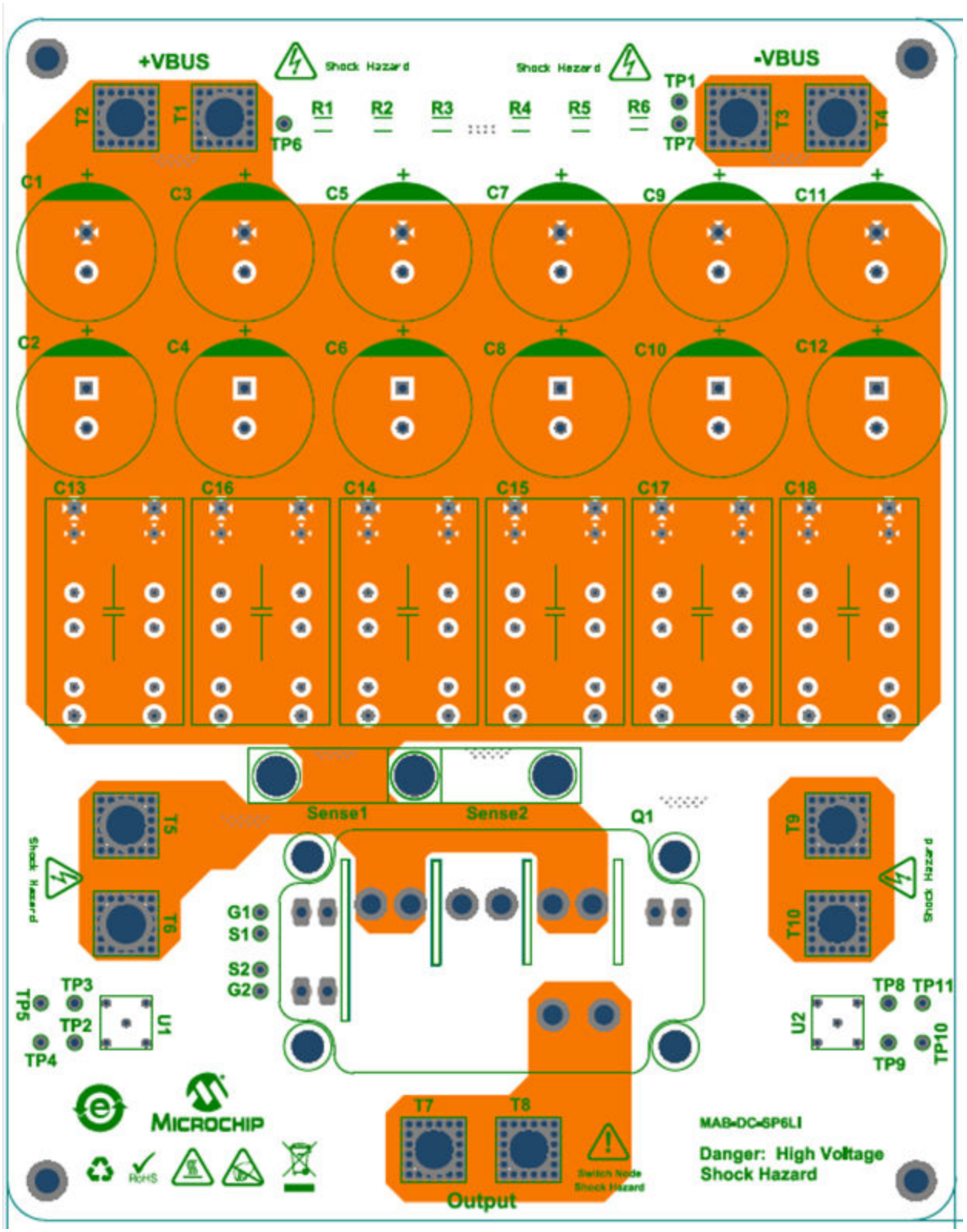


Figure 1-5. SP6LI Evaluation Board Inner Layer 2

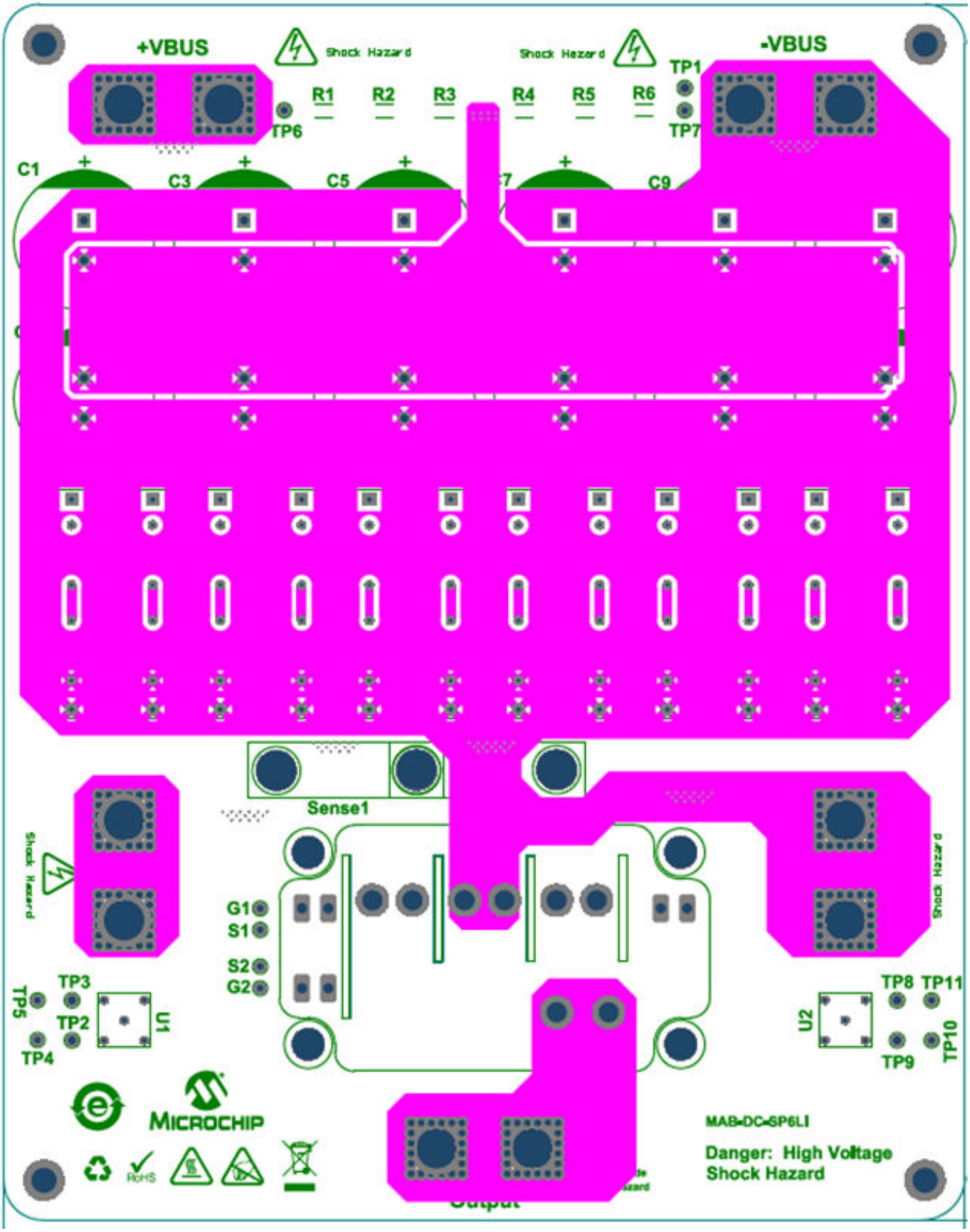


Figure 1-6. SP6LI Evaluation Board Bottom Layer

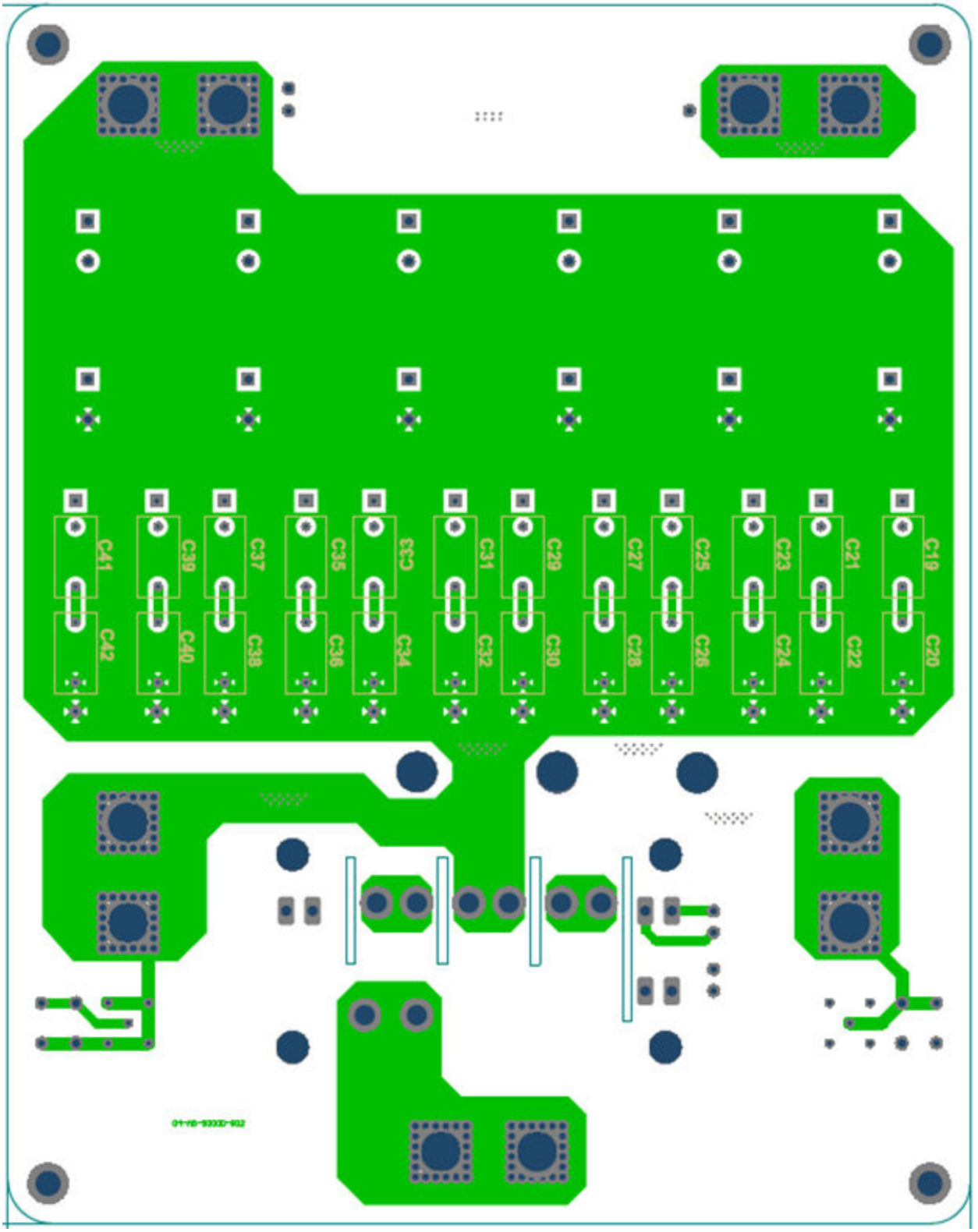
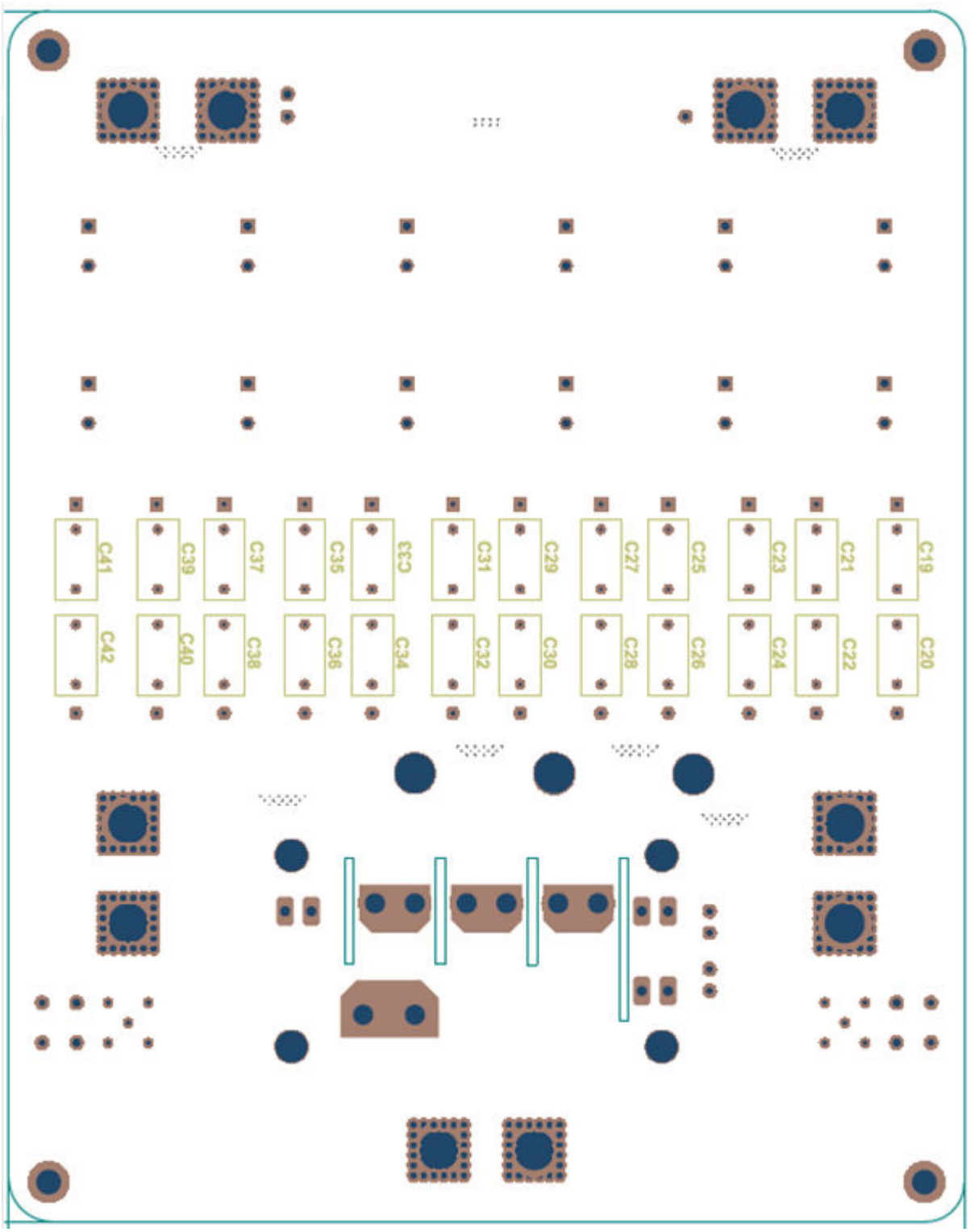


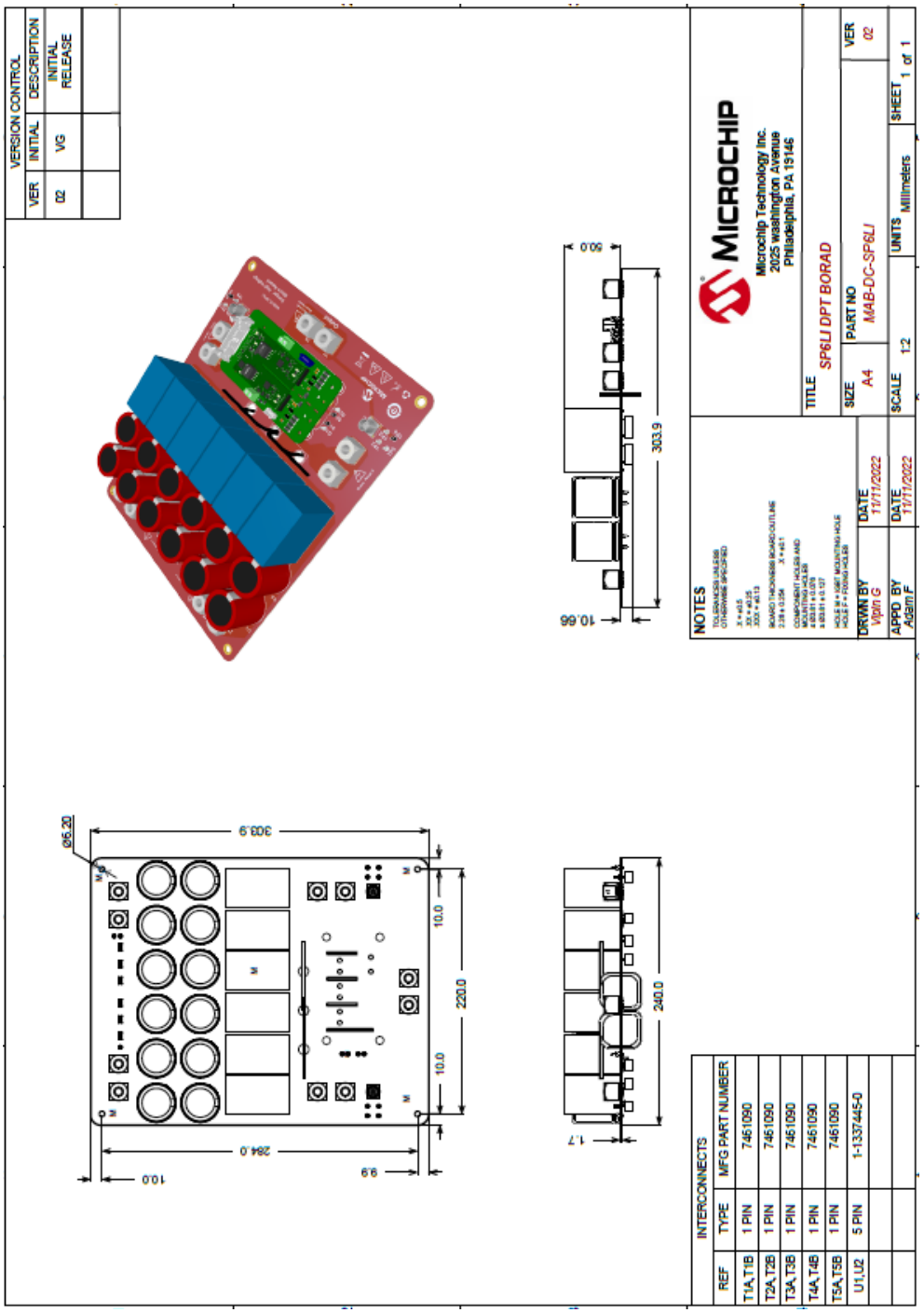
Figure 1-7. SP6LI Evaluation Board Bottom Overlay (Silk-Screen) Layer



1.4 Evaluation Board Mechanical Drawing

The following figure shows the mechanical drawing for the SP6LI evaluation board with placement and mounting of SP6CA1 (core adaptor board) with 2ASC-12A2HP (1200V dual-channel HP augmented core—ASD2).

Figure 1-8. SP6LI Evaluation Board Mechanical Drawing



2. Bill of Materials

The following table lists the bill of materials for the SP6LI evaluation board.

Table 2-1. SP6LI Evaluation Board BOM

Qty	Designator	Description	Manufacturer	Manufacturer Part Number
6	C1, C2, C3, C4, C5, C6	CAP ALUM 680 µF 450V 20% RAD SNAP P10D35H57	TDK Electronics Inc.	B43644A5687M000
6	C13, C14, C15, C16, C17, C18	CAP FILM 22 µF 1500V 5% RAD P52.5L57.5W35H50	KEMET	C4AQSBW5220A3NJ
24	C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42	CAP FILM 0.1 µF 630V 10% B32672L	EPCOS/TDK	B32672L6104K000
4	G1, G2, TP5, TP11	CON TP LOOP White TH	Keystone	5012
1	Q1	SIC PHASE LEG MOSFET MODULE MSCMC120AM02CT6LING SP6	Microsemi	MSCMC120AM02CT6LING
6	R1, R2, R3, R4, R5, R6	RES TKF 47 kΩ 5% 1W SMD 2512	Panasonic Electronic Components	ERJ-1TYJ473U
5	S1, S2, TP4, TP7, TP10	CON TP LOOP Black TH	Keystone	5011
2	Sense1, Sense2	Rogowski coil provision	—	—
5	T1, T3, T5, T7, T9	CON TERMINAL Female REDCUBE M8 20 pin Press Fit Brass TH Vert	Wurth Elektronik	7461090
5	TP1, TP2, TP3, TP8, TP9	CON TP PIN Tin TH	Harwin	H2121-01
1	TP6	CON TP LOOP Red TH	Keystone	5010
2	U1, U2	CON BNC JACK Female 5 pin 50 Ohm TH PCB mount	TE Connectivity AMP Connectors	1-1337445-0
1	PCB	4 Layer Board	Microchip	04-AS-90000-R2

3. Hardware Validation

This section contains test conditions, equipment required for testing, test schematics, and test setup for the SP6LI evaluation board.

3.1 Test Conditions

The following table lists the test conditions for validating the SP6LI evaluation board.

Table 3-1. Test Condition

Parameters	Values
Device under test	MSCSM120AM03CT6LIAG (SP6LI 1200V, 3.1 mΩ)
Grate driver used (core)	Microchip digital gate driver 2ASC-12A2HP
Core adaptor used	SP6CA1
Device placed at	Half bridge high-side and low-side
DC bus voltage	600V
Load current	400A
Gate resistors R_{Gon}	1.1Ω
Gate resistors R_{Goff}	1.1Ω
Temperature	25 °C
Load for DPT test for T_{off}	Inductor of 350 µH
Load for DSAT test	Resistor of 1Ω
Snubber (RC or C)	None
C_{GS}	None
Scope filter	None

3.2 Equipment Required for Testing

The following equipments are required to test and characterize the SP6LI evaluation board:

- Low voltage variable DC power supply (0–30V/2A)
- DC unregulated high-voltage power supply (0–2500V/1.5A)
- Oscilloscope (LeCroy model HDO6104A)
- Rogowski current waveform transducer (1.0 mV/A) (for current measurement)
- GW Instek GOP-050 high-voltage differential probes (for high-voltage measurement)
- PICkit 3/PICkit 4 In-circuit debugger (for programming primary side controller)

Note: Equivalent equipment can be used.

3.3 Test Schematics

The following figures show test schematics for measuring the switching losses for high-side and low-side SiC MOSFET devices.

Figure 3-1. Schematic to Measure the Switching Losses for High-Side SiC MOSFET

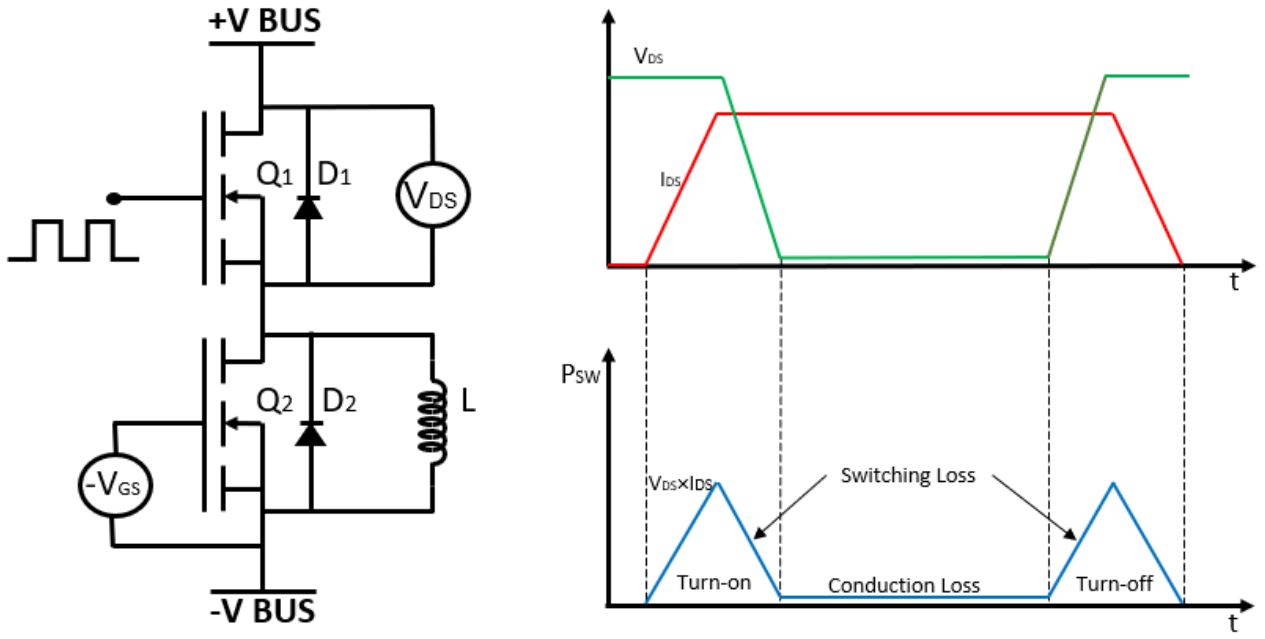
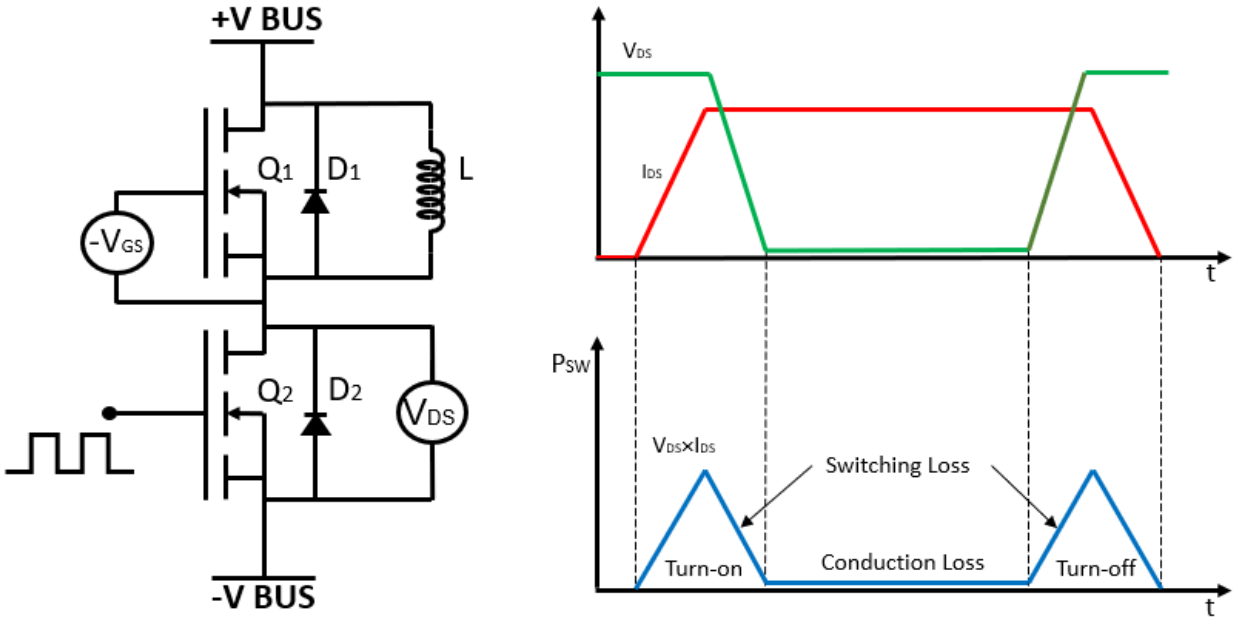


Figure 3-2. Schematic to Measure the Switching Losses for Low-Side SiC MOSFET



3.4 Test Setup

The following figures show the test setup for double-pulse testing and for DSAT testing.

Figure 3-3. Double-Pulse Test Setup for Testing High-Side Switch

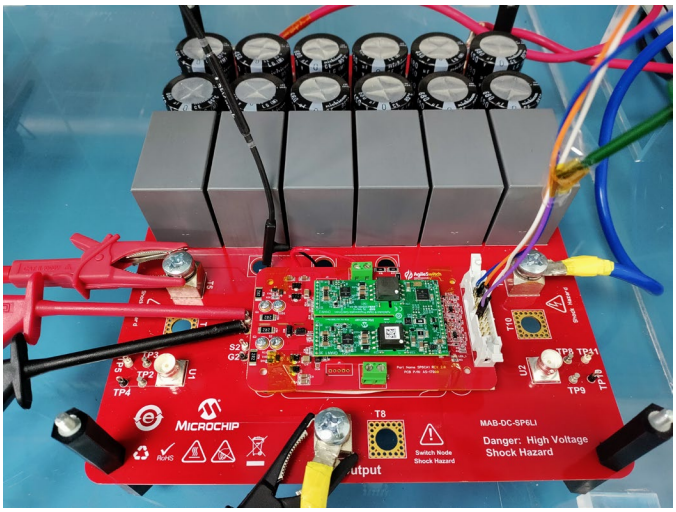


Figure 3-4. Double-Pulse Test Setup for Testing Low-Side Switch

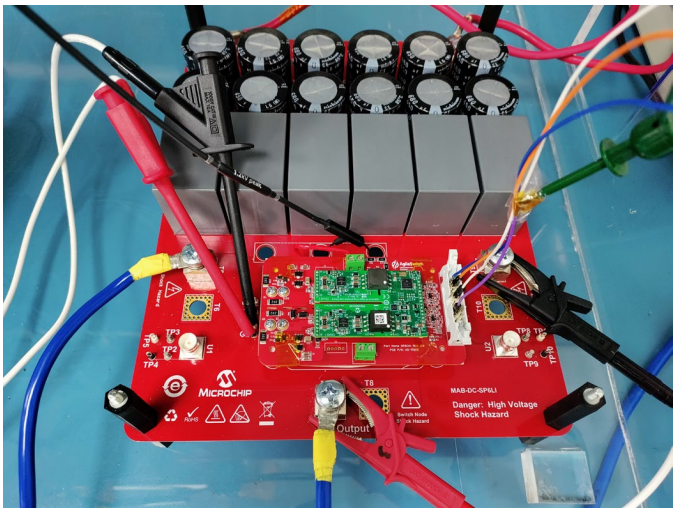


Figure 3-5. DSAT Test Setup for Testing High-Side Switch

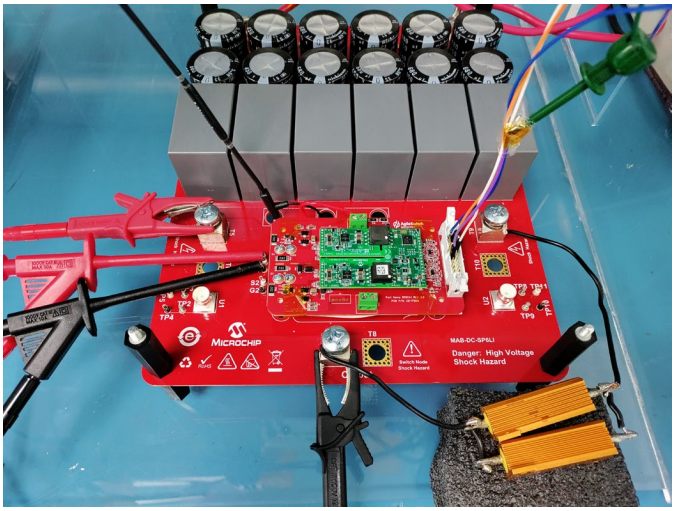
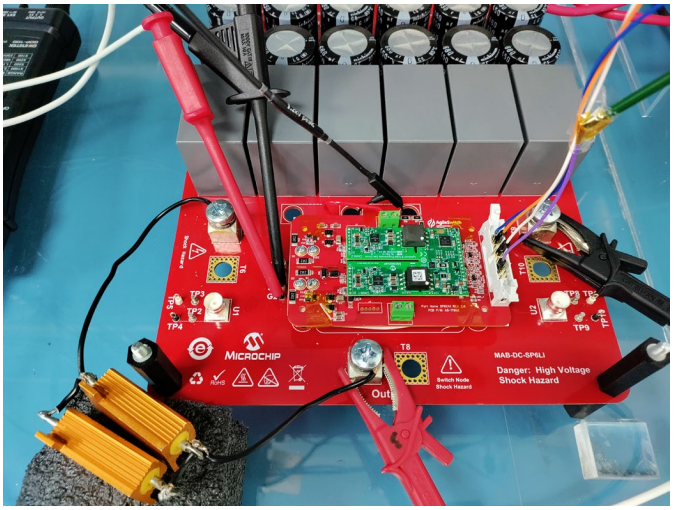


Figure 3-6. DSAT Test Setup for Testing Low-Side Switch



3.5 Test Results

This section shows the test results for turn-on measurement, turn-off measurement, and DSAT operation of high-side and low-side switch.

3.5.1 Turn-On Measurements

The following sections show the results for turn-on of high-side and low-side switch.

High-Side

The following figures show the test results for turn-on of high-side SiC MOSFET.

Figure 3-7. Characteristic Waveform during Turn-On Switching Transients for High-Side SiC MOSFET

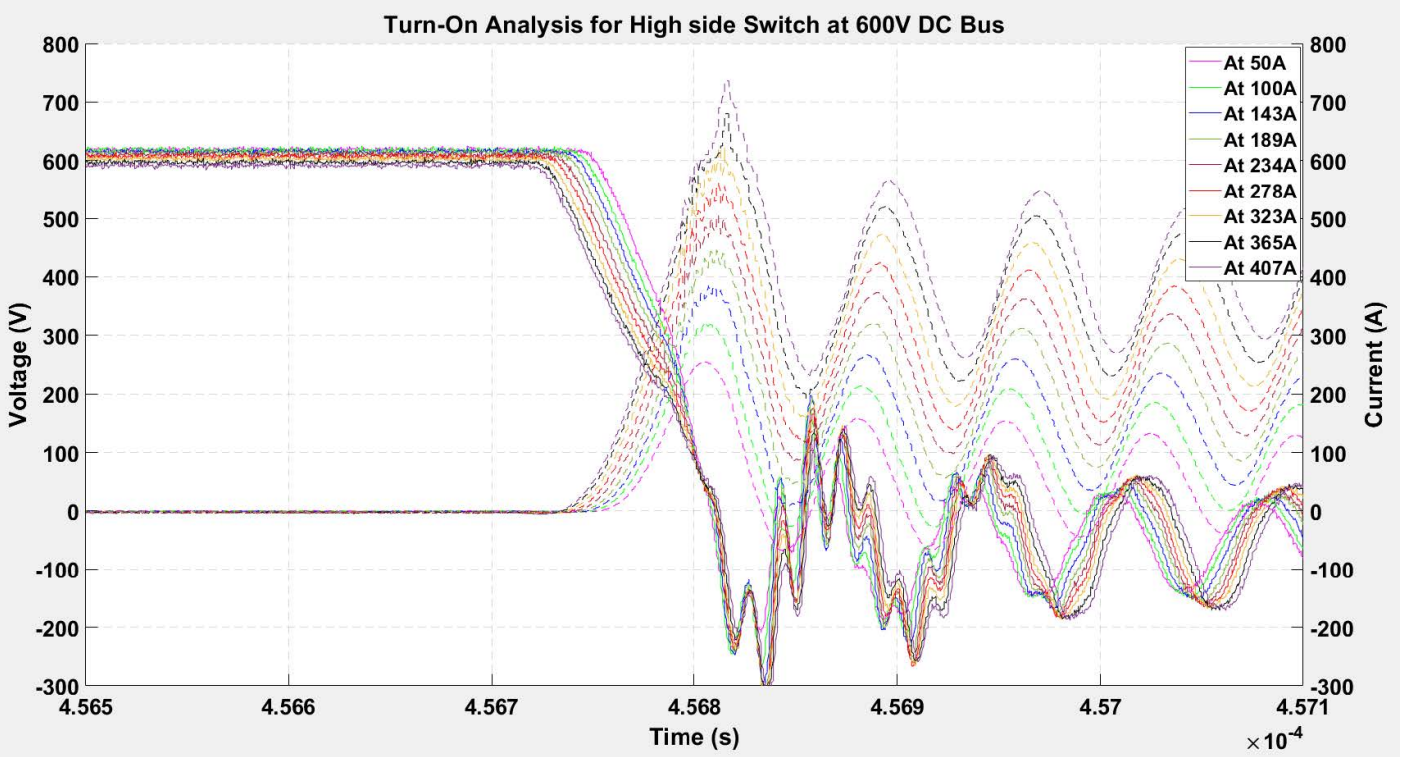
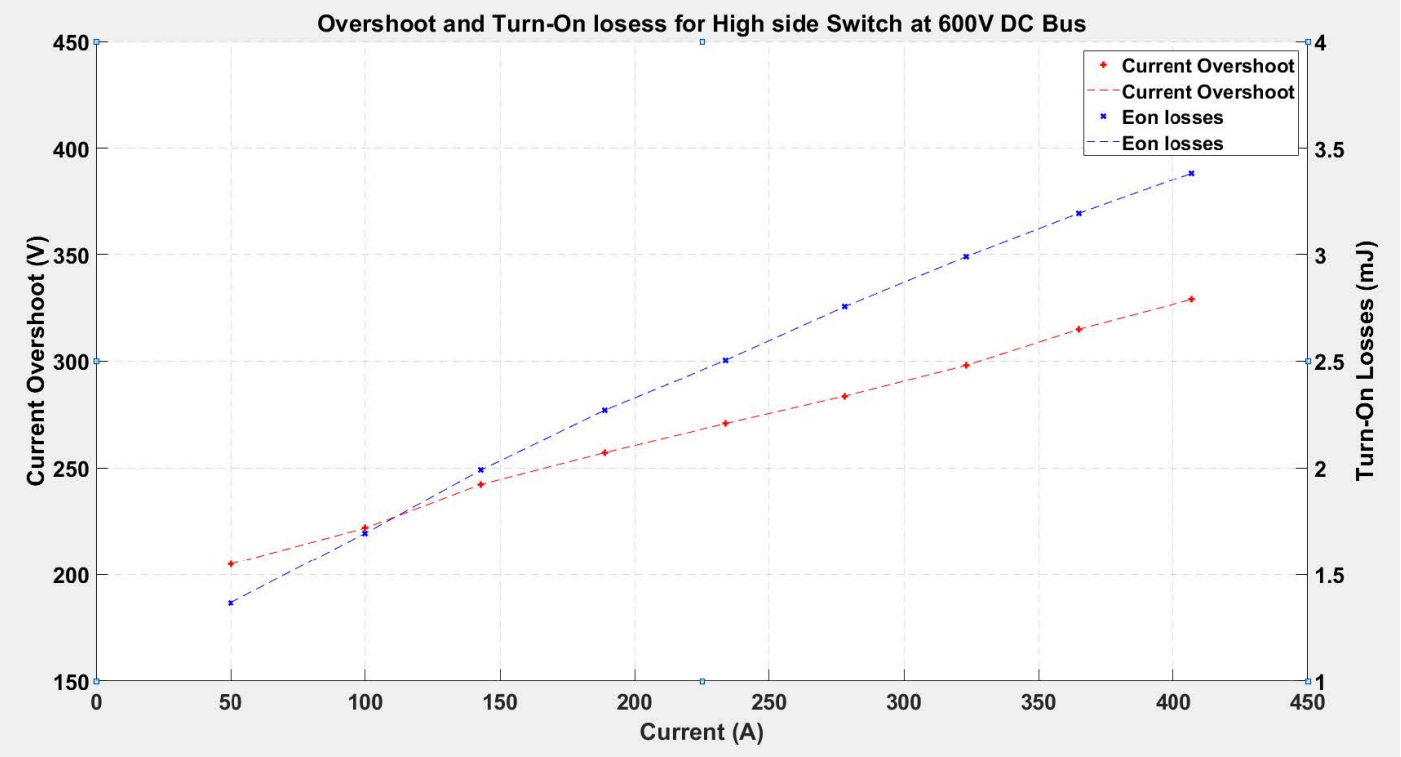


Figure 3-8. Current Overshoot vs Turn-On Losses at 600 V_{DC} Bus with Respect to Change in Current



Low-Side

The following figures show the test results for turn-on of low-side SiC MOSFET.

Figure 3-9. Characteristic Waveform during Turn-On Switching Transients for Low-Side SiC MOSFET

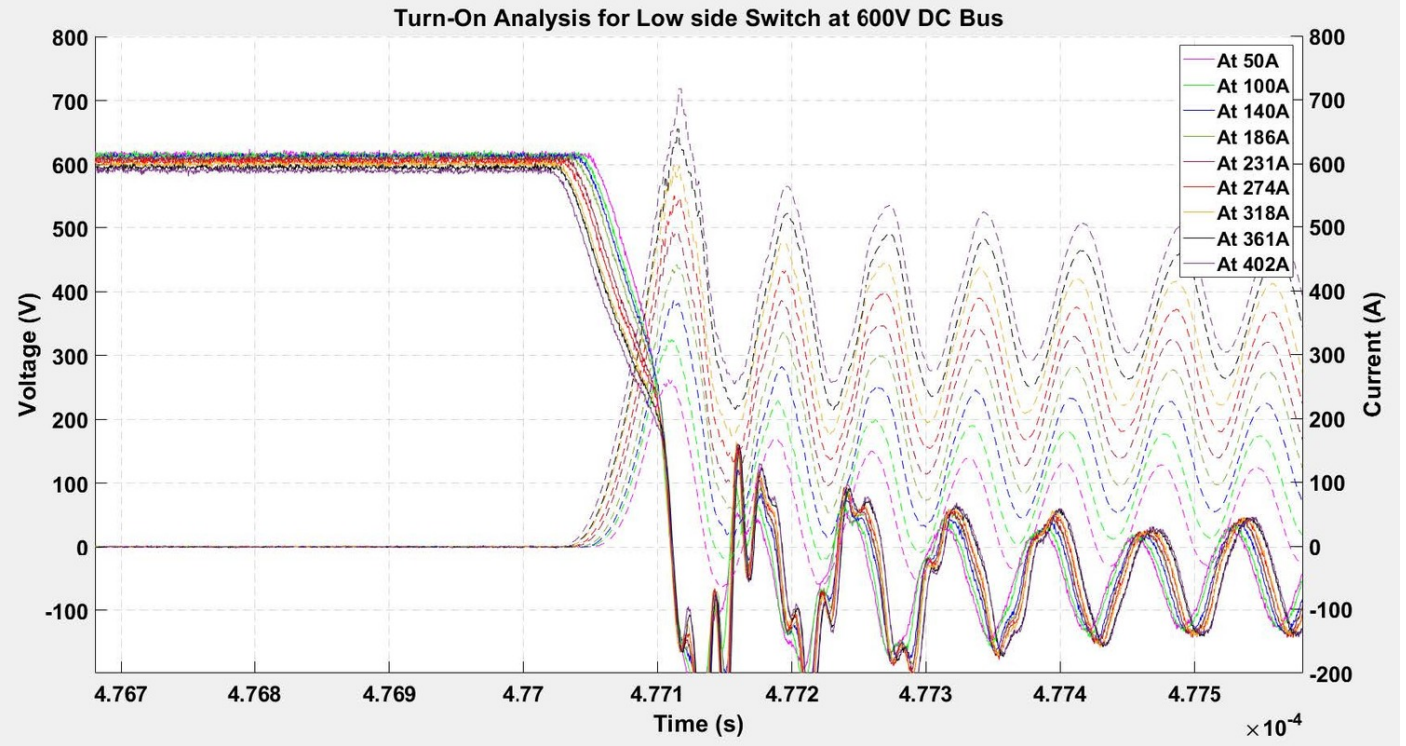
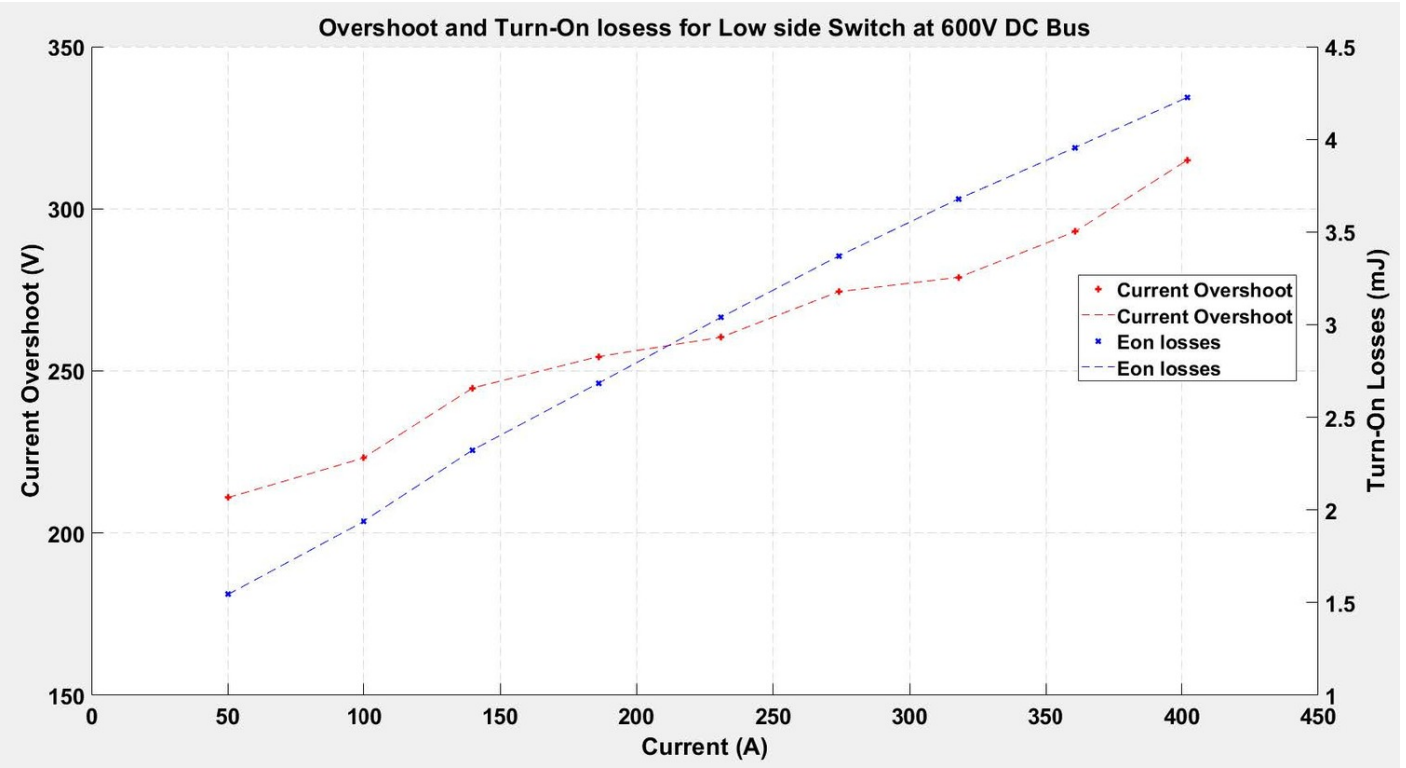


Figure 3-10. Current Overshoot vs Turn-On Losses at 600 V_{DC} Bus with Respect to Change in Current



3.5.2 Turn-Off Measurements

The following sections show the results for turn-off of high-side and low-side.

High-Side

The following figures show the test results for turn-off of high-side switch.

Figure 3-11. Characteristic Waveform during Turn-Off Switching Transients for High-Side SiC MOSFET

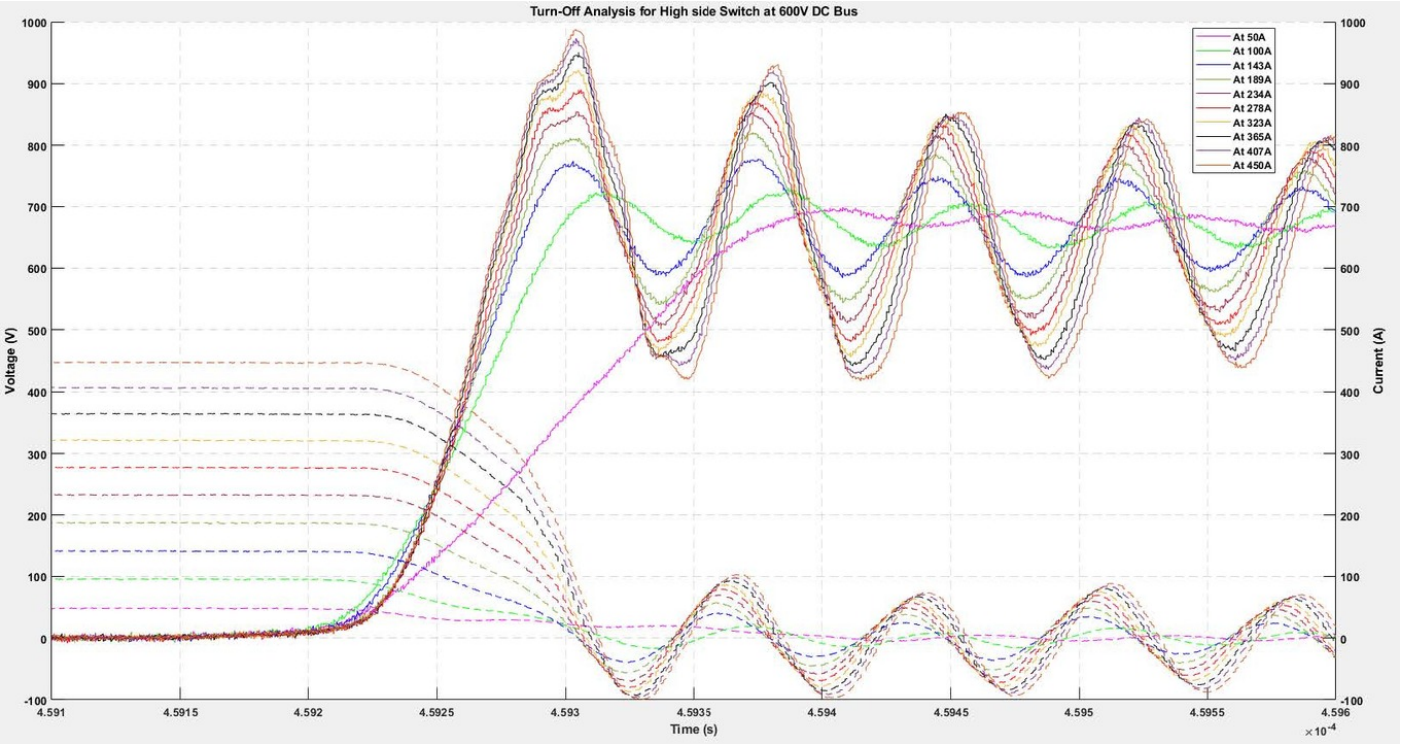
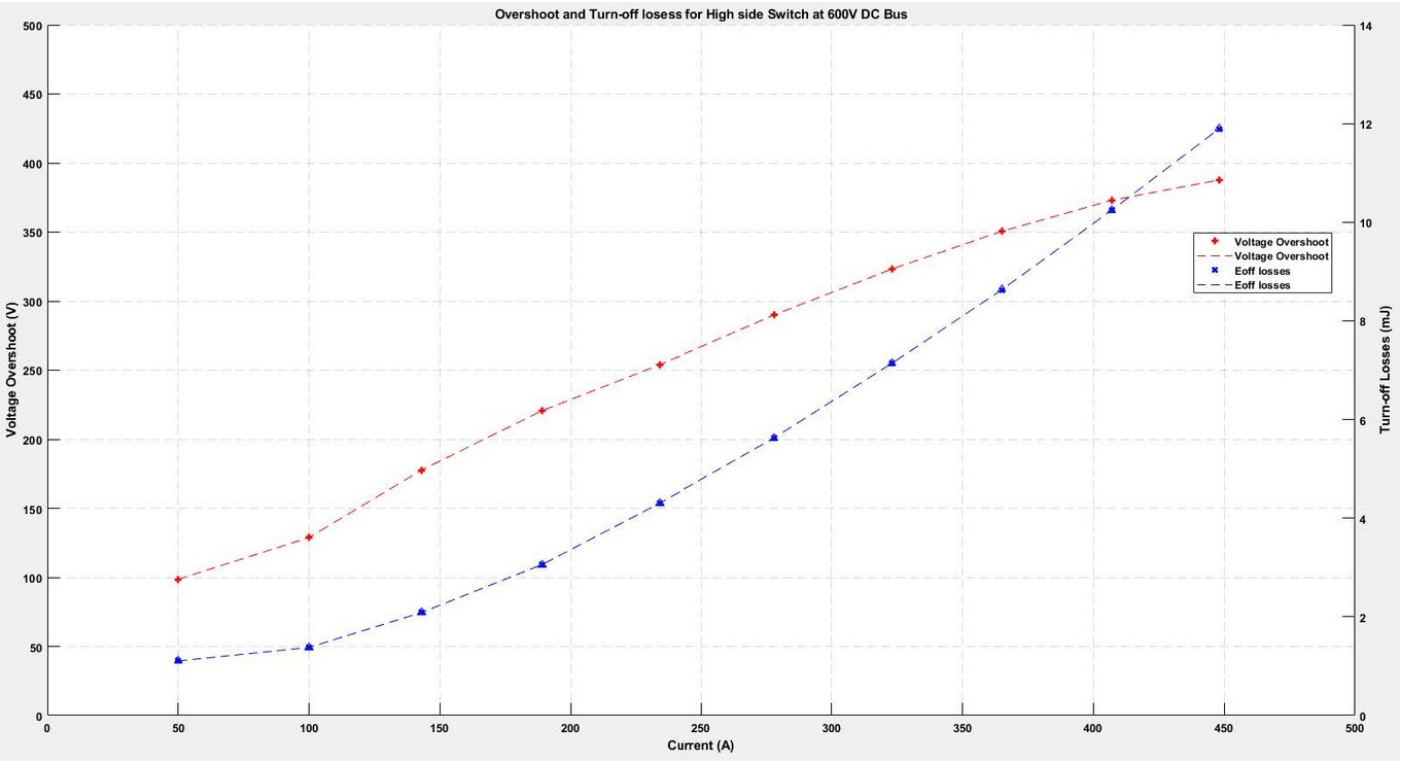


Figure 3-12. Voltage Overshoot vs Turn-On Losses at 600 V_{DC} Bus with Respect to Change in Current



Low-Side

The following figures show the test results for turn-off of low-side switch.

Figure 3-13. Characteristic Waveform during Turn-Off Switching Transients for Low-Side SiC MOSFET

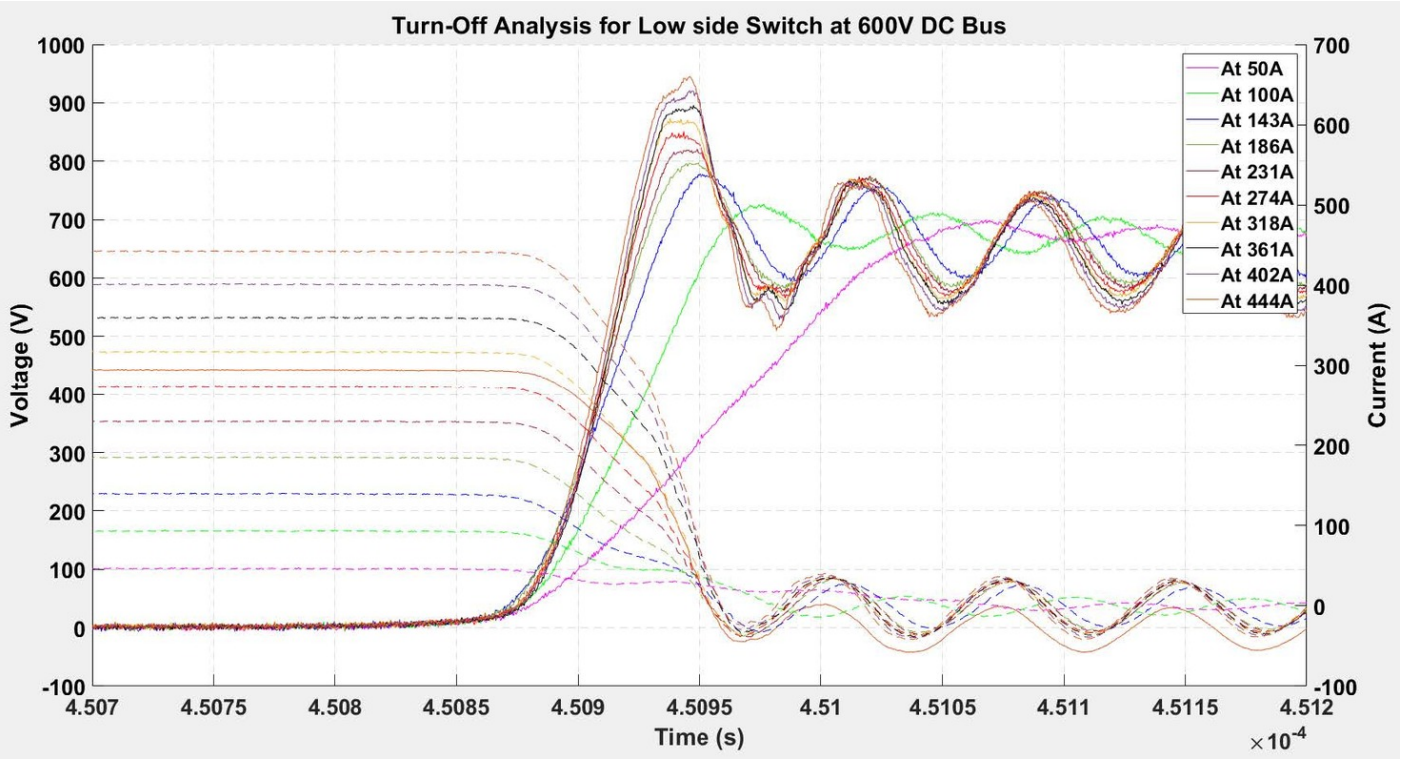
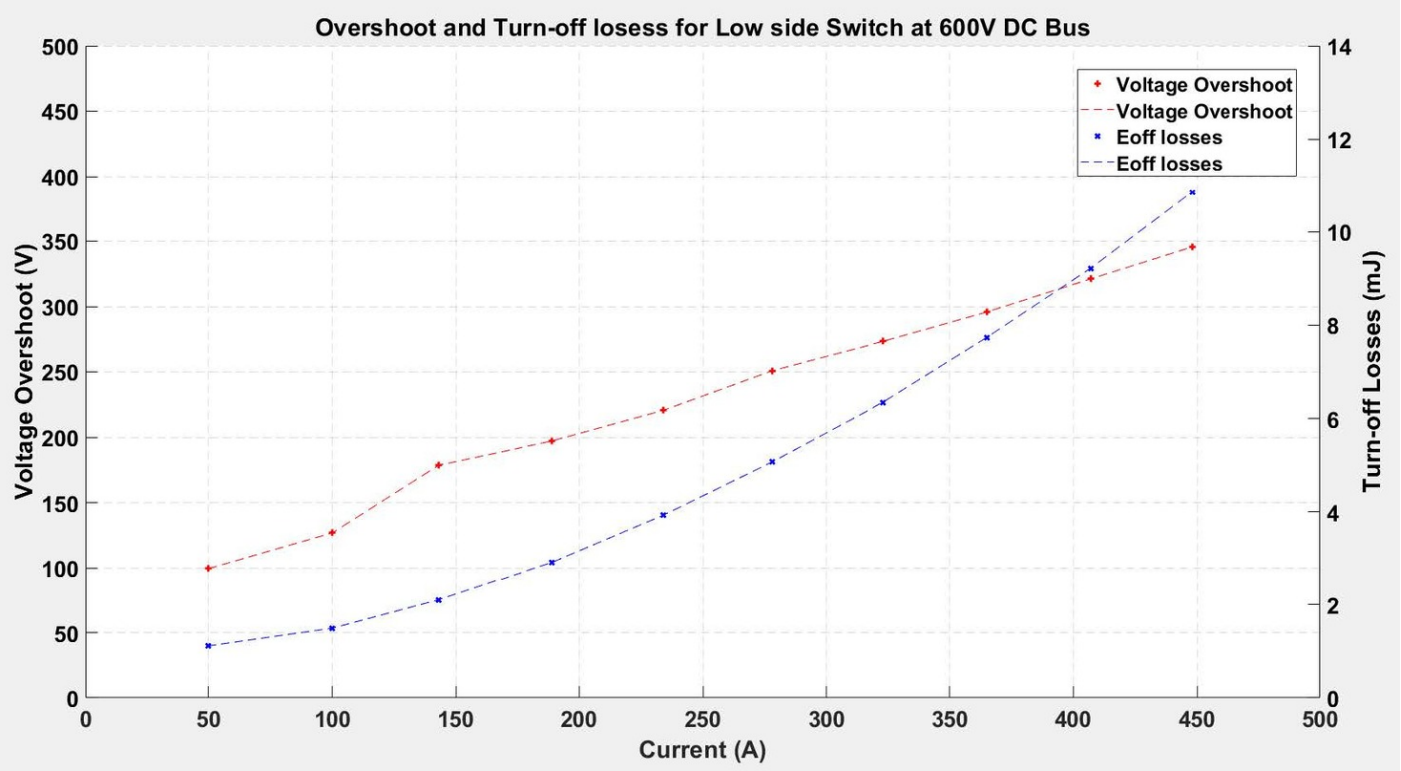


Figure 3-14. Voltage Overshoot vs Turn-On Losses at 600 V_{DC} Bus with Respect to Change in Current



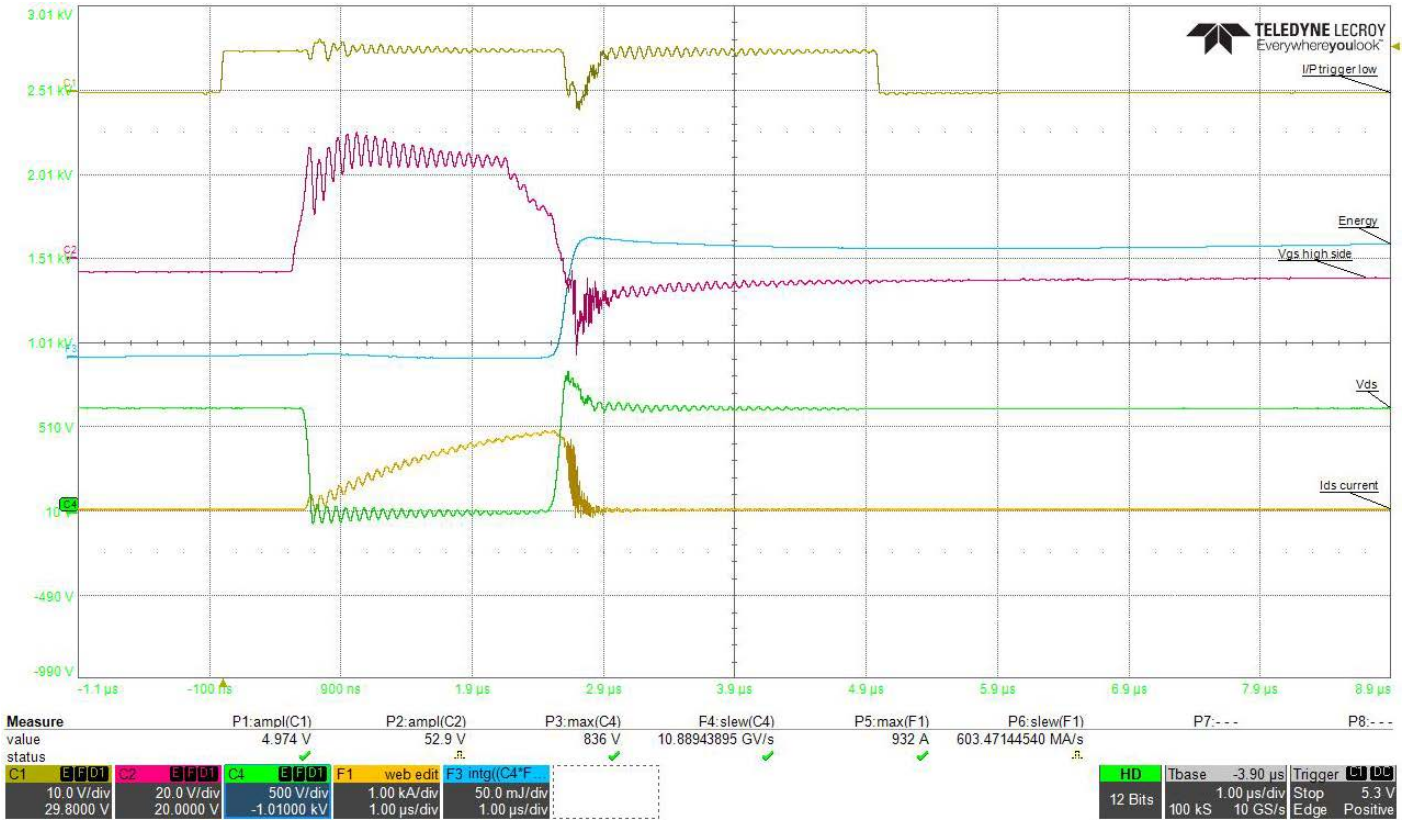
3.5.3 DSAT Operation

The following sections show the results for DSAT (over current protection) of high-side and low-side switch.

High-Side

The following figure shows the test result for DSAT of high-side switch overcurrent condition set at 900A.

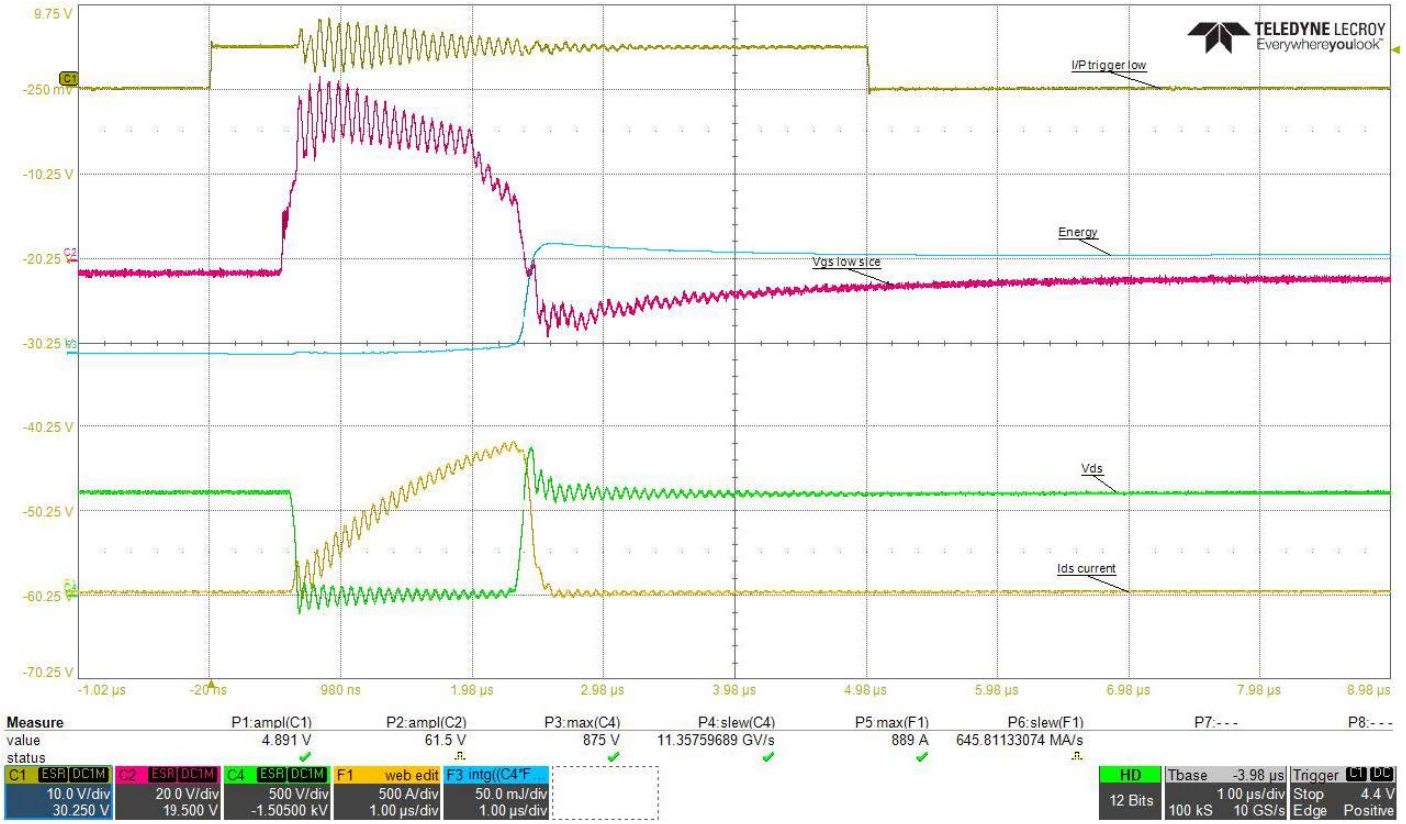
Figure 3-15. High-Side over Current DSAT Test Results at 600 V_{DC}



Low-Side

The following figure shows the test result for DSAT of low-side switch overcurrent condition set at 900A.

Figure 3-16. Low-Side over Current DSAT Test Results at 600 V_{DC}



4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	08/2024	Updated Worldwide Sales and Service.
A	12/2023	Initial revision

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