MCP6576/6R/6U/7/9

1.8V, 40 ns Low Power Open-Drain Output Comparator

Features

- Propagation Delay at V_{DD} = 5.5V:
  40 ns (typical) High-to-Low
- Low Quiescent Current:
  70 µA (Maximum per Comparator)
- Low Input Offset Voltage: ±7 mV (Maximum)
- Supply Voltage Range: 1.8V to 5.5V
- Rail-to-Rail Input
- Power-on Reset (POR)
- Extended Temperature Range: -40°C to +125°C
- AEC-Q100 Qualified
- Packaging:
  - MCP6576/6U: 5-Lead SC70 and SOT-23
  - MCP6576R: 5-Lead SOT-23
  - MCP6577: 8-Lead SOIC and MSOP
  - MCP6579: 14-Lead SOIC and TSSOP

Applications

- Automotive
- Portable Equipment
- Medical Diagnostic Equipment
- RC Timers
- Sensor Conditioning

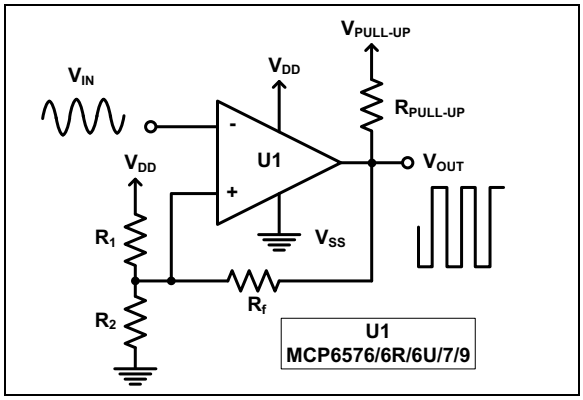
Design Aids

- SPICE Macro Models
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Devices

- Push-Pull Output: MCP6571/1R/1U/2/4

Typical Application



General Description

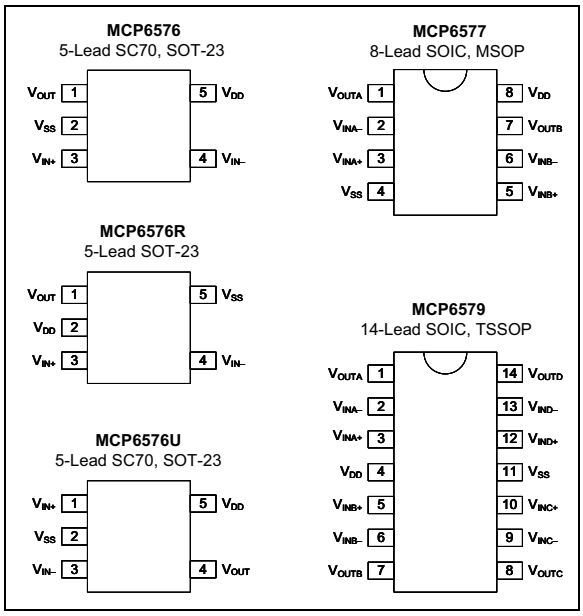
MCP6576/6R/6U/7/9 from Microchip Technology is a family of CMOS/TTL compatible comparators that operate with a single supply voltage, as low as 1.8V, while drawing low quiescent current (70 µA, maximum per amplifier). These comparators incorporate a POR feature that keeps the output high impedance until V_{DD} rises to a sufficient voltage to control the comparator. MCP6576/6R/6U/7/9 also has a low input offset voltage (±7 mV, maximum).

The MCP6576/6R/6U/7/9 comparators are optimized for low power, single supply applications with greater than rail-to-rail input operation. Internal input hysteresis eliminates output switching due to internal input noise voltage, resulting in reduced current draw. The devices are provided with open-drain outputs.

The family of comparators are offered in single (MCP6576/6R/6U), dual (MCP6577), and quad (MCP6579) packages.

All devices are designed using an advanced CMOS process and fully specified in the extended temperature range of -40°C to +125°C.

Package Type (Top View)



1.0 ELECTRICAL SPECIFICATIONS

1.1 Absolute Maximum Ratings

$V_{DD} - V_{SS}$ 6V
Current at Input Pins ($V_{IN}+$, $V_{IN}-$) . . . . . ±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$) (Note 1) . . . . . V_{SS} – 0.5V to V_{DD} + 0.5V
All Other Input and Outputs . . . . . V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage . . . . . $|V_{DD} - V_{SS}|$
Output Short-Circuit Current (Note 2) . . . . . Continuous
Storage Temperature (T_{STG}) . . . . . -65°C to +150°C
Maximum Junction Temperature (T_J) . . . . . +150°C
ESD Protection on All Pins (HBM, CDM) . . . . . ≥ 2 kV, 1.5 kV

Note 1: See **Section 4.2.2, "Input Voltage Limits"**.

2: Short-circuit to GND, one comparator per package.

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, $V_{IN}-$ = $V_{DD}/2$, $V_{IN}+$ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ and $V_{PULL-UP}$ = V_{DD}.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Power-on-Reset Voltage (Note 1)	V_{POR}	—	—	1.6	V	
Quiescent Current per Comparator	I_Q	—	35	—	µA	I_O = 0A, V_{OUT} = High
		30	45	70	µA	I_O = 0A, V_{OUT} = Low
Power Supply Rejection Ratio	PSRR	60	80	—	dB	V_{CM} = $V_{DD}/2$
Input Voltage						
Input Offset Voltage (Note 2)	V_{OS}	-7	—	7	mV	V_{CM} = $V_{DD}/2$
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±1	—	µV/°C	T_A = -40°C to +125°C
Input Hysteresis Voltage (Note 2)	V_{HYST}	1	—	6	mV	V_{CM} = $V_{DD}/2$
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
		—	20	—	pA	T_A = +85°C
		—	50	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||4	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	

Note 1: The output is high impedance until V_{DD} exceeds V_{POR}.

2: V_{OS} is the center of the input-referred trip points. Hysteresis is the difference between the trip points.

3: Guaranteed by characterization.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ and $V_{PULL-UP}$ = V_{DD}.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.2	—	V_{DD} + 0.2	V	T_A = -40°C to +125°C, Note 3
Common Mode Rejection Ratio	CMRR	54	75	—	dB	V_{DD} = 5.5V, V_{CM} = V_{CML} to V_{CMH}
Open-Drain Output						
Pull-up Voltage	$V_{PULL-UP}$	1.6	—	5.5	V	
Output Voltage Swing	V_{OL}	V_{SS} + 0.2	—	$V_{PULL-UP}$	mV	V_{DD} = 5.5V, I_{OUT} = 4 mA
	V_{OH}	V_{SS} + 0.3	—	$V_{PULL-UP}$	mV	V_{DD} = 1.8V, I_{OUT} = 4 mA
Output Short-Circuit Current	I_{SC}	—	±10	—	mA	V_{DD} = 1.8V
		—	±80	—	mA	V_{DD} = 5.5V
Startup Time	t_{START}	—	11	—	µs	V_{DD} = 0V to 5.5V

Note 1: The output is high impedance until V_{DD} exceeds V_{POR}.

2: V_{OS} is the center of the input-referred trip points. Hysteresis is the difference between the trip points.

3: Guaranteed by characterization.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Power Supply						
High-to-Low, 100 mV Overdrive	t_{PHL}	—	40	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Fall Time	t_F	—	5	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Maximum Toggle Frequency	f_{TG}	—	4	—	MHz	V_{DD} = 5.5V
		—	2	—	MHz	V_{DD} = 1.8V
Noise						
Input Noise Voltage	E_{ni}	—	400	—	μV_{P-P}	f = 10 Hz to 100 kHz

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = 1.8V to 5.5V and V_{SS} = GND.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	Note 1
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5-Lead SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	221	—	°C/W	
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8-Lead SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 14-Lead SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum temperature of +150°C.

1.3 Test Circuit Configuration

The test circuit configuration in Figure 1-1 is used to determine the AC and DC electrical specifications.

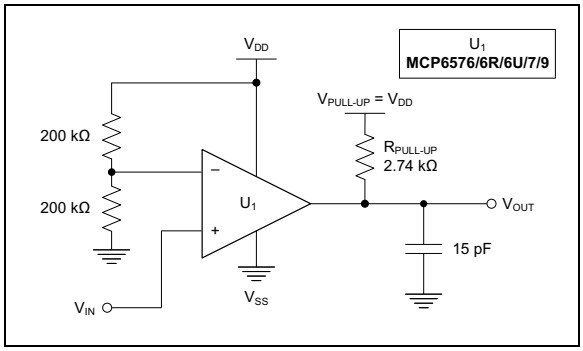


FIGURE 1-1: *AC and DC Test Circuit for the Open-Drain Output Comparators.*

1.4 Propagation Measurement

The diagram in Figure 1-2 is used to determine the propagation delay measurement.

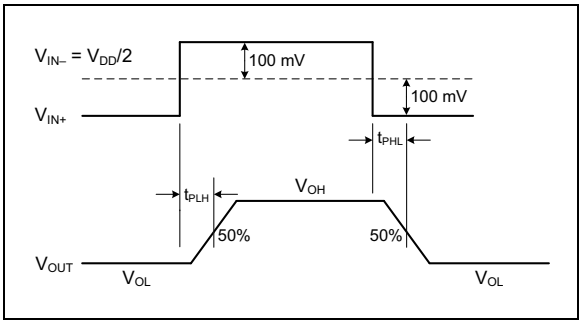


FIGURE 1-2: *Propagation Delay Timing Diagram.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

2.1 DC Inputs

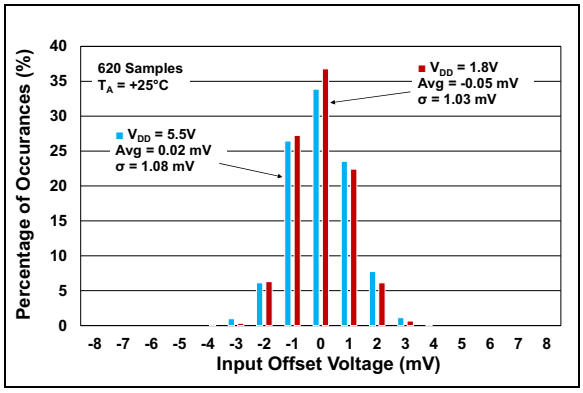


FIGURE 2-1: *Input Offset Voltage Histogram. T_A = +25°C.*

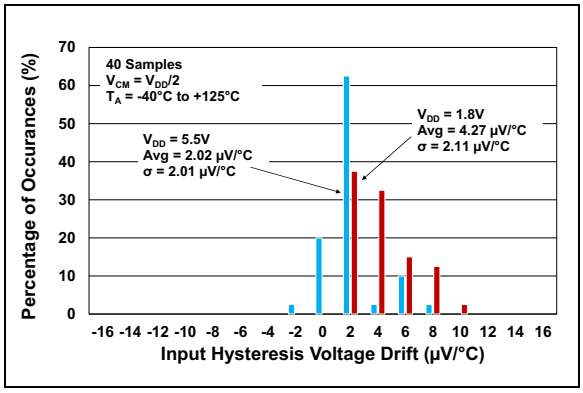


FIGURE 2-4: *Input Hysteresis Voltage Drift Histogram. V_{CM} = V_{DD}/2, T_A = -40°C to +125°C.*

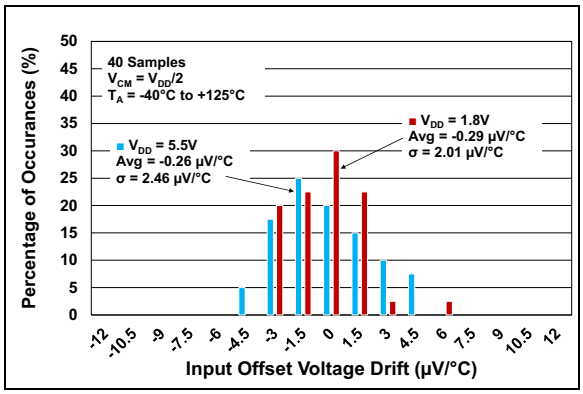


FIGURE 2-2: *Input Offset Voltage Drift Histogram. T_A = -40°C to +125°C.*

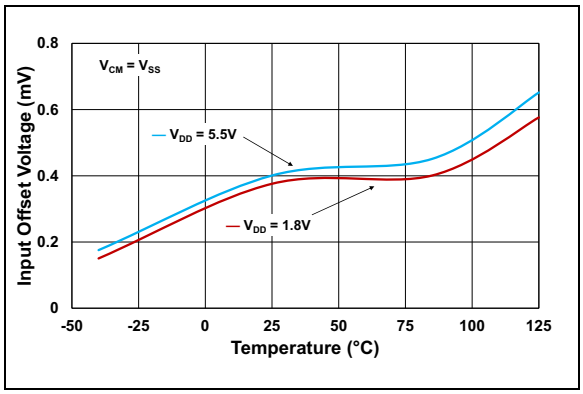


FIGURE 2-5: *Input Offset Voltage vs. Temperature. V_{CM} = V_{SS}.*

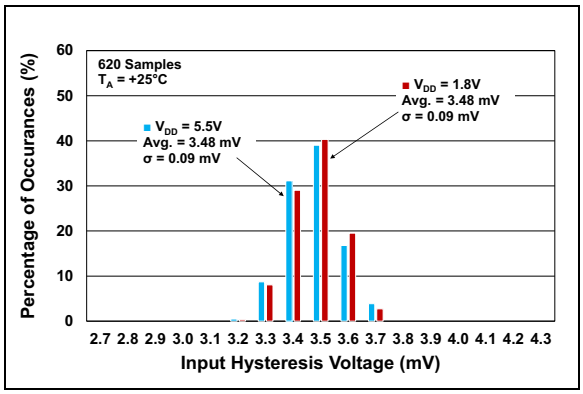


FIGURE 2-3: *Input Hysteresis Voltage Histogram. T_A = +25°C.*

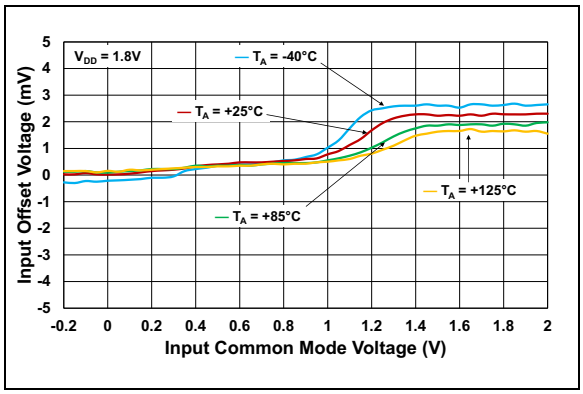


FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage. V_{DD} = 1.8V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

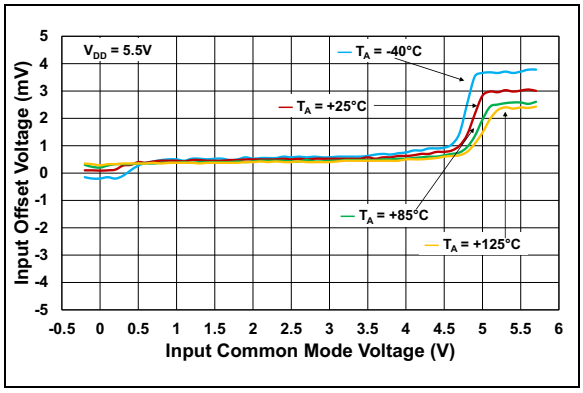


FIGURE 2-7: *Input Offset Voltage vs. Common Mode Input Voltage. V_{DD} = 5.5V.*

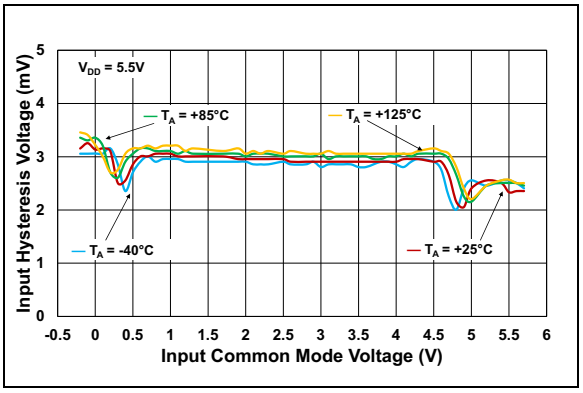


FIGURE 2-10: *Input Hysteresis Voltage vs. Common Mode Input Voltage. V_{DD} = 5.5V.*

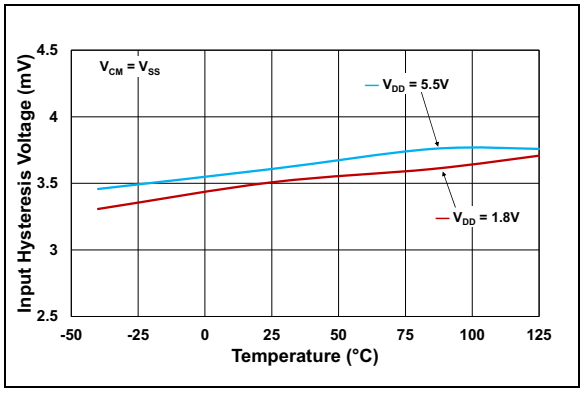


FIGURE 2-8: *Input Hysteresis Voltage vs. Ambient Temperature. V_{CM} = V_{SS}.*

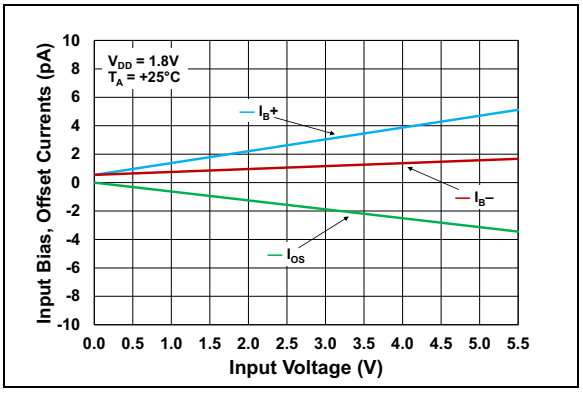


FIGURE 2-11: *Input Bias and Offset Current vs. Common Mode Input Voltage. V_{DD} = 1.8V, T_A = +25°C.*

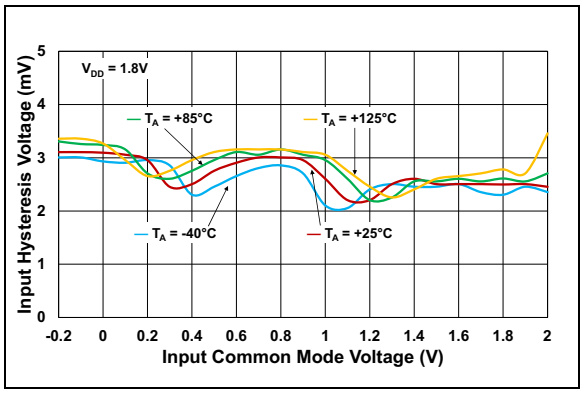


FIGURE 2-9: *Input Hysteresis Voltage vs. Common Mode Input Voltage. V_{DD} = 1.8V.*

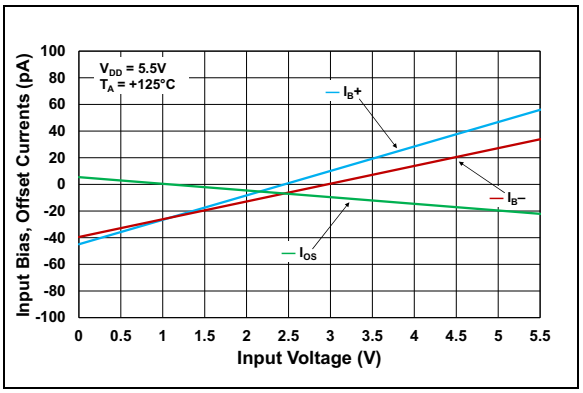


FIGURE 2-12: *Input Bias and Offset Current vs. Common Mode Input Voltage. V_{DD} = 5.5V, T_A = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

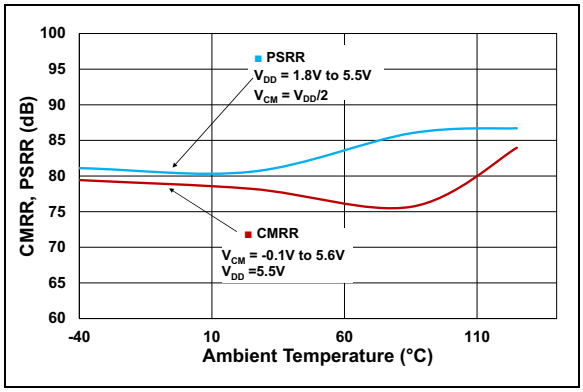


FIGURE 2-13: *CMRR, PSRR vs. Temperature.*

2.2 Other DC Voltages and Currents

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

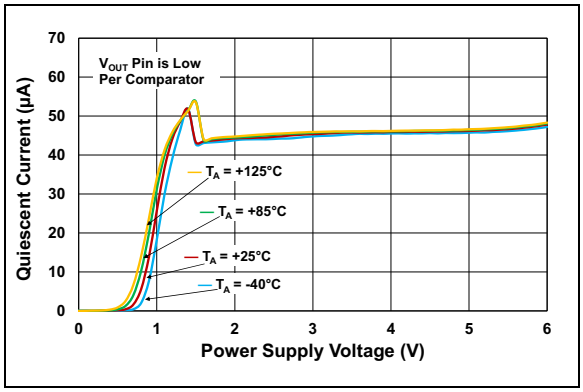


FIGURE 2-14: *Quiescent Current vs. Power Supply Voltage. V_{OUT} Pin is Low.*

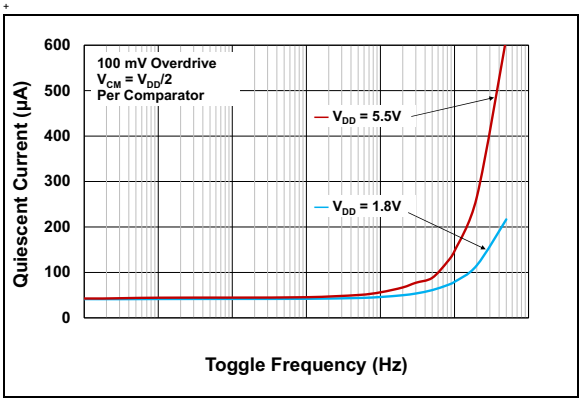


FIGURE 2-17: *Quiescent Current vs. Toggle Frequency.*

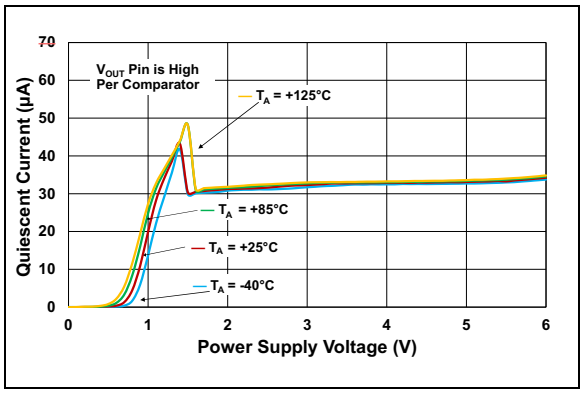


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage. V_{OUT} Pin is High.*

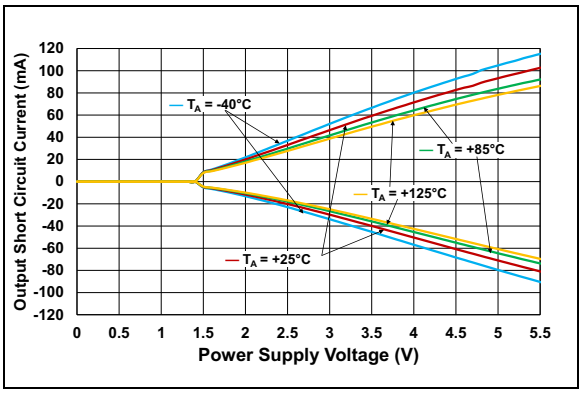


FIGURE 2-18: *Output Short Circuit Current vs. Power Supply Voltage.*

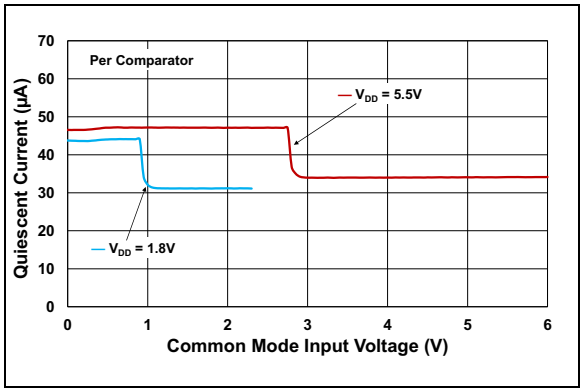


FIGURE 2-16: *Quiescent Current vs. Common Mode Input Voltage.*

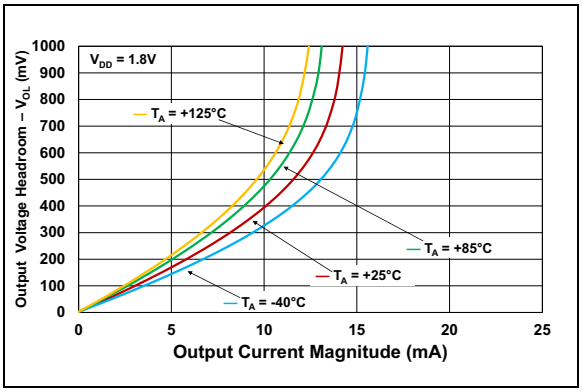


FIGURE 2-19: *Output Voltage Headroom – V_{OL} vs. Output Current. V_{DD} = 1.8V.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

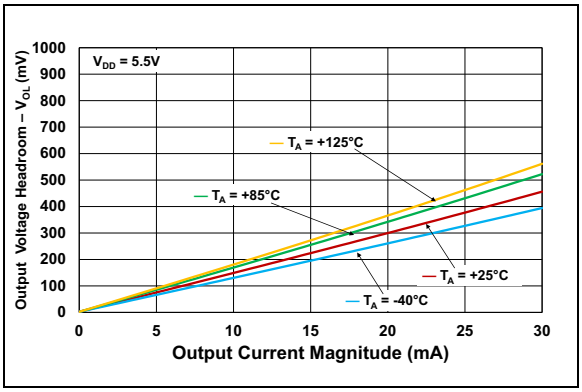


FIGURE 2-20: *Output Voltage Headroom – V_{OL} vs. Output Current. V_{DD} = 5.5V.*

2.3 Time Responses

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

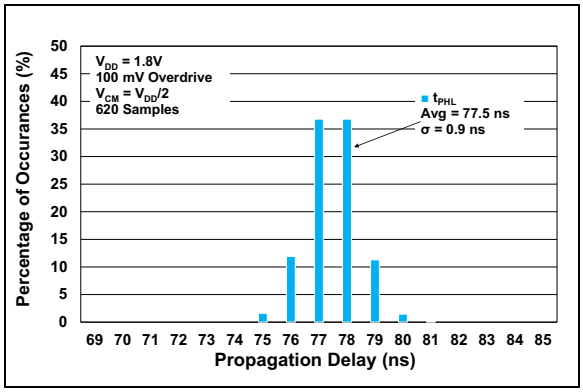


FIGURE 2-21: *High-to-Low Propagation Delay Histogram. V_{DD} = 1.8V.*

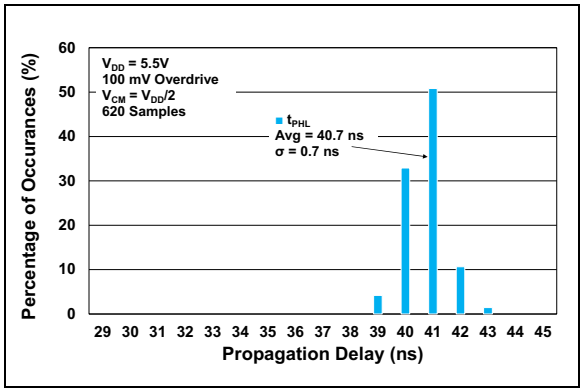


FIGURE 2-22: *High-to-Low Propagation Delay Histogram. V_{DD} = 5.5V*

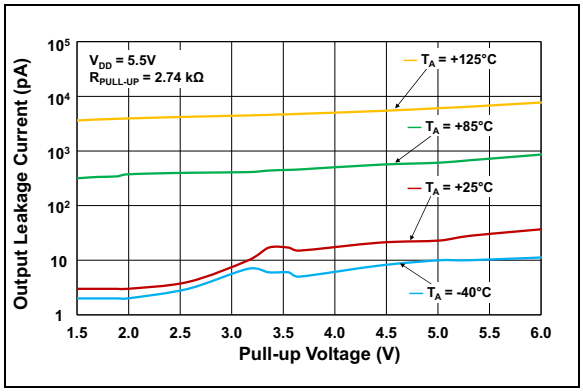


FIGURE 2-23: *Propagation Delay vs. Pull-up Voltage.*

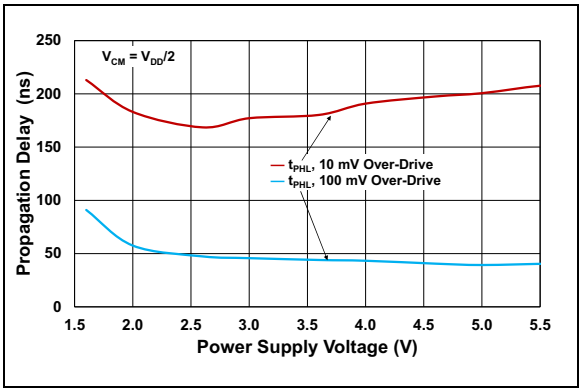


FIGURE 2-24: *Propagation Delay vs. Power Supply Voltage.*

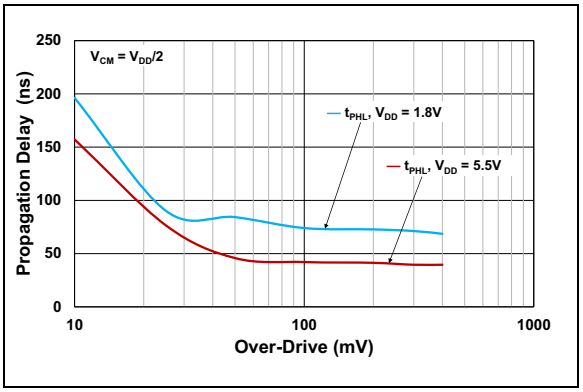


FIGURE 2-25: *Propagation Delay vs. Input Overdrive.*

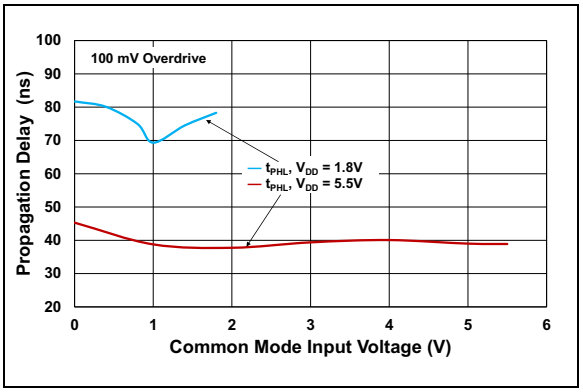


FIGURE 2-26: *Propagation Delay vs. Common Mode Input Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 1.8V to 5.5V, V_{SS} = GND, V_{IN}- = V_{DD}/2, V_{IN}+ = V_{SS}, $R_{PULL-UP}$ = 2.74 kΩ, $V_{PULL-UP}$ = V_{DD} and C_L = 15 pF.

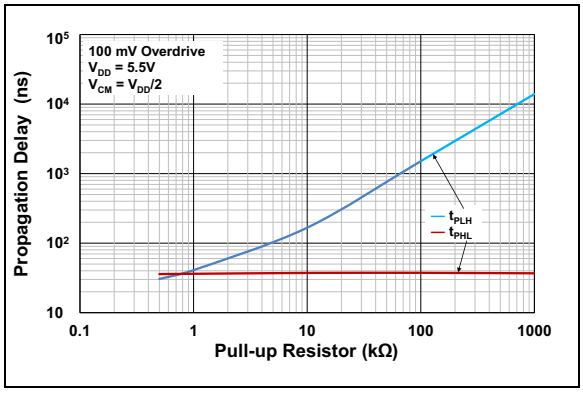


FIGURE 2-27: *Propagation Delay vs. Pull-up Resistor.*

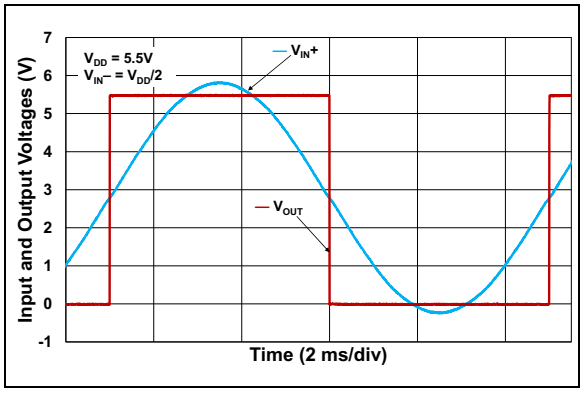


FIGURE 2-30: *Input and Output Voltages, No Phase Reversal.*

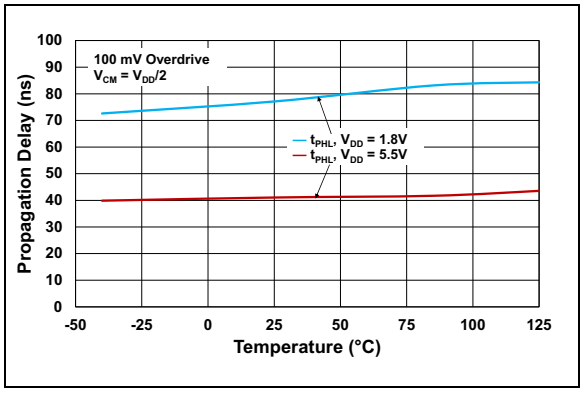


FIGURE 2-28: *Propagation Delay vs. Temperature.*

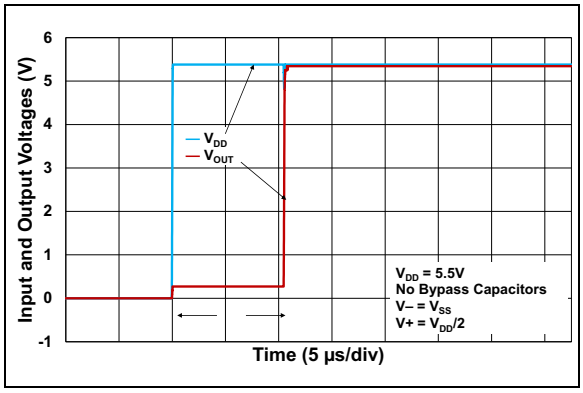


FIGURE 2-31: *Startup Time.*

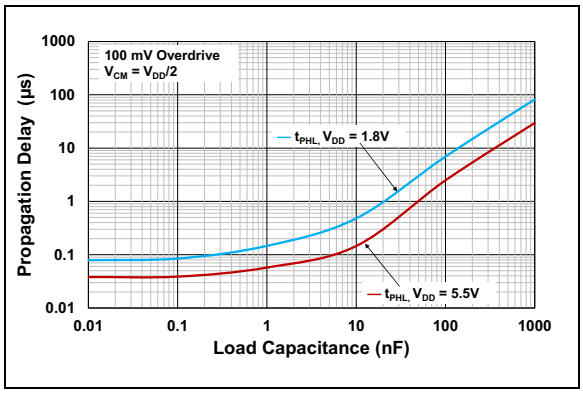


FIGURE 2-29: *Propagation Delay vs. Load Capacitance.*

3.0 PIN DESCRIPTIONS

Pin descriptions are listed in the following tables: Table 3-1 for MCP6576/6R/6U, Table 3-2 for MCP6577 and Table 3-3 for MCP6579.

TABLE 3-1: MCP6576/6R/6U PIN DESCRIPTIONS

MCP6576	MCP6576R	MCP6576U	Symbol	Description
5-Lead SC70, SOT-23	5-Lead SOT-23	5-Lead SC70, SOT-23		
1	1	4	V_{OUT}	Digital Output
2	5	2	V_{SS}	Negative Power Supply
3	3	1	$V_{IN}+$	Noninverting Input
4	4	3	$V_{IN}-$	Inverting Input
5	2	5	V_{DD}	Positive Power Supply

TABLE 3-2: MCP6577 PIN DESCRIPTIONS

MCP6577	Symbol	Description
8-Lead MSOP, SOIC		
1	V_{OUTA}	Digital Output, Comparator A
2	$V_{INA}-$	Inverting Input, Comparator A
3	$V_{INA}+$	Noninverting Input, Comparator A
4	V_{SS}	Negative Power Supply
5	$V_{INB}+$	Noninverting Input, Comparator B
6	$V_{INB}-$	Inverting Input, Comparator B
7	V_{OUTB}	Digital Output, Comparator B
8	V_{DD}	Positive Power Supply

TABLE 3-3: MCP6579 PIN DESCRIPTIONS

MCP6579	Symbol	Description
14-Lead TSSOP, SOIC		
1	V_{OUTA}	Digital Output, Comparator A
2	$V_{INA}-$	Inverting Input, Comparator A
3	$V_{INA}+$	Noninverting Input, Comparator A
4	V_{DD}	Positive Power Supply
5	$V_{INB}+$	Noninverting Input, Comparator B
6	$V_{INB}-$	Inverting Input, Comparator B
7	V_{OUTB}	Digital Output, Comparator B
8	V_{OUTC}	Digital Output, Comparator C
9	$V_{INC}-$	Inverting Input, Comparator C
10	$V_{INC}+$	Noninverting Input, Comparator C
11	V_{SS}	Negative Power Supply
12	$V_{IND}+$	Noninverting Input, Comparator D
13	$V_{IND}-$	Inverting Input, Comparator D
14	V_{OUTD}	Digital Output, Comparator D

3.1 Digital Output Pins (V_{OUTx})

The V_{OUT}, V_{OUTA}, V_{OUTB}, V_{OUTC} and V_{OUTD} pins are CMOS open-drain comparator outputs and require an external pull-up resistor. They are designed to ease the implementation of level shifting and wired OR logic connections.

3.2 Analog Input Pins ($V_{INx}+$, $V_{INx}-$)

The $V_{IN}+$, $V_{IN}-$, $V_{INA}+$, $V_{INA}-$, $V_{INB}+$, $V_{INB}-$, $V_{INC}+$, $V_{INC}-$, $V_{IND}+$ and $V_{IND}-$ pins are analog noninverting ($V_{INx}+$) and inverting ($V_{INx}-$) inputs of the comparators. They are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{SS}, V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). During normal operation, the other pins function at voltages between V_{SS} and V_{DD}.

Usually, MCP6576/6R/6U/7/9 devices are used in single (positive) supply configuration. In this case, the V_{SS} pin connects to ground and the V_{DD} pin connects to the power supply. The positive power voltage requires a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin.

Optionally, the power supply pins can share a bulk capacitor with nearby analog parts, within 100 mm of the pins.

4.0 MCP6576/6R/6U/7/9 DEVICE OPERATION

4.1 General Description

MCP6576/6R/6U/7/9 devices are open-drain output comparators. They are suitable for a wide range of high speed applications requiring low power consumption.

4.2 Comparator Inputs

4.2.1 NORMAL OPERATION

The MCP6576/6R/6U/7/9 devices have internally set hysteresis, V_{HYST}. This voltage is small enough to maintain input offset accuracy across the entire input common mode range (V_{CMR}) and large enough to eliminate output chattering caused by the input noise voltage of the comparator, E_{ni}.

Figure 4-1 shows the output voltage and an 100 mV ramping input voltage, $V_{IN}+$, across the reference voltage, $V_{IN}-$, while Figure 4-2 has a smaller voltage scale to better show the different trigger points on the input voltage.

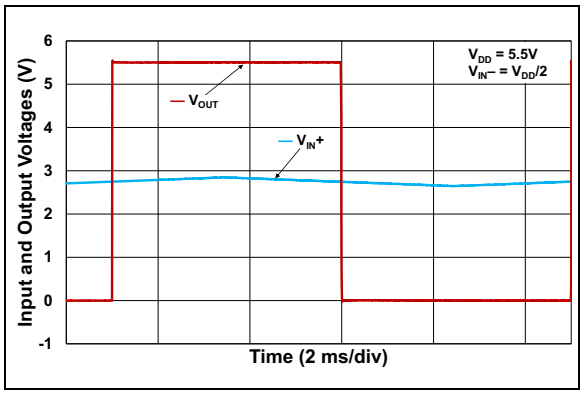


FIGURE 4-1: *Input Voltage Hysteresis, V_{HYST}.*

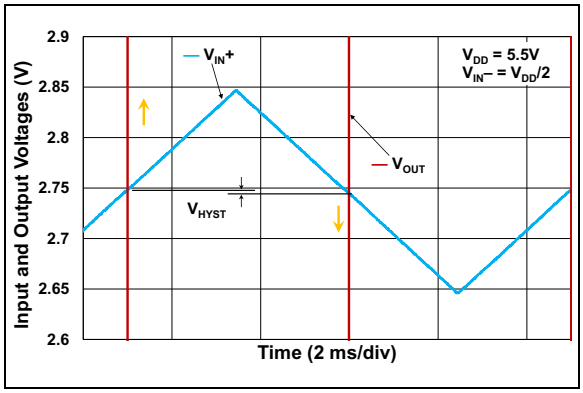


FIGURE 4-2: *Input Voltage Hysteresis, V_{HYST} (Smaller Voltage Scale).*

4.2.2 INPUT VOLTAGE LIMITS

To prevent damage and/or improper amplifier operation, the circuit must limit the voltages at the input pins. For more details, see **Section 1.1, "Absolute Maximum Ratings"**.

The Electrostatic Discharge (ESD) protection on the input pins can be as shown in Figure 4-3. This structure was selected to protect input transistors against many, but not all, overvoltage conditions and to minimize the input bias current, I_B.

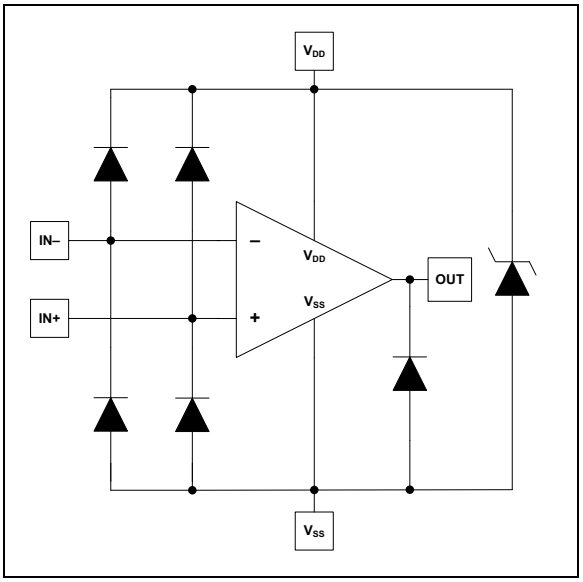


FIGURE 4-3: *Simplified Analog Input ESD Structures.*

ESD diodes clamp inputs that go more than one diode drop below V_{SS}. They also clamp any voltages that exceed V_{DD}. Their breakdown voltage is high enough to allow normal operation. At V_{DD} + 0.5V or V_{SS} – 0.5V, the input currents are typically < 2 mA. Very fast ESD events that meet the specifications are limited to prevent damage.

4.2.3 INPUT CURRENT LIMITS

To prevent damage and/or improper amplifier operation, the circuit must limit the currents at the input pins. For more details, see **Section 1.1, "Absolute Maximum Ratings"**.

Figure 4-4 shows one approach to protect these inputs. Resistors R_1 and R_2 limit the possible currents in or out of the input pins through the ESD diodes to either V_{DD} or V_{SS}. Use Equation 4-1 to determine the minimum value for R_1 and R_2.

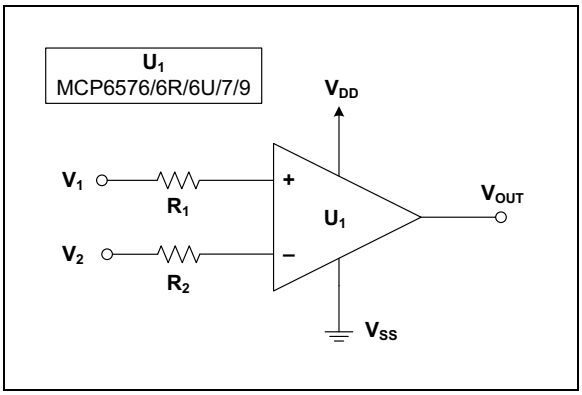


FIGURE 4-4: *Protecting Analog Inputs.*

EQUATION 4-1:

$$min(R_1, R_2) > \frac{V_{SS} - min(V_1, V_2)}{2\ \text{mA}}$$

$$min(R_1, R_2) > \frac{max(V_1, V_2) - V_{DD}}{2\ \text{mA}}$$

Where:

R_1 = Noninverting Input Resistance (kΩ)
R_2 = Inverting Input Resistance (kΩ)
V_{SS} = Negative Supply Voltage (V)
V_1 = Noninverting Input Voltage (V)
V_2 = Inverting Input Voltage (V)
V_{DD} = Positive Supply Voltage (V)

4.2.4 PHASE REVERSAL

MCP6576/6R/6U/7/9 uses CMOS transistors at the input. These transistors are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-30 shows an input voltage that exceeds both supply voltages with no resulting phase inversion.

4.2.5 POWER-ON RESET (POR)

MCP6576/6R/6U/7/9 has a POR circuit that sets the output to high impedance until the supply voltage (V_{DD}) exceeds the POR threshold. When the supply voltage exceeds the POR threshold, the output drives to the correct state determined by the input pins.

Figure 4-5 shows a typical output voltage waveform with a rising supply voltage (V_{DD}). The plot indicates the output is enabled after V_{DD} exceeds 1.45V.

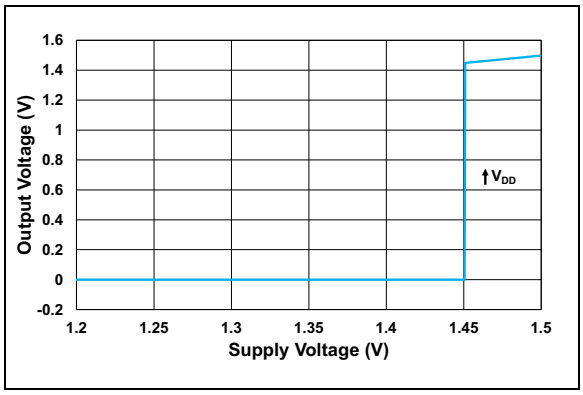


FIGURE 4-5: *POR Rising.*

Figure 4-6 shows the output voltage waveform for the same device when the supply voltage is decreasing. The plot indicates that the output is disabled when V_{DD} falls below 1.36V.

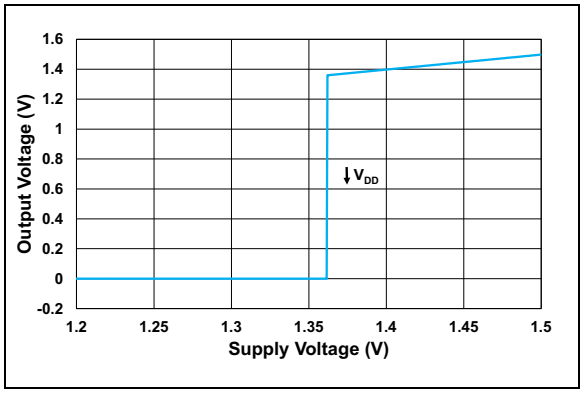


FIGURE 4-6: *POR Falling.*

4.3 Open-Drain Output

The open-drain output is designed to ease the implementation of level shifting and wired OR logic connections. The output stage minimizes switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low or from low-to-high. For more details, see Figure 2-19 and Figure 2-20.

4.4 Externally Set Hysteresis

MCP6576/6R/6U/7/9 have a small internal hysteresis voltage between the rising and falling trigger levels. Use external resistors to achieve larger levels of hysteresis.

The input offset voltage (V_{OS}) is the center (or average) of the input-referred low-to-high and high-to-low trip points, while the input hysteresis voltage (V_{HYST}) is the difference between the same trip points. V_{HYST} reduces output chattering when one input is slowly moving past the other, resulting in a reduced dynamic supply current.

4.4.1 NONINVERTING CIRCUIT

Figure 4-7 shows a noninverting circuit for single supply applications using two external resistors and Figure 4-8 shows the resulting hysteresis diagram. The trip voltage points (V_{TLH} and V_{THL}) are determined using Equation 4-2.

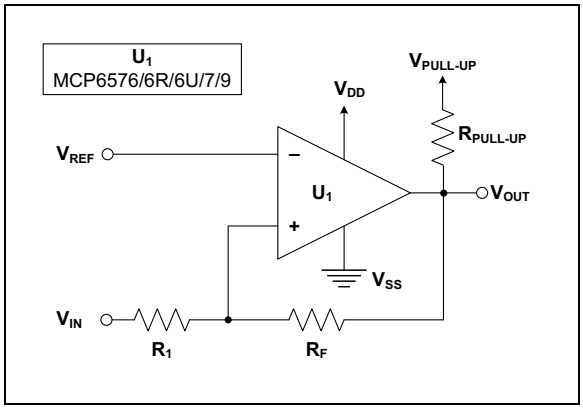


FIGURE 4-7: *Noninverting Circuit with Hysteresis.*

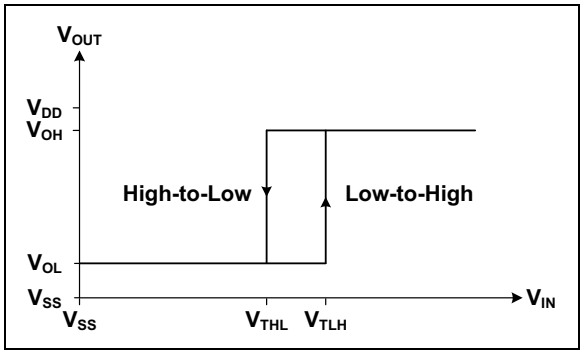


FIGURE 4-8: *Hysteresis Diagram for Noninverting Circuit.*

EQUATION 4-2:

$$V_{TLH} = V_{REF} \times \left(1 + \frac{R_1}{R_F}\right) - V_{OL} \times \frac{R_1}{R_F}$$

$$V_{THL} = V_{REF} \times \left(1 + \frac{R_1}{R_F}\right) - V_{OH} \times \frac{R_1}{R_F}$$

Where:

V_{TLH} = Trip Voltage from Low to High (V)
V_{REF} = Reference Voltage (V)
R_1 = Input Resistance (kΩ)
R_F = Feedback Resistance (kΩ)
V_{OL} = Output Voltage, Low (V)
V_{THL} = Trip Voltage from High to Low (V)
V_{OH} = Output Voltage, High (V)

4.4.2 INVERTING CIRCUIT

Figure 4-9 shows a single supply inverting circuit using two external resistors, while Figure 4-10 shows the resulting hysteresis diagram.

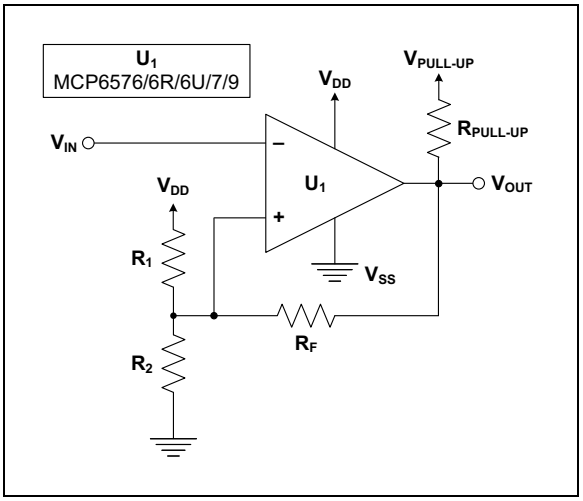


FIGURE 4-9: *Inverting Circuit with Hysteresis.*

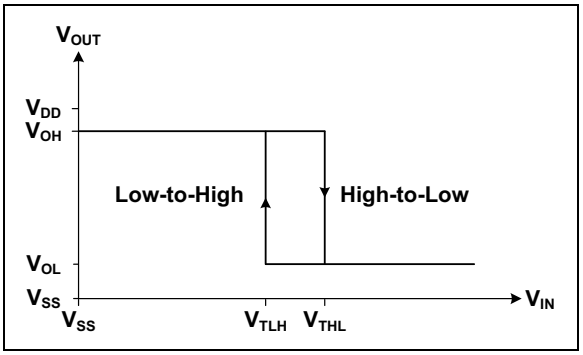


FIGURE 4-10: *Hysteresis Diagram for Inverting Circuit.*

Figure 4-11 shows the Thevenin equivalent circuit, where R_{12} and V_{12} are calculated using Equation 4-3 and the trip points are determined using Equation 4-4.

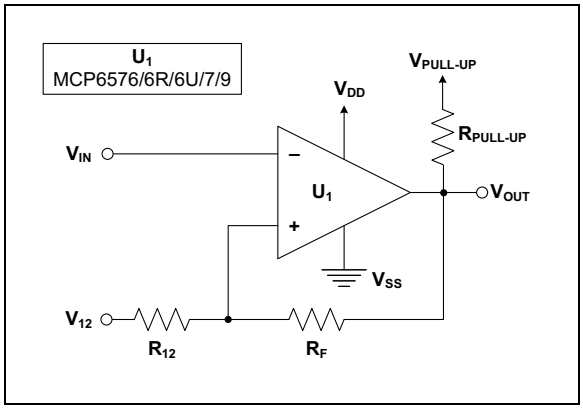


FIGURE 4-11: *Thevenin Equivalent Circuit.*

EQUATION 4-3:

$$R_{12} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{12} = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

Where:

R_{12} = Thevenin Resistance (kΩ)
R_1 = Noninverting Input Resistance (kΩ)
R_2 = inverting Input Resistance (kΩ)
V_{12} = Thevenin Voltage (V)
V_{DD} = Positive Supply Voltage (V)

EQUATION 4-4:

$$V_{TLH} = V_{OL} \times \frac{R_{12}}{R_{12} + R_F} + V_{12} \times \frac{R_F}{R_{12} + R_F}$$

$$V_{THL} = V_{OH} \times \frac{R_{12}}{R_{12} + R_F} + V_{12} \times \frac{R_F}{R_{12} + R_F}$$

Where:

V_{TLH} = Trip Voltage from Low to High (V)
V_{OL} = Output Voltage, Low (V)
R_{12} = Thevenin Resistance (kΩ)
R_F = Feedback Resistance (kΩ)
V_{12} = Thevenin Voltage (V)
V_{THL} = Trip Voltage from High to Low (V)
V_{OH} = Output Voltage, High (V)

4.5 Start-up

MCP6576/6R/6U/7/9 quickly controls the output when power (V_{DD}) is initially applied to the device (start-up). Bypass capacitors are removed during start-up testing to minimize the inrush currents (see Figure 4-12). The start-up time is measured from when V_{DD} is applied to the circuitry and up to when the output toggles high.

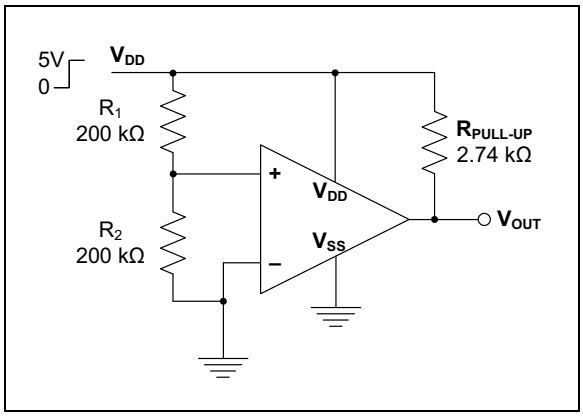


FIGURE 4-12: *Start-up Test Circuit.*

Figure 4-13 shows the power supply voltage (blue line) and the output voltage (red line) for MCP6577. When power is first applied to MCP6577, the output is turned off (point A) and is high impedance until V_{POR} is exceeded. After 11 µs (typical), the output is turned on (point B).

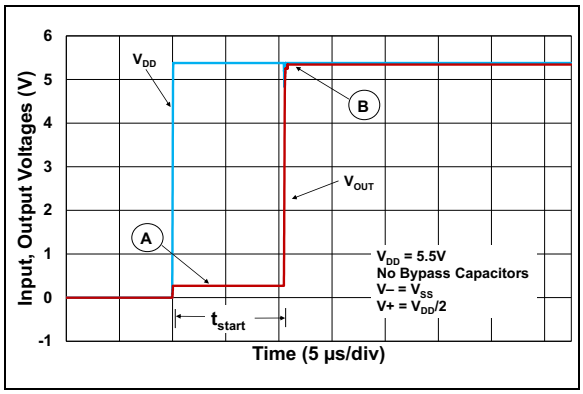


FIGURE 4-13: *Start-up Test Waveforms.*

4.6 Capacitive Loads

MCP6576/6R/6U/7/9 has a push-pull output. When the output switches, an increase in output sinking or sourcing current can appear during output transition. Excessive capacitive loads can increase the supply current and propagation delay or decrease slew rate during output transitions.

Figure 2-29 shows the increase in propagation delay versus the increase in output capacitance. Figure 2-17 shows the increase in quiescent current versus the increase in toggle frequency (rate of transitions from low-to-high and from high-to-low).

4.7 Supply Bypass

For good edge rate performance, connect a local bypass capacitor (0.01 µF to 0.1 µF) within 2 mm of the MCP6576/6R/6U/7/9 power supply pin (VDD for single supply applications).

4.8 PCB Surface Leakage

In applications where low input bias current is critical, take into consideration the printed circuit board (PCB) surface leakage effects. Surface leakage is caused by humidity, dust or other contaminates present on the PCB. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5V difference causes a current of 5 pA to flow. This is greater than the bias current of MCP6576/6R/6U/7/9 at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around pins (or traces) that are susceptible to this effect. The guard ring is biased at the same voltage as the susceptible pin or trace. Figure 4-14 is an example of a guard ring layout.

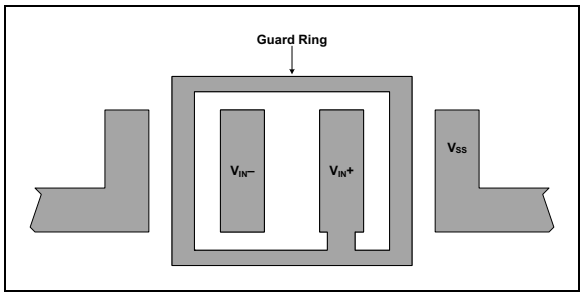


FIGURE 4-14: *Guard Ring Layout for Inverting Gain (Example).*

4.8.1 INVERTING CONFIGURATION

To implement the guard ring in inverting configurations (for example, Figure 4-9), follow these steps:

1. Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage (V_{REF}) as the comparator (for example, V_{DD}/2 or ground).
2. Connect the inverting input pin (V_{IN}-) to the input pad without touching the guard ring.

4.8.2 NONINVERTING CONFIGURATION

To implement the guard ring in noninverting configurations (for example, Figure 4-7), follow these steps:

1. Connect the noninverting input pin (V_{IN}+) to the input pad without touching the guard ring.
2. Connect the guard ring to the inverting pin (V_{IN}-).

4.9 Unused Comparators

MCP6577 has two comparators, while MCP6579 has four comparators. Unused comparators in dual or quad packages must be configured as shown in Figure 4-15. These circuits prevent the output from toggling and causing crosstalk, while using the minimum number of components and drawing minimal current.

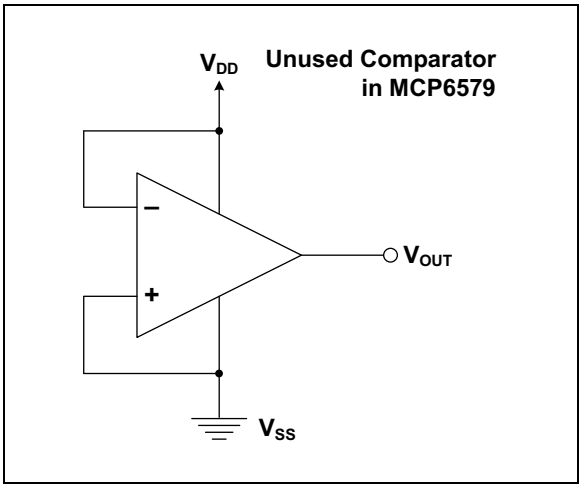


FIGURE 4-15: *Unused Comparator.*

4.10 Application Circuits

4.10.1 WINDOW COMPARATOR

MCP6576/6R/6U/7/9 can be used to make a windowed comparator. Figure 4-16 shows one approach using the MCP6577 dual comparator. The device outputs a logic high when the input voltage is between V_{LO} and V_{HI} (V_{HI} > V_{LO}). Connect a three resistor voltage divider to V_{DD} or another voltage rail to set V_{HI} and V_{LO} thresholds.

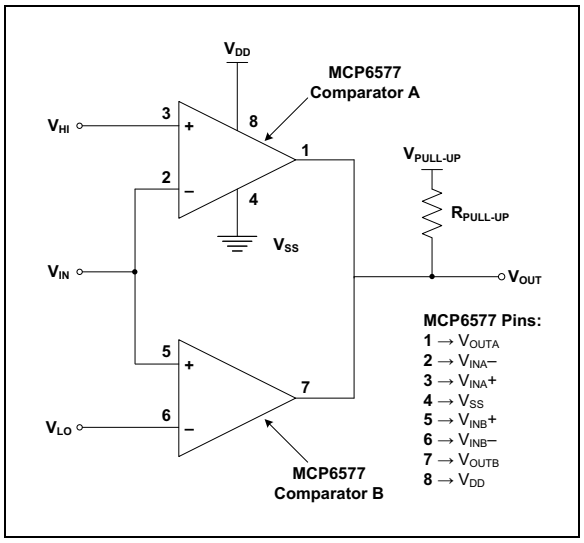


FIGURE 4-16: *Windowed Comparator.*

4.10.2 BISTABLE MULTIVIBRATOR

Figure 4-17 presents a simple bistable multivibrator design. V_{REF} must be between the supply voltages (V_{SS} = GND and V_{DD}) to achieve oscillation. The output duty cycle changes with V_{REF}.

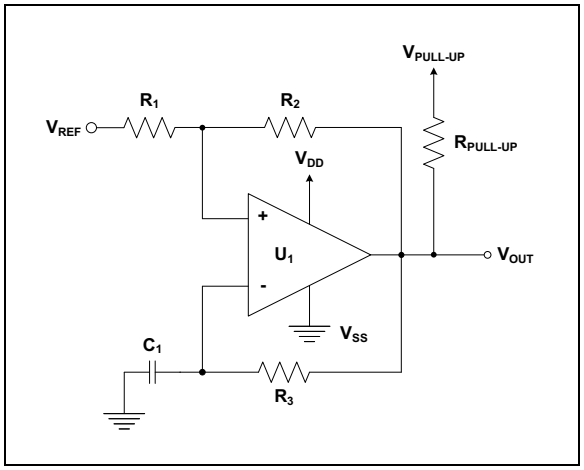


FIGURE 4-17: *Bistable Multivibrator.*

5.0 DESIGN AIDS

Microchip Technology Inc. provides the basic design tools needed for MCP6576/6R/6U/7/9.

5.1 SPICE Macro Model

The latest SPICE macro model for MCP6576/6R/6U/7/9 is available on the Microchip website at microchip.com. This model intends to be an initial design tool that works well in the comparator's linear region of operation over the temperature range. See the SPICE model file for information on its capabilities.

Bench testing is very important in any design and must not be replaced with simulations. Also, validate simulation results using the SPICE macro model by comparing them to the data sheet specifications and characteristic curves.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards designed to facilitate a faster time to market. For a complete listing of these boards and their corresponding User's Guides and technical information, visit the Microchip website at microchipdirect.com.

Following are some boards that are especially useful:

- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- Voltage Supervisor SOT23-5/6 Evaluation Board (P/N VSUPEV2)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

5.3 Applications Notes

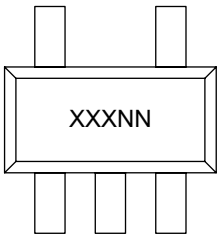
The following Microchip Analog Design Notes and Application Notes are available on the Microchip website at microchip.com/appnotes. These are recommended as supplemental reference resources.

- **AN895** – *"Oscillator Circuits For RTD Temperature Sensors"*, DS00895

6.0 PACKAGING INFORMATION

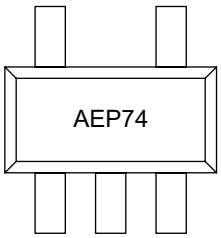
6.1 Package Marking Information

5-Lead SC70 (**MCP6576** and **MCP6576U**)

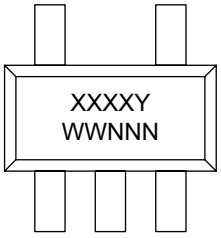


Device	Marking
MCP6576	AEPNN
MCP6576U	AEQNN

Example:

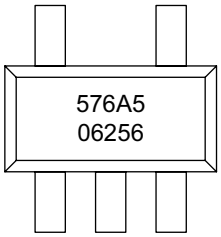


5-Lead SOT-23 (**MCP6576, MCP6576U** and **MCP6576R**)

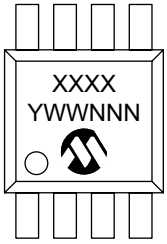


Device	Marking
MCP6576	576AY
MCP6576R	576RY
MCP6576U	576UY

Example:



8-Lead MSOP (**MCP6577**)



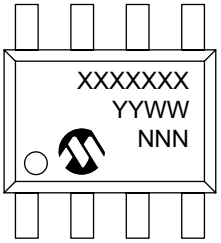
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

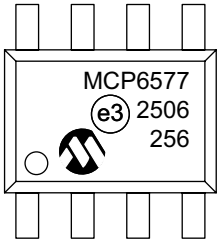
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

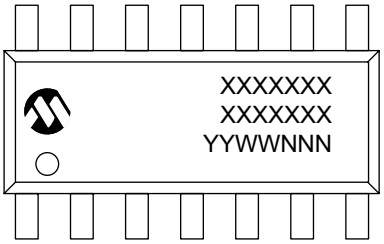
8-Lead SOIC, 150 mil (**MCP6577**)



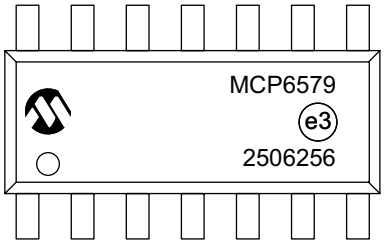
Example:



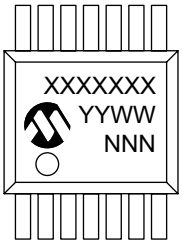
14-Lead SOIC, 150 mil (**MCP6579**)



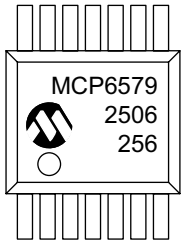
Example:



14-Lead TSSOP (**MCP6579**)



Example:



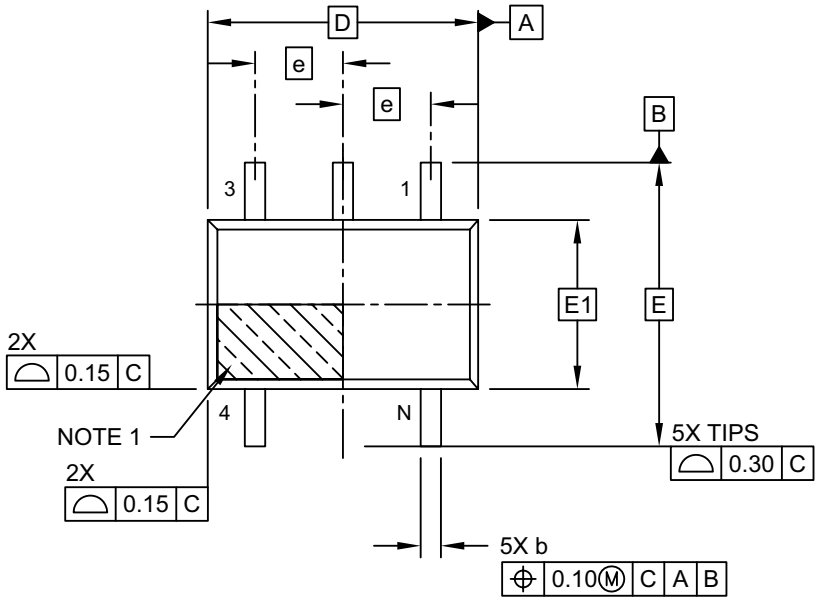
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

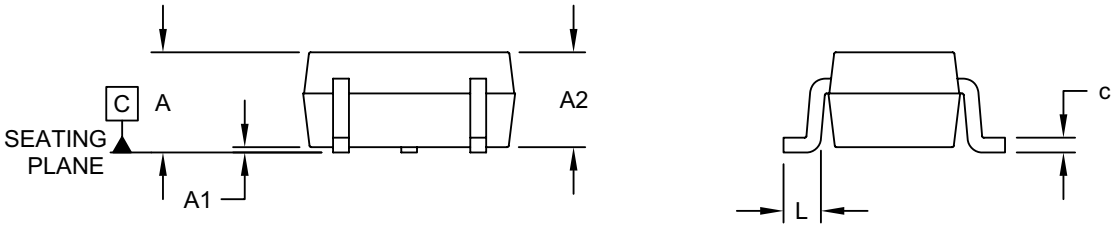
6.2 Package Drawings

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

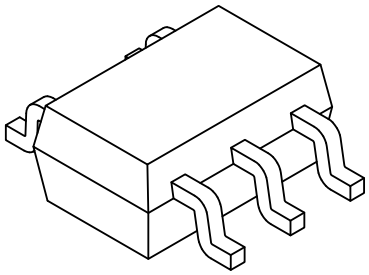


SIDE VIEW END VIEW

Microchip Technology Drawing C04-061-LTY Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

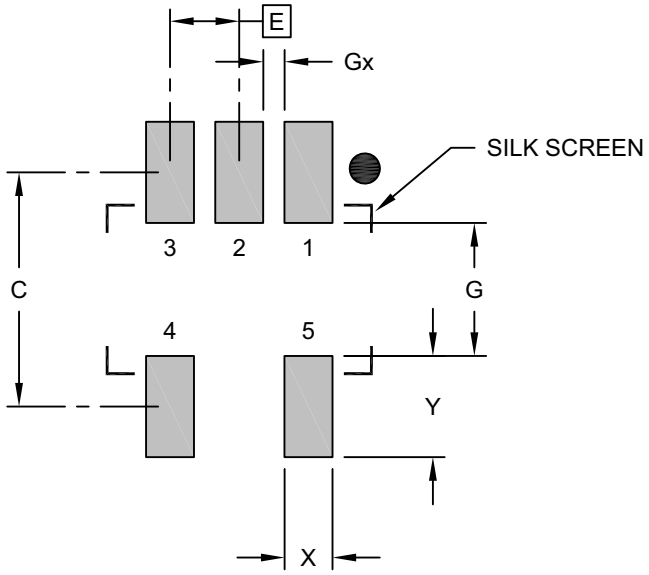
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LTY Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

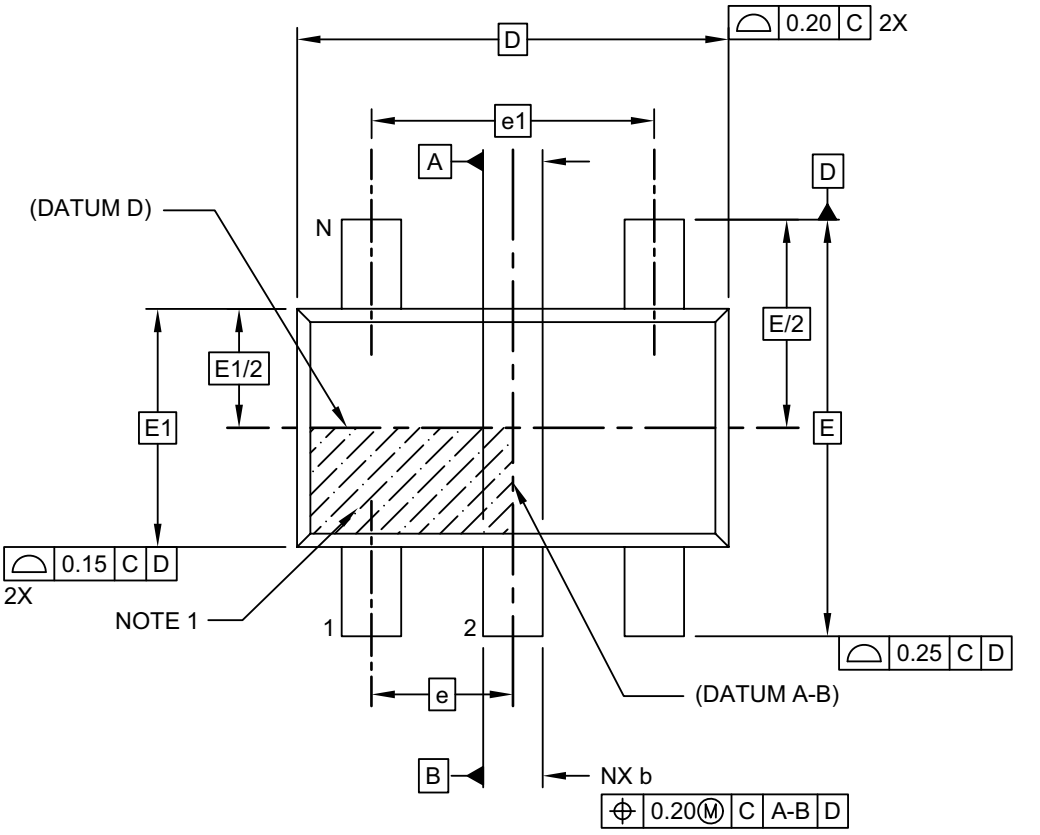
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

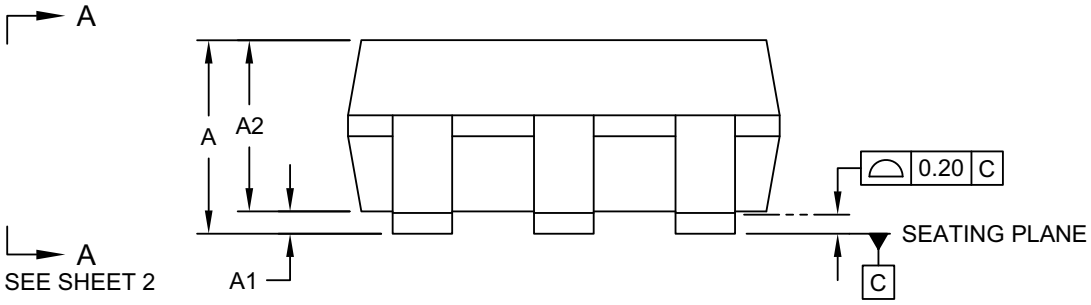
Microchip Technology Drawing No. C04-2061-LTY Rev E

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

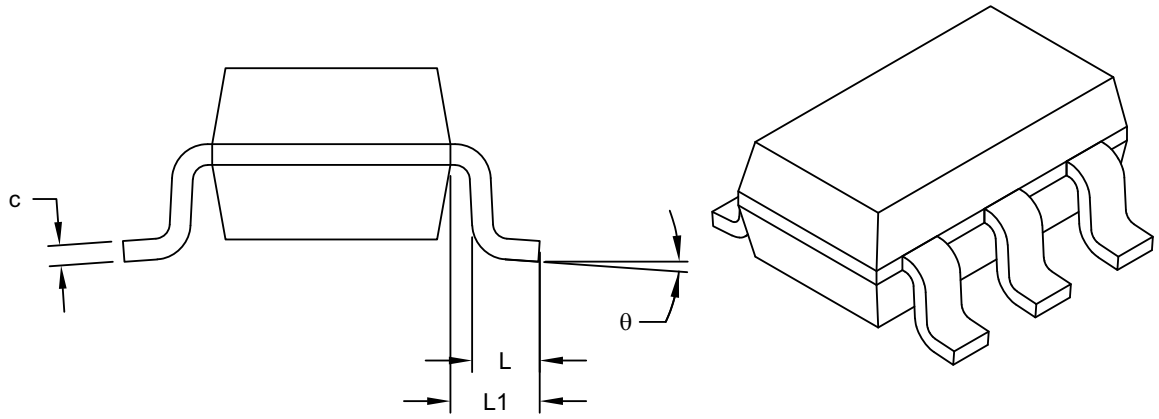


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

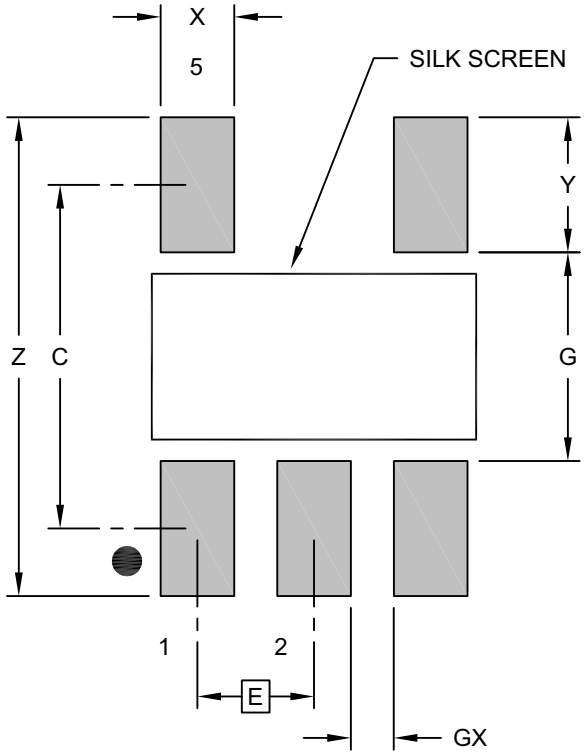
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

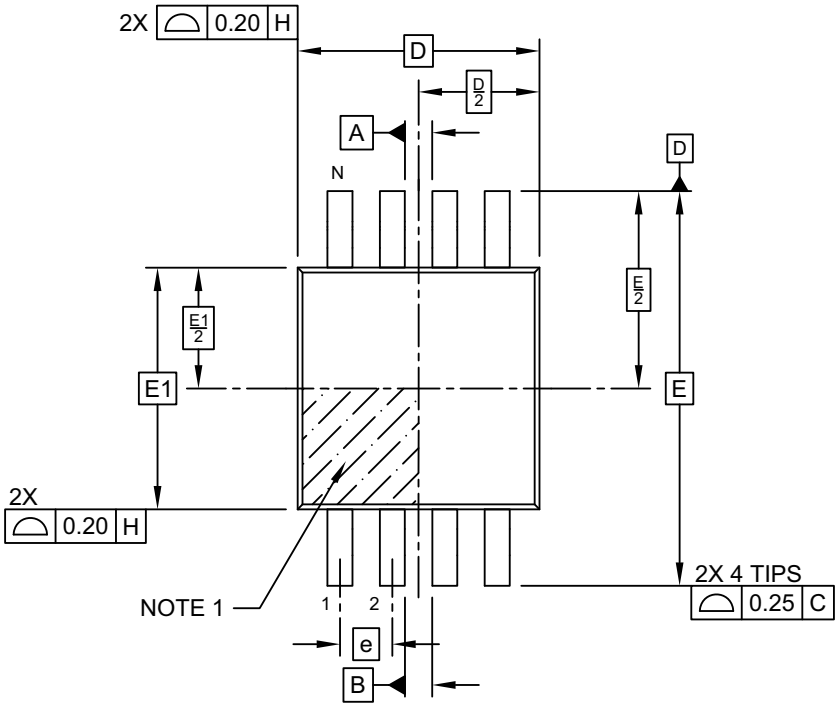
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

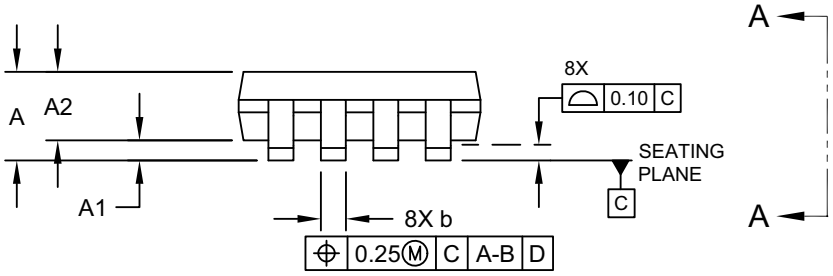
Microchip Technology Drawing No. C04-2091-OT Rev H

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

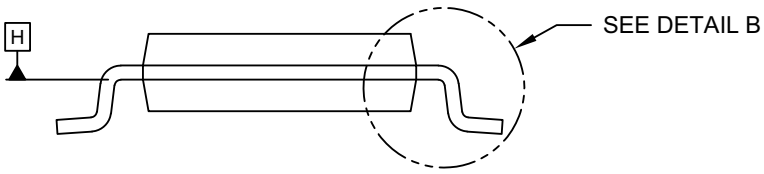
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

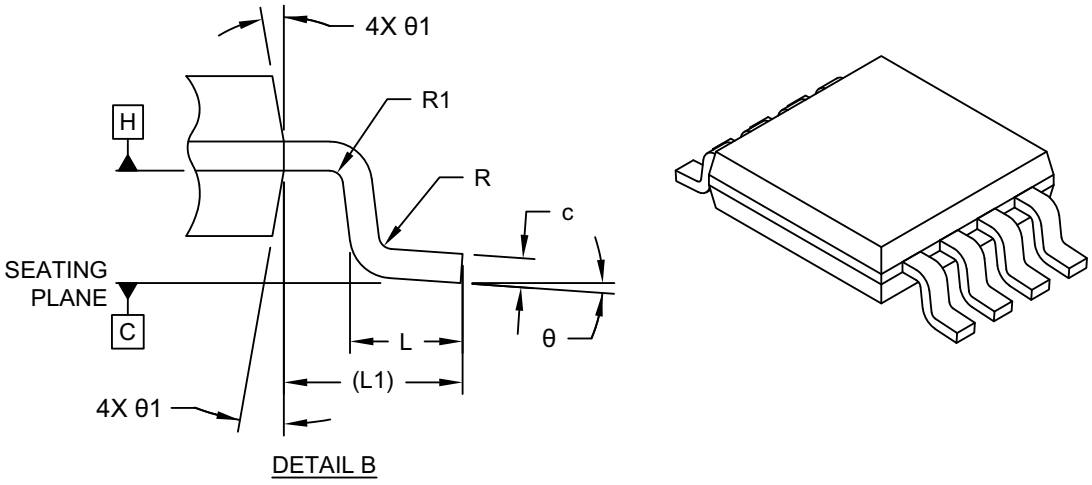


VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

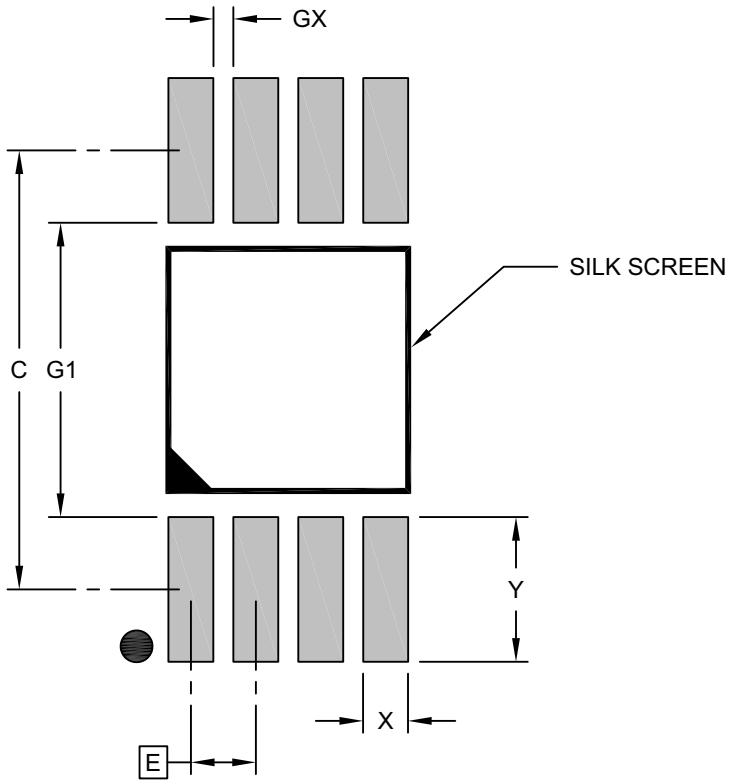
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

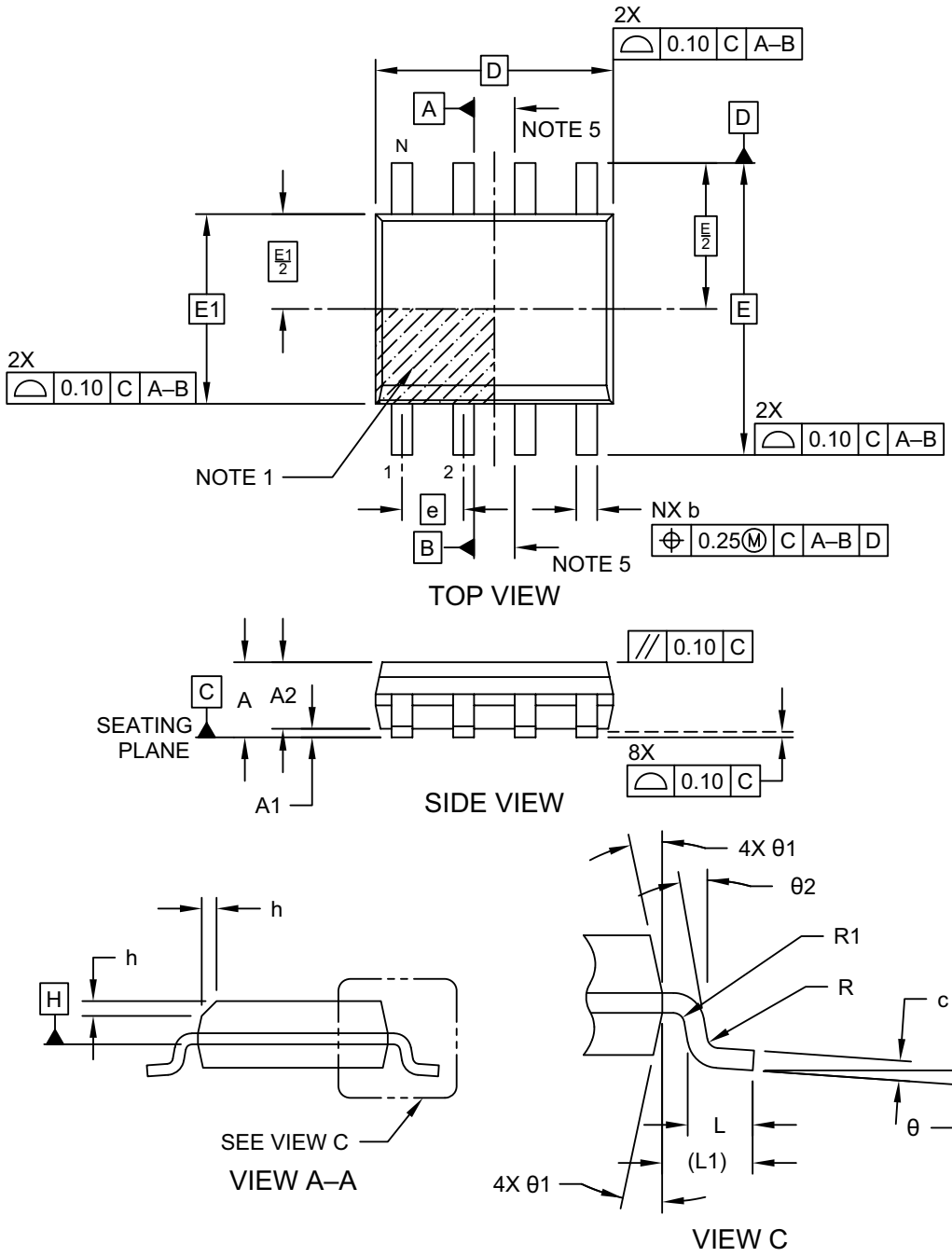
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

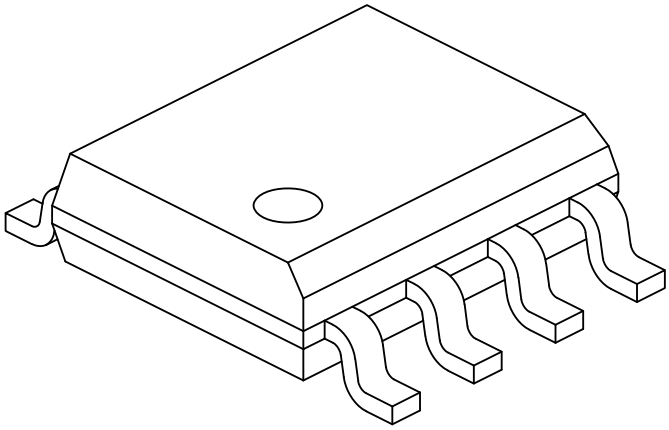
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

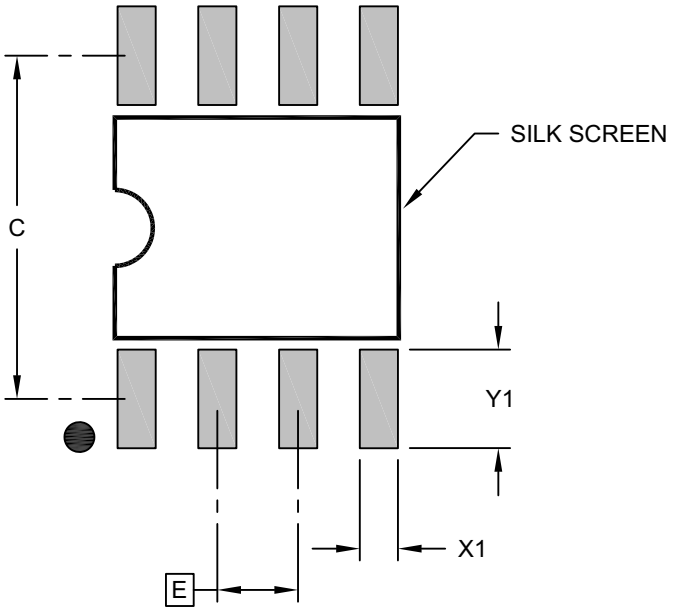
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

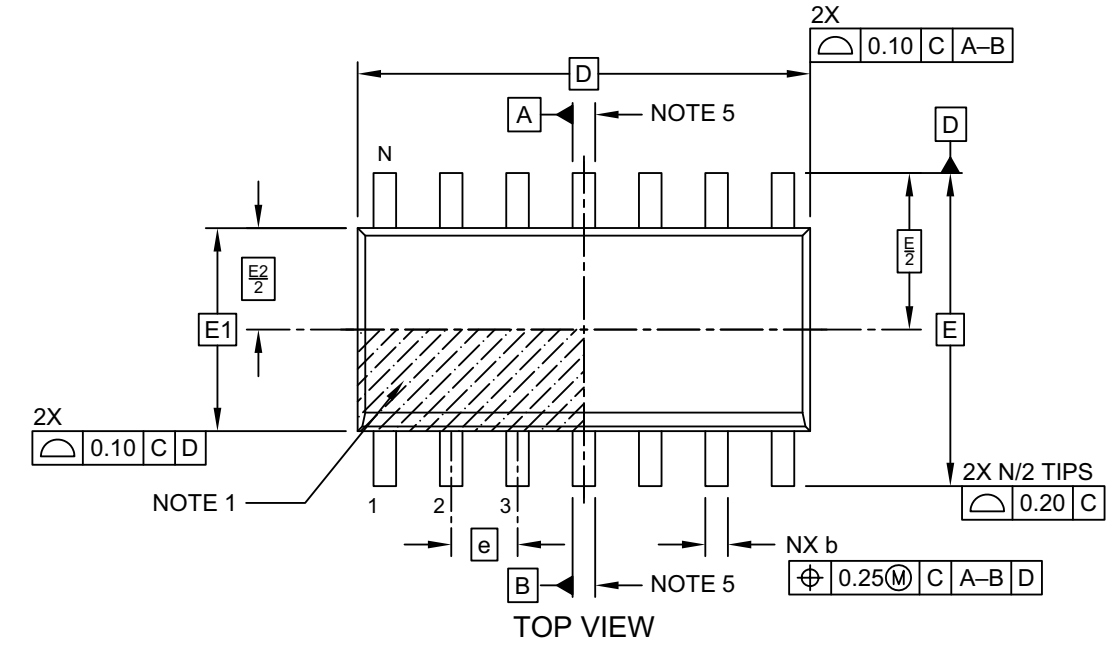
Notes:

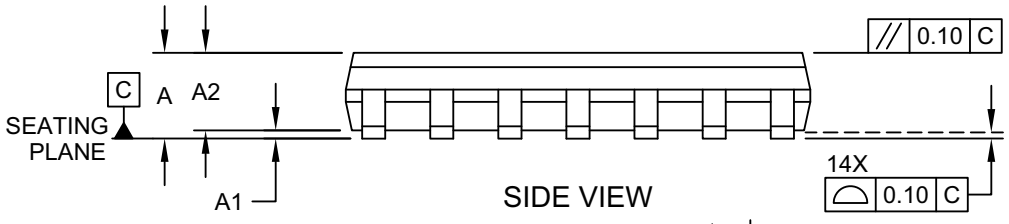
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

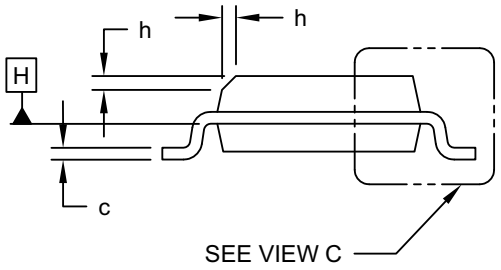
Microchip Technology Drawing C04-2057-SN Rev K

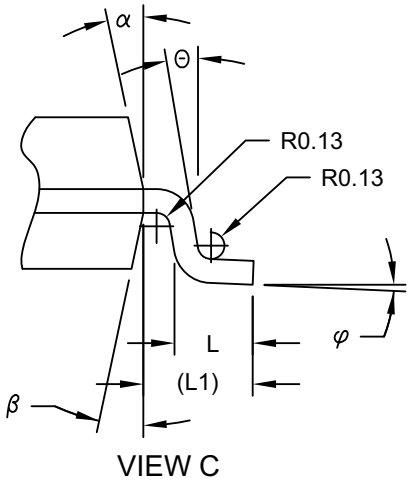
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





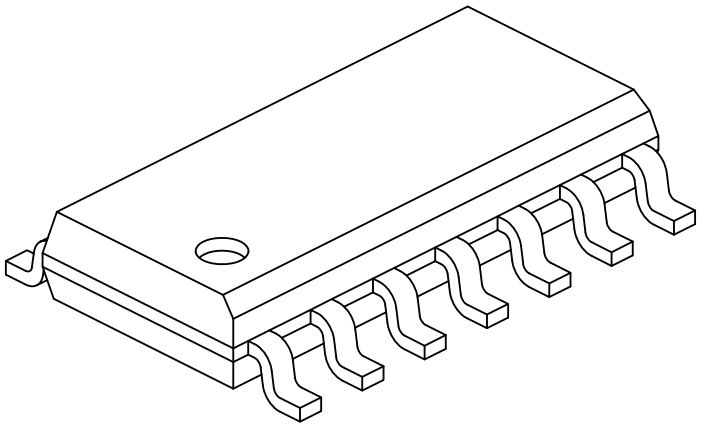




Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

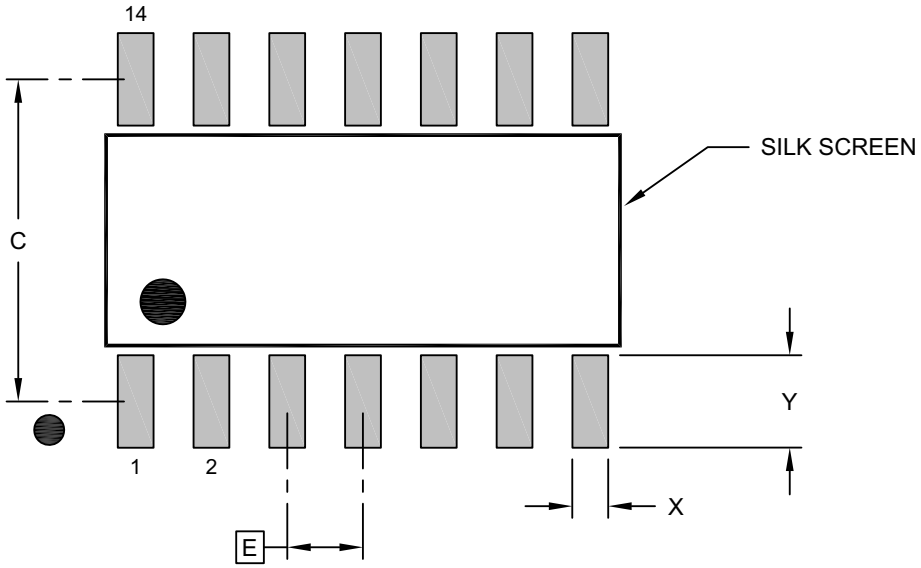
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

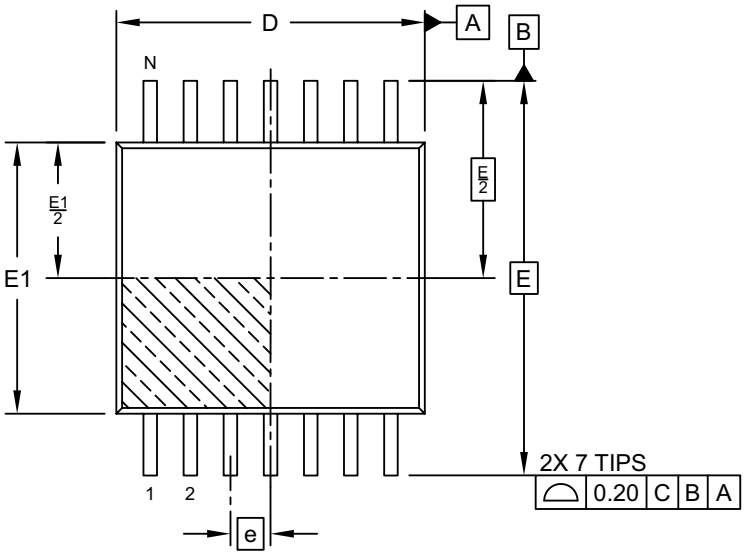
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

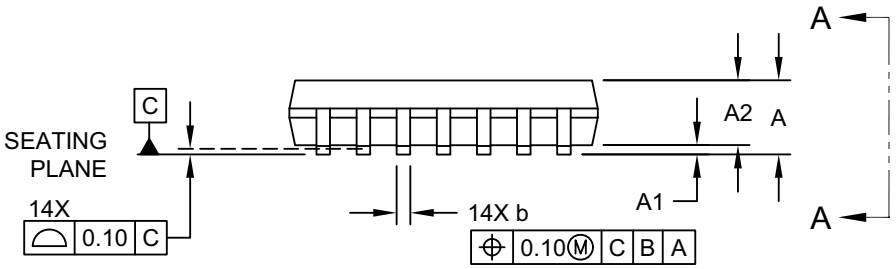
Microchip Technology Drawing No. C04-2065-SL Rev D

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

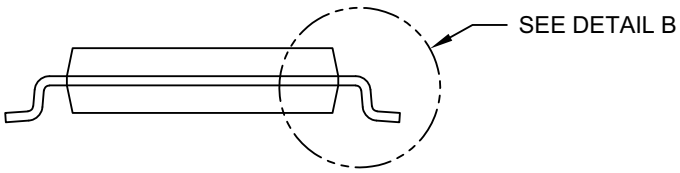
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

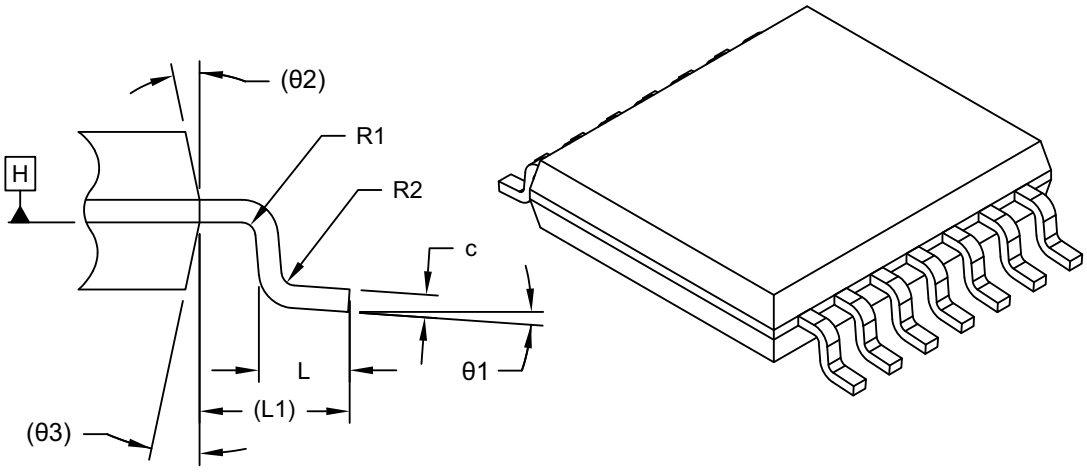


VIEW A–A

Microchip Technology Drawing C04-087 Rev E Sheet 1 of 2

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

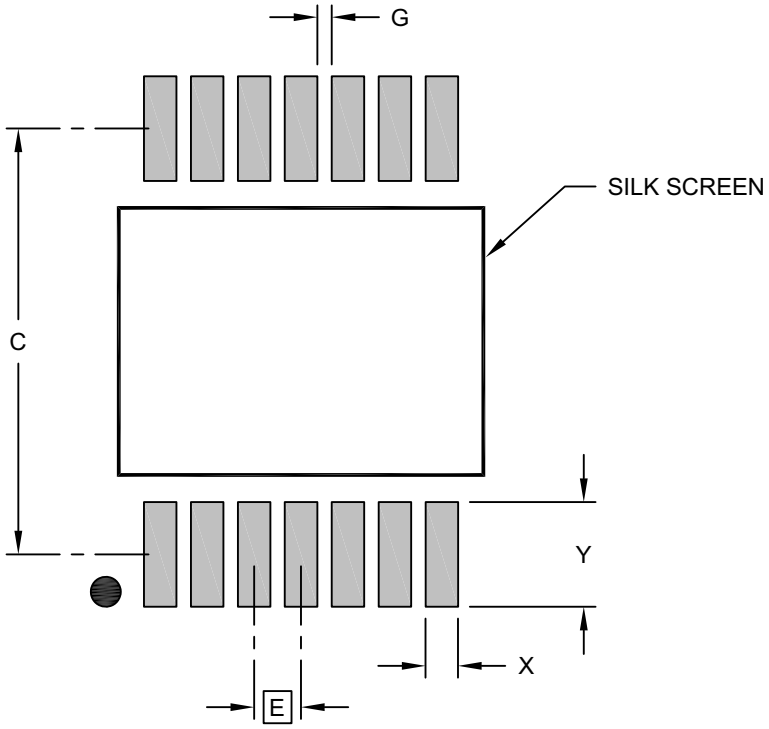
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087 Rev E Sheet 2 of 2

14-Lead Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev E

APPENDIX A: REVISION HISTORY

Revision A (February 2025)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	T[1]	-E	/XX	XXX[2]
Device	Tape and Reel	Temperature Range	Package	Class

Device:	MCP6576	= Low Power Open-Drain Output Single Comparator
	MCP6576R	= Low Power Open-Drain Output Single Comparator
	MCP6576U	= Low Power Open-Drain Output Single Comparator
	MCP6577	= Low Power Open-Drain Output Dual Comparator
	MCP6579	= Low Power Open-Drain Output Quad Comparator
Tape and Reel Option:	T	= Tape and Reel[1]
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	LT	= 5-Lead Plastic Small Outline Transistor (SC70)
	OT	= 5-Lead Plastic Small Outline Transistor (SOT-23)
	MS	= 8-Lead Plastic Micro Small Outline Package, 3x3 mm Body (MSOP)
	SN	= 8-Lead Plastic Small Outline, 150 mil. Body (SOIC)
	SL	= 14-Lead Plastic Small Outline, 3.9 mm Body (SOIC)
	ST	= 14-Lead Thin Shrink Small Outline Package, 4.4 mm Body (TSSOP)
Class:	VAO	= Automotive
	Blank	= Non-Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6576T-E/LT = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SC70

b) MCP6576UT-E/LT = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SC70

c) MCP6576T-E/OT = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23

d) MCP6576RT-E/OT = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23

e) MCP6576UT-E/OT = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23

a) MCP6577T-E/MS = Low Power Open-Drain Output Dual Comparator, Tape and Reel, Extended Temperature, 8-Lead MSOP

b) MCP6577T-E/SN = Low Power Open-Drain Output Dual Comparator, Tape and Reel, Extended Temperature, 8-Lead SOIC

a) MCP6579T-E/SL = Low Power Open-Drain Output Quad Comparator, Tape and Reel, Extended Temperature, 14-Lead SOIC

b) MCP6579T-E/ST = Low Power Open-Drain Output Quad Comparator, Tape and Reel, Extended Temperature, 14-Lead TSSOP

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	T[1]	-E	/XX	XXX[2]
Device	Tape and Reel	Temperature Range	Package	Class

Device:	MCP6576	= Low Power Open-Drain Output Single Comparator
	MCP6576R	= Low Power Open-Drain Output Single Comparator
	MCP6576U	= Low Power Open-Drain Output Single Comparator
	MCP6577	= Low Power Open-Drain Output Dual Comparator
	MCP6579	= Low Power Open-Drain Output Quad Comparator
Tape and Reel Option:	T	= Tape and Reel[1]
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	LT	= 5-Lead Plastic Small Outline Transistor (SC70)
	OT	= 5-Lead Plastic Small Outline Transistor (SOT-23)
	MS	= 8-Lead Plastic Micro Small Outline Package, 3x3 mm Body (MSOP)
	SN	= 8-Lead Plastic Small Outline, 150 mil. Body (SOIC)
	SL	= 14-Lead Plastic Small Outline, 3.9 mm Body (SOIC)
	ST	= 14-Lead Thin Shrink Small Outline Package, 4.4 mm Body (TSSOP)
Class:	VAO	= Automotive
	Blank	= Non-Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a) MCP6576T-E/LTVAO = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SC70, Automotive

b) MCP6576UT-E/LTVAO = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SC70, Automotive

c) MCP6576T-E/OTVAO = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

d) MCP6576RT-E/OTVAO = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

e) MCP6576UT-E/OTVAO = Low Power Open-Drain Output Single Comparator, Tape and Reel, Extended Temperature, 5-Lead SOT-23, Automotive

a) MCP6577T-E/MSVAO = Low Power Open-Drain Output Dual Comparator, Tape and Reel, Extended Temperature, 8-Lead MSOP, Automotive

b) MCP6577T-E/SNVAO = Low Power Open-Drain Output Dual Comparator, Tape and Reel, Extended Temperature, 8-Lead SOIC, Automotive

a) MCP6579T-E/SLVAO = Low Power Open-Drain Output Quad Comparator, Tape and Reel, Extended Temperature, 14-Lead SOIC, Automotive

b) MCP6579T-E/STVAO = Low Power Open-Drain Output Quad Comparator, Tape and Reel, Extended Temperature, 14-Lead TSSOP, Automotive

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