MCP6571/1R/1U/2/4

1.8V, 40 ns Low-Power Push-Pull Output Comparator

Features

- Propagation Delay at V_{DD} = 5.5V:
  - 40 ns (typical) high-to-low
  - 33 ns (typical) low-to-high
- Low Quiescent Current: 70 µA (maximum per comparator)
- Low Input Offset Voltage: ±7 mV (maximum)
- Supply Voltage Range: 1.8V to 5.5V
- Rail-to-Rail Input
- Power-on-Reset
- **Small Packages**:
  - Singles in SC70-5, SOT-23-5
  - Dual in SOIC-8, MSOP-8
  - Quad in SOIC-14, TSSOP-14
- Extended Temperature Range:-40°C to +125°C
- AEC Q100 Qualified see **"Product Identification System (Automotive)"**

Applications

- Automotive
- Portable Equipment
- Medical Diagnostic Equipment
- RC Timers
- Sensor Conditioning

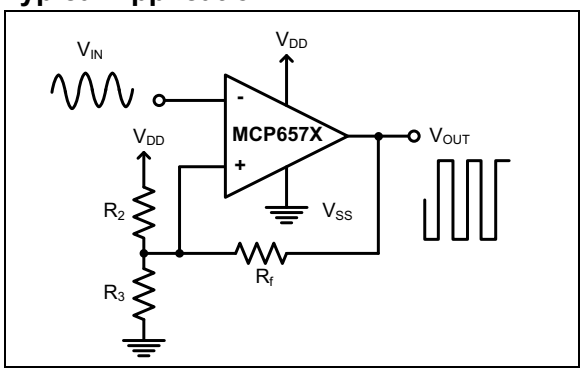
Design Aids

- SPICE Macro Models
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Devices

- Open-Drain Output: MCP6576/6R/6U/7/9

Typical Application



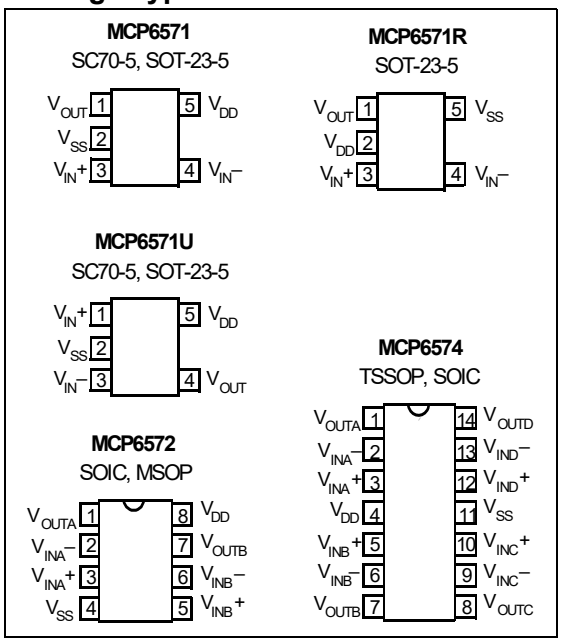
Description

The Microchip Technology Inc. MCP6571/1R/1U/2/4 family of CMOS/TTL compatible comparators operate with a single-supply voltage, as low as 1.8V, while drawing low-quiescent current (70 µA, maximum per comparator). This family of comparators incorporate a Power-on-Reset feature that keeps the output high impedance until the supply voltage V_{DD} rises to a sufficient voltage to control the comparator. They also have a low-input offset voltage (±7 mV, maximum).

These comparators are optimized for low-power, single supply applications with greater than rail-to-rail input operation. Internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw. These comparators are provided with push-pull outputs.

This family is offered in single (MCP6571), dual (MCP6572) and quad (MCP6574) packages. All devices are designed using an advanced CMOS process and fully specified in the extended temperature range from -40°C to +125°C.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

$V_{DD} - V_{SS}$ 6V
Current at Input Pins ($V_{IN}+$, $V_{IN}-$) ..... ±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)†† ..... V_{SS} – 0.5V to V_{DD} + 0.5V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current (Note 1) ..... Continuous
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature (T_J) ..... +1.50°C
ESD Protection on All Pins (HBM; CDM) ..... ≥ 2 kV; 1.5 kV

Note 1: Short-circuit to ground, one comparator per package

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage Limits"**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Power-on-Reset Voltage (1)	V_{POR}	—	—	1.6	V	
Quiescent Current per Comparator	I_Q	—	35	—	µA	I_O = 0, V_{OUT} = High
		30	45	70	µA	I_O = 0, V_{OUT} = Low
Power Supply Rejection Ratio	PSRR	60	80	—	dB	V_{CM} = V_{DD}/2
Input						
Input Offset Voltage (2)	V_{OS}	-7	—	+7	mV	V_{CM} = V_{DD}/2
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±1	—	µV/°C	T_A= -40°C to +125°C
Input Hysteresis Voltage (2)	V_{HYST}	1	—	6	mV	V_{CM} = V_{DD}/2
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	—	pA	
		—	20	—	pA	T_A= 85°C
		—	50	—	pA	T_A= 125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||4	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	

Note 1: The output is high impedance until V_{DD} exceeds V_{POR}.
2: V_{OS} is the center of the input-referred trip points. Hysteresis is the difference between the trip points.

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.2	—	V_{DD} + 0.2	V	T_A= -40°C to +125°C, Guaranteed by Characterization.
Common Mode Rejection Ratio	CMRR	54	75	—	dB	V_{DD} = 5.5V V_{CM} = V_{CML} to V_{CMH}
Push-Pull Output						
Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 0.2	—	V_{DD} – 0.2	V	V_{DD} = 5.5V, I_{OUT} = 4 mA
		V_{SS} + 0.3	—	V_{DD} – 0.42		V_{DD} = 1.8V, I_{OUT} = 4 mA
Output Short-Circuit Current	I_{SC}	—	±10	—	mA	V_{DD} = 1.8V
		—	±80	—	mA	V_{DD} = 5.5V
Startup Time	t_{start}	—	11	—	µs	V_{DD} = 0V to 5.5V

Note 1: The output is high impedance until V_{DD} exceeds V_{POR}.

2: V_{OS} is the center of the input-referred trip points. Hysteresis is the difference between the trip points.

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Propagation Delay						
High-to-Low, 100mV Overdrive	t_{PHL}	—	40	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Low-to-High, 100mV Overdrive	t_{PLH}	—	33	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Propagation Delay Skew (1)	t_{PDS}	—	±5	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Rise Time	t_R	—	5	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Fall Time	t_F	—	5	—	ns	V_{DD} = 5.5V, V_{CM} = V_{DD}/2
Maximum Toggle Frequency	f_{TG}	—	4	—	MHz	V_{DD} = 5.5V
		—	2	—	MHz	V_{DD} = 1.8V
Noise						
Input Noise Voltage	E_{ni}	—	400	—	μV_{P-P}	f = 10 Hz to 100 kHz

Note 1: Propagation delay skew is defined as: t_{PDS} = t_{PLH} - t_{PHL}.

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	221	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.3 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

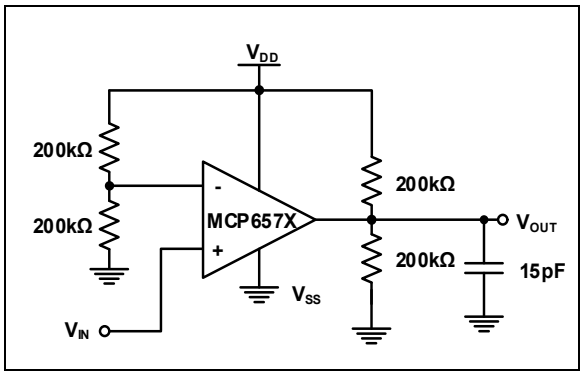


FIGURE 1-1: *AC and DC Test Circuit for the Push-Pull Output Comparators.*

1.4 Propagation Measurement

The following diagram is used to determine the propagation delay measurements.

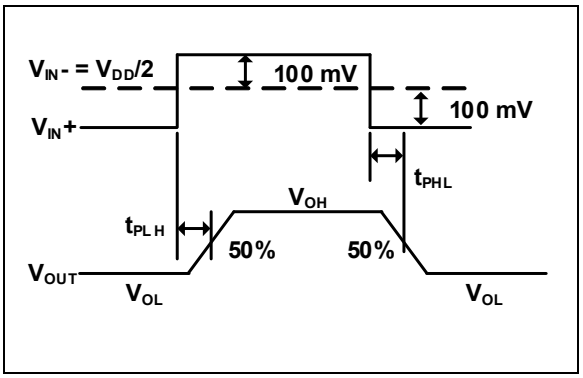


FIGURE 1-2: *Propagation Delay Timing Diagram*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, $V_{IN-} = V_{DD}/2$, $V_{IN+} = V_{SS}$, $V_{OUT} = V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 15 pF.

2.1 DC Inputs

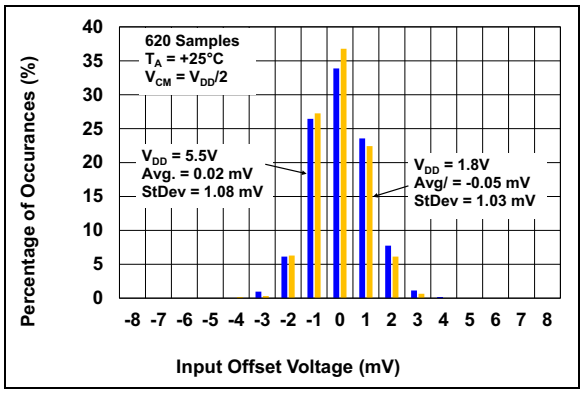


FIGURE 2-1: *Input Offset Voltage Histogram.*

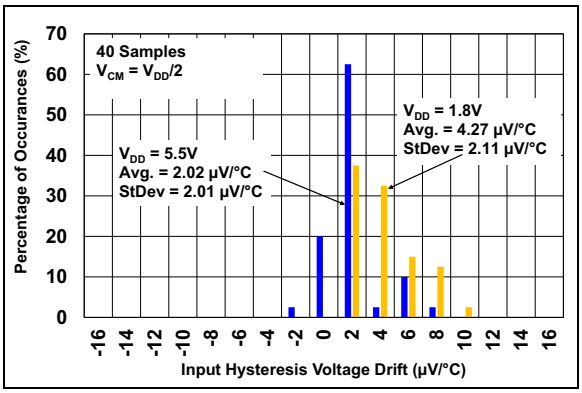


FIGURE 2-4: *Input Hysteresis Voltage Drift Histogram.*

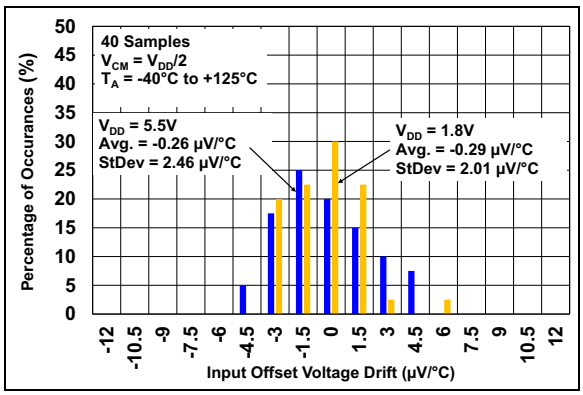


FIGURE 2-2: *Input Offset Voltage Drift Histogram.*

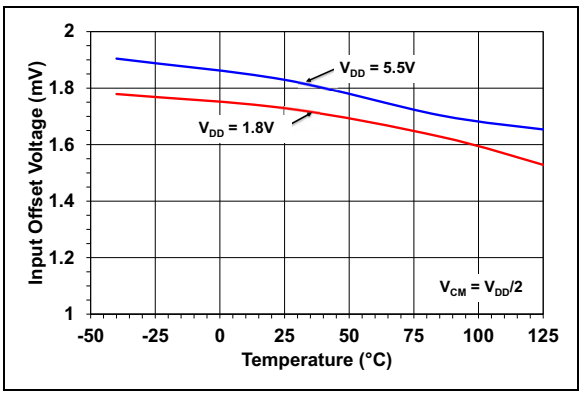


FIGURE 2-5: *Input Offset Voltage vs. Temperature.*

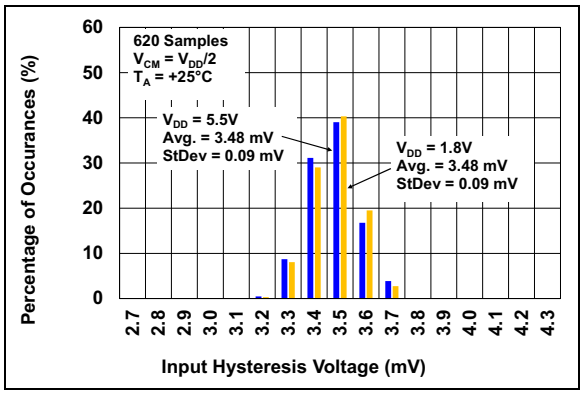


FIGURE 2-3: *Input Hysteresis Voltage Histogram.*

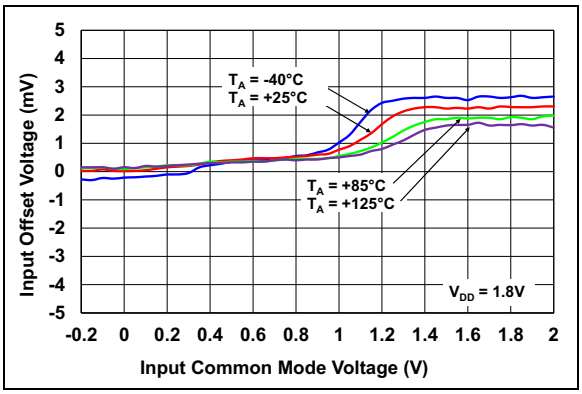


FIGURE 2-6: *Input Offset Voltage vs. Common Mode Input Voltage (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.

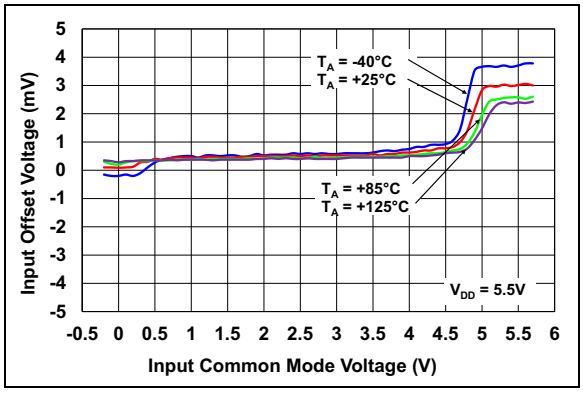


FIGURE 2-7: *Input Offset Voltage vs. Common-Mode Input Voltage (V_{DD} = 5.5V).*

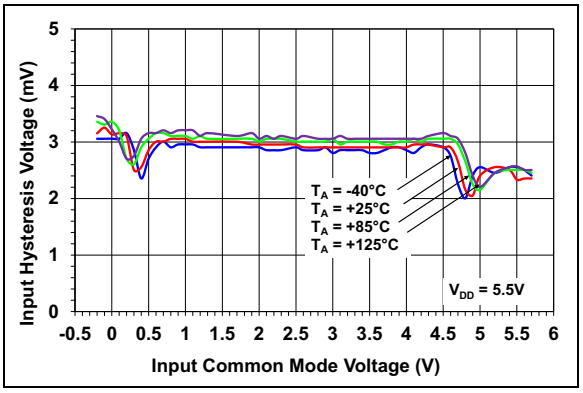


FIGURE 2-10: *Input Hysteresis Voltage vs. Common Mode Input Voltage (V_{DD} = 5.5V).*

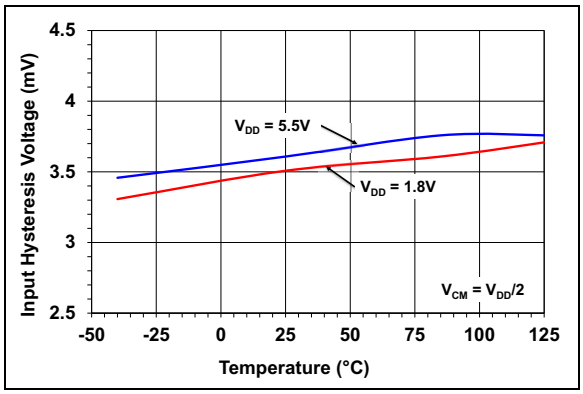


FIGURE 2-8: *Input Hysteresis Voltage vs. Ambient Temperature.*

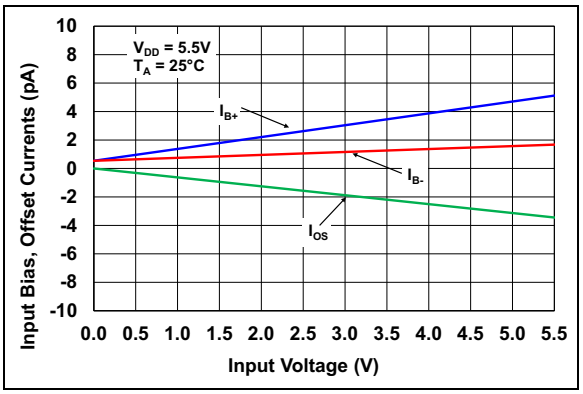


FIGURE 2-11: *Input Bias, Offset Current vs. Input Voltage.*

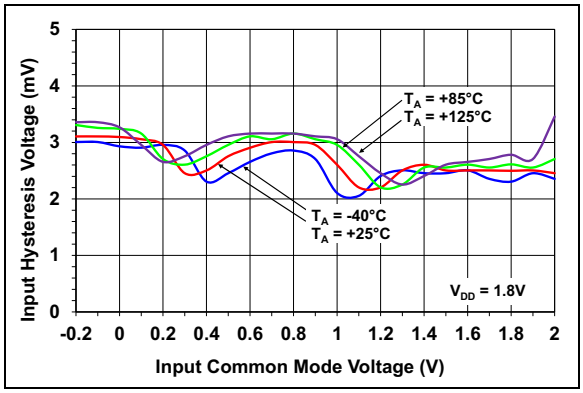


FIGURE 2-9: *Input Hysteresis Voltage vs. Common Mode Input Voltage (V_{DD} = 1.8V).*

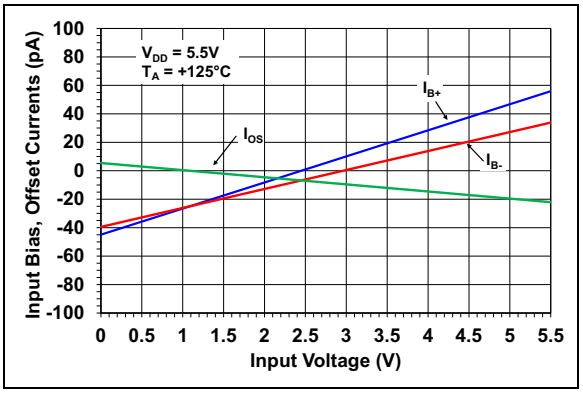


FIGURE 2-12: *Input Bias, Offset Current vs. Input Voltage (High Temp).*

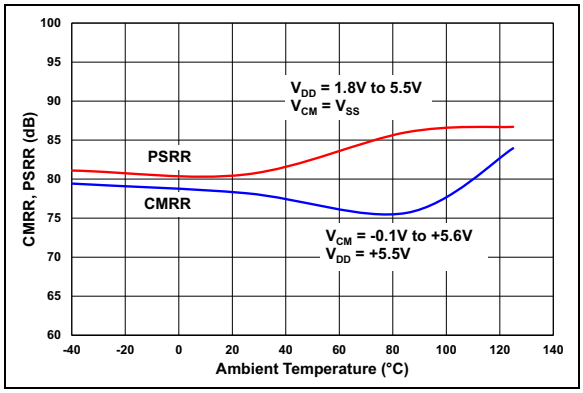


FIGURE 2-13: *CMRR, PSRR vs. Temperature.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.

2.2 Other DC Voltages and Currents

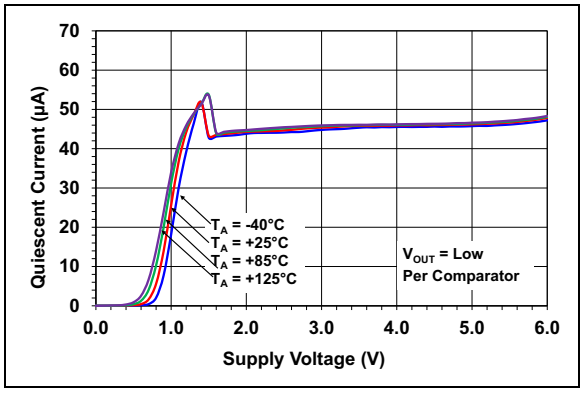


FIGURE 2-14: *Quiescent Current vs. Power Supply Voltage (Output Low).*

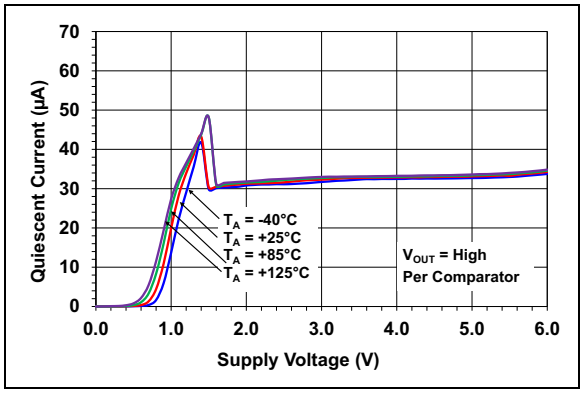


FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage (Output High).*

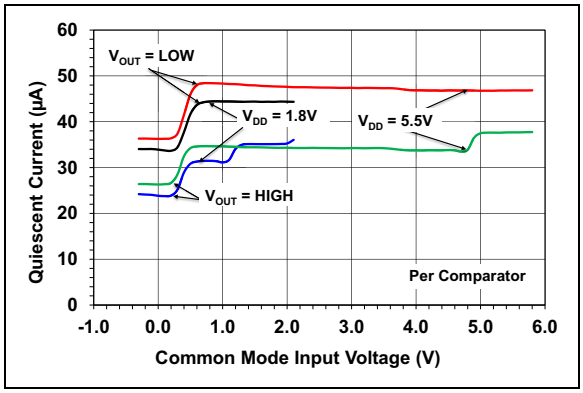


FIGURE 2-16: *Quiescent Current vs. Common Mode Input Voltage.*

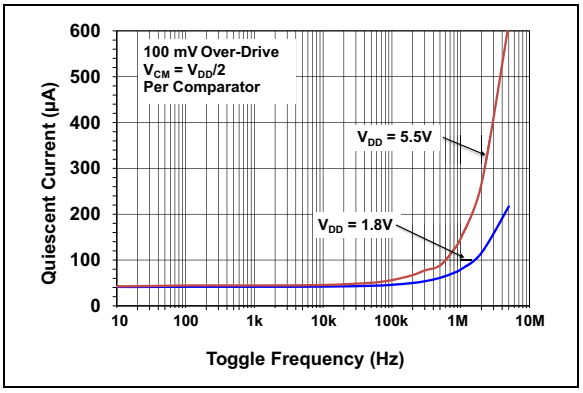


FIGURE 2-17: *Quiescent Current vs. Toggle Frequency.*

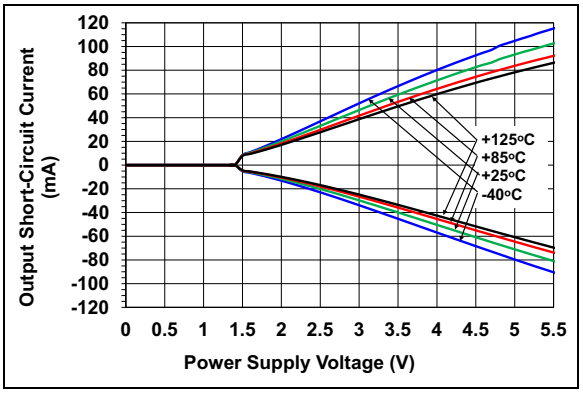


FIGURE 2-18: *Output Short-Circuit Current vs. Power Supply Voltage.*

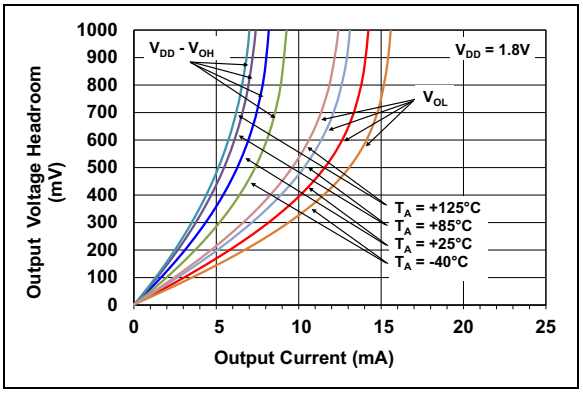


FIGURE 2-19: *Output Voltage Headroom vs. Output Current (V_{DD} = 1.8V).*

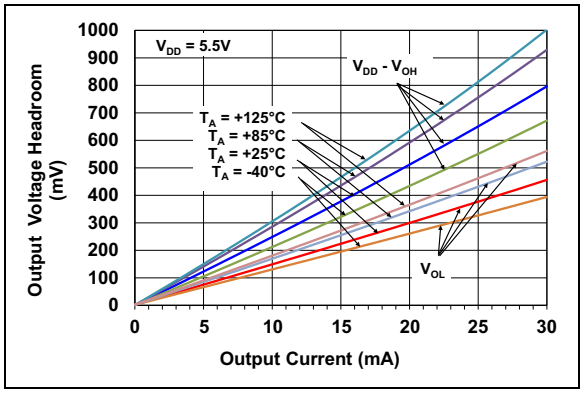


FIGURE 2-20: *Output Voltage Headroom vs. Output Current (V_{DD} = 5.5V).*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.

2.3 Time Response

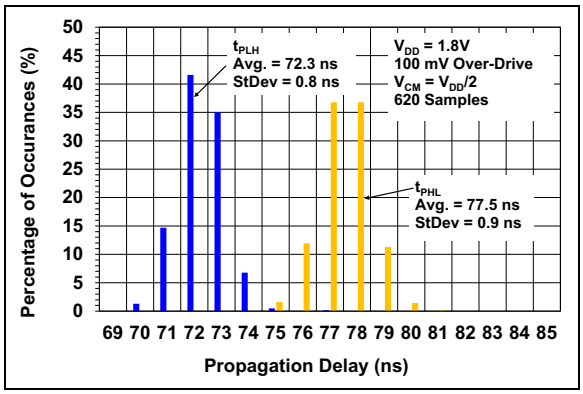


FIGURE 2-21: *High-to-Low and Low-to-High Propagation Delay Histogram (V_{DD} = 1.8V).*

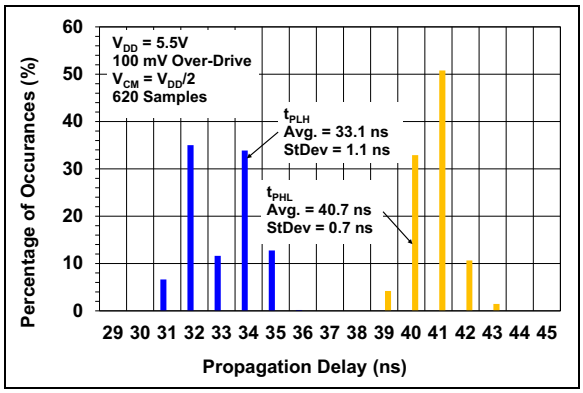


FIGURE 2-22: *High-to-Low and Low-to-High Propagation Delay Histogram (V_{DD} = 5.5V).*

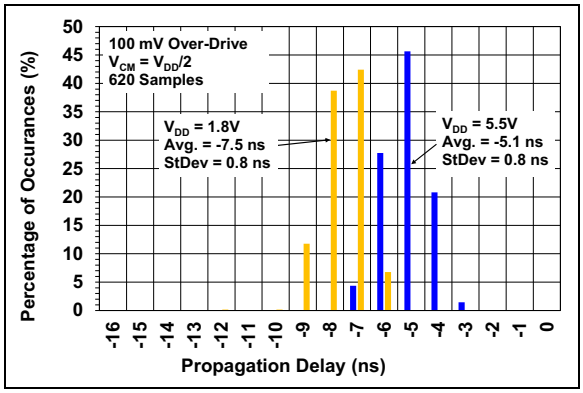


FIGURE 2-23: *Propagation Delay Skew Histogram.*

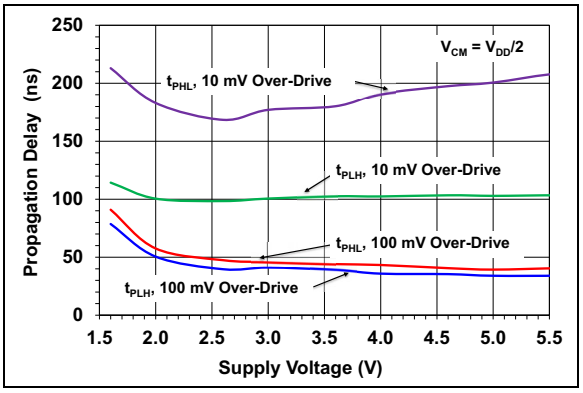


FIGURE 2-24: *Propagation Delay vs. Power Supply Voltage.*

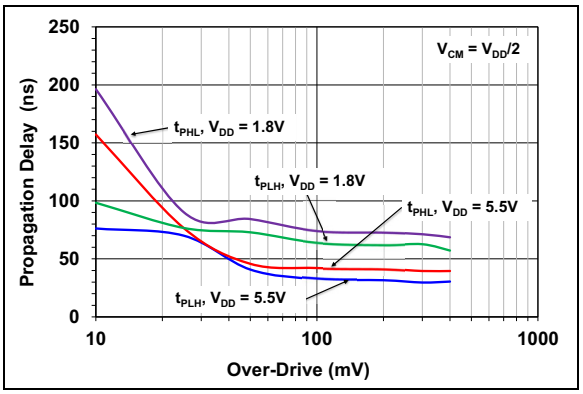


FIGURE 2-25: *Propagation Delay vs. Input Overdrive.*

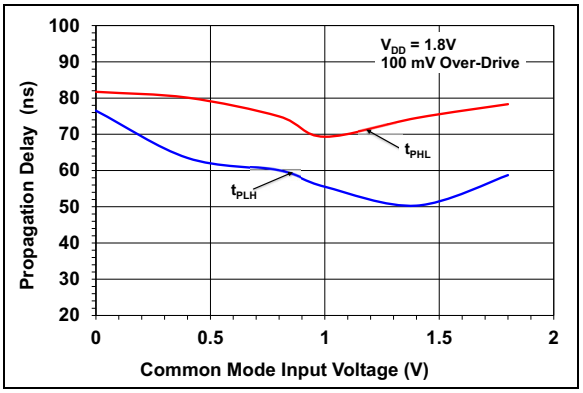


FIGURE 2-26: *Propagation Delay vs. Common Mode Input Voltage (V_{DD} = 1.8V).*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{IN-} = V_{DD}/2, V_{IN+} = V_{SS}, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 15 pF.

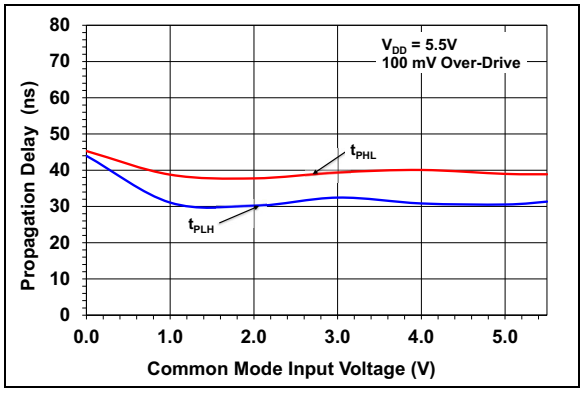


FIGURE 2-27: *Propagation Delay vs. Common Mode Input Voltage (V_{DD} = 5.5V).*

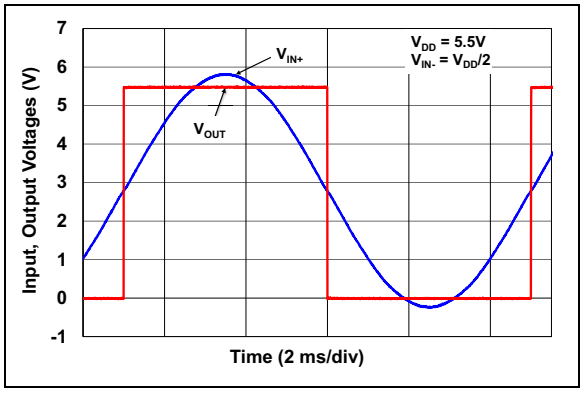


FIGURE 2-30: *Input and Output Signal, No Phase Reversal.*

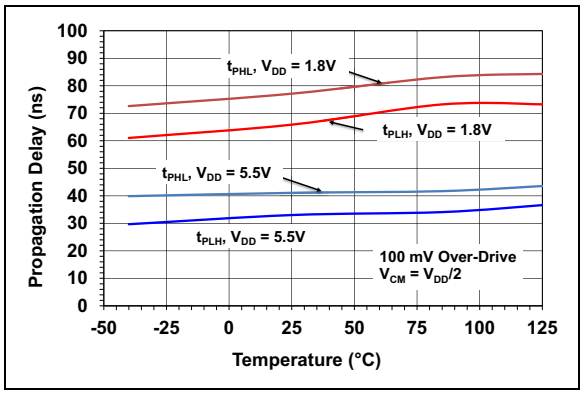


FIGURE 2-28: *Propagation Delay vs. Temperature.*

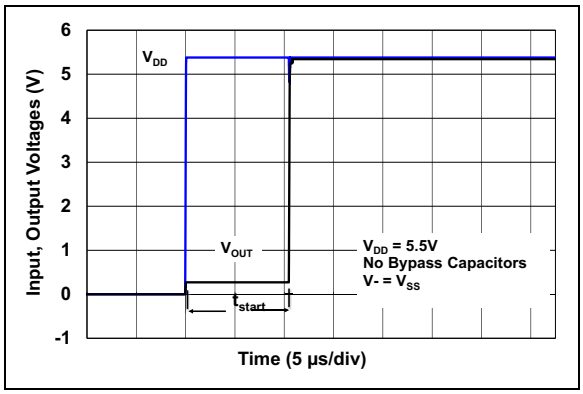


FIGURE 2-31: *Startup Time.*

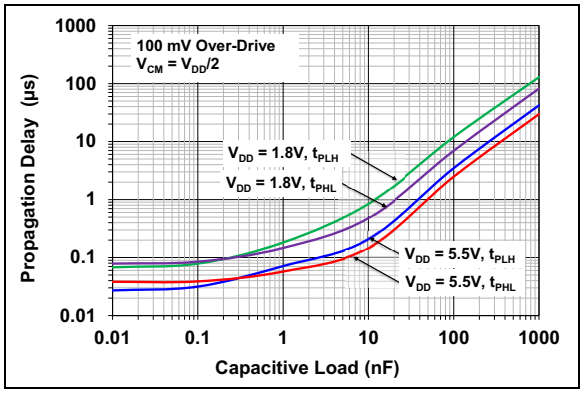


FIGURE 2-29: *Propagation Delay vs. Load Capacitance.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1, Table 3-2, and Table 3-3.

TABLE 3-1: PIN FUNCTION TABLE - SINGLES

MCP6571	MCP6571R	MCP6571U	Symbol	Description
5-Lead SC70, SOT-23	5-Lead SOT-23	5-Lead SC70, SOT-23		
1	1	4	V_{OUT}	Digital Output
2	5	2	V_{SS}	Negative Power Supply
3	3	1	$V_{IN}+$	Noninverting Input
4	4	3	$V_{IN}-$	Inverting Input
5	2	5	V_{DD}	Positive Power Supply

TABLE 3-2: PIN FUNCTION TABLE - DUALS

MCP6572	Symbol	Description
8-Lead MSOP, SOIC		
1	V_{OUTA}	Digital Output; Comparator A
2	$V_{INA}-$	Inverting Input; Comparator A
3	$V_{INA}+$	Noninverting Input; Comparator A
4	V_{SS}	Negative Power Supply
5	$V_{INB}+$	Noninverting Input; Comparator B
6	$V_{INB}-$	Inverting Input; Comparator B
7	V_{OUTB}	Digital Output; Comparator B
8	V_{DD}	Positive Power Supply

TABLE 3-3: PIN FUNCTION TABLE - QUADS

MCP6574	Symbol	Description
14-Lead TSSOP, SOIC		
1	V_{OUTA}	Digital Output; Comparator A
2	$V_{INA}-$	Inverting Input; Comparator A
3	$V_{INA}+$	Noninverting Input; Comparator A
4	V_{DD}	Positive Power Supply
5	$V_{INB}+$	Noninverting Input; Comparator B
6	$V_{INB}-$	Inverting Input; Comparator B
7	V_{OUTB}	Digital Output; Comparator B
8	V_{OUTC}	Digital Output; Comparator C
9	$V_{INC}-$	Inverting Input; Comparator C
10	$V_{INC}+$	Noninverting Input; Comparator C
11	V_{SS}	Negative Power Supply
12	$V_{IND}+$	Noninverting Input; Comparator D
13	$V_{IND}-$	Inverting Input; Comparator D
14	V_{OUTD}	Digital Output; Comparator D

3.1 Digital Outputs

The comparator outputs (V_{OUTx}) are CMOS push-pull, digital outputs. They are designed to be compatible with CMOS and TTL logic, and are capable of driving heavy DC or capacitive loads.

3.2 Analog Inputs

The comparator noninverting and inverting inputs (V_{INx}+, V_{INx}-) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{SS}, V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These pins can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

4.0 APPLICATION INFORMATION

The MCP6571/1R/1U/2/4 is a family of push-pull output comparators. They are suitable for a wide range of high-speed applications requiring low power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The MCP6571/1R/1U/2/4 devices have internally set hysteresis, VHYST, that is small enough to maintain input offset accuracy across the entire input common mode range and large enough to eliminate output chattering caused by the comparator's own input noise voltage, ENI. Figure 4-1 shows the output voltage with a 100 mV ramping input voltage (V_{IN+}) across the reference voltage (V_{IN-}), while Figure 4-2 has a smaller voltage scale to better show the different trigger points on the input voltage.

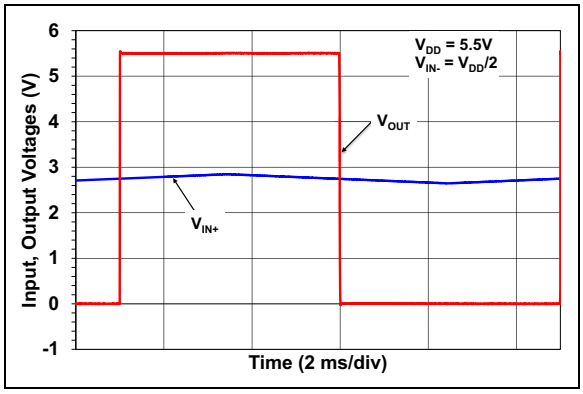


FIGURE 4-1: *Input Voltage Hysteresis.*

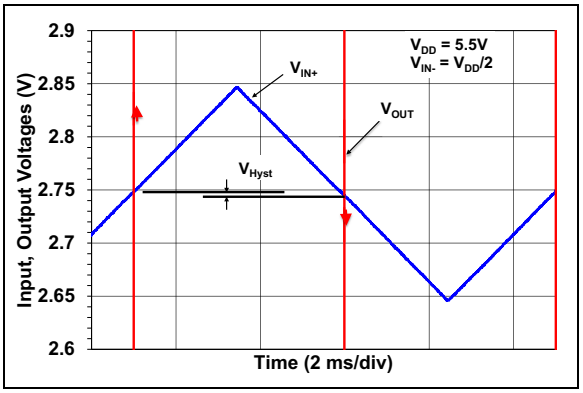


FIGURE 4-2: *Input Voltage Hysteresis (Smaller Voltage Scale).*

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of the comparator, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings†**).

The Electrostatic Discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-3. This structure was chosen to protect the input transistors against many, but not all, overvoltage conditions and to minimize the Input Bias (I_B) current.

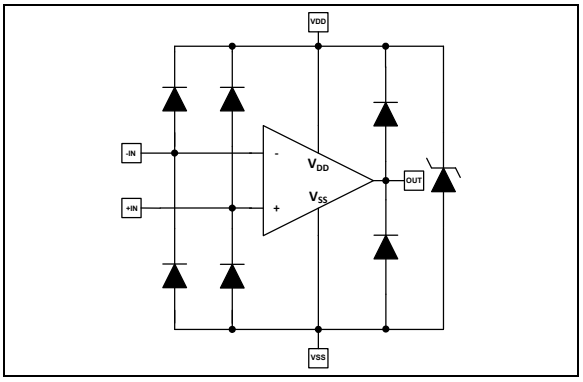


FIGURE 4-3: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}; their breakdown voltage is high enough to allow normal operation. At 0.5V above V_{DD} or below V_{SS}, the input currents are typically less than 5 mA. Very fast ESD events that meet the specifications are limited so that damage does not occur.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of the comparator, the circuit must limit the currents into the input pins (see **Section 1.1, Absolute Maximum Ratings†**).

Figure 4-4 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins through the ESD diodes to either V_{DD} or V_{SS}.

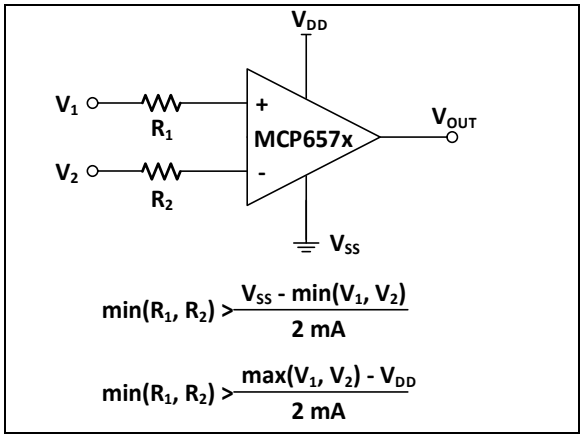


FIGURE 4-4: *Protecting the Analog Inputs.*

4.1.4 PHASE REVERSAL

The MCP6571/1R/1U/2/4 comparator use CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-30 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.1.5 POWER-ON RESET (POR)

The MCP6571/2/4 comparator family is provided with a Power-on Reset (POR) circuit which sets the output to high impedance until the supply voltage (V_{DD}) exceeds the POR threshold. When the supply voltage exceeds the POR threshold, the output will drive to the correct state determined by the input pins. Figure 4-5 shows a typical output voltage waveform with a rising supply voltage (V_{DD}). This plot indicates the output is enabled after V_{DD} exceeds 1.45V. Figure 4-6 shows the output voltage waveform for the same part when the supply voltage is decreasing. This plot indicates that the output is disabled when V_{DD} falls below 1.36V.

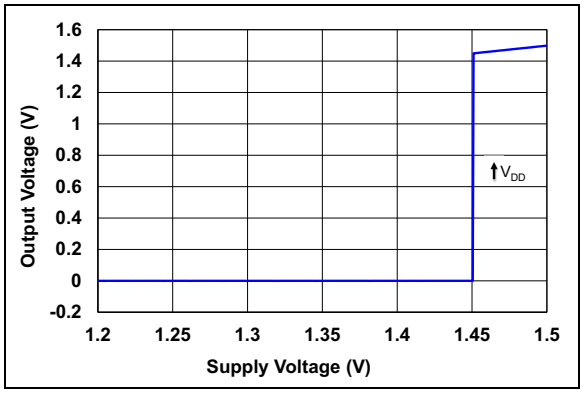


FIGURE 4-5: *POR with Rising Supply Voltage (typical).*

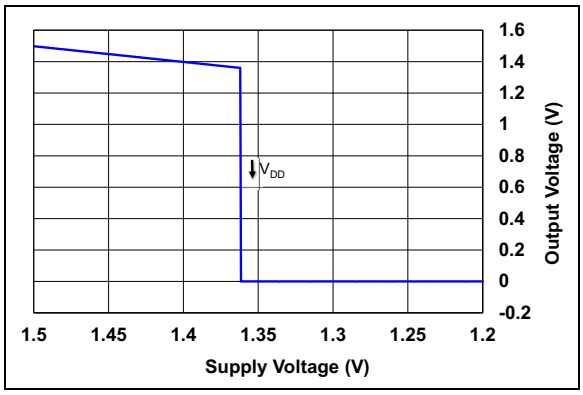


FIGURE 4-6: *POR with Falling Supply Voltage (typical).*

4.2 Push-Pull Output

The push-pull output is designed to be compatible with both CMOS and TTL logic, while the output transistors are configured to give rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply to supply) when the output is transitioned from high-to-low or from low-to-high. Refer to Figures 2-19 and 2-20 for more information.

4.3 Externally Set Hysteresis

The MCP6571/1R/1U/2/4 family of comparators are provided with a small internal hysteresis voltage between the rising and falling trigger levels. Larger levels of hysteresis can be achieved by using external resistors.

The input offset voltage (V_{OS}) is the center (or average) of the input-referred low to high and high to low trip points. Where as the input hysteresis voltage (V_{HYST}) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other and thus reduces dynamic supply current.

4.3.1 NONINVERTING CIRCUIT

Figure 4-7 shows a noninverting circuit for single supply applications using just two external resistors. The resulting hysteresis diagram is shown in Figure 4-8. The trip points (V_{TLH} and V_{THL}) can be determined by Equation 4-1.

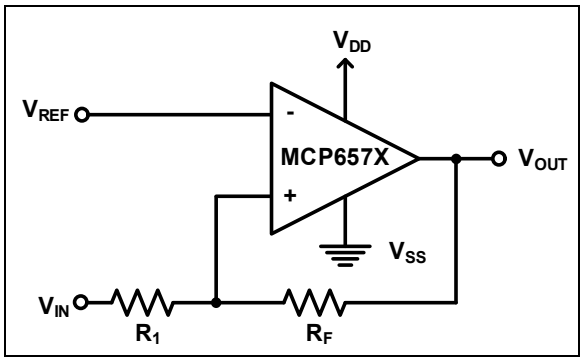


FIGURE 4-7: *Noninverting Circuit with Hysteresis.*

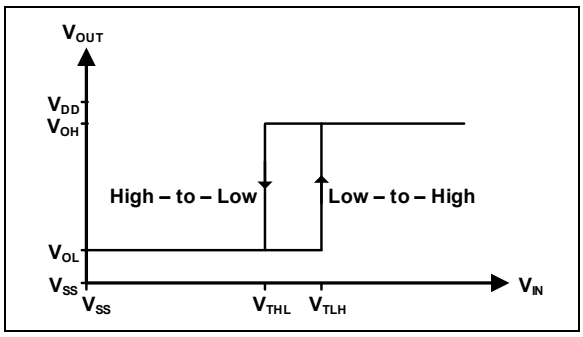


FIGURE 4-8: *Hysteresis Diagram for Noninverting circuit.*

EQUATION 4-1:

$$V_{TLH} = V_{REF}\left(1+\frac{R_1}{R_F}\right) - V_{OL}\left(\frac{R_1}{R_F}\right)$$

$$V_{THL} = V_{REF}\left(1+\frac{R_1}{R_F}\right) - V_{OH}\left(\frac{R_1}{R_F}\right)$$

Where:

V_{TLH} = Trip Voltage from Low-to-High

V_{THL} = Trip Voltage from High-to-Low

4.3.2 INVERTING CIRCUIT

Figure 4-9 shows an inverting circuit for single supply applications using three external resistors. The resulting hysteresis diagram is shown in Figure 4-10. The trip points (V_{TLH} and V_{THL}) can be determined by Equation 4-3.

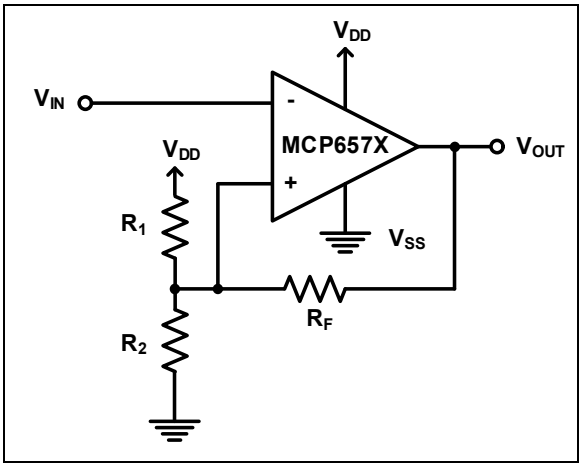


FIGURE 4-9: *Inverting Circuit with Hysteresis.*

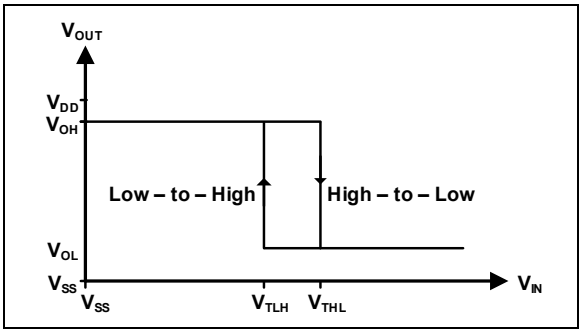


FIGURE 4-10: *Hysteresis Diagram for Inverting circuit.*

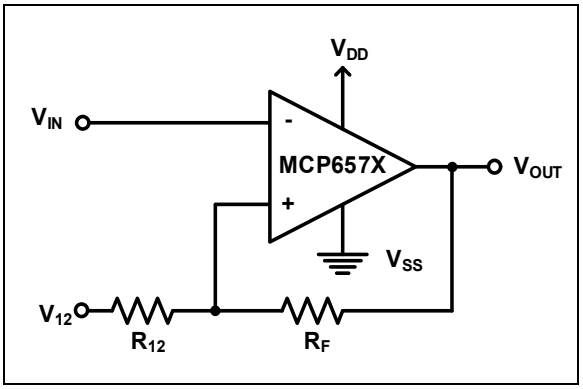


FIGURE 4-11: *Thevenin Equivalent Circuit.*

Where R_{12} and V_{12} can be calculated as shown in Equation 4-2, and the trip points (V_{TLH} and V_{THL}) can be determined by Equation 4-3.

EQUATION 4-2:

$$R_{12} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{12} = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

EQUATION 4-3:

$$V_{THL} = V_{OH}\left(\frac{R_{12}}{R_{12} + R_F}\right) + V_{12}\left(\frac{R_F}{R_{12} + R_F}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{12}}{R_{12} + R_F}\right) + V_{12}\left(\frac{R_F}{R_{12} + R_F}\right)$$

Where:

V_{TLH} = Trip Voltage from Low-to-High

V_{THL} = Trip Voltage from High-to-Low

4.4 Start-up

The MCP6571/1R/1U/2/4 family of parts quickly controls the output when power (V_{DD}) is initially applied to the device (start-up). Bypass capacitors are removed during the start-up testing to minimize the inrush currents (see Figure 4-12). The start-up time is measured from when V_{DD} is applied to when the output toggles high.

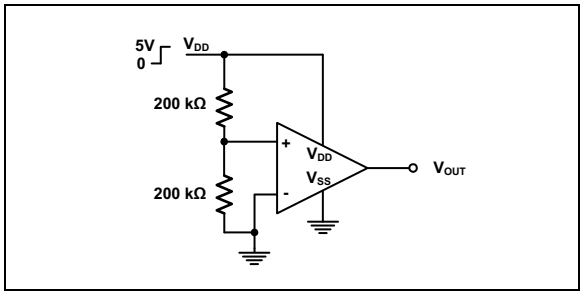


FIGURE 4-12: *Start-Up Test Circuit.*

Figure 4-13 shows the power supply voltage (blue line) for the MCP6572 and the output voltage (black line). When power is first applied to the MCP6572, the output is turned off (Point A) and is high impedance until VPOR is exceeded. After 11 µs (typical), the output is turned on (Point B) and V_{OUT} toggles high.

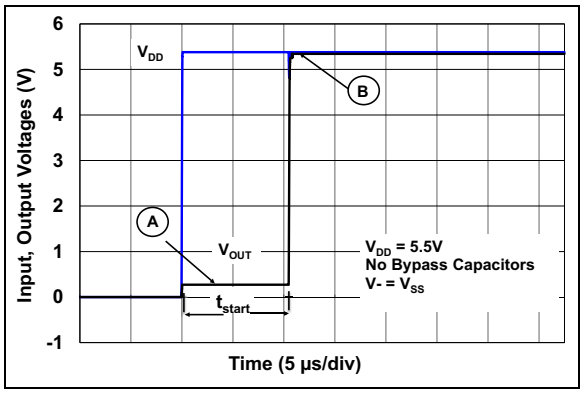


FIGURE 4-13: *Start-Up Test Waveforms.*

4.5 Capacitive Loads

This family of comparators has a push-pull output. When the output switches there can be an increase in output sinking or sourcing current during the transition. Excessive capacitive loads can increase the supply current and propagation delay or decrease slew rate during the output transitions.

Figure 2-29 shows the increase in propagation delay with an increase in output capacitance. Figure 2-17 shows the increase in quiescent current with the increase in toggle frequency (rate of transitions from low-to-high, high-to-low).

4.6 Supply Bypass

The MCP6571/1R/1U/2/4 family of comparators power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

4.7 PCB Surface Leakage

In applications where low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6571/1R/1U/2/4's bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-14.

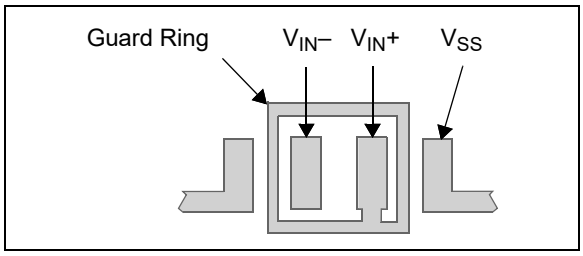


FIGURE 4-14: *Example Guard Ring Layout for Inverting Gain.*

1. Inverting Configuration (Fig and Figure 4-14)
   a) Connect the guard ring to the noninverting pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g. $V_{DD}/2$ or ground).
   b) Connect the inverting input pin (V_{IN}–) to the input pad without touching the guard ring.
2. Noninverting Configuration (Figure 4-7)
   a) Connect the noninverting input pin (V_{IN}+) to the input pad without touching the guard ring.
   b) Connect the guard ring to the inverting pin (V_{IN}-).

4.8 Unused Comparators

An unused comparator in a dual (MCP6572) or quad (MCP6574) package should be configured as shown in Figure 4-15. These circuits prevent the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current.

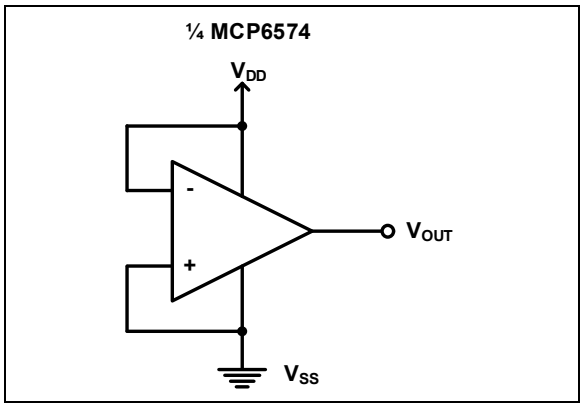


FIGURE 4-15: *Unused Comparators.*

4.9 Application Circuits

4.9.1 WINDOW COMPARATOR

The MCP6571/2/4 comparator can be used to create a windowed comparator. Figure 4-16 shows one approach using the MCP6572 dual comparator with an AND gate. The AND gate output will produce a logic high when the input voltage is between V_{LO} and V_{HI} ($V_{HI} > V_{LO}$).

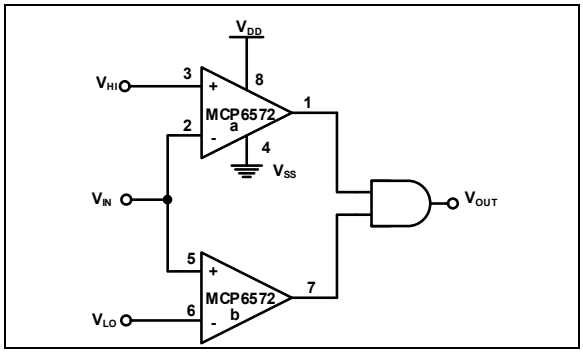


FIGURE 4-16: *Windowed Comparator.*

4.9.2 BISTABLE MULTIVIBRATOR

A simple bistable multivibrator design is shown in Figure 4-17. V_{REF} needs to be between the power supplies (V_{SS} = GND and V_{DD}) to achieve oscillation. The output duty cycle changes with V_{REF}.

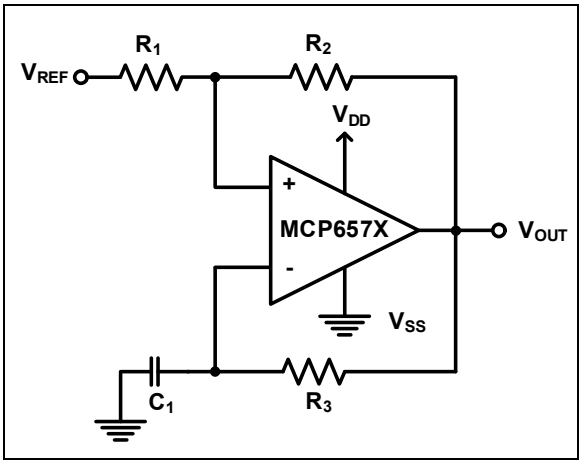


FIGURE 4-17: *Bistable Multivibrator.*

5.0 DESIGN AIDS

Microchip Technology Inc. provides the basic design tools needed for the MCP6571/1R/1U/2/4 comparator.

5.1 SPICE Macro Model

The latest SPICE macro model for the comparator MCP6571/1R/1U/2/4 is available on the Microchip website at www.microchip.com. This model is intended to be an initial design tool that works well in the comparator's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analog tools..

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 2 (P/N DS51668)
- MCP6XXX Amplifier Evaluation Board 3 (P/N DS51673)
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board (P/N SOIC8EV)
- 5/6-Pin SOT-23 Evaluation Board (P/N VSUPEV2)
- 14-Pin SOIC/TSSOP/DIP Evaluation Board (P/N SOIC14EV)

5.3 Application Notes

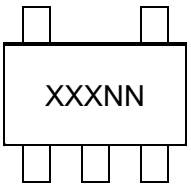
The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **AN895 –** *"Oscillator Circuits For RTD Temperature Sensors",* DS00895

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

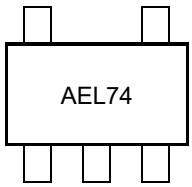
5-Lead SC70 (**MCP6571/1U**)



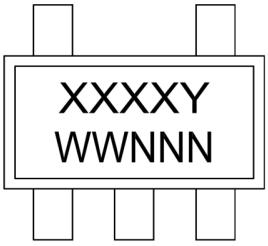
Device	Marking
MCP6571	AELNN
MCP6571U	AEMNN

Note: Applies to 5-Lead SC-70.

Example:



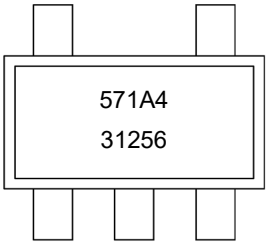
5-Lead SOT-23 (**MCP6571/1U/1R**)



Device	Marking
MCP6571	571AY
MCP6571U	571UY
MCP6571R	571RY

Note: Applies to 5-Lead SOT-23.

Example:

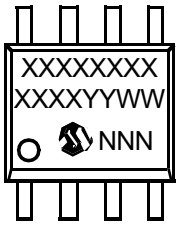


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

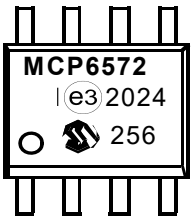
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

8-Lead SOIC (150 mil) **(MCP6572)**



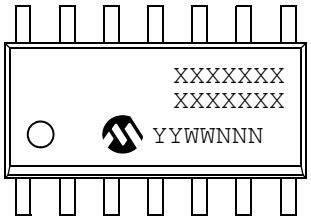
Example:



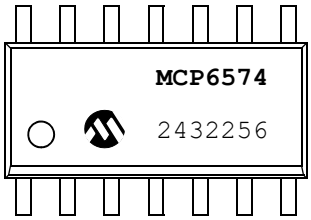
8-Lead MSOP

Example:

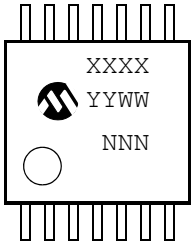
14-Lead SOIC (150 mil) (**MCP6574**)



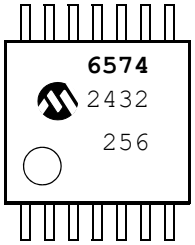
Example:



14-Lead TSSOP (**MCP6574**)

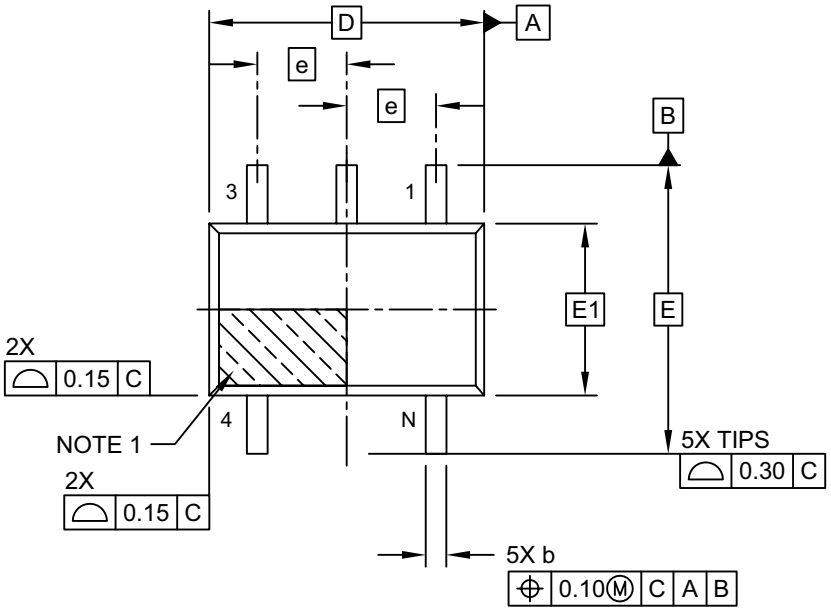


Example:

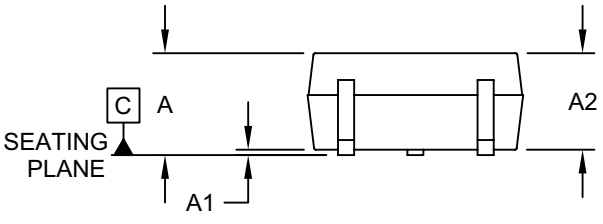


5-Lead Plastic Small Outline Transistor (LTY) [SC70]

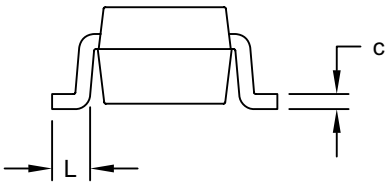
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

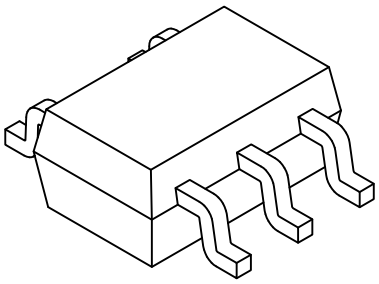


END VIEW

Microchip Technology Drawing C04-061-LTY Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D		2.00 BSC	
Overall Width	E		2.10 BSC	
Molded Package Width	E1		1.25 BSC	
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

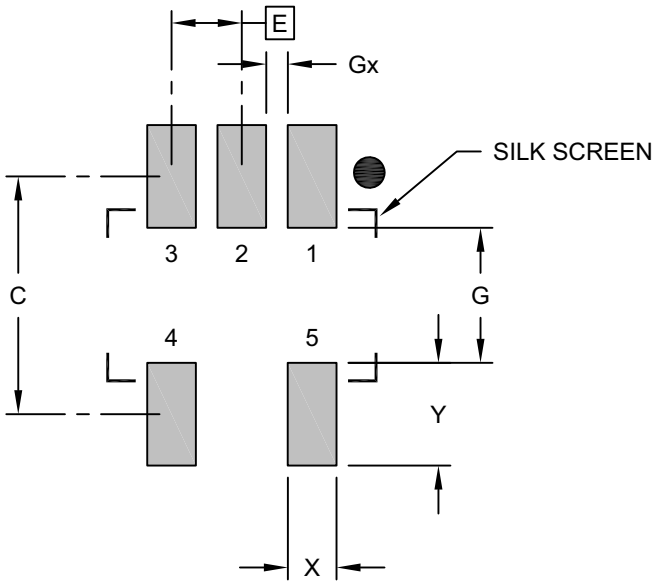
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LTY Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

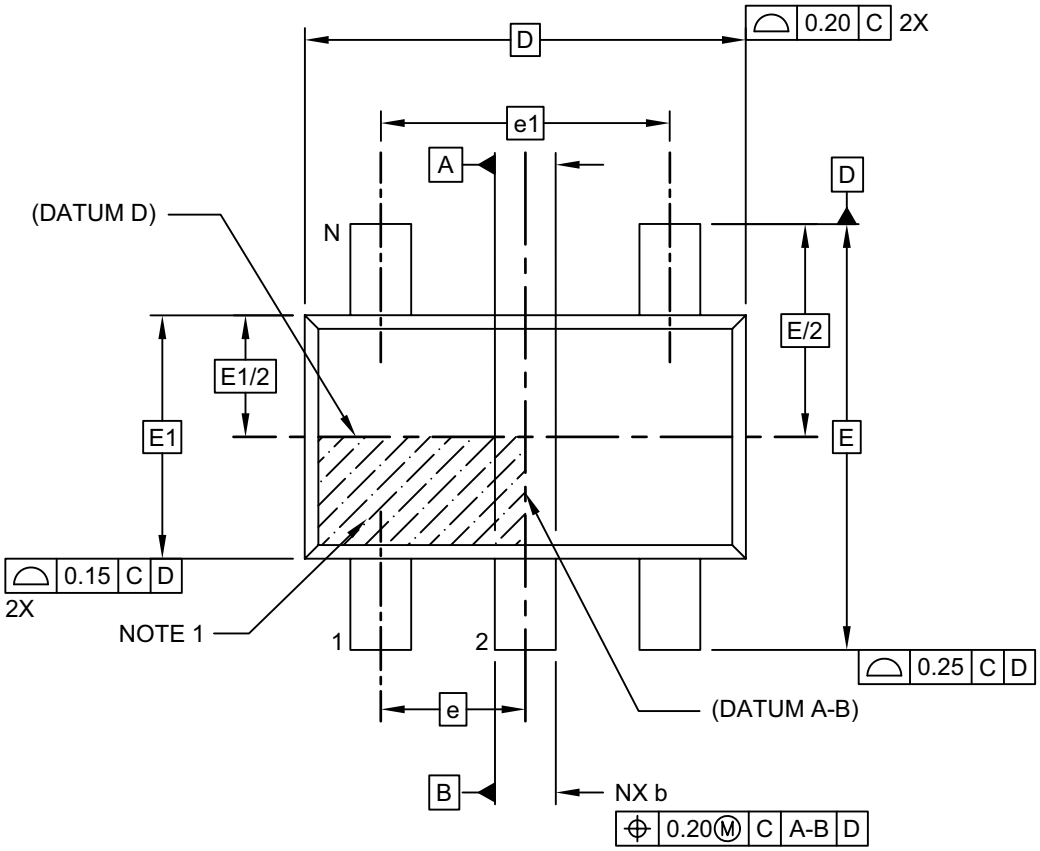
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

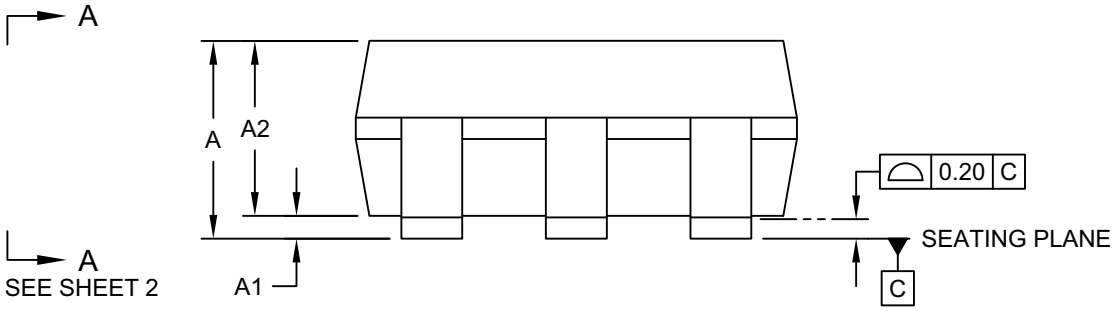
Microchip Technology Drawing No. C04-2061-LTY Rev E

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

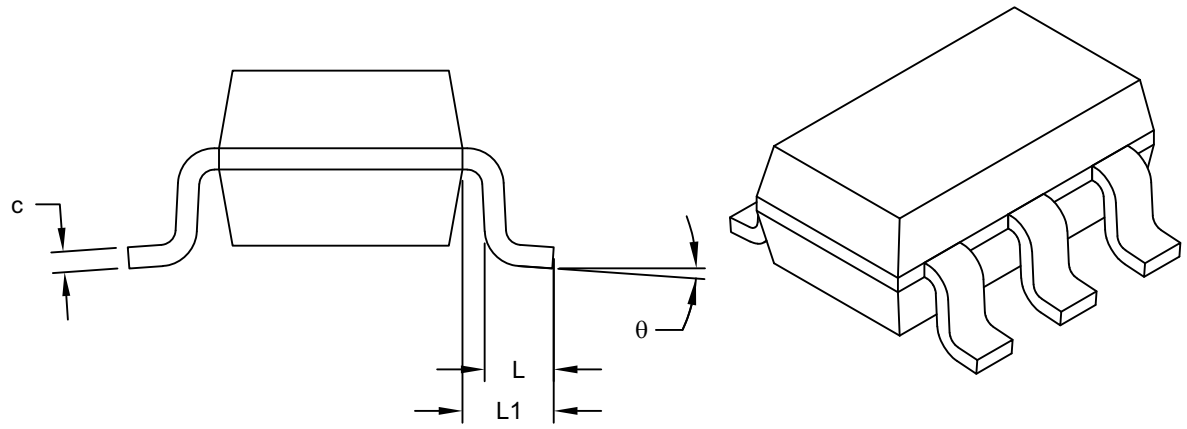


SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.95 BSC	
Outside lead pitch	e1		1.90 BSC	
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E		2.80 BSC	
Molded Package Width	E1		1.60 BSC	
Overall Length	D		2.90 BSC	
Foot Length	L	0.30	-	0.60
Footprint	L1		0.60 REF	
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

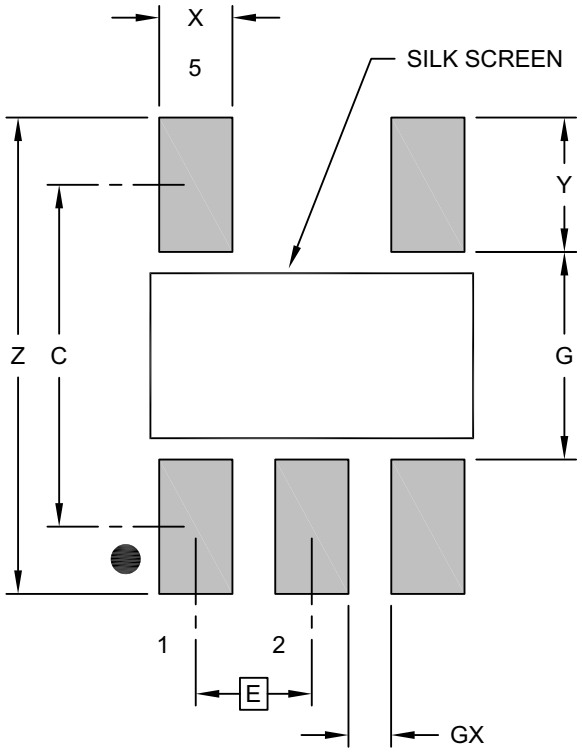
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

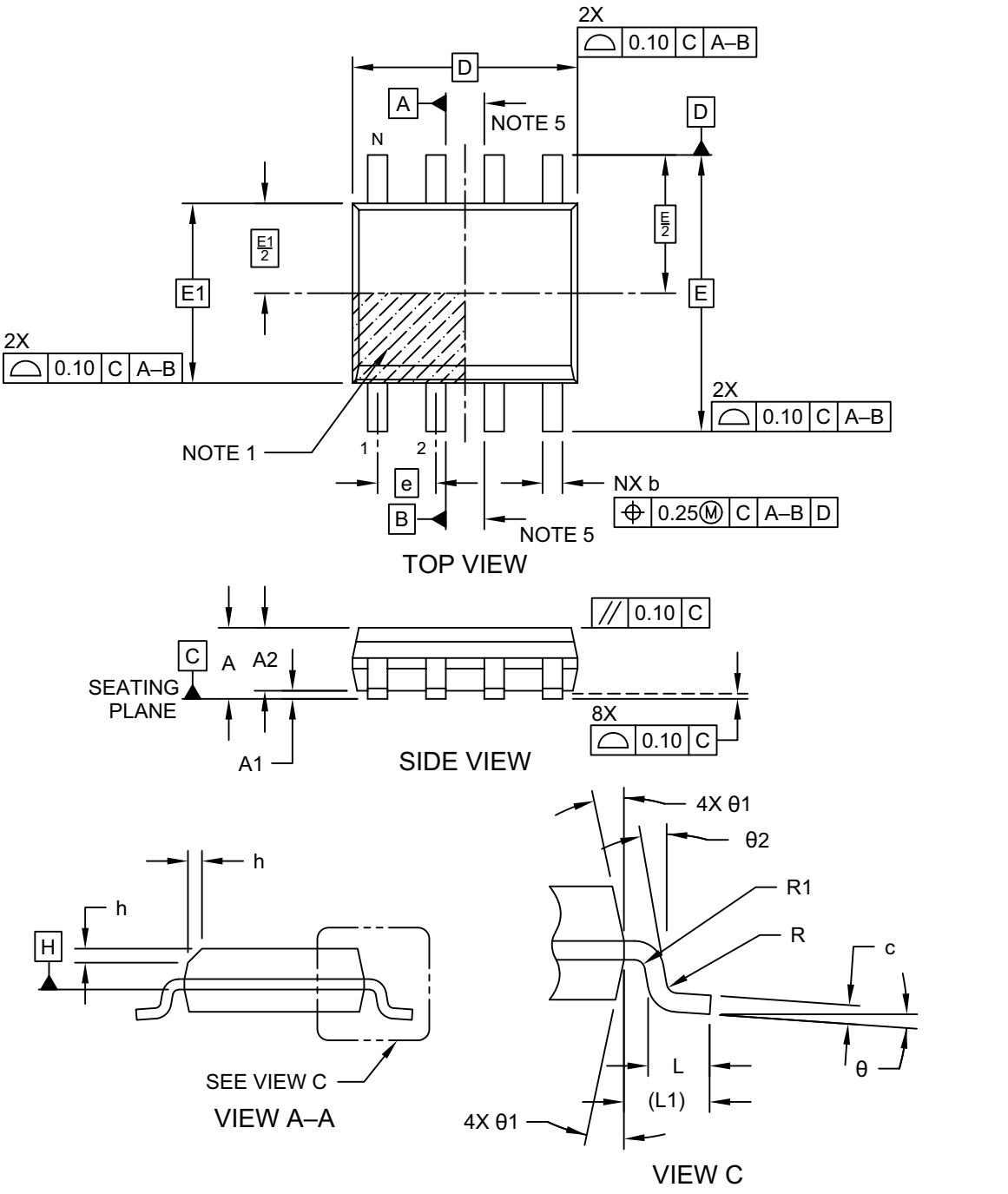
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev H

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

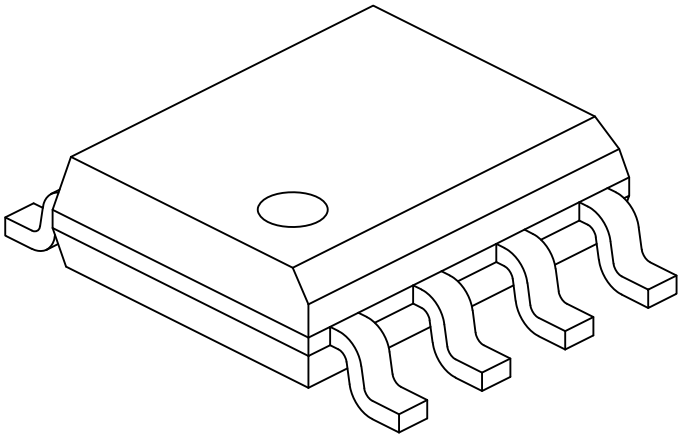
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

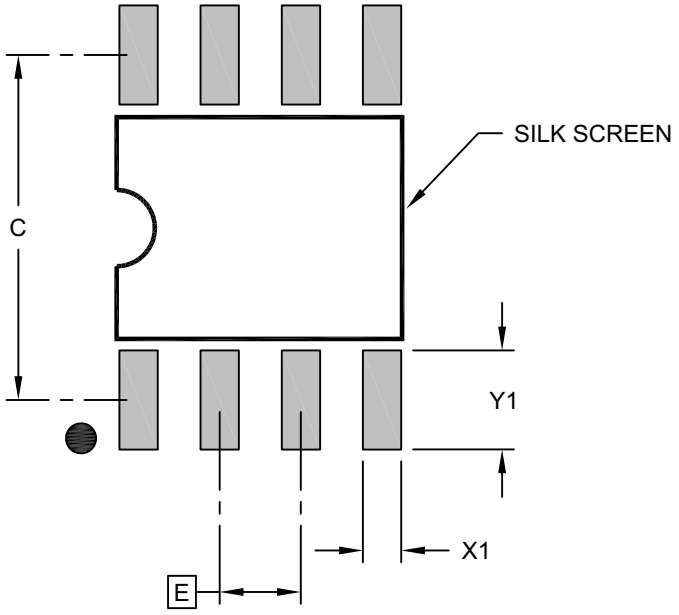
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

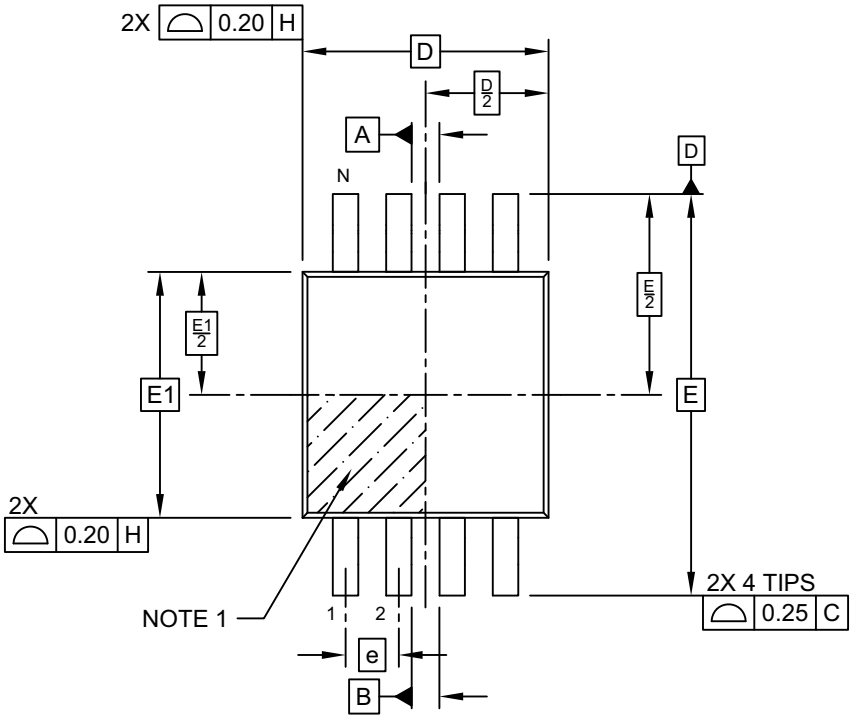
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

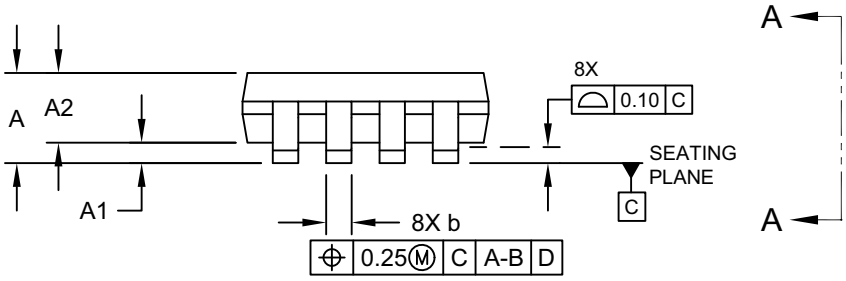
Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

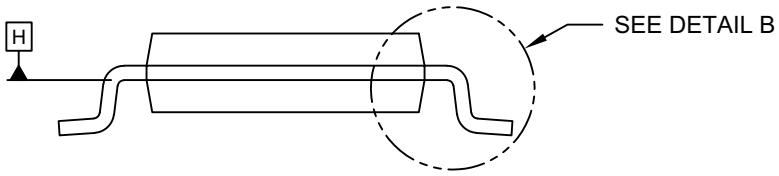
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

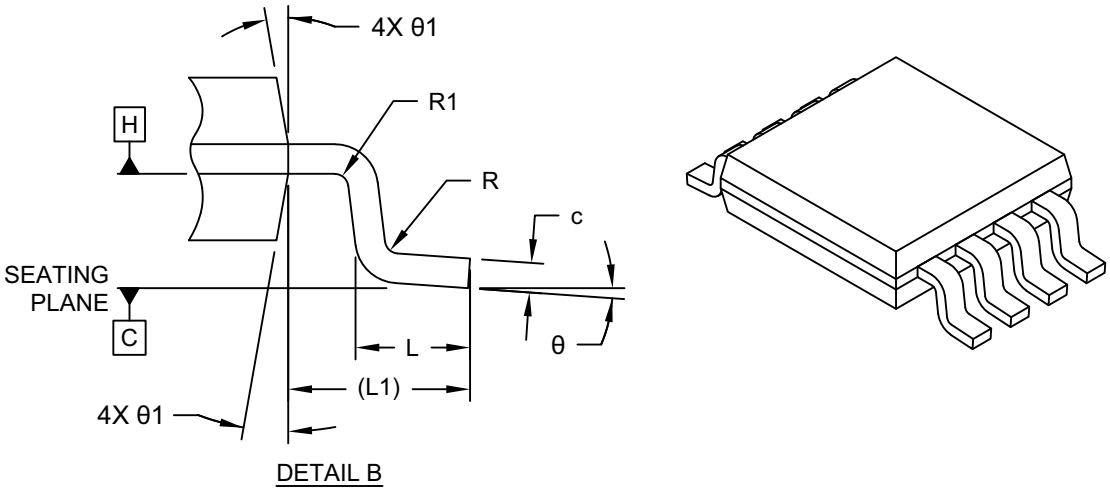


VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

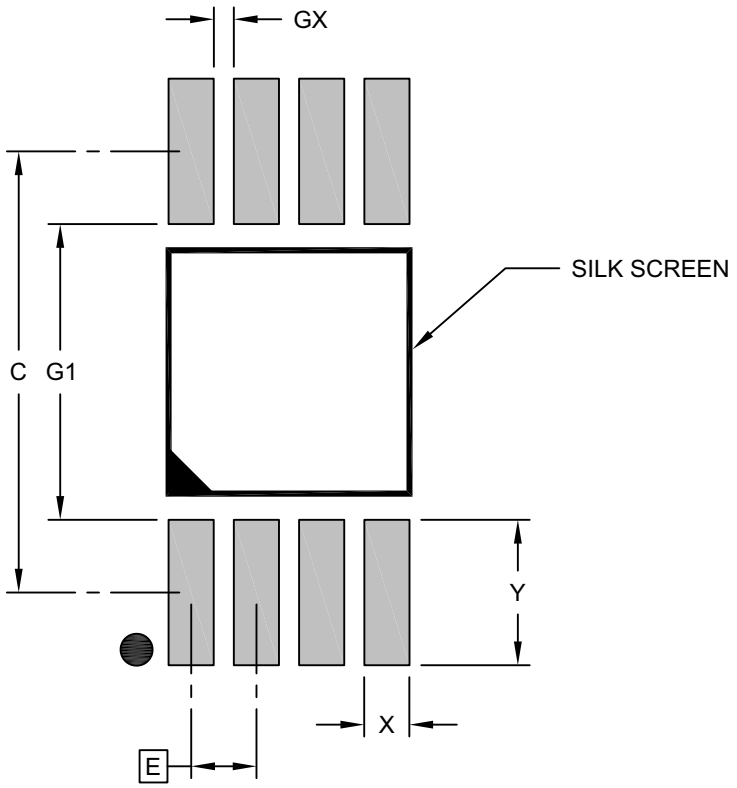
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

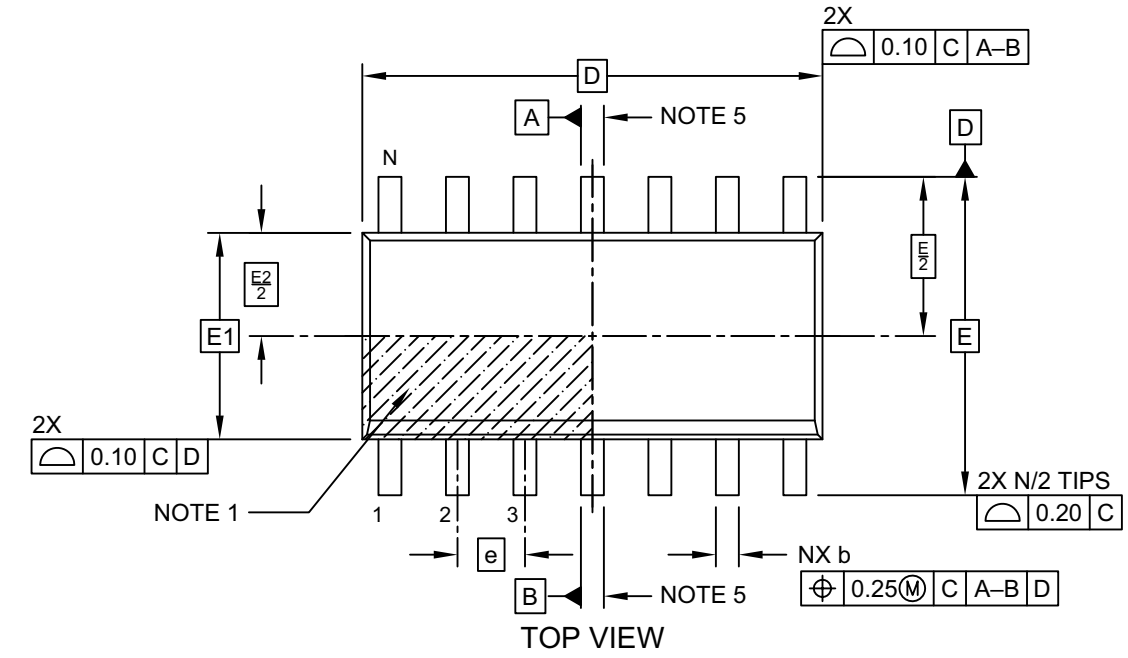
Notes:

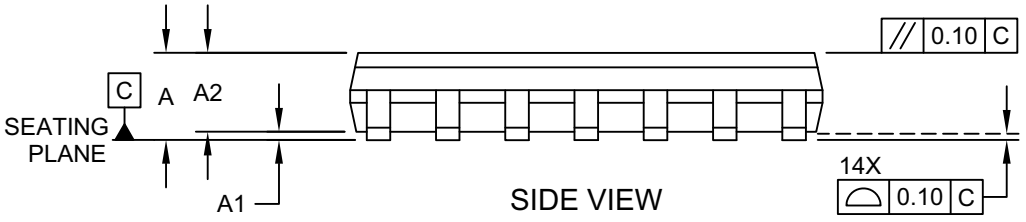
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

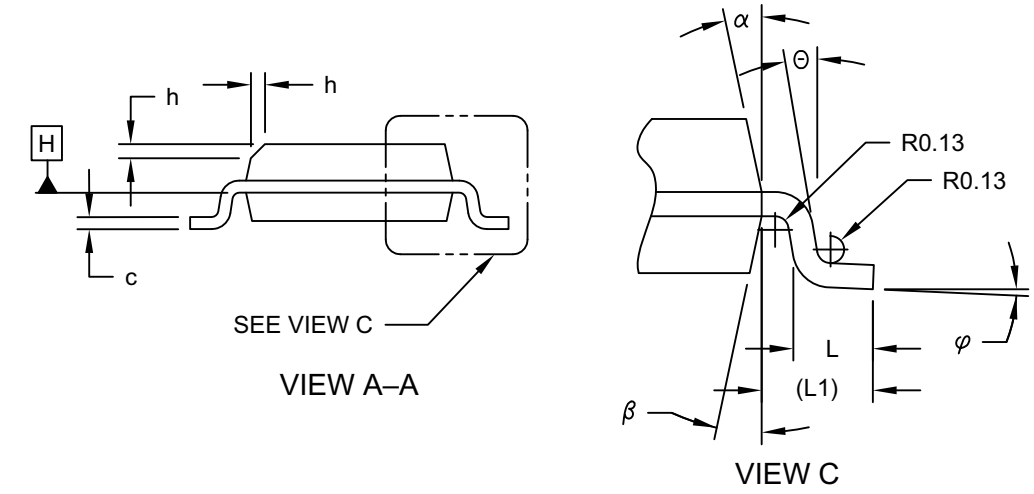
Microchip Technology Drawing C04-2111-MS Rev F

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



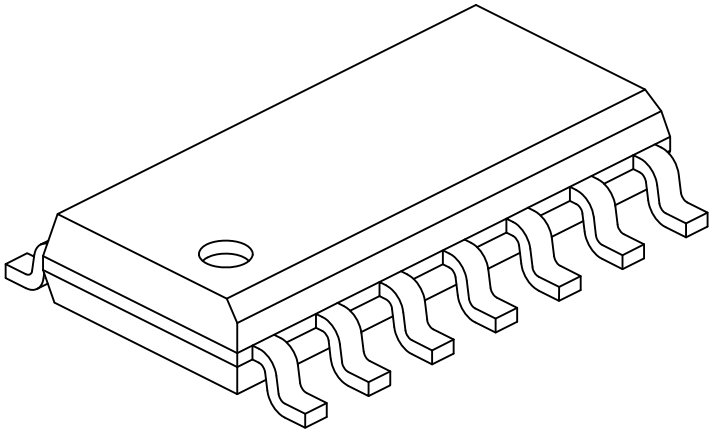




Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

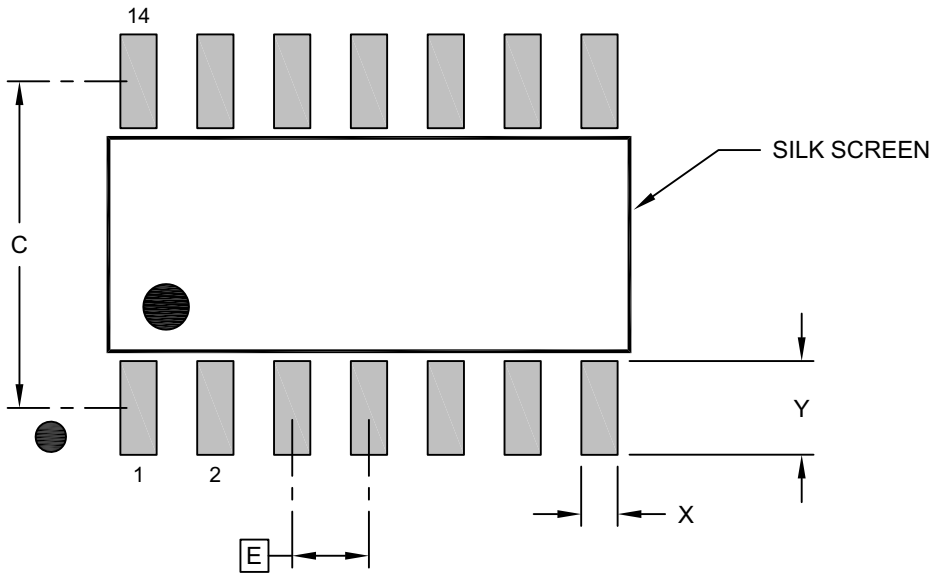
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

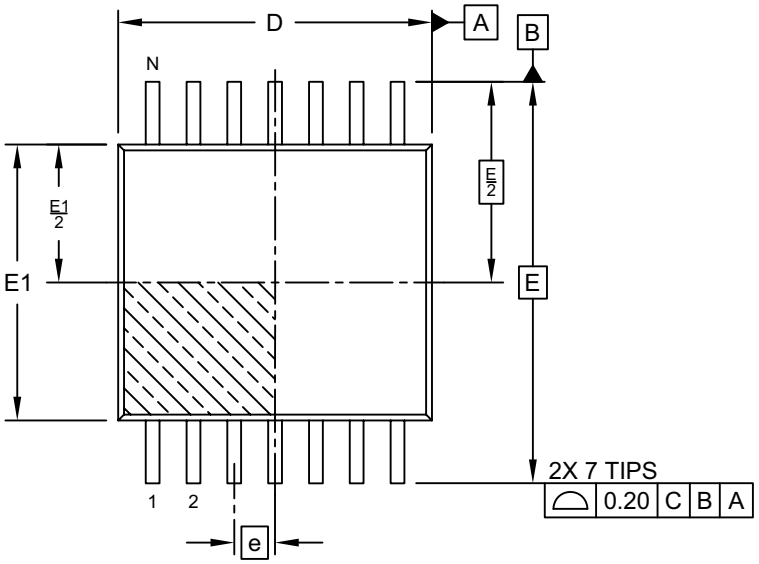
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

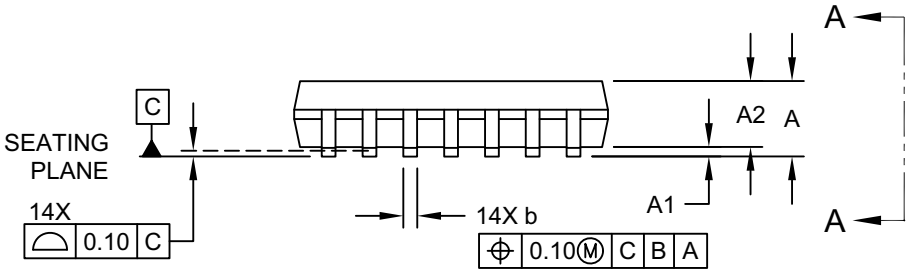
Microchip Technology Drawing No. C04-2065-SL Rev D

14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

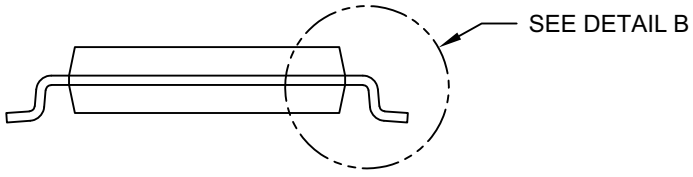
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

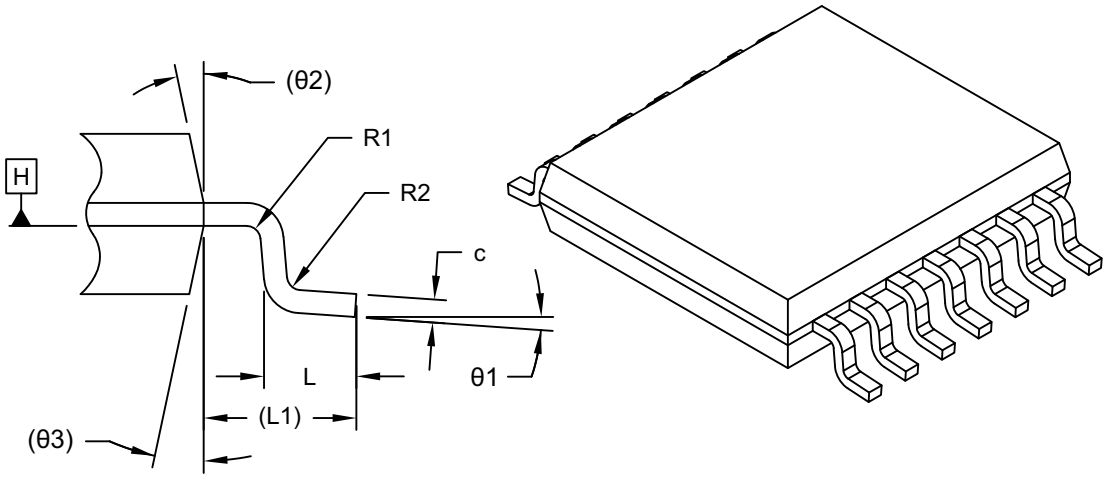


VIEW A–A

Microchip Technology Drawing C04-087-ST Rev F Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

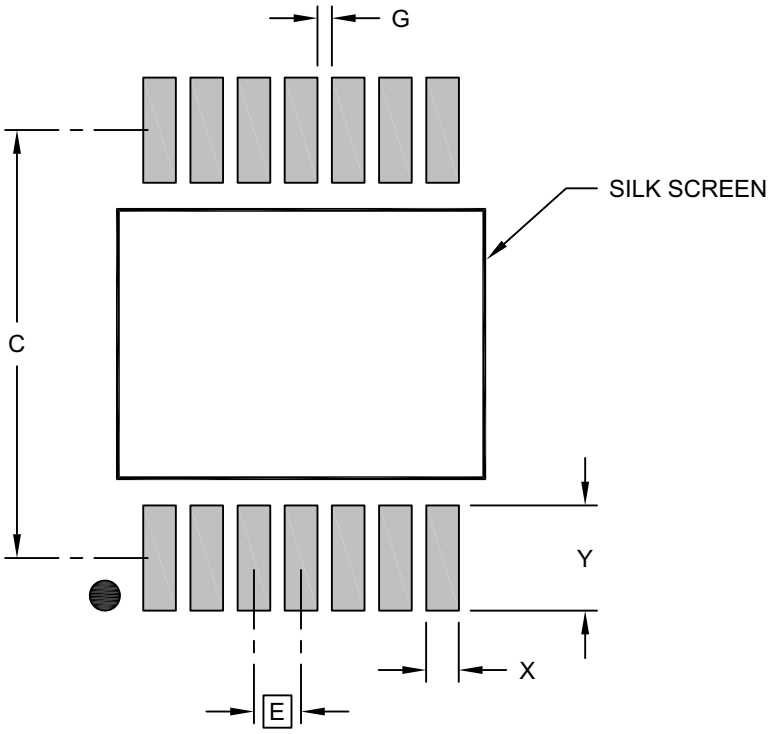
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087-ST Rev F Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline Package [ST] – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X14)	X			0.45
Contact Pad Length (X14)	Y			1.45
Contact Pad to Contact Pad (X12)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087-ST Rev F

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2025)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XX	XXX(2)
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:

MCP6571T	Single Comparator (Tape and Reel) (SC-70, SOT-23)
MCP6571RT	Single Comparator (Tape and Reel) (SOT-23)
MCP6571UT	Single Comparator (Tape and Reel) (SC-70, SOT-23)
MCP6572T	Dual Comparator (Tape and Reel for SOIC, MSOP)
MCP6574T	Quad Comparator (Tape and Reel for TSSOP and SOIC)

Temperature Range: E = -40°C to +125°C

Package:

LT	=	Plastic Package (SC-70), 5-lead (MCP6571 only)
OT	=	Plastic Small Outline transistor (SOT-23), 5-lead (MCP6571 only)
SN	=	Plastic Small Outline, (3.90 mm), 8-lead (MCP6572 only)
MS	=	Plastic MSOP, 8-lead (MCP6572 only)
ST	=	Plastic Thin Shrink Small Outline (4.4 mm), 14-lead (MCP6574 only)
SL	=	Plastic Small Outline, (3.90 mm), 14-lead (MCP6574 only)

Class:

(Blank)	=	Non-Automotive
VAO	=	Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a)MCP6571T-E/LT:	Tape and Reel, Extended temperature, 5LD SC-70 package
b)MCP6571T-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
c)MCP6571RT-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
d)MCP6571UT-E/LT:	Tape and Reel, Extended temperature, 5LD SC-70 package
e)MCP6571UT-E/OT:	Tape and Reel, Extended temperature, 5LD SOT-23 package
a)MCP6572T-E/SN:	Tape and Reel, Extended temperature, 8LD SOIC package
b)MCP6572T-E/MS:	Tape and Reel, Extended temperature, 8LD MSOP package
a)MCP6574T-E/ST:	Tape and Reel, Extended temperature, 14LD TSSOP package
b)MCP6574T-E/SL:	Tape and Reel, Extended temperature, 14LD SOIC package

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XX	XXX(2)
Device	Tape and Reel Option	Temperature Range	Package	CLASS

Device:

MCP6571T	Single Comparator (Tape and Reel) (SC-70, SOT-23)
MCP6571RT	Single Comparator (Tape and Reel) (SOT-23)
MCP6571UT	Single Comparator (Tape and Reel) (SC-70, SOT-23)
MCP6572T	Dual Comparator (Tape and Reel for SOIC, MSOP)
MCP6574T	Quad Comparator (Tape and Reel for TSSOP and SOIC)

Temperature Range: E = -40°C to +125°C

Package:

LT= Plastic Package (SC-70), 5-lead (MCP6571 only)

OT=Plastic Small Outline transistor (SOT-23), 5-lead (MCP6571 only)

SN=Plastic Small Outline, (3.90 mm), 8-lead (MCP6572 only)

MS=Plastic MSOP, 8-lead (MCP6572 only)

ST=Plastic Thin Shrink Small Outline (4.4 mm), 14-lead (MCP6574 only)

SL=Plastic Small Outline, (3.90 mm), 14-lead (MCP6574 only)

Class: (Blank)= Non-Automotive

VAO = Automotive

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Automotive parts are AEC-Q100 qualified. Grade 1.

Examples:

a)MCP6571T-E/LTVAO:	Tape and Reel, Automotive, Extended temperature,5LD SC-70 package
b)MCP6571T-E/OTVAO:	Tape and Reel, Automotive, Extended temperature, 5LD SOT-23 package
c)MCP6571RT-E/OTVAO:	Tape and Reel, Extended temperature, 5LD SOT-23 package
d)MCP6571UT-E/LTVAO:	Tape and Reel, Automotive, Extended temperature, 5LD SC-70 package
e)MCP6571UT-E/OTVAO:	Tape and Reel, Automotive Extended temperature, 5LD SOT-23 package
a)MCP6572T-E/SNVAO:	Tape and Reel, Automotive, Extended temperature, 8LD SOIC package
b)MCP6572T-E/MSVAO:	Tape and Reel, Extended temperature, 8LD MSOP package
a)MCP6574T-E/STVAO:	Tape and Reel, Extended temperature, 14LD TSSOP package
b)MCP6574T-E/SLVAO:	Tape and Reel, Extended temperature, 14LD SOIC package

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