a MICROCHIP company

6 Lake Street, Lawrence, MA 01841
1-800-446-1158 / (978) 620-2600 / Fax: (978) 689-0803
Website: http://www.microsemi.com

Gort Road Business Park, Ennis, Co. Clare, Ireland
Tel: +353 (0) 65 6840044 Fax: +353 (0) 65 6822298

TECHNICAL DATA SHEET

ZENER DIODE

- **Monolithic Temperature Compensated Zener Reference Chips**
- **All Junctions Completely Protected with Silicon Dioxide**
- **Electrically Equivalent to 1N821 Thru 1N829**
- **Compatible with all Wire Bonding and Die Attach Techniques with the Exception of Solder Reflow**

DEVICES

CD821 thru CD829A

QUALIFIED LEVELS

JANHC
JANKC

MAXIMUM RATING AT 25°C

Operating Temperature: -65°C to +175°C
Storage Temperature: -65°C to +175°C

REVERSE LEAKAGE CURRENT

I_R = 2µA @ 25°C & V_R = 3Vdc

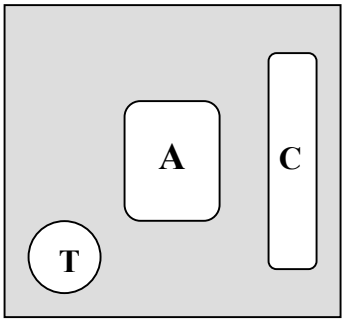
ELECTRICAL CHARACTERISTICS ***(T_A = 25°C, unless otherwise specified)***

TYPE NUMBER	ZENER VOLTAGE V_{ZT} @ I_{ZT}	ZENER TEST CURRENT I_{ZT}	MAXIMUM ZENER IMPEDANCE Z_{ZT} (Note 1)	-55° to +100° VOLTAGE TEMPERATURE STABILITY ΔV_{ZT} (Note 2)	EFFECTIVE TEMPERATURE COEFFICIENT α_{VZ}
	VOLTS	mA	OHMS	mV	% / °C
CD821	5.9 – 6.5	7.5	15	96	0.01
CD821A	5.9 – 6.5	7.5	13	96	0.01
CD823	5.9 – 6.5	7.5	15	48	0.005
CD823A	5.9 – 6.5	7.5	13	48	0.005
CD825	5.9 – 6.5	7.5	15	19	0.002
CD825A	5.9 – 6.5	7.5	13	19	0.002
CD826	5.9 – 6.5	7.5	15	20	0.002
CD827	5.9 – 6.5	7.5	15	9	0.001
CD827A	5.9 – 6.5	7.5	13	9	0.001
CD828	6.2 – 6.9	7.5	15	10	0.001
CD829	5.9 – 6.5	7.5	15	5	0.0005
CD829A	5.9 – 6.5	7.5	13	5	0.0005

NOTE:

1. Zener impedance is derived by superimposing on I_{ZT} a 60 Hz rms ac current equal to 10% of I_{ZT}. The A suffix devices have different limits than the original JEDEC registration.
2. The maximum allowable change observed over the entire temperature range i.e., the diode voltage will not exceed the specified mV at any discrete temperature between the established limits, per JEDEC standard No.5

Figure 1



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TYPICAL CHANGE OF TEMPERATURE COEFFICIENT WITH CHANGE IN OPERATING CURRENT

Qualified per MIL-PRF-19500/159

CD821 thru CD829A

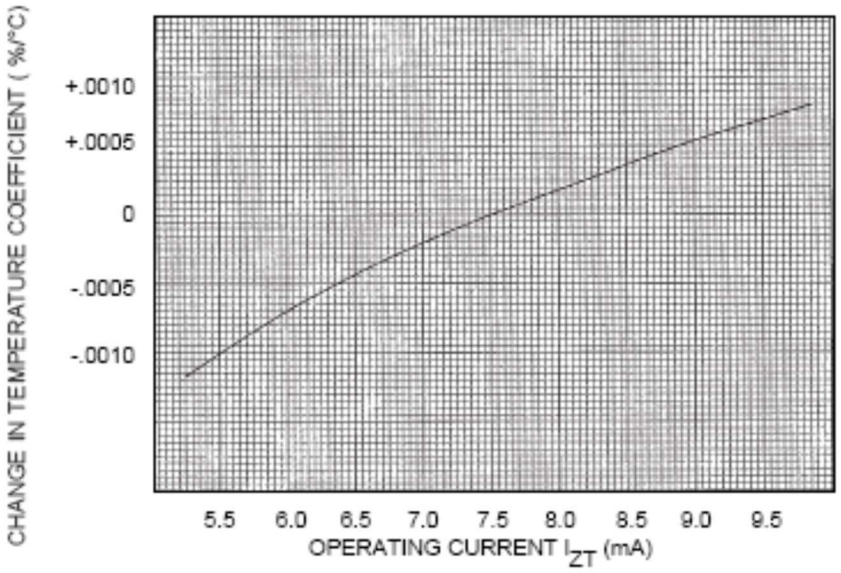

FIGURE 2

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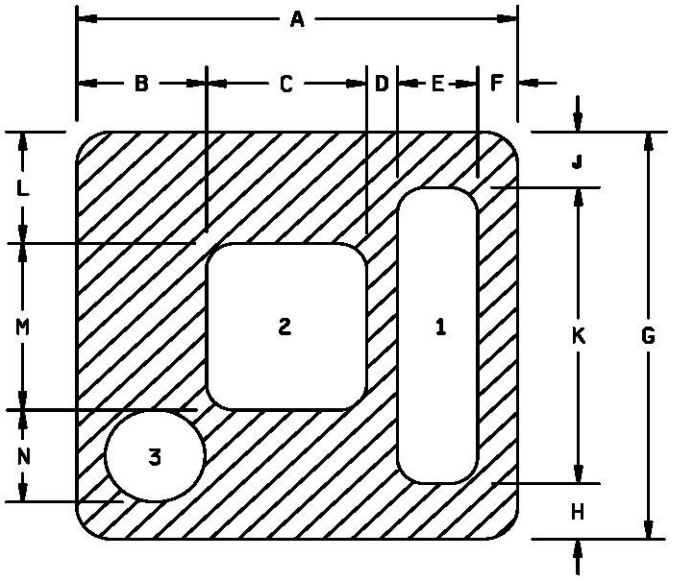
TECHNICAL DATA SHEET

PACKAGE DIMENSIONS



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.0280	.0320	.711	.813
B	.0080	.0100	.203	.254
C	.0104	.0106	.264	.269
D	.0019	.0021	.048	.053
E	.0054	.0056	.137	.142
F	.0020	.0040	.050	.102
G	.0280	.0320	.711	.813
H	.0030	.0050	.076	.127
J	.0030	.0050	.076	.127
K	.0209	.0211	.531	.536
L	.0080	.0100	.203	.254
M	.0104	.0106	.264	.269
N	.0059	.0061	.150	.155

Backside must be electrically isolated to ensure proper performance.

Figure 3

DESIGN DATA

Metallization:

Top:	1 (Cathode)	Al	Circuit layout data:
	2 (Anode)	Al	For zener operation, cathode must be operated positive with respect to anode.
	3 (Test pad)	Al	Test pad is for wire bond evaluation only. No electrical contact is made with test pad.
Back:		Au	

Al thickness	25,000Å minimum.
Gold thickness	4,000Å minimum.
Chip thickness	.010 inch (0.25 mm) ±0.002 inch (+0.05 mm).

NOTES:

1. Dimensions are in inches unless otherwise indicated.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

JANHC and JANKC (A-version) die dimensions.