LAN8267

Quad 1G/10G 1588 Optical Ethernet PHY Transceiver

Highlights

- Four 1G/10G serial Host interfaces
  - IEEE 802.3-2018 compliant
  - Backplane Ethernet with KR/RS FEC
- Four 1G/10G serial Line interfaces
  - IEEE 802.3-2018 compliant
  - SFP, XFP, SFP+, QSFP+
- Integrated cross-connect features
  - Any line port connectible to any host port
  - 1:1 and 1+1 host redundancy
- IEEE 1588 and 802.1AS timestamping
- TSN frame preemption
- PCS and MAC retimer modes
- 256-BALL HFC-BGA (14 x 14 mm)
- Extended temperature range -40°C (T_A) to +110°C (T_J)

Target Applications

- 5G Small Cell (up to class D requirements)
- Industrial
- Enterprise IT
- Broadband

Key Benefits

- IEEE 1588 -2008/2019 and 802.1AS -2011/2020
  - Supporting ITU-T G.8273.2 Classes C and D and IEEE 802.1CM-2018 Category A+
  - Highly flexible classification engine supports combinations of Ethernet, IPv4, IPv6, UDP, MPLS and Pseudowire. Multiple flows per port are supported.
  - Support for OC (PTP TimeTransmitter and TimeReceiver), BC and TC (one-step and two-step)
  - 1PPS In/Out, with flexible TOD Load options
  - Timestamped 1588 frames can be Express frames or non-fragmented Preemptible frames
- PCS Retimer mode (Ethernet serial PHY w/ 1588)
  - Fully configurable Ethernet PHY on Host and Line
  - Host and Line must be of same speed but can be of different formats (e.g. Host is Backplane Ethernet with KR FEC)
  - Host and Line may be synchronous or may have PPM clock differences handled by rate adaptation
  - IEEE 1588 timestamping and Synchronous Ethernet support
  - TSN Frame Preemption support
- MAC Retimer (Ethernet serial PHY with 1588 mode)
  - Fully configurable Ethernet MAC and PHY on Host and Line
  - Host and Line must be of the same speed (e.g., 10G Ethernet), but can be of different formats (e.g., KR FEC on Host and no FEC on Line)
  - Host and Line may be fully synchronous or may have PPM clock differences handled by rate adaptation
  - IEEE 1588 timestamping and Synchronous Ethernet support
  - TSN Frame Preemption support
- IEEE 802.3-2018 support for:
  - 1000BASE: KX, SX, LX
  - 10GBASE: “CR”, KR, SR, LR, ER
    -KR: KR FEC, ANEG, Training
- Loopback support
- Diagnostics
  - RX Eye Monitor plot
  - PRBS generator/checker
- Support for jumbo frames up to 10 KB (10,240 bytes)
- PHY Management Interface is MDIO or SPI
  - High-speed SPI can be used simultaneously with MDIO to support high-bandwidth management needs of 1588
- Pin-strapping options
- 40 GPIOs which alternately support:
  - Two-wire Module Management Interface per port
  - Two chip Interrupts
  - Two LEDs (Link, Activity) per port
- Coma mode support to eliminate port link bouncing at startup and to synchronize LEDs
- Power down and power saving modes
- Reference clock inputs
  - System Reference Clock
  - 1588 Reference Clock
- Synchronous Ethernet support
  - Two recovered clock outputs, each selectable to be from any Line recovered clock
  - Recovered clock outputs are optionally squelched when the applicable clock is deemed unreliable
- JTAG support

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1.0 INTRODUCTION

1.1 General Description

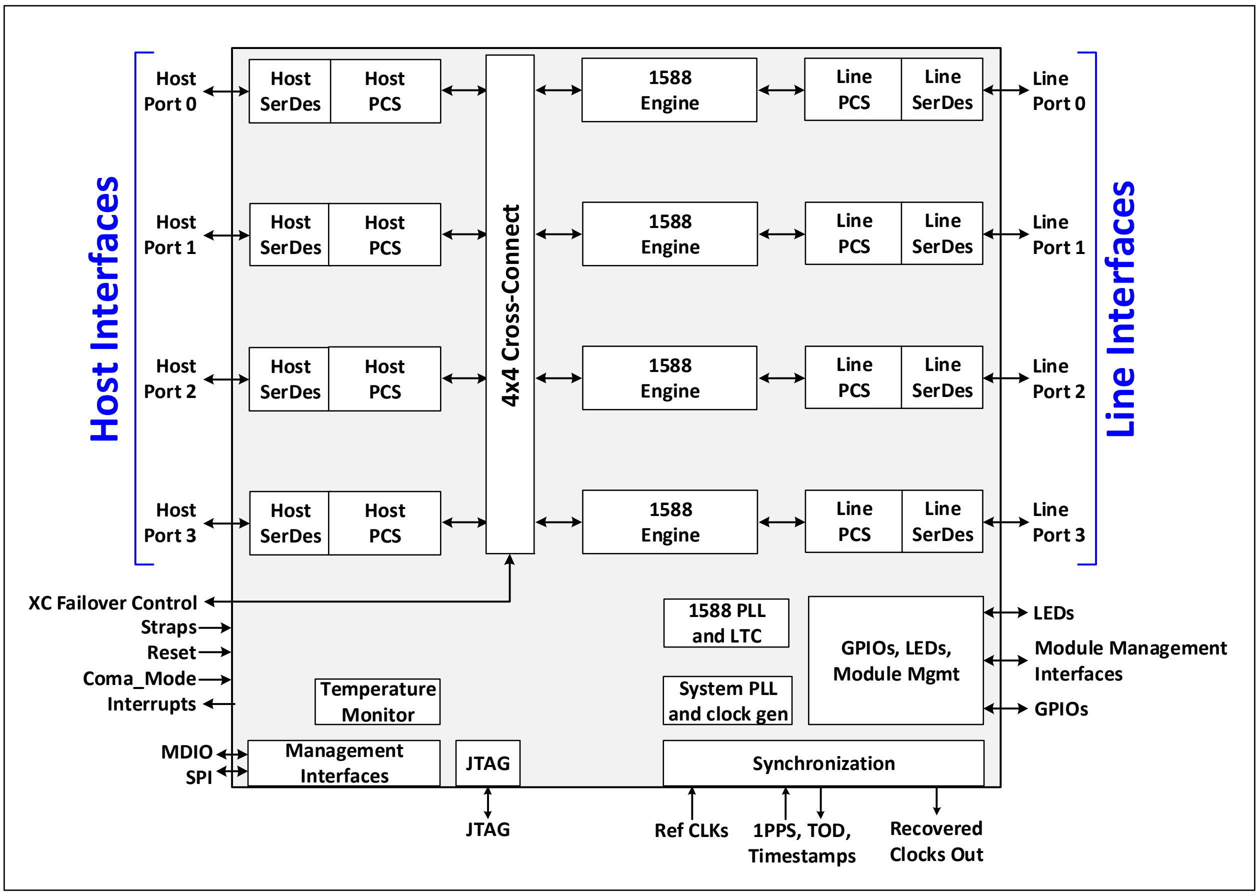
The Microchip LAN8267 is a quad-port 1G/10G serial optical Ethernet PHY transceiver which provides multiple line and host interface options. On the line interfaces, the supports transmission and reception of data over a variety of optical module serial interfaces. These serial interfaces support both optical modules and copper cables. On the host interfaces, the LAN8267 supports transmission and reception of data over a variety of chip-to-chip and backplane serial interfaces. An integrated Cross-Connect function enables any line port to connect to any host port. Host Redundancy options are provided.

LAN8267 includes high-accuracy timestamping functions to support IEEE-1588 solutions using Microchip Ethernet switches, as well as customer solutions based on SoCs and FPGAs. Synchronous Ethernet (SyncE) and TSN Frame Preemption is supported.

The LAN8267 provides a complete suite of on-chip instrumentation including built-in self-test (BIST) functions, line-side and client-side circuit loopbacks, pattern generation and error detection. It is well-suited for SFP+ optical modules and direct-attach copper (DAC) cabling as well as challenging backplane interface applications.

An internal block diagram of the LAN8267 is shown in Figure 1-1.

FIGURE 1-1: LAN8267 INTERNAL BLOCK DIAGRAM



The following diagrams illustrate three primary target use cases:

- PHY with High-Accuracy 1588 Timestamping
- PHY with Backplane Signal Reconditioning
- PHY with Backplane Signal Reconditioning and System Redundancy

FIGURE 1-2: PHY WITH HIGH-ACCURACY 1588 TIMESTAMPING

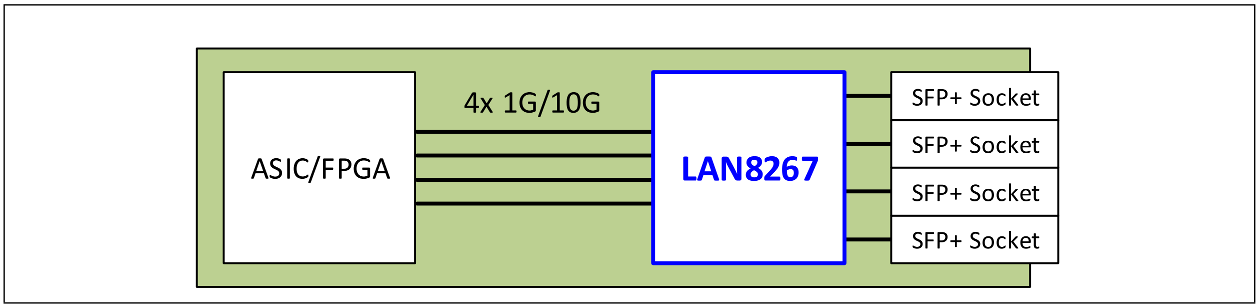


Figure 1-2 details a printed circuit board (PCB) which includes an ASIC/FPGA, LAN8267, and SFP+ sockets. The LAN8267 may be required in such a design for the following reasons:

- Addition of advanced 1588 timestamping
- Ethernet format conversion such as adding FEC or FEC termination / regeneration
- Standardization on the LAN8267 for all such interfaces

FIGURE 1-3: PHY WITH BACKPLANE SIGNAL RECONDITIONING

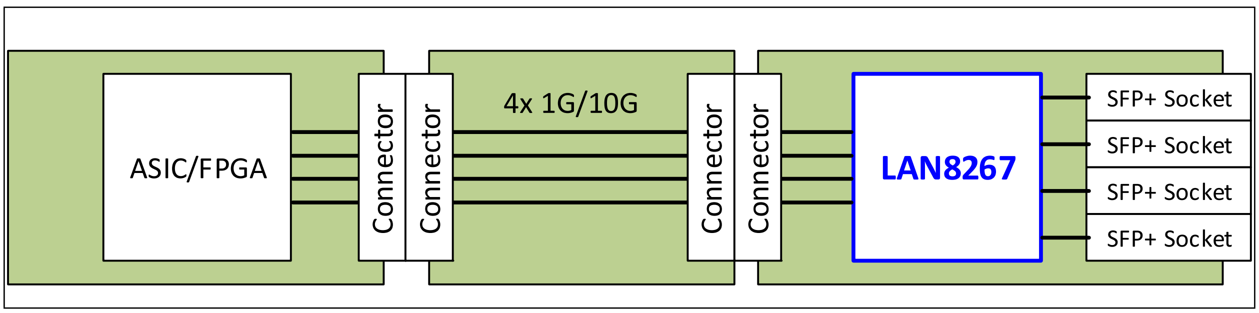


Figure 1-3 details a modular chassis system with the following elements:

- A pluggable switching or processing card containing an ASIC or FPGA with four serial interfaces to the backplane. Each interface is a separate 1G or 10G Ethernet port.
- A backplane integrated into the chassis, supporting a variety of pluggable cards.
- A pluggable Optical Media Card with four SFP+ sockets. These sockets support pluggable optical modules such as 1 GbE SFP and 10 GbE SFP+. These sockets also support Direct Attach Copper (DAC) twinax cables.

The signals are connected over the backplane using backplane Ethernet formats (1GBASE-KX or 10GBASE-KR). The LAN8267 terminates the backplane signals, processes the Ethernet frames, and generates clean signals into the network, meeting optical module or cable specifications (and performs similar functions in the opposite direction).

The LAN8267 can perform a range of processing functions in this role:

- Signal reconditioning across the backplane, both electrical and timing
- Ethernet format conversion functions between the backplane (host) and line interfaces, such as FEC termination / regeneration
- Advanced 1588 timestamping

Note:	The LAN8267 only supports individual Ethernet ports up to 10 Gbps and does not support multi-lane Ethernet ports such as 40 Gbps or 100 Gbps.

FIGURE 1-4: PHY WITH BACKPLANE SIGNAL RECONDITIONING AND SYSTEM REDUNDANCY

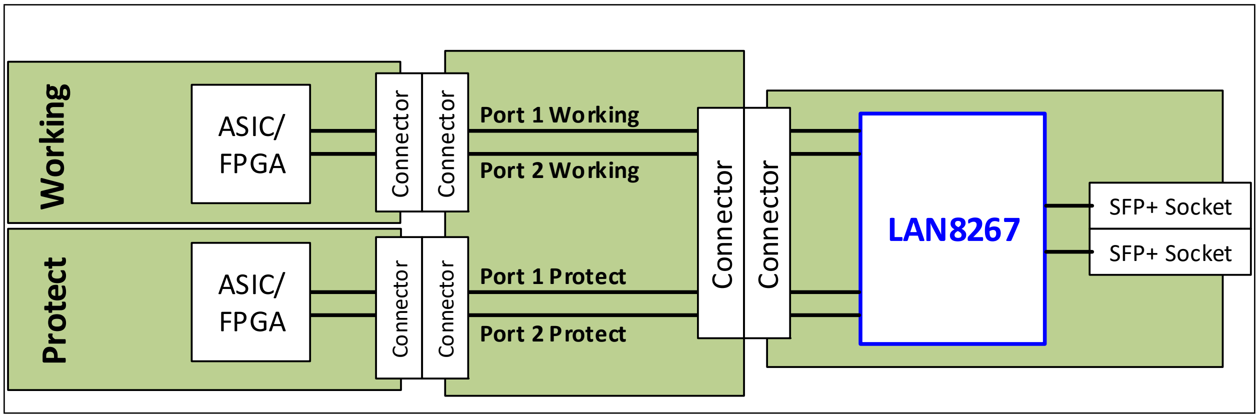


Figure 1-4 details a modular chassis system. It is similar to Figure 1-3 but also has a redundant pair of pluggable switching or processing cards, each containing an ASIC or FPGA and each having two serial interfaces across the backplane to the LAN8267. In this mode, the LAN8267 can only support two optical modules.

The LAN8267 still supports the previously mentioned signal reconditioning, Ethernet format conversion, and 1588 timestamping functions. However, in this example the LAN8267 additionally provides fault detection and fail-over capabilities, enabling redundant connections across the backplane.

2.0 PIN DESCRIPTIONS

This chapter included the following sections:

- Pin Assignments
- PinDescriptions
- Buffer Types

2.1 Pin Assignments

FIGURE 2-1: 256-BGA BALL ASSIGNMENTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VSS	RXIN0N	VDDHS_N	TXOUT0P	VDDHS_N	RXIN1N	VDDHS_N	TXOUT1P	VDDHS_N	RXIN2N	VDDHS_N	TXOUT2P	VDDHS_N	RXIN3N	VDDHS_N	VSS
B	VSS	RXIN0P	VSS	TXOUT0N	VSS	RXIN1P	VSS	TXOUT1N	VSS	RXIN2P	VSS	TXOUT2N	VSS	RXIN3P	VSS	TXOUT3P
C	GPIO32	GPIO33	FAILOVEROUT0/ STRAP_RSVD_1	RESET_N	VSS	VDDH18_N	VDDH18_N	VDDHS_N	VDDHS_N	VDDH18_N	VDDH18_N	VSS	VSS	VSS	VSS	TXOUT3N
D	LREFCKP	LREFCKN	FAILOVERIN0	JTAG_SEL	COMA_MODE	VSS	VSS	VDDHV_N	VDDHV_N	VSS	VSS	VDD	GPIO39	GPIO38	GPIO37	VSS
E	TEST	TMS	TDO	TDI	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	GPIO36	GPIO31	GPIO30	GPIO29
F	TCK	PTP1588_STI_CLK	PTP1588_STI_DO	PTP1588_STI_CS_N	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDO_B	GPIO28	GPIO27	GPIO26	GPIO25
G	PTP1588_LSC_2	PTP1588_LSC_1	PTP1588_LSC_0	RCKOUTB	VDDO_A	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_B	GPIO24	GPIO23	GPIO22	GPIO21
H	SPI_CLIENT_MISO	SPI_CLIENT_MOSI	RCKOUTA	MDIO	VDDO_A	VDDO_A	VSS	VSS	VSS	VSS	VDDO_B	VDDO_B	GPIO20	GPIO19	GPIO18	GPIO17
J	SPI_CLIENT_SCK	SPI_CLIENT_SNN	MDC	GPIO35	VDDO_A	VDDO_A	VSS	VSS	VSS	VSS	VDDO_B	VDDO_B	GPIO16	GPIO15	GPIO14	GPIO13
K	VDDA_1588APLL	VSSA_1588APLL	GPIO34	TRST	VDDO_18	VSS	VSS	VSS	VSS	VSS	VSS	VDDO_18	GPIO12	GPIO11	GPIO10	GPIO9
L	PTP1588_LSC_3_P	PTP1588_LSC_3_N	PADDR4	PADDR3	VDDO_18	VDD	VDD	VDD	VDD	VDD	VDD	RESERVED	THERMD_Sn	GPIO8	GPIO7	GPIO6
M	VDDA_SYSPLL	VSSA_SYSPLL	PADDR2	PADDR1	VDD	VDD	VDD	VDD	VDD	VDD	VDD	TESTA	THERMD_Sp	GPIO5	GPIO4	GPIO3
N	SYSREFCKP	SYSREFCKN	PADDR0	FAILOVEROUT1	VDD	VSS	VSS	VDDHV_S	VDDHV_S	VSS	VSS	VDD	THERMD_Fn	GPIO2	GPIO1	GPIO0
P	VSS	VSS	FAILOVERIN1	VDDO_A_MODE	VDDO_B_MODE	VDDH18_S	VDDH18_S	VDDHS_S	VDDHS_S	VDDH18_S	VDDH18_S	VSS	THERMD_Fp	VSS	VSS	TXIN3P
R	VSS	RXOUT0N	VSS	TXIN0P	VSS	RXOUT1N	VSS	TXIN1P	VSS	RXOUT2N	VSS	TXIN2P	VSS	RXOUT3N	VSS	TXIN3N
T	VSS	RXOUT0P	VDDHS_S	TXIN0N	VDDHS_S	RXOUT1P	VDDHS_S	TXIN1N	VDDHS_S	RXOUT2P	VDDHS_S	TXIN2N	VDDHS_S	RXOUT3P	VDDHS_S	VSS

Top of 256-HFC-BGA Package

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 2-1: 256-BGA BALL ASSIGNMENTS (1-8)

Ball	1	2	3	4	5	6	7	8
A	VSS	RXIN0N	VDDHS_N	TXOUT0P	VDDHS_N	RXIN1N	VDDHS_N	TXOUT1P
B	VSS	RXIN0P	VSS	TXOUT0N	VSS	RXIN1P	VSS	TXOUT1N
C	GPIO32	GPIO33	FAILOVEROUT0/ STRAP_RSVD_1	RESET_N	VSS	VDDH18_N	VDDH18_N	VDDHS_N
D	LREFCKP	LREFCKN	FAILOVERIN0	JTAG_SEL	COMA_MODE	VSS	VSS	VDDHV_N
E	TEST	TMS	TDO	TDI	VDD	VDD	VDD	VDD
F	TCK	PTP1588_STI_CLK	PTP1588_STI_DO	PTP1588_STI_CS_N	VDD	VDD	VDD	VDD
G	PTP1588_LSC_2	PTP1588_LSC_1	PTP1588_LSC_0	RCKOUTB	VDDO_A	VSS	VSS	VSS
H	SPI_CLIENT _MISO	SPI_CLIENT _MOSI	RCKOUTA	MDIO	VDDO_A	VDDO_A	VSS	VSS
J	SPI_CLIENT _SCK	SPI_CLIENT _SSN	MDC	GPIO35	VDDO_A	VDDO_A	VSS	VSS
K	VDDA_1588APLL	VSSA_1588APLL	GPIO34	TRST	VDDO_18	VSS	VSS	VSS
L	PTP1588 _LSC_3_P	PTP1588 _LSC_3_N	PADDR4	PADDR3	VDDO_18	VDD	VDD	VDD
M	VDDA_SYSPLL	VSSA_SYSPLL	PADDR2	PADDR1	VDD	VDD	VDD	VDD
N	SYSREFCKP	SYSREFCKN	PADDR0	FAILOVEROUT1	VDD	VSS	VSS	VDDHV_S
P	VSS	VSS	FAILOVERIN1	VDDO_A_MODE	VDDO_B_MODE	VDDH18_S	VDDH18_S	VDDHS_S
R	VSS	RXOUT0N	VSS	TXIN0P	VSS	RXOUT1N	VSS	TXIN1P
T	VSS	RXOUT0P	VDDHS_S	TXIN0N	VDDHS_S	RXOUT1P	VDDHS_S	TXIN1N

TABLE 2-2: 256-BGA BALL ASSIGNMENTS (9-16)

Ball	9	10	11	12	13	14	15	16
A	VDDHS_N	RXIN2N	VDDHS_N	TXOUT2P	VDDHS_N	RXIN3N	VDDHS_N	VSS
B	VSS	RXIN2P	VSS	TXOUT2N	VSS	RXIN3P	VSS	TXOUT3P
C	VDDHS_N	VDDH18_N	VDDH18_N	VSS	VSS	VSS	VSS	TXOUT3N
D	VDDHV_N	VSS	VSS	VDD	GPIO39	GPIO38	GPIO37	VSS
E	VDD	VDD	VDD	VDD	GPIO36	GPIO31	GPIO30	GPIO29
F	VDD	VDD	VDD	VDDO_B	GPIO28	GPIO27	GPIO26	GPIO25
G	VSS	VSS	VSS	VDDO_B	GPIO24	GPIO23	GPIO22	GPIO21
H	VSS	VSS	VDDO_B	VDDO_B	GPIO20	GPIO19	GPIO18	GPIO17
J	VSS	VSS	VDDO_B	VDDO_B	GPIO16	GPIO15	GPIO14	GPIO13
K	VSS	VSS	VSS	VDDO_18	GPIO12	GPIO11	GPIO10	GPIO9
L	VDD	VDD	VDD	RESERVED	THERMD_Sn	GPIO8	GPIO7	GPIO6
M	VDD	VDD	VDD	TESTA	THERMD_Sp	GPIO5	GPIO4	GPIO3
N	VDDHV_S	VSS	VSS	VDD	THERMD_Fn	GPIO2	GPIO1	GPIO0
P	VDDHS_S	VDDH18_S	VDDH18_S	VSS	THERMD_Fp	VSS	VSS	TXIN3P
R	VSS	RXOUT2N	VSS	TXIN2P	VSS	RXOUT3N	VSS	TXIN3N
T	VDDHS_S	RXOUT2P	VDDHS_S	TXIN2N	VDDHS_S	RXOUT3P	VDDHS_S	VSS

2.2 Pin Descriptions

This section contains descriptions of the various LAN8267 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 2-3: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Ethernet (Line Interface)			
Ethernet Line Port 0 Input Data Negative	**RXIN0N**	AI	Negative input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Input Data Positive	**RXIN0P**	AI	Positive input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Input Data Negative	**RXIN1N**	AI	Negative input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Input Data Positive	**RXIN1P**	AI	Positive input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Input Data Negative	**RXIN2N**	AI	Negative input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Input Data Positive	**RXIN2P**	AI	Positive input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Line Port 3 Input Data Negative	**RXIN3N**	AI	Negative input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 3 Input Data Positive	**RXIN3P**	AI	Positive input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Output Data Negative	**TXOUT0N**	AO	Negative output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 0 Output Data Positive	**TXOUT0P**	AO	Positive output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Output Data Negative	**TXOUT1N**	AO	Negative output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 1 Output Data Positive	**TXOUT1P**	AO	Positive output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Output Data Negative	**TXOUT2N**	AO	Negative output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 2 Output Data Positive	**TXOUT2P**	AO	Positive output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Line Port 3 Output Data Negative	TXOUT3N	AO	Negative output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet Line Port 3 Output Data Positive	TXOUT3P	AO	Positive output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required and is typically built into the SFP module.
Ethernet (Host Interface)			
Ethernet Host Port 0 Input Data Negative	TXIN0N	AI	Negative input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Input Data Positive	TXIN0P	AI	Positive input signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Input Data Negative	TXIN1N	AI	Negative input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Input Data Positive	TXIN1P	AI	Positive input signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Input Data Negative	TXIN2N	AI	Negative input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Input Data Positive	TXIN2P	AI	Positive input signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Input Data Negative	TXIN3N	AI	Negative input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Host Port 3 Input Data Positive	**TXIN3P**	AI	Positive input signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Output Data Negative	**RXOUT0N**	AO	Negative output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 0 Output Data Positive	**RXOUT0P**	AO	Positive output signal of Port 0 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Output Data Negative	**RXOUT1N**	AO	Negative output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 1 Output Data Positive	**RXOUT1P**	AO	Positive output signal of Port 1 differential pair. **Note:** Internal 100 Ohms (nominal) differential input termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Output Data Negative	**RXOUT2N**	AO	Negative output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 2 Output Data Positive	**RXOUT2P**	AO	Positive output signal of Port 2 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Output Data Negative	**RXOUT3N**	AO	Negative output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Ethernet Host Port 3 Output Data Positive	**RXOUT3P**	AO	Positive output signal of Port 3 differential pair. **Note:** Internal 100 Ohms (nominal) differential output termination. **Note:** External AC coupling is required.
Reference Clocks			
Host Port / 1588 / System Reference Clock Input Negative	**SYSREFCKN**	CLOCK	Negative input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Host Port / 1588 / System Reference Clock Input Positive	**SYSREFCKP**	CLOCK	Positive input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Line Port Reference Clock Input Negative	**LREFCKN**	CLOCK	Negative input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Line Port Reference Clock Input Positive	**LREFCKP**	CLOCK	Positive input signal of differential pair. An external AC coupling capacitor is required. **Note:** Internal 100 Ohms (nominal) differential input termination.
Recovered Output Clocks			
Recovered Clock Output A	**RCKOUTA**	LVCMOS Out (4 ma)	Output clock signal. Selectable from: • Any Host Port recovered clock • Any Line Port recovered clock • System PLL • 1588 PLL
Recovered Clock Output B	**RCKOUTB**	LVCMOS Out (4 ma)	Output clock signal. Selectable from: • Any Host Port recovered clock • Any Line Port recovered clock • System PLL • 1588 PLL
Cross Connect Failover Control			
System Port 0 Failover Control In	**FAILOVERIN0**	LVCMOS In (4 ma)	Cross Connect Failover indication. Indicates to the device that a Working / Protect pair failover was performed by the host system.
System Port 0 Failover Control Out	**FAILOVEROUT0**	LVCMOS Out	Cross Connect Failover indication. Indicates to the host system that a Working / Protect pair failover was performed by the device.
System Port 1 Failover Control In	**FAILOVERIN1**	LVCMOS In	Cross Connect Failover indication. Indicates to the device that a Working / Protect pair failover was performed by the host system.
System Port 1 Failover Control Out	**FAILOVEROUT1**	LVCMOS Out (4 ma)	Cross Connect Failover indication. Indicates to the host system that a Working / Protect pair failover was performed by the device.
PHY Management Interface			
PHY Management Interface Clock	**MDC**	LVCMOS In	PHY Management clock input
PHY Management Interface Data	**MDIO**	LVCMOS I/O (4 ma)	PHY Management data interface

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PHY Base Address [4:0]	**PADDR[4:0]**	LVCMOS In	PHY MDIO Management Base Address [4:0] Any tie high or pull-up must be to **VDDO_A**.
PHY SPI Client Clock	**SPI_CLIENT_SCK**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO**/**MDC**.
PHY SPI Client Data Out	**SPI_CLIENT_MISO**	LVCMOS Out (4ma)	Client SPI can be used in place of or fully in parallel with **MDIO**/**MDC**.
PHY SPI Client Data In	**SPI_CLIENT_MOSI**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO**/**MDC**.
PHY SPI Client Chip Select	**SPI_CLIENT_SSN**	LVCMOS In	Client SPI can be used in place of or fully in parallel with **MDIO**/**MDC**.
IEEE 1588 Interface			
PTP 1588 Load/ Save/Clock In 3 Negative	**PTP1588_LSC_3_N**	LVDS In	Controls loading and saving of the 1588 LTC. TOD serial input and clock reference. Supports ePPS format, where the PPS is combined with the clock. Can also be used as sampling clock for another 1PPS **PTP1588_LSC_*x*** input pin. **Note:** The LVDS pair requires an external differential termination of 100 Ohms placed as close to the pins as possible. **Note:** If not used, the LVDS pair should be tied with the _P ball to VDDO_18 and the _N ball to VSS.
PTP 1588 Load/ Save/Clock In 3 Positive	**PTP1588_LSC_3_P**	LVDS In	Controls loading and saving of the 1588 LTC. TOD serial input and clock reference. Supports ePPS format, where the PPS is combined with the clock. Can also be used as sampling clock for another 1PPS **PTP1588_LSC_*x*** input pin. **Note:** The LVDS pair requires an external differential termination of 100 Ohms placed as close to the pins as possible. **Note:** If not used, the LVDS pair should be tied with the _P ball to VDDO_18 and the _N ball to VSS.
PTP 1588 Load/ Save/Clock In/Out 2	**PTP1588_LSC_2**	LVCMOS I/O (4 ma)	Controls loading and saving of the 1588 LTC. TOD serial input and clock reference. Supports ePPS format, where the PPS is combined with the clock. Can also be used as sampling clock for another 1PPS **PTP1588_LSC_*x*** input pin. Selectable waveform, including 1PPS or TOD output.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
PTP 1588 Load/ Save/Clock In/Out 1	**PTP1588_LSC_1**	LVCMOS I/O (4 ma)	Controls loading and saving of the 1588 LTC. TOD serial input and clock reference. Supports ePPS format, where the PPS is combined with the clock. Can also be used as sampling clock for another 1PPS **PTP1588_LSC_*x*** input pin. Selectable waveform, including 1PPS or TOD output.
PTP 1588 Load/ Save/Clock In/Out 0	**PTP1588_LSC_0**	LVCMOS I/O (4 ma)	Controls loading and saving of the 1588 LTC. TOD serial input and clock reference. Supports ePPS format, where the PPS is combined with the clock. Can also be used as sampling clock for another 1PPS **PTP1588_LSC_*x*** input pin. Selectable waveform, including 1PPS or TOD output.
PTP 1588 Serial Timestamp Interface Clock Out	**PTP1588_STI_CLK**	LVCMOS Out (4 ma)	PTP 1588 serial timestamp interface clock output.
PTP 1588 Serial Timestamp Interface Chip Select Out	**PTP1588_STI_CS_N**	LVCMOS Out (4 ma)	PTP 1588 serial timestamp interface chip select output.
PTP 1588 Serial Timestamp Interface Data Out	**PTP1588_STI_DO**	LVCMOS Out (4 ma)	PTP 1588 serial timestamp interface data output.
Miscellaneous			
GPIOs [39:0]	**GPIO[39:0]**	LVCMOS I/O (4 ma) (PU)	General Purpose Inputs/Outputs 39-0. Open-Drain/Push-Pull, configurable polarity. Many GPIOs are shared with other functions. Alternate function selection is configured via GPIO registers. Refer to Table 2-4 for additional details. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
System Reset	**RESET_N**	LVCMOS In (Schmitt)	Active low chip reset. At power-up, **RESET_N** must not be deasserted until all power and clocks have been stable for the specified minimum duration. Configuration strap values are latched at the deassertion (rising edge) of **RESET_N**.
Coma Mode Control	**COMA_MODE**	LVCMOS In	Drive high to activate Coma Mode. After all ports are configured, drive low to enable normal operation. Hold low to disable this feature.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Test Mode	**TEST**	LVCMOS In (PD) (Schmitt)	Enables test mode. For proper operation, this pin should be tied low. 0 = Functional Mode 1 = Test Mode
Thermal Diode Force Positive	**THERMD_Fp**	AI	Thermal Diode 1.5mA current source.
Thermal Diode Force Negative	**THERMD_Fn**	AI	Thermal Diode current ground.
Thermal Diode Sense Positive	**THERMD_Sp**	AO	Thermal Diode sense positive. **Note:** For measurement only; never drive current on this signal.
Thermal Diode Sense Negative	**THERMD_Sn**	AO	Thermal Diode sense negative. **Note:** For measurement only; never drive current on this signal.
Reserved	**TESTA**	LVCMOS I/O (PD) (Schmitt)	For proper operation, this pin should be tied low.
Reserved	**RESERVED**	-	These pins are reserved for future use and should not be used.
		JTAG	
JTAG Test Data Input	**TDI**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) data input. **Note:** When not used, tie this pin high.
JTAG Test Data Output	**TDO**	LVCMOS Out (8 ma)	JTAG (IEEE 1149.1) test data output.
JTAG Test Reset	**TRST**	LVCMOS In (PD) (Schmitt)	JTAG (IEEE 1149.1) test reset. Resets the TAP controller’s state machine. For proper operation, this pin should be tied low.
JTAG Test Clock	**TCK**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) test clock. **Note:** When not used, tie this pin low.
JTAG Test Mode Select	**TMS**	LVCMOS In (Schmitt)	JTAG (IEEE 1149.1) test mode select. **Note:** When not used, tie this pin low.
JTAG Select Input	**JTAG_SEL**	LVCMOS In (PD) (Schmitt)	For proper operation, this pin should be tied low.
		Power	
+0.9V Digital Core Logic Power Supply Input	**VDD**	P	+0.9V digital core logic power supply input.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.8V SerDes Power Supply Input (North Side)	VDDH18_N	P	+1.8V SerDes power supply input. (North Side)
+1.0V SerDes Analog TX/RX Power Supply Input (North Side)	VDDHS_N	P	+1.0V SerDes analog TX/RX power supply input. (North Side)
+1.0V SerDes Analog VCO Power Supply Input (North Side)	VDDHV_N	P	+1.0V SerDes analog Voltage Controlled Oscillator (VCO) power supply input. (North Side)
+1.8V SerDes Power Supply Input (South Side)	VDDH18_S	P	+1.8V SerDes power supply input. (South Side)
+1.0V SerDes Analog TX/RX Power Supply Input (South Side)	VDDHS_S	P	+1.0V SerDes analog TX/RX power supply input. (South Side)
+1.0V SerDes Analog VCO Power Supply Input (South Side)	VDDHV_S	P	+1.0V SerDes analog Voltage Controlled Oscillator (VCO) power supply input. (South Side)
+1.8V/+3.3V LVCMOS I/O Group A Power Supply Input	VDDO_A	P	+1.8V/+3.3V LVCMOS I/O Group A power supply input.
+1.8V/+3.3V LVCMOS I/O Group B Power Supply Input	VDDO_B	P	+1.8V/+3.3V LVCMOS I/O Group B power supply input.
+1.8V LVCMOS I/O Group Fixed Voltage Power Supply Input	VDDO_18	P	+1.8V LVCMOS I/O group fixed voltage power supply input.
+1.8V 1588 PLL Analog Power Supply Input	VDDA_1588APLL	P	+1.8V PLL Analog power supply input.
Ground	VSS	P	Common ground.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
1588 PLL Analog Ground	**VSSA_1588APLL**	P	PLL analog ground.
+1.8V System PLL Analog Power Supply Input	**VDDA_SYSPLL**	P	PLL analog system.
System PLL Analog Ground	**VSSA_SYSPLL**	P	PLL analog system.
Power Supply Group A Voltage Mode	**VDDO_A_MODE**	LVCMOS In	Used to set the I/O voltage of group A signals. 1 = 3.3V 0 = 1.8V **Note:** If tied high or pulled up, these signals must be connected to 1.8V.
Power Supply Group B Voltage Mode	**VDDO_B_MODE**	LVCMOS In	Used to set the I/O voltage of group B signals. 1 = 3.3V 0 = 1.8V **Note:** If tied high or pulled up, these signals must be connected to 1.8V.

Table 2-4 details the GPIO alternate functions and indicates the default function of each pin (GPIO or alternate).

Note: All GPIOs have an internal pull-up enabled by default. This pull-up can be disabled if not desired.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
General GPIOs				
GPIO32 (Default)	-	-	LVCMOS I/O (4 ma) (PU)	General Purpose Input/Output. Configurable Open-Drain/Push-Pull, configurable polarity. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
GPIO33 (Default)	-	-	LVCMOS I/O (4 ma) (PU)	General Purpose Input/Output. Configurable Open-Drain/Push-Pull, configurable polarity. **Note:** GPIO pins should not be allowed to float. Internal pull-ups are enabled by default.
PHY Management Interface Interrupt Outputs				
GPIO34 (Default)	PHY Interrupt A	**INTR_A**	LVCMOS Out (4 ma)	Programmable PHY interrupt A output. Open-drain, configurable polarity (typically active low).

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO35 (Default)	PHY Interrupt B	**INTR_B**	LVCMOS Out (4 ma)	Programmable PHY interrupt B output. Open-drain, configurable polarity (typically active low).
Fiber Module Management Interface				
GPIO0 (Default)	Port 0 Module Rate Select 0	**PORT0_RATESEL0**	LVCMOS Out (4 ma)	Port 0 rate select 0. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 0 Module Power Down	**PORT0_PDOWN**	LVCMOS Out (4 ma)	Port 0 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 0 Module Reset	**PORT0_RST**	LVCMOS Out (4 ma)	Port 0 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO1 (Default)	Port 0 Module Absent	**PORT0_MOD_ABS**	LVCMOS In (PU)	Port 0 module absent This input indicates if the optical module is attached. 0 = module present
GPIO2 (Default)	Port 0 Module TWI Host Clock	**PORT0_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 0 module management interface clock. Open-drain.
GPIO3 (Default)	Port 0 Module TWI Host Data	**PORT0_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 0 module management interface data. Open-drain.
GPIO4 (Default)	Port 0 Module Transmitter Disable	**PORT0_TX_DIS**	LVCMOS Out (4 ma)	Port 0 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO5 (Default)	Port 0 Module Transmitter Fault	**PORT0_TX_FAULT**	LVCMOS In (PU)	Port 0 TX fault. This GPIO input indicates a laser fault. 1 = fault

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO6 (Default)	Port 0 Module Receiver Loss of Signal	**PORT0_RXLOS**	LVCMOS In (PU)	Port 0 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 0 Module Interrupt	**PORT0_INTL**	LVCMOS In (PU)	Port 0 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO8 (Default)	Port 1 Module Rate Select 0 / Power Down / Reset	**PORT1_RATESEL0**	LVCMOS Out (4 ma)	Port 1 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 1 Module Power Down	**PORT1_PDOWN**	LVCMOS Out (4 ma)	Port 1 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 1 Module Reset	**PORT1_RST**	LVCMOS Out (4 ma)	Port 1 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO9 (Default)	Port 1 Module Absent	**PORT1_MOD_ABS**	LVCMOS In (PU)	Port 1 module absent This input indicates if the optical module is attached. 0 = module present
GPIO10 (Default)	Port 1 Module TWI Host Clock	**PORT1_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 1 module management interface clock. Open-drain.
GPIO11 (Default)	Port 1 Module TWI Host Data	**PORT1_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 1 module management interface data. Open-drain.
GPIO12 (Default)	Port 1 Module Transmitter Disable	**PORT1_TX_DIS**	LVCMOS Out (4 ma)	Port 1 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO13 (Default)	Port 1 Module Transmitter Fault	**PORT1_TX_FAULT**	LVCMOS In (PU)	Port 1 TX fault. This input indicates a laser fault. 1 = fault
GPIO14 (Default)	Port 1 Module Receiver Loss of Signal	**PORT1_RXLOS**	LVCMOS In (PU)	Port 1 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 1 Module Interrupt	**PORT1_INTL**	LVCMOS In (PU)	Port 1 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO16 (Default)	Port 2 Module Rate Select 0 / Power Down / Reset	**PORT2_RATESEL0**	LVCMOS Out (4 ma)	Port 2 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 2 Module Power Down	**PORT2_PDOWN**	LVCMOS Out (4 ma)	Port 2 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 2 Module Reset	**PORT2_RST**	LVCMOS Out (4 ma)	Port 2 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO17 (Default)	Port 2 Module Absent	**PORT2_MOD_ABS**	LVCMOS In (PU)	Port 2 module absent This GPIO input indicates if the optical module is attached. 0 = module present
GPIO18 (Default)	Port 2 Module TWI Host Clock	**PORT2_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 2 module management interface clock. Open-drain.
GPIO19 (Default)	Port 2 Module TWI Host Data	**PORT2_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 2 module management interface data. Open-drain.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO20 (Default)	Port 2 Module Transmitter Disable	**PORT2_TX_DIS**	LVCMOS Out (4 ma)	Port 2 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO21 (Default)	Port 2 Module Transmitter Fault	**PORT2_TX_FAULT**	LVCMOS In (PU)	Port 2 TX fault. This input indicates a laser fault. 1 = fault
GPIO22 (Default)	Port 2 Module Receiver Loss of Signal	**PORT2_RXLOS**	LVCMOS In (PU)	Port 2 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 2 Module Interrupt	**PORT2_INTL**	LVCMOS In (PU)	Port 2 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
GPIO24 (Default)	Port 3 Module Rate Select 0 / Power Down / Reset	**PORT3_RATESEL0**	LVCMOS Out (4 ma)	Port 1 rate select 0 / power down / reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 3 Module Power Down	**PORT3_PDOWN**	LVCMOS Out (4 ma)	Port 3 power down. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
	Port 3 Module Reset	**PORT3_RST**	LVCMOS Out (4 ma)	Port 3 reset. Open-drain, configurable polarity. This output has varied usage based on the optical module type.
GPIO25 (Default)	Port 3 Module Absent	**PORT3_MOD_ABS**	LVCMOS In (PU)	Port 3 module absent This input indicates if the optical module is attached. 0 = module present
GPIO26 (Default)	Port 3 Module TWI Host Clock	**PORT3_TWI_SCL**	LVCMOS I/O (4 ma) (PU)	Port 3 module management interface clock. Open-drain.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO27 (Default)	Port 3 Module TWI Host Data	**PORT3_TWI_SDA**	LVCMOS I/O (4 ma) (PU)	Port 3 module management interface data. Open-drain.
GPIO28 (Default)	Port 3 Module Transmitter Disable	**PORT3_TX_DIS**	LVCMOS Out (4 ma)	Port 3 module transmitter disable / low power mode. Open drain, configurable polarity (typically high). This output is used to shut down the transmitter optical input or place it in a low power mode.
GPIO29 (Default)	Port 3 Module Transmitter Fault	**PORT3_TX_FAULT**	LVCMOS In (PU)	Port 3 TX fault. This input indicates a laser fault. 1 = fault
GPIO30 (Default)	Port 3 Module Receiver Loss of Signal	**PORT3_RXLOS**	LVCMOS In (PU)	Port 3 RX loss of signal. Configurable polarity. This input indicates insufficient optical power for reliable signal reception. The polarity depends on the optical module type.
	Port 3 Module Interrupt	**PORT3_INTL**	LVCMOS In (PU)	Port 3 module interrupt. Typically active low, this input indicates an interrupt request from the module 0 = interrupt
LEDs				
GPIO7 (Default)	Port 0 Link Up LED	**PORT0_LINK_LED**	LVCMOS Out (4 ma)	Line Port 0 Link LED. This signal displays Port 0’s Line Side Link Status. Open-drain, active low.
GPIO36 (Default)	Port 0 Activity LED	**PORT0_ACTIVITY_LED**	LVCMOS Out (4 ma)	Line Port 0 Activity LED. This signal displays Port 0’s Line Side Combined TX/RX Activity. Open-drain, active low.
GPIO15 (Default)	Port 1 Link Up LED	**PORT1_LINK_LED**	LVCMOS Out (4 ma)	Line Port 1 Link LED. This signal displays Port 1’s Line Side Link Status. Open-drain, active low.
GPIO37 (Default)	Port 1 Activity LED	**PORT1_ACTIVITY_LED**	LVCMOS Out (4 ma)	Line Port 1 Activity LED. This signal displays Port 1’s Line Side Combined TX/RX Activity. Open-drain, active low.

TABLE 2-4: GPIO ALTERNATE FUNCTIONS / SYSTEM USAGE (CONTINUED)

GPIO	Alternate Function / System Usage	Symbol	Buffer Type	Description
GPIO23 (Default)	Port 2 Link Up LED	**PORT2_LINK_LED**	LVCMOS Out (4 ma)	Line Port 2 Link LED. This signal displays Port 2's Line Side Link Status. Open-drain, active low.
GPIO38 (Default)	Port 2 Activity LED	**PORT2_ACTIVITY_LED**	LVCMOS Out (4 ma)	Line Port 2 Activity LED. This signal displays Port 2's Line Side Combined TX/RX Activity. Open-drain, active low.
GPIO31 (Default)	Port 3 Link Up LED	**PORT3_LINK_LED**	LVCMOS Out (4 ma)	Line Port 3 Link LED. This signal displays Port 3's Line Side Link Status. Open-drain, active low.
GPIO39 (Default)	Port 3 Activity LED	**PORT3_ACTIVITY_LED**	LVCMOS Out (4 ma)	Line Port 3 Activity LED. This signal displays Port 3's Line Side Combined TX/RX Activity. Open-drain, active low.

TABLE 2-5: STRAP INPUTS

Name	Symbol	Buffer Type	Description
Strap Pins			
Reserved Strap 1	**STRAP_RSVD_1**	LVCMOS In (PD)	Reserved Strap. **Note:** Any tie high or pull-up must be to **VDDO_A.**

2.3 Buffer Types

TABLE 2-6: BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
AI	Analog input
AO	Analog output
CLOCK	Differential clock input
GND	Ground pin
LVCMOS In	LVCMOS input pin
LVCMOS I/O	LVCMOS I/O pin
LVCMOS Out	LVCMOS output pin
LVDS In	LVDS input pin
P	Power pin
PD	Internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
PU	Internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.

3.0 FUNCTIONAL DESCRIPTIONS

The LAN8267 device is a quad-port 1G/10G serial optical Ethernet PHY transceiver which provides multiple Line Port and Host Port options. On the line ports, the LAN8267 supports transmission and reception of data over a variety of serial interfaces. These serial interfaces support both optical modules and copper cables. On the Host Ports, the LAN8267 supports transmission and reception of data over a variety of chip-to-chip and backplane serial interfaces. An integrated Cross-Connect function enables any line port to connect to any host port. Host Redundancy options are provided.

This section includes a functional block diagram, information on the operating modes, and descriptions of the major functional blocks of the LAN8267 device.

3.1 IEEE 802.3 Alignment

The LAN8267 device offers IEEE 802.3-2018 compliance, and is fully compatible with the following interfaces:

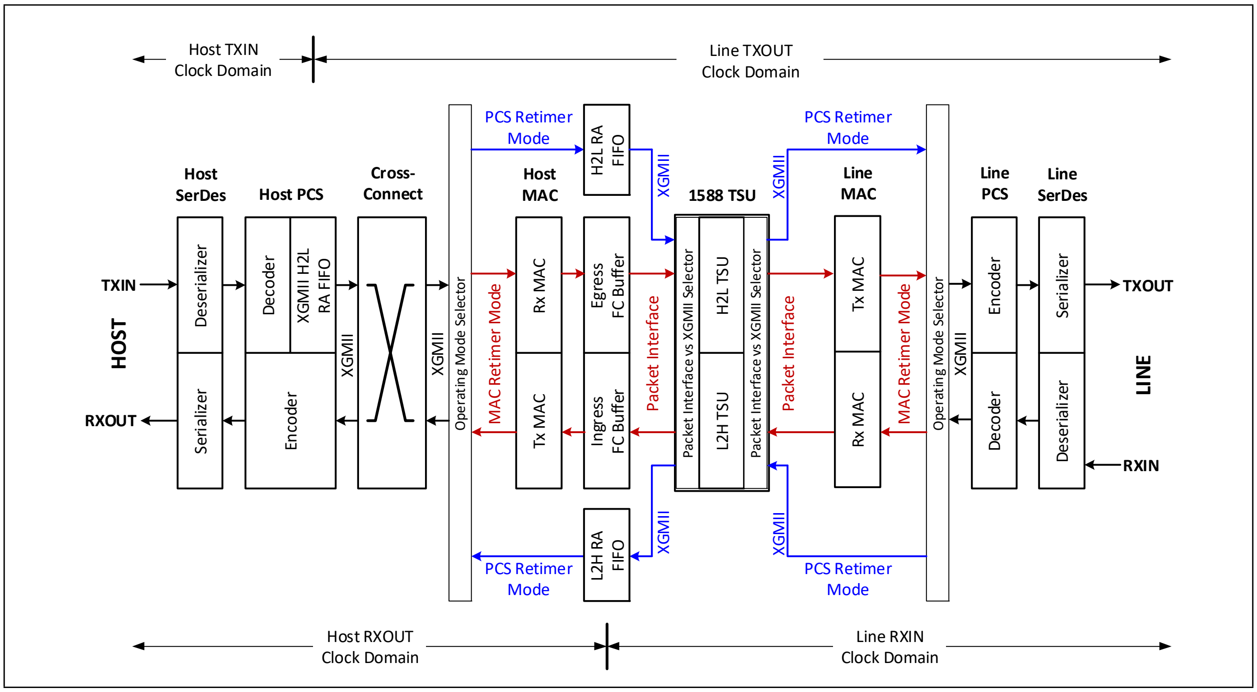
- 10GBASE-KR
- 10GBASE-SR
- 10GBASE-LR
- 10GBASE-ER
- 10GBASE-AOC
- 10GBASE-DAC
- 1000BASE-KX
- 1000BASE-SX
- 1000BASE-LX

3.2 Data Path Overview

The LAN8267 device supports four Host ports and four Line ports, with a Cross-Connect to interconnect any Host with any Line (Host Redundancy options are covered later). Figure 3-1 illustrates the data path where one Line is connected to one Host, and includes the following functions:

- Fully configurable Ethernet PHY on Host and Line
  - Host and Line must be of the same speed (for example, 10G Ethernet), but can be of different formats (for example, KR FEC on Host and no FEC on Line).
  - Host and Line may be fully synchronous or may have PPM clock differences handled by rate adaptation.
- Two Operating modes
  - PCS Retimer, which is a traditional PHY with optional 1588 timestamping
  - MAC Retimer, which is an advanced mode with PHYs and MACs and 1588 timestamping
- IEEE 1588 timestamping and Synchronous Ethernet support
- TSN Frame Preemption support

FIGURE 3-1: LAN8267 DATA PATH



3.2.1 OPERATING MODES

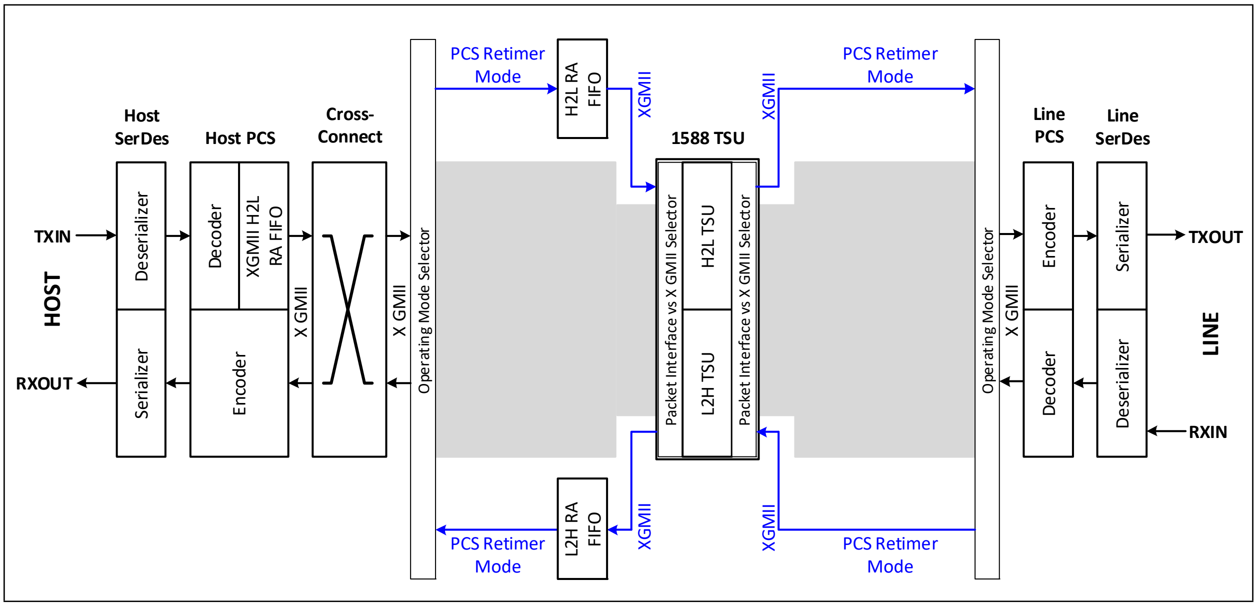
Two basic data path modes are supported, which are selected by the Operating Mode Selectors:

- Ethernet PHY, PCS Retimer: This is a traditional PHY (PCS + SerDes) on both Host and Line, with 1588 TSU also available. MAC functions are not available.
- Ethernet PHY, MAC Retimer: This is the fully featured PHY with 1588 support and uses all data path blocks. Of special note, in this mode, there is both a MAC and a PHY on both the Host and Line ports.

3.2.1.1 Ethernet PHY, PCS Retimer Mode

This mode is essentially a standard Ethernet PHY with 1588 timestamping.

FIGURE 3-2: ETHERNET PHY, PCS RETIMER MODE DATA PATH



Data is received by the SerDes on one side (Host or Line), deserialized, processed by core logic and passed to the opposite side (Line or Host) SerDes. There, the data is serialized and transmitted.

In this mode, the transmit (serializer) clock is required to be the same nominal frequency as the clock recovered from the opposite receiver. PPM clock differences are allowed and are handled by rate adaptation logic (inserting or deleting idles to adapt to the slightly different frequency) associated with the XGMII H2L RA FIFO and the L2H RA FIFO. Each port is retimed to a port clock based on the System reference clock.

Note: Even though the nominal frequency of Line and Host must both be the same, it is possible to use different Ethernet PHY modes. So for example, the Host might be 10GBASE-KR with KR FEC and the Line might be 10GBASE-LR with no FEC.

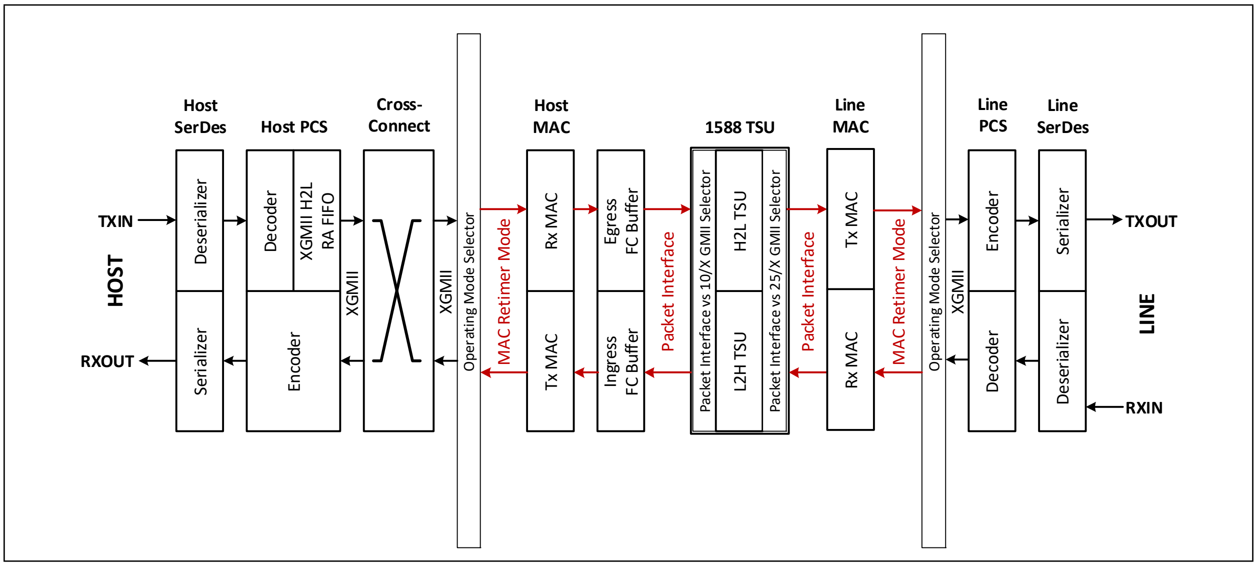
Synchronous Ethernet requires external timing functions, as described in Section 3.8.3.

1588 timestamping support is available in this mode.

3.2.1.2 Ethernet PHY, MAC Retimer Mode

This mode is an advanced Ethernet PHY MACs, supporting 1588 timestamping.

FIGURE 3-3: ETHERNET PHY, MAC RETIMER MODE DATA PATH



MAC Retimer mode is similar to the Ethernet PHY, PCS Retimer mode in that:

- Data is received by the SerDes on one side (Host or Line), deserialized, processed by core logic and passed to the opposite side (Line or Host) SerDes where the data is serialized and transmitted.
- The transmit (serializer) clock is required to be the same nominal frequency as the clock recovered from the opposite receiver. PPM clock differences are supported. Each port is retimed to a port clock based on the System reference clock.
- Synchronous Ethernet and 1588 timestamping are supported.

MAC Retimer mode also provides functions related to IFG, preamble and Pause.

The LAN8267 Host MAC communicates with the Host's MAC.

The LAN8267 MACs may also be used without 1588.

3.2.2 PTP

- PTP may be enabled toward the Line in both PCS Retimer and MAC Retimer operating modes, at any operating speed.

3.2.3 SERDES

The SD25G SerDes supports Ethernet 1 Gbps and 10 Gbps operation by running at 1.25G baud and 10.3125G baud.

3.2.3.1 SD25G SerDes

The SD25G SerDes provides the following operational capabilities:

- RX 5-tap Decision Feedback Equalizer (DFE) to reduce Inter Symbol Interference (ISI). The DFE can operate adaptively or statically.
- RX Continuous Time Linear Equalizer (CTLE) for high-pass filtering.
- RX variable gain control
- RX Loss of Signal and Loss of Lock
- TX 3-tap Feed Forward Equalizer (FFE) for TX de-emphasis to compensate for frequency-dependent channel loss.
- TX output amplitude control

In addition, the SD25G provides the following support capabilities:

- RX Eye Monitor
- Loopbacks in multiple locations (see below and Section 3.2.10, "Loopbacks and Packet BIST").

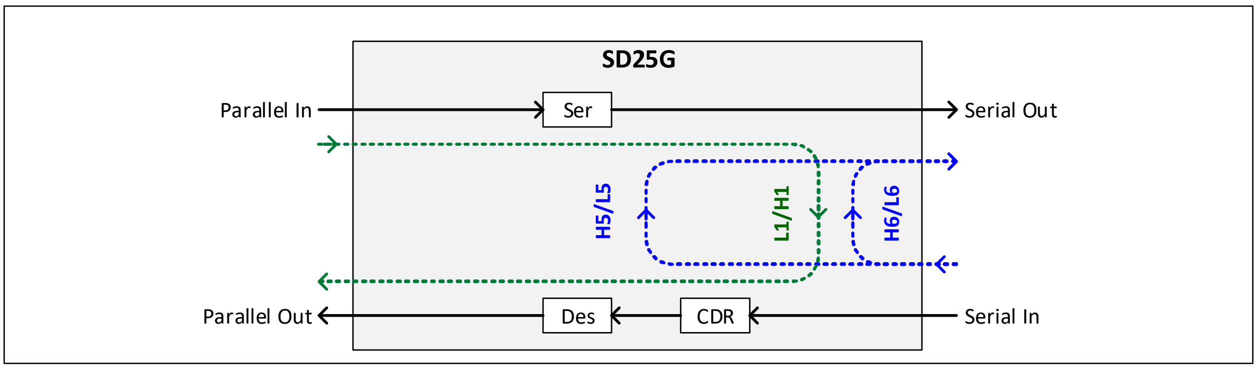
- PRBS generator and checker, supporting PRBS-7, 9, 11, 15, 23 and 31. User-defined patterns are also supported.
- Polarity inversion control

Each CMU receives SYSREFCKP/N as input, and generates the TX_PMA_CK and RX_PMA_CK used by the data path. See Section 3.8.

The SD25G supports the following loopbacks

- LAN8267 H1/L1 Serial Out to Serial In Loopback
  In this loopback the data is internally looped at the SD25G serial interface back toward the LAN8267 core. The internal pma_rx_ck will be synchronous to the pma_tx_ck.
  This loopback is enabled by setting LN_CFG_TX2RX_LP_EN=1 and LN_CFG_TXLB_EN=1.
- LAN8267 H5/L5 Serial In to Serial Out Loopback, post-CDR
  In this loopback the data is internally looped back toward the serial interface. The data is retimed by the CDR but the link partner will still receive the looped data using the same timing that the link partner used to generate the data.
  This loopback is enabled by setting LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXLB_EN=1, and LN_CFG_C-DRCK_EN=1
- LAN8267 H6/L6 Serial In to Serial Out Loopback
  In this loopback the data is internally looped back toward the serial interface without re-timing. The link partner will received the looped data using the same timing that the link partner used to generate the data.
  This loopback is enabled by setting LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXLB_EN=1, and LN_CFG_C-DRCK_EN=0.

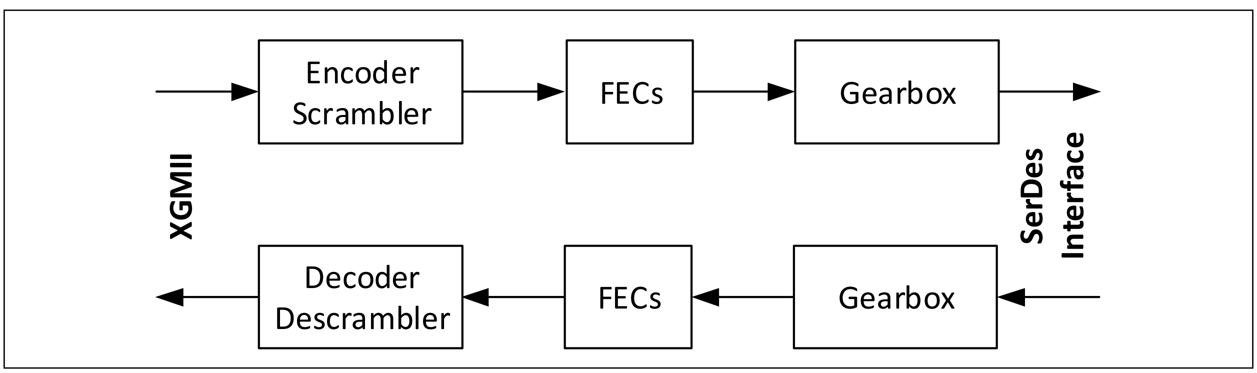
FIGURE 3-4: SD25G LOOPBACKS



3.2.4 PCS25G

The PCS25G block supports a 10G port speed.

FIGURE 3-5: PCS25G BLOCK DIAGRAM



The PCS25G supports the following features and capabilities:

- 10GBASE-R PCS per IEEE 802.3 Clause 49 which connects to an SFP+ / QSFP+ module (which can be optical or direct attach cable). PCS25G also supports Clause 72 10GBASE-KR Backplane Ethernet. Operation is always 10 Gbps and full duplex. KR FEC is available.
- BASE-R FEC per IEEE 802.3 Clause 74
  - Also called KR FEC
- Test Pattern Generator per IEEE 802.3 Clause 49.2.8, and Test Pattern Checker per IEEE 802.3 Clause 49.2.12
- Auto-Negotiation is not supported for the 10G ports other than the Clause 73 Backplane ANEG listed below.
- Bit Error Rate monitoring
- Local Fault detection - A Local Fault is detected by the receiver and indicated onto the XGMII RX interface based upon a loss of link (due to RS-FEC mode loss of alignment). Local Fault is also indicated due to a high Bit Error Rate.

Note the following capabilities are supported external to PCS25G:

- Backplane ANEG is supported per IEEE 802.3 Clause 73 by the KR IP block.

LAN8267 H2/L2 and H3P/L3P Loopbacks. See Section 3.2.10, Loopbacks and Packet BIST for detailed descriptions.

3.2.4.1 KR Forward Error Correction (KR FEC)

The IEEE 802.3 Clause 74 defines a KR Forward Error Correction (KR FEC) sublayer for Base-R PHYs, which is optionally used on a SerDes lane. The KR FEC provides coding gain to increase the link budget and BER (Bit Error Rate) performance.

The KR FEC operates after the PCS on the 66bit datastream.

To enable KR FEC mode,

Set PCS25G_FEC74_CFG.FEC74_ENA_TX=1 and PCS25G_FEC74_CFG.FEC74_ENA_RX=1

3.2.5 1G PCS

The PCS1G supports the following features and capabilities:

- 1000BASE-X PCS per IEEE 802.3 Clause 36, which connects to a 1000BASE-X SFP optical module. PCS1G also supports Clause 70 1000BASE-KX Backplane Ethernet
- 1000BASE-X Auto-Negotiation (ANEG) per IEEE 802.3 Clause 37
  - 1000BASE-LX/SX (optical) ANEG is supported for Pause and Remote Fault Signaling. Operation is always 1 Gbps and full duplex
  - If ANEG is not wanted, software can manually set up the link parameters. For this case SW_RESOLVE_ENA must be set to 1.
- Pattern Generation and Pattern Detect/Check per IEEE 802.3 Annex 36A.1-36A.5, supporting:
  - High frequency test pattern
  - Low frequency test pattern
  - Mixed frequency test pattern
  - Continuous random test pattern with long frames
  - Continuous random test pattern with short frames
- Unidirectional operation per 802.3 Clause 66.
- On the Host side, when MCH is enabled, the preamble must not be shortened due to Idle sequencing. This is controlled by setting SAVE_PREAMBLE_ENA=1.
  - On the Line side, SAVE_PREAMBLE_ENA must always be 0 to ensure 1588 timestamping accuracy.
- If a preamble less than 8 bytes is received, PCS1G will regenerate the full eight-byte preamble. This is enabled using REGEN_PREAMBLE_ENA, which must be set to 1 on both Line and Host to prevent XGMII bus errors.
- Note the following capabilities are performed external to PCS1G:
  - Backplane ANEG per IEEE Clause 73 is supported by the KR IP block
  - The LAN8267 H2/L2 and H3P/L3P Loopbacks. See Section 3.2.10, Loopbacks and Packet BIST for detailed descriptions

When using 1G PCS Retimer mode (no MACs), the minimum IPG might be 5 bytes instead of the required 8 bytes. This is a relatively minor violation as most implementations can accept 5 bytes of IPG. However if compliance is required the MACs can be enabled (MAC Retimer mode) to ensure minimum IPG requirements are met.

3.2.6 CROSS CONNECT

The LAN8267 Cross-Connect supports these system use cases:

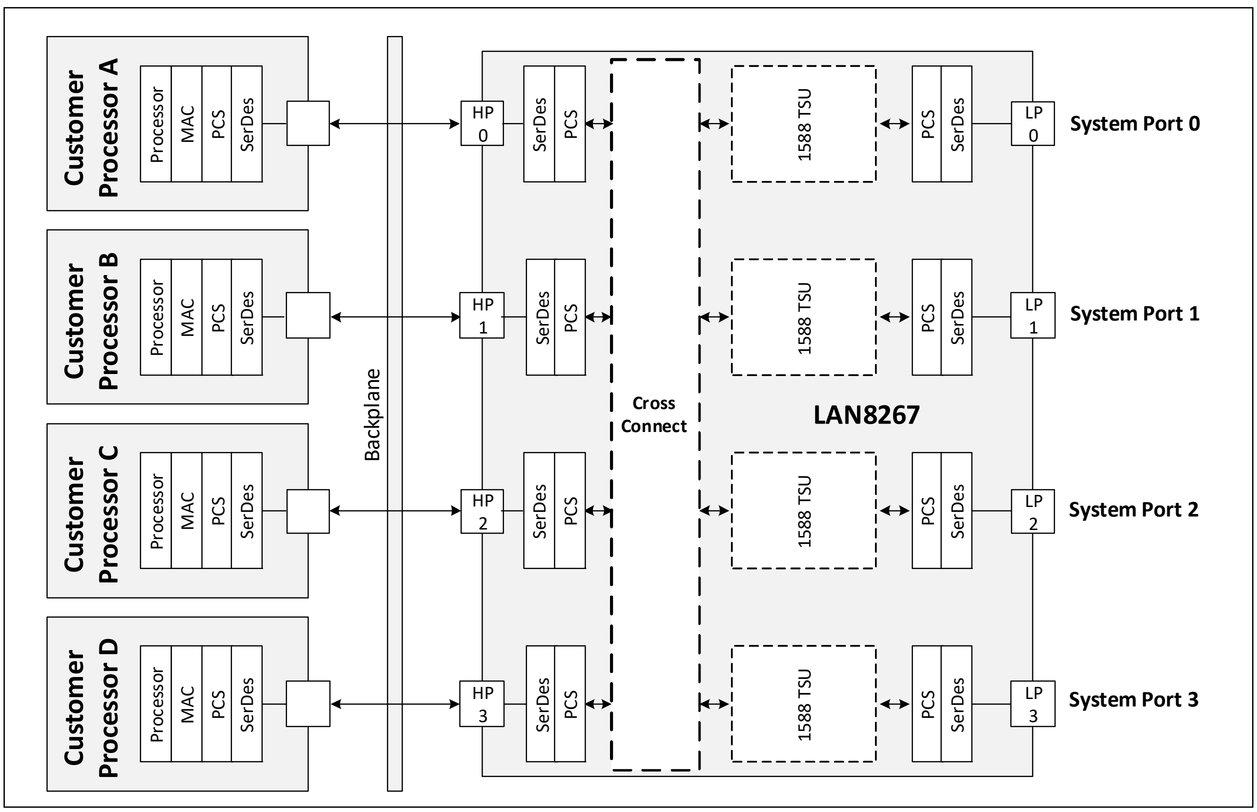
- Any Line to Any Host
- 1:1 Host Protection
- 1+1 Host Protection

3.2.6.1 Any Line to Any Host

Figure 3-6 illustrates the Any Line to Any Host system use case. It shows:

- A LAN8267 having four external Line Ports [0, 1, 2 and 3]
- Four Host System Functions [A, B, C and D] connected to the four LAN8267 Host Ports [0, 1, 2 and 3]. The Cross-Connect enables any-to-any mapping of the four Line Ports [0, 1, 2 and 3] to the four Host System Functions [A, B, C and D]. It is possible to configure the mapping at any time, not just at startup, and also to reconfigure the mapping. However the mappings are considered “static”, meaning they are not expected to change often, and frame flow must be completely stopped on applicable Line and Host Ports during the reconfiguration and then re-enabled. An example scenario:
- Shortly after startup, Line Port 0 is initialized and mapped to Host System Function D (Host Port 3). Line Port 0 and Host Port 3 must be the same port speed.
- Much later, Line Port 1 is initialized and mapped to Host System Function A (Host Port 0). Line Port 1 and Host Port 0 must be the same port speed. Line Port 0 continues to be connected to Host System Function D (Host Port 3) without disruption.
- A while later, Line Port 0 is remapped to Host System Function C (Host Port 2). Frame flow on Line Port 0 will be interrupted during this remapping.

FIGURE 3-6: ANY LINE TO ANY HOST



3.2.6.2 1:1 or 1+1 Host Protection

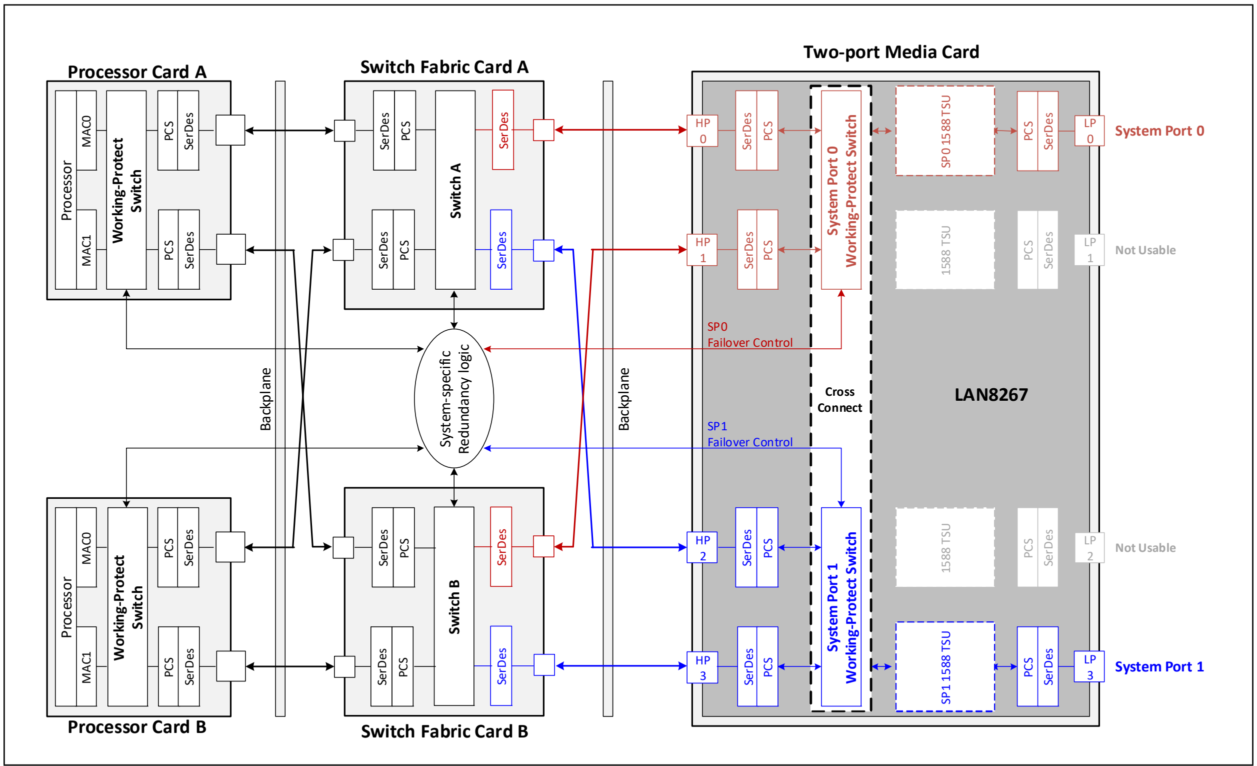
Figure 3-7 illustrates the Host Protection system use cases. It shows:

- A Two-port Media Card consisting of a LAN8267 with two Line Ports and four Host Ports. In this mode only Line Ports 0 and 3 are available for use.
- The Cross-Connect in the LAN8267 implements a Working/Protect Switch for Line Port 0 (W/P Switch 0) and a Working/Protect Switch for Line port 1 (W/P Switch 1).
- A redundant pair of Host System Functions [A and B] connected over a backplane to the four LAN8267 Host Ports [0, 1, 2 and 3].
- System-specific Redundancy Logic which connects to the redundant pair of Host System Functions and the LAN8267.

This system configuration supports the following internal redundancy options:

- 1:1 Host System Function protection, where one Host System Function is actively using both LAN8267 Line Ports, and the other Host System Function is on standby ready to assume active duty in the event of a Host System Function fault.
- 1:1 Host System Function protection, where each Host System Function is actively using one LAN8267 Line Port. In the event of a Host System Function fault, that Host System Function's Line Port will be mapped to the remaining Host System Function.
- 1+1 Host System Function protection, where both Host System Functions are actively connected to the LAN8267 until a failure occurs. In other words, as seen in Figure 3-7, both Host Ports 0 and 1, as well as Host Ports 2 and 3 receive identical copies of each frame flowing between fabric card and the media card

FIGURE 3-7: 1:1 OR 1+1 HOST PROTECTION



3.2.6.2.1 Host Protection Terminology

- Protected connection pair (PCP): two bi-directional serial links (connections) between the LAN8267 and a Host System Function, transporting bi-directional data for a single Line Port. The PCP can protect against a single Active Connection Fault by failing over to the Standby connection.
- 1:1-protected connection pair: a protection scheme where only one bi-directional connection carries data (“is Active” or “is in the Active state”). The other bi-directional connection carries no data (“is Standby” or “is in the

Standby state") but is prepared to take over if the active connection fails ("is Failed" or "is in the Failed state").

- 1+1-protected connection pair: a protection scheme where both bi-directional connections carry data (assuming no Connection Fault) and the receiver selects which connection is Active and which is Standby. If a Connection Fault is detected, that connection becomes Failed and no longer carries data in either direction.
- Connection protect states: Once protection is configured and enabled, each connection may be in one of three protect states: Active, Standby, Failed
  - Active connection: the connection currently being used to transport data. It may be the Default_Active or Default_Standby connection, depending on the connection protect states.
  - Standby connection: the non-failed connection not being used to transport data, backing up the Active connection. It may be the Default_Active or Default_Standby connection, depending on the connection protect states.
  - Failed connection: a connection not capable of transporting data because of a Connection Fault. Either the Default_Active or Default_Standby connection, or even both, may be Failed.
- Default_Active and Default_Standby connections: one of the connections is designated through configuration to be the Default_Active connection, and the other connection is designated through configuration to be the Default_Standby connection.
- Connection Fault: A Hardware-detected fault on a PCP connection. If protection is enabled on the PCP, a Connection Fault will put that connection into the Failed state, and may trigger a W/P Switch failover.
- Failover Control (FC) Signals: Two FC signals connect each LAN8267 W/P Switch to the System-specific Redundancy Logic and implement a "shoot-shot" Failover Control functionality between each W/P Switch (local) and the System specific Redundancy Logic (remote).
- FC Signal Fault: When FC signal use is not disabled, when the W/P Switch initiates a failover, it expects to receive an FC Signal acknowledgment that the System-specific Redundancy Logic has also failed over. If this ACK is not received before the expiration of the configurable FC ACK Timer, an FC Signal Fault interrupt is generated which must be resolved by software. Also when the System-specific Redundancy Logic initiates a failover, the W/P Switch will send an FC Signal acknowledgment that the W/P Switch has also failed over.
- Working/Protect (W/P) Switch: The LAN8267 PCP protection switching hardware. A W/P Switch failover is a data path switching action performed by W/P Switch hardware to ensure the PCP can continue to pass data frames in the event of a single PCP Connection Fault.
- Working and Protect roles: Working and Protect roles must be tracked in software if wanted, the LAN8267 has no knowledge of these roles. The LAN8267 is only aware of Default_Active and Default_Standby roles.

3.2.6.2.2 Hardware W/P Switch Failover

1:1 and 1+1 Hardware W/P Switch Failover are supported as described below.

1:1 Automatic Hardware Protection:

In 1:1 protection in a fully working system each end of the PCP always receives only one copy of each frame.

- When the Default_Active connection is in the Active state the frame copies come over the Default_Active connection. The Default_Standby connection must be either in the Standby or Failed state, and no frames are delivered over the Default_Standby connection.
- When the Default_Standby connection is in the Active state the frame copies come over the Default_Standby connection. The Default_Active connection must be in the Failed state, and no frames are delivered over the Default_Active connection.
- Both the transmit and receive parts of both ends of the PCP use the same Active connection (protection is bidirectional - it is not allowed to use the Default_Active connection in one direction and the Default_Standby connection in the opposite direction except for a short interval during the protection switching operation).
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_Standby connection is in the Standby state, LAN8267 hardware automatically performs a W/P Switch failover to the Default_Standby connection. The Default_Standby connection is now in the Active state and carries frames, while the Default_Active connection is now in the Failed state and does not carry frames. No more hardware failover is possible without further software action, hardware protection is now effectively disabled.
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_Standby connection is in the Failed state, no W/P Switch failover is possible, and no connection can carry frames.

1+1 Automatic Hardware Protection:

In 1+1 protection in a fully working system each end of the PCP receives two copies of each frame, one copy from each connection.

- When the Default_Active connection is in the Active state the frame copies received over the Default_Active connection are used. If the Default_Standby connection is in the Standby state, frames are also delivered over the Default_Standby connection. If the Default_Standby connection is the Failed state, frames are only delivered over the Default_Active connection.
- When the Default_Standby connection is in the Active state the frame copies received over the Default_Standby connection are used. The Default_Active connection must be in the Failed state, and no frames are delivered over the Default_Active connection.
- The receive and transmit parts of both ends of the PCP always use the same Active connection (protection is bidirectional - it is not allowed to use the Default_Active connection in one direction and the Default_Standby connection in the opposite direction except for a short interval during the protection switching operation).
- If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_Standby connection is in the Standby state, LAN8267 hardware automatically performs a W/P Switch failover to the Default_Standby connection. The Default_Standby connection is now in the Active state and carries frames, while the Default_Active connection is now in the Failed state and does not carry frames. Hardware protection switching is now disarmed by hardware.

If a Connection Fault is detected on the Default_Active connection when in the Active state, and the Default_Standby connection is in the Failed state, no W/P Switch failover is possible, and no connection can carry frames.

Connection Fault detection:

Each of these conditions is configurable to be considered a Connection Fault:

- SD25G
  - PLL Loss of Lock
  - Loss of Signal
- PCS25G
  - Link Down
- PCS1G
  - Link Down
  - PCS Sync Status

Connection Fault Detection filtering:

The enabled faults listed above are OR'd and then filtered such that the combined result must be continuously true for a minimum time. Similar, the combined result must be continuously false for a minimum time before a fault indication is cleared.

Software-controlled W/P Switch Failover:

Software may initiate a LAN8267 hardware W/P Switch failover action using W_P_SWITCH_m:WPS_FAILOVER_CTRL:WPS_FORCE_FAILOVER. The W/P Switch failover proceeds as if hardware had detected a Connection Fault, resulting in the applicable W/P Switch being in the [Default_Active/Failed, Default_Standby/Active] state (assuming no Connection Faults, and use of the FC signals is not disabled). No more hardware failover is possible without further software action, hardware protection is now effectively disabled.

FC Signals:

Each W/P Switch utilizes two FC signals as follows:

- FAILOVEROUT indicating a W/P Switch failover was initiated by the LAN8267.
- FAILOVERIN indicating a W/P Switch failover was initiated by the System-specific Redundancy Logic.
- In all use cases, failover initiated at one end of a PCP must be signaled to the other end of the PCP (if use of FC signals is enabled), triggering a partner failover. The partner must signal back to the initiator that the failover was executed.
  - Software is able to read the status of both FC signals at W_P_SWITCH_m:WPS_STATUS:WPS_FLOVR_CTRL_STS[1:0]
  - It is possible to disable use of the FC signals at W_P_SWITCH_m:WPS_FAILOVER_CONTROL:FC_SIGNAL_DISABLE
  - If FC signal use is not disabled, each end of the PCP accepts the FC signal input from the partner and uses it as described above. In this case, the partner is able to directly initiate a local W/P Switch failover, and the partner must not complete any failover until it receives an acknowledgment back from the local W/P Switch.
    - The W/P Switch acknowledgment wait time is configurable at W_P_SWITCH_m:WPS_FAILOVER_CONTROL:FC_ACK_TIMER

- If FC signal use is disabled, the local W/P Switch does not accept the FC signal input from the partner. In this case, the partner is not able to directly initiate a local W/P Switch failover (indirect triggering is still possible through software), and the partner completes any failover without needing an acknowledgment back from the local W/P Switch. The local W/P Switch will also not look for the acknowledgment from the partner.

FC Signal Fault detection:

An acknowledgment from the partner is received by the local W/P Switch (if use of FC signals is not disabled). In the event that the local W/P Switch failed over but does not receive an acknowledgment from the partner, an interrupt is generated (if enabled) providing FC Signal Fault detection.

Interrupts:

The WPS_CONN_FAULT_INTR_m interrupt is generated (if enabled) when a Connection Fault is detected on the Default_Active connection.

The WPS_FC_ACK_TIMER_INTR_m interrupt is generated (if enabled) if a FC Signal Fault is detected (if use of FC signals is not disabled).

- The WPS_FAILOVER_INTR_m interrupt is generated (if enabled) whenever a W/P Switch failover occurs.

Interrupts also exist on all Host and Line Ports covering fault cases of interest. These interrupts are not part of the W/P Switch design, but are still available when hardware protection is enabled. One expected use of these interrupts is to notify software of a Standby connection failure (which is not monitored by the W/P Switch hardware).

3.2.7 1588 TSU

The TSU supports the implementation of the Precision Time Protocol (PTP) defined in IEEE 1588-2019 and IEEE 802.1AS-2020 in PHY hardware by providing a mechanism for timestamp update. IEEE 802.1AS is a profile of IEEE 1588 and, when referring to PTP, no distinction is made unless explicitly stated.

The TSU block works with other blocks to identify PTP messages, process these messages and insert accurate time-stamps where necessary. For IEEE 1588 timing distribution, LAN8267 supports ordinary clocks, boundary clocks, end-to-end transparent clocks and peer-to-peer transparent clocks in a chassis based IEEE 1588 capable system. One-step and two-step processing is also supported. For IEEE 802.1AS timing distribution LAN8267 supports PTP End Stations and PTP Relay Stations using 2-step operation. For details on the timing protocols, refer to IEEE 1588-2019 and IEEE 802.1AS-2020. The TSU block implements part of the functionality required for full IEEE 1588/802.1AS compliance.

LAN8267 supports two basic 1588 operating modes:

- 1588 Standalone Mode: The TSU supports full classification and full 1588 processing. This mode is to be used where the host device is not an advanced Microchip switch capable of operating with the MCH header.
- 1588 MCH Mode: No classification and only limited 1588 processing is available. This mode is to be used where the host device is an advanced Microchip switch capable of operating with the MCH header.

The TSU supports two different data path interfaces, aligning with the two LAN8267 Operating Modes

- X GMII interface, used in PCS Retimer mode. The X GMII carries the frame CRC (FCS or mCRC) as well as pre-amble/SFD/SMD (1588 Standalone Mode) or MCH (1588 MCH Mode).
- • Packet Interface, used in MAC Retimer Mode. The Packet Interface carries frame preemption controls as well as the MCH (1588 MCH Mode), but does not carry the frame CRC or preamble/SFD/SMD (1588 Standalone Mode).

The TSU can also be configured to have data bypass the timestamping function.

3.2.8 MAC

The MAC is used on both the Line and Host side, and consists of the following major sub-functions:

- MAC Kernel supporting traditional 802.3 MAC layer functions
- MAC Merge supporting 802.3 Frame Preemption functions
- Packet Interface Wrapper which implements the Packet Interface
- Port Statistics supporting p-MAC and e-MAC statistics per 802.3

3.2.8.1 MAC Kernel

The TX MAC Kernel performs the following tasks:

- Implement IEEE 802.3 Reconciliation Sublayer function
- Calculate and insert the CRC for all frames including CRC corruption for error cases.
- Convert frames received from the MAC Host Port to X GMII format which includes adding appropriate framing

control characters and FCS
  - Note in this case “MAC Host Port” refers to the interface between the MAC Kernel and the MAC Merge blocks
  - [MCH disabled] Preamble is passed transparently though the MAC Kernel
  - [MCH enabled] MCH is passed transparently through the MAC Kernel
- Generate the interframe gap (IFG) on the X GMII using the IEEE 802.3 Deficit Idle Count (DIC) algorithm to achieve an average IFG of 12 bytes
- Maintain TX statistics counters located in the Port Statistics function
- Support Link Fault Signaling (LFS, IEEE 802.3 clause 46.3.4) and Unidirectional Ethernet (IEEE 802.3 clause 66.4). Since LAN8267 has a MAC (not a normal PHY function), the LF/RF ordered sets can be terminated either by outside MAC or the Line MAC.
  - If it is desired that the LAN8267 Line MAC is to handle LFS [LFS Line Side Mode], then the Line MAC's LFS_MODE_ENA must be set to 1, and LF_RELAY_ENA and RF_RELAY_ENA must both be set to 0. These registers must all be set to 0 on the Host MAC.
  - If the customer system MAC is to handle LFS [LFS Transparent Mode], then LFS_MODE_ENA must be set to 0 on both Host and Line MAC, and LF_RELAY_ENA and RF_RELAY_ENA must be set to 1 on both Host and Line MAC.
  - Unidirectional operation is independent of LFS handling, and is configured using LFS_UNIDIR_ENA.
  - The MAC can be controlled to generate LF or RF using force_lf_i or force_rf_i.

The RX MAC Kernel performs the following tasks:

- Implement IEEE 802.3 Reconciliation Sublayer function
- Calculate and check the CRC of each frame for validity and abort mark any frame with an invalid CRC
- Convert frames received in X GMII format into the MAC host format which includes removing the framing control characters
  - Note in this case “MAC Host Port” refers to the interface between the MAC Kernel and the MAC Merge blocks
  - [MCH disabled] Preamble is passed transparently through the MAC Kernel
  - [MCH enabled] MCH is passed transparently through the MAC Kernel
- Perform a variety of length checks including looking for runt frames (less than 64 bytes), oversized and jabber frames (longer than the configured maximum). Length checks are supported for frames with up to four VLAN tags.
- Maintain RX statistics counters located in the Port Statistics function
- Support LFS if enabled (see TX MAC Kernel description)
  - When the MAC detects LF or RF it asserts lf_received or rf_received

VLAN tag support:

- Up to four VLAN tags, where VLAN tags can occur in any order (any enabled TPID value can exist in any of the up to four VLAN tag locations and the same TPID value can exist in multiple VLAN tag locations)
- Native understanding of the standard Tag Protocol ID (TPID) values for C-tag (0x8100) and S-tag (0x88A8)
- Two configurable TPID values beyond the standard values

3.2.8.2 MAC Merge

The TX MAC Merge function implements the Frame Preemption Transmit Processing State Diagram of IEEE 802.3-2018. If MCH is disabled it encodes the SMDx accordingly for preamble modification. If MCH is enabled it updates the MCH accordingly including updating the MCH CRC - note the MCH was inserted by the 1588 TSU

The RX MAC Merge function implements the Frame Preemption Receive Processing State Diagram of IEEE 802.3-2018. This block performs frame count & fragment count checks for proper reassembly. If MCH is disabled, preemption functions are based on the SMDx. If MCH is enabled, preemption functions are based on the MCH which includes verifying the MCH CRC. Note in LAN8267 the fragments are never actually reassembled into complete frames. In case of a fragment count mismatch or FCS error, it asserts an error indication (note a mismatched mCRC is not an error rather it indicates the CRC is actually an FCS). If the MCH is present it is passed unmodified as packet data to the Packet IF.

The Verify Respond function implements the Verify and Respond State Diagrams of IEEE 802.3-2018.

3.2.8.3 Packet Interface Wrapper

The Packet Interface Wrapper handles the following functions:

- Provide a Packet Interface to FC Buffer blocks. On this Packet Interface, frames are transported without Preamble, SFD/SMD, and CRC.

- [MCH disabled] Preamble and SFD/SMD are stripped from frames toward the Packet Interface, and are added to frames received from the Packet Interface.
- [MCH enabled] The MCH is sent as part of the packet toward the Packet Interface, and received as part of the packet from the Packet Interface.
- For frames heading toward the Packet Interface, the CRC is already checked by the Rx MAC Kernel. The Wrapper strips the CRC and also passes along the CRC error indication from the Rx MAC Kernel to the Packet Interface.
- For frames arriving from the Packet Interface, the Wrapper inserts a dummy CRC at the end of the frame and performs any padding if needed. The Tx MAC Kernel updates the dummy CRC. For frames requiring a corrupt CRC, Wrapper signals the Tx MAC Kernel to corrupt the CRC. A CRC corruption scheme is supported and configurable in the tx MAC kernel:
  - CRC Inversion. The CRC is calculated and inverted.

- [Host Packet IF Wrapper] Process the Egress Host Interface Format bytes as applicable toward the Rx MAC Packet Interface. Generate the Ingress Host Interface Format bytes as applicable toward the Tx MAC Kernel.
- If an error condition is detected, discard and count the errored frame.

3.2.8.4 Port Statistics

The following counters count the number of bytes or frames received or transmitted. The counters count continuously and are only cleared if the device is reset or the counter is written with 0 through the CPU interface. These counters wrap continuously, rolling over to 0 when the maximum value is reached.

Unless specified otherwise, each counter is 32 bits.

- RX_IN_BYTES_CNT (64 bits) counts the total bytes received including preamble
- RX_OK_BYTES_CNT (64 bits) counts the number of bytes received in valid frames
- RX_BAD_BYTES_CNT counts the number of bytes received in invalid frames
- TX_OUT_BYTES_CNT (64 bits) counts the total number of bytes transmitted including preamble
- TX_OK_BYTES_CNT (64 bits) counts the number of bytes in successfully transmitted frames

The following counters are based on the type of frame received or transmitted:

- RX_PAUSE_CNT counts the number of pause frames received
- RX_UNSUP_OPCODE_CNT counts the number of control frames received with unsupported opcodes
- RX_UC_CNT counts the number of unicast frames received
- RX_MC_CNT counts the number of multicast frames received
- RX_BC_CNT counts the number of broadcast frames received
- TX_PAUSE_CNT counts the number of pause frames transmitted
- TX_UC_CNT counts the number of unicast frames transmitted
- TX_MC_CNT counts the number of multicast frames transmitted
- TX_BC_CNT counts the number of broadcast frames transmitted

The following error counters are provided:

- RX_SYMBOL_ERR_CNT counts the number of symbol errors received
- RX_CRC_ERR_CNT counts the number of frames received with CRC errors
- RX_UNDERSIZE_CNT counts the number of undersized frames received with valid CRC
- RX_FRAGMENTS_CNT counts the number of undersized frames received with invalid CRC
- RX_IN_RANGE_LENGTH_ERR_CNT counts the number of frames where the length field does not match the frame length
- RX_OUT_OF_RANGE_LENGTH_ERR_CNT counts the number of frames with an illegal length field
- RX_OVERSIZE_CNT counts the number of oversize frames with valid CRC
- RX_JABBERS_CNT counts the number of oversize frames with an invalid CRC
- RX_XGMII_PROT_ERR_CNT counts the number of XGMII protocol errors detected.

The following size histogram counters are provided for both transmit and receive directions:

- Frames with 64-byte payloads
- Frames with 65-byte to 127-byte payloads
- Frames with 128-byte to 255-byte payloads

- Frames with 256-byte to 511-byte payloads
- Frames with 512-byte to 1023-byte payloads
- Frames with 1024-byte to 1518-byte payloads
- Frames with 1519-byte to maximum size payloads

Frame size counters also count invalid frames, as long as they are not short frames, fragments, long frames, or jabber frames. Long frames are defined as those greater than MAX_LEN bytes. The above counters are all 32 bits unless otherwise noted, and all counters wrap.

3.2.9 FLOW CONTROL BUFFER

The Flow Control Buffer provides:

- Buffering from the Host and Pause generation toward the Host to accommodate 1588 latency control and receipt of Pause frames from the Line.
  - Pause generation toward the Host is configurable based on XON/XOFF thresholds.
  - Cut-through operation
- Special handling of MAC Control Frames which must pass from Host to Line bypassing the FC Buffer.
  - Control frames are buffered in a dedicated queue which has strict priority scheduling over the normal data frame queue, and are not stopped due to receipt of Pause frames from the Line

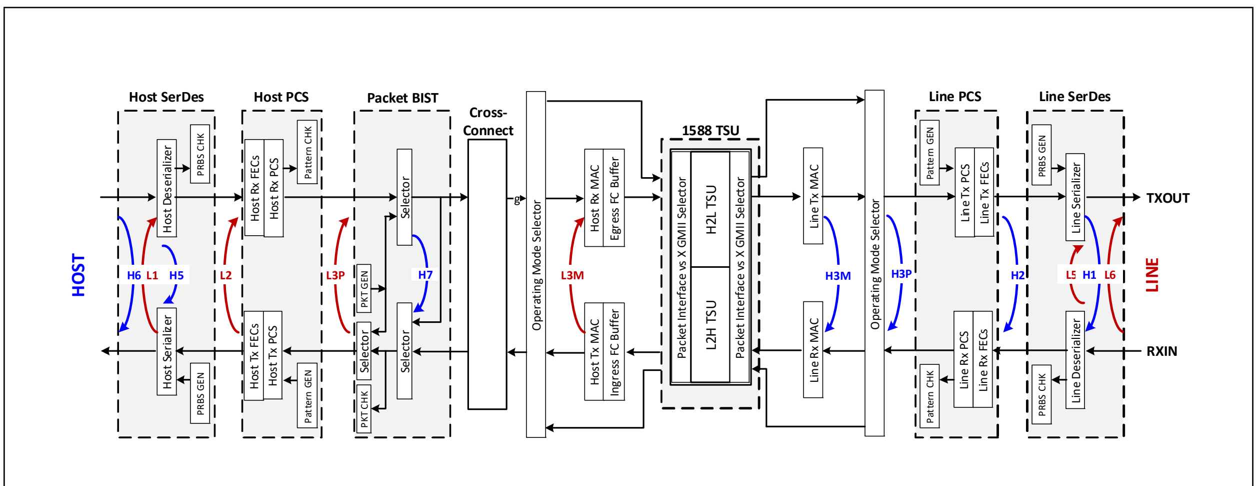
The ingress_fc_buffer provides:

- Buffering toward the Host to allow Pause frame insertion toward the Host.
  - IFG shrink is available if enabled and if necessary to provide some speedup toward the Host to compensate for Pause frame insertion.
  - Cut-through operation

3.2.10 LOOPBACKS AND PACKET BIST

LAN8267 supports loopbacks and data plane BIST as shown in Figure 3-8.

FIGURE 3-8: LOOPBACKS AND DATA PLANE BIST



3.2.10.1 Loopbacks

Loopback details are provided in Table 3-1.

TABLE 3-1: LOOPBACKS

LB Name	Description	Applicable Registers
H1/L1	H1: Line SerDes TXOUT to RXIN Serial LB L1: Host SerDes RXOUT to TXIN Serial LB	Set both LN_CFG_TX2RX_LP_EN=1 and LN_CFG_TXLB_EN=1 HOST_PMA_EXT : LANE_GRP_0:LANE_04.LN_CFG_TX2RX_LP_EN and HOST_PMA_EXT :LANE_GRP_0:LANE_19.LN_CFG_TXLB_EN
H2/L2	H2: Line PCS PMA-Side LB back toward XC L2: Host PCS PMA-Side LB back toward XC Loopback comes after all FEC functions Clock is looped, no Rate Adaptation performed H2/L2 Loopbacks also provide these options: • Forward packets to the SerDes • Block packet forwarding to the SerDes and instead send zeros to the SerDes • Block packet forwarding to the SerDes and instead send 00FF pattern to the SerDes	HOST_SLICE:HOST_P-MA_PCS_LPBK:L2_LPBK:L2_LPBK LINE_SLICE:LINE_P-MA_PCS_LPBK:H2_LPBK:H2_LPBK
H3P/L3P	H3P: Line PCS Core-Side LB back toward XC L3P: Host PCS Core-Side LB back toward XC Clock is looped, Rate Adaptation is performed H3P/L3P Loopbacks also provide these options: • Forward packets to the PCS • Block packet forwarding to the PCS and instead send XGMII Idles to the PCS	HOST_SLICE:HOST_P-MA_PCS_LPBK:L3P_LPBK:L3P_LPBK LINE_SLICE:LINE_P-MA_PCS_LPBK:H3P_LPBK:H3P_LPBK
H3M/L3M	H3M: Line MAC PCS-Side LB back toward XC L3M: Host MAC PCS-Side LB back toward Line	(H3M) LINE_MAC_LB_CFG:XGMII_HOST_LB_EN (L3M) HOST_MAC_LB_CFG:XGMII_HOST_LB_EN
H5/L5	H5: Host SerDes RXIN to TXOUT Serial LB L5: Line SerDes RXIN to TXOUT Serial LB	Set all LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXL-B_EN=1, and LN_CFG_CDRCK_EN=1
H6/L6	H6: Host SerDes RXIN to TXOUT Serial LB L6: Line SerDes RXIN to TXOUT Serial LB	Set all LN_CFG_RX2TX_LP_EN=1, LN_CFG_RXL-B_EN=1, and LN_CFG_CDRCK_EN=0.
H7	H7: Packet BIST Core-Side LB toward Host L7: N/A - does not exist H7 supports both Packet BIST operations as well as Host PCS Core-Side LB back toward Host.	HOST_SLICE:PKTBIST_DATAPATH_CONTROL: IGR_XGMII_PG_SEL2

3.2.10.2 Data Plane BIST

LAN8267 supports the following data plane BIST:

- SD25G PRBS Generator and Checker.
- PCS1G Pattern Generator and Checker.
- PCS25G Pattern Generator and Checker.
- PKT_BIST Packet Generator and Checker, described below.

The Packet BIST consists of a Packet Generator, Packet Checker, and data path selectors. The data path selectors implement the LAN8267 H7 Loopback, which supports the Packet BIST functions but can also be used as a general-purpose data path loopback supporting all ports speeds.

The **Packet Generator** generates configurable X GMII Ethernet frames, either toward the Cross Connect or toward the Host PCS. The Packet Generator supports the following features:

- Standard Packet or PTP Packet, with some amount of programmable fields.
- Standard Ethernet frame with Preamble and FCS. Advanced features such as P-frames/fragments and MCH are not supported.
- Standard Packet payload is always PRBS31, packet length is configurable.
- PTP Packet payload is a mix of Fixed and Configurable fields, always a 64 Byte Ethernet frame, which includes two bytes of padding but does not count the 8 Bytes of preamble.
- When not sending Ethernet frames it sends Idles. It can also send a constant stream of Idles.
- Provides a count of Packets Sent
- Standard Packet Length, IPG, and lane alignment to X GMII bus are all configurable
- Support added for IEEE 1588-2019 format

Table 3-2 shows the fixed and configurable fields for generating a Standard Packet.

TABLE 3-2: PACKET GENERATOR STANDARD PACKET

Field	Bits	Content
Preamble	64	0xFB555555555555D5[1]
Destination Address	48	Configurable
Source Address	48	Configurable
EtherType	16	Configurable
PRBS31	Variable	Continuous 2^31-1 pattern
FCS	32	Standard Ethernet CRC-32
Terminate	8	0xFD[2]

Note 1: The “FB” becomes a “55” when transmitted on the network.
2: The “Terminate” is an internal indication and is not transmitted on the network.

Table 3-3 shows the fixed and configurable fields for generating a PTP Packet.

TABLE 3-3: PACKET GENERATOR PTP PACKET

Field	Bits	Content
Preamble	64	0xFB555555555555D5[1]
Destination Address	48	Configurable
Source Address	48	Configurable
EtherType	16	0x88F7
transportSpecific (v2) **majorSdoId (v2.1)**	4	Configurable
messageType	4	0x0
versionPTP	4	0x2
reserved (v2) **minorVersionPTP (v2.1)**	4	Configurable
messageLength	16	0x002C
domainNumber	8	0x00
reserved (v2) **minorSdoId (v2.1)**	8	Configurable
flagField	16	0x0000
correctionField	64	Configurable
reserved (v2) **messageTypeSpecific (v2.1)**	32	Configurable
sourcePortIdentity	80	0x00000000000000000000
sequenceId	16	Increments with each PTP packet

TABLE 3-3: PACKET GENERATOR PTP PACKET (CONTINUED)

Field	Bits	Content
controlField	8	0x00
logMessageInterval	8	0x7F
originTimestamp	80	Lowest 16 bits are configurable
pad	16	0x0000[2]
FCS	32	Standard Ethernet CRC-32
Terminate	8	0xFD[3]

Note 1: The “FB” becomes a “55” when transmitted on the network.
2: The PRBS is not used for PTP frames.
3: The “Terminate” is an internal indication and is not transmitted on the network.

For PTP packets, the Packet Generator will send a configurable number of Standard Packets in between each PTP Packet, and the sequenceid will increment with each PTP Packet sent.

The Packet Checker monitors incoming X GMII Ethernet frames arriving from one of three places:

- The Cross-Connect (LAN8267 ingress direction)
- The Host RX PCS (LAN8267 egress direction)
- The Packet Generator (mainly useful as a Packet BIST self-test)

The Packet Checker supports the following features:

- Counts Ethernet frames received with correct FCS
- Counts Ethernet frames received with incorrect FCS
- Counts PRBS31 bit errors
- Counts Ethernet frame fragments received
- Counts Local Fault (LF) ordered sets received in IPG
- Captures the 80-bit originTimestamp from the 10 most recently received PTP Packets

The Packet Generator and Checker provides basic test capabilities covering the following:

- PCS and SerDes: Runs at rate and covers all speeds, FECs, and datapaths (e.g. PCS Retimer and MAC Retimer).
  - No coverage of ANEG or KR Training
- Cross-Connect
- PTP TSU and Timestamping: Checks that basic PTP is configured and running properly.
  - Many encapsulations and advanced timestamping functions are not covered.
  - 1588-2088 (v2) and 1588-2019 (v2.1) can both be generated and checked.
  - Looped frames can also be passed through to the outside system to verify formatting is as expected.

Frame Preemption cannot be tested. Only e-Frames can be generated or checked.

3.3 Frame Preemption Verify/Respond System Operation

As described in 802.3, frame preemption is enabled in the transmit direction only if it is determined that the Link Partner supports the preemption capability. This is a two-step process:

1. Discovery. Link Partner preemption capability is advertised using the Additional Ethernet Capabilities TLV in an LLDPDU addressed to the Nearest Bridge group address (see IEEE Std 802.1Q).
2. Verification. Frame preemption capability is verified using the Verify/Respond protocol, executed by the MAC Merge functions at each end of the link. The MAC Merge function initiates verification by sending a verify mPacket, expecting receipt of a respond mPacket to confirm that the Link Partner supports frame preemption.

Without an intervening LAN8267, the MAC Merge function in the customer system Host MAC would communicate directly with the MAC Merge function in the Link Partner Line MAC to verify frame preemption capability.

With an intervening LAN8267 operating in MAC Retimer mode, two additional MAC Merge functions are introduced: one in the LAN8267 Host MAC and the other in the LAN8267 Line MAC.

LAN8267 supports two Frame Preemption Verify / Respond options toward the Line Port:

- Verify / Respond Line Side Mode

The MAC Merge function in the LAN8267 Line MAC executes the Verify / Respond protocol for the system. The customer system must read the result from the LAN8267 Line MAC and configure its own Host MAC accordingly.

- Verify / Respond Transparent Mode
  The MAC Merge function in the customer system Host MAC executes the Verify / Respond protocol for the system. Verify and Respond mPackets are passed transparently through the LAN8267 in both directions. The customer system Host MAC and Link Partner Line MAC resolve the verification state, and must configure all MACs accordingly.

Once preemption verification is complete, operation is the same regardless of which Verify/Respond mode was used:

- If preemption is enabled in MAC Retimer mode fragments are passed through the LAN8267 in both directions, but are checked for proper formatting.
- If preemption is disabled in MAC Retimer mode the LAN8267 will filter fragments received from the Line. The LAN8267 will pass fragments received from the Host but they should not occur in a proper configuration.
- In PCS Retimer mode fragments are passed through the LAN8267 transparently in both directions.

Frame Preemption verification should not be performed between the Host and the LAN8267 Host MAC.

3.4 Link Fault Signaling System Operation

Link Fault Signaling (LFS) provides fault detection and reporting for 10G links per 802.3 clause 46.3.4. Two types of link fault are detected and reported by the Reconciliation Sublayer (RS), which is part of the MAC:

- Local Fault (LF): a receive fault which is between the link partner RS and the local RS
- Remote Fault (RF): a transmit fault which is between the local RS and the link partner RS

Without an intervening LAN8267, the RS function in the customer system Host MAC would communicate fault status directly with the RS function in the Link Partner Line MAC.

With an intervening LAN8267 operating in MAC Retimer mode, two additional RS functions are introduced: one in the LAN8267 Host MAC and the other in the LAN8267 Line MAC.

LAN8267 supports two LFS options toward the Line Port:

- LFS Line Side Mode
  The RS function in the LAN8267 Line MAC executes the LFS protocol for the system. LF/RF symbols from the Line Port are terminated in the Line MAC, LF/RF symbols from the Host Port are terminated in the Host MAC.
- LFS Transparent Mode
  The RS function in the customer system Host MAC executes the LFS protocol for the system. The LAN8267 transparently passes the LF and RF symbols between Line and Host Ports.

In PCS Retimer mode the LAN8267 passes the LF and RF symbols between Line and Host Ports.

3.5 Flow Control System Operation

3.5.1 PAUSE HANDLING AND FLOW CONTROL

The LAN8267 supports all the following Flow Control capabilities in MAC Retimer mode:

- Options for handling Pause from Line MAC partner:
  - React at the Egress Flow Control Buffer output
  - React at the TX Line MAC
  - Do not react to Pause in LAN8267, pass the Pause frame to the Host
- Internal flow control to the Egress Flow Control Buffer from the TX Line MAC block
- Forwarding Pause from the Host to the TX Line Port
  - LAN8267 never generates Pause to the Line Port

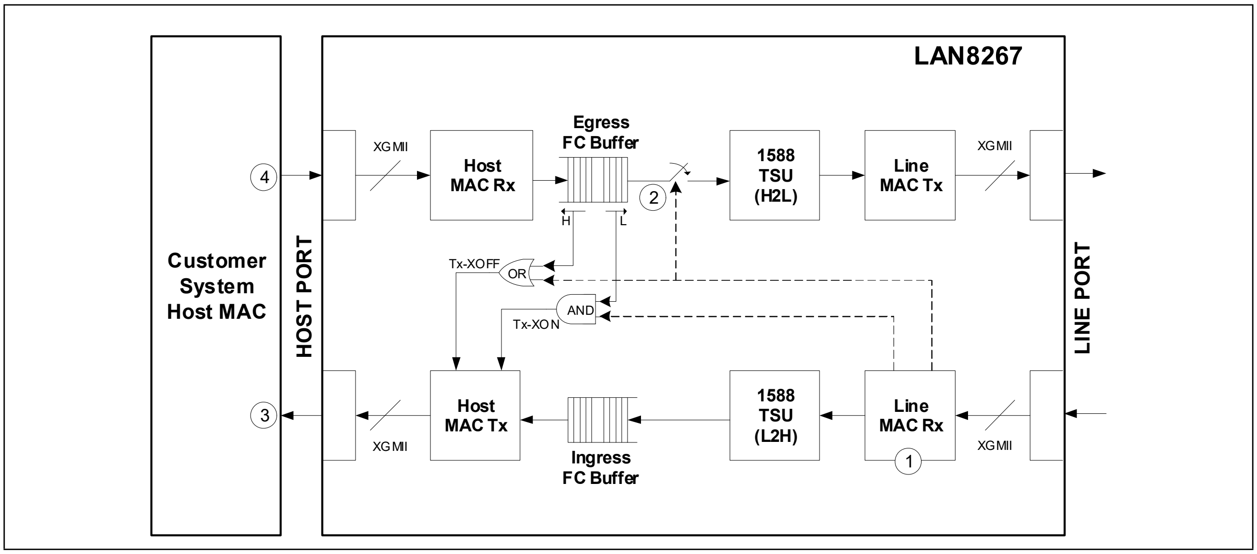
3.5.2 BASIC FLOW CONTROL HANDLING

"Basic Flow Control" in this section describes:

- Receiving Pause from the Line MAC partner and reacting to it at the Egress FC Buffer output
- Generating Pause toward the Host due to filling of the Egress FC Buffer.
- Forwarding Pause from the Host to the TX Line Port.

Figure 3-9 illustrates Basic Flow Control operation when a pause frame is received from the Line:

FIGURE 3-9: BASIC FLOW CONTROL, PAUSE FROM THE LINE



Follow the tags 1, 2, 3, 4 in the figure.

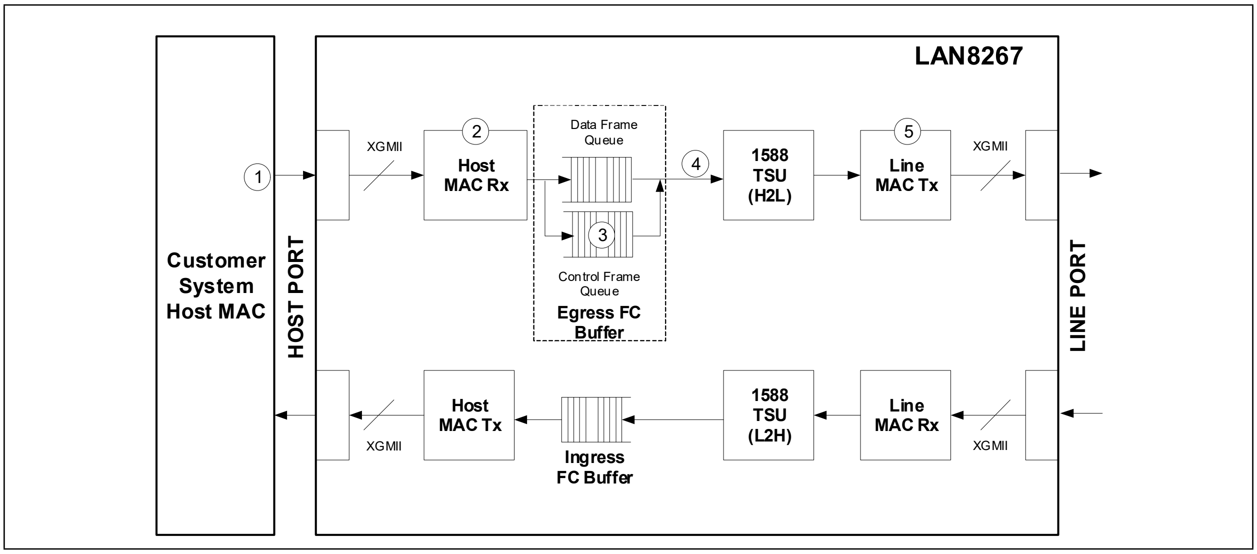
1. A pause frame (XOFF) is received by the LAN8267 Line MAC RX. This frame is internally consumed by the Line MAC. The Line MAC RX signals the Egress FC Buffer indicating Pause was received and providing the Pause quanta.
2. The Egress FC Buffer goes into the Pause state at the next TX frame boundary. The Pause Timer is maintained by the Egress FC Buffer and is started only after it goes into the Pause state. In the worst case, the Egress FC Buffer may immediately go into the Pause state. Hence, the Egress FC Buffer drain rate is 0 and the fill rate can be the full Host Port speed. The Egress FC buffer will signal XOFF to the Host MAC TX ASAP to schedule a pause transmission toward the Host. This signaling is shown via the optional “OR” gate.
3. The LAN8267 Host MAC TX can schedule a pause frame for transmission toward the Host at the next RX frame boundary. In the worst case, the LAN8267 Host MAC TX has just started transmitting a jumbo frame toward the Host. During this time the Egress FC Buffer is continuing to receive frames from the Host. The Egress FC Buffer must have the capability to hold at least one Jumbo frame until the XOFF pause frame is received by the customer system Host MAC.
4. It is possible that the customer system Host MAC may have started transmitting a jumbo frame toward the Egress FC Buffer. So the Egress FC Buffer must also have the capability to hold a second Jumbo frame until the customer system Host MAC stops sending.
   - In addition to the two jumbo frames, there is also an 802.3-specified reaction time that the customer system Host MAC is expected to meet, during which the Egress Flow Control Buffer is continuing to receive frames from the Host.

The following Egress FC Buffer configuration settings control the handling of pause frames received from the Line in Basic Flow Control operation:

- PAUSE_REACT_ENA - Enables pause reaction and pause timer maintenance in the Egress FC Buffer. This should be set to 1.
- PAUSE_GEN_ENA - Enables XON and XOFF pause frame signaling to the LAN8267 Host MAC TX based on XON and XOFF thresholds. This should be set to 1.
- INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN - Enables the optional “OR” and “AND” gates in the previous figure. Recommended to be set to 1. When disabled the LAN8267 Host MAC TX will only generate pause frames toward the Host based on Egress FC Buffer XOFF/XON thresholds.

Figure 3-10 illustrates Basic Flow Control operation when a pause frame is received from the Host:

FIGURE 3-10: BASIC FLOW CONTROL, PAUSE FROM THE HOST



Follow the tags 1, 2, 3, 4, 5 in the figure.

1. The Host experiences congestion in Ingress and sends a pause (XOFF) to the LAN8267 Host Port. Ultimately this pause frame should reach the LAN8267 Line MAC link partner and control it to stop sending frames to the LAN8267 and ultimately toward the Host.
2. The LAN8267 Host MAC RX receives this pause frame but it is not enabled to react on received pause frames. The pause frame is passed by the LAN8267 Host MAC RX to the Egress FC Buffer.
   - LAN8267 never pauses the ingress stream toward the Host since it is not designed with large Ingress FC Buffers.
3. The Egress FC Buffer maintains two logical queues, one for Data frames and one for MAC Control frames (such as a pause frame). MAC Control frames cut ahead of any Data frames or fragments. In case a data frame is already scheduled and in progress, the MAC Control frames are transmitted from the Egress FC Buffer at the next boundary irrespective of if there are other data frames in the Data frame queue. This is done to quickly relay MAC Control frames to the Line.
4. The Egress FC Buffer might be in the Pause state due to pause (XOFF) received from the Line. Irrespective of the Pause state, the Egress FC Buffer transmits any or all MAC Control frames from the Control frame queue.
5. The pause frame passes through the 1588 block and also through the Line MAC TX block to the Line.
6. Not shown, but when the pause frame reaches the Line MAC link partner, it is expected that the Line MAC link partner will react to the pause frame and stop sending frames toward the LAN8267.

The following Egress FC Buffer configuration settings control the handling of pause frames received from the Host in Basic Flow Control operation:

- TX_CTRL_QUEUE_ENA determines if the Control frame queue is enabled in the Egress FC Buffer. This should be set to 1 in Basic Flow Control mode.
- TX_CTRL_QUEUE_START/END and TX_DATA_QUEUE_START/END configure the partitioning of Egress FC Buffer physical memory between Data frame and Control frame queues.

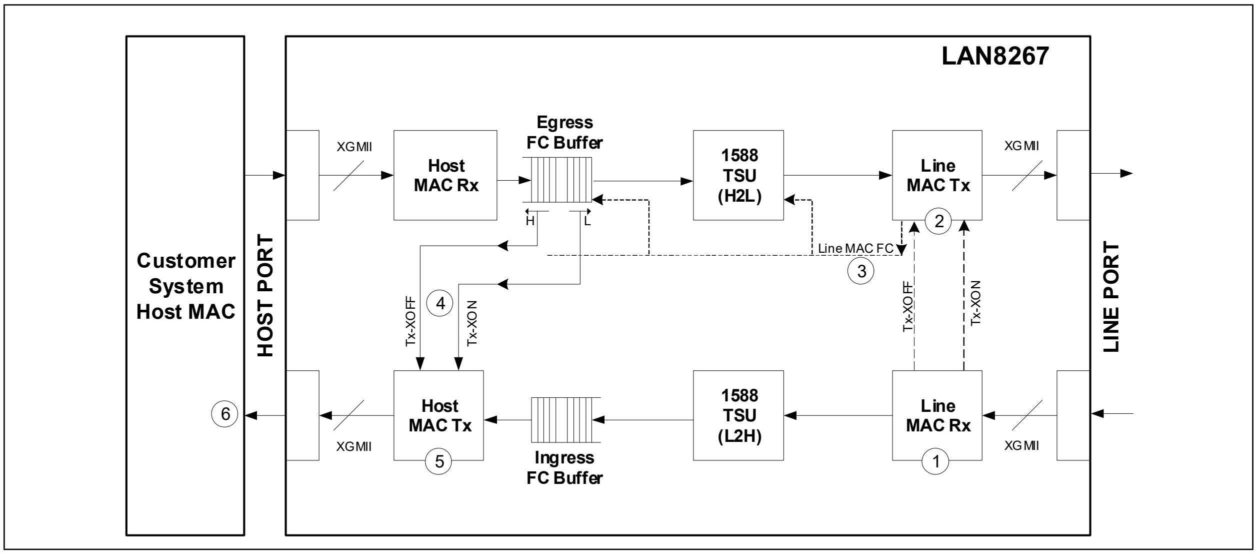
3.5.3 ADVANCED FLOW CONTROL HANDLING

“Advanced Flow Control” in this section describes:

- Receiving Pause from the LAN8267 Line MAC partner and reacting to it at the LAN8267 Line MAC TX.
- LAN8267 Line MAC TX flow-controlling the Egress FC Buffer.
- Generating Pause toward the Host due to filling of the Egress FC Buffer.
- Forwarding Pause from the Host to the TX Line Port while in this mode.

Figure 3-11 illustrates Advanced Flow Control operation when a pause frame is received from the Line:

FIGURE 3-11: ADVANCED FLOW CONTROL, PAUSE FROM THE LINE

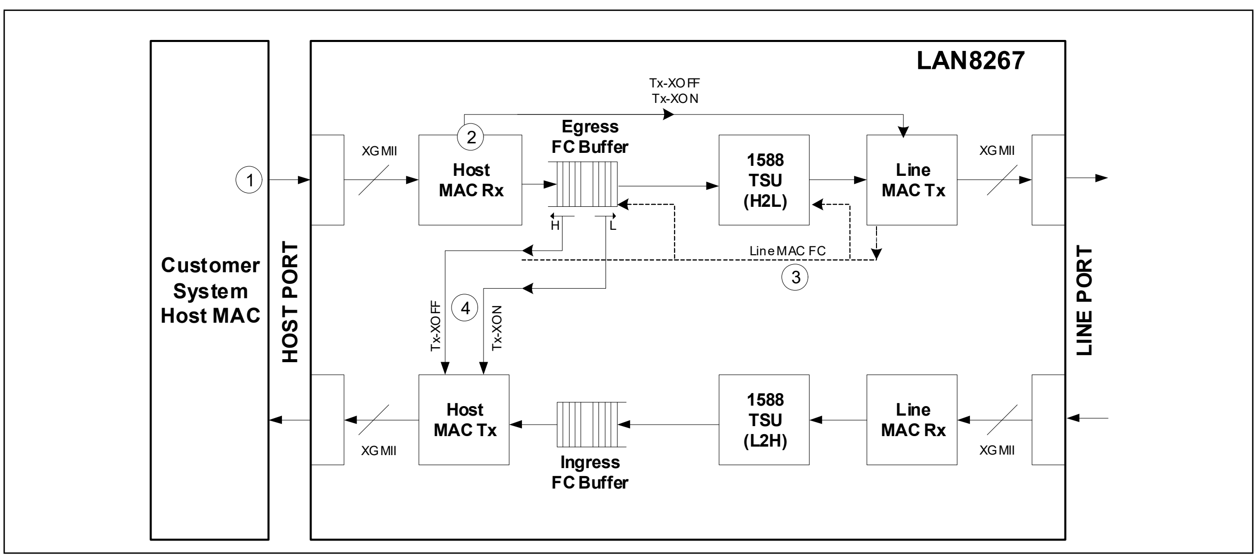


Follow the tags 1, 2, 3, 4, 5, 6 in the figure.

1. A pause frame (XOFF) is received by the LAN8267 Line MAC RX. This frame is internally consumed by the Line MAC.
2. The Line MAC RX signals the Line MAC TX indicating Pause was received and providing the Pause quanta. The Line MAC TX goes into the Pause state at the next TX frame boundary. The Pause Timer is maintained by the Line MAC TX and is started only after it goes into the Pause state.
3. The Line MAC TX issues Line MAC FC to stall the 1588 TSU (H2L) and the Egress FC Buffer.
4. The Egress FC Buffer signals XOFF/XON to the LAN8267 Host MAC TX based on the XOFF/XON thresholds.
5. The LAN8267 Host MAC TX can schedule a pause frame for transmission toward the Host at the next RX frame boundary.
6. The customer system Host MAC receives the pause frame and stops transmitting toward the Egress FC Buffer.

Figure 3-12 illustrates Advanced Flow Control operation when a pause frame is received from the Host:

FIGURE 3-12: ADVANCED FLOW CONTROL, PAUSE FROM THE HOST



Follow the tags 1, 2, 3, 4, 5 in the figure.

1. The Host experiences congestion in Ingress and sends a pause (XOFF) to the LAN8267 Host Port.
2. The LAN8267 Host MAC RX receives and consumes this pause frame. The Pause timer is maintained in the LAN8267 Host MAC RX (instead of Line MAC TX) which generates XOFF / XON control to the LAN8267 Line MAC TX.
3. The LAN8267 Line MAC TX issues Line MAC FC to stall the 1588 TSU (H2L) and the Egress FC Buffer in order to transmit a pause frame (either XOFF or XON) to the Line. This path will work irrespective of whether the LAN8267 Line MAC TX is in the Pause state.
4. The Egress FC Buffer is not expected to fill up due to Line MAC FC, but it can still signal XOFF/XON to the LAN8267 Host MAC TX based on the XOFF/XON thresholds

The following Egress FC Buffer configuration settings control Advanced Flow Control operation:

- PAUSE_GEN_ENA must be set to 1 to enable signaling to the LAN8267 Line MAC TX.

PAUSE_REACT_ENA, INCLUDE_PAUSE_RCVD_IN_PAUSE_GEN and TX_CTRL_QUEUE_ENA must all be set to 0.

3.6 Auto-negotiation and Training

The LAN8267 supports Auto-Negotiation per IEEE 802.3 clause 73 for the following link types:

- 1000BASE-KX (backplane)
- 10GBASE-KR (backplane)
- 10GBASE-CR (DAC)

Clause 73 auto-negotiation enables devices at both ends of a link segment to advertise abilities, acknowledge receipt, and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Clause 73 auto-negotiation also provides a parallel detection function to allow devices to connect to and inter-operate with devices which do not support Clause 73 auto-negotiation or have auto-negotiation disabled.

The LAN8267 also supports Auto-Negotiation per IEEE 802.3 clause 37 for the 1000BASE-LX and 1000BASE-SX (optical) link types. Auto-negotiation is supported for Pause and Remote Fault Signaling only, these link types are only supported at 1 Gbps and with full duplex.

The LAN8267 allows management to separately enable or disable clause 37 and clause 73 auto-negotiation, and to select a specific operational mode. Note there is no auto-negotiation support for 10G optical link types.

The LAN8267 supports Link Training per IEEE 802.3 clause 72 for the following link types:

- 10GBASE-KR (backplane), follows Clause 72.6.10
- 10GBASE-CR (DAC), follows Clause 72.6.10

Clause 72 Link Training allows the devices at both ends of the link to dynamically select digital filter tap settings which optimize link performance.

The LAN8267 allows management to disable dynamic link training and to statically configure the filter settings.

3.7 IEEE 1588 Operation

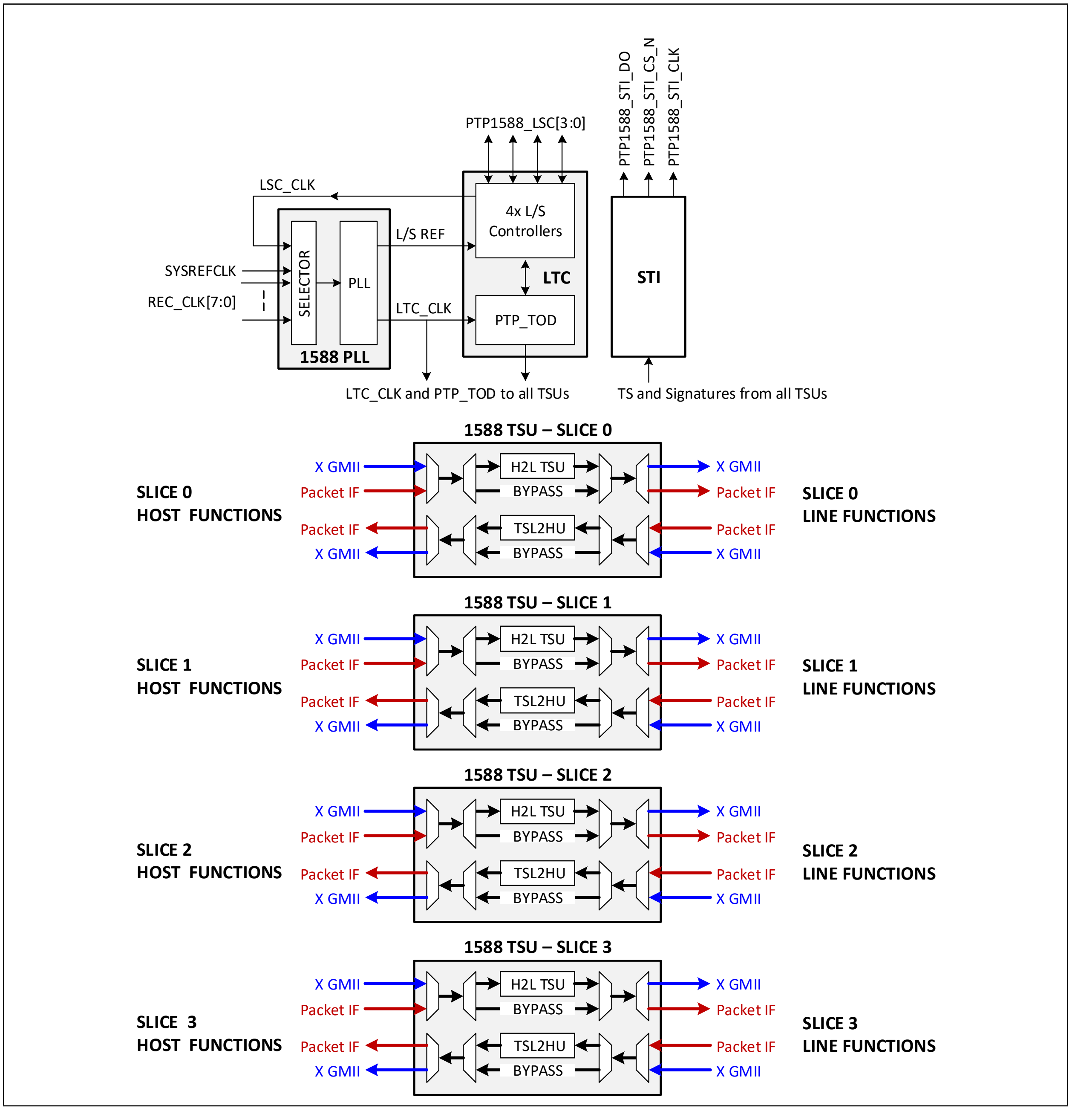
The LAN8267 device contains Microchip's third-generation IEEE 1588 engine that is backward compatible with the second-generation engine used in the VSC825x devices.

This third-generation IEEE 1588 engine supports the following new features:

- Ethernet interfaces up to 10 Gbps
- Frame Preemption support. Timestamping of unfragmented frames, configurable to be express only, preemptable only, or both
- Sub-nanosecond 1588 timestamp accuracy and resolution
- Support for IEEE standards 1588-2019 and 802.1AS-2020
- Fully non-shared 1588 engine and configuration per direction per slice
- Support of MCH header in conjunction with Microchip Ethernet switches
- Ability to capture egress timestamp in TS FIFO even for one-step, in support of Clause 16.11 timeReceiver
- Event Monitoring and Annex M Performance Monitoring Options
- Timestamp FIFO support for 8-bit sub-ns value

3.7.1 IMPLEMENTATION

FIGURE 3-13: 1588 BLOCK DIAGRAM



The 1588 architecture is shown in Figure 3-13 and consists of:

- A1588 PLL which provides clocks for the LTC and TSUs.
- A Local Time Counter (LTC), which maintains the PTP Time of Day (TOD) used by all TSUs. The PTP TOD counter is of the form 48-bit second//32-bit nanosecond//8-bit fractional nanosecond.

  The LTC block also contains the four Load/Store Controllers, which are used to load TOD, generate one pulse-per-second (1PPS), and with TOD-synchronous generation and capture operations.
- Per-slice 1588 Time Stamp Units (TSUs) each of which sits in the data path of each slice. The TSUs perform SOF detection, PTP frame analysis, MCH processing, timestamp generation, and frame rewriter operations related to

timestamping.

Two Timestamp Modes are supported:

- Standalone TS Mode, where each H2L and L2H frame is analyzed by the TSU to determine if any timestamping operation is required.
- MCH TS Mode, where H2L frame timestamping operations are controlled by the use of the Microchip Control Header (MCH) which is added to each H2L frame by the Host and consumed by the TSU.

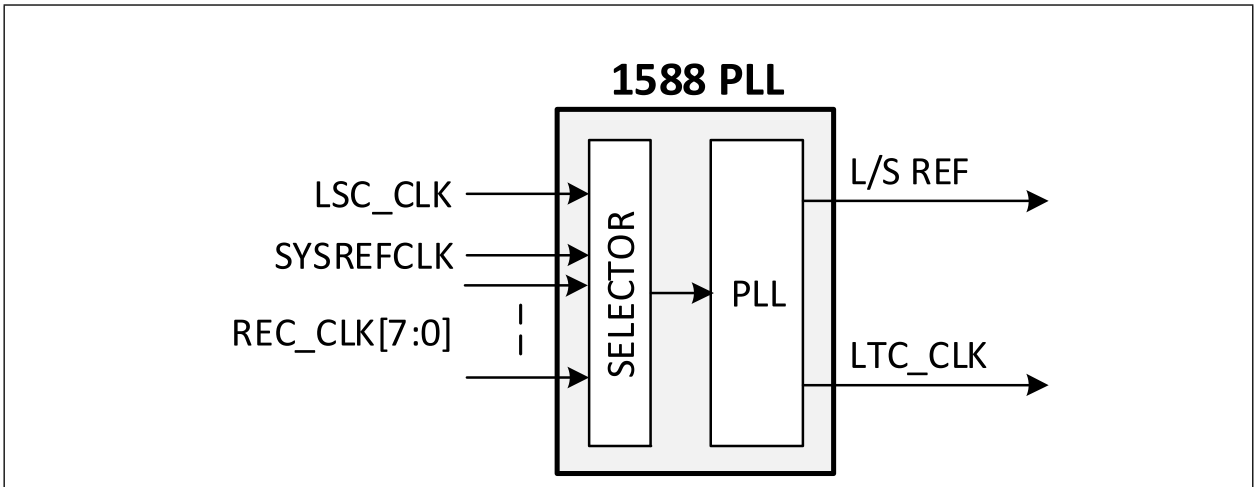
  In MCH TS Mode, all L2H frames will carry an arrival timestamp in the MCH which is added to each L2H frame by the TSU and consumed by the Host.

- A Serial Timestamp Interface (STI), shared by all slices. The STI provides H2L timestamps with corresponding frame signatures, such that the PTP application can correlate timestamps with frames/PTP flows.

3.7.2 1588 PLL

The 1588 PLL is shown in Figure 3-14

FIGURE 3-14: 1588 PLL



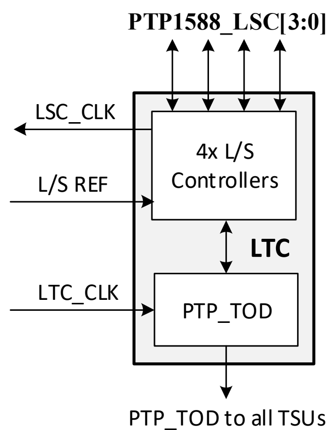
The 1588 PLL normally uses the 156.25 MHz SYSREFCK as its reference but can optionally also use the 25/125 MHz Load/Store Controller input clock or any of the eight Line or Host recovered clocks (varying frequencies) as references.

The 1588 PLL generates the 318.31 MHz LTC_CLK which runs the LTC and is used for timestamping operations. The 1588 PLL also generates the L/S REF clock which is directly divided down from the selected 1588 PLL reference and can optionally be used by Load/Store Controllers.

3.7.3 1588 LTC

The 1588 LTC is shown in Figure 3-15:

FIGURE 3-15: 1588 LTC



The LTC contains the PTP_TOD counter, containing the local PHY time. The initial Time of Day (TOD) value is loaded in one of the following ways:

- Software configures TOD but the value is loaded into PTP_TOD only when the next external 1PPS or ePPS strobe occurs (most accurate)
- Software configures and loads TOD directly into PTP_TOD (least accurate)

Once loaded the PTP_TOD counter is updates every LTC_CLK with a configurable value. The configured update value can be changed as needed by software to account for ppb clock drift.

Software access to the PTP_TOD counter is done through direct register access or via one of the four load/store (L/S) controllers. Each LSC is able to get or set a TOD counter immediately or when a **PTP1588_LSC[x]** edge is detected and they can be used to generate **PTP1588_LSC[x]** waveforms controlled by the TOD counter value.

The LTC also contains four Load/Store Controllers (LSC) which support the following:

- TOD LOAD operation into PTP_TOD using 1PPS or ePPS strobe
- TOD STORE operation by latching the PTP_TOD for software use using 1PPS or ePPS strobe
- TOD DELTA operation by adding or subtracting a configured value to/from the PTP_TOD using 1PPS or ePPS strobe
- Extraction of LSC_CLK for use as a reference by the 1588 PLL. The LSC_CLK is either 25 MHz or 125 MHz and may come from the external 1PPS Sync Clock input, or may be extracted from the ePPS.
- Generation of a waveform or pulse synchronized to PTP_TOD (LSC[2:0] only).
- Generation of serial TOD output synchronized to PTP_TOD (LSC[2:0] only).
- Each LSC normally operates from the LTC_CLK but can be configured to use the L/S Reference clock instead.

3.7.3.1 LSC External Interface

LSCs support the following via external pins:

1. 1PPS Input, which is used with TOD LOAD, STORE, and DELTA operations.
2. 1PPS Input with embedded Serial TOD, which is used with TOD LOAD and STORE (but not DELTA) operations.
3. 1PPS Sync Clock Input, which is used with 1PPS and 1PPS with embedded Serial TOD. This clock is also used to synchronize 1588 output events and can be extracted as LSC_CLK for use as the 1588 PLL reference.
4. ePPS (clock with embedded PPS) Input, which is used with TOD LOAD, STORE, and DELTA operations. The clock can also be extracted as LSC_CLK for use as the 1588 PLL reference.
5. Waveform Generator Output (LSC[2:0] only)

3.7.3.2 TOD LOAD / STORE / DELTA Operations

LOAD/STORE/DELTA actions may be immediate or delayed based on the PTP_PIN_SYNC configuration bits.

- If PTP_PIN_SYNC[0] is cleared, the action is immediate (executed when software writes to the command register).
- If PTP_PIN_SYNC[0] is set, the action, pending in the command register, will be executed when an active edge is detected on the selected **PTP1588_LSC[x]** pin using one of three options:

1. Asynchronous (one-pin): The edge is sampled using the internal LSC_CLK which results in sampling inaccuracy of ~ 1.6 ns.
2. External Synchronous (two-pin): The edge is sampled using the external 1PPS Sync Clock which provides sub-ns accuracy.
3. Internal Synchronous (one-pin): If the edge is synchronous to the 1588 PLL reference clock, then that reference clock can be selected in lieu of the second **PTP1588_LSC[x]** input, providing sub-ns accuracy.

For either value of PTP_PIN_SYNC, the LOAD/STORE/DELTA command bits are automatically returned to IDLE when complete (i.e. self-cleared).

The LOAD value is configured in registers by software or is externally available, using a selected **PTP1588_LSC[x]**, while using "1PPS LOAD with embedded TOD". In the latter case only seconds are supplied with ns:fns set to 0:0.

The DELTA value is always configured in registers by software.

When PTP_PIN_SYNC=1, the active edge input on the configured pin is possible in several formats:

- **1PPS:** Typically 1 Pulse Per Second (1PPS), it can also be a non-repeating signal or a signal which repeats at some rate other than 1 Hz.
  1PPS can be used for LOAD, STORE and DELTA operations.
- **1PPS with embedded ToD:** Similar to the 1PPS, however ToD is serially encoded on the same pin that receives 1PPS. The encoded ToD occurs following the 1PPS indication with the extracted value for potential use on the following PPS, 1 second later. Therefore a 1 second adjustment is made in hardware. Note that the TOD value is serially input every second but it is only loaded into the ToD counter if SW has enabled the operation.
- 1PPS with embedded ToD can be used only for TOD LOAD and STORE operations. TOD DELTA operation is not supported. But unlike with plan 1PPS, a TOD STORE operation using 1PPS with embedded TOD stores the received serially encoded time for software usage without loading the time into the ToD counter.
- **ePPS:** ePPS can be used for TOD LOAD, STORE and DELTA operations.

3.7.3.3 ePPS Format

The **PTP1588_LSC[x]** must have a clock with a duty cycle of 40-50%. A synchronous event is indicated by a single cycle with a duty cycle of 10-40%.

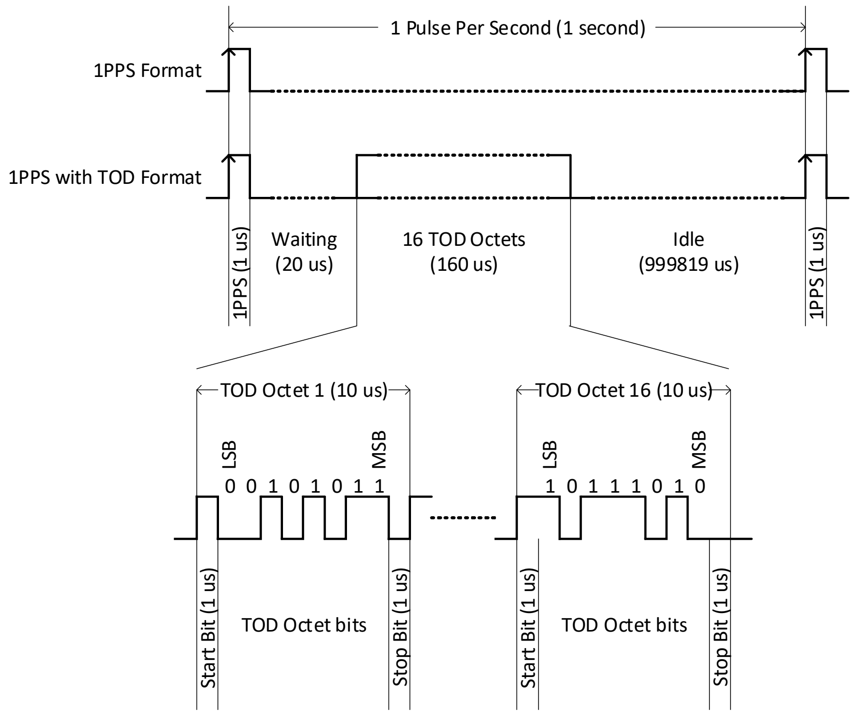
3.7.3.4 1PPS with Embedded Serial Time of Day Format

The 1PPS with TOD format is as follows:

- 1PPS: Rising edge indicates the 1PPS position, the pulse width is 1 us.
- Waiting: a gap of 20 us (logic low) between PPS and TOD
- TOD: 16 TOD octets, each occupies 10 us consisting of a start bit (logic high), eight TOD bits (LSB-first) and a stop bit (logic low).
  - The first six octets are Seconds in IEEE 1588-2008 format. These octets are used by LAN8267
  - The next six octets are Date in 0xYYMMHHMMSS decimal format. These octets are ignored by LAN8267
  - The final four octets are Reserved. These octets are ignored by LAN8267
  - Idle: a gap of 999819 us (logic low) between TOD and the next PPS rising edge.

As mentioned previously, the encoded ToD occurs following the 1PPS indication with the extracted value for potential use on the following PPS, 1 second later.

FIGURE 3-16: 1PPS SERIAL TOD FORMAT



3.7.4 WAVEFORM GENERATOR OUTPUT

The LSC Waveform Generator is able to generate a waveform, clock, 1PPS, ePPS, or Serial TOD on a selected output pin based on the PTP_ToD counter.

The LSC Waveform Generator uses both edges of the LTC_CLK. Due to this, the output signal changes have a half-clock uncertainty (misalignment compared to PTP_TOD counter changes). This uncertainty is measured by the Waveform Generator and provided to software in the PTP_PIN_OUTP_OFS register.

If configured to output a repeating waveform:

- The high period is configured in nanoseconds using PIN_WF_HIGH_PERIOD (WFH)
- The low period is configured in nanoseconds using PIN_WF_LOW_PERIOD (WFL)
- The minimum supported high or low period is 8 ns (maximum frequency 62.5 MHz)

If configured to output a clock:

- The output is connected to one of the PTP_TOD "nanoseconds" counter bits (bits 3-29 are available to be used for this purpose). For example, when connected to PTP_TOD counter.nsec[3] the output will toggle every 8 ns, resulting in a 62.5 MHz clock.
- The maximum supported frequency is 62.5 MHz

If configured to output a 1PPS:

- The pulse occurs each time the ToD reaches the value in PIN_WF_LOW_PERIOD (WFL)
- The pulse width is specified in PIN_WF_HIGH_PERIOD (WFH)
- The minimum supported pulse width is 8 ns.

If configured to output an ePPS :

- The output is connected to one of the PTP_TOD "nanoseconds" counter bits (bits 3-29 are available to be used for this purpose). For example, when connected to PTP_TOD counter.nsec[3] the output will toggle every 8 ns, resulting in a 62.5 MHz clock.
- The maximum supported frequency is 62.5 MHz

- The PPS clock cycle occurs each time the TOD reaches the value in PIN_WF_LOW_PERIOD (WFL)

If configured to output a Serial TOD:

- The Serial TOD will be generated every second when the PTP_TOD counter reaches the value in PIN_WF_LOW_PERIOD (WFL).
- The width of each bit is specified in PIN_WF_HIGH_PERIOD (WFH)
- The minimum supported high or low period is 8 ns
- The format is as follows:
  - The first 21 bits are a preamble <1000…0>
  - The next 16 bytes contain the TOD as <1><abcdefgh><0>, of which the first 6 bytes are the seconds value, the remaining bytes are 0.The endianness within the 6 bytes and each byte are both configurable

3.7.5 SERIAL TIMESTAMP INTERFACE (STI)

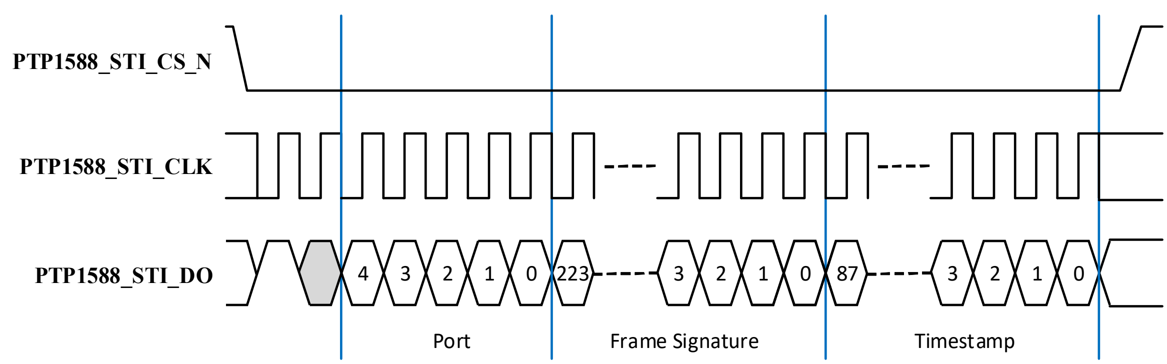
When the 1588 Serial Timestamp Interface (STI) is enabled, it pushes the egress (H2L) 1588 timestamps and frame signatures off-chip for collection by an external device.

When the STI is disabled, the egress H2L0 1588 timestamps and signatures are available to be read via software registers.

Timestamps and signatures are provided in both one-step and two-step 1588 operation.

The STI uses Serial Peripheral Interface (SPI) format where LAN8267 is the SPI Host, as shown:

FIGURE 3-17: STI FORMAT TIMING



Where a TSframe consists of:

- **Port** is the 5-bit PHY Address
- **Frame Signature** is:
  - Standalone TS Mode: Up to 224-bit value from the Analyzer
  - MCH TS Mode: 8- or 16-bit value from the MCH header
- **TimeStamp** is one of:
  - 32-bit departure timestamp
  - 40-bit departure timestamp
  - 80-bit departure timestamp
  - 88-bit departure timestamp

The maximum TSframe size is 88 + 224 + 5 = 317 bits.

The minimum TSframe size is 32 + 8 + 5 = 45 bits.

The STI is configurable as follows:

- The **PTP1588_STI_CLK** frequency is configurable between ~19.89 MHz and ~79.58 MHz, based on dividing the ~318 MHz LTC_CLK by integer values between [4, 16].
  - Maximum clock frequency is 79.58 MHz delivering ~239K TSframes/sec, assuming 317-bit TSframes, and

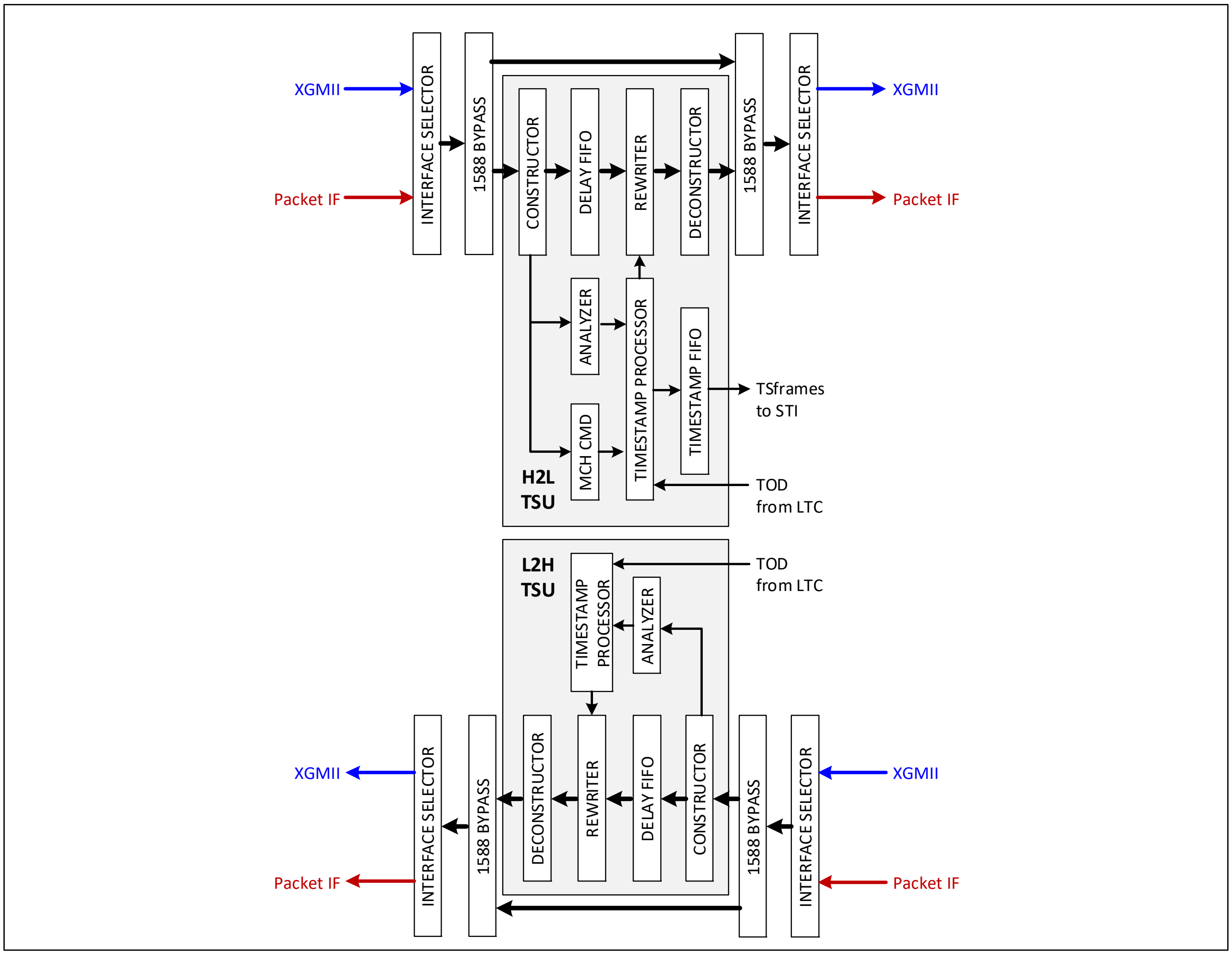
leaving two bytes between each TSframe.

- The number of **PTP1588_STI_CLK** periods (**PTP1588_STI_CS_N** deasserted) between consecutive TSframes is configurable.
- The number of **PTP1588_STI_CLKs** between **PTP1588_STI_CS_N** assertion and first valid bit of **PTP1588_STI_DO** is configurable.

3.7.6 TIME STAMP UNIT (TSU)

The 1588 Time Stamp Unit is shown in Figure 3-18:

FIGURE 3-18: 1588 TIME STAMP UNIT



The 1588 TSU supports both LAN8267 Operating Modes:

- PCS Retimer Mode where the TSU uses X GMIIs
- MAC Retimer Mode where the TSU uses Packet Interfaces

Interface selection and conversion is handled by the Interface Selectors, Constructor and Deconstructor.

Standalone TS Mode (Analyzer controls timestamping in both H2L and L2H directions) and MCH TS Mode (MCH controls timestamping in H2L direction, all frames carry a timestamp in L2H direction) are both available in both Operating Modes (PCS and MAC Retimer).

The 1588 TSU also supports a full 1588 Bypass.

When enabled the 1588 TSU provides timestamping for these PTP message types:

- Sync
- Delay_Req

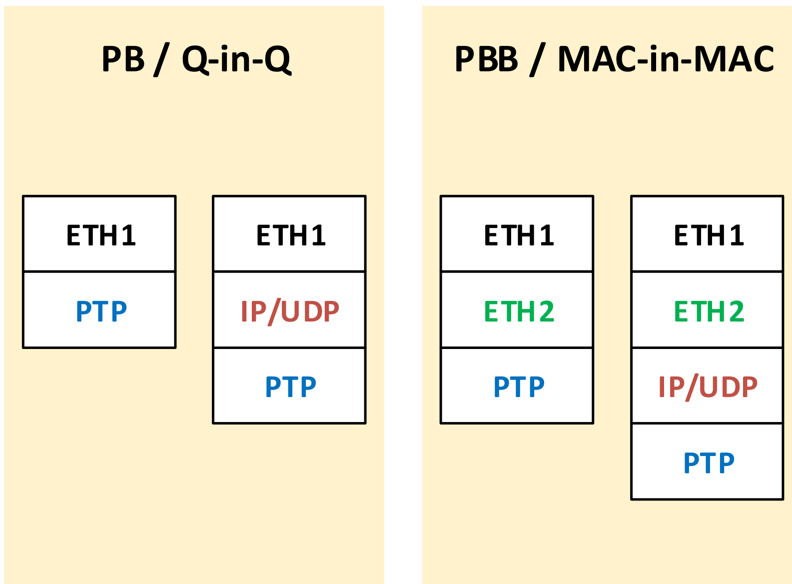
- PDelay_Req
- PDelay_Resp

The 1588 TSU provides timestamping for these PTP messages even when encapsulated in other protocols several layers deep. The supported encapsulations are as follows:

- Ethernet, with a variety of VLAN tag options
- UDP over IPv4 or IPv6
- MPLS and MPLS pseudowires
- PBB and PBB-TE tunnels

The following illustration shows an overview of the supported PTP encapsulations. Note that the implementation is flexible such that encapsulations not defined here may also be covered.

FIGURE 3-19: PTP PACKET ENCAPSULATIONS



In Standalone TS Mode each TSU detects and updates up to three different encapsulations of PTP. Non-matching frames are transferred transparently.

In MCH TS Mode each H2L frame arrives at the H2L TSU with an MCH including a command to update the Correction Field and UDP checksum when applicable. In the L2H direction the L2H TSU adds an MCH to each frame containing the arrival timestamp.

The H2L TSU also contains a Timestamp FIFO to capture departure timestamps for software use. The system design may to either have software read the Timestamp FIFO directly via registers, or make use of the STI to push timestamps to an external device.

3.7.6.1 Interface Selector

The Interface Selectors follow the Operating Mode. In PCS Retimer Mode, the X GMIIs are selected. In MAC Retimer Mode, the Packet Interfaces are selected.

3.7.6.2 Constructor, Deconstructor and Delay FIFO

The data arriving from the selected interface (X GMII or Packet Interface) is first fed to the Constructor which converts the data to a consistent internal format. This data is then fed to the Delay FIFO and either the Analyzer (Standalone TS Mode) or MCH Command Extractor (MCH TS Mode).

The Delay FIFO delays the data by the time needed to complete the operations necessary to update the PTP frame.

The Deconstructor then converts the data back to the selected interface (X GMII or Packet Interface).

3.7.6.3 Analyzer

The Analyzer is used in Standalone TS Mode. It searches the data stream for encapsulated PTP frames, and it determines the appropriate operations to be performed based on the PTP configuration and the type of PTP frame detected.

The Analyzers (and therefore the PTP encapsulations and flows being detected) are unique for each port and each direction.

Each Analyzer supports three different PTP encapsulation stacks using three Encapsulation Engines, and each Encapsulation Engine supports up to 8 different PTP flows. So for example:

- Engine A could be configured to support PTP inside MPLS pseudowires. A match could be determined using "any" pseudowire label, or up to eight unique pseudowire labels could be explicitly matched.
- Engine B could be configured to support PTP inside IPv4/UDP. A match could be determined using "any" IP Address, or up to eight unique IP Addresses could be explicitly matched.
- Engine C could be configured to support PTP inside Ethernet. A match could be determined using "any" VLAN ID, or up to eight unique VLAN IDs could be explicitly matched.

Each Encapsulation engine has multiple Encapsulation Comparators and one PTP Comparator. Each Encapsulation Comparator matches one encapsulation protocol (e.g. a VLAN ID, an MPLS Label an IP Address, etc) in the encapsulation stack. The PTP Comparator matches fields in the PTP PDU.

Encapsulation Engines A and B each provide six Encapsulation Comparators and one PTP Comparator, enabling deep encapsulation stack matching.

Encapsulation Engine C provides three Encapsulation Comparators and one PTP Comparator, providing a third (simpler) encapsulation stack matching capability.

The order of the Encapsulation Comparators and their capabilities are configurable within each Engine. Frame matching is performed Comparator-by-Comparator until the entire frame header has been parsed or a mismatch detected.

Encapsulation Comparators are tailored toward matching common protocols:

- Ethernet/SNAP Comparators support Ethernet
- MPLS Comparators support MPLS
- IP/UDP Comparators support IP/UDP, but are also highly flexible and able to support other protocols

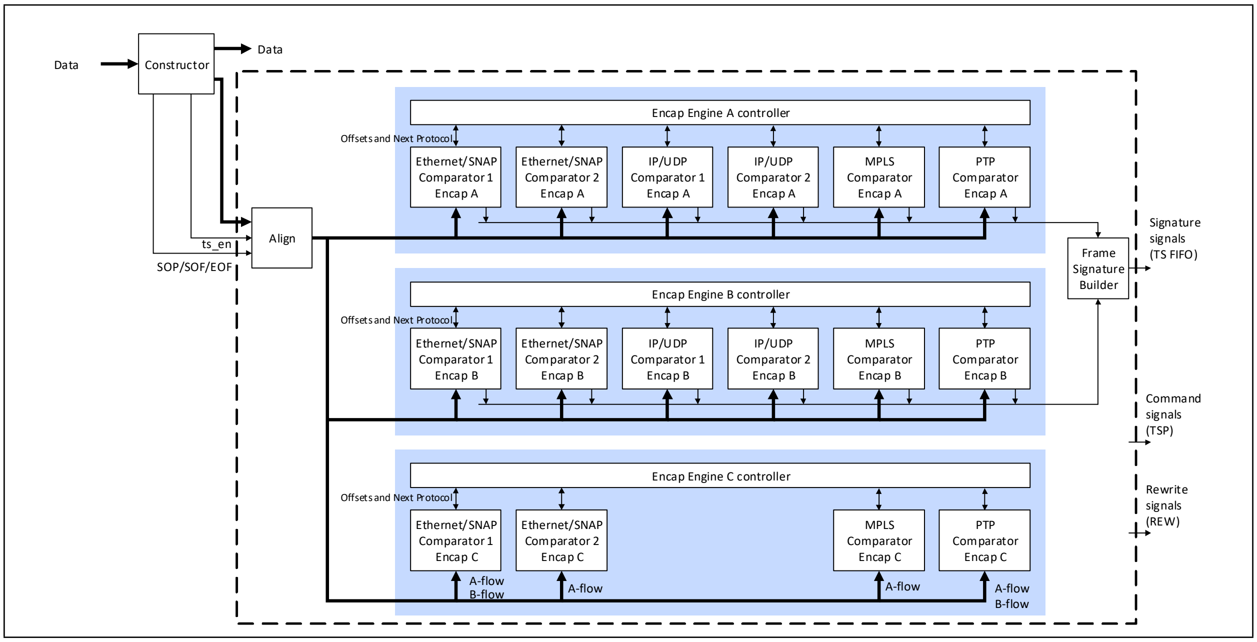
The results of frame analysis are:

Extracted bytes to use in generating the TSframe signature

- A command used by the Timestamp Processor and Rewriter, including location of any relevant fields (e.g. CorrectionField, UDP checksum). For frames not needing any timestamp action, the Analyzer generates a NOP command.

The following illustration shows a block diagram of the Analyzer.

FIGURE 3-20: ANALYZER BLOCK DIAGRAM



3.7.6.3.1 *Protocol Formats*

This section describes the headers and formats for the supported protocols.

FIGURE 3-21: ETHERNET WITH 0, 1, AND 2 VLANS

Ethernet

Bytes	Offset	
6	0	Destination address
6	6	Source address
2	12	Etype
N	14	Payload

Bytes	Offset	
6	0	Destination address
6	6	Source address
4	12	VLAN
2	16	Etype
N	18	Payload

Bytes	Offset	
6	0	Destination address
6	6	Source address
4	12	VLAN
4	16	VLAN
2	20	Etype
N	22	Payload

A maximum of 2 VLANs is supported.

FIGURE 3-22: ETHERNET WITH SNAP

Ethernet w/SNAP

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
2	12	Length
1	14	DSAP (0xAA/AB)
1	15	SSAP (0xAA/AB)
1	16	Ctl (0x03)
5	17	Protocol ID 0x000000 + Etype
2	22	Etype
N	24	Payload

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
2	12	Length
1	14	DSAP (0xAA/AB)
1	15	SSAP (0xAA/AB)
1	16	Ctl (0x03)
5	17	Protocol ID 0x000000 + VLAN Etype
2	22	VLAN ID
N	24	Payload

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
4	12	VLAN
4	16	VLAN
2	20	Etype
1	22	DSAP (0xAA/AB)
1	23	SSAP (0xAA/AB)
1	24	Ctl (0x03)
5	25	Protocol ID 0x000000 + Etype
2	30	Etype
N	32	Payload

FIGURE 3-23: PROVIDER BACKBONE ETHERNET

Provider Backbone

Comparator	Bytes	Offset	Field
1	6	0	Backbone Destination address
	6	6	Backbone Source address
	2	12	Etype (0x88E7)
	1	14	Flags
	3	15	SID
2	6	18	Customer Destination address
	6	24	Source address
		30	Rest of E-net header
			Payload

Comparator	Bytes	Offset	Field
1	6	0	Backbone Destination address
	6	6	Backbone Source address
	4	12	B-TAG
	2	12	Etype (0x88E7)
	1	14	Flags
	3	15	SID
2	6	18	Customer Destination address
	6	24	Source address
		30	Rest of E-net header
			Payload

FIGURE 3-24: MPLS

Ethernet w/MPLS

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
2	12	Etype
4	14	Label
		Payload

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
2	12	Etype
4	14	Label
4	18	Label
		Payload

Bytes	Offset	Field
6	0	Destination address
6	6	Source address
2	12	Etype
4	14	Label
4	18	Label
4	22	Label
4	26	Label
		Payload

FIGURE 3-25: IPV4 AND IPV6

UDP/IPv4

	Bytes	Offset	Fields			
IPv4	4	0	version	hdr length	Differentiated services	Total length
	4	4	Identification		Flags	Fragment offset
	4	8	Time to live		Protocol	Header checksum
	4	12	Source address			
	4	16	Destination address			
UDP	4	20	Source port		Destination port	
	4	24	Length		Checksum (overwrite with zero)	
	28					

UDP/IPv6

	Bytes	Offset	Fields			
IPv6	4	0	version	Traffic Class	Flow Label	
	4	4	Payload Length		Next Header	Hop Limit
	16	8	Source address			
	16	24	Destination address			
UDP	4	40	Source port		Destination port	
	4	44	Length		Checksum	
	48					

Note that when the PTP message is IPsec authenticated or encrypted, 2-step using MCH is suggested.

FIGURE 3-26: PTP

SYNC & Delay_req

Bytes	Offset	Field	
1	0	majorSdoId	Msg Type
1	1	minorVersionPTP	verPTP
2	2	Message length	
1	4	domainNumber	
1	5	minorSdoId	
2	6	flagfield	
8	8	correctionField	
4	16	messageTypeSpecific	
10	20	sourcePortIdentity	
2	30	sequenceID	
1	32	controlField	
1	33	logMessageInterval	
10	34	originTimestamp	
44			

Pdelay_req

Bytes	Offset	Field	
1	0	majorSdoId	Msg Type
1	1	minorVersionPTP	verPTP
2	2	Message length	
1	4	domainNumber	
1	5	minorSdoId	
2	6	flagfield	
8	8	correctionField	
4	16	messageTypeSpecific	
10	20	sourcePortIdentity	
2	30	sequenceID	
1	32	controlField	
1	33	logMessageInterval	
10	34	originTimestamp	
10	44	reserved	
54			

Pdelay_resp

Bytes	Offset	Field	
1	0	majorSdoId	Msg Type
1	1	minorVersionPTP	verPTP
2	2	Message length	
1	4	domainNumber	
1	5	minorSdoId	
2	6	flagfield	
8	8	correctionField	
4	16	messageTypeSpecific	
10	20	sourcePortIdentity	
2	30	sequenceID	
1	32	controlField	
1	33	logMessageInterval	
10	34	requestReceiptTimestamp	
10	44	reserved	
54			

FIGURE 3-27: EXAMPLES OF PTP OVER UPD/IPVX/MPLS/ETHERNET

PTP over UDP/IPv6/MPLS/Ethernet

	Bytes	Offset	Field	
Ethernet	6	0	Destination address	
	6	6	Source address	
	4	12	VLAN	
	2	16	Etype	
MPLS	4	18	Label	
	4	22	Label	
	4	26	Label	
	4	30	Label	
IPv6	8	34	Hdr	
	32	42	SIP/DIP	
UDP	4	74	S-port/D-port	
	4	78	Length/checksum	
SYNC & Delay_req	1	82	majorSdoId	Msg Type
	1	83	minorVersionPTP	verPTP
	2	84	Message length	
	1	86	domainNumber	
	1	87	minorSdoId	
	2	88	flagfield	
	8	90	correctionField	
	4	98	reserved	
	10	102	sourcePortIdentity	
	2	112	sequenceID	
	1	114	controlField	
	1	115	logMessageInterval	
	10	116	originTimestamp	
	126			

PTP over UDP/IPv4/MPLS/Ethernet

	Bytes	Offset	Field	
Ethernet	6	0	Destination address	
	6	6	Source address	
	4	12	VLAN	
	2	16	Etype	
MPLS	4	18	Label	
	4	22	Label	
	4	26	Label	
	4	30	Label	
IPv4	12	34	Hdr	
	8	46	SIP/DIP	
UDP	4	54	S-port/D-port	
	4	58	Length/checksum	
SYNC & Delay_req	1	62	majorSdoId	Msg Type
	1	63	minorVersionPTP	verPTP
	2	64	Message length	
	1	66	domainNumber	
	1	67	minorSdoId	
	2	68	flagfield	
	8	70	correctionField	
	4	78	reserved	
	10	82	sourcePortIdentity	
	2	92	sequenceID	
	1	94	controlField	
	1	95	logMessageInterval	
	10	96	originTimestamp	
	106			

3.7.6.3.2 Timestamping Options

Timestamping options are shown in Table 3-4

TABLE 3-4: TIMESTAMP OPTIONS

Mode	Figure	Command/Mode	Fields Affected	Format Options	Resolution
H2L, standard mode					
	A	SUB_ADD	correctionField	48b ns:16b fns	8b-frac ns
			messageTypeSpecific	30b ns 32b ns	
	B	WRITE_1588	correctionField	48b ns:16b fns	8b-frac ns
			messageTypeSpecific	30b ns 32b ns	
	C	ADD_2	correctionField	48b ns:16b fns	8b-frac ns
L2H, standard mode					
	D	WRITE_NS	correctionField	48b ns:16b fns	8b-frac ns
			messageTypeSpecific	30b ns 32b ns	
	E	WRITE_NS_P2P	correctionField	48b ns:16b fns	8b-frac ns
			messageTypeSpecific	30b ns 32b ns	
	F	SUB_2	correctionField	48b ns:16b fns	8b-frac ns
	G	Replace FCS	Preamble FCS	32b	ns
H2L, MCH mode					
	H	ADD_2	correctionField	48b ns:16b fns	8b-frac ns
L2H, MCH mode					
	I	Timestamp-all	MCH Extension[31:0]	30b:0b ns:fns 28b:4b ns:fns 24b:8b ns:fns 16b:16b ns:fns	ns 4b frac ns 8b frac ns 8b frac ns

3.7.6.4 H2L MCH

In MCH TS Mode, all H2L frames arrive from the Host Ports with the preamble replaced with the MCH H2L header.

The MCH Command Extractor is used in the H2L direction in MCH TS Mode. It extracts the MCH header from each H2L frame, parses the MCH, and generates the following results directly based on the MCH contents:

- The TSframe signature
- A command used by the Timestamp Processor and Rewriter, including location of any relevant fields (e.g. CorrectionField, UDP checksum). For frames not needing any timestamp action, the Analyzer generates a NOP command.

The H2L MCH header format is shown in Table 3-28:

FIGURE 3-28: MCH H2L HEADER FORMAT (FROM HOST SIDE)

Host/Line side Format (same Tx and Rx): standard Ethernet preamble

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	0x55	0x55	0x55	0x55	0x55	0x55	SFD or SMD	Packet Data

Host/Line side Format (same Tx and Rx): Preempted segment preamble

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	0x55	0x55	0x55	0x55	0x55	SDM-C	FRAC_ COUNT	Packet Data

Host side Format (H2L): MCH Header

	Byte 0	Byte 1			Byte 2	Byte 3	Byte 4		Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	PktTyp[1:0]	SubPort ID[3:0]	ExtTy[1:0]	Extension [39:32] Rsvd/ Preempt state	Extension [31:17] Reserved		Encrypt_en	Extension [15:0] 1-step/2-step Cmd & Signature		CRC[7:0]	Packet Data

MCH Byte 0 is the Start of Packet Delimiter (SPD), which is the same as in the standard preamble.

MCH Bytes 1-6 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0]=00 = valid MCH header
- SubPortID[3:0]= LAN8267 slice number (0, 1, 2, or 3)
- ExtTy[1:0] indicates e-frame or p-frame
  - If Preemption is enabled all frames on the port are expected to have ExtTy[1:0]=10 = Preemption Enabled.
    - However, frames with ExtTy[1:0] = 00 are treated as valid unfragmented frames which are passed to the line with valid preambles, and will not be counted as Extension Type Mismatch errors.
    - Frames with ExtTy[1:0] = 01 or 11 are treated as invalid frames. They are counted as Extension Type Mismatch errors, and discarded by the LAN8267.
  - If Preemption is disabled all frames on the port are expected to have ExtTy[1:0] = 01 = Preemption Disabled.
    - However, frames with ExtTy[1:0] = 00 are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles, and will not be counted as Extension Type Mismatch errors.
    - Frames with ExtTy[1:0] = 10 or 11 are treated as invalid frames. They are counted as Extension Type Mismatch errors, and discarded by the 10G transmit PHY.
- Extension[39:32] conveys preemption state
  - Extension[39:38]: Preemption (IET) Frame Type
    - 00: High-priority frame (eMAC)
    - 01: Low-priority preemptable frame or initial fragment (pMAC)
    - 10: Low-priority intermediate fragment or last fragment (pMAC)
    - 11: Verify/Respond frame
  - Extension[37:36]: Type of Verify/Respond
    - 00: Verify
    - 01: Respond
    - 10/11: Reserved
- Extension[35:34]: Frame Count is a 2-bit binary of low-priority Fragmented frames
- Extension[33:32]: Fragment Count is a 2-bit binary count of low-priority Intermediate or Last Fragment frame
- Extension[31]=unused/ignore

- Extension[30:17]=unused/ignore
- Extension[15]=0 indicates two-step timestamping
  - Extension[14:10]=Frame Signature to send to the TS FIFO
  - Extension[9]=unused/ignore
  - Extension[8:7]= unused/ignore
  - Extension[6:0]=unused/ignore
- Extension[15]=1 indicates one-step timestamping
  - Extension[14:10]=Signature to send to the TS FIFO
  - Extension[9]=UdpFix.
    - UdpFix=1 indicates this is a PTP/UDP/IPv6 frame, and the two UDP checksum pad bytes are to be incrementally updated.
    - UdpFix=1=do not update UDP checksum pad bytes
  - Extension[8:7]=10 indicates this is a PTP frame to be timestamped and the correctionField must be updated using the ADD_2 (48-bit add) operation. Other values of Extension[8:7] are unused/ignored (these frames are not timestamped).
  - Extension[6:0]=DataOfs[6:0]. For PTP frames where the correctionField must be updated, this provides the location of the sixteen-bit correctionField, starting with the first 16 bits of packet data following MCH CRC[7:0].
- CRC[7:0]=CRC-8 covering MCH as per the USGMII specification

3.7.6.5 L2H MCH

In MCH TS Mode, all L2H frames are sent to the Host Ports with the preamble replaced with the MCH L2H header. The Analyzer is not used in MCH TS Mode; all PTP frames arriving from the Line Ports given an arrival timestamp with one of four configurable formats.

The L2H MCH header format is shown in Figure 3-29:

FIGURE 3-29: MCH L2H HEADER FORMAT (TOWARD HOST)

	Host/Line side Format (same Tx and Rx): standard Ethernet preamble								
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	0x55	0x55	0x55	0x55	0x55	0x55	SFD or SMD	Packet Data

	Host/Line side Format (same Tx and Rx): Preempted segment preamble								
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	0x55	0x55	0x55	0x55	0x55	SDM-C	FRAC_ COUNT	Packet Data

	Host side Format (L2H): MCH Header								
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	
IDLE (0x00)	SPD 0xfb	PktTyp[1:0] / SubPort ID[3:0] / ExtTy[1:0]	Extension [39:32] Rsvd/ Preempt state	Extension [31:0] Arrival TimeStamp				CRC[7:0]	Packet Data

MCH Byte 0 is the Start of Packet Delimiter (SPD), which is the same as in the standard preamble.

MCH Bytes 1 and 2 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0]=00 = valid MCH header
- SubPortID[3:0]= LAN8267 slice number (0, 1, 2, or 3)
- ExtTy[1:0] indicates e-frame or p-frame
  - If Preemption is enabled all frames on the port will have ExtTy[1:0]=10 = Preemption Enabled.

- If Preemption is disabled all frames on the port will have ExtTy[1:0] = 01 = Preemption Disabled.

- Extension[39:32] conveys preemption state
  - Extension[39:38]: Preemption (IET) Frame Type
    - 00: High-priority frame (eMAC)
    - 01: Low-priority preemptable frame or initial fragment (pMAC)
    - 10: Low-priority intermediate fragment or last fragment (pMAC)
    - 11: Verify/Respond frame
  - Extension[37:36]: Type of Verify/Respond
    - 00: Verify
    - 01: Respond
    - 10/11: Reserved
  - Extension[35:34]: Frame Count is a 2-bit binary of low-priority Fragmented frames
  - Extension[33:32]: Fragment Count is a 2-bit binary count of low-priority Intermediate or Last Fragment frame
- Extension[31:0] carries the Arrival Timestamp, which is configurable to support the following formats:
  - 32.0 Format: 32 bit nsec [0,0, 30-bit nsec]
  - 28.4 Format: 28 bit of ns + 4-bit Fractional ns
  - 24.8 Format: 24-bit of ns + 8-bit of Fractional ns
  - 16.16 Format: 16-bit of ns + 16-bit of Fractional ns

Note: Note the 8 lower bits of the 16-bit Fractional ns are always zero

3.7.6.6 Timestamp Processor

The Time Stamp Processor (TSP) builds the new timestamp that is to be written into the PTP frame or MCH.

The H2L TSP generates the new timestamp and always provides it to the Timestamp FIFO. For one-step operation, the H2L TSP also provides this timestamp to the Rewriter to update the PTP frame.

The L2H TSP generates the new timestamp and always provides it to the Rewriter to update the PTP frame (Standalone TS Mode) or MCH header (MCH TS Mode).

3.7.6.7 Timestamp FIFO

The Timestamp FIFO (TS FIFO) is only used in the H2L direction. It stores at least 16 timestamps (received from the TSP) along with frame signature information (from the Analyzer or MCH Cmd Extract). This information can be read out by a CPU and used in two-step operation to create Follow-up messages, or in one-step operation to monitor the time-stamps. It can also be transferred to the STI interface.

The TS FIFO supports four Timestamp formats:

- 48.32.0 Format: 48 bit seconds, 32 bit nsec, no Fractional-ns
- 0.32.0 Format: 32 bit nsec, no seconds or Fractional-ns
- 48.32.8 Format: 48 bit seconds, 32 bit nsec, 8 bit Fractional-ns
- 0.32.8 Format: 32 bit nsec, 8 bit Fractional-ns, no seconds

The stored frame signature can be of varying sizes:

- In Standalone TS Mode the frame signature can be up to 224 bits
- In MCH TS Mode the frame signature is either 8 or 16 bits

The TS FIFO depth varies depending on the size of the Timestamp and the frame signature. Some examples are shown in Table 3-5.

TABLE 3-5: TIMESTAMP AND FRAME SIGNATURE SIZES

Timestamp Size (bits)	Frame Signature Size (bits)	TS FIFO entries
32	8	124
40	16	89
40	128	29
40	224	18
80	16	52
80	128	24
88	16	48
88	128	23
88	224	16

3.7.6.8 Rewriter

The Rewriter handles the actual writing of the new timestamp into the PTP frame or MCH header.

For IPv6 the Rewriter incrementally updates the IPv6 UDP dummy bytes, which are always the last two bytes in the frame ahead of the frame CRC. These bytes are incrementally updated to ensure the UDP checksum is correct after the timestamping operation.

For IPv4, the LAN8267 requires that the UDP checksum is set to zero as per the PTP standard.

The Rewriter is also able to clear a number of consecutive bytes to zero, which is normally used to clear the PTP reserved bytes on egress, but can be used to clear the IPv4 UDP checksum bytes. Only one of these operations can be supported however.

The Rewriter also contains Ethernet CRC check and update functions which are used in PCS Retimer Mode. Only one Ethernet CRC can be updated per frame, and it is only updated if the frame is timestamped. If the original Ethernet CRC was in error, the updated frame CRC will also be in error.

3.7.6.9 1588 Bypass

1588 Bypass can be used in both Operating Modes (PCS Retimer and MAC Retimer) PCS Retimer Operating mode, as well as both Timestamp Modes (Standalone and MCH). 1588 Bypass reduces latency and can be enabled/disabled dynamically.

3.8 Clocking

3.8.1 DATA PATH CLOCKING

Each slice data path Tx and Rx clocks are generated by that slice's SerDes CMU. Tx datapath clocks are generated from the 156.25 MHz SYSREFCK and are frequency synchronous across all slices. Rx datapath clocks are recovered from the Rx serial datastream and may be frequency asynchronous to other clocks.

Loop timing of a port (using the receive clock as the transmit clock) is not supported.

3.8.2 SYSTEM CLOCK GENERATION

The following internal chip clocks are generated by the System PLL which uses the 156.25 MHz SYSREFCK as reference:

- 300 MHz for SPI, MDIO, and internal CSR register logic
- 300 MHz for TWI Host

3.8.3 SYNCHRONOUS ETHERNET AND RECOVERED CLOCKS

The LAN8267 supports Synchronous Ethernet as specified by ITU-T G.8261 is supported in LAN8267 as described below. A system with LAN8267 may support Synchronous Ethernet only, IEEE 1588 only or both Synchronous Ethernet and IEEE 1588.

Table 3-6 illustrates a system using LAN8267 to support Synchronous Ethernet. Typical requirements include:

- Ability to select any Line Port recovered clock as the Primary timing reference. The LAN8267 RCKOUTA can be used for this purpose.

- Ability to select any Line Port recovered clock as the Secondary timing reference. The LAN8267 RCKOUTB can be used for this purpose.
- Ability to use a local high-quality oscillator as the Primary, Secondary or Hold-over timing reference. The OCXO provides this function in this example. OCXO specifics are out of scope for this example.
- The selected timing reference must be qualified and cleaned up by the DPLL, which also may perform timing failover and frequency conversion functions. DPLL specifics are out of scope for this example.
- All Line Ports will use the DPLL output as their reference timing. This becomes the 156.25MHz SYSREFCK input into the LAN8267.

The LAN8267 provides two Recovered Clock outputs supporting the following capabilities:

- Each output is selectable to provide the recovered clock from any LAN8267 Line Port
- Each output has a configurable divider which can provide frequencies per Table 3-6
- Each output has a Squelch function, where the output is disabled for Line Port fault conditions. Squelching the clock immediately in hardware can be used to achieve faster timing failover. Note that when squelched, the recovered clocks can stop either high or low. Clock Squelch can also be disabled.
  The applicable fault conditions are:
  - Link Down (condition can be ignored by setting PCS_LINK_STS_SQUELCH_ENA=0)
  - Loss of Signal (LOS) (condition can be ignored by setting SD_LOS_SQUELCH_ENA=0)
  - Link is in the Training state (condition is always applicable)

TABLE 3-6: RECOVERED CLOCK OUTPUT FREQUENCIES

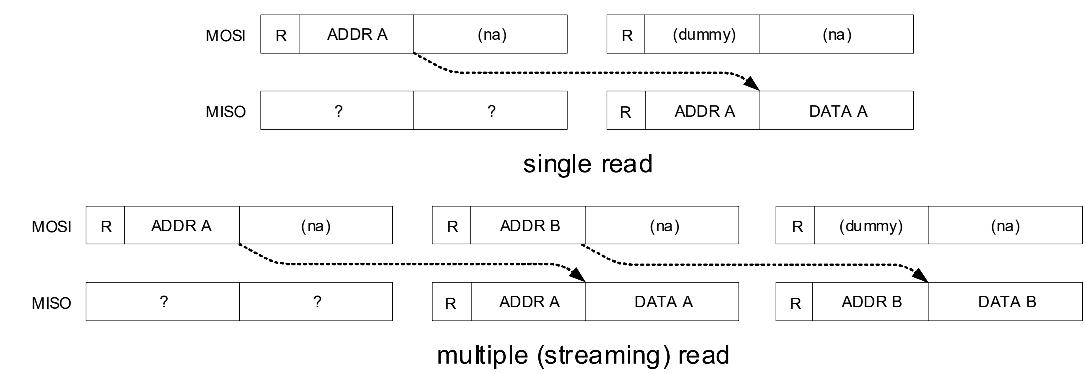
Port Speed	Recovered Clock Frequency	Recovered Clock Output Divider	Recovered Clock Output Frequency
1G	125.00 MHz	1	125
		2	62.5
		4	31.25
		8	15.625
10G	257.8125 MHz	1	Not Available
		2	128.90625
		4	64.453125
		8	32.2265625

3.9 Device Management

3.9.1 SPI CLIENT INTERFACE

LAN8267 supports the SPI Client interface as a high bandwidth interface for reading 1588 time stamp data and classification updates. The SPI interface is also capable of accessing the entire status and configuration register space. The SPI Client interface consists of the SPI_CLIENT_SCK serial clock input, the SPI_CLIENT_MOSI data input, the SPI_-CLIENT_MISO data output and the SPI_CLIENT_SSN input (active low).The SPI Client interface is implemented as a pipeline system, addressing the bandwidth requirement for reading data from the 1588 time stamp and FIFO registers (as opposed to using the Serial Timestamp Interface (STI) push interface). As such, the data read back during any READ transaction is the value request from the previous transaction. To illustrate, single and multi-register reads would look like Figure 3-30.

FIGURE 3-30: SPI CLIENT PIPELINED READS



From a software perspective, a read of a single address would have to actually do two SPI reads. However, for streaming out many registers at once, the interface is using the full bandwidth while retaining random access.

SPI instruction consists of a 56-bit format as shown in Table 3-7:

TABLE 3-7: SPI CLIENT INSTRUCTION FORMAT

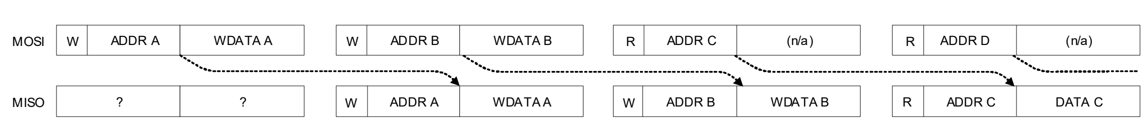
Bit	Name	Description
55	Read/Write	1 = Write, 0 = Read
54:53	Slice Number	0 = Slice 1 1 = Slice 2 2 = Slice 3 3 = Slice 4
52:48	Device Number	5 bits for devices 1 - 31
47:32	Address	16 bits Register access
31:0	Data	32 bits

APPLICATION NOTE: When accessing FIFOs or other change on read registers, either singly or streaming, care must be taken to not inadvertently perform an excess read during the second / final phase of the pipeline access. For example the dummy address should not access a FIFO or change on read register. A safe dummy address would be that of the Device_ID register in the GLOBAL target (device 0x1E).

Writes happen at the end of the command (they are not pipelined).

The read-back data of the transaction following a write is the last write parameters.

FIGURE 3-31: SPI CLIENT PIPELINED WRITES FOLLOWED BY READS



3.9.2 MANAGEMENT DATA INPUT/OUTPUT (MDIO) INTERFACE

LAN8267 supports the Management Data Input/Output (MDIO) Interface as a low to medium bandwidth interface for basic PHY management.

APPLICATION NOTE: Although the Management Data Input/Output (MDIO) Interface can access the entire status and configuration register space, due to its slow bandwidth and high latency, the Management Data Input/Output (MDIO) Interface is not recommended as the only interface to access the device.

LAN8267 supports the Management Data Input/Output (MDIO) Interface as defined clause 45 of the IEEE 802.3 Ethernet specification. The Management Data Input/Output (MDIO) Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC).

The base port address is determined by the PADDR inputs and can be any value from 0 to 28 for quad Slice devices. Each Slice is addressed at an offset from the base address. Slice 0 is at PADDR, Slice 1 at PADDR+1,etc.

If the base address is set too high, the offset of the higher Slices would wrap past zero. Do not to exceed a PHY base address of 28 (for quad Slice devices).

3.10 Fiber Modules and Management

3.10.1 TWO-WIRE INTERFACE

A serial Two Wire Interface (TWI) Host, enabled as GPIO Alternate Functions, is available for optical module management per Line Port.

The TWI Host must be configured before initiating any TWI instructions. The Client ID to be transmitted in the first byte of every instruction is selectable in the TWI_CLIENT_ID register (default value 0x50).

The interface's data rate is determined by the PRESCALE register. The TWI Host can operate from 916 Hz to 1 MHz. The logic is clocked at 300 MHz with the data rate controlled by the PRESCALE register using this formula:

- TWI SCL frequency = (300 MHz) / [5 * (PRESCALE+1)], where
  - PRESCALE is valid between 0x003B and 0xFFFF (0x003B = 1 MHz, default of 0x0095 = 400 kHz, 0x0257 = 100 kHz)

The TWI Host transmits instructions to the optical module with 8-bit data registers and 256 register addresses per Client ID. The TWI_BUS_STATUS.TWI_BUS_BUSY or TWI_READ_STATUS_DATA.TWI_BUS_BUSY register bit should be read to verify the previous instruction has finished prior to initiating a new instruction. Instructions initiated when the interface is busy will be ignored. Both registers report the same interface busy status purely for user convenience.

Read Instructions

A read instruction is initiated by the TWI Host when the TWI_READ_ADDR register is written. The value written to TWI_READ_ADDR.READ_ADDR field is the optical module register address to be read. Once the TWI_READ_STATUS_DATA.TWI_BUS_BUSY bit clears, indicating the read instruction completed, the returned data is available in the TWI_READ_STATUS_DATA.READ_DATA field.

The TWI Host does not support read-increment instructions.

Write Instructions

A write instruction is initiated by the TWI Host when the TWI_WRITE_CTRL register is written. The value written to TWI_WRITE_CTRL.WRITE_ADDR field is the optical module register address to be written while the value written to TWI_WRITE_CTRL.WRITE_DATA field is the optical module register data.

The TWI_BUS_STATUS register reports the status of the write instruction. TWI_BUS_STATUS.TWI_WRITE_ACK=1 indicates that the TWI Host received ACKs from the optical module at appropriate times. TWI_BUS_STATUS.TWI_WRITE_ACK is cleared each time a new instruction is issued. TWI_BUS_STATUS.TWI_WRITE_ACK=0 indicates the TWI Host did not receive ACKs from the optical module at appropriate times, meaning the interface is likely stuck in a state waiting for the ACK.

Clock Stretching

The optical module may hold the TWI_SCL signal low following the ACK cycle. This will cause the TWI Host to be wait-stated.

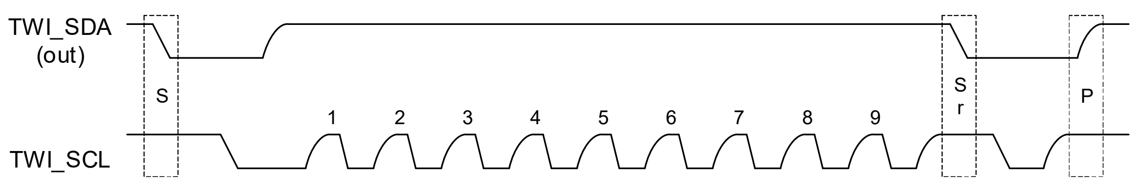
Bus clear

Writing a 1 to the BLOCK_LEVEL_RESET1.TWIM_RESET register bit will reset the TWI Host and release it from its stuck state. An external reset should be issued to the optical module as well.

The TWI Host and the optical module can become out-of-sync due to these resets and a bus clear sequence should be issued by writing any value to the TWI_RESET_SEQ register. This will put the optical module’s two-wire interface back into a state that allows it to receive future two-wire serial instructions.

The following illustration shows a two-wire serial bus clear sequence. The bus clear sequence consists of a START symbol (S), nine SCK clock pulses while SDA is high, a repeated START symbol (Sr) and a STOP symbol (P).

FIGURE 3-32: TWI BUS CLEAR



3.10.2 FIBER MODULE SUPPORT

LAN8267 supports the following optical modules, with GPIO mappings as described. Signal polarity is generally consistent across module types (e.g. 0 on the MOD_ABS input indicates a module is present) but module-specific differences exist. In some modules dual-purpose signal (e.g. IntL/RxLOSL) behavior is configurable in the module using the TWI interface.

TABLE 3-8: OPTICAL MODULE INTERFACES

LAN8267 Pins	Optical Module Pins			
	SFP *INF-8074i*	**XFP** *INF-8077i*	**SFP+** *SFF8431*	**QSFP+** *SFF8436* *SFF8679*
RATESEL0 (output)	RATESELECT Full vs Reduced Rate Not often used	PDOWN/RST	RS0 / RS1 Full vs Reduced Rate Not often used	ResetL
MOD_ABS (input)	MOD-DEF0 0=module present	MOD_ABS 0=module present	MOD_ABS 0=module present	ModPrsL 0=module present
TWI_HST_SCL (output)	MOD-DEF1 =I2C SCL	SCL	SCL	SCL
TWI_HST_SDA (I/O)	MOD-DEF2 =I2C SDA	SDA	SDA	SDA
TX_DIS (output)	TXDISABLE	TX_DIS	TX_DISABLE	LPMode/TxDis
TX_FAULT (input)	TXFAULT	MOD_NR		
RXLOS (input)[1]	LOS	RX_LOS	RX_LOS	IntL/RxLOSL
		MOD_DESEL Tie low		ModSelL Tie low

1: When enabled as an Alternate Function, RX_LOS is internally combined with the Line SerDes LOS into the applicable PCS to force an immediate Link Down condition when either the optical receive signal or SerDes receive signal is lost.

I^2C (TWI) is supported by a dedicated TWI Host in each LAN8267 slice.

3.11 LEDs

LAN8267 supports two LEDs per Line Port: Activity and Link Up, which operate as follows:

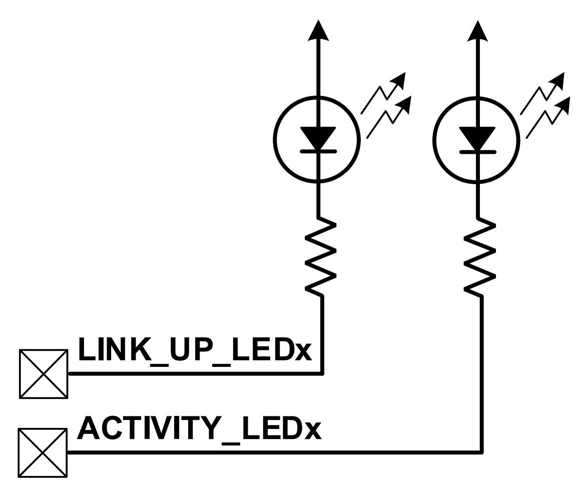
1. The Line Port Activity LED blinks at a configurable rate when either TX or RX Line Port activity is detected. The Line Port Activity LED is not lit and does not blink when the Line Port Link is down.
2. The Line Port Link Up LED is lit solid when the Line Port Link is up and is not be lit when the Line Port Link is down.
3. LEDs functions as above for all Line Port speeds and PCSs.
4. Each LED is active low (GPIO output = 0 turns the LED on).

APPLICATION NOTE: LEDs are internally active low, therefore the GPIO polarity should be non-inverted (GPIOOUT_INVx = 0) to achieve an active low pin.

APPLICATION NOTE: LEDs are typically set to open-drain operation by setting GPIOOUT_PPx = 0.

Blinking is configured via the ACTIVITY_LED_BLINK_TIME register.

FIGURE 3-33: LINE PORT LEDS



3.12 GPIOs

LAN8267 provides 40 GPIOs with the following functionality:

- Each pin can function as a normal GPIO which can operate as an Input, Output or I/O.
  - GPIOFUN_SELx must be set to a 1 for the GPIO mode.
  - There are is no explicit “GPIO output data bit” for software to control. GPIO output data is normally a 0 when the GPIO output is enabled. The GPIO output can be set to 1 by inverting the output (setting GPIOOUT_INVx = 1).
  - GPIO outputs are selectable push-pull or open drain. If configured as an open drain output or I/O pin, an external pull-up resistor is always required for proper operation.
  - Each GPIO pin can be configured to be an interrupt source.

  Note: Internal pull-ups are enabled by default but are only meant to prevent floating inputs.

- Alternately, each pin can be configured as an Alternate Function. Alternate Functions support one optical module interface per Line Port, two Aggregate Interrupts to an external Host CPU and two LEDs per Line port.
  - GPIOFUN_SELx must be set to a 0 for the Alternate Function to be selected.
  - GPIOOUT_ENx must be set to a 1 for the Alternate Function to be output.
  - The GPIOOUT_INVx can be used to invert the Alternate Function.
  - Alternate Function outputs are selectable push-pull or open drain.

- By default all pins default to GPIOs, have internal pull-up enabled, are output disabled, open-drain and non-inverted
- GPIOFUN_SELx = 1, GPIOOUT_ENx = 0, GPIOOUT_PPx = 0, GPIOOUT_INVx = 0).

Note: Some optical module interface signals are supported as standard GPIOs (i.e. no extra hardware) while some connect through an Alternate Function path.

Note: GPIO and interrupt source input paths continue to function while configured as an Alternate Function (thus allowing software and hardware to monitor pin states).

Note: For Alternate Functions (which have an input path) set as a GPIO, the Alternate Function input value is set inactive as stated in Table 3-10

For GPIOs which do not have an Alternate Function output, the Alternate Function output value is to be a ‘1’. Assuming GPIOOUT_INVx = 0, if the GPIOFUN_SELx is set for ‘Alternate Function’ the pin will not be driven.

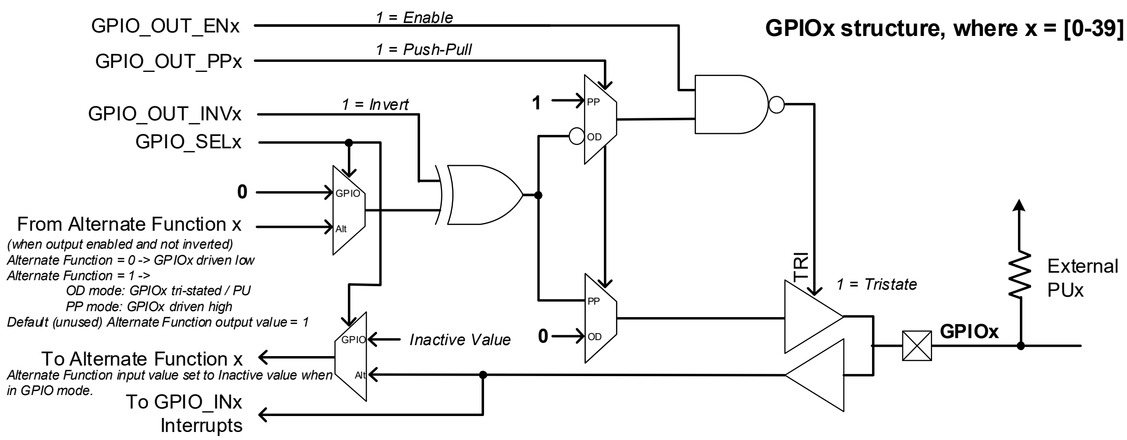
The GPIO output logic is as follows:

TABLE 3-9: GPIO OUTPUT TRUTH TABLE

<table>
<tr><th>GPIOOUT_ENx
(0=disabled
1=enabled)</th><th>GPIOFUN_SELx
(0=alternate
1=GPIO)</th><th>GPIOOUT_PPx
(0=open-drain
1=push-pull)</th><th>GPIOOUT_INVx
(0=non-inverted
1=inverted)</th><th>Alt Function</th><th>GPIOx Output</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>Hi-Z (PU)</td></tr>
<tr><td rowspan="12">1</td><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td>X</td><td>0</td></tr>
<tr><td>1</td><td>X</td><td>Hi-Z (PU)</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>X</td><td>0</td></tr>
<tr><td>1</td><td>X</td><td>1</td></tr>
<tr><td rowspan="8">0</td><td rowspan="4">0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>Hi-Z (PU)</td></tr>
<tr><td>1</td><td>0</td><td>Hi-Z (PU)</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td rowspan="4">1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>

Figure 3-34 shows a high-level view of a representative GPIO. This structure is repeated per GPIO.

FIGURE 3-34: GPIO STRUCTURE



LAN8267 GPIO functions are described in Table 3-10

TABLE 3-10: SUPPORTED GPIO FUNCTIONS

GPIO	Alternate Function	Internal Mapping	Setting	System Purpose	
GPIO0	-		GPIO (Output)	CH0_RATESEL0 / PDOWN / RST	Line Port 0 Module Interface
GPIO1	-		GPIO (Input)	CH0_MOD_ABS	
GPIO2	CH0_TWI_HST_SCL	CH0 TWI Host	Alt Fn (Output)	CH0_TWI_HST_SCL	
GPIO3	CH0_TWI_HST_SDA	CH0 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH0_TWI_HST_SDA	
GPIO4	-		GPIO (Output)	CH0_TX_DIS	
GPIO5	-		GPIO (Input)	CH0_TX_FAULT	
GPIO6	CH0_Optical_LOS	CH0 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH0_RXLOS	
	-	-		CH0_INTL	
GPIO7	CH0_RX_LED	CH0 LP LED logic	Alt Fn (Output)	CH0_LINK_LED	Line Port 0 Link LED
GPIO8	-		GPIO (Output)	CH1_RATESEL0 / PDOWN / RST	Line Port 1 Module Interface
GPIO9	-		GPIO (Input)	CH1_MOD_ABS	
GPIO10	CH1_TWI_HST_SCL	CH1 TWI Host	Alt Fn (Output)	CH1_TWI_HST_SCL	
GPIO11	CH1_TWI_HST_SDA	CH1 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH1_TWI_HST_SDA	
GPIO12	-		GPIO (Output)	CH1_TX_DIS	
GPIO13	-		GPIO (Input)	CH1_TX_FAULT	
GPIO14	CH1_Optical_LOS	CH1 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH1_RXLOS	
	-	-		CH1_INTL	
GPIO15	CH1_RX_LED	CH1 LP LED logic	Alt Fn (Output)	CH1_LINK_LED	Line Port 1 Link LED

TABLE 3-10: SUPPORTED GPIO FUNCTIONS (CONTINUED)

GPIO	Alternate Function	Internal Mapping	Setting	System Purpose	
GPIO16	-		GPIO (Output)	CH2_RATESEL0 / PDOWN / RST	Line Port 2 Module Interface
GPIO17	-		GPIO (Input)	CH2_MOD_ABS	
GPIO18	CH2_TWI_HST_SCL	CH2 TWI Host	Alt Fn (Output)	CH2_TWI_HST_SCL	
GPIO19	CH2_TWI_HST_SDA	CH2 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH2_TWI_HST_SDA	
GPIO20	-		GPIO (Output)	CH2_TX_DIS	
GPIO21	-		GPIO (Input)	CH2_TX_FAULT	
GPIO22	CH2_Optical_LOS	CH2 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH2_RXLOS	
	-	-		CH2_INTL	
GPIO23	CH2_RX_LED	CH2 LP LED logic	Alt Fn (Output)	CH2_LINK_LED	Line Port 2 Link LED
GPIO24	-		GPIO (Output)	CH3_RATESEL0 / PDOWN / RST	Line Port 3 Module Interface
GPIO25	-		GPIO (Input)	CH3_MOD_ABS	
GPIO26	CH3_TWI_HST_SCL	CH3 TWI Host	Alt Fn (Output)	CH3_TWI_HST_SCL	
GPIO27	CH3_TWI_HST_SDA	CH3 TWI Host Inactive Value = 0	Alt Fn (I/O)	CH3_TWI_HST_SDA	
GPIO28	-		GPIO (Output)	CH3_TX_DIS	
GPIO29	-		GPIO (Input)	CH3_TX_FAULT	
GPIO30	CH3_Optical_LOS	CH3 PCS LOS logic Inactive Value = 0	Alt Fn (Input)	CH3_RXLOS	
	-	-		CH3_INTL	
GPIO31	CH3_RX_LED	CH3 LP LED logic	Alt Fn (Output)	CH3_LINK_LED	Line Port 3 Link LED
GPIO32	-	-	GPIO (Output)	GPIO32	Available GPIO
GPIO33	-	-	GPIO (Output)	GPIO33	Available GPIO
GPIO34	INTR_A	Aggregate Interrupt 0	Alt Fn (Output)	INTR_A	Host CPU Interrupts
GPIO35	INTR_B	Aggregate Interrupt 1	Alt Fn (Output)	INTR_B	
GPIO36	CH0_TX_LED	CH0 LP LED logic	Alt Fn (Output)	CH0_ACTIVITY_LED	Line Ports 0-3 Activity LEDs
GPIO37	CH1_TX_LED	CH1 LP LED logic	Alt Fn (Output)	CH1_ACTIVITY_LED	
GPIO38	CH2_TX_LED	CH2 LP LED logic	Alt Fn (Output)	CH2_ACTIVITY_LED	
GPIO39	CH3_TX_LED	CH3 LP LED logic	Alt Fn (Output)	CH3_ACTIVITY_LED	

3.12.1 GPIO INTERRUPTS

Each GPIO pin can be configured as an interrupt source. The pin must be configured as an input and will generate an input upon state change. The minimum pulse width that must be reliably detected is 100 ns. Any smaller pulse may or may not be detected.

APPLICATION NOTE: Following reset(s) a false GPIO interrupt might be indicated due to the settling of the change detect logic.

GPIOs are always enabled as inputs. Any pin change due to GPIO or Alternate Function output will cause a GPIO interrupt.

3.13 Resets and Power-On Self-Test

3.13.1 RESETS

LAN8267 supports the following resets.

- Global Hardware Reset
  - Global Hardware Reset is asserted by the RESET_N pin input which is required at power-up and available for the system to initiate a full chip reset without cycling power.
  - Global Hardware Reset resets all chip functions except PLLs and clocks.
- Global Software Reset
  - Global Software Reset is asserted by Software writing to the appropriate GLOBAL_FAST_RESET or BLOCK_LEVEL_SOFTWARE_RESET1 register bit. Global Fast reset bits are self-clearing.
  - The Global Software Reset resets all chip functions except PLLs, clocks, GPIOs, and certain Global functions.
- Global Software Block Resets
  - Global Software Block Resets are asserted by Software writing to the appropriate BLOCK_LEVEL_SOFTWARE_RESET1/2. Global Software Block reset bits are self-clearing.
- Host Slice and Line Slice Software Resets
  - Host Slice and Line Slice Software Resets are asserted by Software writing to the appropriate BLOCK_LEVEL_SOFTWARE_RESET1 or GLOBAL_FAST_RESET register bits. Global Fast reset bits are self-clearing.
  - Slice Software Resets reset the Slice logic, as well as the applicable Slice interface of the Cross-Connect.
- CSR Ring Software Resets
  CSR Ring Software Resets are asserted by Software writing to the appropriate GLOBAL_FAST_RESET register bit.

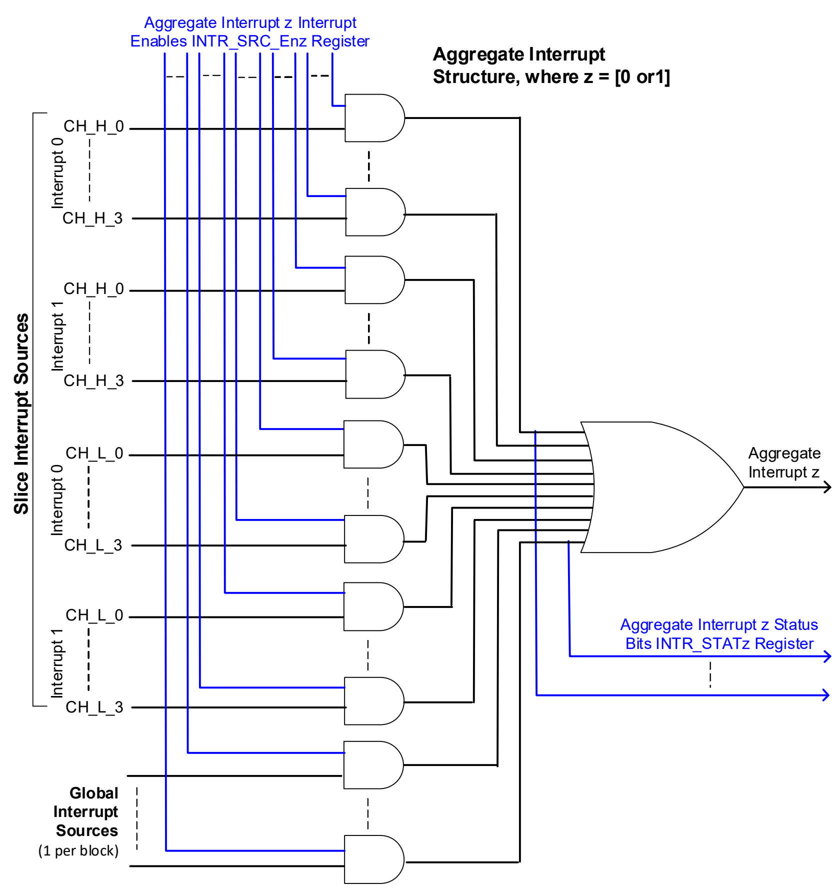
3.14 Host Interrupts

LAN8267 supports two Aggregate Interrupts to an external Host CPU, Aggregate Interrupt 0 and Aggregate Interrupt 1, each of which can be generated from any of the following interrupt sources:

- Any slice-level interrupt source
- Any chip-level interrupt source

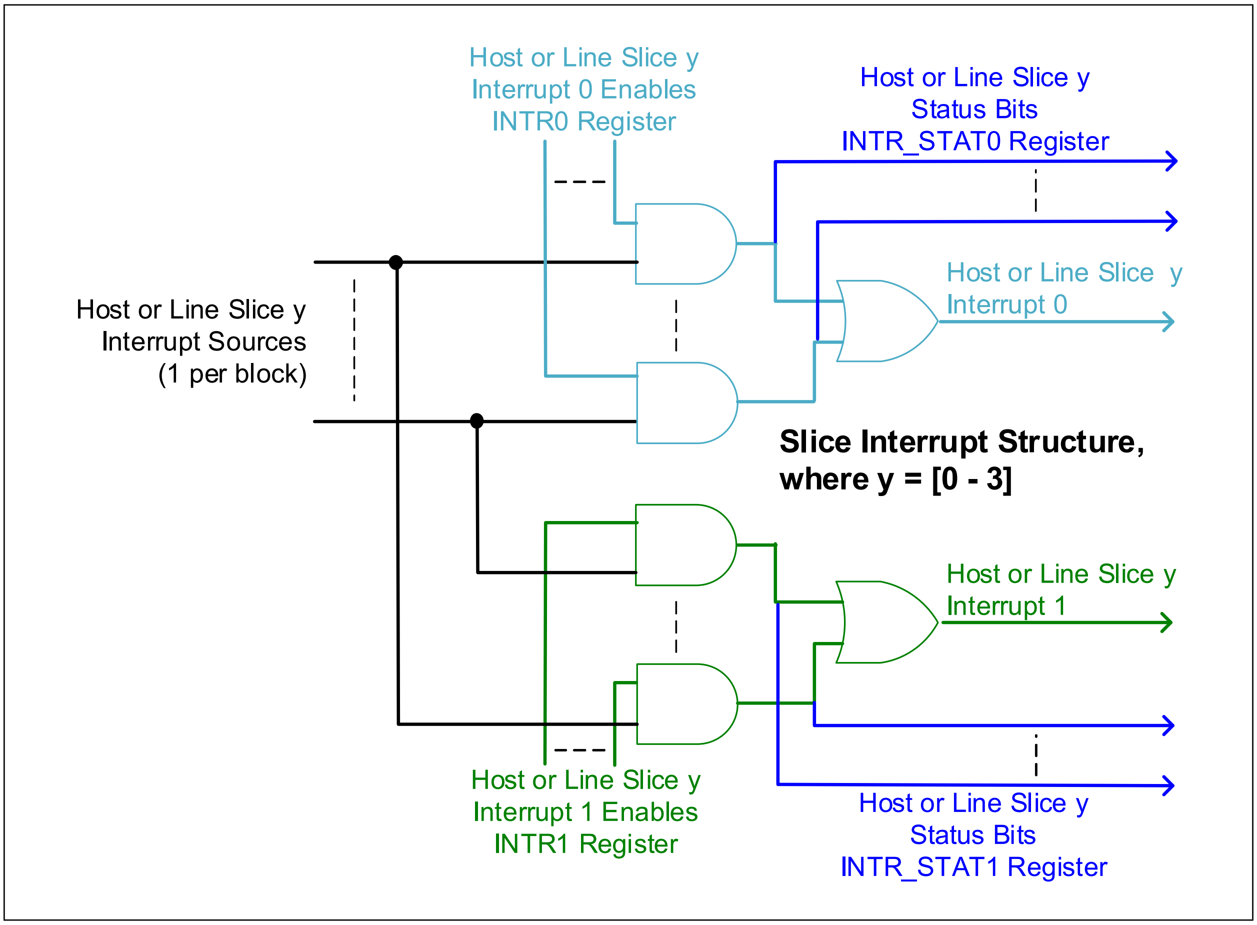
Figure 3-35 shows how interrupts are generated and is repeated for each of the two Aggregate Interrupts. Interrupts are active high by default but can be active low by inverting the GPIO pin.

FIGURE 3-35: GLOBAL AGGREGATE INTERRUPTS



Each of the four Host slices generates a CH_H_0 and a CH_H_1 interrupt and each of the four Line slices generates a CH_L_0 and a CH_L_1 interrupt. Each of the Host slice interrupts is identical as is each of the Line slice interrupts.

FIGURE 3-36: SLICE INTERRUPTS



Interrupt Masks (Enables) are organized as follows:

- Aggregate Interrupt 0: The global ISR INTR_SRC_EN0 register contains an enable bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Aggregate Interrupt 1: The global ISR INTR_SRC_EN1 register contains an enable bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Slice interrupts: Each Host slice and each Line slice has an INTR0 register for its Slice Interrupt 0 and an INTR1 register for its Slice Interrupt 1. In these registers is an interrupt enable bit for each slice-level block with interrupt capability.
- Each chip-level and slice-level block with interrupt capability contains a register with a mask or enable bit for each interrupt in the block.

Effectively slice-level interrupts have 3 levels of enable, one at the Aggregate level, one at the slice level and one at each block. Chip-level interrupts have 2 levels of enable, one at the Aggregate level and one at each block.

Interrupt Status is organized as follows:

- Aggregate Interrupt 0: The global INTR_STAT0 register contains a read-only, masked interrupt status bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Aggregate Interrupt 1: The global INTR_STAT1 register contains a read-only, masked interrupt status bit for each chip-level block with interrupt capability, the eight Slice Interrupts 0 and the eight Slice Interrupts 1.
- Slice interrupts: Each Host slice and each Line slice has an INTR_STAT0 register for its Slice Interrupt 0 and an INTR_STAT1 register for its Slice Interrupt 1. In these registers is a read-only, masked interrupt status bit for each slice-level block with interrupt capability.
- Each chip-level and slice-level block with interrupt capability contains one or more interrupt status registers with a

status bit for each interrupt in the block. Interrupts are latched and cleared at this level.

Effectively slice-level interrupts have 3 levels of status, one at the Aggregate level, one at the slice level and one at each block. Chip-level interrupts have 2 levels of status, one at the Aggregate level and one at each block. Note the status at the Aggregate and slice levels return the masked interrupts while the status at the block level return the unmasked interrupts.

3.15 JTAG

The device includes an integrated JTAG test port. The interface consists of five standard pins (TDI, TDO, TCK, TMS and TRST). A sixth pin, JTAG_SEL, is used for test mode. The JTAG interface conforms to the IEEE Standard 1149.1 - 2001 Standard Test Access Port (TAP) and Boundary-Scan Architecture.

3.15.1 TEST TAP CONTROLLER

All input and output data is synchronous to the TCK test clock input. TAP input signals TMS and TDI are clocked into the test logic on the rising edge of TCK, while the output signal TDO is clocked on the falling edge.

The implemented IEEE 1149.1 instructions and their op codes are shown in the following table. The length of the instruction is 4 bits.

TABLE 3-11: IEEE 1149.1 OP CODES

Instruction	Op Code	Comment
BYPASS 0	all 0’s	Mandatory Instruction
BYPASS 1	all 1’s	Mandatory Instruction
SAMPLE	0101	Mandatory Instruction
EXTEST	0001	Mandatory Instruction
CLAMP	0000	Optional Instruction
ID_CODE	1000	Optional Instruction
HIGHZ	0110	Optional Instruction
INTEST	0100	Optional Instruction
EXTEST_PULSE	0010	Mandatory Instruction for 1149.6
EXTEST_TRAIN	0011	Mandatory Instruction for 1149.6
HOSTIJTAG 1	0111	Mandatory AccessLink Instruction for IEEE 1687 (iJTAG)

Access to device test mode registers are implemented with private instructions as listed in the LAN8267 Test Controller Specification.

3.15.1.1 JTAG Timing Requirements

The JTAG test tap must run at 25 MHz or better.

3.15.2 TEST MODES

Test modes are accessed via the JTAG interface when the JTAG_SEL pin is set low. Test modes are selected using internal user data registers. The functionality of the test controller is left to design.

At design discretion, RAM and ROM BIST maybe directly controlled by test registers or may be controlled using the BIST registers in the CSR Ring.

3.15.3 CSR RING ACCESS

JTAG test mode may access the CSR Ring registers.

JTAG test mode access to the CSR Ring registers will statically take over the CSR Ring Origins from the PHY management interface.

As opposed to using the channel number / MMD / register mapping scheme that is used by the SPI and MDIO accesses, JTAG access to the CSR Ring registers will directly specify the ring number, target ID and full register address.

3.15.4 BOUNDARY SCAN

Standard JTAG 1149.1 boundary scan is provided on the digital pins.

The SerDeses' TX and RX pairs support AC boundary scan (JTAG 1149.6). Some support logic is required.

3.16 Miscellaneous

3.16.1 POWER MANAGEMENT

LAN8267 supports the following Power Management capabilities:

SerDes

Each SerDes may be dynamically powered down to save power.

Data Path Clocks

Each SerDes CMU supports powering down its VCO and various clock drivers effectively providing clock gating to each slice's data path.

3.16.2 WARM RESTART

Hardware support for software based Warm Restart.

3.16.3 TEMPERATURE SENSOR

LAN8267 contains a Temperature Sensor with accuracy of ±1.5°C (to be finalized during characterization). It is read and controlled via registers in the GLOBAL target.

3.17 Configuration Straps

3.17.1 FUNCTION MODE STRAPS

Several pin based straps are available to select firmware, Host software or hardware implemented options.

Configuration straps are multi-function pins that are driven as outputs during normal operation. During a System Reset (**RESET_N**) these outputs are not driven. The externally pulled high or low state of the signal is latched following deassertion of **RESET_N** and is used to determine the value of the Strap_Read register and the default value of the Strap_Override register.

Note: Functional configuration straps include internal pull-down resistors.

Bit assignments are as follows.

Note: Firmware or Host software implemented assignments are non-hardware committed in that they can be redefined in the future.

TABLE 3-12: STRAP PIN ASSIGNMENTS

Bit	Description	Pin or logic level	Firmware, Software or Hardware
7	Test	TEST (Note 1)	Firmware
6	unused	‘b0	n/a
5	unused	‘b0	n/a
4	unused	‘b0	n/a
3	BIST Bypass (BIST_BYPASS_STRAP)	FAILOVEROUT1	Software, Firmware, Hardware
2	Reserved Strap1	FAILOVEROUT0	n/a
1	RESERVED	0	
0	RESERVED	0	

1: Not really a strap, but rather a the live pin value.

Note: The system designer must guarantee that configuration straps meet the timing requirements. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note: When externally pulling configuration straps high the strap should be tied to the VDDO associated with the shared pin.

A 16-bit Strap_Override register allows for Host software determined reconfiguration as well as for extra option bits.

4.0 OPERATIONAL CHARACTERISTICS

4.1 Absolute Maximum Ratings*

Supply Voltage (**VDD**) (Note 4-1) .... -0.3V to +0.99V

Supply Voltage (**VDDHS_N, VDDHS_S, VDDHV_N, VDDHV_S**) .... -0.3V to +1.10V

Supply Voltage (**VDDH18_N, VDDH18_S, VDDO_18, VDDA_SYSPLL, VDDA_1588APLL**) .... -0.3V to +1.96V

Variable Supply Voltage (**VDDO_A, VDDO_B**) .... -0.3V to +3.465V

Positive voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground .... **VDDO_A/B** +0.5V

Negative voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground .... -0.5V

Positive voltage on input signal pins (referenced to **VDDO_18**), with respect to ground .... +2.1V

Negative voltage on input signal pins (referenced to **VDDO_18**), with respect to ground .... -0.5V

LVDS input signal pins voltage, with respect to ground .... 0V to +2.4V

Storage Temperature .... -55°C to +150°C

Lead Temperature Range .... Refer to JEDEC Spec. J-STD-020

HBM ESD Performance (**RXIN[0:3]N/P, TXOUT[0:3]N/P, RXOUT[0:3]N/P, TXIN[0:3]N/P**) .... +/-1 kV

HBM ESD Performance (all others) .... +/-2 kV

CDM ESD Performance .... +/-200V

Note 4-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 4.2, Operating Conditions**, Section 4.5, DC Specifications, or any other applicable section of this specification is not implied.

4.2 Operating Conditions**

Supply Voltage (**VDD**) .... (+/-5%) 0.855V to +0.945V

Supply Voltage @ 1 Gbps / 10 Gbps (**VDDHS_N, VDDHS_S, VDDHV_N, VDDHV_S**) .... (+/-5%) 0.95V to +1.05V

Supply Voltage (**VDDH18_N, VDDH18_S, VDDO_18, VDDA_SYSPLL, VDDA_1588APLL**) .... (+/-5%) 1.71V to +1.89V

Variable Supply Voltage, @1.8V (**VDDO_A, VDDO_B**) .... (+/-5%) 1.71V to +1.89V

Variable Supply Voltage, @3.3V (**VDDO_A, VDDO_B**) .... (+/-5%) 3.135V to +3.465V

Positive voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground .... **VDDO_A/B** +0.5V

Negative voltage on input signal pins (referenced to **VDDO_A, VDDO_B**), with respect to ground .... -0.5V

Positive voltage on input signal pins (referenced to **VDDO_18**), with respect to ground .... +2.1V

Negative voltage on input signal pins (referenced to **VDDO_18**), with respect to ground .... -0.5V

LVDS input signal pins voltage, with respect to ground .... 0V to +2.4V

Operating Temperature .... T_A= -40°C to T_J=110°C

**Proper operation of the device is guaranteed only within the ranges specified in this section.

4.3 Package Thermal Specifications

4.3.1 256-BGA

TABLE 4-1: PACKAGE THERMAL PARAMETERS (256-BGA)

Symbol	Value	Units	Notes
Θ_{JA}	14.38	°C/W	0 Meters/second
	11.42	°C/W	1 Meters/second
	10.39	°C/W	2.5 Meters/second
Θ_{JB}	2.82	°C/W	
Θ_{JC}	0.70	°C/W	
Ψ_{JT}	0.25	°C/W	

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

4.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation at various operating voltages. Power dissipation is impacted by temperature, supply voltage and external source/sink requirements.

Power dissipation is impacted by temperature, supply voltage and external source/sink requirements. All worst-case measurements were taken at the maximum temperature/voltages from the Operating Conditions. All typical measurements were taken at +25°C unless otherwise noted.

4.4.1 WORST CASE FOUR PORT OPERATION

All worst case measurements were taken at voltage +5% and maximum operating temperature unless otherwise noted.

TABLE 4-2: WORST CASE 10G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL VDDA_1588APLL/ VDDO_18 Total (mA) (Note 4-2)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 10 Gbps, 100% utilization	1360	70	2040	10	305	30	30	4323
4 ports Host/Line 10 Gbps, 100% utilization, PTP enabled	1526	70	2040	10	305	30	30	4480
After Hardware Reset Deassertion	400	70	628	10	30	40	20	1413

Note 4-2 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_1588APLL.

4.4.2 TYPICAL USAGE FOUR PORT OPERATION

All typical usage measurements were taken at +25°C unless otherwise noted.

TABLE 4-3: TYPICAL USAGE 10G FOUR PORT (0.9V, 1.0V, 1.0V, 1.8V, 1.8V, 3.3V)

Modes	0.9V VDD Total (mA)	1.0V VDDHV_N/S Total (mA)	1.0V VDDHS_N/S Total (mA)	1.8V VDDA_SYSPLL VDDA_1588APLL/ VDDO_18 Total (mA) (Note 4-3)	1.8V VDDH18_N/S Total (mA)	3.3V VDDO_A Total (mA)	3.3V VDDO_B Total (mA)	Total Power (mW)
4 ports Host/Line 10 Gbps, 100% utilization	605	70	1862	10	300	20	30	3264
4 ports Host/Line 10 Gbps, 100% utilization, PTP enabled	745	70	1862	10	300	20	30	3390
After Hardware Reset Deassertion	226	70	650	10	30	20	30	1194

Note 4-3 VDDO_18 is its own power rail and operates independently of VDDA_SYSPLL/VDDA_1588APLL.

4.5 DC Specifications

TABLE 4-4: DC ELECTRICAL CHARACTERISTICS FOR 1.8V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
Low Input Level	V_{IL}	-	0.693	V	Non-Schmitt mode
High Input Level	V_{IH}	1	-	V	Non-Schmitt mode
Schmitt Mode Falling Trip Point	V_{T-}	0.3*VDDO_18	0.6*VDDO_18	V	
Schmitt Mode Rising Trip Point	V_{T+}	0.4*VDDO_18	0.7*VDDO_18	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.1*VDDO_18	0.4*VDDO_18	V	
Input Leakage (V_{IN} = VSS or VDDO_18)	I_{IH}	-5	5	µA	Note 4-4
Pull-Up Resistance (V_{IN} = VSS)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = VDDO_18)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA
High Output Level	V_{OH}	VDDO_18 - 0.4	-	V	I_{OH} = 4/8/16/20 mA

Note 4-4 This specification applies to all inputs and three-stated bi-directional pins.

TABLE 4-5: DC ELECTRICAL CHARACTERISTICS FOR SELECTABLE 1.8V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
1.8V Operation					
Low Input Level	V_{IL}	-0.3	0.693	V	Non-Schmitt mode
High Input Level	V_{IH}	1	2.28	V	Non-Schmitt mode
Schmitt Mode Low Input Level	V_{IL}	0.3*VDDO_A/B	0.6*VDDO_A/B	V	Note 4-5
Schmitt Mode High Input Level	V_{IH}	0.4*VDDO_A/B	0.7*VDDO_A/B	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.1*VDDO_A/B	-	V	
Input Leakage (V_{IN} = VSS or VDDO_A/B)	I_{IH}	-40	20	µA	
Pull-Up Resistance (V_{IN} = VSS)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = VDDO_A/B)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA Note 4-6
High Output Level	V_{OH}	VDDO_A/B - 0.4	-	V	I_{OH} = 4/8/16/20 mA Note 4-6
DC Sinking Current	I_{SINK}	-	10	mA	Note 4-7
DC Sourcing Current	I_{SOURCE}	-	10	mA	Note 4-7

Note 4-5 This specification applies to all inputs and three-stated bi-directional pins.

Note 4-6 The I_{OH}/I_{OL} values are NOT the actual DC currents supported for a lifetime of 10 years. The Electro-migration limit determines the maximum current supported under various modes of operation. The DC current supported for a lifetime of 10 years is defined as I_{SOURCE} and I_{SINK}.

Note 4-7 The max. DC current drive is obtained by setting drive strength to 20 mA. Under this mode the IO can sink 10 mA average current for 10 years within the limits of acceptable EM degradation.

TABLE 4-6: DC ELECTRICAL CHARACTERISTICS FOR SELECTABLE 3.3V LVCMOS I/O

Parameter	Symbol	Min	Max	Units	Notes
3.3V Operation					
Low Input Level	V_{IL}	-0.3	1.22	V	Non-Schmitt mode
High Input Level	V_{IH}	1.93	**VDDO_A/B** + 0.3	V	Non-Schmitt mode
Schmitt Mode Low Input Level	V_{IL}	0.7	1.9	V	
Schmitt Mode High Input Level	V_{IH}	0.9	2.1	V	
Schmitt Mode Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	0.3	-	V	
Input Leakage (V_{IN} = **VSS** or **VDDO_A/B**)	I_{IH}	-40	20	µA	Note 4-8
Pull-Up Resistance (V_{IN} = **VSS**)	R_{DPU}	10	-	kΩ	
Pull-Down Resistance (V_{IN} = **VDDO_A/B**)	R_{DPD}	10	-	kΩ	
Low Output Level	V_{OL}	-	0.4	V	I_{OL} = -4/8/16/20 mA Note 4-9
High Output Level	V_{OH}	**VDDO_A/B** - 0.4	-	V	I_{OH} = 4/8/16/20 mA Note 4-9
DC Sinking Current	I_{SINK}	-	10	mA	Note 4-10
DC Sourcing Current	I_{SOURCE}	-	10	mA	Note 4-10

Note 4-8 This specification applies to all inputs and three-stated bi-directional pins.

Note 4-9 The I_{OH}/I_{OL} values are NOT the actual DC currents supported for a lifetime of 10 years. The Electromigration limit determines the maximum current supported under various modes of operation. The DC current supported for a lifetime of 10 years is defined as I_{SOURCE} and I_{SINK}.

Note 4-10 The max. DC current drive is obtained by setting drive strength to 20 mA. Under this mode the IO can sink 10 mA average current for 10 years within the limits of acceptable EM degradation.

4.5.1 SYSREFCK AND LREFCK CLOCK INPUTS DC ELECTRICAL CHARACTERISTICS

TABLE 4-7: SYSREFCK AND LREFCK DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units
Clock source output DC Impedance	Z_{C-DC}	40	50	60	Ω Note 4-12
Input DC differential termination	R_I	80	-	100	Ω Note 4-13
Differential peak-to-peak input swing	$\|V_{ID}\|$	600	-	1600	mVppd Note 4-14
Input common-mode voltage	V_{CM}	-	900	-	mV

Note 4-11 Clock signal must be AC coupled.

Note 4-12 50 ohm DPLL Clock output termination used

Note 4-13 100ohm differential input termination used

Note 4-14 Covered 400mV and 800mV

4.5.2 SERDES DC ELECTRICAL CHARACTERISTICS

TABLE 4-8: SD25G TRANSMITTER

Parameter	Symbol	Min	Typical	Max	Units	Condition
Differential resistance	R_{DIFF}	80	100	120	Ω	-

Note 4-15 Differential output swing is register configurable.

Note 4-16 The minimum drive level is the lowest guaranteed drive level achievable with the maximum amplitude configuration applied.

TABLE 4-9: SD25G RECEIVER

Parameter	Symbol	Min	Typical	Max	Units	Condition
Differential peak-to-peak input voltage	V_{I_DIFF}	100	-	1200	mVppd	Clean eye sensitivity Note 4-17
AC-Coupling Note 4-18	-	-	-	100	nF	Note 4-19

Note 4-17 RX JTOL testing covered.

Note 4-18 AC-coupling should be done at receiver.

Note 4-19 100nf AC cap used for testing

4.6 AC Specifications

4.6.1 POWER SEQUENCING

During power on and off, **VDDHS_S**, **VDDHS_N**, **VDDHV_S**, and **VDDHV_N** must never be more than 300 mV above **VDD**. The maximum rising slope of the **VDDHS_S, VDDHS_N, VDDHV_S, VDDHV_N**, **VDDH18_S,** and **VDDH18_N** supplies during power turn-on must be below 5 V/ms to limit the inrush current.

In summary, the following power up sequence should be followed: 0.9V before 1.0V before 1.8V before 3.3V. The **RESET_N** and **TRST** inputs must be held low until all power supply voltages have reached their recommended operating condition values.

4.6.2 SYSREFCK AND LREFCK CLOCK INPUTS AC ELECTRICAL CHARACTERISTICS

TABLE 4-10: SYSREFCK AND LREFCK AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Condition
REFCLK frequency Note 4-20	f	-100 ppm	156.25	100 ppm	MHz	-
Clock duty cycle	-	40	-	60	%	Measured at 50% threshold
Rise time and fall time	t_R, t_F	-	-	0.5	ns	Within ±200 mV relative to common mode.
REFCLK input peak-to-peak jitter, bandwidth from 2.5 kHz to 10 MHz Note 4-21	-	-	-	30	ps	-

Note 4-20 SYSREFCK and LREFCK must be frequency synchronous.

Note 4-21 Peak-to-peak values are typically higher than the RMS value by a factor of 10 to 14.

4.6.3 SERDES AC ELECTRICAL CHARACTERISTICS

This section describes the AC specifications for the SerDes transceiver. The transceiver supports:

- SFP
- 1000BASE
- 10GBASE

Table 4-11 lists the AC characteristics for the SerDes transmitter.

TABLE 4-11: 1G SFP, 1000BASE-KX TRANSMITTER OUTPUT

Parameter	Symbol	Min	Max	Units	Condition
Data Rate	-	1.25 - 100 ppm	1.25 + 100 ppm	Gbps	SFP (SFP-MSA), 1000BASE-KX (IEEE 802.3, clause 70)
Rise time and fall time Note 4-22	t_R, t_F	35.6	320	ps	20% to 80%, 1000BASE-KX
Random jitter	R_J	-	0.15	UI_{PP}	At BER 10-12, 1000BASE-KX
Deterministic jitter	D_J	-	0.15	UI_{PP}	At BER 10-12, 1000BASE-KX
Total jitter	T_J	-	0.25	UI_{PP}	At BER 10-12, 1000BASE-KX
Eye mask	X1	-	0.125	UI	
Eye mask	X2	-	0.325	UI	
Eye mask	Y1	350	-	mV	
Eye mask	Y2	-	800	mV	

Note 4-22 Slew rate is programmable.

Table 4-12 lists the AC characteristics for the SerDes transmitter.

TABLE 4-12: 1G SFP, 1000BASE-KX RECEIVER

Parameter	Symbol	Min	Max	Units	Condition
Data Rate	-	1.25 - 100 ppm	1.25 + 100 ppm	Gbps	SFP 1000BASE-KX
Differential input return loss	RLI_{SDD11}	-	-10	dB	50 MHz to 1289 MHz
Differential input return loss	RLI_{SDD11}	-	-10 + 13.275 x log (ƒ/1289 MHz)	dB	1289 MHz to 3750 MHz
Common-mode input return loss	RLO_{SCC11}	- -	-7 + 13.275 x log (ƒ/1250 MHz)	dB	100 MHz to 1250 MHz 1250 MHz to 3750 MHz
Jitter tolerance, total Note 4-23	TOL_{TJ}	600	-	ps	1G mode measured according to IEEE 802.3 Clause 38.6.8
Jitter tolerance, deterministic Note 4-23	TOL_{DJ}	370	-	ps	1G mode measured according to IEEE 802.3 Clause 38.6.8
Wideband SyncE jitter tolerance	WJT	312.5	-	UI_{P-P}	1G mode. 10 Hz to 12.1 Hz. Measured according to ITU-T G.8262, section 9.2
Wideband SyncE jitter tolerance	WJT	3750/ƒ	-	UI_{P-P}	1G mode. 12.1 Hz to 2.5 kHz (ƒ). Measured according to ITU-T G.8262, section 9.2
Wideband SyncE jitter tolerance	WJT	1.5	-	UI_{P-P}	1G mode. 2.5 kHz to 50 kHz. Measured according to ITU-T G.8262, section 9.2

Note 4-23 Jitter requirements represent high-frequency jitter (above 637 kHz) and not low-frequency jitter or wander.

TABLE 4-13: 10G TRANSMITTER OUTPUT (SFI POINT B, HOST)

Parameter	Symbol	Min	Max	Units	Condition
Termination mismatch	ΔZ_M	-	5	%	-
AC common-mode voltage	V_{OCM_AC}	-	15	mV_{RMS}	Note 4-24
Total jitter Note 4-24	T_J	-	0.28	UI	Note 4-24
Data-dependent jitter	DDJ	-	0.1	UI	Note 4-24
Pulse shrinkage jitter	DDPWS	-	0.062	UI_{RMS}	Measured at point B, as specified in SFF-8431, revision 4.1. 6 dB channel loss (For 9 dB channel loss, worst case is 0.08 UI) Note 4-25
Uncorrelated jitter	UJ	-	0.023	UI_{RMS}	Note 4-24
Eye mask	X1	-	0.12	UI	Measured at 5e-5 mask hit ratio Note 4-24
Eye mask	X2	-	0.33	UI	Measured at 5e-5 mask hit ratio Note 4-24
Eye mask	Y1	95	-	mV	Measured at 5e-5 mask hit ratio Maximum SFI Channel loss of 3 dB Note 4-24
Eye mast	Y2	-	350	mV	Note 4-24

Note 4-24 With a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 10G output.

Note 4-25 Measure at Point B as specified in SFF-8431, revision 4.1. A test channel of 5.5 dB insertion loss at 5.156 GHz was used.

TABLE 4-14: 10G RECEIVER INPUT (SFI POINT C AND C”, HOST)

Parameter	Symbol	Min	Max	Units	Condition
Pulse width shrinkage jitter	$DDPWS_{JIT\_P-P}$	-	0.3	UI	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask X1	X1	-	0.35	UI	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask Y1	Y1	150	-	mV	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1
Eye mask Y2	Y2	-	425	mV	Calibrated and measured at point C”, as specified in SFF-8431, revision 4.1

TABLE 4-15: 10GBASE-KR TRANSMITTER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	10.3125 - 100 ppm	10.3125 + 100 ppm	Gbps	KR
Differential output return loss Note 4-26	RLO_{SDD22}	-	-9	dB	50 MHz to 2.5 GHz
Differential output return loss	RLO_{SDD22}	-	-9 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz
Common-mode output return loss	RLO_{SCC22}	-	-6	dB	50 MHz to 2.5 GHz
Common-mode output return loss	RLO_{SCC22}	-	-6 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz
Rise time and fall time	t_R, t_F	-	47	UI_{P-P}	-
Random jitter	R_J	-	0.15	UI_{P-P}	-
Deterministic jitter	D_J	-	0.15	UI_{P-P}	-
Duty cycle distortion (part of DJ)	DCD	-	0.035	UI_{P-P}	-
Total jitter Note 4-27	TJ	-	0.28	UI_{P-P}	-

Note 4-26 Informative, system related: maximum insertion loss is 15 dB @ 5 Ghz (10 Gbps) (vs ~25 dB based on the KR spec). This is to allow low cost interface implementation, while meeting system requirements.

Note 4-27 With a jitter-free reference clock. Any **REFCLK** jitter with a frequency content below 7 MHz will add to the jitter generated at the 10 Gbps output.

TABLE 4-16: 10GBASE-KR RECEIVER

Parameter	Symbol	Min	Max	Units	Condition
Data rate	-	10.3125 - 100 ppm	10.3125 + 100 ppm	Gbps	KR
Differential input return loss Note 4-28	RLI_{SDD11}	-	-9	dB	50 MHz to 2.5 GHz
Differential input return loss	RLI_{SDD11}	-	-9 + 12 x log (ƒ/2.5 GHz)	dB	2.5 GHz to 7.5 GHz

Note 4-28 Maximum insertion loss is 15 dB @ 5 GHz (10 Gbps) (vs ~25 dB based on the KR spec). This is to allow low cost interface implementation, while meeting system requirements.

4.6.4 TWI HOST TIMING

This section specifies the Twisted Wire Interface format and timing of the device.

FIGURE 4-1: TWI HOST TIMING

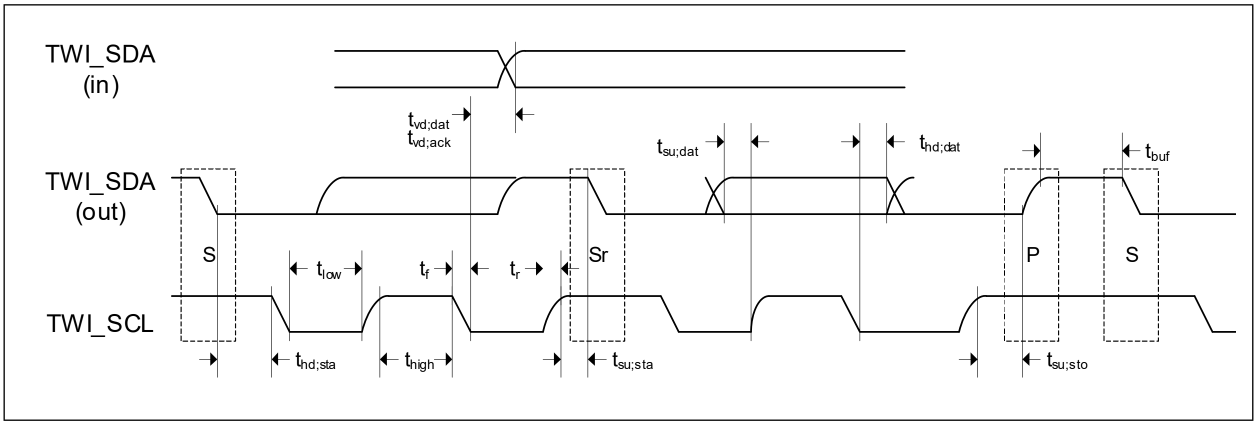


TABLE 4-17: TWI HOST TIMING VALUES

Symbol	Description	Standard Mode		Fast Mode		Fast Mode Plus		
		Min	Max	Min	Max	Min	Max	Units
f_{scl}	TWI_SCL clock frequency		100		400		1000	kHz
t_{high}	TWI_SCL high time (Note 4-29)	3.0		0.6		0.26		µs
t_{low}	TWI_SCL low time (Note 4-30)	4.7		1.2		0.48		µs
t_r	Rise time of TWI_SDA and TWI_SCL		1000		300		120	ns
t_f	Fall time of TWI_SDA and TWI_SCL		300		300		120	ns
$t_{su;sta}$	Setup time (provided to client) of TWI_SCL high before TWI_SDA output falling for repeated start condition (Note 4-31)	4.9		0.9		0.38		µs
$t_{hd;sta}$	Hold time (provided to client) of TWI_SCL after TWI_SDA output low for start or repeated start condition (Note 4-32)	4.5		0.9		0.38		µs
$t_{vd;dat}$	TWI_SDA data input valid (from client) after TWI_SCL low. (Note 4-33)		3400		850		400	ns
$t_{vd;ack}$	TWI_SDA acknowledge input valid (from client) after TWI_SCL low (Note 4-33)		3400		850		400	ns
$t_{su;dat}$	Setup time (provided to client) TWI_SDA output before TWI_SCL rising (Note 4-33)	300		150		100		ns
$t_{hd;dat}$	Hold time (provided to client) of TWI_SDA output after TWI_SCL falling (Note 4-33)	50	3400	50	850	50		ns
$t_{su;sto}$	Setup time (provided to client) of TWI_SCL high before TWI_SDA output rising for stop condition (Note 4-32)	4.5		0.9		0.38		µs

TABLE 4-17: TWI HOST TIMING VALUES (CONTINUED)

Symbol	Description	Standard Mode		Fast Mode		Fast Mode Plus		
		Min	Max	Min	Max	Min	Max	Units
t_{buf}	Bus free time	4.7		1.3		0.5		µs
C_B	Capacitive load for TWI_SCL and TWI_SDA bus line		400		330			pF
R_P	External pull-up resistor (Note 4-34)	900	8 x 10^{-7}/ C_B	900	3 x 10^{-7}/ C_B			Ω

Note 4-29 Assumes worst case rise time and zero fall time. Nominally t_{high} is 40% of the period.

Note 4-30 Assumes worst case fall time and zero rise time. Nominally t_{low} is 60% of the period.

Note 4-31 These values provide 200, 300 and 120 (respectively) ns of margin compared to the I^2C specification.

Note 4-32 These values provide 500, 300 and 120 (respectively) ns of margin compared to the I^2C specification.

Note 4-33 These values provide 50 ns of margin compared to the I^2C specification.

Note 4-34 Minimum value is determined from IOL and internal reliability requirements. Maximum value is determined by load capacitance. Microchip recommends 10 kΩ for typical applications in which capacitance loads are below the specified minimums.

Note 4-35 Assumes a drive strength setting of 4 ma.

4.6.5 MDC/MDIO CLIENT

This section specifies the MDC/MDIO format and timing of the device.

FIGURE 4-2: MDC/MDIO TIMING

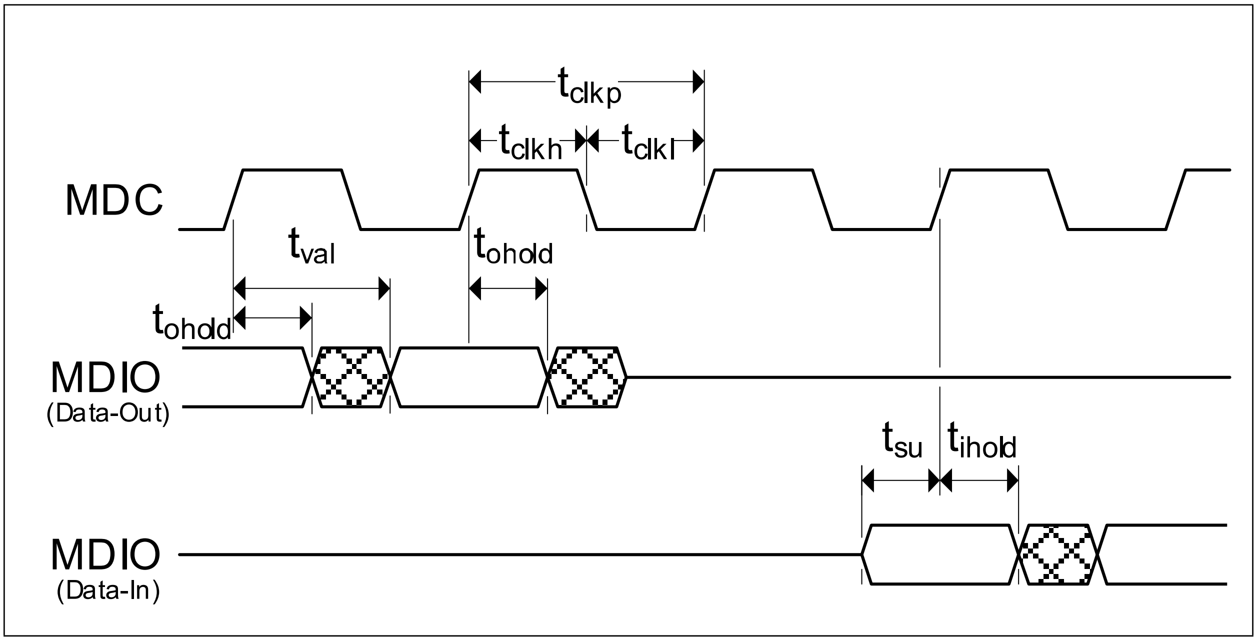


TABLE 4-18: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	**MDC** period	40	400	Note 4-36	ns
t_{clkh}	**MDC** high time	10			ns
t_{clkl}	**MDC** low time	10			ns
t_{val}	**MDIO** (read from PHY) output valid from rising edge of **MDC**	0		14	ns
t_{ohold}	**MDIO** (read from PHY) output hold from rising edge of **MDC**	0			ns
t_{su}	**MDIO** (write to PHY) input setup time to rising edge of **MDC**	8 Note 4-37			ns
t_{ihold}	**MDIO** (write to PHY) input hold time after rising edge of **MDC**	8 Note 4-37			ns

Note 4-36 As a client, the device can operate with MDC clock frequencies as low as in the range of 10s/100s of Hertz as could be generated by the host using bit banging techniques on its GPIO pins. There is no maximum clock period.

Note 4-37 These values provide 2 ns margin beyond the IEEE specification.

Note 4-38 Assumes PCB loading of 5 pf. Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default. Higher drive settings may achieve faster times especially at higher PCB loading.

4.6.6 SPI CLIENT

This section specifies the SPI format and timing of the device.t

FIGURE 4-3: SPI CLIENT NORMAL MODE

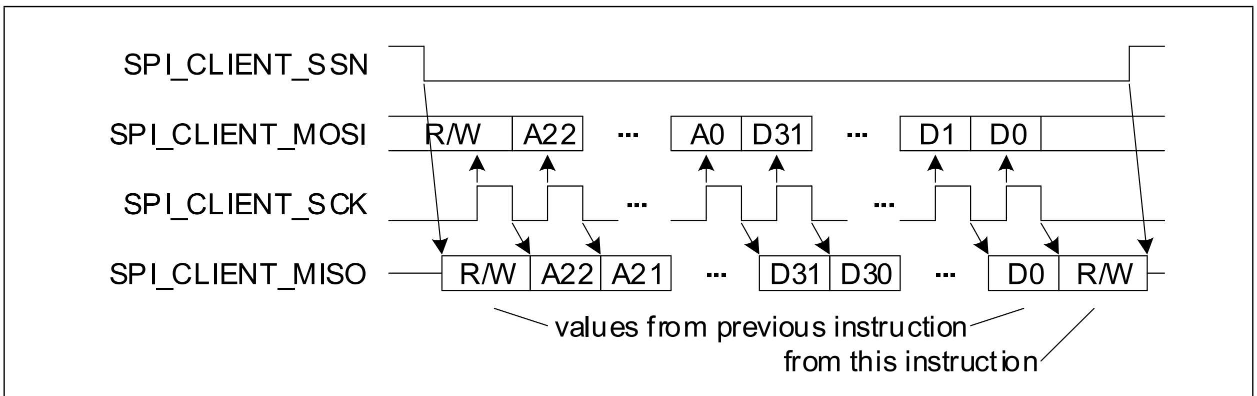


FIGURE 4-4: SPI CLIENT FAST MODE

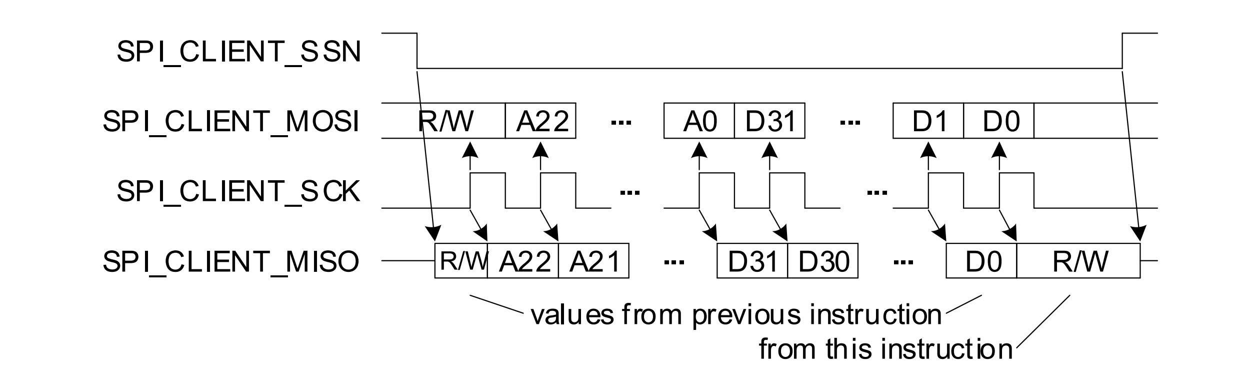


FIGURE 4-5: SPI CLIENT TIMING

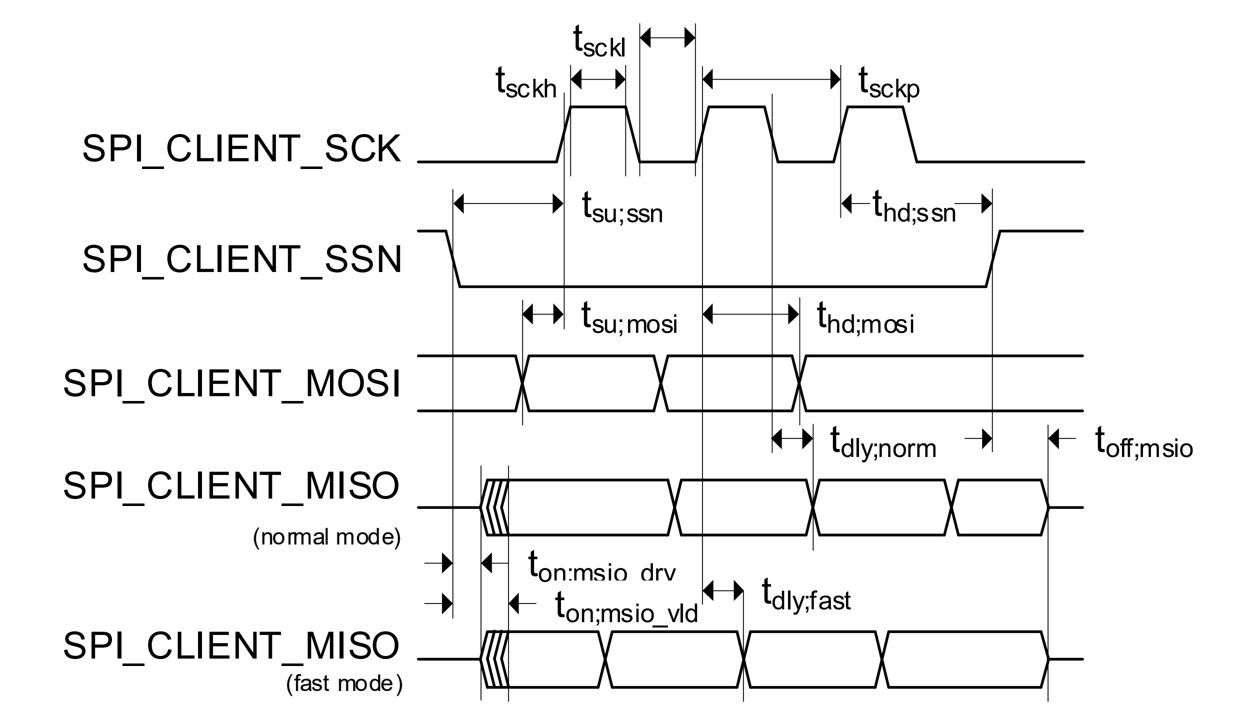


TABLE 4-19: SPI CLIENT TIMING VALUES

Symbol	Description	Min	Max	Units
t_{sckp}	SPI_CLIENT_SCK period - normal mode	50	Note 4-39	ns
	SPI_CLIENT_SCK period - fast mode	22	Note 4-39	ns

TABLE 4-19: SPI CLIENT TIMING VALUES (CONTINUED)

Symbol	Description	Min	Max	Units
t_{sckh}	**SPI_CLIENT_SCK** high time - normal mode	22		ns
	SPI_CLIENT_SCK high time - fast mode	8		ns
t_{sckl}	**SPI_CLIENT_SCK** low time - normal mode	22		ns
	SPI_CLIENT_SCK low time - fast mode	8		ns
$t_{su;mosi}$	**SPI_CLIENT_MOSI** data setup time to **SPI_CLIENT_SCK** rising	8		ns
$t_{hd;mosi}$	**SPI_CLIENT_MOSI** data hold time from **SPI_CLIENT_SCK** rising	8		ns
$t_{su;ssn}$	**SPI_CLIENT_SSN** active setup time to **SPI_CLIENT_SCK** rising	12		ns
$t_{hd;ssn}$	**SPI_CLIENT_SSN** inactive hold time from **SPI_CLIENT_SCK** rising	SCK period + 12		ns
$t_{on;miso\_drv}$	**SPI_CLIENT_SSN** transition low to **SPI_CLIENT_MISO** drive	0		ns
$t_{on;miso\_vld}$	**SPI_CLIENT_SSN** transition low to **SPI_CLIENT_MISO** valid		8 / 13 / 18 Note 4-41	ns
$t_{off;miso}$	**SPI_CLIENT_SSN** transition high to **SPI_CLIENT_MISO** high impedance		10	ns
$t_{dly;norm}$	Falling **SPI_CLIENT_SCK** to valid **SPI_CLIENT_MISO** data, normal mode	6 Note 4-40	16 / 20 / 25 Note 4-41	ns
$t_{dly;fast}$	Rising **SPI_CLIENT_SCK** to valid **SPI_CLIENT_MISO** data, fast mode	6 Note 4-40	16 / 20 / 25 Note 4-41	ns

Note 4-39 The device can operate with clock frequencies in the 10s/100s of Hertz.

Note 4-40 Guaranteed by design minimum of 2 system clock periods at 300 MHz.

Note 4-41 Assumes PCB loading of 5 pf, 50 pf and 100 pf respectively.
Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default. Higher drive settings may achieve faster times especially at higher PCB loading

Device input to output time only. Does not include PCB routing delay or host setup time.

The data output propagation delay may require delayed data sampling at the Host (i.e. data output is valid into the next clock cycle) or the use of a lower frequency.

4.6.7 PPS AND LSC INPUTS/OUTPUTS

4.6.7.1 Input Timing

This section specifies the input timing of the device.

FIGURE 4-6: PTP EXTERNAL (2-PIN) SYNCHRONOUS PPS, PPS W/TOD INPUT TIMING

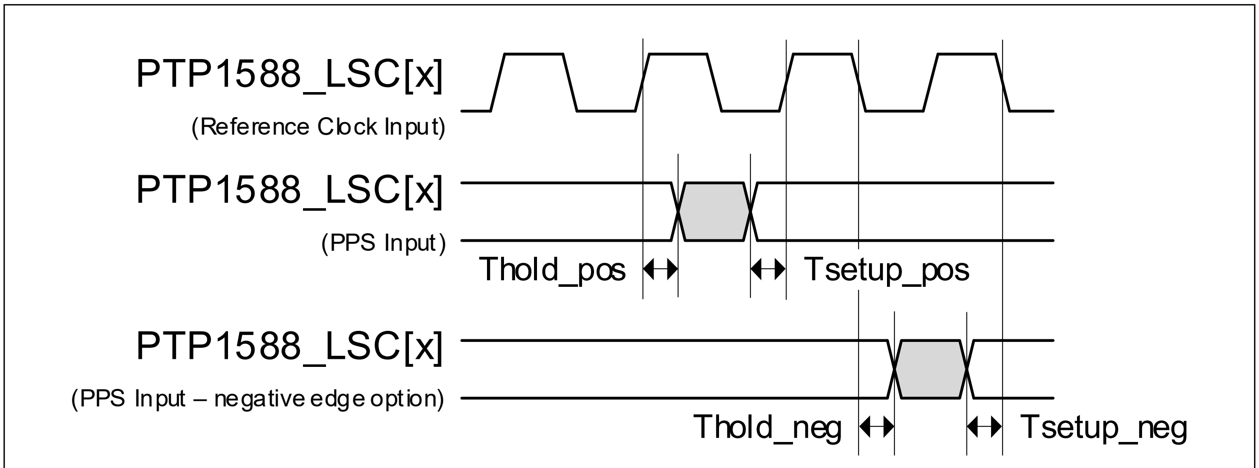


TABLE 4-20: PTP EXTERNAL (2-PIN) SYNCHRONOUS PPS, PPS W/TOD INPUT TIMING VALUES

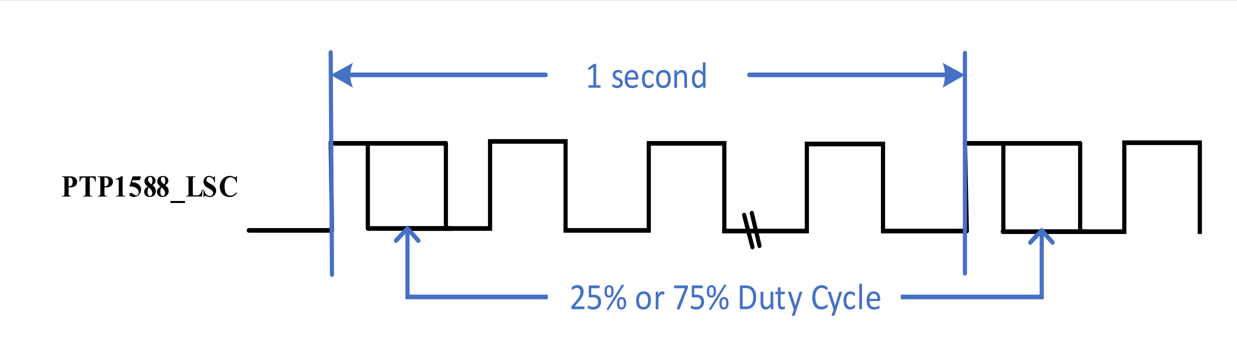
Symbol	Description	Min	Typ	Max	Units
t_{setup_pos}	PPS input setup to Reference clock rising when negative sampling option is disabled.	2			ns
t_{hold_pos}	PPS input hold from Reference clock rising when negative sampling option is disabled.	2			ns
t_{setup_neg}	PPS input setup to Reference clock falling when negative sampling option is enabled.	2			ns
t_{hold_neg}	PPS input hold from Reference clock falling when negative sampling option is enabled.	2			ns

4.6.7.2 PTP1588_LSC[x] Reference Clock Timing

This section specifies the **PTP1588_LSC[x]** reference clock timing of the device.

- Non ePPS mode
  - Duty Cycle: (40% minimum, 50% typical, 60% maximum)
  - Jitter: < 100 ps rms
  - Frequency: 25 MHz, 50 MHz, or 125 MHz ± 50 ppm
- ePPS mode
  - Duty Cycle except for ePPS edge: (40% minimum, 50% typical, 60% maximum)
  - Duty cycle at ePPS edge: (20% minimum, 25% typical, 30% maximum) or (70% minimum, 75% typical, 80% maximum)
  - Jitter: < 100 ps rms
  - Frequency: 25 MHz or 50 MHz ± 50 ppm

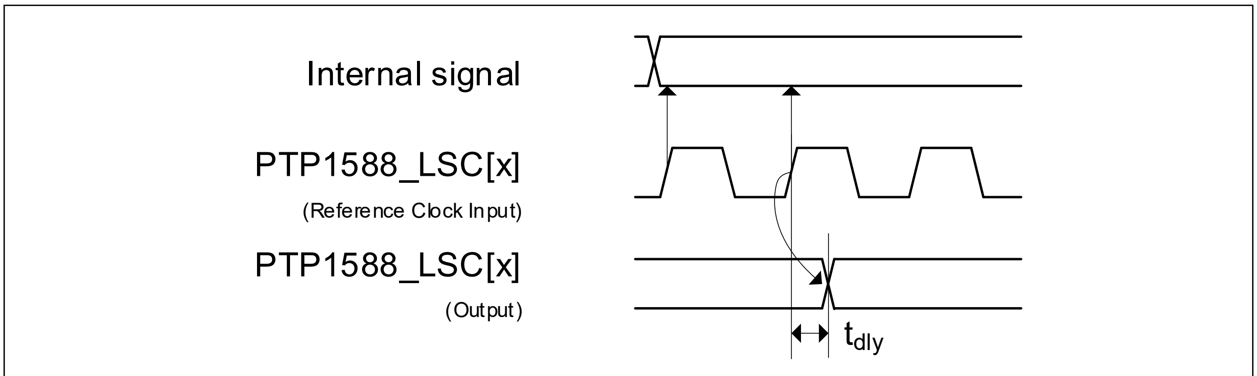
FIGURE 4-7: 1588 REFERENCE CLOCK TIMING



4.6.7.3 Output Timing

This section specifies the output timing of the device.

FIGURE 4-8: PTP RE-SYNCHRONIZED OUTPUT TIMING



Note: There is an implicit one-cycle internal propagation delay from the PTP1588_LSC[x] reference clock input update of internal time-of-day register, before the bit value is driven to an output PTP1588_LSC[x] pin. The implicit delay is shown in the Figure 4-8, included in the min-5/max-15 nanoseconds t_dly shown. It should be noted that this is not applicable to the ePPS output mode shown in Figure 4-9.

FIGURE 4-9: PTP EPPS OUTPUT TIMING

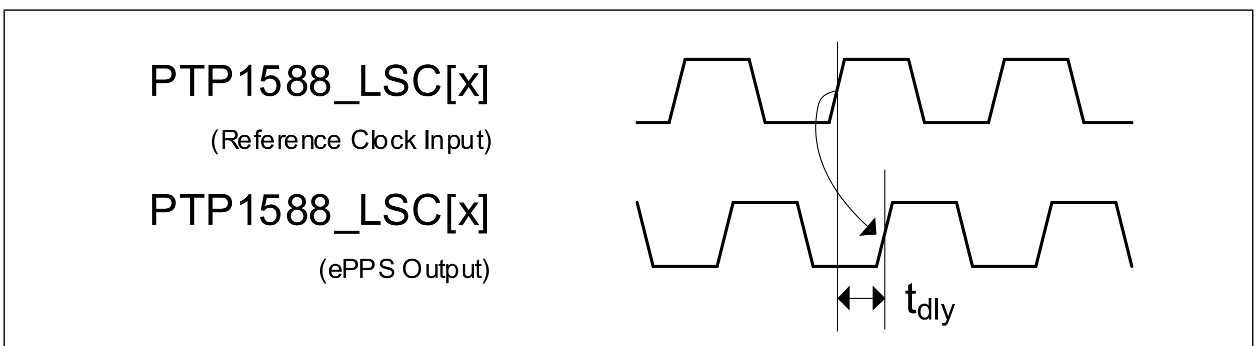


TABLE 4-21: PTP EPPS OUTPUT TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{dly}	Reference clock in to ePPS output	2		10	ns
Note: Assumes PCB loading of 5 pf. Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default.					

TABLE 4-22: EPPS OUTPUT SUMMARY

PTP1588_LSC[0-3] pins (no divider)		
Input	Input (MHz)	ePPS (MHz)
PTP1588_LSC[0-3]	50	50
	25	25
	10	

4.6.8 SERIAL TIMESTAMP INTERFACE (STI) FORMAT & TIMING

This section specifies the 1588 Serial Timestamp Interface format and timing of the device.

FIGURE 4-10: 1588 SERIAL TIMESTAMP INTERFACE FORMAT AND TIMING (MAX SIZE)

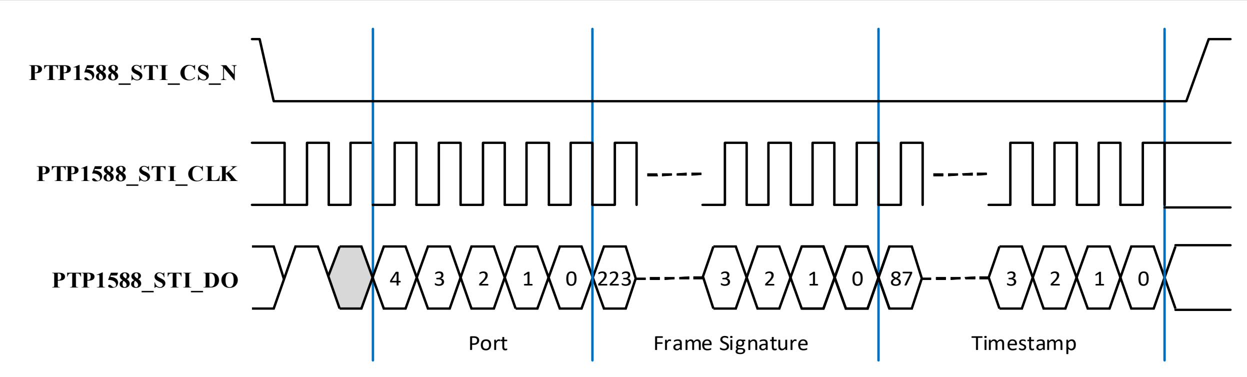


TABLE 4-23: 1588 SERIAL TIMESTAMP INTERFACE TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	**PTP1588_STI_CLK** period	12.56		50.27	ns
$t_{clkduty}$	**PTP1588_STI_CLK** duty cycle (Note 4-43)	40		60	%
t_{cs_val}	**PTP1588_STI_CS_N** output valid prior to rising edge of **PTP1588_STI_CLK**	4			ns
t_{cs_hold}	**PTP1588_STI_CS_N** output hold time after rising edge of **PTP1588_STI_CLK**	4			ns

TABLE 4-23: 1588 SERIAL TIMESTAMP INTERFACE TIMING VALUES (CONTINUED)

t_{do_val}	**PTP1588_STI_DO** output valid prior to rising edge of **PTP1588_STI_CLK**	4			ns
t_{do_hold}	**PTP1588_STI_DO** output hold time after rising edge of **PTP1588_STI_CLK**	4			ns

Note 4-42 Assumes PCB loading of 5 pf. Assumes a drive strength setting of 8 ma. Note that 8 ma is not the device default. Higher drive settings may achieve faster times especially at higher PCB loading.

Note 4-43 Assumes a nominal 50/50 duty cycle when PTP_STI:TS_FIFO_SI:TS_FIFO_SI_CFG.SI_CLK_HI_CYCS and SI_CLK_LO_CYCS have the same value. For unequal values, the duty cycle range is the nominal +/-10%.

4.6.9 RECOVERED CLOCK TIMING REQUIREMENTS

The recovered clock output duty cycle requirement is 40% minimum, 50% typical, 60% maximum.

TABLE 4-24: RECOVERED CLOCK RISE / FALL TIME

Symbol	Description	Condition	Min	Typ	Max	Units
t_{rise}	Rise time	8 ma drive, 10 pF load, 3.3V IO Supply	0.67	0.84	1.15	ns
		8 ma drive, 10 pF load, 1.8V IO Supply	0.71	0.85	0.90	ns
		8 ma drive, 25 pF load, 3.3V IO Supply	1.31	1.64	2.27	ns
		8 ma drive, 25 pF load, 1.8V IO Supply	1.30	1.58	1.68	ns
t_{fall}	Fall time	8 ma drive, 10 pF load, 3.3V IO Supply	0.61	0.73	0.98	ns
		8 ma drive, 10 pF load, 1.8V IO Supply	0.69	0.83	0.86	ns
		8 ma drive, 25 pF load, 3.3V IO Supply	1.15	1.39	1.50	ns
		8 ma drive, 25 pF load, 1.8V IO Supply	1.24	1.51	1.60	ns

TABLE 4-25: RECOVERED CLOCK OUT FREQUENCIES

Operating Mode	Internal Recovered Clock Frequency (MHz)	N	Recovered Clock Out Frequency (MHz)
1G	125.00	1	125.00
		2	62.50
		4	31.25
		8	15.625
10G	257.8125	1	Reserved
		2	128.90625
		4	64.453125
		8	32.2265625

4.6.10 RESET PIN CONFIGURATION STRAP TIMING

Figure 4-11 illustrates the **RESET_N** timing requirements and its relation to the configuration straps. In addition to the specified power and clock stable minimum duration, **RESET_N** must be asserted for the minimum period specified.

FIGURE 4-11: RESET_N CONFIGURATION STRAP TIMING

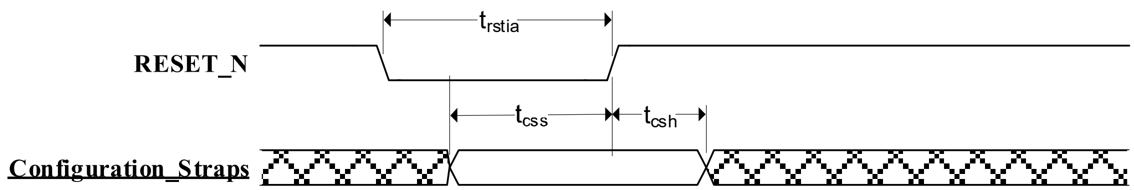


TABLE 4-26: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Max	Units
t_{rstia}	**RESET_N** input assertion time	1		µs
t_{css}	Configuration strap setup before **RESET_N** deassertion	10		ns
t_{csh}	Configuration strap hold after **RESET_N** deassertion	10		ns
t_{odad}	Output drive after **RESET_N** deassertion	150		ns

4.6.11 JTAG TIMING VALUES

4.6.11.1 JTAG Timing Requirements

The JTAG test tap must run at 25 MHz or better.

FIGURE 4-12: JTAG TIMING

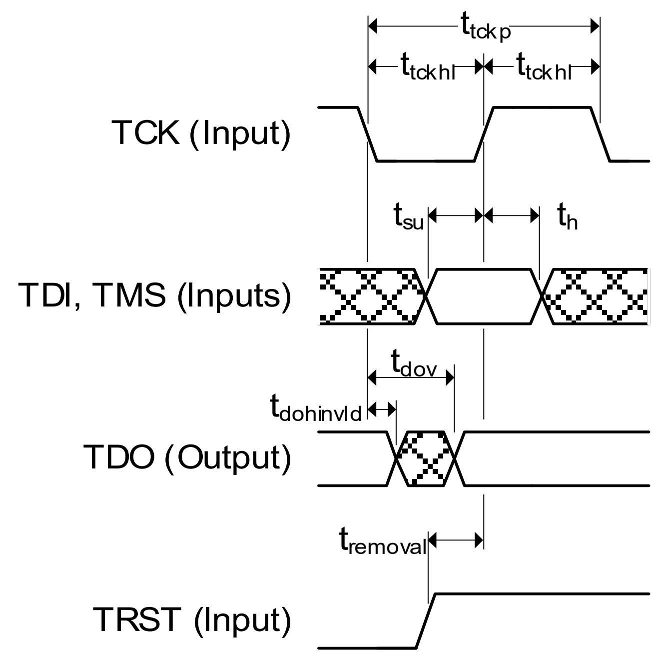
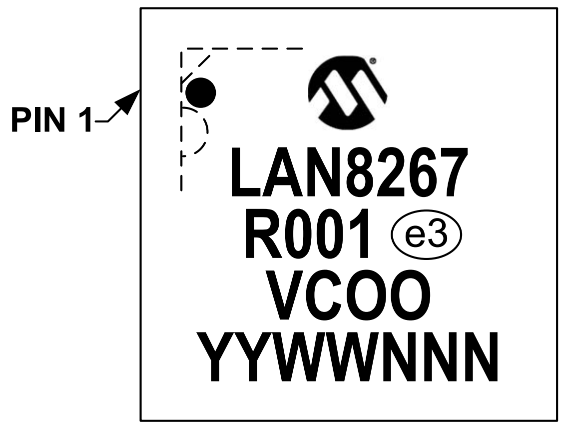


TABLE 4-27: JTAG TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{tckp}	**TCK** clock period	40		ns	ns
t_{tckhl}	**TCK** clock high/low time	t_{tckp}*0.4		t_{tckp}*0.6	ns
t_{su}	**TDI**, **TMS** setup to **TCK** rising edge	10			ns
t_h	**TDI**, **TMS** hold from **TCK** rising edge	10			ns
t_{dov}	**TDO** output valid from **TCK** falling edge			16	ns
$t_{doinvld}$	**TDO** output invalid from **TCK** falling edge	0			ns
$t_{removal}$	**TRST** release before **TCK** rising edge	10			ns
Note: Assumes PCB loading of 25 pf. Assumes a drive strength setting of 8 mA.					

5.0 PACKAGE INFORMATION

5.1 Top Marking



Legend:

R	Product revision
000	Internal code
e3	Pb-free JEDEC® designator for Matte Tin (Sn)
V	Plant of assembly
COO	Country of origin
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code

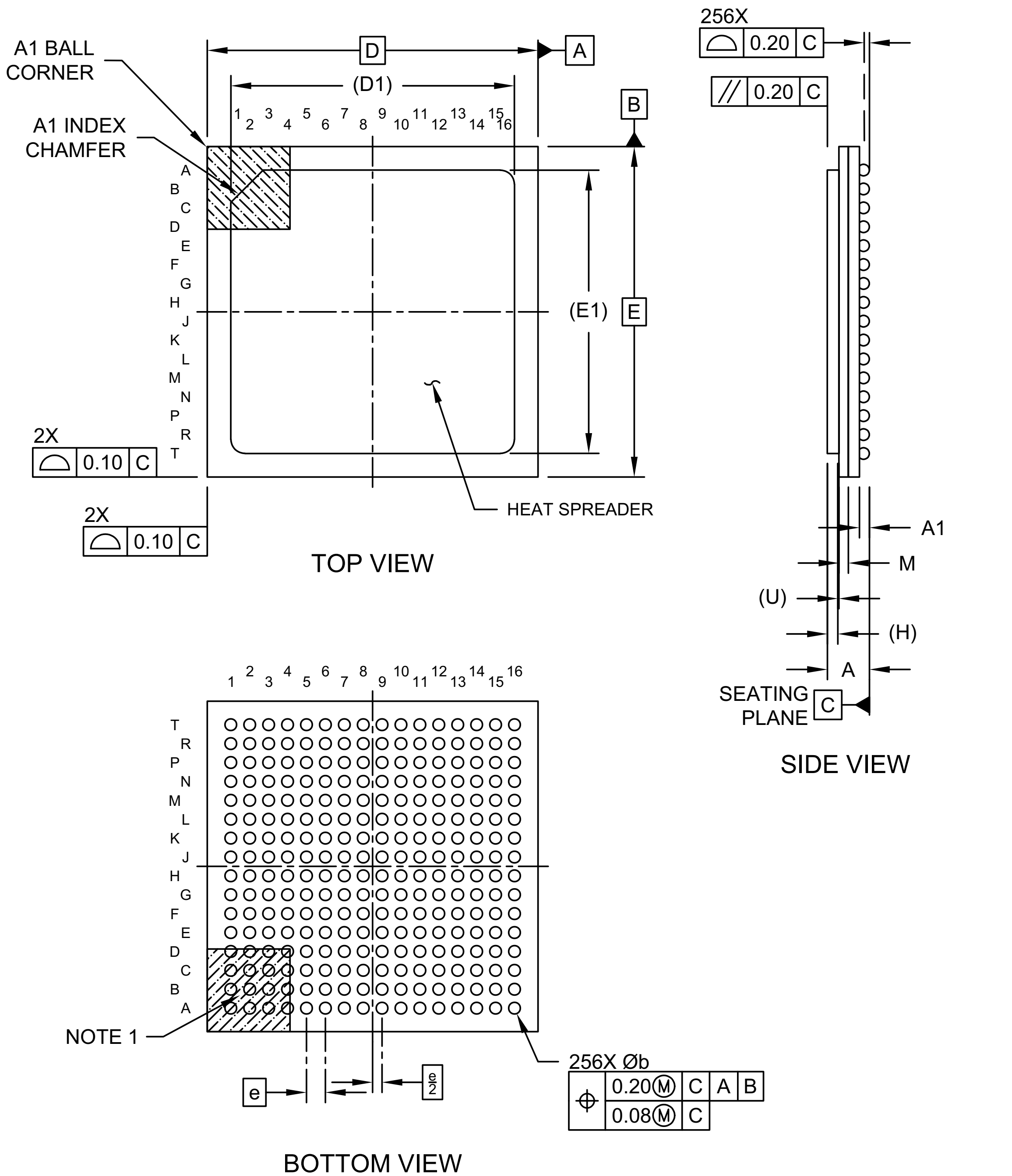
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information

5.2 256-BGA

FIGURE 5-1: 256-BGA PACKAGE DRAWING

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

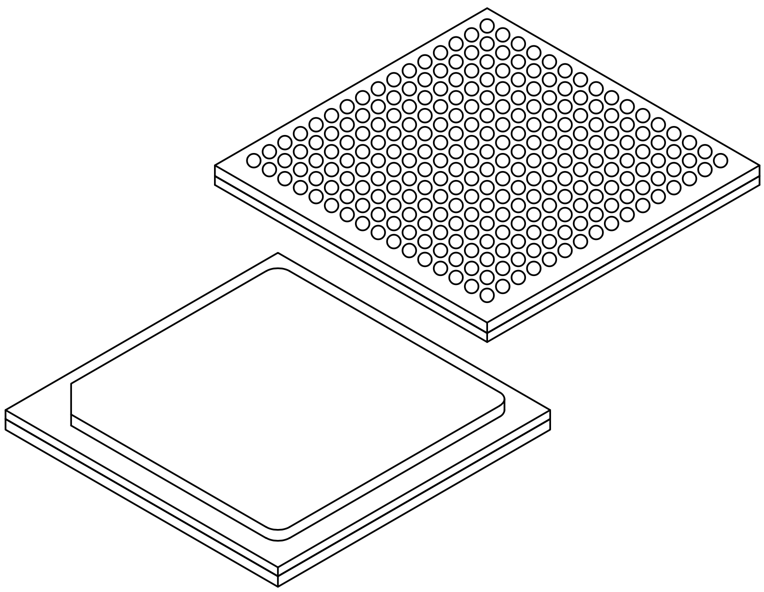


Microchip Technology Drawing C04-563 Rev B Sheet 1 of 2

FIGURE 5-2: 256-BGA DIMENSIONS

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		256	
Pitch	e		0.80 BSC	
Overall Height	A	1.48	1.63	1.78
Ball Height	A1	0.37	0.42	0.47
Mold Cap Thickness	M	0.35	0.40	0.45
Heat Seperator Epoxy Thickness	U		0.05 REF	
Heat Spreader Thickness	H		0.30 REF	
Overall Length	D		14.00 BSC	
Heat Spreader Length	D1		12.00 REF	
Overall Width	E		14.00 BSC	
Heat Spreader Width	E1		12.00 REF	
Ball Diameter	b	0.46	0.51	0.56

Notes:

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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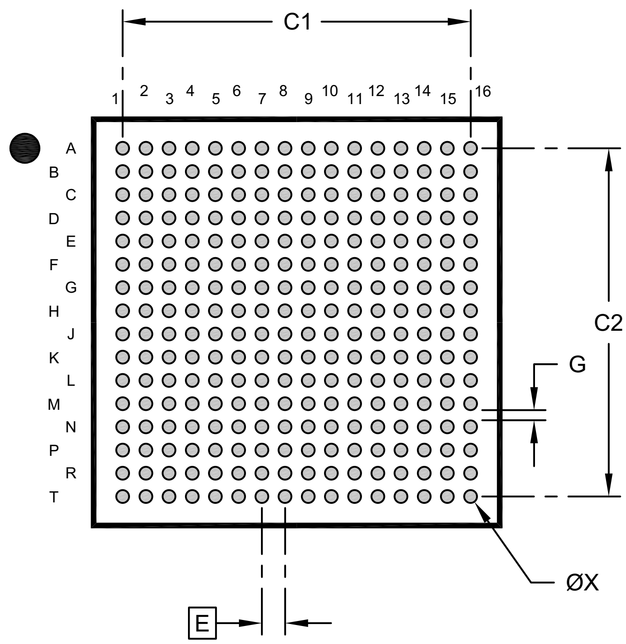
FIGURE 5-3: 256-BGA LAND PATTERN

256-Ball FlipChip Chip Scale Package (3HW) - 14x14x1.78 mm Body [FCCSP] With Heat Spreader

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		12.00	
Contact Pad Spacing	C2		12.00	
Contact Pad Diameter (X256)	X			0.45
Contact Pad to Contact Pad	G	0.35		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, please refer to current industry standard IPC-7093.

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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00006166B (11-03-25)		Removed confidential footer
DS00006166A (09-19-25)		Initial Release

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-	X	/	XXX
Device		Temperature Range		Package

Device:	LAN8267 = Quad 1G/10G PHY w/ 1588
Temperature Range:	V = -40°C (T_A) to +110°C (T_J) (Extended Temperature)
Package:	3HW = 256-ball HFC-BGA

Example:

a) LAN8267-V/3HW
Tray, -40°C (T_A) to +110°C (T_J), 256-ball BGA

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