# 2.7 GHz–3.5 GHz 70W GaN MMIC PA

## ICP0349P

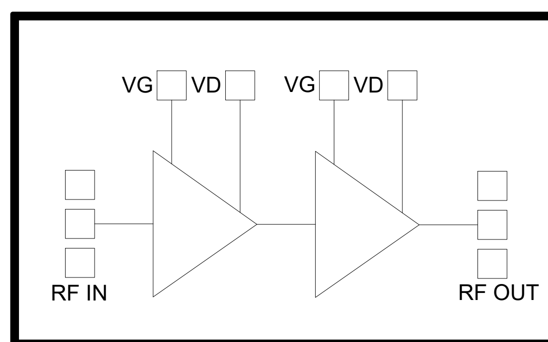
## Product Overview

Microchip's ICP0349P is a 2 stage power amplifier, 50 ohm matched with integrated DC blocking capacitors packaged in a plastic QFN. Fabricated using a GaN on SiC process, ICP0349P operates from 2.7–3.5 GHz with over 48.5 dBm output power and 58% PAE. ICP0349P is well suited to both commercial and defense radar applications.

***Key Features***

- Frequency Range: 2.7–3.5 GHz
- Pout: 48.5 dBm @ 25 dBm Pin
- PAE: 58 %
- Small Signal Gain: 26.5 dB
- Bias: $V_d$=28V $I_{dq}$=200mA
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Package Dimensions: 7.0 x 7.0 x 0.85 mm

***Functional Block Diagram***




## Applications

- Commercial Radar
- Aerospace & Defense

**Table 1.** Electrical Specifications |Test Conditions: $V_d$=28V, $I_{dq}$=200 mA, $T_A$=25 °C, Pulsed = 10% (100 us/1 ms)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Frequency | | 2.7 | | 3.5 | GHz |
| Output Power @ Psat | Pin=25 dBm | 48 | 48.5 | | dBm |
| PAE @ $P_{sat}$ | Pin=25 dBm | | 58 | | % |
| Drain current @ $P_{sat}$ | Pin=25 dBm | | 4 | | A |
| Small Signal Gain | | | 26.5 | | dB |
| Input Return Loss | | | 12 | | dB |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# Table of Contents

Product Overview....................1

1. Electrical Specification....................3
   1.1. Absolute Maximum Ratings....................3
   1.2. Small Signal Performance....................4
   1.3. Pulsed Large Signal Performance....................5

2. Mechanical Drawing....................11

3. Application Circuit....................14

4. Evaluation Board....................15

5. Other considerations....................16

6. Ordering, Shipping, and Handling....................17

7. Revision History....................18

Microchip Information....................19
   Trademarks....................19
   Legal Notice....................19
   Microchip Devices Code Protection Feature....................19


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# 1. Electrical Specification

## 1.1. Absolute Maximum Ratings

**Table 1-1.** Absolute Maximum Ratings

| Parameter | Absolute Maximum |
|---|---|
| Drain Voltage ($V_d$) | 32V |
| Gate Voltage Range ($V_g$) | -8 to 1.5V |
| Gate Current ($I_g$) $T_A$=25ºC | 14 mA |
| Drain Current (continuous) $T_A$=25ºC | 4.3 A |
| Power Dissipation (continuous) $T_A$=25ºC<br>Power Dissipation (continuous) $T_A$=85ºC | 104W<br>73W |
| Continuous Input Power 50 Ohm, $T_A$=25°C | 27 dBm |
| Channel Temperature | 225°C |
| Storage Temperature | -65°C to +150°C |
| Input Power VSWR (2:1), $V_d$=28V, $I_{dq}$=200mA | 20 dBm |
| Reflow Profile | 260°C |

**Notes:**

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

**Table 1-2.** Thermal and Reliability

| Parameter | Value |
|---|---|
| Thermal Resistance | 1.81 °C/W |

**Note:** Thermal resistance calculated using IR measurement of the channel temperature.


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## 1.2. Small Signal Performance

### 1.2.1. Typical CW Power Data over Temperature

Test Conditions: $V_d$= 28V and $I_{DQ}$= 200 mA

**Figure 1-1.** S11 vs Frequency

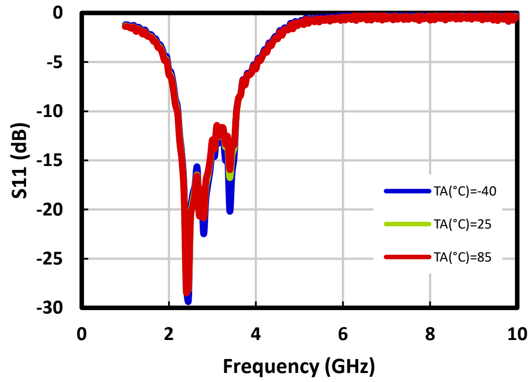



**Figure 1-2.** S21 vs Frequency

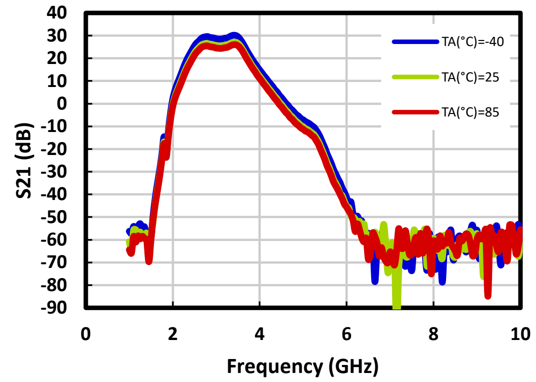



**Figure 1-3.** S12 vs Frequency

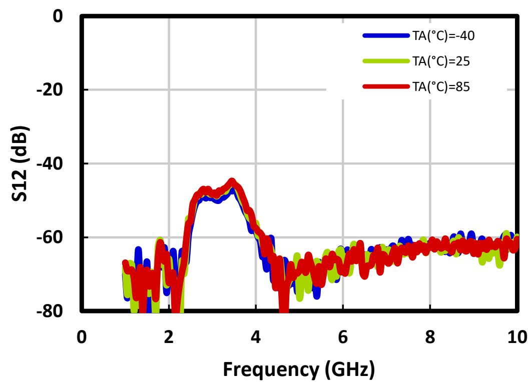
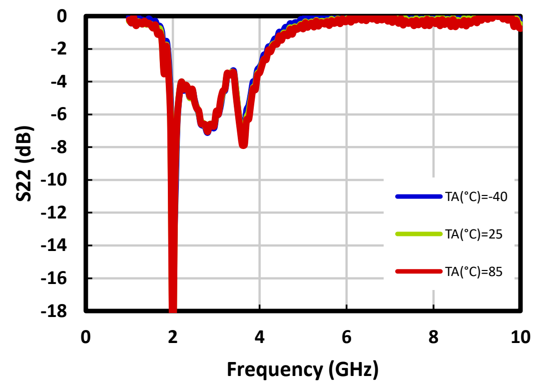



**Figure 1-4.** S22 vs Frequency





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## 1.3. Pulsed Large Signal Performance

### Typical Pulsed Power Data at Ambient

Test Conditions:$V_d$=28V, $I_{dq}$=200mA, $T_A$=25°C, Pulsed= 10% (100 us/1ms)

**Figure 1-5.** Pout vs Pin

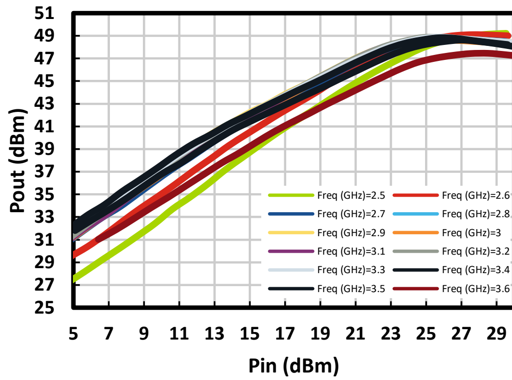



**Figure 1-6.** Gain vs Pin

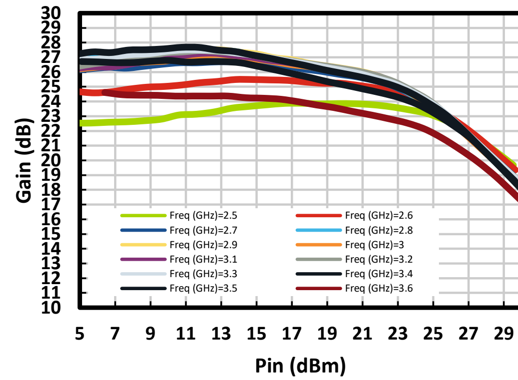



**Figure 1-7.** PAE vs Pin

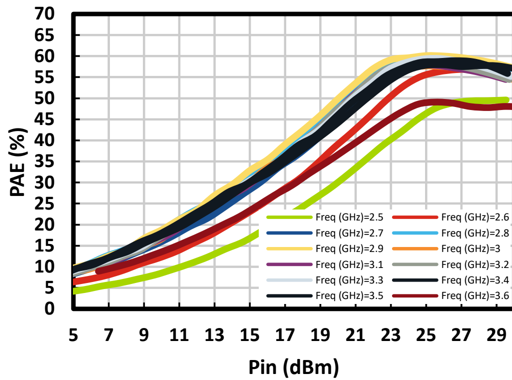



**Figure 1-8.** Id vs Pin

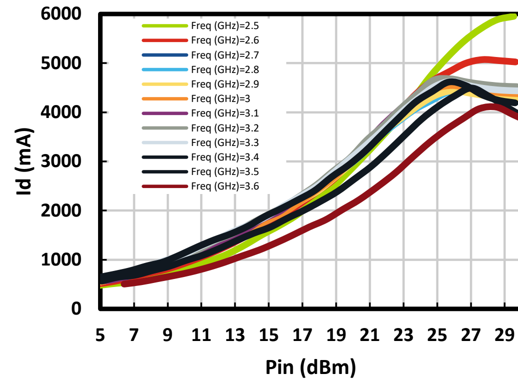



**Figure 1-9.** Pout vs Freq

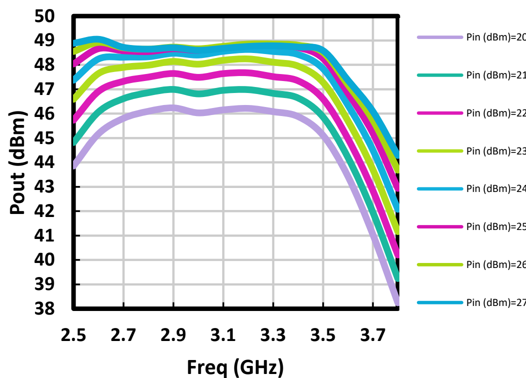
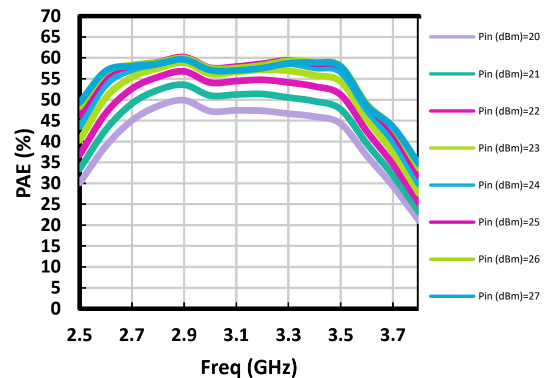



**Figure 1-10.** PAE vs Freq





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## Typical Pulsed Power Data over temperature

Test Conditions:$V_d$=28V, $I_{dq}$=200mA, $T_A$=25°C, Pulsed= 10% (100 us/1ms)

**Figure 1-11.** Pout vs Pin at 2.7GHz

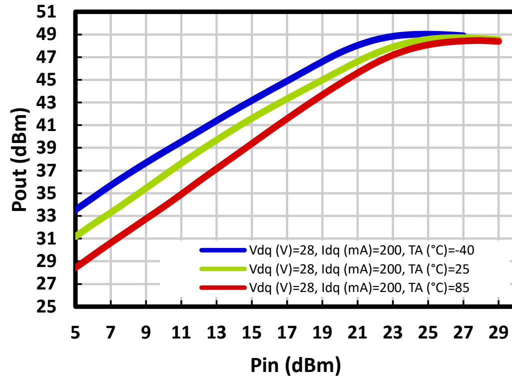


**Figure 1-12.** PAE vs Pin at 2.7GHz

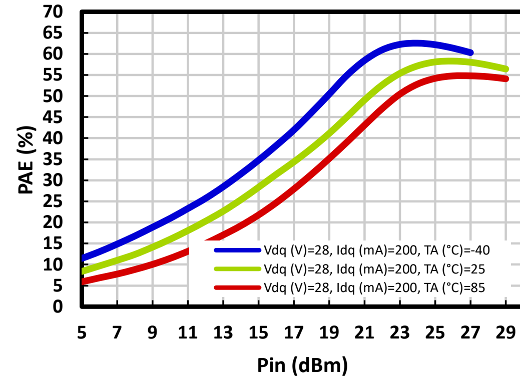


**Figure 1-13.** Gain vs Pout at 2.7GHz

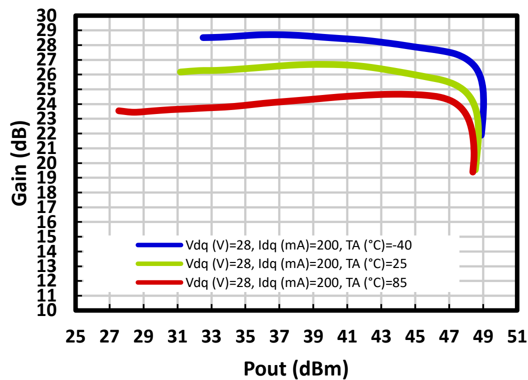


**Figure 1-14.** PAE vs Pout at 2.7GHz

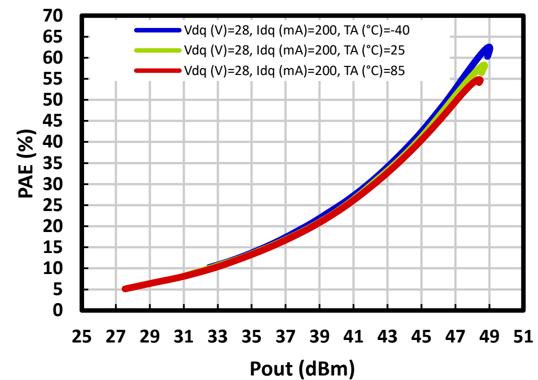


**Figure 1-15.** Id vs Pout at 2.7GHz

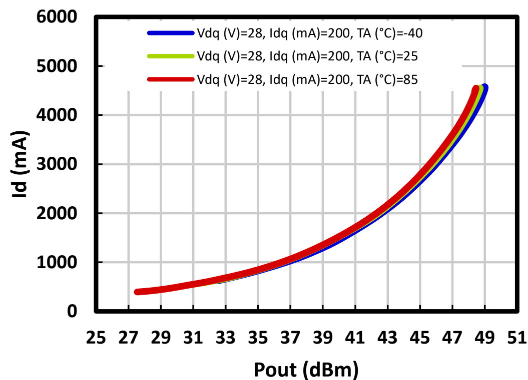


**Figure 1-16.** Ig vs Pout at 2.7GHz

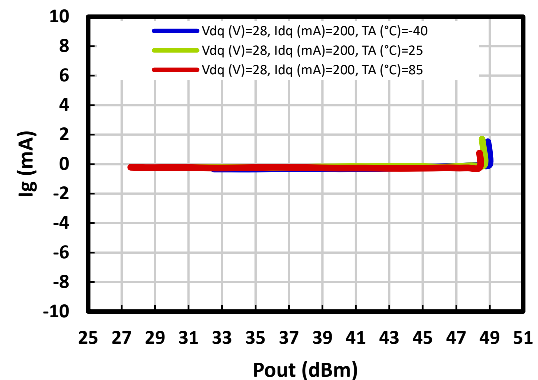



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**Figure 1-17.** Pout vs Pin at 3.1GHz

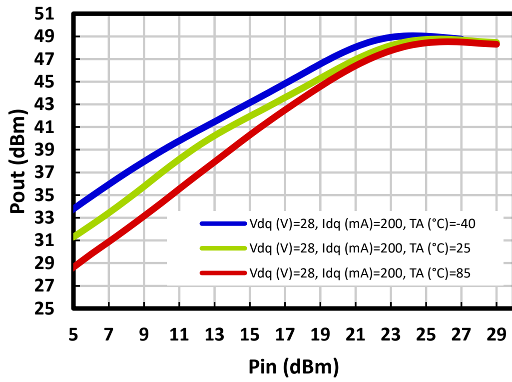


**Figure 1-18.** PAE vs Pin at 3.1GHz

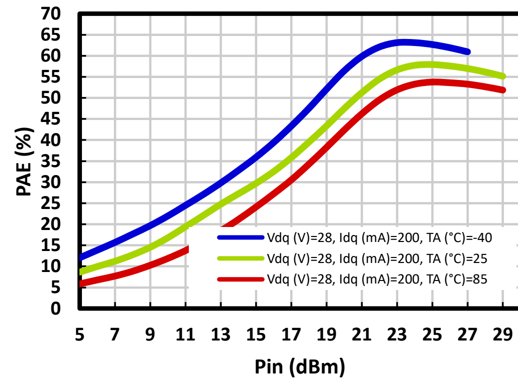


**Figure 1-19.** Gain vs Pout at 3.1GHz

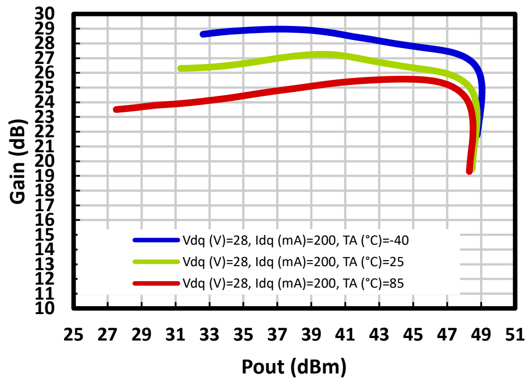


**Figure 1-20.** PAE vs Pout at 3.1GHz

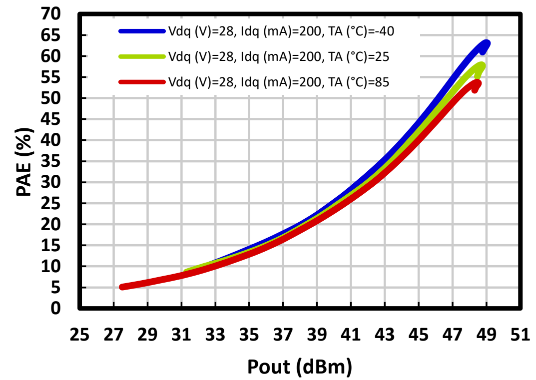


**Figure 1-21.** Id vs Pout at 3.1GHz

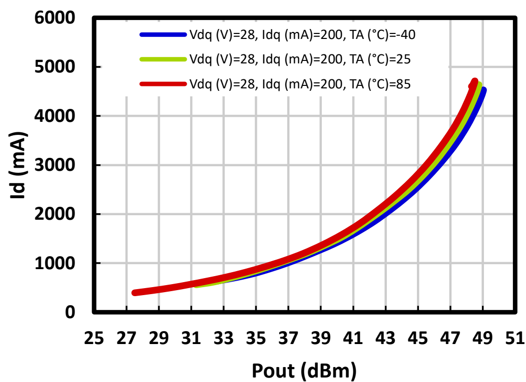


**Figure 1-22.** Ig vs Pout at 3.1GHz

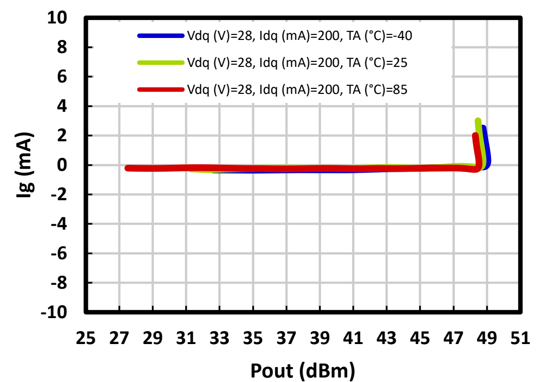



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**Figure 1-23.** Pout vs Pin at 3.5GHz

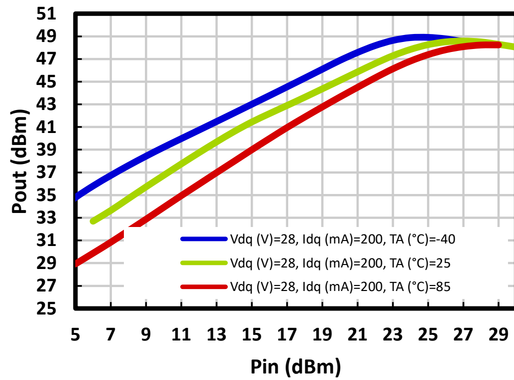



**Figure 1-24.** PAE vs Pin at 3.5GHz

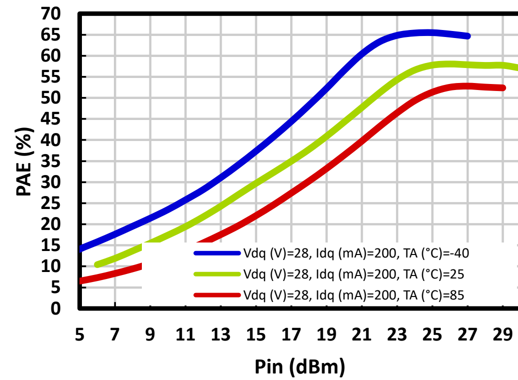



**Figure 1-25.** Gain vs Pout at 3.5GHz

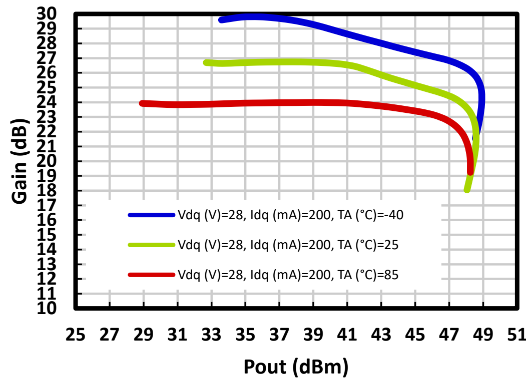



**Figure 1-26.** PAE vs Pout at 3.5GHz

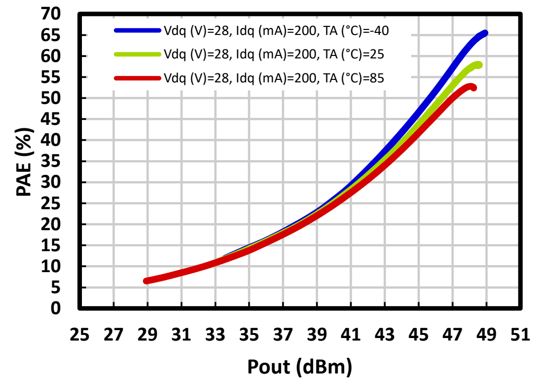



**Figure 1-27.** Id vs Pout at 3.5GHz

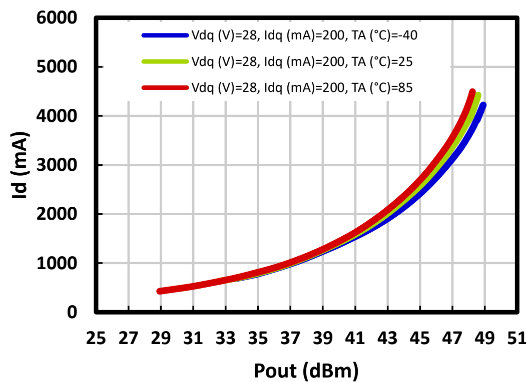
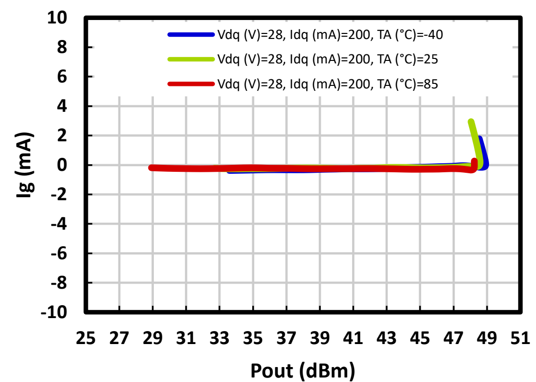



**Figure 1-28.** Ig vs Pout at 3.5GHz





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## Typical Pulsed Power Data over $V_d$

Test Conditions:$I_{dq}$=200mA, $T_A$ =25°C, Pulsed= 10% (100 us/1ms)

**Figure 1-29.** Gain vs Pout at 2.7GHz

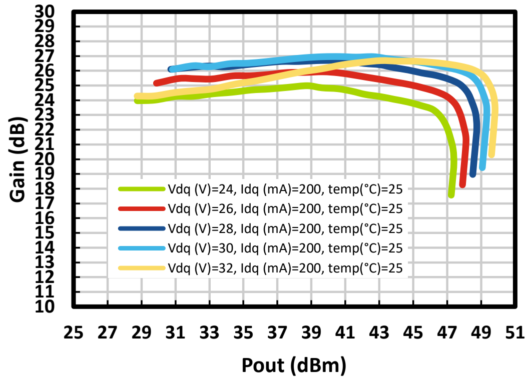



**Figure 1-30.** PAE vs Pout at 2.7GHz

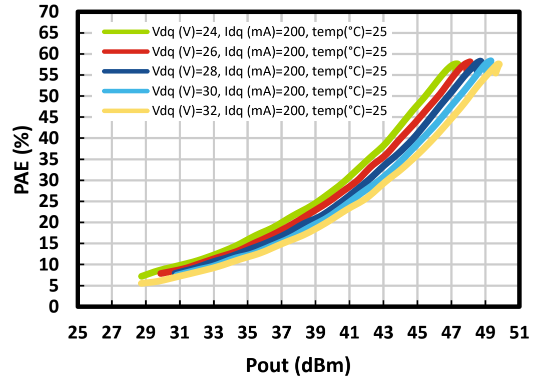



**Figure 1-31.** Gain vs Pout at 3.1GHz

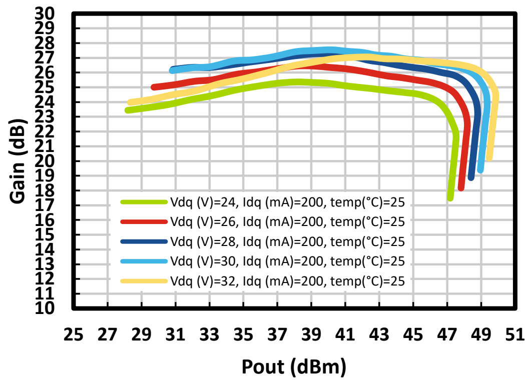



**Figure 1-32.** PAE vs Pout at 3.1GHz

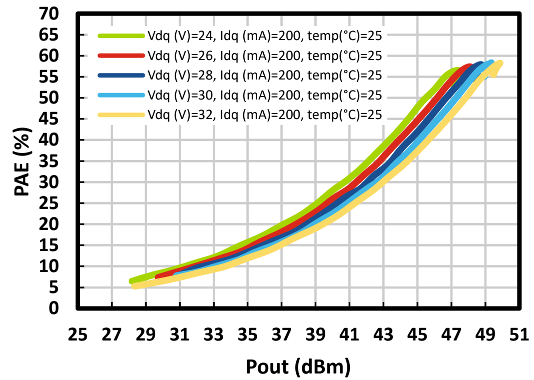



**Figure 1-33.** Gain vs Pout at 3.5GHz

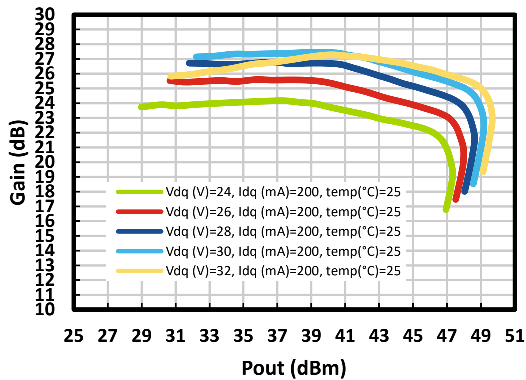
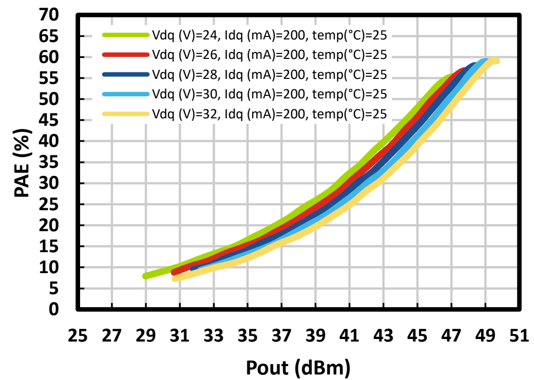



**Figure 1-34.** PAE vs Pout at 3.5GHz





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### Typical Pulsed Power Data over $I_{dq}$

Test Conditions:$V_d$=28V, $T_A$ =25°C, Pulsed= 10% (100 us/1ms)

**Figure 1-35.** Gain vs Pout at 2.7GHz

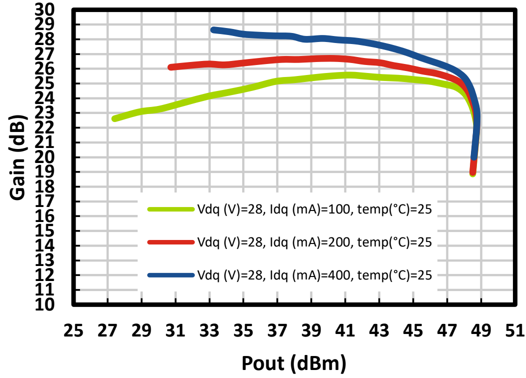



**Figure 1-36.** PAE vs Pout at 2.7GHz

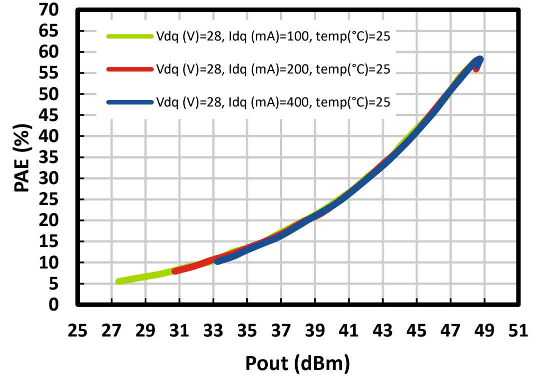



**Figure 1-37.** Gain vs Pout at 3.1GHz

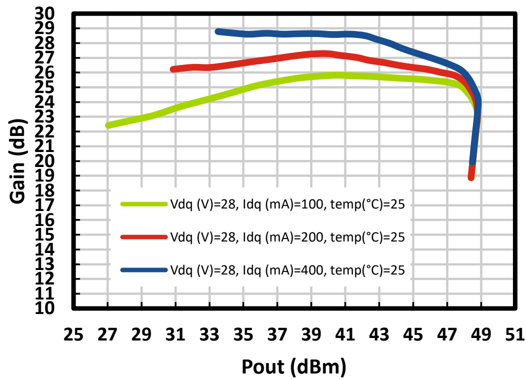



**Figure 1-38.** PAE vs Pout at 3.1GHz

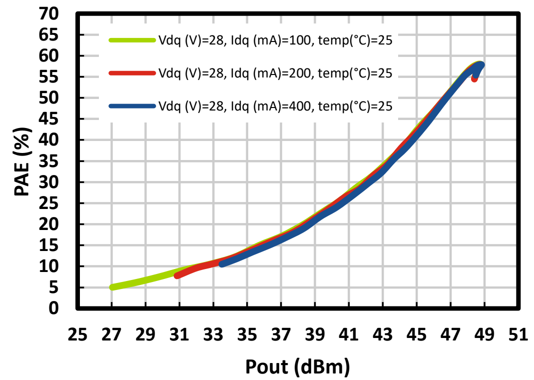



**Figure 1-39.** Gain vs Pout at 3.5GHz

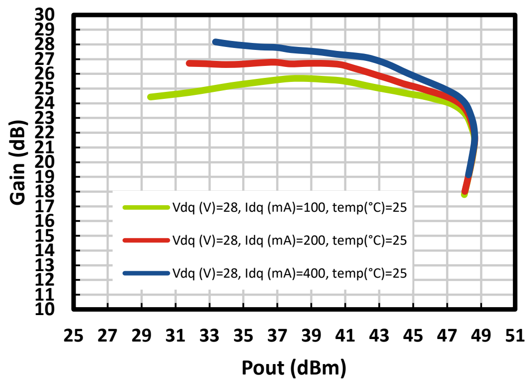
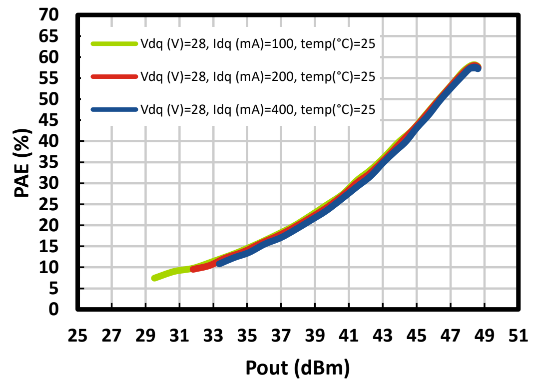



**Figure 1-40.** PAE vs Pout at 3.5GHz





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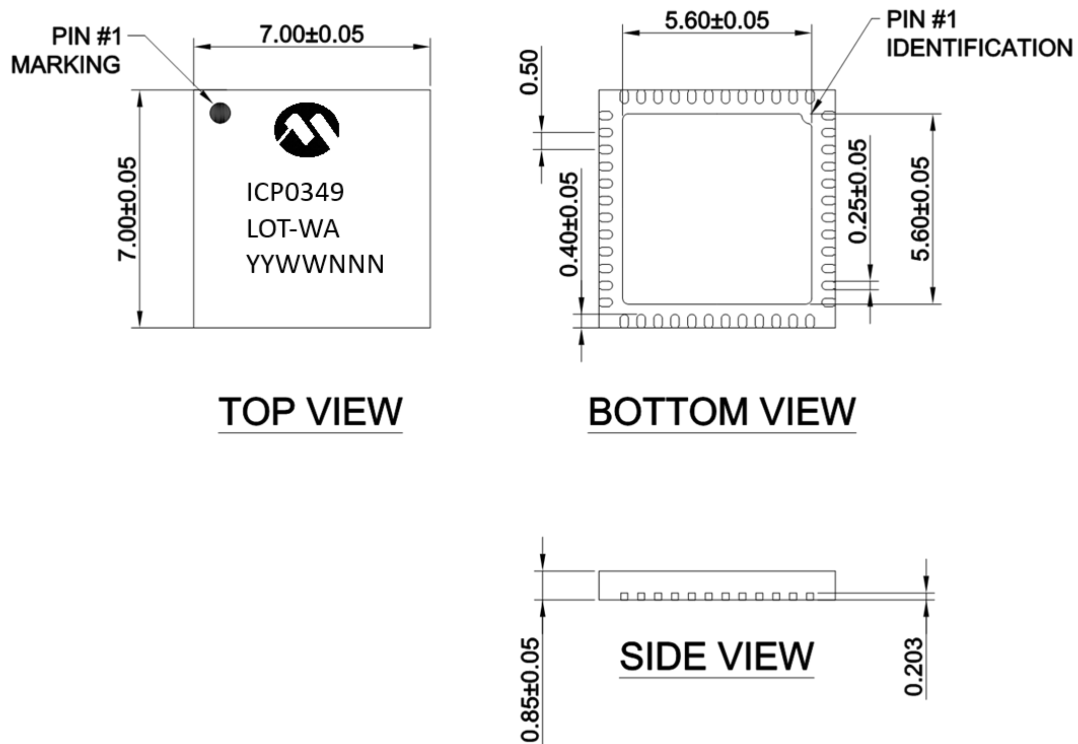
# 2. Mechanical Drawing

**Figure 2-1.** Outline Drawing




**Note:** Unit; mm, Backside of package is RF and DC Ground.

| Package marking | |
|---|---|
| LOT-WA | lot and wafer number |
| YY | Manufacturing year |
| WW | Manufacturing week |
| NNN | Internal code |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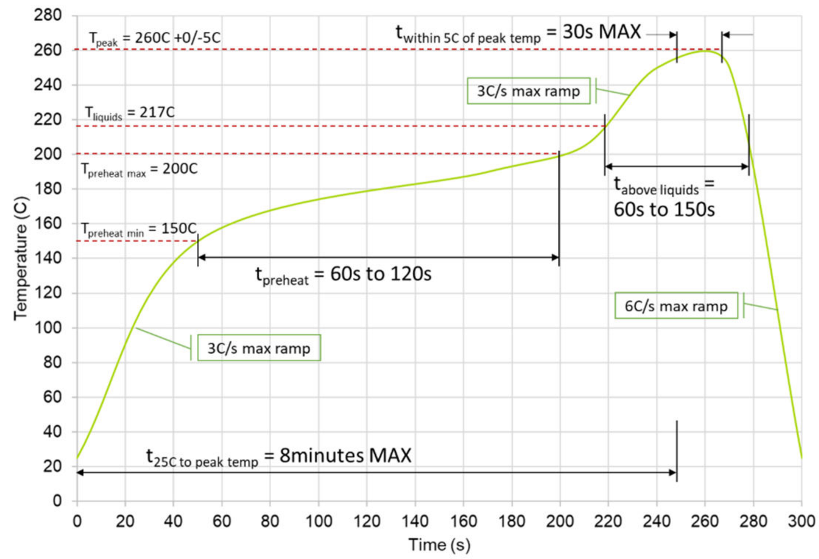
Recommended Soldering Temperature Profile
$T_{peak}$ = 260C +0/-5C
$t_{within\ 5C\ of\ peak\ temp}$ = 30s MAX
3C/s max ramp
$T_{liquids}$ = 217C
$T_{preheat\ max}$ = 200C
$t_{above\ liquids}$ =
60s to 150s
$T_{preheat\ min}$ = 150C
$t_{preheat}$ = 60s to 120s
6C/s max ramp
3C/s max ramp
$t_{25C\ to\ peak\ temp}$ = 8minutes MAX
Temperature (C)
Time (s)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

**Figure 2-2.** Pinout

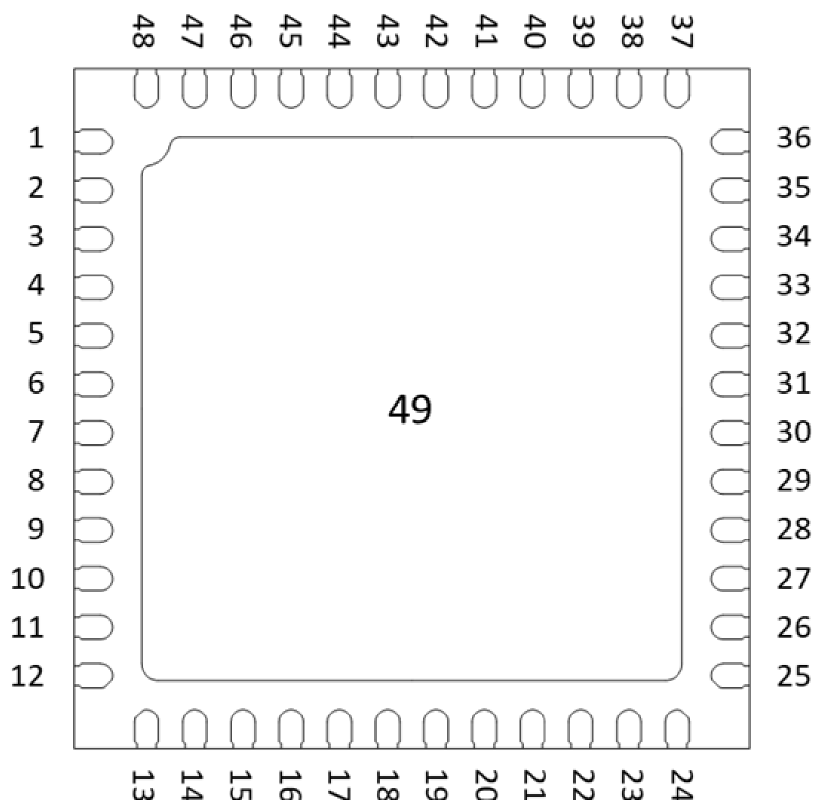


**Table 2-1.**

| Pad No | Function | Description |
| --- | --- | --- |
| 1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47 | NC | Not connected. Can be grounded |
| 49 | GND | Ground Connection |
| 6, 7 | RFIN | RF input, 50 ohm, DC blocked |
| 13, 48 | $V_{G1}$ | 1st stage gate bias, decoupling and bypass caps required, must be biased from both pins (VG1 and VG2 can be tied together in application) |
| 15, 46 | $V_{D1}$ | 1st stage drain voltage, decoupling and bypass caps required, must be biased from both pins (VD1 and VD2 can be tied together in application) |
| 17, 44 | $V_{G2}$ | 2nd stage gate bias, decoupling and bypass caps required, must be biased from both pins (VG1 and VG2 can be tied together in application) |
| 23, 38 | $V_{D2}$ | 2nd stage drain voltage, decoupling and bypass caps required,must be biased from both pins (VD1 and VD2 can be tied together in application) |
| 30, 31 | RFOUT | RF output, 50 ohm, DC blocked, pin is DC grounded |


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# 3. Application Circuit

**Figure 3-1.** Application

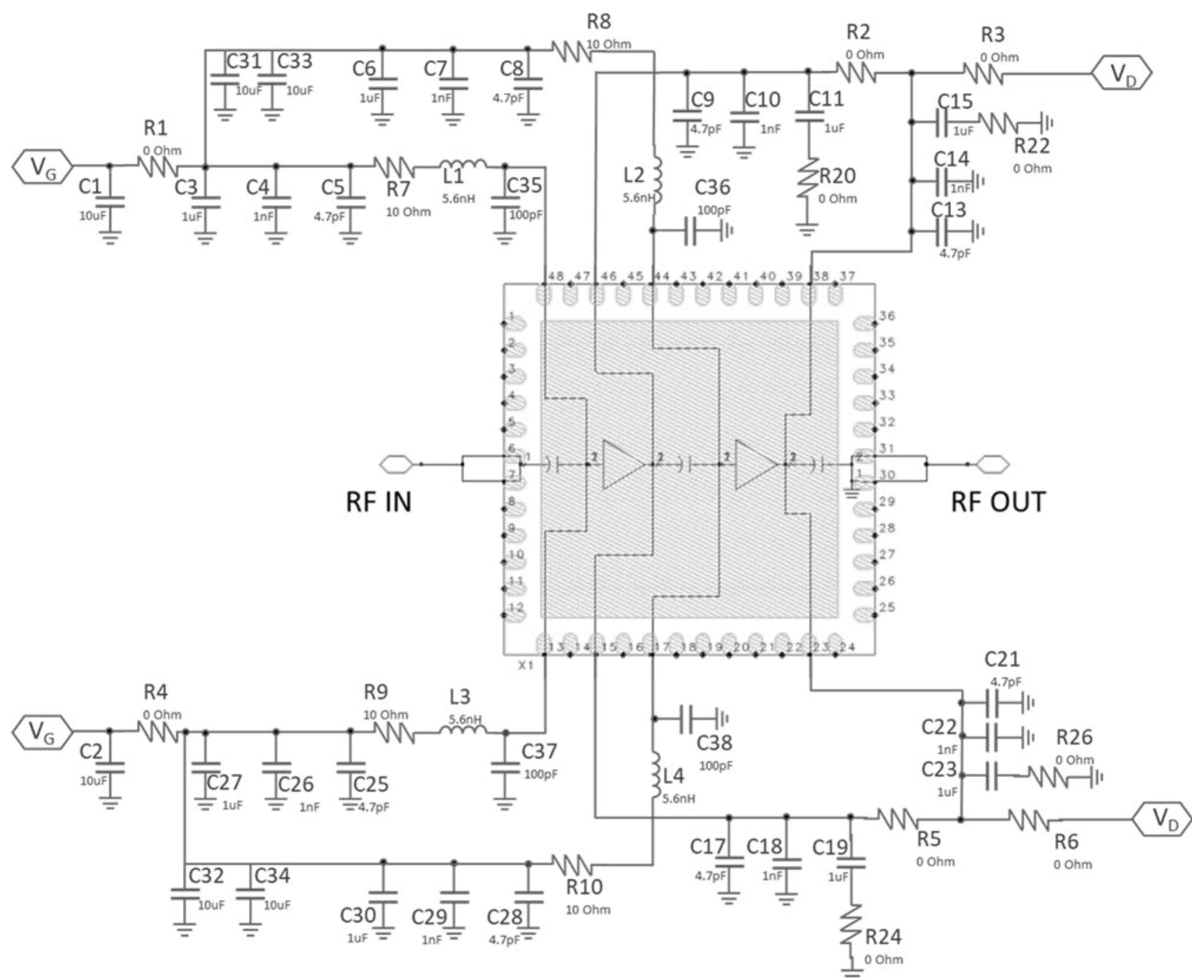


**Table 3-1.** Bill of Materials

| Component ID | Value | Details | Qty | Manufacturer Part no |
|---|---|---|---|---|
| C1, C2 | 10uF | 10uF Capacitor 1206 | 2 | Various |
| C31 - C34 | 10uF | 10uF Capacitor 0603 | 4 | Various |
| C3, C6, C11, C15, C19, C23, C27, C30 | 1uF | 1uF Capacitor 0402, X8R, 50V | 10 | Various |
| C4, C7, C10, C14,C18, C22, C26, C29 | 1nF | 1nF Capacitor 0402, C0G, 50V | 8 | Various |
| C35 - C38 | 100pF | 100pF Capacitor 0402, C0G, 50V | 4 | Various |
| C5, C8, C9, C13, C17, C21, C25, C28 | 4.7pF | 4.7pF Capacitor 0402, C0G, 50V | 8 | Various |
| L1 - L4 | 5.6nH | 5.6nH Inductor 0402 | 4 | Various |
| R7 - R10 | 10Ohm | 10ohm Resistor 0402 | 4 | Various |
| R20, R22, R24, R26 | 0Ohm | 0ohm Resistor 0402 (link) | 6 | Various |
| R1, R2, R3, R4, R5, R6 | 0Ohm | 0ohm Resistor 2010 (link) | 6 | Various |


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# 4. Evaluation Board

**Figure 4-1.** Evaluation Board

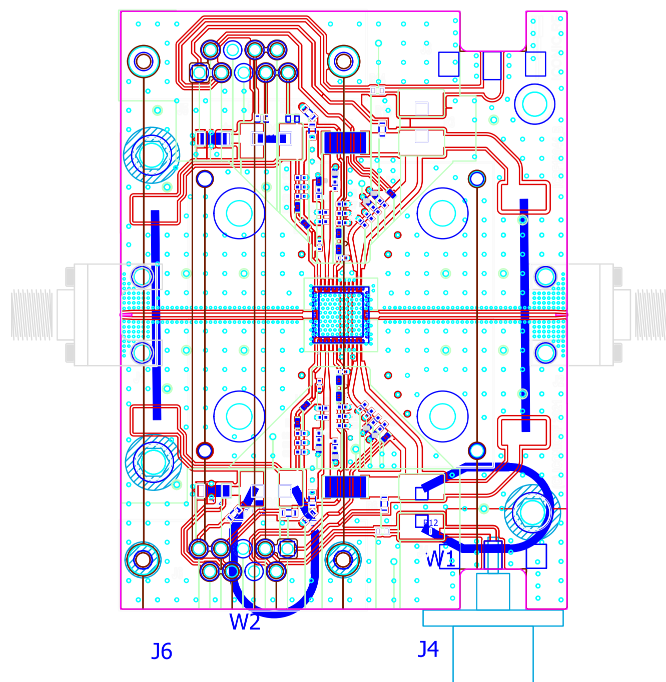


**Table 4-1.** Bill of Materials

| Component ID | Value | Details | Qty | Manufacturer Part No. |
|---|---|---|---|---|
| J1, J2 | n/a | HLT End Launch connector | 2 | CPSM-KF-01A |
| J3. J4 | n/a | Amphenol BNC Panel Jack | 2 | 112639 |
| J5, J6 | n/a | 9way Dsub connector | 2 | Various |
| C1, C2 | 10uF | 10uF Capacitor 1206 | 2 | Various |
| C31 - C34 | 10uF | 10uF Capacitor 0603 | 4 | Various |
| C3, C6, C11, C15, C19, C23, C27, C30 | 1uF | 1uF Capacitor 0402, X8R, 50V | 10 | Various |
| C4, C7, C10, C14,C18, C22, C26, C29 | 1nF | 1nF Capacitor 0402, C0G, 50V | 8 | Various |
| C35 - C38 | 100pF | 100pF Capacitor 0402, C0G, 50V | 4 | Various |
| C5, C8, C9, C13, C17, C21, C25, C28 | 4.7pF | 4.7pF Capacitor 0402, C0G, 50V | 8 | Various |
| L1 - L4 | 5.6 nH | 5.6nH Inductor 0402 | 4 | Various |
| R7 - R10 | 10 Ohm | 10ohm Resistor 0402 | 4 | Various |
| R20, R22, R24, R26 | 0 Ohm | 0ohm Resistor 0402 (link) | 6 | Various |
| R1, R2, R3, R4, R5, R6 | 0 Ohm | 0ohm Resistor 2010 (link) | 6 | Various |


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# 5. Other considerations

### Assembly Guidance

The package must be bolted to a thermally conductive base plate and the pins aligned with the PCB tracks. For optimum thermal transfer use an electrically conductive thermal compound before fixing the package.

### Solderability

Its recommended to manually solder the leads to the PCB using a no-clean solder. This avoids washing the part after soldering.

Components are compatible with lead-free solder with a temperature of 260ºC

For optimum RF and thermal performance Microchip recommends the die assembly base plate is adequately bolted to a forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 17μm thick) for optimal heat transfer.

There are many variables of the second level assembly between the die base plate and heat sink that Microchip are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and heat sink.

The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces are cleaned and free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.

### Bias-up procedure

1. Set $V_G$ to -5V
2. Set $V_D$ to 28V
3. Adjust $V_G$ positive until $I_D$ quiescent is 200mA
4. Limit $I_D$ to 7A
5. Apply RF signal

### Bias-down procedure

1. Turn off RF
2. Turn off $V_D$, allow drain capacitors to discharge
3. Turn off $V_G$


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# 6. Ordering, Shipping, and Handling

## Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

| Moisture Sensitivity Level |
|---|
| Level 3 (IPC/JEDEC J–STD–020) |

## Ordering Information

For additional ordering information, contact your Microchip sales representative.

| Part Number | Description |
|---|---|
| ICP0349-1-670I | 2.7–3.5 GHz 70W Packaged GaN Power Amplifier, 7x7 mm QFN Package in Tape and Reel Format |
| EV24J15A | Dev Tool for ICP0349-1-670I, Fully Assembled Board with RF Test Data. |


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# 7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

| Revision | Date | Section | Description |
| --- | --- | --- | --- |
| 1 | 02/2026 | | Initial Revision |


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