EQCO5X31

Industrial Dual Channel USB 3.2 Gen 1 Reclocker/Redriver

Features

- Extending the reach of USB 3.2 Gen 1 (SuperSpeed) up to 16m
- Cable types supported are STP (Shielded Twisted Pair) and Coax
- Cable lengths supported
  - Up to 5m when USB 2.0 signaling included in cable
  - Up to 16m when USB 3.2 only
- *EyeOpen*™ technology automatically performs cable compensation 0 to 24 dB with 1 dB steps
- *MarginLink*™ integrated signal integrity test capability
- CDR (Clock-Data Recovery) restores signal timing integrity in both directions
- Reference Clock-free operation (no crystal or clock needed)
- Internal terminations for low external component count
- Transparent for all USB 3.2 SuperSpeed signaling including LFPS and electrical-idle
- Dual Channel Single Lane
- 20 pin 4 mm QFN package with wettable flanks
- Low power consumption / single supply @ 1.2V
- Ultra low power sleep mode when link is idle for a sustained period
- Industrial temperature range

Applications

- Extended reach for video conference systems
- Extended reach cable for VR gaming applications
- Extending active USB 3.2 cables
- Extending USB3 Vision™ systems

General Description

The EQCO5X31 is a fully qualified single chip USB 3.2 SuperSpeed Reclocker/Redriver with *EyeOpen*™ and *MarginLink*™ technology for the industrial and commercial market segments. The EQCO5X31 will reclock and drive a USB 3.2 SuperSpeed signal over a cable up to 16m reliably. Furthermore, the EQCO5X31 extends max cable length from a recommended 1m to 5m to meet the maximum length of USB2.0 and up to 16m for USB 3.2 links for longer reach applications. Now designers can easily create applications to support both USB 2.0 and USB 3.2 up to 5 meters and USB 3.2 only up to 16m meters in cable length.

The EQCO5X31 is a single chip (equalizer, driver, reclocker) that repeats high speed data signals with a rate of 5 Gbps. From a cable or PCB trace pair, the signal is received by an auto-adaptive equalizer that compensates for higher-frequency losses in the preceding channel. A reference-less clock-data recovery (CDR) subsequently resets jitter back to meet USB 3.2 specifications for maintaining signal integrity. A cable driver launches this clean signal back onto a cable or PCB trace pair. When placed in series as a repeater, a signal can travel through several EQCO5X31 devices to the destination. The EQCO5X31 CDR restores signal timing integrity at each link along the way.

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Errata

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Conventions

The following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
SIGNAL	Signal Name
msb, lsb	Most significant bit, least significant bit
MSB, LSB	Most significant byte, least significant byte
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Emphasis, Reference, Section or Document name.
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don’t care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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1.0 OVERVIEW

The EQCO5X31 is a USB Reclocker/Redriver intended to increase the cable distances of USB 3.2 SuperSpeed ports in industrial environments. A typical EQCO5X31 Link Set-up is shown in Figure 1-1 along with an internal block diagram showing pin connections in Figure 1-2. See the Section 5.0 of the Data Sheet for additional use-case scenarios.Other use-case scenarios are shown in Section 5.0 “Application Information”.

FIGURE 1-1: TYPICAL EQCO5X31 LINK SET_UP

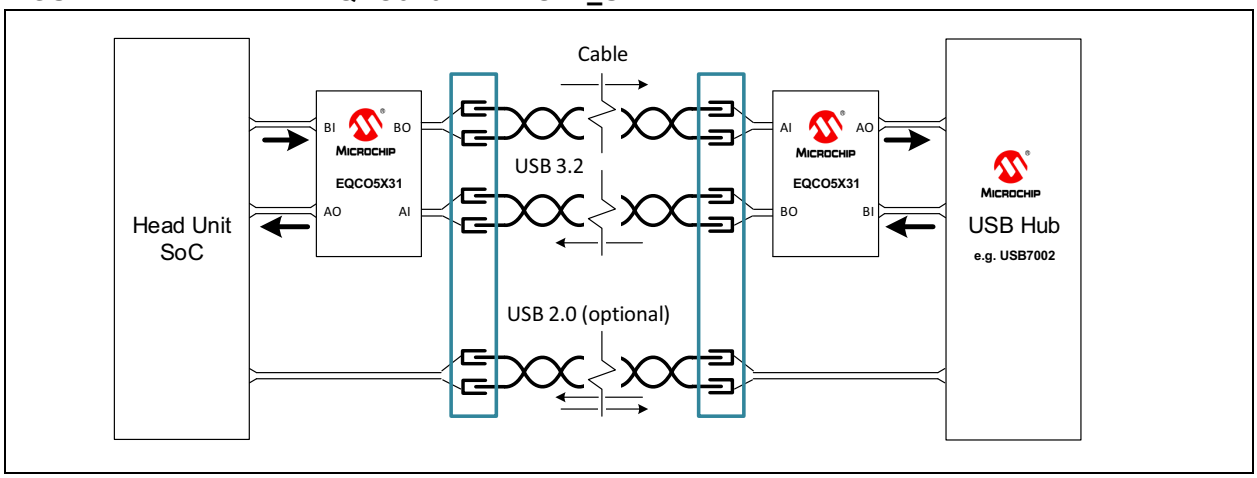
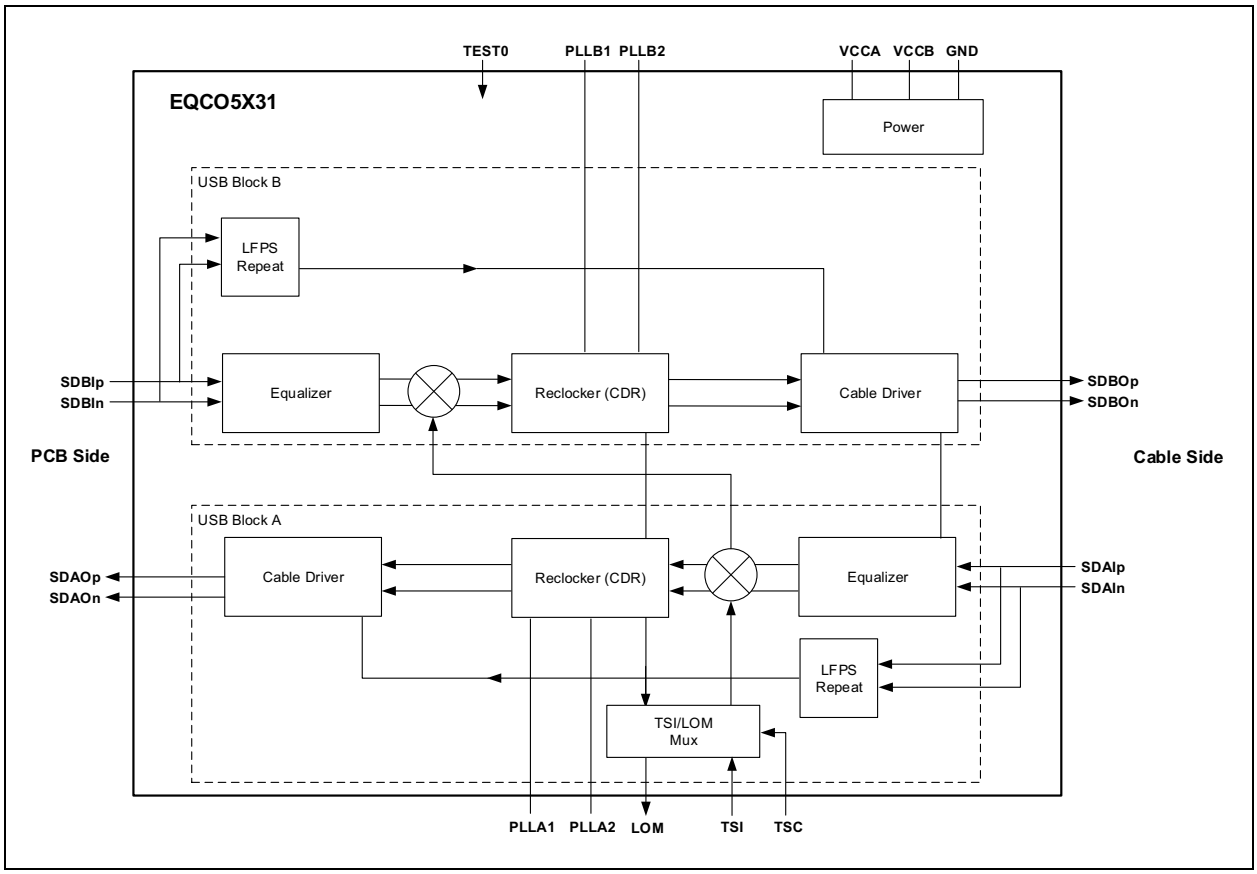


FIGURE 1-2: EQCO5X31 BLOCK DIAGRAM SHOWING PIN CONNECTIONS



Note: The EQCO5X31 has two sides: the Cable side, which is typically routed to a cable connector, and the PCB side which is typically routed on a PCB to an IC. The cores in each direction are identical and each can drive cable or PCB traces.

2.0 EQCO5X31 PINOUT

FIGURE 2-1: EQCO5X31 PIN DIAGRAM (VIEWED FROM TOP)

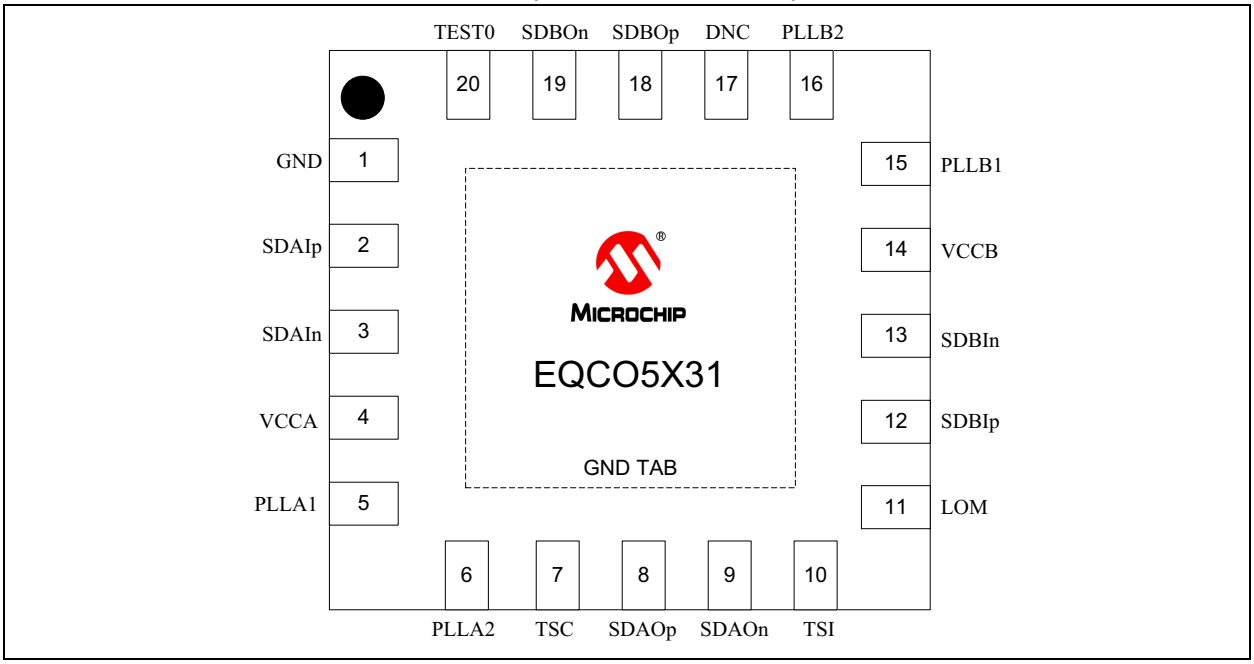


TABLE 2-1: EQCO5X31 PIN DESCRIPTIONS TABLE

Pin Number	Name	Type	Description
(TAB)	**GND**	Power	Connect to Ground. This pad should be connected to ground with in-pad vias.
1	**GND**	Power	Connect to GND TAB directly.
2,3	**SDAIp/SDAIn**	Differential Input	USB Cable side differential serial input pair.
4	**VCCA**	Power	Connect to +1.2V of power supply.
5	**PLLA1**	Power	Connect to +1.2V of power supply through a ferrite bead.
6	**PLLA2**	Power	Connect to PLLA1 through a capacitor.
7	**TSC**	Digital Input	Test Select Channel input. This pin selects the channel (A or B) that the TSI and LOM pins are associated with, High = Chan A, Low = Chan B. See Section 5.4 for further details on how to use this pin.
8,9	**SDAOp/SDAOn**	Differential Output	PCB side differential serial output pair.
10	**TSI**	Analog Input	Test Signal Integrity input for channel A or channel B (selected by TSC pin). This pin has a weak internal pull down (20 kΩ) so it can be left unconnected if not used. See Section 5.4 for further details on how to use this pin.
11	**LOM**	Digital Output	Low Margin. A low to high pulse indicates when a bit error is detected on channel A or channel B (selected by TSC pin). See Section 5.4 for further details on how to use this pin.
12,13	**SDBIp/SDBIn**	Differential Input	PCB side differential serial input pair.
14	**VCCB**	Power	Connect to +1.2V of power supply.
15	**PLLB1**	Power	Connect to +1.2V of power supply through a ferrite bead.
16	**PLLB2**	Power	Connect to PLLB1 through a capacitor.
17	**DNC**	-	Do Not Connect. The pin must be left floating externally.
18,19	**SDBOp/SDBOn**	Differential Output	USB Cable side differential serial output pair.
20	**TEST0**	Input	Must be low. Either tie directly to GND or if compliance mode support is needed, tie to GND with a 0Ω resistor, and add a test point on the pin. See Section 5.5 for more information about compliance mode.

3.0 EQCO5X31 CIRCUIT CONNECTION

3.1 *EyeOpen*™ Equalizer Cores

The EQCO5X31 has an integrated receiver / equalizer in each direction with the following characteristics.

- Auto-adaptive

  The equalizer controls a multiple pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 3-1. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

  The EQCO5X31 equalizer has variable gain to compensate for low frequency attenuation through the cable and variations in transmit amplitude.

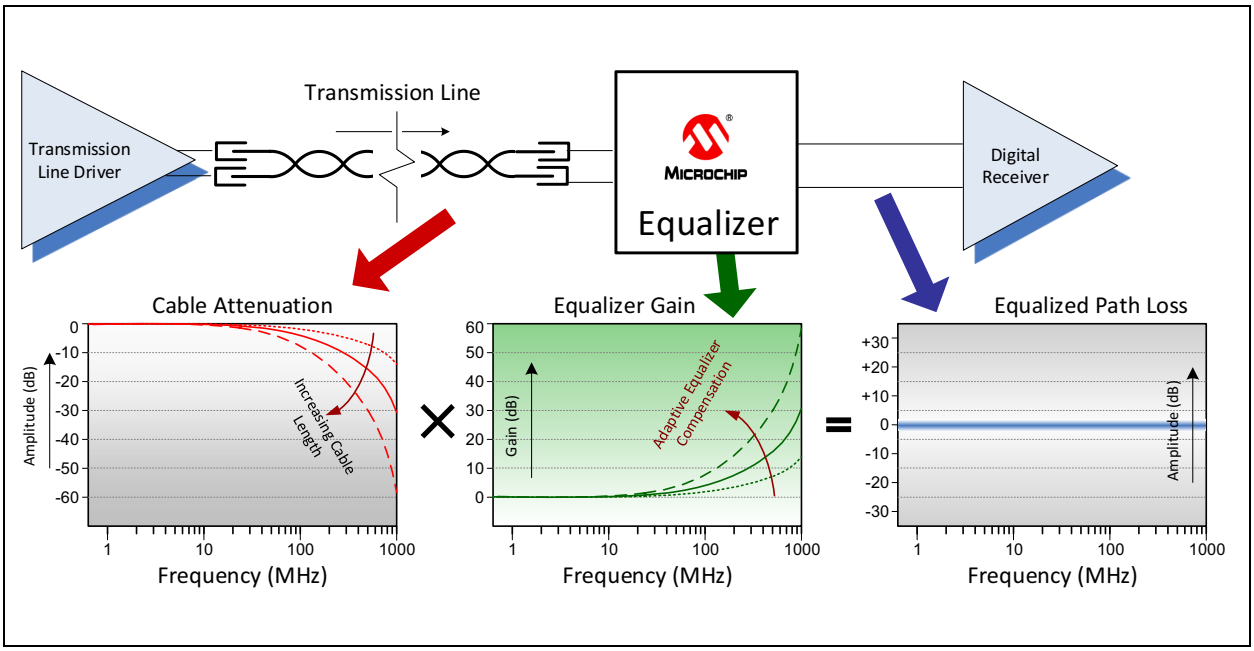
- Single speed

  The EQCO5X31 equalizer cores work at a data rate of 5 Gbps (USB 3.2 SuperSpeed).

- Integrated termination

  The EQCO5X31 receiver includes on-chip termination, no external termination components are required.

FIGURE 3-1: EQUALIZER CORES



3.2 Reclocker Cores

The EQCO5X31 has an integrated reclocker (CDR) in each data direction. The reference-less clock-data recovery subsequently resets the jitter back to a low value for maintaining signal timing integrity, as illustrated in Figure 3-2.

- Reference-clock free operation

  The reclocker cores do not require any external reference clock or crystal.

- Single speed

  The EQCO5X31 reclocker cores work at a data rate of 5 Gbps (USB 3.2 SuperSpeed).

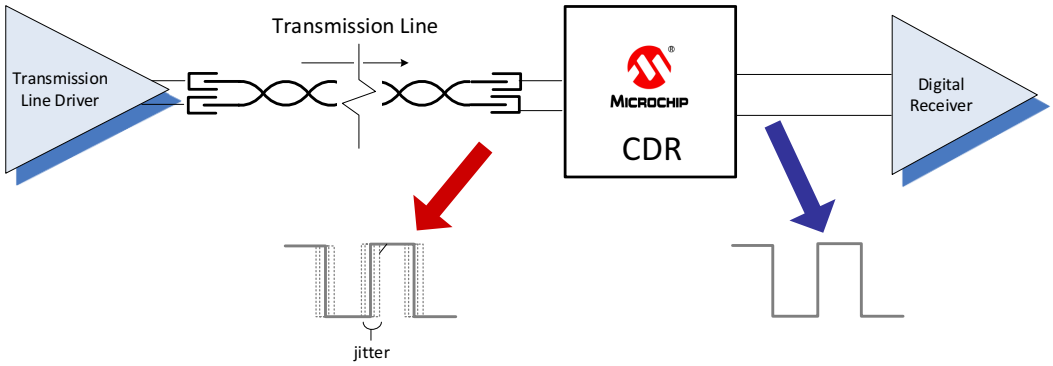
- Analog **VCC** and **GND**

  For best performance the reclocker cores have their own analog power pins along with external filter components. This provides a clean supply rail for the internal PLL. For more details see the Section 5.7 “Power Connectivity”.

- Integrated signal integrity testing

  For purposes of testing and verification, impairment can be added to the signal path just before the reclocker, via the **TSI** pin and results measured via the **LOM** pin. This added impairment has similar effects as adding extra cable length and thus provides a quick way to test a design for adequate margin. See Section 5.4 "*MarginLink™ Signal Integrity Pins (TSI, LOM and TSC)*" for more information on how **TSI** and **LOM** can be used.

FIGURE 3-2: RECLOCKER CORES



Note:	The high speed data sent over the USB 3.2 SuperSpeed ports MUST be 8b/10b encoded.

3.3 Cable Driver Cores

The EQCO5X31 has integrated cable driver cores in each direction with the following characteristics:

- Cable Driver Operation

  The cable driver drives the digital signals onto the **SDxOp/SDxOn** pins and is designed to work with single-ended or differential interfaces. The cable driver takes its output to electrical idle (squelch) when there is no high frequency or LFPS input at the **SDxIp/SDxIn** pins. The cable driver also includes circuits which determine the presence of RX termination on the remote side in accordance with the standard.

- Single speed

  The EQCO5X31 cable driver cores work at a single speed of 5 Gbps (USB 3.2 SuperSpeed).

- Integrated termination

  The EQCO5X31 cable driver includes on-chip termination, no external termination components are required.

3.4 LFPS Repeat Cores

The EQCO5X31 has integrated LFPS (Low Frequency Periodic Signaling) repeat cores in each direction. The LFPS Repeat cores detect LFPS at the input, condition the LFPS timing and send to the output. Spread Spectrum modulation is applied to the LFPS signal output to reduce EMI.

3.5 Sleep Mode

The power block takes the EQCO5X31 to a low power state when both directions are in sustained idle.

4.0 ELECTRICAL SPECIFICATIONS

Specifications are subject to change without notice.

4.1 Absolute Maximum Ratings

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

Parameter [1]	Conditions	Min	Typ	Max	Unit
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Supply Voltage to Ground		-0.5		+1.4	V
DC Input Voltage		-0.5		+1.6	V
DC Voltage to Outputs		-0.5		+1.6	V
Current into Outputs	Outputs Low			90	mA

Note 1: Stresses above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions may affect device reliability.

4.2 Electrical Characteristics

Over the Operating V_{CC} and temperature range. All pertinent USB Gen 1 electrical parameters from the USB 3.2 Specifications [1] have been validated.

TABLE 4-2: ELECTRICAL CHARACTERISTICS

Parameter	Description	Min	Typ	Max	Unit
Temperature (see additional package thermal data in Section 6.2)					
T_a	Ambient Temperature	-40		85	°C
Power Supply					
V_{CC}	Supply Voltage	1.14	1.2	1.26	V
I_s (operational)	Supply current, both directions operating at 5 Gbps		100	145 @ 1.2V 168 @ 1.26V	mA
I_s (sleep)	Supply Current in sleep mode			210 @ 25C 600 @ 85C	µA
LOM ***Output***					
V_{oh}	Output High Voltage	1.0	1.2		V
V_{ol}	Output Low Voltage		GND	0.1	V
t_{LOM}	High Pulse Width	18	36	60	ns
TSC ***Input***					
V_{ih}	Input High Voltage	1.0	1.2		V
V_{il}	Input Low Voltage		GND	0.15	V
TSI ***Input***					
V_i	Input Voltage	GND		V_{CC}	V

5.0 APPLICATION INFORMATION

5.1 Usage Diagrams

The following figures show examples of how the EQCO5X31 can be used in different scenarios. Other applications that need extension of USB 3.2 signaling are also possible. One example of this would be USB3 Vision™.

5.1.1 USB 3.2 WITH USB 2.0 CO-EXISTENCE

For extending USB 3.2 connections that include USB 2.0, cables up to 8 meters can be supported. For cable lengths up to 3 meters, a single EQCO5X31 can be used to provide extra margin and reliability over standard 3-meter links (see Figure 5-1). For cable lengths up to 5 meters, two EQCO5X31 parts are required, one on each end (see Figure 5-2). For cable lengths up to 8 meters, the USB 2.0 signals can also be extended by using a Microchip hub with *PHYboost* technology (see Figure 5-3). Some example use cases are shown below.

FIGURE 5-1: IMPROVED INTEGRITY / RELIABILITY AT USB 3.2 STANDARD LENGTHS

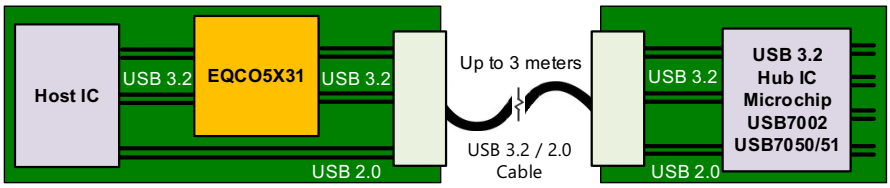


FIGURE 5-2: EXTENDING USB 3.2 TO MATCH USB 2.0 STANDARD LENGTHS

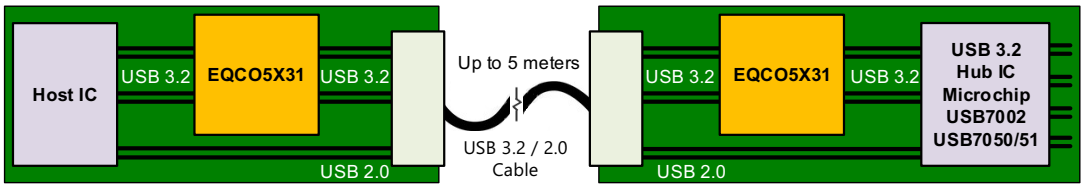
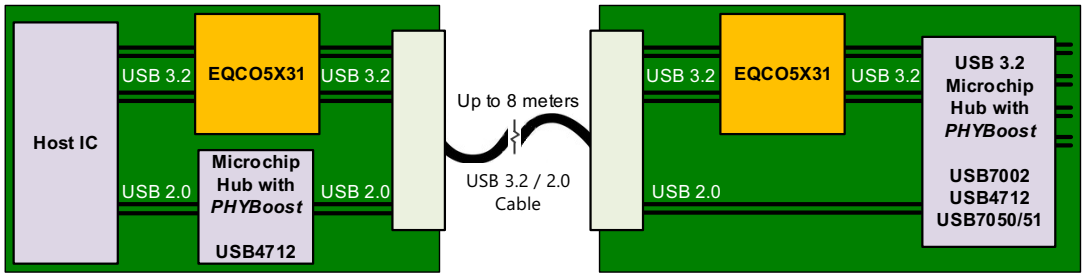


FIGURE 5-3: EXTENDING USB 3.2 AND USB 2.0



5.1.2 LONGER CABLES FOR USB 3.2 ONLY

For extending USB 3.2 connections that do not include USB 2.0, longer cables can be supported. For cable lengths beyond 5 meters, upgraded connectors and cables might be required that have improved crosstalk and loss parameters. Please see Section 5.2 for more information on cable lengths. Some example use-cases are shown below.

FIGURE 5-4: EXTENDING USB 3.2 ONLY CONNECTIONS

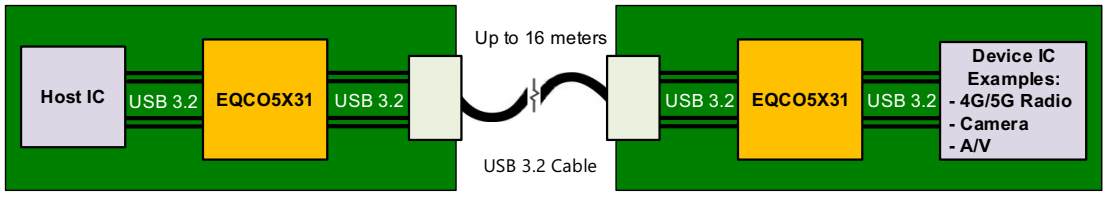


FIGURE 5-5: EXTENDING USB 3.2 ACTIVE CABLE USING ONE CENTER PLACED EQCO5X31

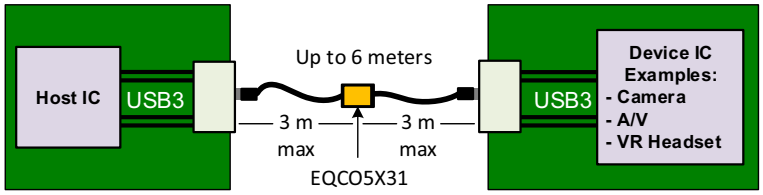


FIGURE 5-6: EXTENDING USB 3.2 ACTIVE CABLE USING TWO END PLACED EQCO5X31

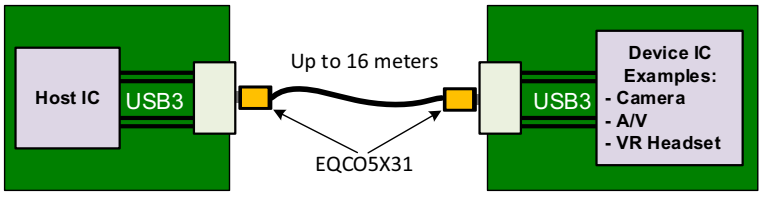


FIGURE 5-7: EXTENDING USB 3.2 ACTIVE CABLE USING TWO NEAR-END PLACED EQCO5X31

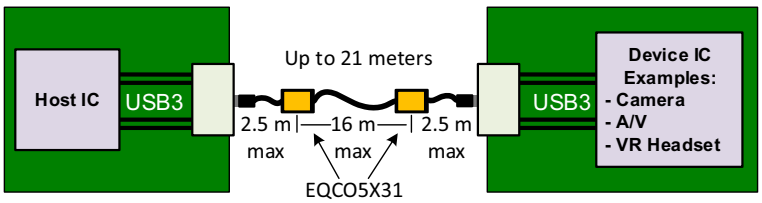
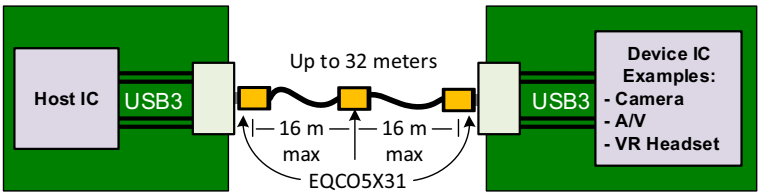


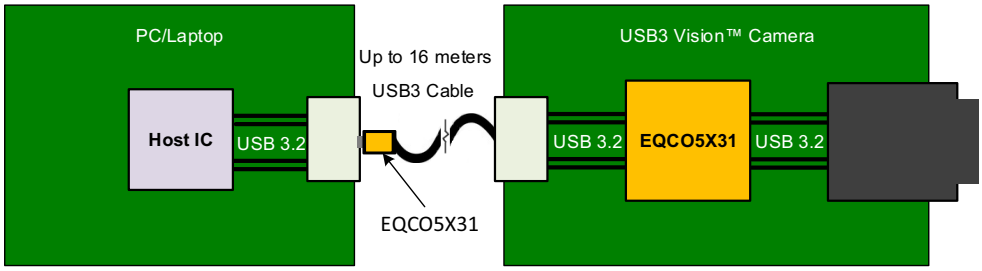
FIGURE 5-8: EXTENDING USB 3.2 ACTIVE CABLE USING THREE EQCO5X31



5.1.3 LONGER CABLES FOR USB3 VISION™

USB3 Vision™ is an interface standard for industrial cameras. It describes a specification on top of the USB standard, with a particular focus on supporting high-performance cameras based on USB 3.0. An example use-case for USB3 Vision™ shown in Figure 5-9, illustrates how the EQCO5X31 can be integrated into the camera to provide a superior differentiated product.

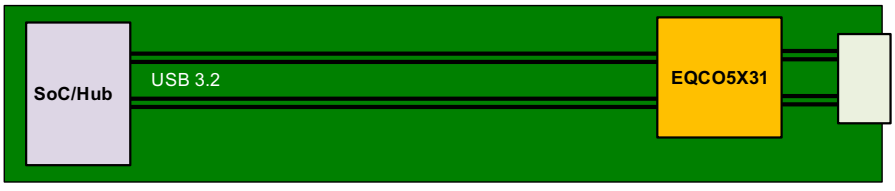
FIGURE 5-9: EXTENDING FOR USB3 VISION™ APPLICATIONS



5.1.4 RESTORING PCB LOSSES

Sometimes the USB controller/SoC cannot be physically near the USB connector on the PCB or is located on a separate board entirely. In these cases the EQCO5X31 can be located near the USB connector, restoring the signal integrity lost through the PCB traces/connector. Please see Section 5.2 for more information on cable lengths. An example use case is shown below.

FIGURE 5-10: EXTENDING EXTRA LONG PCB TRACES AND/OR BOARD-TO-BOARD/ BACKPLANE CONNECTIONS



5.2 Cable Information

5.2.1 CABLE LENGTH

Because the EQCO5X31 is intended to work with lossier channels than defined in the USB 3.2 Specifications [1], it was designed to provide a minimum of 24 dB of compensation at the Nyquist frequency (2.5 GHz) using its *EyeOpen*™ technology. That figure is a conservative minimum taking account factors such as temperature, cable aging and industrial environmental noise. Using that figure then, a maximum cable length can be determined that should work in an industrial environment. To determine the maximum cable length when an EQCO5X31 device is present at both ends of the cable, the following equations should be used:

1. IL (Insertion Loss) <= 24 dB
2. SNR (Signal to Noise Ratio) >= 16 dB, where SNR = NEXT (Near End Crosstalk) – IL

For example, a cable with an IL of 2 dB/m can achieve up to 12 meters length. At that length, the cable + connector with a NEXT of 40 dB or greater would be required to achieve the SNR. In the same way, PCB maximum trace lengths can be calculated by knowing the IL of the trace.

Insertion Loss is largely a matter of the cables AWG rating, long cables would need to have smaller AWG (thicker wire) ratings to achieve lower IL. NEXT is largely a matter of the quality of the cable and connector, the wire arrangement, wire shielding and wire attachment method.

5.2.2 OTHER CABLE TYPES

Although the EQCO5X31 was primarily designed for 90Ω or 100Ω STP (Shielded Twisted Pair), it has also been designed to work with 50Ω coaxial cable, and has been tested to a limited extent.

To obtain further application information pertaining to other cable types and required circuit changes, please contact Microchip support via the Microchip support portal.

5.3 Guidelines for Design and Layout

5.3.1 GENERAL RULES

Below are the general rules that should be used in the schematic and PCB layout. These rules have been implemented in our reference designs. It is best to follow these rules by copying our reference designs as closely as possible. In addition, customer designs should be reviewed by Microchip before building product. This is done through our EQCOcheck process. We highly encourage our customers to send in their designs for review as significant issues are often found during this review. Please contact Microchip support via the Microchip support portal.

1. The 1.2V supply for the EQCO5X31 should be supplied by a low ripple LDO regulator with a high PSRR at the switching frequencies that might be present at its input. Please see our reference design for suggested part selection. For boards with multiple EQCO5X31's, each should have its own regulator.
2. Place and route decoupling capacitors for VCCA and VCCB power pins using low inductance techniques, such as short and wide traces and multiple vias to planes. Microchip recommends placing the decoupling capacitors on the opposite side of the board from the EQCO5X31 so that the ground side of the capacitors can attach directly to a center GND pad via, as is done on our reference designs.
3. Differential PCB traces should be as short as possible and routed as 90Ω or 100Ω (as preferred). The two traces of the pair should be as symmetrical as possible to each other (to reduce mode conversions) and should be routed next to a continuous plane. Copper features such as vias and copper co-planar pours should be kept away from the traces by a distance of 3-4x the trace width. Crosstalk between the RX and TX pairs should be reduced as much as possible, this implies keeping these trace routes as far away from each other as practical. Other crosstalk mitigation techniques such as using different non-adjacent layers and orthogonal routing can also be used.

5.3.2 USB DE-EMPHASIS

The USB 3.2 Specifications [1] allows transmit de-emphasis to be used as a method of equalization to compensate for long cable losses. The EQCO5X31 receive equalizer operates equally well when receiving signals that were launched with or without de-emphasis. The EQCO5X31 does not apply de-emphasis on its transmit outputs. If transmit de-empha-

sis is desired, it is something that can be easily implemented with a few external passive components. Microchip can provide more details on an external circuit to implement transmit de-emphasis. Please contact Microchip support via the Microchip support portal.

5.3.3 ESD GUIDELINES

The EQCO5X31 has extremely strong and robust ESD protection built into the device, so it is generally not required to add external ESD protection in most applications. If the application must be further hardened, external ESD diodes can be added on each differential pair signal located nearest the USB connector. Microchip has the following guidelines with regards to the ESD diode selection:

a. Low capacitance (< 1 pF or preferably < 0.5 pF)
b. TLP voltages in both directions less than 9V at a TLP current of 15A,
c. A dual diode part (or quad) in a single package is better than individual diodes for best matching
d. The diodes should be placed in-line with the differential routes, so stubs are reduced as much as possible.

5.4 *MarginLink*™ Signal Integrity Pins (TSI, LOM and TSC)

USB links typically operate with a very low Bit-Error-Rate (BER). Unfortunately, there is usually no mechanism to determine if there is sufficient operational BER system margin. It is possible that the BER might be low but near a cliff that with just a small additional impairment might result in a much higher BER. This impairment, resulting in increased jitter and eye-opening degradations, can be caused by many factors including but not limited to long cables, damaged cables/connectors and poor PCB layout.

The Test Signal Integrity (**TSI**) pin and Low Margin (**LOM**) pin of the EQCO5X31 are therefore introduced to allow run-time evaluation of the integrity of the whole signal path. When an analog voltage is applied to the **TSI** pin, a controlled level of signal impairment (both timing and amplitude) is intentionally added to the signal just before the reclocker (CDR). Hence, the high frequency jitter margin of the EQCO5X31 will be reduced for a given BER. In case too little margin is present, this will be noticeable by a substantial rise in bit errors. The **LOM** pin output can then be used to detect these bit errors.

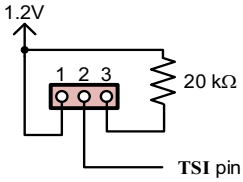
The **TSI** pin is an analog input with an internal pull-down to ground of 20 kΩ. This allows an external resistor to form a voltage divider with the internal resistor and thus generate the desired voltage and impairment level. From 300 mV (±100 mV) onwards, signal impairment is added. At the power supply voltage (1.2V) there is 100% of the maximum allowed impairment, likewise at 50% of the power supply voltage, there is 50% of maximum allowed impairment. For typical applications it is advised to test with 50% level, and for safety critical applications 100% is advised. For example, the jumper configuration as shown in Figure 5-11 could be added to a board design. In this way three different impairment values can be configured manually.

The **LOM** pin is a digital output that indicates when a bit error is detected. Although **LOM** is usually used in conjunction with **TSI**, the function is independent of **TSI**, which means it can be used as a general error indicator. The **LOM** output is normally low but when a bit error is detected, it will output a high (1.2V) pulse. Note that if multiple errors occur during the high pulse width, only one error will be reported.

There are several potential ways to monitor the **LOM** pin output including but not limited to:

1. Counting: A digital counter would count on each rising edge seen. A pass/fail test can be implemented by counting total errors per unit of time. FPGA's and most microcontrollers have counter functions fast enough for this purpose.
2. Integration: A capacitor could be used to integrate the pulses and provide an analog voltage that could be used as input to an ADC or comparator. A pass/fail test can be made by measuring the analog voltage does not exceed a defined threshold.
3. Pulse stretching: This might be done to provide a longer pulse that would drive a visual indicator such as an LED. The LED flashing on would indicate an error occurred, or multiple errors could be roughly measured via the intensity of the LED.

FIGURE 5-11: EQCO5X31 - TSI TEST JUMPER



- No jumper installed = no impairment added
- Jumper 2-3 would provide approximately 50% of maximum allowed impairment
- Jumper 1-2 would provide approximately 100% of maximum allowed impairment

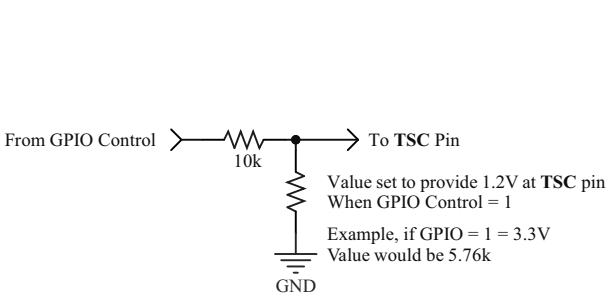
The connection to **TSI** pin should be short and kept away from other signals.

The **TSC** pin is a digital input that selects the channel (A or B, see Figure 1-2) that **TSI** and **LOM** are associated with, High = Chan A, Low = Chan B. For example, if **TSC** is high, channel A will be selected so that **TSI** will impair the channel A receiver, and **LOM** will indicate errors on Channel A receiver. Conversely, if **TSC** is low, **TSI** and **LOM** are associated with Channel B. For most customers, **TSI** and **LOM** should be associated with channel A, because that is the cable side channel input, and it is usually more important to check the margin of the cable side connections.

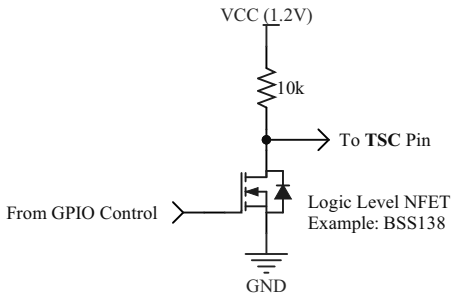
The **TSC** input can be set high or low using the following methods.

1. Resistor Pullup or Pulldown. To tie the **TSC** pin low, a direct tie to ground or a 0Ω resistor to ground is recommended. To tie the **TSC** pin high, a 10 kΩ resistor to VCC is recommended. Do not tie the **TSC** pin directly to VCC or leave floating.
2. Controlled from GPIO. See Figure 5-12 for two options to set or clear the **TSC** pin from a GPIO.

FIGURE 5-12: EQCO5X31 - SET OR CLEAR THE TSC PIN FROM A GPIO



GPIO Control Option 1: Voltage Divider



GPIO Control Option 2: NFET Open Drain Inverter
High at Gate Input = Low at output
Low at Gate Input = High at output

5.5 TEST0 Pin and Compliance Mode

Link partners (Host or Device) are required to support USB 3.2 Compliance Mode [4]. This is a special test mode used to generate test patterns that would enable physical measurements to be made at the transmitter (such as scope measurements, eye diagrams, etc.). As the EQCO5X31 is not a Host or Device, it does not by default support Compliance mode, nor does it normally pass these special test patterns through the device. However, it is possible to enable the EQCO5X31 to pass through and re-drive CP0 and CP1 patterns needed for electrical compliance testing by programming the EQCO5X31 through its **TEST0** pin. This is detailed in AN1686: EQCO5X31 Compliance with USB 3.2 Gen 1 Application Note [5].

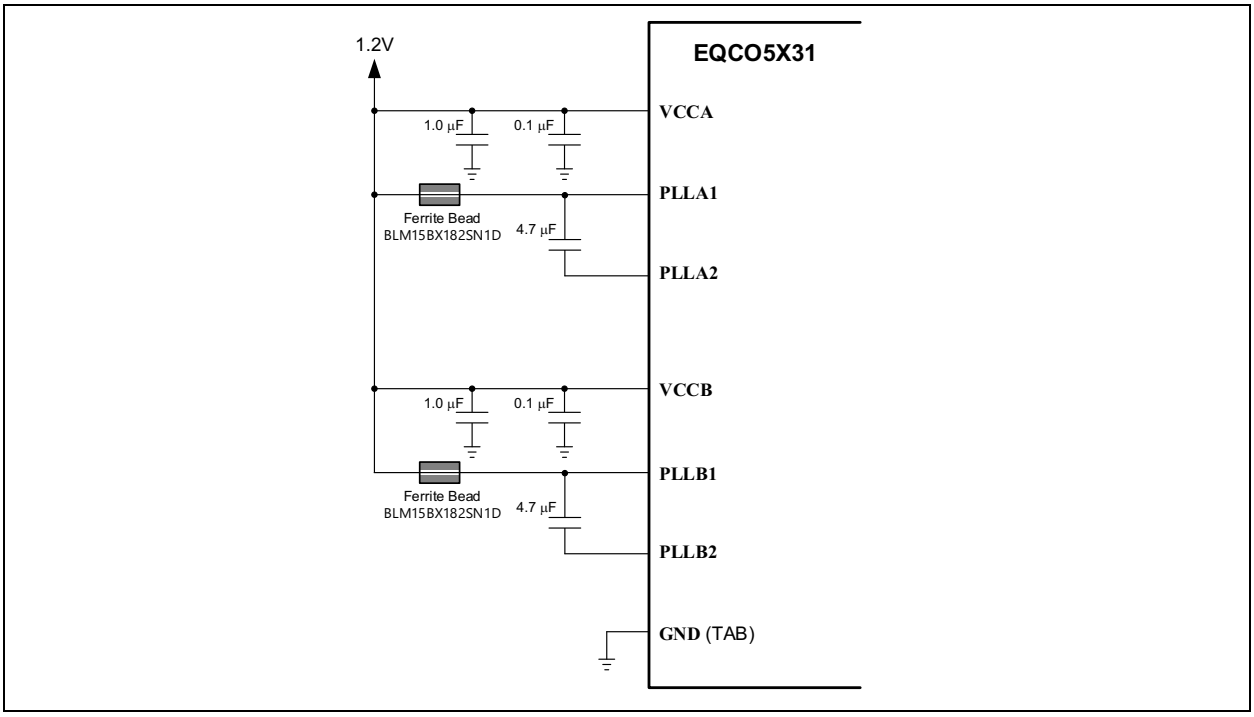
5.6 Data Pins (SDxOp/SDxOn and SDxIp/SDxIn)

The connection to these pins should follow the general rules in Section 5.3.1. The transmit outputs (**SDxOp/SDxOn**) must include DC blocking capacitors with a value between 75-265 nF. Microchip recommends 100 nF / 50V as these can be readily obtained in 0402 (1005 metric) size. The USB specifications do not require capacitors on the receiver inputs (**SDxIp/SDxIn**), but for reasons of industrial safety and protection, it is recommended. If receiver capacitors are used, the value must be between 297-363 nF. Microchip recommends 330 nF / 50V..

5.7 Power Connectivity

Figure 5-13 illustrates the power configuration for the EQCO5X31 with recommended filtering and decoupling. The EQCO5X31 requires only a single 1.2V power supply, which must supply both VCC pins (VCCA and VCCB must be connected together). It is important to power each EQCO5X31 from a low ripple LDO regulator with a high PSRR at the switching frequencies that might be present at its input. Ripple on the power supply adversely affects CDR operation, signal integrity, and cable distance that can be supported.

FIGURE 5-13: POWER CONNECTIVITY



5.8 Microchip EQCO5X31 Reference Designs

Microchip offers the following reference designs and evaluation boards for the EQCO5X31.

1. EQCO5X31 Evaluation Board, AIS20001
2. EV40G35A EVB-EQCO5X31-TYPE-C EXTENDER
3. EV23B43A EVB-EQCO5X31-TYPE-C REPEATER

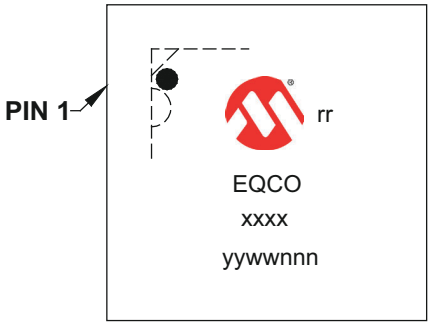
Design files and evaluation boards are available upon request. Please contact Microchip support via the Microchip support portal.

It is highly recommended to start with a Microchip reference design before beginning a new project. Customer designs should be reviewed by Microchip before building product. This is done through our EQCOcheck process. We highly encourage our customers to send in their designs for review. Significant issues are often found during this review. Please contact Microchip support via the Microchip support portal.

6.0 PACKAGING INFORMATION

6.1 Package Marking

FIGURE 6-1: EQCO5X31 TOP MARKING



Device Identifier
rr - Product Revision Code
xxxx - 5X31
yy - last two digits of Assembly Year
ww - Assembly Work Week
nnn - Tracking Number
- Pb-free JEDEC designator for Matte Tin (Sn)
(e3) - This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6.2 Package Thermal Characteristics

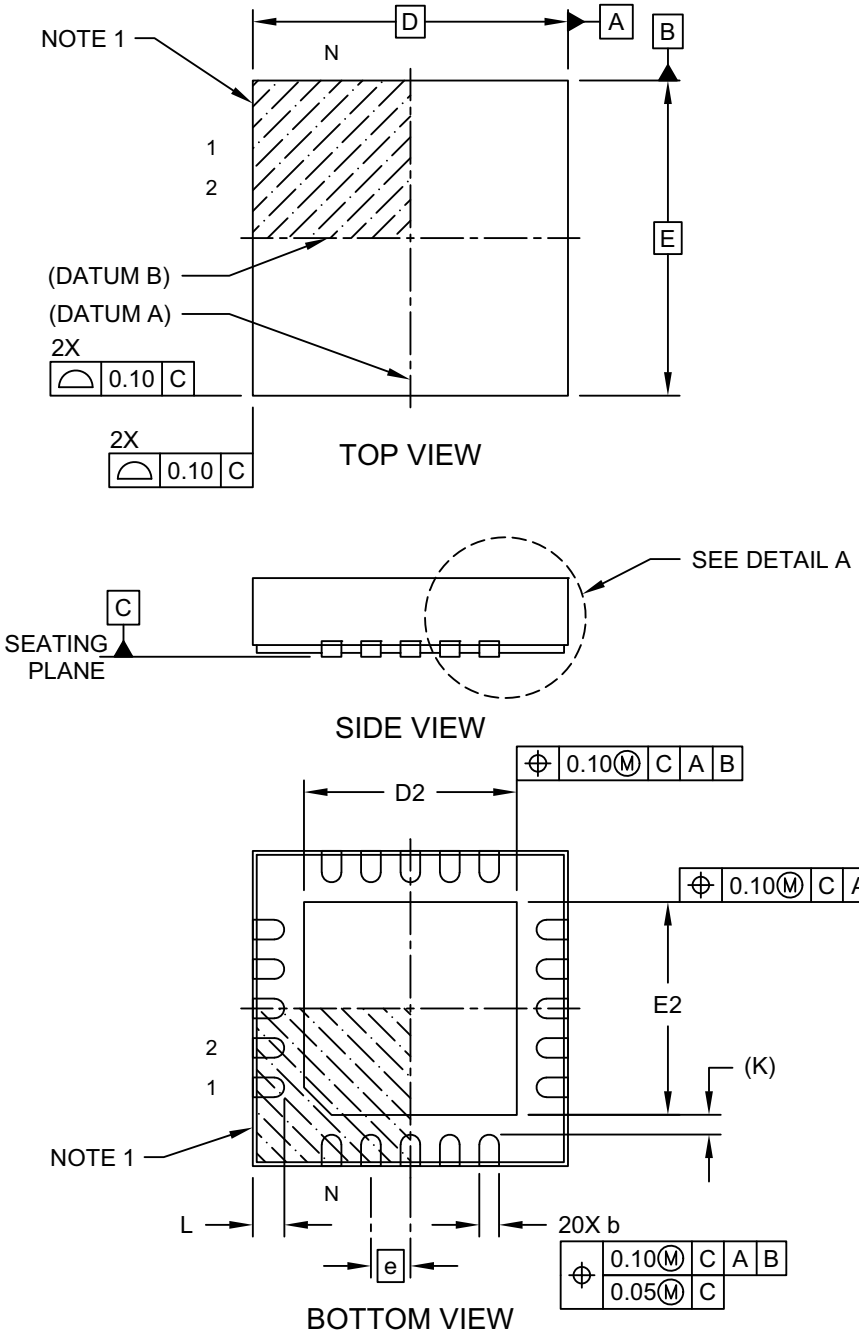
TABLE 6-1: EQCO5X31 20 LEAD PLASTIC QUAD FLAT, NO LEAD PACKAGE (6N)

Parameter	Symbol	Value	Unit
Typical Junction to Ambient	Θ_{JA}	43.9	°C/W
Typical Junction to Case	Θ_{JC}	28.5	°C/W
Typical Junction to Board	Θ_{JB}	20.43	°C/W

6.3 Package Drawings

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

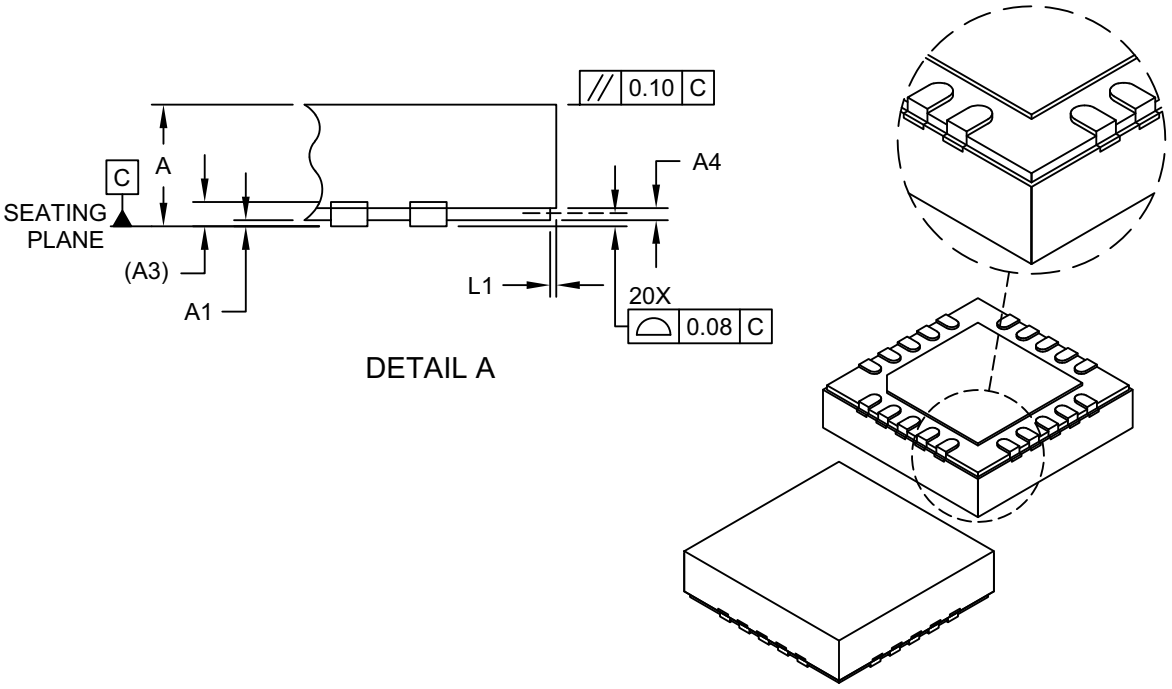
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-402E Sheet 1 of 2

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Step Height	A4	0.10	–	0.19
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Step Length	L1	0.035	0.060	0.085
Terminal-to-Exposed Pad	K		0.25 REF	

Notes:

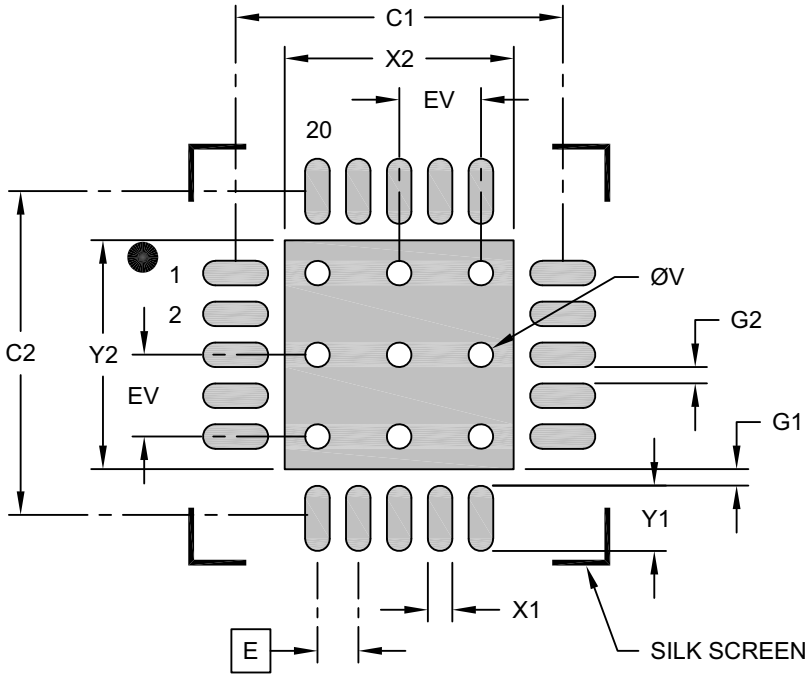
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-402E Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (6N,6NX) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.25		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2402E

APPENDIX A: REFERENCES

Documents listed below and referenced within this publication are current as of the release of this publication and may have been reissued with more current information. To obtain the latest releases of Microchip documentation please visit the Microchip website. Please note, some Microchip documentation may require approval. Contact information can be found at www.microchip.com.

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[1] USB 3.2 Specifications
https://www.usb.org/

[2] Patents: US7894515B2 & EP2182688B1

[3] Patents & Patents Pending: US10277340 (B1)

[4] Universal Serial Bus 3.2 Specification. Revision 1.1 June 2022 - Section 7.5.5

[5] AN1686: EQCO5X31 Compliance with USB 3.2 Gen 1 Application Note

APPENDIX B: REVISION HISTORY

B.1 Current Revision

DS60001668E (July 2024)

- Updated section 2.0 Pinout
- Added section 5.5 **TEST0** Pin and Compliance Mode

B.2 Previous Revision

DS60001668D (August 2023)

- Updated section 6.3 Package Drawings

DS60001668C (March 2023)

- Updated section 2.0 Pinout
- Updated section 4.2 Electrical Characteristics
- Updated section 5.3.3 ESD guidelines
- Updated section 5.7 Microchip EQCO5X31 Reference Designs

DS60001668B (December 2021)

- Updated entire document for new pins **TSC**, **TEST2** and **TEST3**
- Updated Table 4-2 to add digital pins **LOM**, **TSC** and Analog pin **TSI** to electrical table
- Updated section 5.1 Usage Diagrams, added USB2 extension Figure and USB3 Vision™ Figure
- Updated section 5.3.2 regarding de-emphasis
- Added section 5.3.3 ESD Guidelines.

DS60001668A (December 2020)

- Initial document release.

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PART NO.	R	P	G	M
Device	Silicon Revision	Package Option	Grade	MCHP Package #

Device	EQCO5X31	
Silicon Revision	R rr	 = Designates Silicon Revision (example C0)
Packing Option	P T Blank	 = Tape and Reel = Tray
Grade	G I	 = Industrial
MCHP Internal Package Number	M 6NX	 = QFN Package

ORDERING INFORMATION

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b. EQCO5X31rrT-I/6NX

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