

High Performance CMOS MEMS Oscillator

Features

- Wide Frequency Range: 2.5 MHz to 170 MHz (CMOS)
- Very Low RMS Phase Jitter: 650 fs (typ.)
- High Stability: ± 20 ppm, ± 25 ppm, ± 50 ppm
- Wide Temperature Range:
 - Automotive: -40°C to $+125^{\circ}\text{C}$
 - Extended Industrial: -40°C to $+105^{\circ}\text{C}$
 - Industrial: -40°C to $+85^{\circ}\text{C}$
 - Commercial: -20°C to $+70^{\circ}\text{C}$
- Small Industry-Standard Footprints
 - 2.5 mm x 2.0 mm
 - 3.2 mm x 2.5 mm
 - 5.0 mm x 3.2 mm
 - 7.0 mm x 5.0 mm
- Excellent Shock and Vibration Immunity
 - Qualified to MIL-STD-883
- High Reliability
 - 20x Better MTF than Quartz Oscillators
- Supply Range of 2.25V to 3.63V
- Standby, Frequency Select, and Output Enable Functions
- Lead-Free and RoHS-Compliant
- For AEC-Q100 Qualified Parts, Refer to DSA1201 Family

Applications

- Storage Area Networks
- Passive Optical Networks
- 10/100G Ethernet
- HD/SD/SDI Video and Surveillance
- Display Port

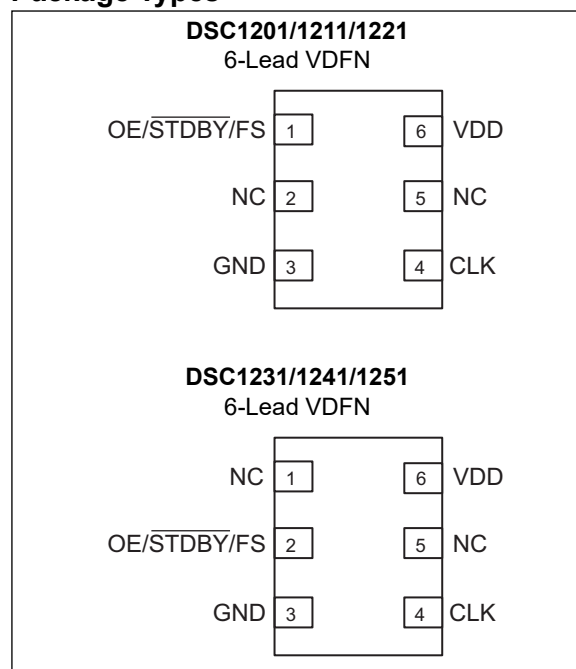
General Description

The DSC12x1 family of high performance oscillators utilizes the latest generation of silicon MEMS technology that improves phase noise and provides excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

The DSC12x1 family features a control function on pin 1 or pin 2 that permits either a standby feature (complete power down when $\overline{\text{STDBY}}$ is low), output enable (output is tri-stated with OE low), or a frequency select (choice of two frequencies selected by FS high/low). See the [Product Identification System](#) section for detailed information.

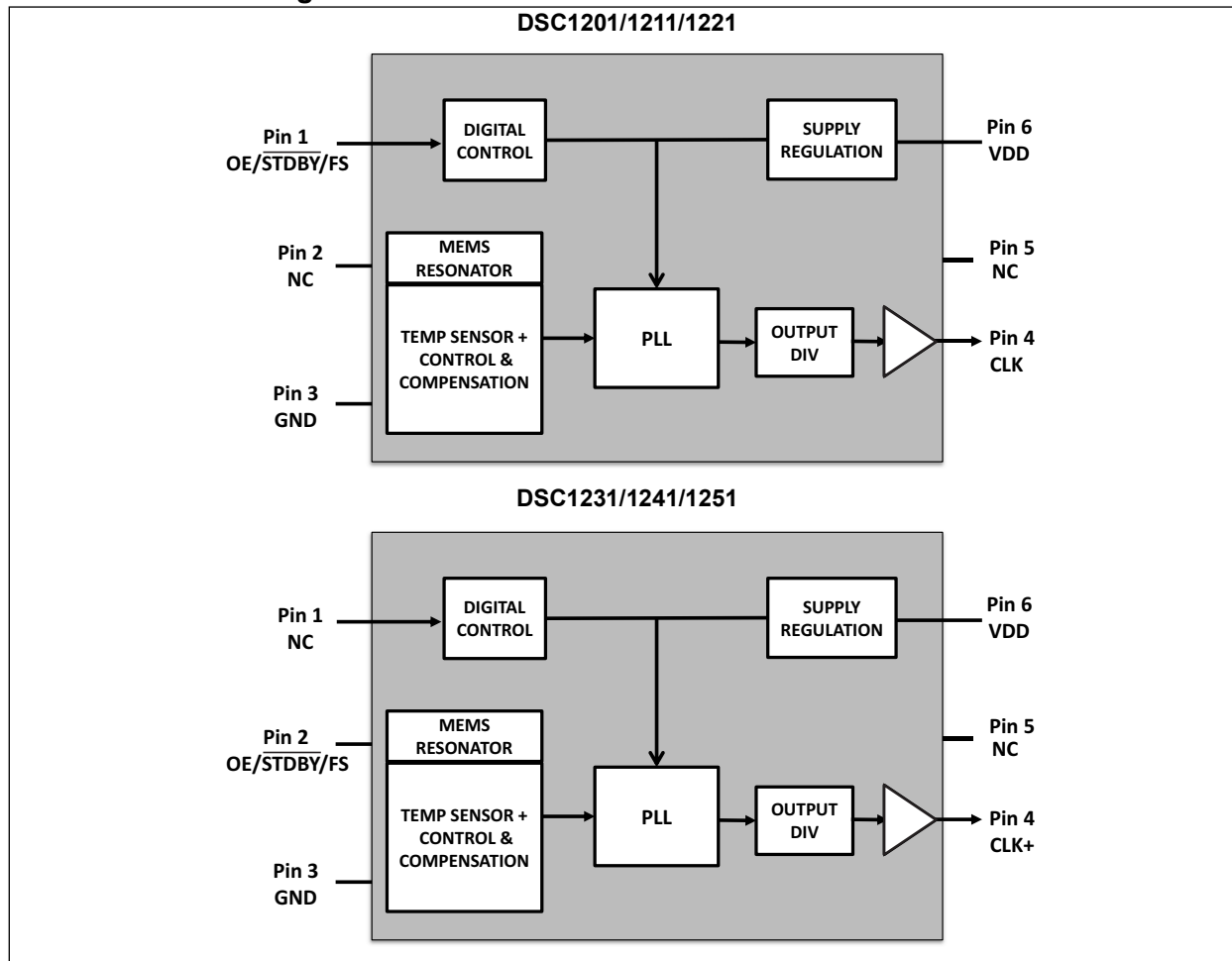
All oscillators are available in industry-standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 4-pin and 6-pin CMOS quartz crystal oscillators.

Package Types



DSC12X1

Functional Block Diagrams



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage	–0.3V to +4.0V
Input Voltage	–0.3V to $V_{DD} + 0.3V$
ESD Protection (HBM)	4 kV
ESD Protection (MM)	400V
ESD Protection (CDM)	1.5 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{DD} = 2.5V \pm 10\%$ or $3.3V \pm 10\%$; $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.25	—	3.63	V	Note 1
Supply Current	I_{DD}	—	27	—	mA	Output enabled, CMOS (no load), $f_{OUT} = 100$ MHz
		—	23	—		Output disabled (tri-state), $f_{OUT} = 100$ MHz
Standby Current	I_{STDBY}	—	2.5	5	μA	Input pin = STDBY = Asserted ($V_{DD} = 3.3V$)
Frequency Stability	f_{STAB}	—	—	± 20	ppm	Includes frequency variations due to initial tolerance, temp., and power supply voltage
		—	—	± 25		
		—	—	± 50		
Aging	Δf	—	—	± 5	ppm	First year at $25^{\circ}C$
		—	—	± 1		Per year after first year
Startup Time	t_{SU}	—	5.5	6	ms	From 90% V_{DD} to valid clock output, $T = +25^{\circ}C$, Note 2
Input Logic Levels	V_{IH}	$0.75 \times V_{DD}$	—	—	V	Input logic high
	V_{IL}	—	—	$0.25 \times V_{DD}$		Input logic low
Output Disable Time	t_{DA}	—	—	25	ns	Note 3
Output Enable Time	t_{EN}	—	—	6	ms	STDBY
		—	—	350	ns	OE
Enable Pull-Up Resistor	—	—	1.5	—	M Ω	Pull-up resistor on pin 1, Note 4
Frequency	f_0	2.5	—	170	MHz	—
Output Logic Level High	V_{OH}	$0.8 \times V_{DD}$	—	—	V	$I = \pm 12$ mA
Output Logic Level Low	V_{OL}	—	—	$0.2 \times V_{DD}$		
Output Transition Time, Rise 20% to 80%; $C_L = 15$ pF	t_R	—	1.2	—	ns	—
Output Transition Time, Fall 20% to 80%; $C_L = 15$ pF	t_F	—	1.1	—	ns	—

DSC12X1

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{DD} = 2.5V \pm 10\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+125^\circ C$, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Duty Cycle	SYM	45	—	55	%	—
Period Jitter, Peak-to-Peak	J_{PTP}	—	25	—	ps	$f_{OUT} = 100$ MHz
Cycle-to-Cycle Jitter, Peak	J_{CC}	—	22	—	ps	$f_{OUT} = 100$ MHz
Integrated Phase Noise (Random)	J_{PH}	—	0.65	—	ps_{RMS}	12 kHz to 20 MHz @ 100 MHz, $T_A = +105^\circ C$

- Note 1:** V_{DD} pin should be filtered with a 0.1 μF capacitor.
- 2:** t_{SU} is the time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.
- 3:** t_{DA} : See the [Output Waveform](#) and the [Test Circuit](#) sections for more information.
- 4:** Output is enabled if pad is floated (not connected).

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	$^\circ C$	—
Storage Temperature Range	T_S	–55	—	+150	$^\circ C$	—
Lead Temperature	—	—	—	+260	$^\circ C$	Soldering, 40s

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#) and [Table 2-2](#).

TABLE 2-1: DSC1201/1211/1221 PIN FUNCTION TABLE

Pin Number	DSC1201		DSC1211		DSC1221	
	Pin Name	Description	Pin Name	Description	Pin Name	Description
1	$\overline{\text{STDBY}}$	Standby.	FS	Frequency select.	OE	Output enable.
2	NC	No connect.	NC	No connect.	NC	No connect.
3	GND	Power supply ground.	GND	Power supply ground.	GND	Power supply ground.
4	CLK	Clock output.	CLK	Clock output.	CLK	Clock output.
5	NC	No connect.	NC	No connect.	NC	No connect.
6	VDD	Power supply.	VDD	Power supply.	VDD	Power supply.

TABLE 2-2: DSC1231/1241/1251 PIN FUNCTION TABLE

Pin Number	DSC1231		DSC1241		DSC1251	
	Pin Name	Description	Pin Name	Description	Pin Name	Description
1	NC	No connect.	NC	No connect.	NC	No connect.
2	$\overline{\text{STDBY}}$	Standby.	FS	Frequency select.	OE	Output enable.
3	GND	Power supply ground.	GND	Power supply ground.	GND	Power supply ground.
4	CLK	Clock output.	CLK	Clock output.	CLK	Clock output.
5	NC	No connect.	NC	No connect.	NC	No connect.
6	VDD	Power supply.	VDD	Power supply.	VDD	Power supply.

2.1 Standby

Complete power down when $\overline{\text{STDBY}}$ is low.

2.2 Frequency Select

Two frequencies may be chosen, selected by FS = High or Low. Please use the [ClockWorks](#) tool to customize frequencies.

2.3 Output Enable

Output buffers (only) are tri-stated when OE is low.

3.0 TERMINATION SCHEME

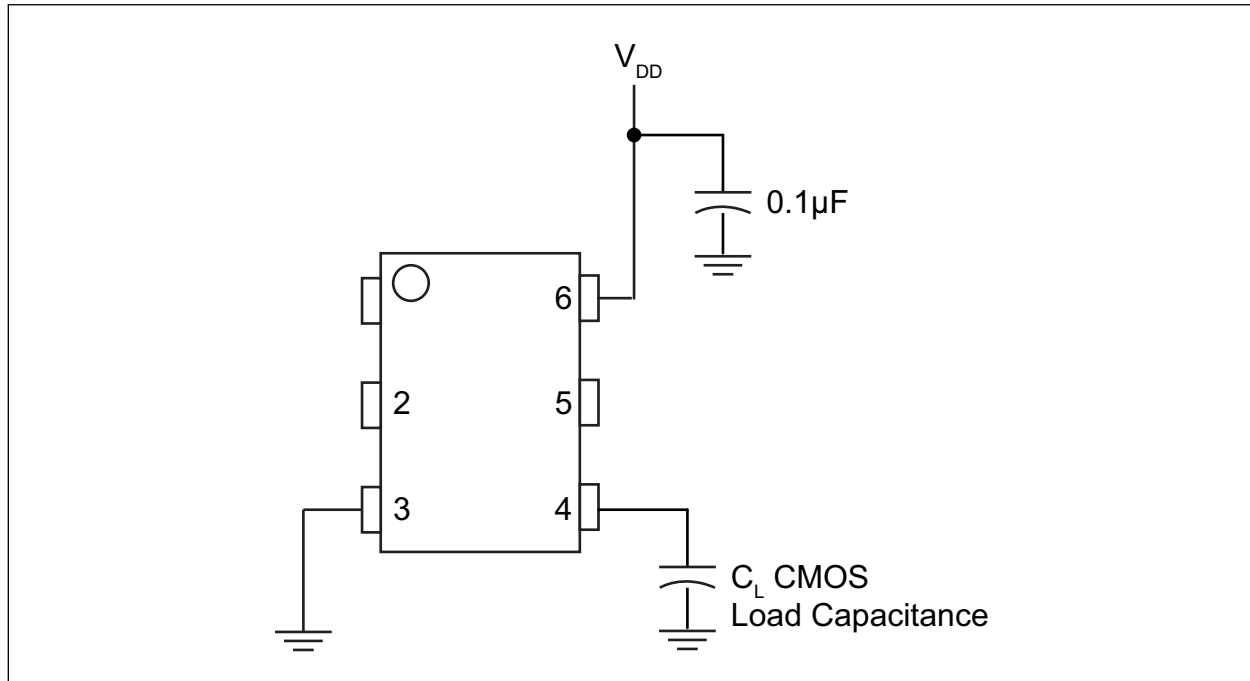


FIGURE 3-1: CMOS Termination.

4.0 OUTPUT WAVEFORM

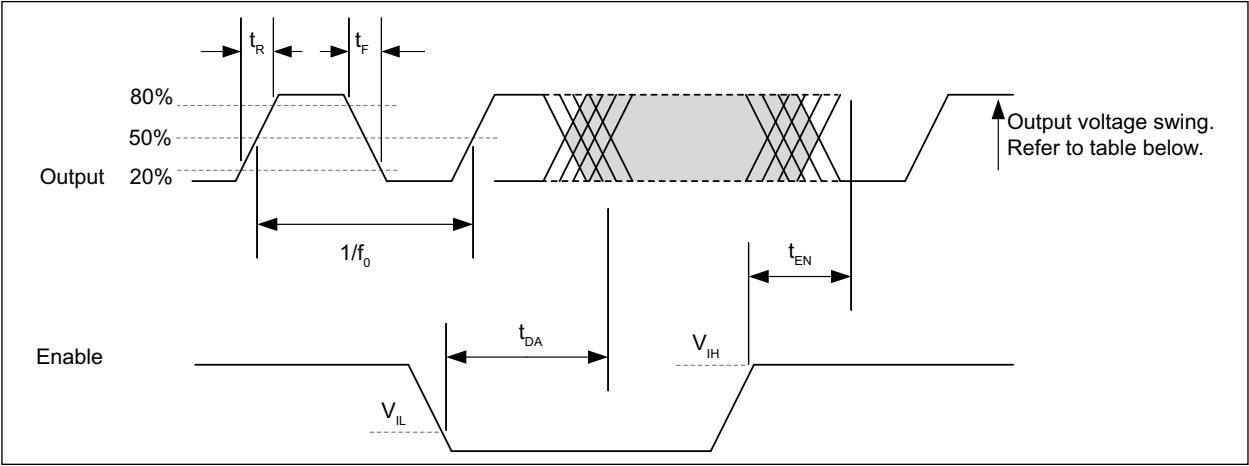


FIGURE 4-1: CMOS Output Waveform.

TABLE 4-1: OUTPUT VOLTAGE SWING BY LOGIC TYPE

Output Logic Protocol	Typical Peak-to-Peak Output Swing
CMOS	V_{OH}, V_{OL}

5.0 TEST CIRCUIT

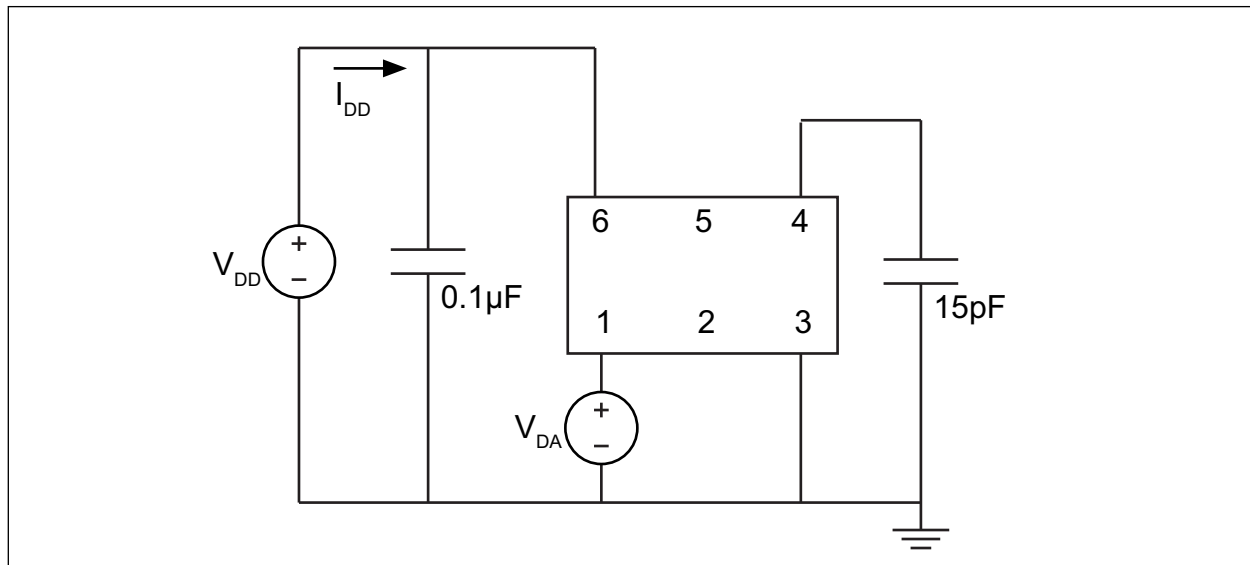


FIGURE 5-1: CMOS Test Circuit.

6.0 SOLDER REFLOW PROFILE

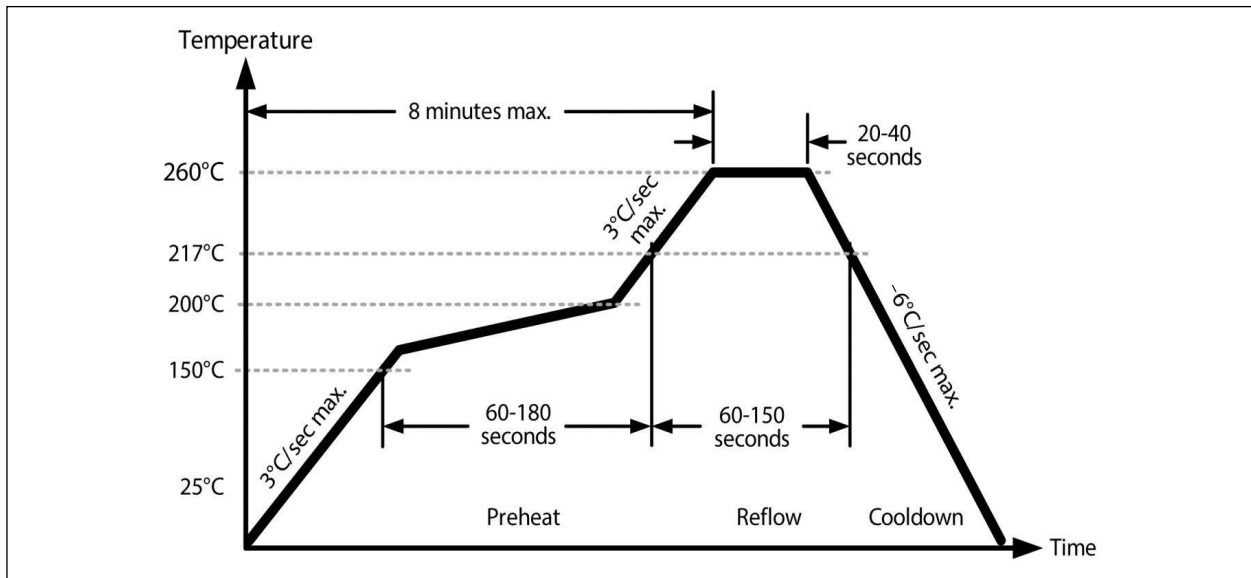


FIGURE 6-1: Solder Reflow Profile.

TABLE 6-1: SOLDER REFLOW

MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	-6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

DSC12X1

7.0 BOARD LAYOUT (RECOMMENDED)

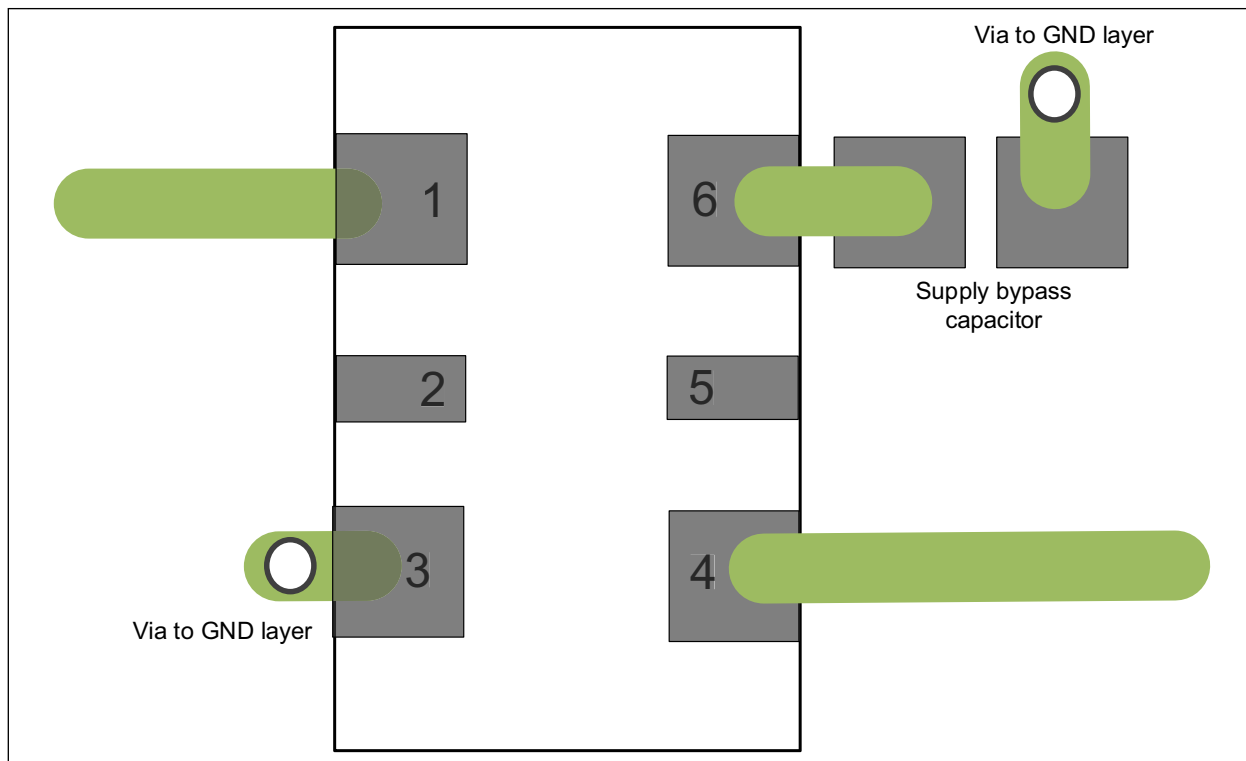


FIGURE 7-1: *DSC12x1 Recommended Board Layout.*

8.0 PHASE NOISE

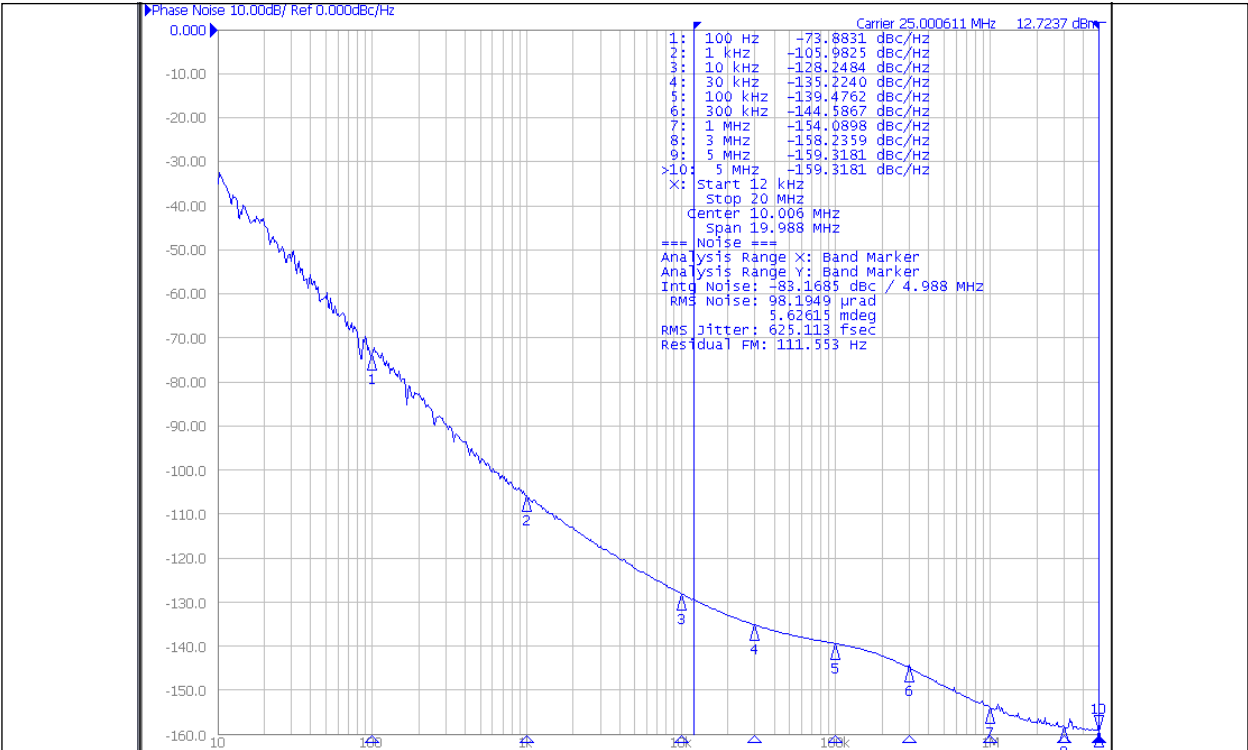


FIGURE 8-1: DSC12x1 Phase Noise at 25 MHz.

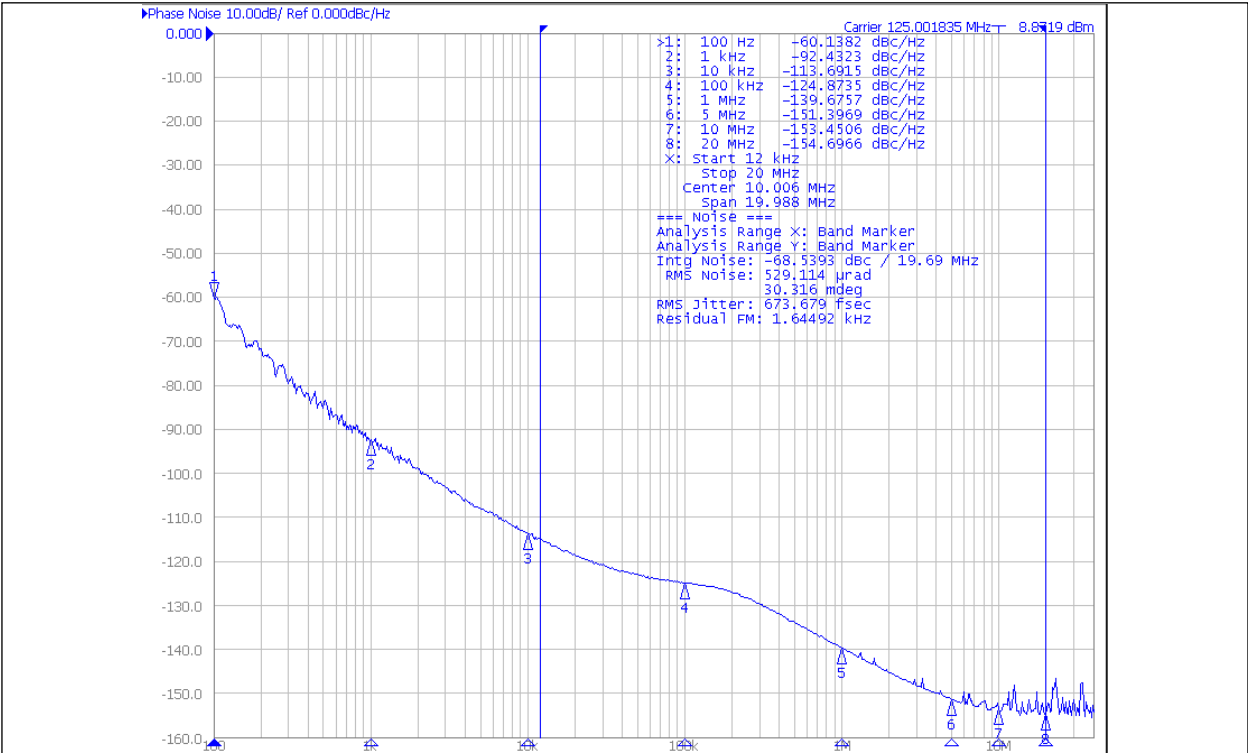
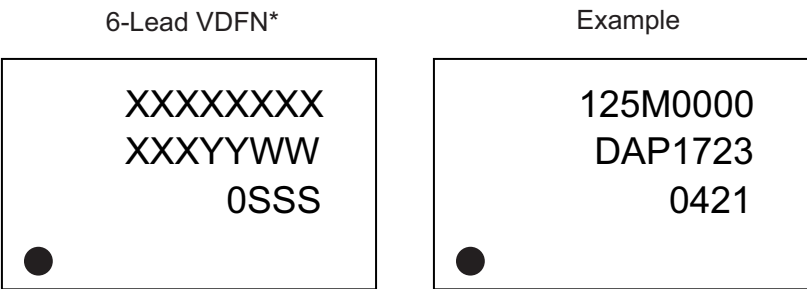


FIGURE 8-2: DSC12x1 Phase Noise at 125 MHz.

9.0 PACKAGING INFORMATION

9.1 Package Marking Information



Legend:

XX...X

Y

YY

WW

SSS

(e3)

*

Product code or customer-specific information

Year code (last digit of calendar year)

Year code (last 2 digits of calendar year)

Week code (week of January 1 is week '01')

Alphanumeric traceability code

Pb-free JEDEC® designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

•, ▲, ▼

Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note:

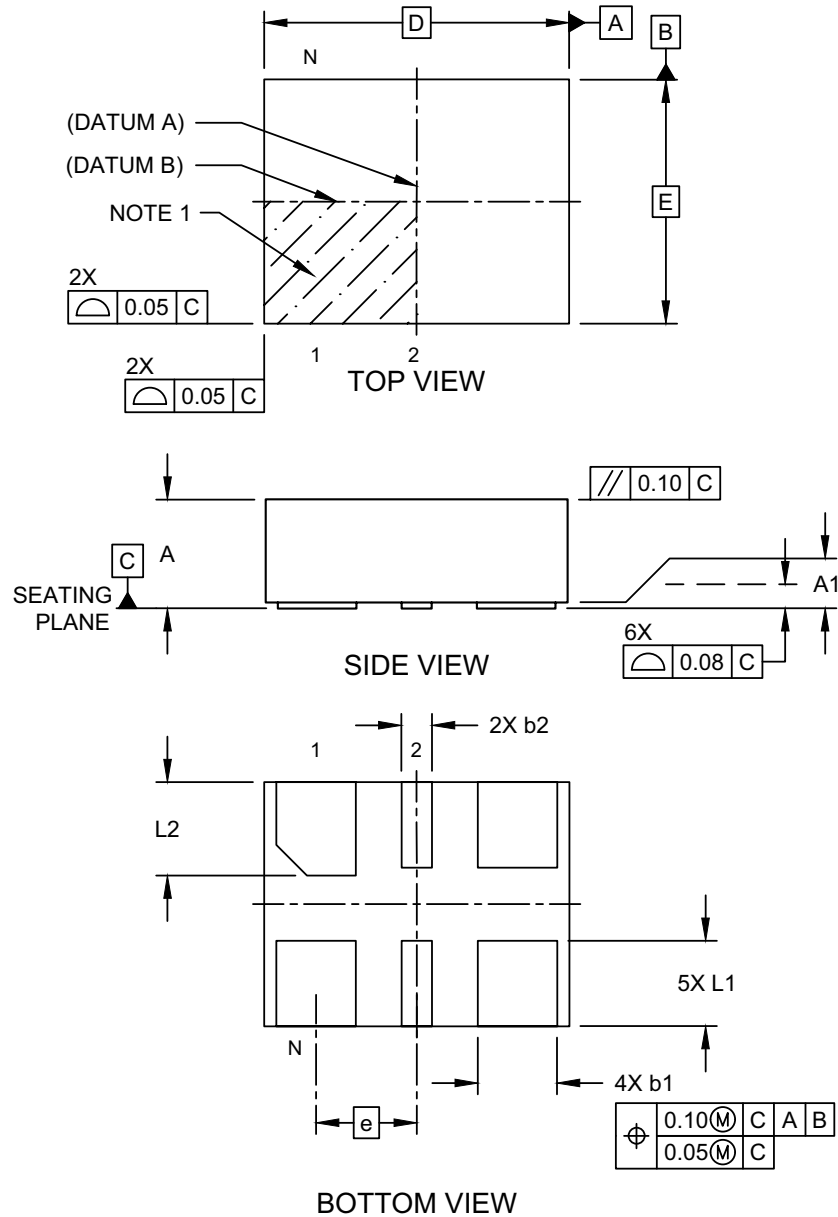
In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: Devices may not include a top-line frequency marking. Product identity and output frequency are defined by the ordering code and accompanying documentation. Devices without a frequency marking remain fully compliant with all applicable datasheet specifications.

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



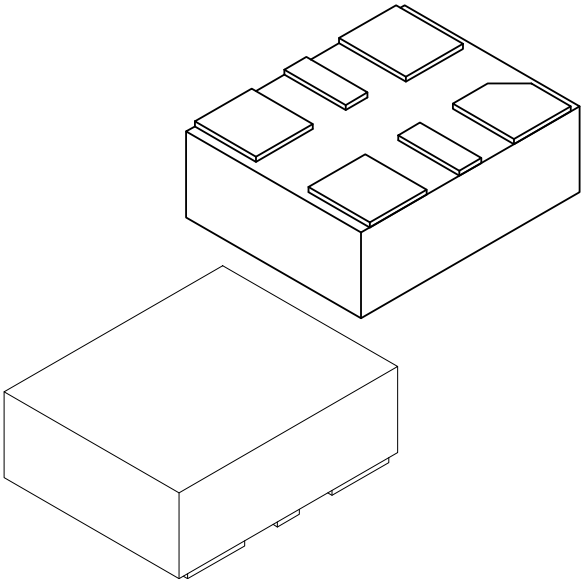
Microchip Technology Drawing C04-1005-J7A Rev E Sheet 1 of 2

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DSC12X1

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.825 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	2.50 BSC		
Overall Width	E	2.00 BSC		
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

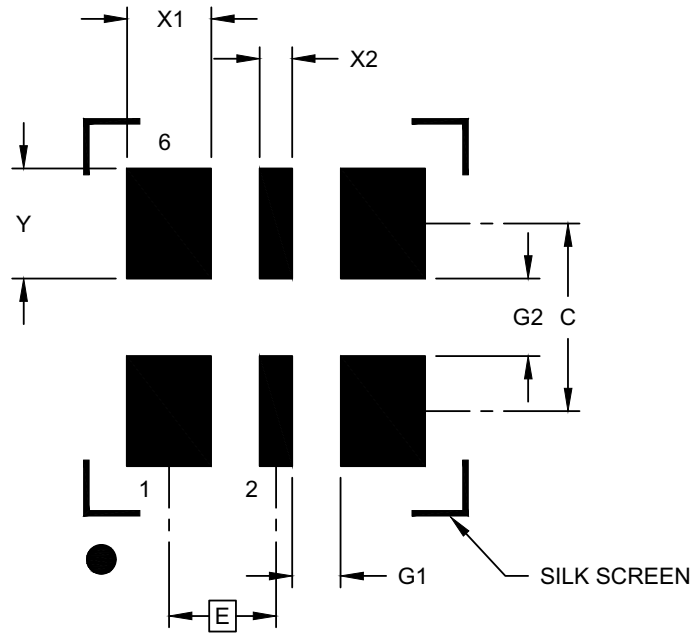
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005-J7A Rev E Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
		MIN	NOM	MAX
Dimension Limits	E		0.825 BSC	
Contact Pitch				
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

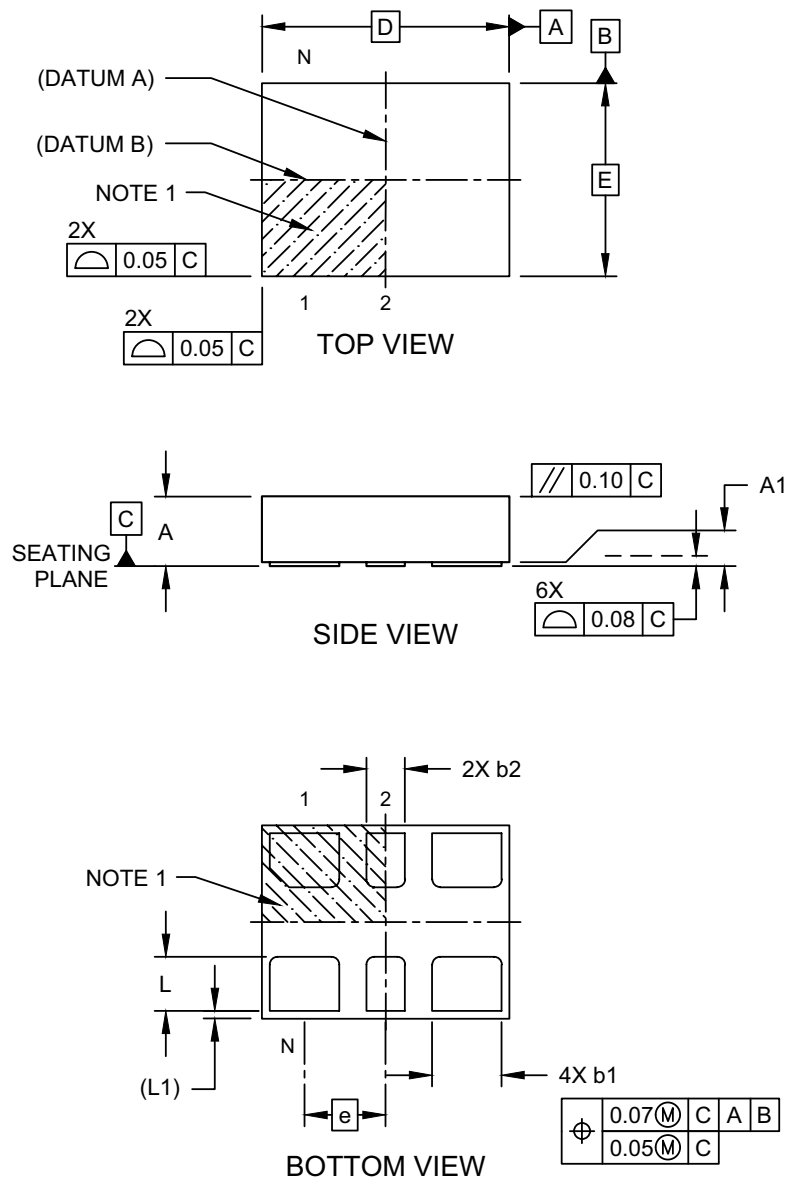
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005-J7A Rev E

DSC12X1

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

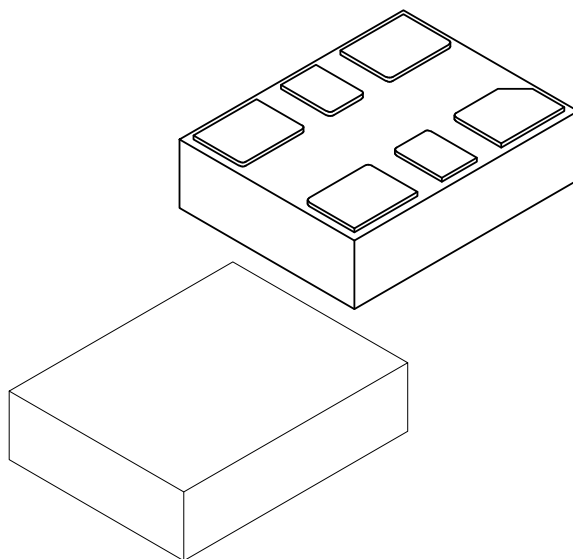


Microchip Technology Drawing C04-1007-H5A Rev C Sheet 1 of 2

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6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	1.05 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	3.20 BSC		
Overall Width	E	2.50 BSC		
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1	0.10 REF		

Notes:

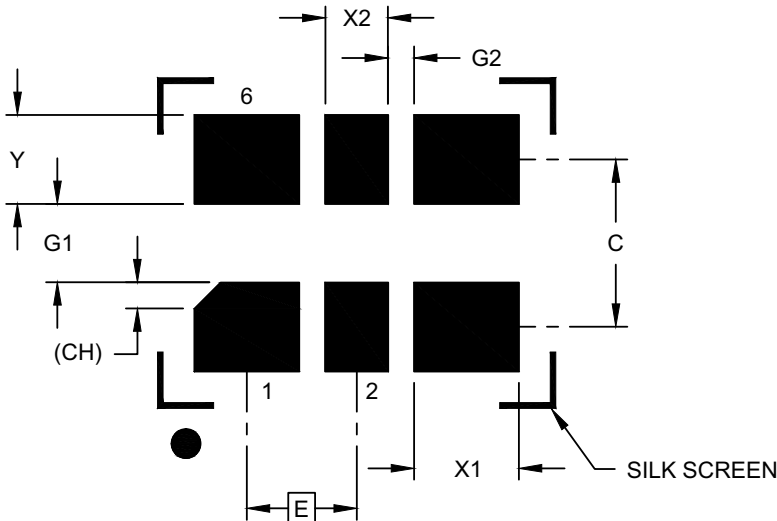
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007-H5A Rev C Sheet 2 of 2

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6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

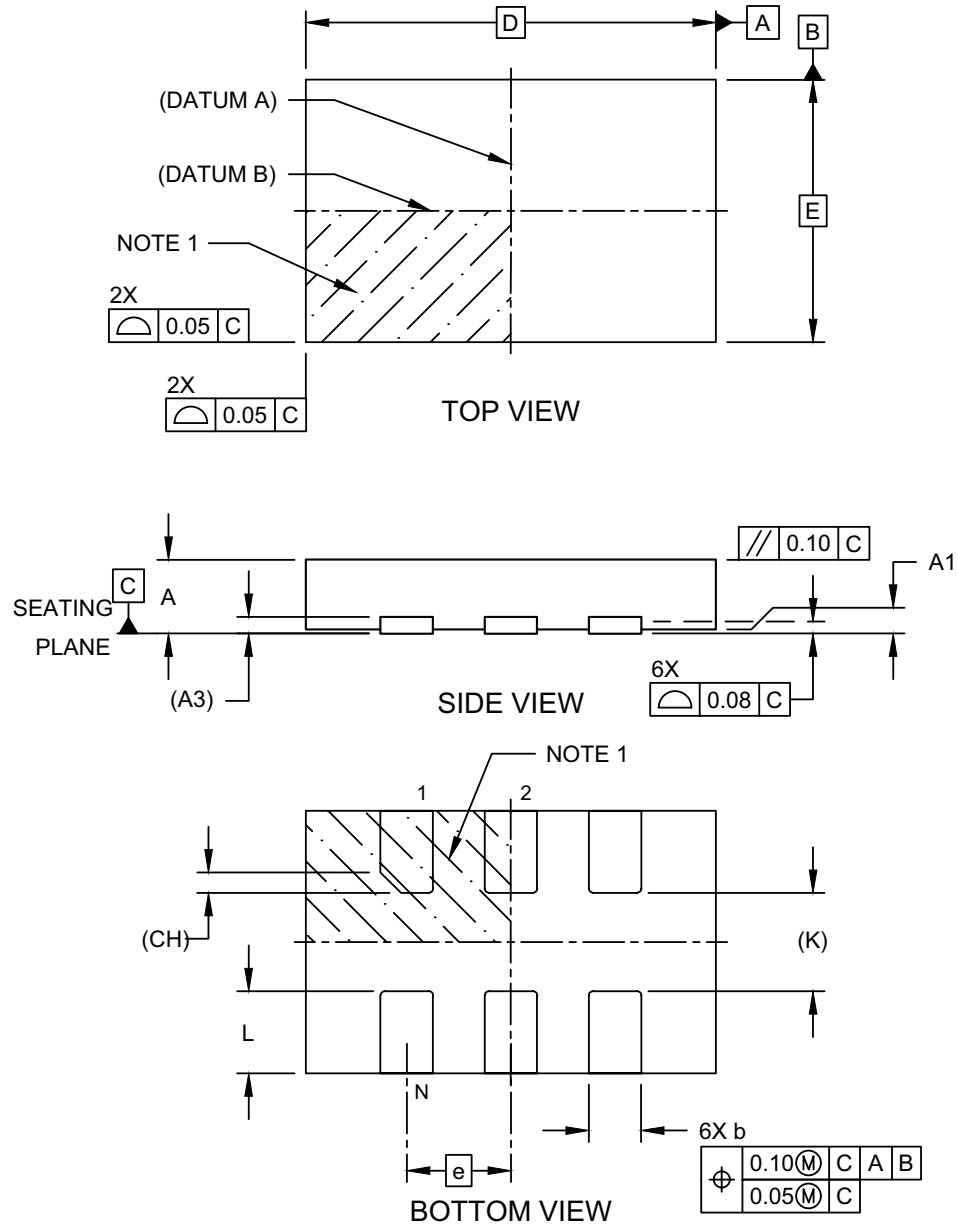
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.05 BSC		
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.75		
Space Between Contacts (X3)	G2	0.25		
Pin 1 Index Chamfer (X4)	CH		0.25	

- Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007-H5A Rev C

6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



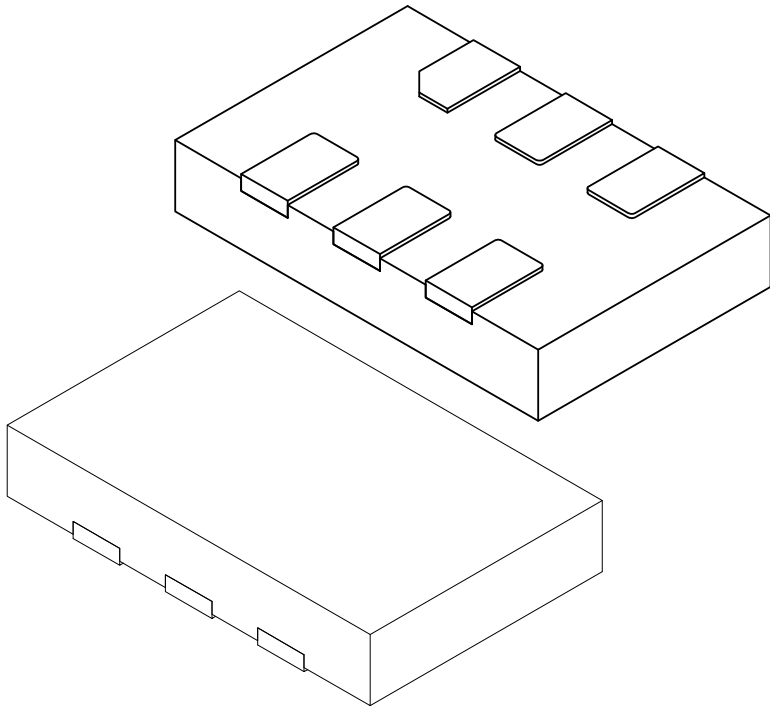
Microchip Technology Drawing C04-1009-H7A Rev B Sheet 1 of 2

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DSC12X1

6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	1.27 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	5.00 BSC		
Overall Width	E	3.20 BSC		
Terminal Width	b	0.59	0.64	0.69
Terminal Length	L	0.90	1.00	1.10
Terminal 1 Index Chamfer	CH	0.25 REF		
Terminal-to-Terminal	K	1.20 REF		

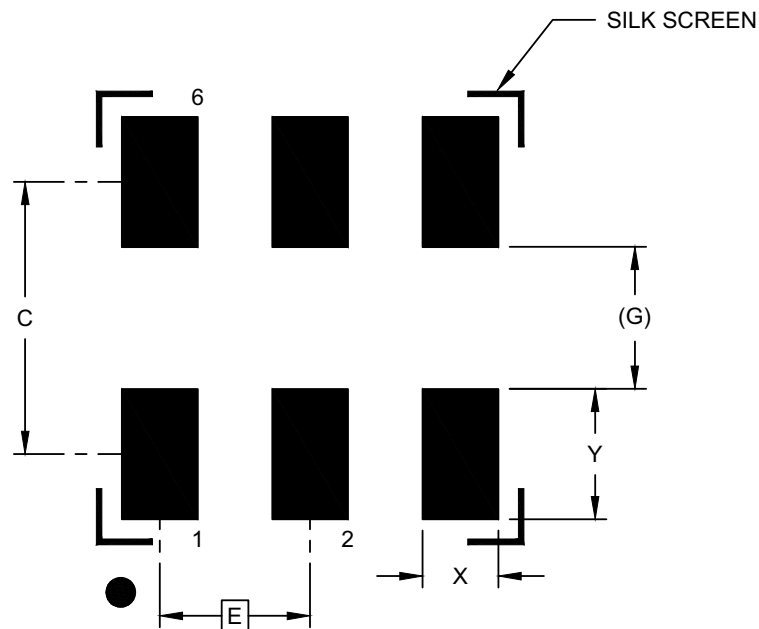
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1009-H7A Rev B Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (H7A) - 3.2x5.0 x0.9 Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		2.30	
Contact Pad Width (X6)	X			0.64
Contact Pad Length (X6)	Y			1.10
Contact Pad to Contact Pad (X4)	G	1.20 REF		

Notes:

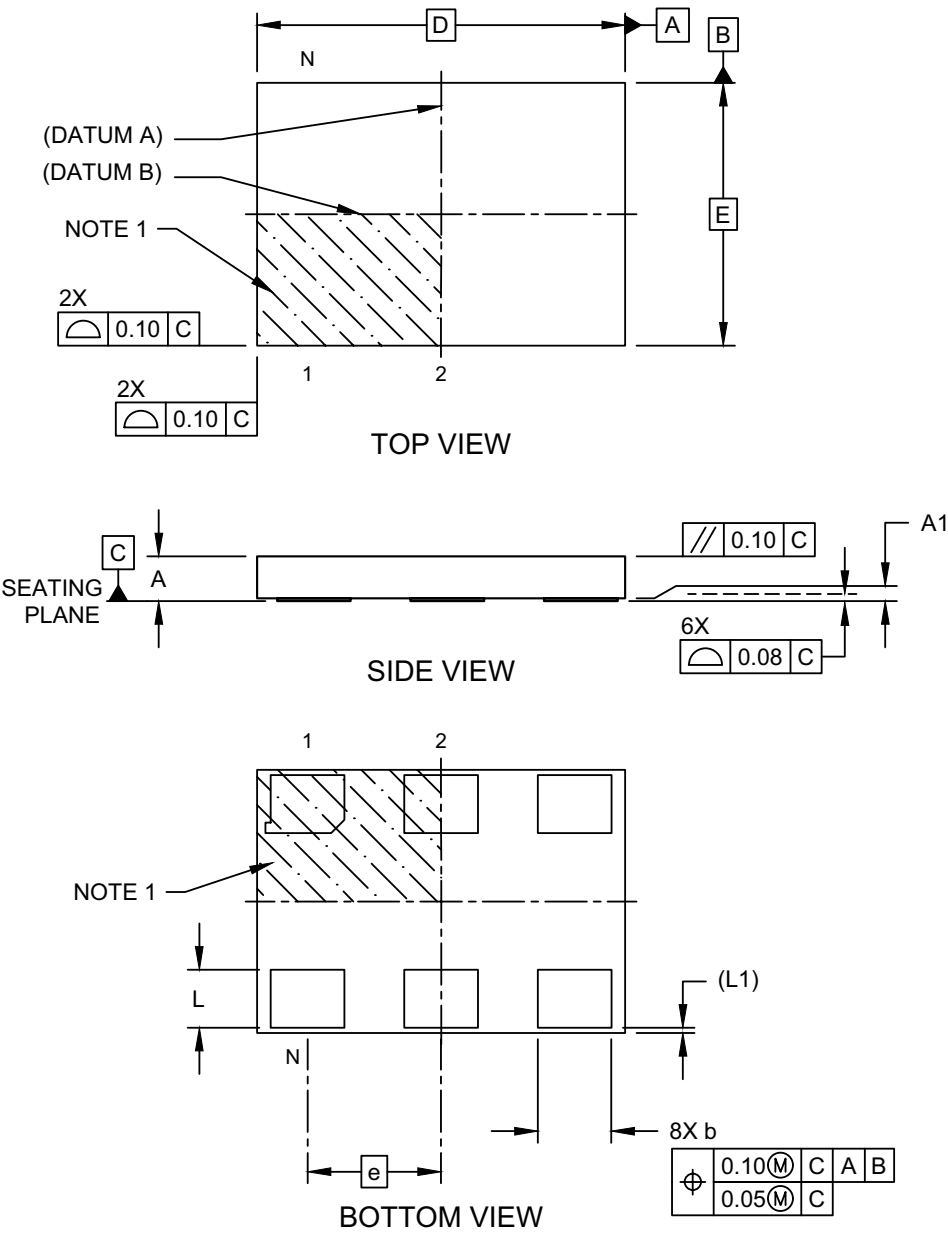
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3009-H7A Rev B

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6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

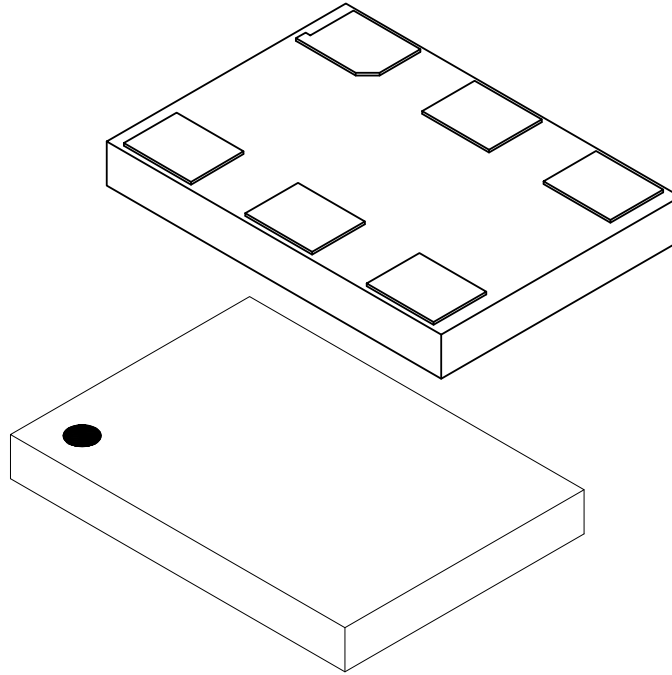
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1227-HPA Rev B Sheet 1 of 2

6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		6		
Pitch	e		2.54 BSC		
Overall Height	A		0.80	0.85	0.90
Standoff	A1		0.00	0.02	0.05
Overall Length	D		7.00 BSC		
Overall Width	E		5.00 BSC		
Terminal Width	b		1.30	1.40	1.50
Terminal Length	L		1.00	1.10	1.20
Pullback	L1		0.10 REF		

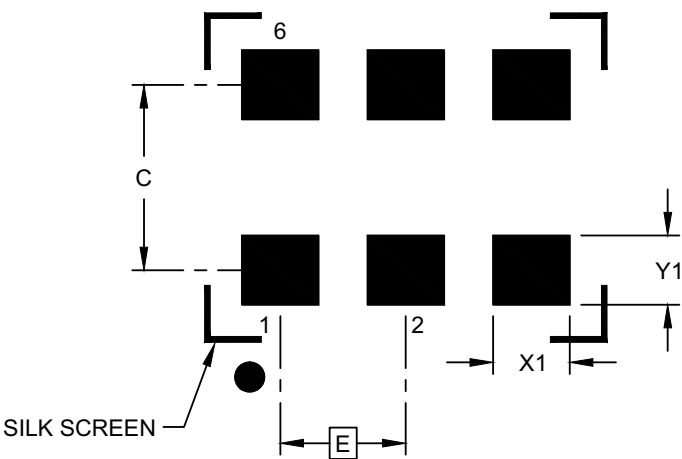
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1227-HPA Rev B Sheet 2 of 2

6-Lead Very Thin Dual Flatpack, No Lead Package (HPA) - 7x5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Contact Pad Spacing	C		3.90	
Contact Pad Width (X6)	X1			1.55
Contact Pad Length (X6)	Y1			1.40

- Notes:
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3227-HPA Rev B

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Initial release of DSC12x1 as Microchip data sheet DS20006010A.

Revision B (September 2024)

- Updated values and conditions for Output Logic Levels, Output Transition Times, Period Jitter, and Cycle-to-Cycle Jitter in the [Electrical Characteristics](#) table.

Revision C (June 2025)

- Added DSA1201 reference to [Features](#) and the [Product Identification System](#) sections for customers seeking AEC-Q100 qualified parts.
- Updated the package outline drawings to the most current versions.

Revision D (March 2026)

- Added a note regarding bulk quantities to the [Product Identification System](#) section.
- Added aging data to the [Electrical Characteristics](#) table.

Revision E (July 2026)

- Added a note at the end of the [Package Marking Information](#) section about frequency marking.

DSC12X1

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		X	X	X	X	X	-XXXXXXXX	X
Device		Control Pin	Output Format	Package	Temperature	Freq. Stability	Output Frequency	Media Type
Device:		DSC12: High Performance CMOS MEMS Oscillator (Note 3)						
Control Pin:		0 = Pin 1 $\overline{\text{STDBY}}$ with Pull-up 1 = Pin 1 Frequency Select with Pull-up (Note 1) 2 = Pin 1 OE with Pull-up 3 = Pin 2 $\overline{\text{STDBY}}$ with Pull-up 4 = Pin 2 Frequency Select with Pull-up (Note 1) 5 = Pin 2 OE with Pull-up						
Output Format:		1 = CMOS						
Package:		N = 7 mm x 5 mm 6-Lead VDFN (Note 2) B = 5 mm x 3.2 mm 6-Lead VDFN C = 3.2 mm x 2.5 mm 6-Lead VDFN D = 2.5 mm x 2 mm 6-Lead VDFN						
Temperature:		A = -40°C to +125°C L = -40°C to +105°C I = -40°C to +85°C E = -20°C to +70°C						
Frequency Stability:		1 = ±50 ppm 2 = ±25 ppm 3 = ±20 ppm						
Output Frequency:		xMxxxxx= <10 MHz xxMxxxx= <100 MHz xxxMxxxx= >100 MHz CCCCC= with Frequency Select PROG = TimeFlash						
Media Type:		<blank>= Bulk (Note 4) T = 1,000/Reel B = 3,000/Reel						

Examples:

a) DSC1201NE1-25M00000T: Pin 1 $\overline{\text{STDBY}}$ with Pull-up, CMOS Output, 7x5 VDFN, -20°C to +70°C, ±50 ppm, 25 MHz Output Frequency, 1,000/Reel

b) DSC1211CL3-C0013: Pin 1 Frequency Select with Pull-up, CMOS Output, 3.2x2.5 VDFN, -40°C to +105°C, ±20 ppm, Frequency Select: 24 MHz & 25 MHz, Bulk

c) DSC1221BI2-19M5000000B: Pin 1 OE with Pull-up, CMOS Output, 5x3.2 VDFN, -40°C to +85°C, ±25 ppm, 19.5 MHz Output Frequency, 3,000/Reel

d) DSC1251DL3-55M82000T: Pin 2 OE with Pull-up, CMOS Output, 2.5x2 VDFN, -40°C to +105°C, ±20 ppm, 55.82 MHz Output Frequency, 1,000/Reel

e) DSC1231NI1-C0014B: Pin 2 $\overline{\text{STDBY}}$ with Pull-up, CMOS Output, 7x5 VDFN, -40°C to +85°C, ±50 ppm, Frequency Select: 100 MHz & 156.25 MHz, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 1: Please use the [ClockWorks](#) tool to select two frequencies and create the customized full part number.

2: With the N package option, only Pin 1 can be used for control (only allowable control pin options are 0, 1, or 2).

3: For AEC-Q100 qualified parts, please refer to the DSA1201 family.

4: On orders for bulk CPNs, product may be supplied in either cut tape (without a reel) or tube packaging, depending on availability. For Tape & Reel orders that are <1000 pieces, product may be supplied on cut tape (without a reel) depending on availability.

Examples:

- a) DSC1201NE1-25M00000T: Pin 1 STDBY with Pull-up, CMOS Output, 7x5 VDFN, -20°C to +70°C, ±50 ppm, 25 MHz Output Frequency, 1,000/Reel
- b) DSC1211CL3-C0013: Pin 1 Frequency Select with Pull-up, CMOS Output, 3.2x2.5 VDFN, -40°C to +105°C, ±20 ppm, Frequency Select: 24 MHz & 25 MHz, Bulk
- c) DSC1221BI2-19M500000B: Pin 1 OE with Pull-up, CMOS Output, 5x3.2 VDFN, -40°C to +85°C, ±25 ppm, 19.5 MHz Output Frequency, 3,000/Reel
- d) DSC1251DL3-55M82000T: Pin 2 OE with Pull-up, CMOS Output, 2.5x2 VDFN, -40°C to +105°C, ±20 ppm, 55.82 MHz Output Frequency, 1,000/Reel
- e) DSC1231NI1-C0014B: Pin 2 STDBY with Pull-up, CMOS Output, 7x5 VDFN, -40°C to +85°C, ±50 ppm, Frequency Select: 100 MHz & 156.25 MHz, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

DSC12X1

NOTES:

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