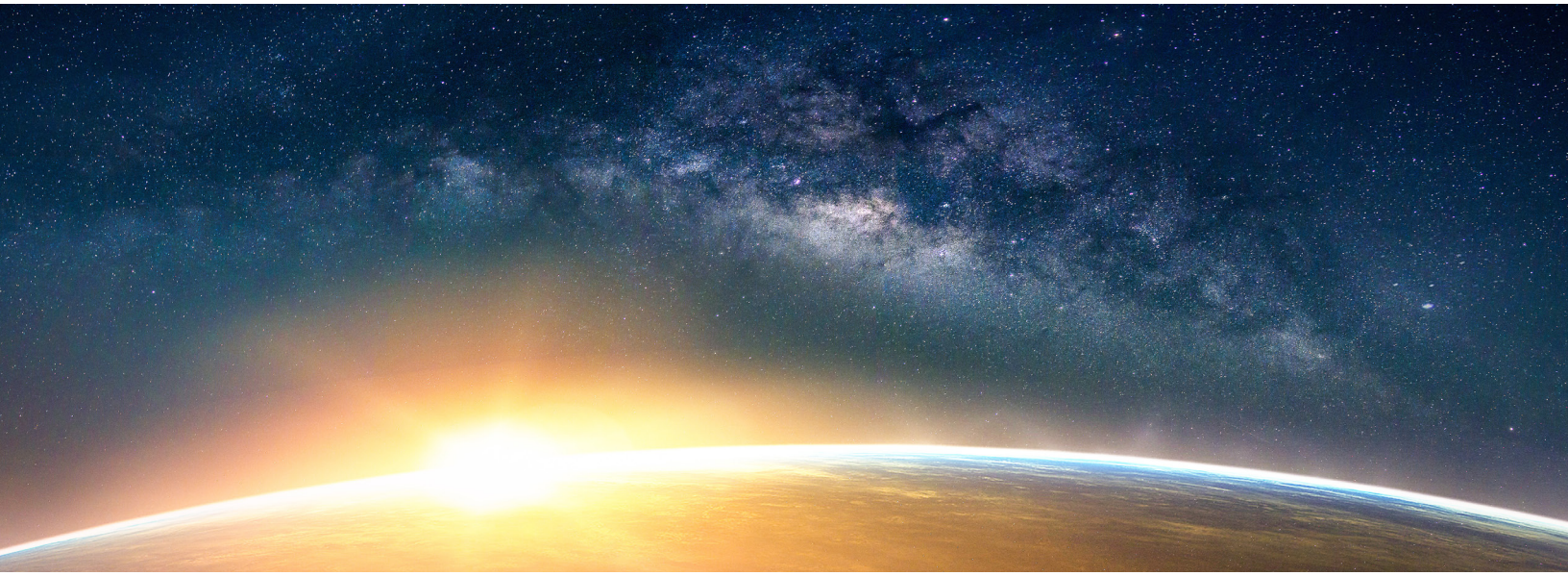
Aerospace and Defense

MICROCHIP

Radiation-Tolerant FPGAs

Space Solutions









www.microchip.com

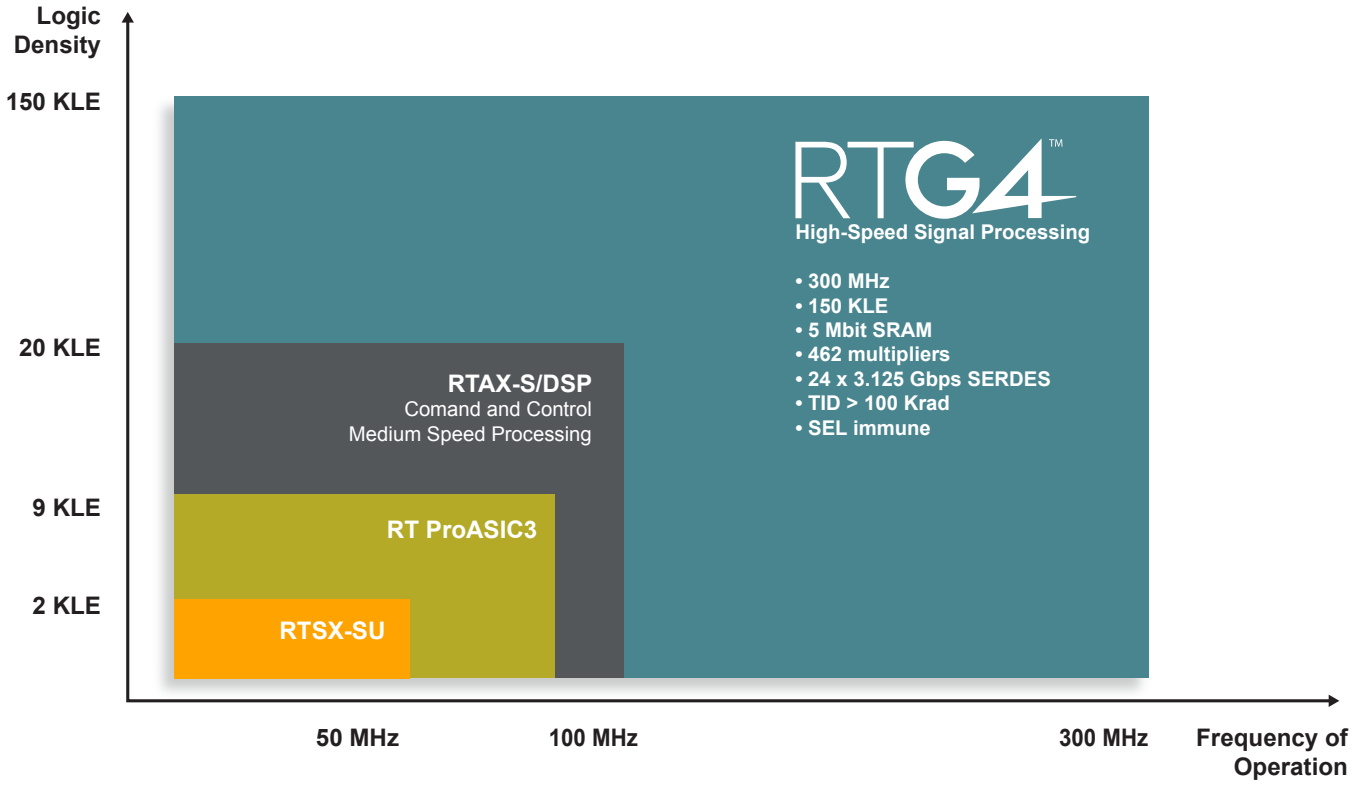
Taking Designs From Earth to Outer Space

Microchip's high-reliability, low-power spaceflight FPGAs are your best design choice for low Earth orbit, deep space or anything in between. With a history of providing the most reliable, robust, low-power Flash- and antifuse-based FPGAs in the industry, we offer the best combination of features, performance and radiation tolerance.

In addition to FPGAs, we provide radiation-hardened and radiation-tolerant solutions ranging from diodes, transistors and power converters to ASICs, RF components, oscillators and timing products, to mixed-signal integrated circuits, custom semiconductor packaging and integrated power distribution systems.

Now Delivering High-Speed Signal Processing

Microchip's FPGAs facilitate the design of high-speed communications payloads, high-resolution sensors and instruments, and flight-critical systems that enable tomorrow's space missions. Only we can meet the power, size, cost and reliability targets that reduce time-to-launch and minimize cost and schedule risks.



Flight Heritage

RTSX-SU

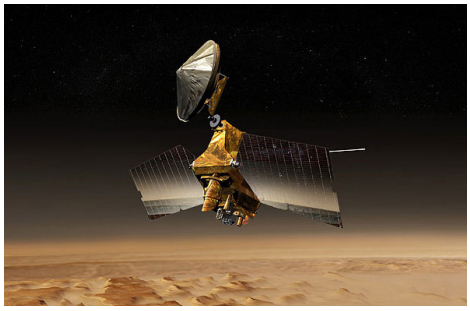
- Flight heritage since 2005
- EAR-controlled
- QML class Q qualified

RTAX

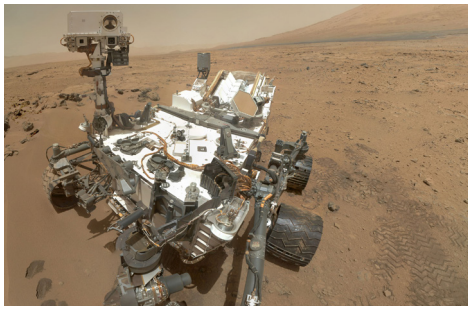
- Flight heritage since 2007
- On-board SRAM and DSP Mathblocks
- EAR-controlled
- QML class V qualified

RT ProASIC3

- Flight heritage since 2013
- First Flash-based RT FPGA in space
- EAR-controlled
- QML class Q qualified



Mars Reconnaissance Orbiter



Curiosity (Mars Science Lab)

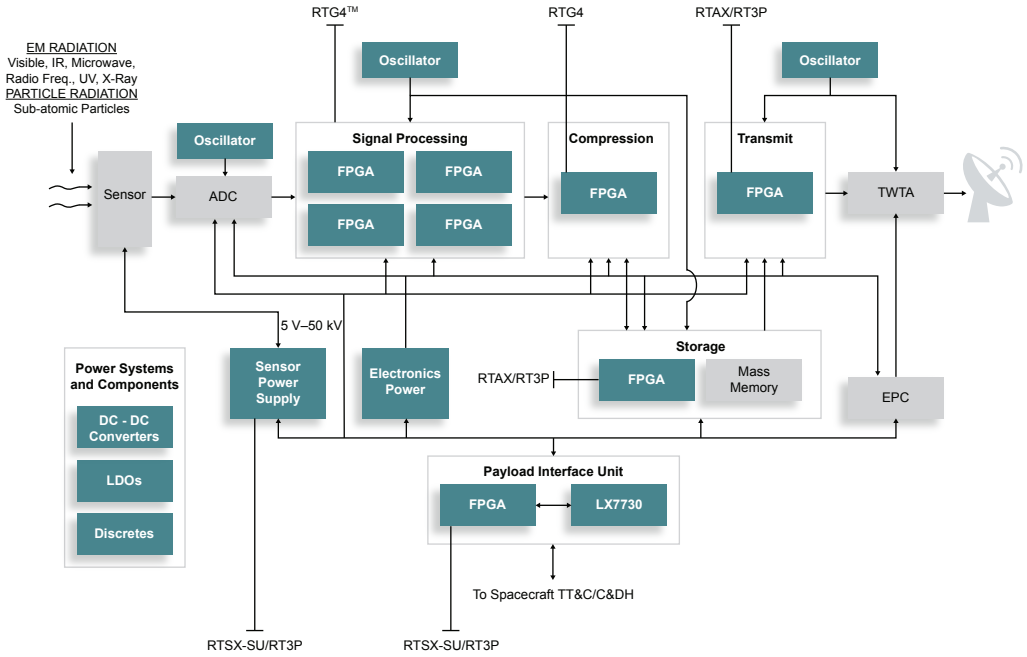


NASA IRIS

For more information, see www.microsemi.com/products/fpga-soc/rad-tolerant-fpgas

Remote Sensing Payload Example

Microchip FPGAs have achieved flight heritage on many programs in command and control applications that require limited amounts of logic and modest performance levels. RTG4™ has much greater logic density and much higher performance, which give a >20x improvement in signal processing throughput. Now, designers of high-speed datapaths in space payloads can use RTG4 to take advantage of the flexibility and ease-of-use of programmable logic. This is particularly important for remote sensing instruments, which must perform rapidly increasing amounts of on-board processing, as sensor resolution is increasing faster than downlink bandwidth.



RTSX-SU, RTAX and RT ProASIC3 FPGAs are used for command, control and interfacing applications, where limited logic and performance is needed. RTG4 can be deployed where maximum data throughput is needed, such as in signal processing and compression.

RTG4 Radiation Effects

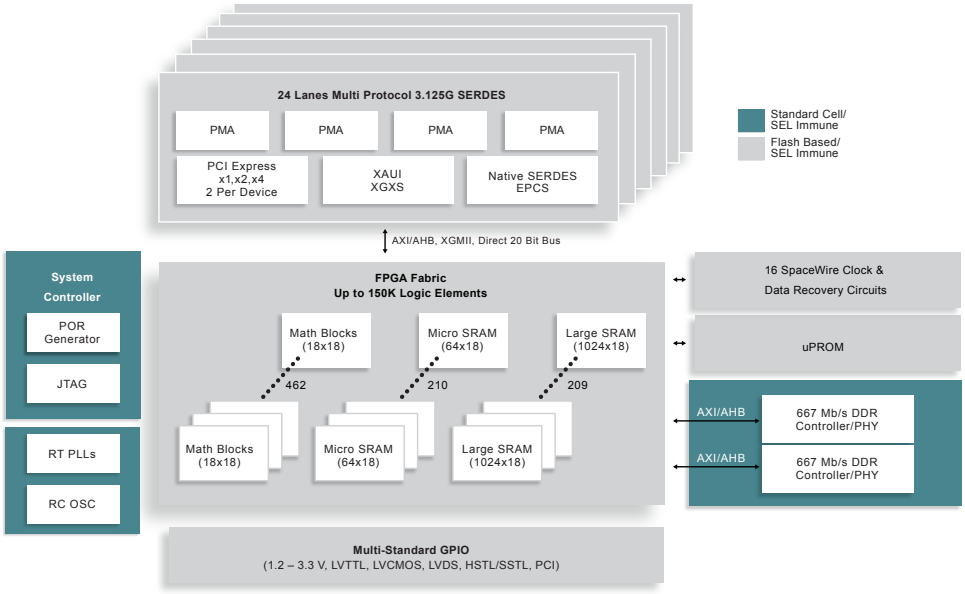
RTG4 FPGAs are manufactured on a low-power 65 nm process with substantial reliability heritage. RTG4 FPGAs are qualified to MIL-STD-883 Class B, and Microchip will seek QML Class Q and Class V qualification.

RTG4 FPGAs are immune to radiation (SEU)-induced changes in configuration due to the robustness of the Flash cells used to connect and configure logic resources and routing tracks. No background scrubbing or reconfiguration of the FPGA is needed to mitigate changes in configuration due to radiation effects. Data errors due to radiation are mitigated by hardwired SEU resistant flip-flops in the logic cells and mathblocks. Single Error Correct Double Error Detect (SECDED) protection is optional for the embedded SRAM (LSRAM and uSRAM) and the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories.

- Immune to single event latch-up
- Immune to configuration upsets
- Total ionizing dose to >100 Krad (Si)
- Single event upsets <1 x 10^{-11} errors/bit-day (GEO solar min)

High-Speed RT FPGAs for Signal-Processing Applications

RTG4 FPGAs integrate Microchip's fourth-generation Flash-based FPGA fabric high-performance serialization/deserialization (SERDES) transceivers on a single chip while maintaining resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO and deep space), high-altitude aviation, medical electronics, and nuclear power plant control.



RTG4 Product Family

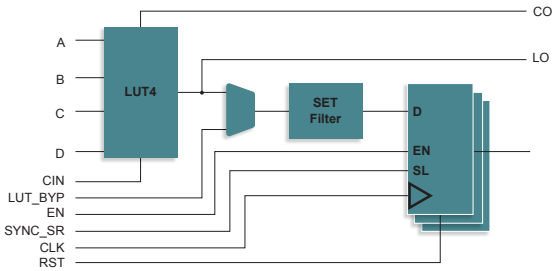
	Features	RT4G150	
	Packages	**CCGA/CLGA 1657**	**CQ352**
Logic/DSP	Maximum logic elements (LUT4 + TMR flip-flop)	151, 824	151, 824
	Mathblocks (18-bit x 18-bit)	462	462
	Radiation-tolerant PLLs	8	8
Memory	LSRAM 24.5 kbit blocks (with ECC)	209	209
	uSRAM 1.5 kbit blocks (with ECC)	210	210
	Total SRAM Mbits	5.2	5.2
	uPROM Kbits	374	374
High-Speed Interface	SERDES lanes (3.125 Gbps)	24	4
	PCIe endpoints	2	1
	DDR2/3 SDRAM controllers (with ECC)	2	0
	SpaceWire clock and data recovery circuits	16	4
User I/Os	MSIO (3.3V)	240	166
	MSIOD (2.5V)	300	0
	DDRIO (2.5V)	180	0
	User I/O (excluding SERDES)	720	166

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4

Logic Module

Dedicated STMR flip-flop with asynchronous self correction

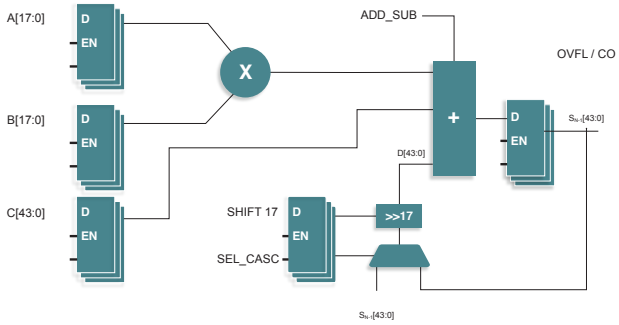
- With enable, global asynchronous set/reset and local synchronous set/reset
- Fast carry chain to complement Mathblock performance
- 300 MHz for 32-bit functions (no SET filter)
- 250 MHz for 32-bit function (SET filter deployed)
- Industry standard LUT4 for efficient synthesis
- LUT4 and flip-flop in same module can be used independently
- Hierarchical routing architecture enables >95% module utilization



Mathblock

18 × 18 multiplier with advanced accumulate

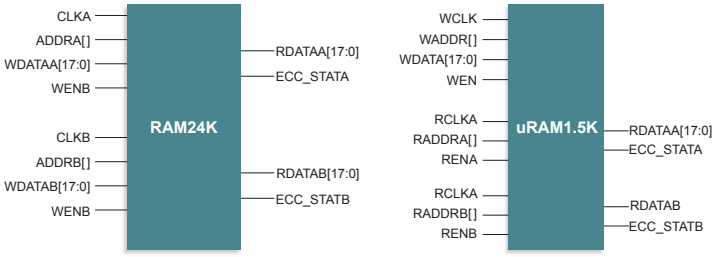
- High performance for signal processing throughput
- 300 MHz without SET mitigation
- 250 MHz with SET mitigation
- New 3-input adder function: (C + D) ± (A * B)
- Optional SEU-protected registers on inputs and outputs (including C input)



Memory Blocks

Radiation-Tolerant built-in optional EDAC (SECDED)

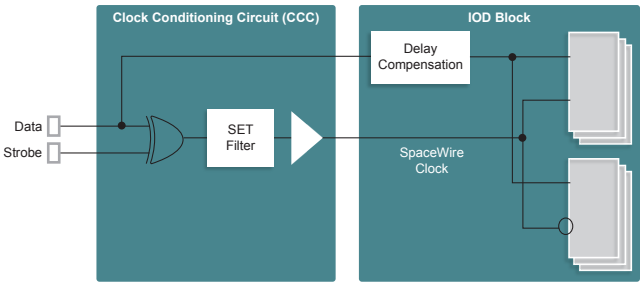
- Resistant to multi-bit upset
- LSRAM up to 24.5 KBit
- Dual-port and two-port option
- High-performance synchronous operation
- Example usage—large FFT memory
- uRAM up to 1.5 KBit
- Three port memory—synchronous write port, two asynchronous or synchronous read ports
- Example usage—folded FIR filters and FFT twiddle factors



SpaceWire Receiver Interface

SpaceWire clock and data recovery

- Up to 16 hardwired clock and data recovery circuits
- Up to 200 Mbps SpaceWire data rate under optimum conditions
- Delay compensation for optimum alignment of clock and data
- Supports LVDS and LVTTL inputs



For the latest DLA cross-reference information, see
www.microsemi.com/document-portal/doc_download/130726-dla-cross-reference-guide

Radiation-Tolerant FPGA Alternative to Radiation-Hardened ASICs

RTAX-S/SL radiation-tolerant FPGAs offer industry-leading advantages for designers of spaceflight systems. High-performance, low-power consumption, true single-chip form factor and live-at-power-up operation all combine to make RTAX-S/SL devices the FPGAs of choice for space designers.

- Single event latch-up (SEL) immune to LET_{TH} in excess of 117 MeV-cm^2/mg
- Single event upset (SEU) less than 1E^{-10} errors per bit-day (worst-case geosynchronous orbit)
- Total ionizing dose (TID): 300 krad functional, 200 krad parametric
- Pin-compatible commercial devices for easy and inexpensive prototyping
- Ceramic package offerings (CQFP, CCGA, CLGA)
- Prototype units with same footprint and timing as flight units
- Up to 840 user-programmable I/Os
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow
  V Flow: MIL-PRF-38535 QML Class V

RTAX-S/SL Devices

RTAX-S/SL Devices	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL
Equivalent System Gates Capacity	250,000	1,000,000	2,000,000	4,000,000
Register (R-cells) Modules	1,408	6,048	10,752	20,160
Combinatorial (C-cells) Modules	2,816	12,096	21,504	40,320
Embedded RAM/FIFO Blocks (without EDAC)	12	36	64	120
Embedded RAM/FIFO (without EDAC) (k = 1,024 bits)	54k	162k	288k	540k
Hardwired Clocks (segmentable)	4	4	4	4
Routed Clocks (segmentable)	4	4	4	4
I/O Banks	8	8	8	8
User I/Os (maximum)	248	418	684	840
I/O Registers	744	1,548	2,052	2,520
CG/LG Package Pins	624	624	624, 1152	1272
CQ Package Pins	208, 352	352	256, 352	352

I/Os per Package

RTAX-S/SL Devices	RTAX250S/SL				RTAX1000S/SL				RTAX2000S/SL				RTAX4000S/SL			
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os	Single-Ended I/Os	Differential I/O Pairs	Non-Adjacent I/O Pairs	Total I/Os
CQ208	7	41	13	115												
CQ256									4	66	0	136				
CQ352	2	98	0	198	2	98	0	198	2	98	0	198	4	81	0	166
CG624	0	124	0	248	68	170	5	418	52	178	5	418				
CG1152									0	342	0	684				
CG1272													0	420	0	840

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-s-sl

Industry's Most Reliable Spaceflight FPGAs With DSP Capabilities

RTAX-DSP spaceflight FPGAs add embedded radiation-tolerant, multiply-accumulate blocks to the tried-and-trusted industry standard RTAX-S/SL product family. The result is a dramatic increase in device performance and utilization when implementing arithmetic functions (such as those encountered in DSP algorithms) without sacrificing reliability or radiation tolerance. RTAX-DSP integrates complex DSP functions into a single device without any external components for code storage or multiple-chip implementations for radiation mitigation.

- Highly reliable, nonvolatile antifuse technology
- 2,000,000 to 4,000,000 system gates
- Up to 120 DSP mathblocks with 125 MHz 18 × 18 bit multiply-accumulate
- Up to 540 Kbits of embedded memory with optional EDAC protection
- Up to 840 user-programmable I/Os
- RTAX-DL version with low static power
- Total dose: 300 Krad (functional) and 200 Krad (parametric)
- SEU less than $1E^{-10}$ errors per bit-day (worst-case GEO)
- SEL immune to LETTH in excess of 117 MeV-cm^2/mg
- Enhanced SET for R-cells: 0.12 events/RTAX2000D device/100 years at 120 MHz
- Advanced CCGA and LGA packaging for space applications
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow
  V Flow: MIL-PRF-38535 QML Class V

RTAX-DSP Devices

RTAX-DSP Devices	RTAX2000D/DL	RTAX4000D/DL
Equivalent System Gates Capacity	2,000,000	4,000,000
Register (R-cells) Modules	9,856	18,480
Combinatorial (C-cells) Modules	19,712	36,960
Embedded Multiply-Accumulate DSP Mathblocks	64	120
Embedded RAM/FIFO Blocks (without EDAC)	64	120
Embedded RAM/FIFO (without EDAC) (k=1,024 bits)	288k	540k
Hardwired Clocks (segmentable)	4	4
Routed Clocks (segmentable)	4	4
I/O Banks	8	8
User I/Os (maximum)	684	840
I/O Registers	2,052	2,520
CG/LG (DSP)* Package Pins	1272	1272
CQ Package Pins	352	352

Note: The body size of the 1272-pin CCGA and LGA packages used on the RTAX4000D/DL FPGAs are slightly larger than the body size of the 1272-pin CCGA and LGA used on the RTAX4000S/SL devices.

I/Os per Package

RTAX-DSP Devices	RTAX2000D	RTAX4000D
CQ352	166	166
CG1272/LG1272	684	840

Note: The user I/Os include clock buffers.

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-dsp

Low-Power, Reprogrammable FPGAs for Space

Radiation-Tolerant (RT) ProASIC®3 FPGAs are the first to offer designers of spaceflight hardware a radiation-tolerant, reprogrammable, nonvolatile logic integration vehicle. They are intended for low-power space applications requiring up to 3,000,000 system gates.

- Ceramic column grid array with Six Sigma™ copper-wrapped lead-tin columns
- Supports single-voltage system operation
- Total ionizing dose: 25 krad to 30 krad with less than 10% propagation delay change at standard test dose rate; up to 40 krad at low-dose rate
- Up to 504 Kbits of true dual-port SRAM
- Live-At-Power-Up (LAPU) level 0 support
- In System Programming (ISP) protected with industry standard on-chip 128-bit advanced encryption
- Standard (AES) decryption via JTAG (IEEE 1532–compliant)
- Screening:
  B Flow: MIL-STD-883B
  E Flow: Microchip Extended Flow

RT ProASIC3 Devices

RT ProASIC3 Devices	RT3PE600L	RT3PE3000L
System Gates	600,000	3,000,000
VersaTiles (D-flip-flops)	13,824	75,264
RAM (k = 1,024 bits)	108k	504k
RAM Blocks (4,608 bits)	24	112
FlashROM (Kbits)	1	1
Secure (AES) ISP	Yes	Yes
Integrated PLL in CCCs	6	6
VersaNet Globals	18	18
I/O Banks	8	8
Maximum User I/Os	270	620
CG/LG Package Pins	484	484,896
CQ Package Pins	256	256

I/Os per Package

RT ProASIC3 Devices	RT3PE600L		RT3PE3000L	
I/O Type	Single-Ended I/Os	Differential I/O Pairs	Single-Ended I/Os	Differential I/O Pairs
CG/LG484	270	135	341	168
CG/LG896	–	–	620	310
CQ256	166	82	166	82

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rt-proasic3

Flight-Proven in Space—Time After Time

RTSX-SU radiation-tolerant FPGAs are enhanced versions of Microchip's commercial SX-A family of devices specifically designed for enhanced radiation performance. Featuring SEU-hardened D-type flip-flops that offer the benefits of Triple Module Redundancy (TMR) without requiring cumbersome user intervention, the RTSX-SU family is a unique product for space applications.

- Very-low power consumption (up to 68 µW at standby)
- 3.3V and 5.0V mixed voltage
- Configurable I/O support for 3.3V/5V PCI, LVTTL, TTL and CMOS
- Secure programming technology protects against reverse engineering and design theft
- 100% circuit resource utilization with 100% pin locking
- Unique in-system diagnostic and verification capability with Silicon Explorer II
- Low-cost prototyping option
- Deterministic, user-controllable timing
- JTAG boundary scan testing in compliance with IEEE Standard 1149.1—dedicated JTAG reset (TRST) pin
- Highly reliable, nonvolatile antifuse technology
- 32,000 to 72,000 ASIC gates (48,000 to 108,000 system gates)
- Up to 360 user-programmable I/Os
- Hermetically-sealed packages for space applications (CQFP, CCGA/CLGA, CCLG)

RTSX-SU Devices

RTSX-SU Devices	RTSX32SU	RTSX72SU
Typical Gates Capacity	32,000	72,000
System Gates Capacity	48,000	108,000
Combinatorial Cells Logic Module	1,800	4,024
SEU-Hardened Register Cells (D-Flip-Flops) Logic Module	1,080	2,012
Maximum Flip-Flops Logic Module	1,980	4,024
Maximum User I/Os Logic Module	227	360
Clocks Logic Module	3	3
Quadrant Clocks Logic Module	0	4
Speed Grades Logic Module	Std., –1	Std., –1
CQ Package Pins	84, 208, 256	208, 256
CG Package Pins		624
CC Package Pins	256	

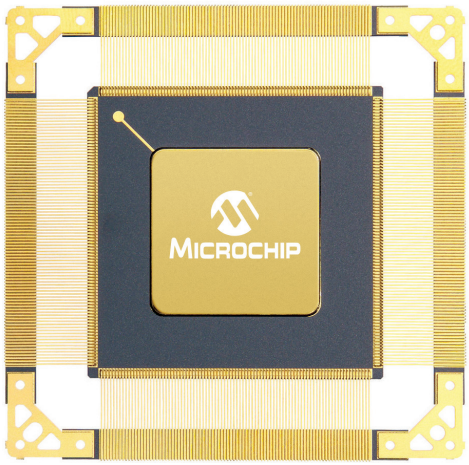
I/Os per Package

RTSX-SU Devices	RTSX32SU	RTSX72SU
CQ84	62	
CQ208	173	170
CQ256	227	212
CC256	202	
CG624	–	360

Note: The user I/Os include clock buffers.

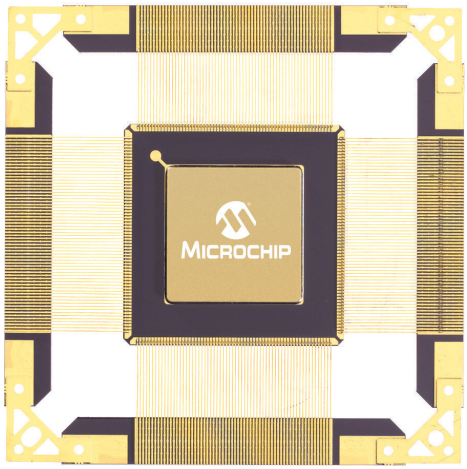
For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtsx-su

FPGA Packages



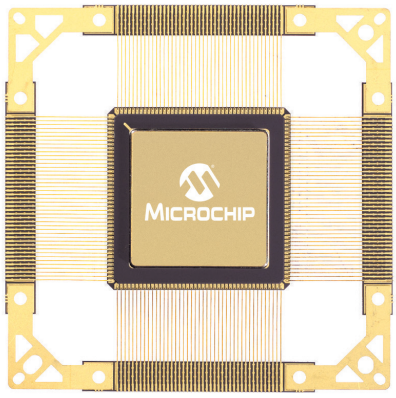
CQ352

b.s. 1.890" x 1.890" (48 mm x 48 mm)
h. RTAX—105 mils (2.67 mm)
h. RTG4—89 mils (2.25 mm)
p. 20 mils (0.50 mm)



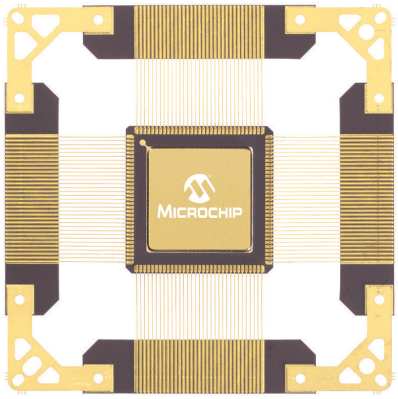
CQ256

b.s. 1.417" x 1.417" (36 mm x 36 mm)
h. 105 mils (2.67 mm)
p. 20 mils (0.50 mm)



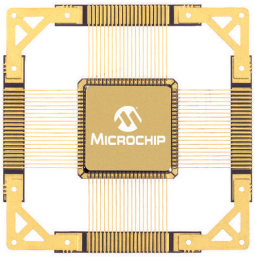
CQ172

b.s. 1.18" x 1.18" (29.972 mm x 29.972 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



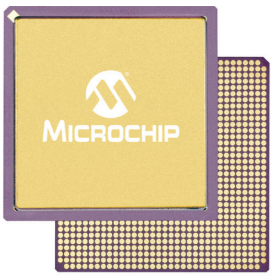
CQ132

b.s. 0.95" x 0.95" (24.13 mm x 24.13 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



CQ84

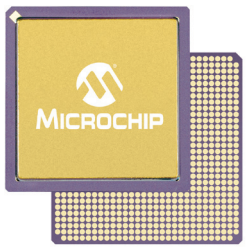
b.s. 0.65" x 0.65" (16.51 mm x 16.51 mm)
h. 90 mils (2.29 mm)
p. 25 mils (0.64 mm)



CG1152/LG1152

RTAX2000S and RTAX2000SL only

b.s. 1.378" x 1.378" (35 mm x 35 mm)
h. CCGA—218 mils (5.535 mm)
h. LGA—129 mils (3.28 mm)
p. 39 mils (1.00 mm)

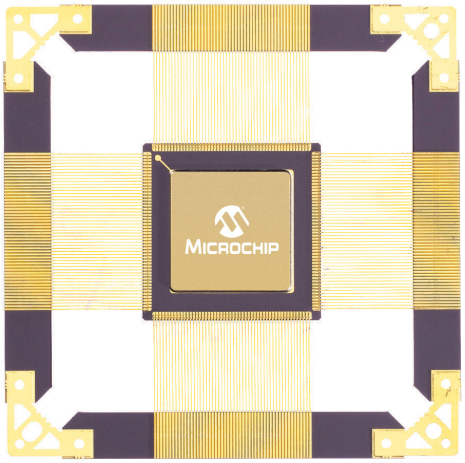


CG896/LG896

b.s. 1.220" x 1.220" (31 mm x 31 mm
h. CCGA—218 mils (5.535 mm)
h. LGA—129 mils (3.28 mm)
p. 39 mils (1.00 mm)

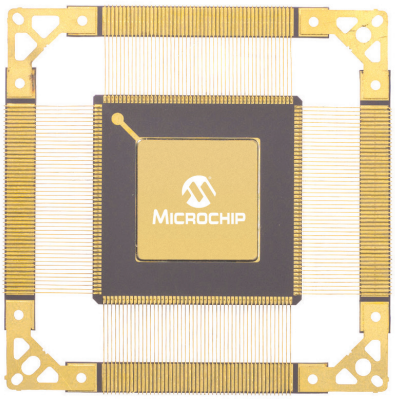
Note: b.s. is nominal package body size excluding leads, h is package thickness, and p is pin/ball pitch.

For more information refer to the Microchip Package Mechanical Drawings document located at www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtax-s-sl#documents



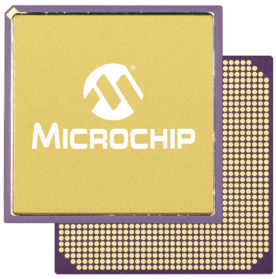
CQ208

b.s. 1.15" x 1.15" (29.21 mm x 29.21 mm)
h. 105 mils (2.67 mm)
p. 20 mils (0.50 mm)



CQ196

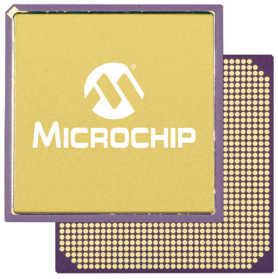
b.s. 1.35" x 1.35" (34.29 mm x 34.29 mm)
h. 105 mils (2.67 mm)
p. 25 mils (0.64 mm)



CB1657/CG1657/LG1657

RT4G150

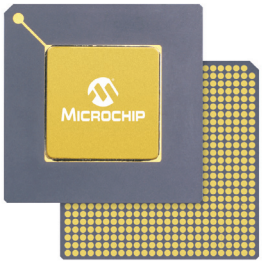
b.s. 1.693" x 1.693" (43 mm x 43 mm)
h. CBGA—156 mils (3.97 mm)
h. CCGA—213 mils (5.42 mm)
h. CLGA—126 mils (3.21 mm)
p. 39 mils (1.00 mm)



CG1272/LG1272

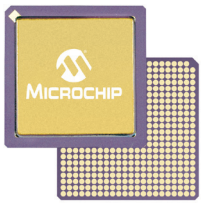
RTAX4000S, RTAX4000SL, and RTAX2000D only

b.s. 1.457" x 1.457" (37 mm x 37 mm)
h. CCGA—218 mils (5.535 mm)
h. CLGA—129 mils (3.28 mm)
h. CLGA—126 mils (3.21 mm)
p. 39 mils (1.00 mm)



CG624/LG624

b.s. 1.27" x 1.27" (32.50 mm x 32.50 mm)
h. CCGA—194 mils (4.94 mm)
h. LGA—90 mils (2.30 mm)
p. 50 mils (1.27 mm)



CG484/LG484

b.s. 0.91" x 0.91" (23.00 mm x 23.00 mm)
h. CCGA—225 mils (5.72 mm)
h. LGA—138 mils (3.51 mm)
p. 7.5 mils (0.19 mm)



CC256

b.s. 0.67" x 0.67" (17 mm x 17 mm)
h. 72 mils (1.847 mm)
p. 7.5 mils (0.19 mm)

Note: b.s. is nominal package body size excluding leads, h is package thickness, and p is pin/ball pitch.

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data

Libero® IDE Should be Used for Designing With Antifuse and Legacy Flash FPGAs

Libero IDE supports:

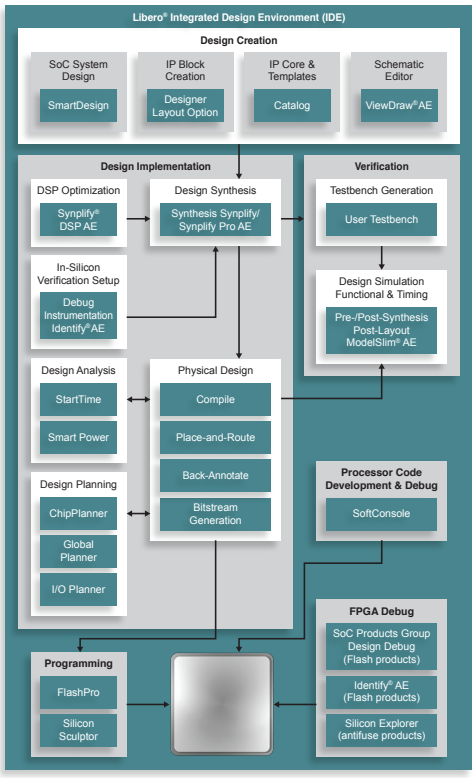
- SX/SX-A (including RTSX/-S/-SU)
- Axcelerator (including RTAX-S, RTAX-DSP)

Microchip system-critical FPGAs are fully supported by Libero Integrated Design Environment (IDE) software. Libero IDE is an integrated design manager that integrates design tools while guiding the user through the design flow, managing all design and log files and passing necessary design data among tools. Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify Pro® AE from Synopsys®, ModelSim® HDL Simulator from Mentor Graphics and design implementation software from Microchip.

Designer software includes sophisticated place-and-route features plus a comprehensive suite of backend support tools for timing constraints, timing and power analysis, I/O attribute and pin assignment, and much more.

Our SmartDesign tool simplifies the use of Microchip's IP in user designs and offers a simple way to build on-chip processors with custom peripherals. Most IP cores are now included by default in Libero IDE as either obfuscated or RTL versions, depending on the license selected.

For embedded designers, we offer SoftConsole Eclipse-based IDE for use with Arm® Cortex®-M1 and Cortex-M3, and Core8051s, as well as evaluation versions from Keil™ and IAR Systems®, full versions are available from the respective suppliers.



FPGA Design Support

Libero® IDE Licenses		Gold	Platinum	Standalone
Device Support	All families	Up to 1,500,000 gates	All devices	All devices
Microchip IP		Libero IP bundle obfuscated and selected RTL IPs	RTL for Libero IP bundle cores	RTL for Libero IP bundle cores
Synthesis	Synplify® Pro ME	✓	✓	–
Simulation	ModelSim® ME	✓	✓	–
Debug	Identify® ME	✓	✓	–
	Microchip Debug	✓	✓	✓
Program File		✓	✓	–

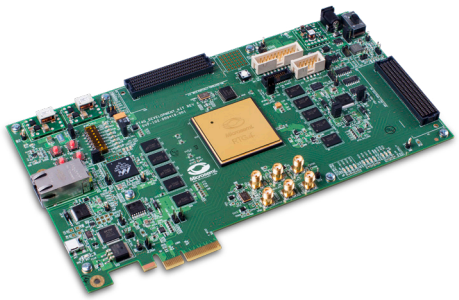
Note: FPGA programming is only supported in Windows® XP Pro, Windows Vista and Windows 7.

Operating System Support

Tool	Libero® IDE	SoftConsole	Keil	IAR	FlashPro	FlashPro USB Driver
Windows® XP Professional	✓	✓	✓	✓	✓	Now (32-bit and 64-bit)
Windows 7 Professional	✓	✓	✓	✓	✓	Now (32-bit and 64-bit)
RHEL 5 (Tikanga)1	✓	–	–	–	–	–
RHEL 6 (Tikanga)2	✓	–	–	–	–	–

For more information, see www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-ide

RTG4 Development Kit



The RTG4 Development Kit provides space customers with an evaluation and development platform for applications such as data transmission, serial connectivity, bus interface and high-speed designs using the latest radiation-tolerant, high-density, high-performance FPGA family, RTG4. The development board features an RT4G150 device offering more than 150,000 logic elements in a ceramic package with 1,657 pins.

The RTG4 Development Kit board includes the following features:

- Two 1 GB DDR3 synchronous dynamic random access memory (SDRAM)
- 2 GB SPI Flash memory
- PCI Express Gen1 ×1 interface
- PCIe ×4 edge connector
- One pair of SMA connectors for testing of the full-duplex SERDES channel
- Two FMC connectors with HPC/LPC pinout for expansion
- RJ45 interface for 10/100/1000 Ethernet
- USB micro-AB connector
- Headers for SPI, GPIOs
- FTDI programmer interface to program the external SPI Flash
- JTAG programming interface
- RVI header for application programming and debug
- Embedded FlashPro5 programmer
- Flashpro programming header available if external programmer is used
- Embedded Trace Macro (ETM) cell header for debug
- Dual In-Line Package (DIP) switches for user application
- Push-button switches and LEDs for demo purposes
- Current measurement test points

For more information, see www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit

RTG4 Design Software—Libero SoC

Microchip's Libero System-on-Chip (SoC) Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microchip's RTG4 FPGAs. The suite integrates industry-standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.

Features

- Design entry—multiple approaches using SmartDesign, HDL, or embedded design flows
- Simulation—functional, gate-level, and timing verification using Mentor Graphics ModelSim ME
- Synthesis—design optimization for power and performance using Synopsys Synplify Pro ME and Synphony Model Compiler ME
- Place and route—advanced, incremental, power-driven, and multi-pass layout options
- Power analysis—in-depth visualization of power consumption for each individual design element using SmartPower
- Timing analysis—support for multiple constraint scenarios to optimize timing using SmartTime
- Programming—complete solution with industry's first Secure Production Programming Solution (SPPS)
- Debug—best-in-class debug solution with SmartDebug and Synopsys Identify ME

Easy to Learn

- Intuitive design flow
- GUI wizards guiding through the design process

Easy to Adopt

- Rich IP library of DirectCores and CompanionCores
- Availability of complete reference designs and development kits

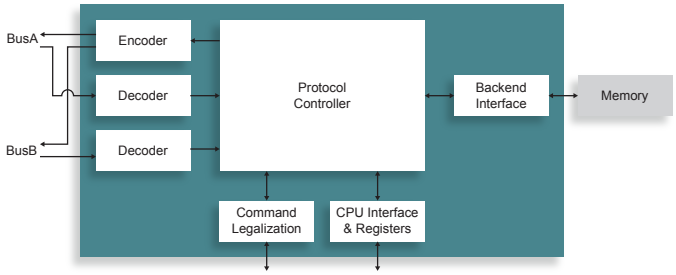
For more information, see www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc

Intellectual Property Cores for System Critical FPGAs

Microchip has more than 180 Intellectual Property (IP) products designed and optimized to support communications, consumer, military, industrial, automotive and aerospace markets. Microchip IP solutions streamline designs, enable faster time-to-market, and minimize design costs and risk. Microchip IP cores are accessible through the Libero design suite of development tools through the SmartDesign IP design interface. Many cores feature firmware drivers accessible through the firmware catalog tool. Integrated solutions are also available, featuring IP and highlighting the advantages of Microchip's intrinsically low-power FPGAs.

MIL-STD-1553B IP Cores

MIL-STD-1553 is a command/response, dual-redundant, time-multiplexed serial data bus used in severe environments. Microchip Core1553 IP cores provide robust, fully tested MIL-STD-1553A and B implementations that are compatible with legacy 1553 solutions. We provide everything needed to incorporate one or more 1553B cores into a system design. Core1553BRM, Core1553BRT, Core1553BRT-EBR, and Core1553BBC are available.



Core1553BRM

- Compliant to MIL-STD-1553A and B
- Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT)
- Simultaneous RT/MT operation
- 12, 16, 20, or 24 MHz clock operation
- Built-in test capability
- Advanced RT functions
- Sophisticated BC reduces host overhead
- Interfaces to standard transceivers
- Redundancy for severe environments
- Low-power operation

Digital Signal Processing IP Cores

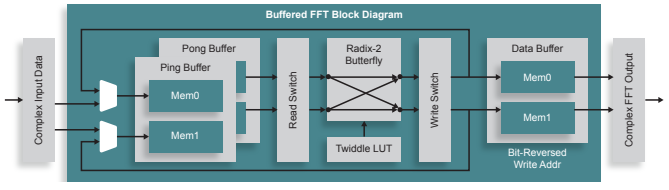
Microchip Digital Signal Processing (DSP) cores deliver digital filtering and signal processing capabilities. Cores taking advantage of on-chip multiplier blocks in Microchip's RTAX-DSP and new RTG4 devices offer outstanding performance in spaceflight applications.

CoreFFT

- Highly parameterizable DirectCore RTL generator optimized for the RTAX-DSP and RTG4 families support forward and inverse complex FFT
- Transforms sizes from 32 to 8,192 points
- 8-to 32-bits I/O real and imaginary data and twiddle coefficients
- Two's complement I/O data
- Bit-reversed or natural output order
- Selection of unconditional or conditional block floating point scaling
- Embedded RAM-block-based twiddle LUT
- Built-in memory buffers with optional extensive or minimal memory buffering configurations
- Handshake signals to facilitate easy interface to user circuitry

CoreFIR

- Highly parameterizable DirectCore RTL generator optimized for the RTAX-DSP and RTG4 families implement a range of filter types, including single rate fully enumerated (parallel), single-rate folded (semi-parallel) filter and multi-rate polyphase interpolation FIR filter
- Performance up to 124 MHz
- Supports up to 1,024 FIR filter taps
- Run-time reloadable coefficients, multiple coefficient sets, or fixed coefficients
- 2-bit to 18-bit input data and coefficient precision
- Signed or unsigned data and coefficients
- Full precision output
- Coefficient symmetry optimization (on the fully enumerated filters)



For more information and additional IP cores, see www.microsemi.com/products/fpga-soc/design-resources/ip-cores

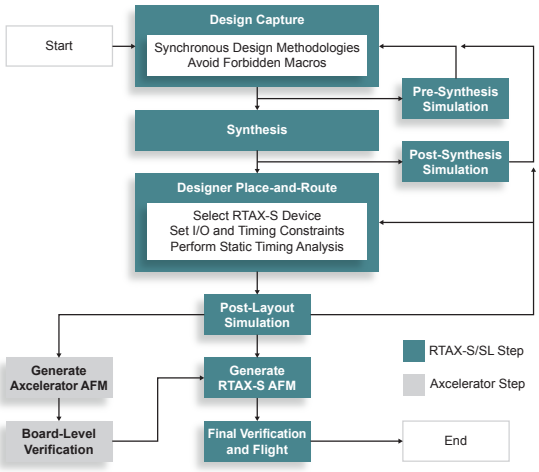
With the introduction of Microchip's RTAX-S/SL devices, you now have access to the most powerful FPGAs available for aerospace and radiation-intensive applications. Prototype verification is an important step in system integration where accurate behavioral simulation and static timing analysis are crucial. Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, we have developed various prototyping options for RTAX-S/SL for early design development and functional verification.

Prototyping with Axcelerator Units

The prototyping solution using the commercial Axcelerator devices consists of two parts.

- A well-documented design flow that allows the customer to target an RTAX-S/SL design to the equivalent commercial Axcelerator device
- A set of extender circuit boards that map the commercial device package to the appropriate RTAX-S/SL package footprint

This methodology provides the user with a cost-effective solution while maintaining the short time-to-market associated with Microchip FPGAs.



Prototyping with RTAX-S/SL/DSP or RTSX-SU PROTO Units

The RTAX-S/SL/DSP or RTSX-SU PROTO units offer a prototyping solution that can be used for final timing verification of the flight design. The RTAX-S/SL/DSP or RTSX-SU PROTO prototype units have the same timing attributes as the RTAX-S/SL/DSP or RTSX-SU flight units. Prototype units are offered in non-hermetic ceramic packages. The prototype units include PROTO in their part number, and PROTO is marked on devices to indicate that they are not intended for space flight. They also are not intended for applications that require the quality of spaceflight units, such as qualification of spaceflight hardware. RT-PROTO units offer no guarantee of hermeticity, and no MIL-STD-883B processing. At a minimum, you should plan on using class B level devices for all qualification activities. The RT-PROTO units are electrically tested in a manner to guarantee their performance over the full military temperature range. The RT-PROTO units will also be offered in –1 or standard speed grades, so as to enable customers to validate the timing attributes of their space designs using actual flight silicon.

RTAX-S/SL Prototyping with Flash Devices

Aldec's RTAX-S/SL prototyping solution allows customers to take advantage of Flash-based reprogrammable ProASIC3 devices. Aldec provides software that remaps antifuse primitives to Flash, which reduces design time and cost. In addition, the hardware adapter is footprint compatible with RTAX-S/SL; therefore, you do not need to redesign a new board for prototyping.

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/prototyping-solutions

Prototyping With RTG4 PROTO Units



RTG4 PROTO FPGAs offer a development and prototyping solution for development and final timing validation of the flight design. As the RTG4 PROTO units use the same reprogrammable Flash technology as the flight units, the PROTO devices can be reprogrammed many times without removing them from the development board. The RTG4 PROTO prototype units have the same timing attributes as the RTG4 flight units, including support for the same speed grades as the flight parts. The RT-PROTO units are electrically tested in a manner to guarantee their performance over the full military temperature range. Prototype units are offered in non-hermetic, ceramic packages. The prototype units include **PROTO** in their part number, and **PROTO** is marked on devices to indicate that they are not intended for space flight. They are also not intended for applications that require the quality of spaceflight units, such as qualification of spaceflight hardware. RT-PROTO units offer no guarantee of hermeticity, and no Mil-STD-883 class B processing. At a minimum, users should plan on using class B devices for all qualification activities.

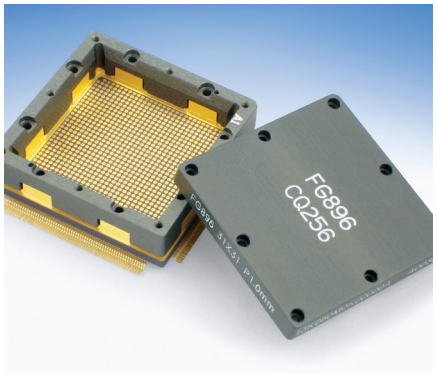
Package Prototyping Solutions

Microchip has developed multiple low-cost prototyping solutions for RTAX-S/SL devices that ultimately are packaged in CQFP or CCGA for the production system. These solutions utilize the Axcelerator family Fine Pitch Ball Grid Array (FBGA) or Ceramic Land Grid Array (CLGA) packages as prototyping vehicles:

- CQFP to FBGA adapter socket
- CQFP to CLGA adapter socket
- CCGA to FBGA adapter socket
- CCGA to CLGA adapter socket

The CQFP to FBGA adapter sockets have an FBGA configuration on the top and a CQFP configuration on the bottom. The adapter sockets enable customers to use a commercial Axcelerator FG package during prototyping, then switch to an equivalent CQ256 or CQ352 package for production.

Adapter Socket	Ordering Part Number	Prototyped and Prototype Device
CQ352 to FG484	SK-AX250-CQ352RTFG484S	For prototyping RTAX250S/ L-CQ352 or AX250-CQ352 using AX250-FG484 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CQ352-KITBTM	For prototyping RTAX1000S/ L-CQ352 or AX1000-CQ352 using AX1000-FG896 package
CQ352 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CQ352-KITBTM	For prototyping RTAX2000S/ L-CQ352 or AX2000-CQ352 using AX2000-FG896 package
CQ256 to FG896	SH-AX2-CQ256-KITTOP and SK-AX2-CQ256-KITBTM	For prototyping RTAX2000S/ L-CQ352 or AX2000-CQ256 using AX2000-FG896 package
CG624 to FG484	SK-SX72-CG624RTFG484	For prototyping RTSX72SU-CG624 or A54SX72A-CG624 using A54SX72A-FG484 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX1-CG624-KITBTM	For prototyping RTAX1000S-CG624, RTAX1000SL-CG624, or AX1000-CG624 using AX1000-FG896 package
CG624 to FG896	SK-AX1-AX2-KITTOP and SK-AX2-CG624-KITBTM	For prototyping RTAX2000S-CG624, RTAX2000SL-CG624, or AX2000-CG624 using AX2000-FG896 package



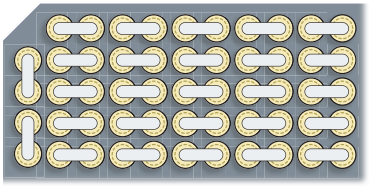
RTAX2000S CQ256 to FG896 Ceramic Adapter, Top and Bottom

For more information, see www.microsemi.com/products/fpga-soc/radtolerant-fpgas/prototyping-solutions

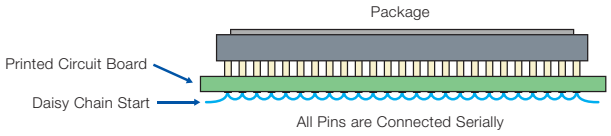
Daisy-chained Packages

To facilitate the qualification of a target FPGA device socket and board assembly practices without using costly flight-quality parts, Microchip offers certain Ceramic Column Grid Array (CCGA) and Ceramic Land Grid Array (CLGA) packages with adjacent pairs of pins tied together. By assembling these packages onto a qualification PC board that is laid out with adjacent pairs of solder pads tied together but offset by one pin as compared to the package, a single signal can be fed into one pin of the package and routed into and out of the entire package in a serial daisy chain fashion so all pins of the package are used. This is useful for performing continuity and impedance tests to validate board assembly techniques with surface-mount grid array packages. Microchip's daisy chain packages feature metal routing tracks between adjacent pairs of package pins, internal to the package. For package qualification, an unbonded silicon die is included in the package.

Microchip Part Number	Mechanical Package
LG624 DAISY CHAIN-1	624-pin CLGA
LG1152 DAISY CHAIN	1152-pin CLGA
LG1272 DAISY CHAIN	1272-pin CLGA
LG1657 DAISY CHAIN	1657-pin CLGA
CG484 DAISY CHAIN	484-pin CCGA
CG624 DAISY CHAIN SIX	624-pin CCGA
CG896 DAISY CHAIN	896-pin CCGA
CG1152 DAISY CHAIN	1152-pin CCGA
CG1272 DAISY CHAIN	1272-pin CCGA
CG1657 DAISY CHAIN	1657-pin CCGA



Partial View of 624 CGA with Adjacent Pin Pairs Tied Together



Device Programming

Silicon Sculptor 4

The Silicon Sculptor 4 programmer, which supports both antifuse and Flash FPGAs, delivers high data throughput and promotes ease-of-use, while lowering the overall cost of ownership. The Silicon Sculptor 4 programmer includes a high-speed USB 2.0 interface that enables customers to connect multiple programmers to a single PC. This enables an easily expandable, low to medium volume production programming system to be dynamically assembled. Through the use of universal Microchip socket adapters, the Silicon Sculptor 4 programs Microchip packages, including PLCC, PQFP, VQFP, TQFP, QFN, PBGA, FBGA, CSP, CPGA, CQFP, CCGA and CLGA.

FlashPro4 and FlashPro5

The FlashPro4 and FlashPro5 programmers for Flash FPGAs utilize a JTAG interface, where a single JTAG chain can be used for multiple Flash devices on a JTAG chain. In-system programming using the JTAG port adds the flexibility of field upgrades or post-assembly production-line characterization. The elimination of expensive sockets on the board results in significantly-reduced production costs.

All FlashPro programmers use JEDEC-standard STAPL files, meaning there are no algorithms built into the software. The FlashPro software and user interface support FlashPro4, and FlashPro5 programmers, eliminating the need to learn new software to switch from one hardware programmer to another.

For more information, see www.microsemi.com/products/fpga-soc/design-resources/programming-debug

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Microchip is committed to supporting its customers in developing products faster and more efficiently. We maintain a worldwide network of field applications engineers and technical support ready to provide product and system assistance. For more information, please visit www.microchip.com:

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If additional training interests you, Microchip offers several resources including in-depth technical training and reference material, self-paced tutorials and significant online resources.

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China - Hangzhou
Tel: 86-571-8792-8115

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Tel: 852-2943-5100

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Tel: 86-25-8473-2460

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