

Four Output Ultra-Low Additive Phase Noise PCIe, Gen 1 to 6, and UPI/QPI Fanout Buffer

Features

- One Differential Input which Accepts Any Differential Format
- Four Differential HCSL Outputs
- Ultra-Low Additive Jitter: 33 fs (in 12 kHz to 20 MHz Integration Band at 491.52 MHz Clock Frequency)
- Supports Clock Frequencies from 0 MHz to 600 MHz
- Supports 2.5V or 3.3V Power Supplies for HCSL Outputs
- Embedded Low Drop Out (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output to Output Skew of 50 ps
- Individual Output Enable Pin for Each Differential Pair
- Transfers Spread-Spectrum without Attenuation

Applications

- PCI Express Generation 1/2/3/4/5/6 Clock Distribution
- UPI/QPI Clock Distribution
- Low Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- High-Performance Microprocessor Clock Distribution
- Test Equipment

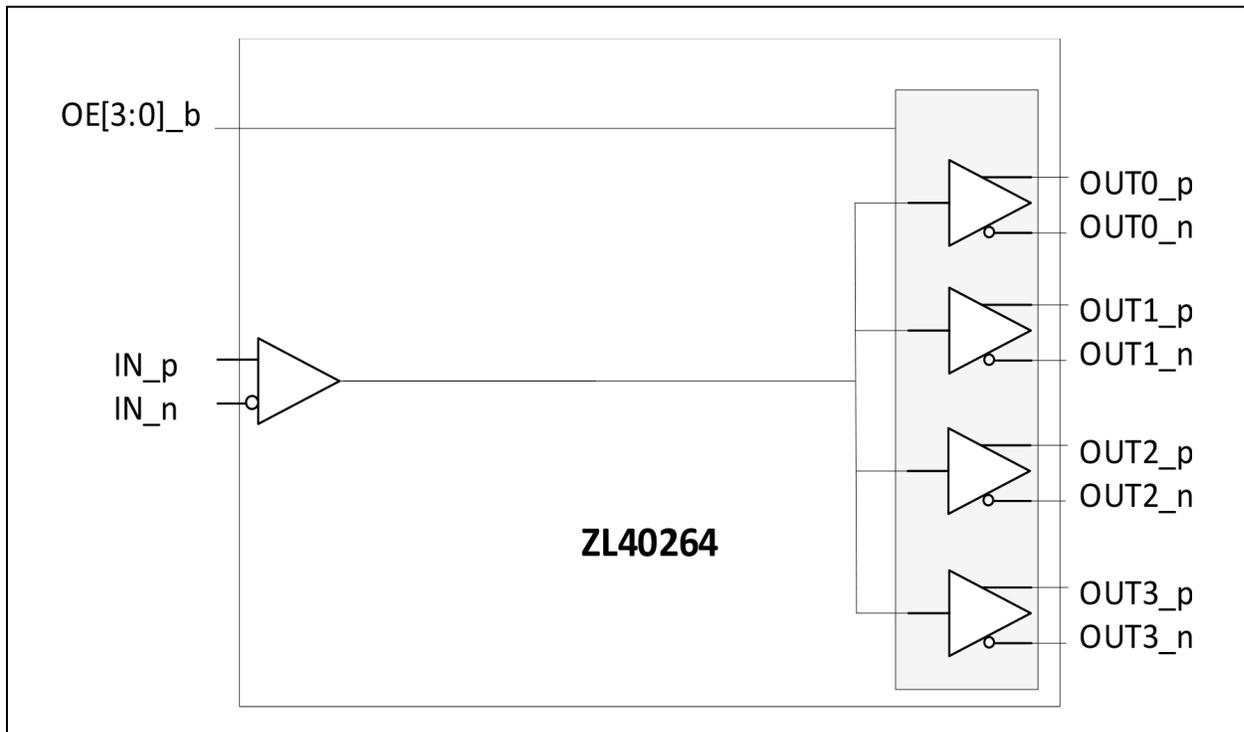


FIGURE 0-1: Functional Block Diagram.

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

TABLE OF CONTENTS

1.0 “Pin Description And Configuration”	6
1.1 “Pin Descriptions”	7
2.0 “Functional Description”	9
2.1 “Clock Inputs”	9
2.2 “Clock Outputs”	11
2.3 “Termination of Unused Inputs and Outputs”	12
2.4 “Power Consumption”	12
2.5 “Power Supply Filtering”	12
2.6 “Power Supplies and Power-up Sequence”	13
2.7 “Device Control”	13
2.8 “Typical phase noise performance”	13
3.0 “AC and DC Electrical Characteristics”	17
4.0 “Package Outline”	27
Appendix A: “Data Sheet Revision History”	32
“Product Identification System”	34
“Worldwide Sales and Service”	36

List of Figures

FIGURE 0-1: “Functional Block Diagram.”	1
FIGURE 1-1: “20-Lead 4 mm x 4 mm VQFN Pin Diagram.”	6
FIGURE 2-1: “Input driven by source terminated HCSL.”	9
FIGURE 2-2: “Input driven by receiver terminated HCSL.”	10
FIGURE 2-3: “Input driven by AC-coupled LVPECL output.”	10
FIGURE 2-4: “Input driven by AC-coupled LVDS.”	10
FIGURE 2-5: “Input driven by a single-ended output.”	11
FIGURE 2-6: “Source-terminated HCSL.”	11
FIGURE 2-7: “Receiver-terminated HCSL.”	11
FIGURE 2-8: “Power Supply Filtering.”	13
FIGURE 2-9: “100 MHz HCSL Phase Noise.”	13
FIGURE 2-10: “133 MHz HCSL Phase Noise.”	14
FIGURE 2-11: “400 MHz HCSL Phase Noise.”	14
FIGURE 2-12: “491.52 MHz HCSL Phase Noise.”	15
FIGURE 3-1: “Single-Ended Measurement Points for Absolute Cross Point and Swing.”	24
FIGURE 3-2: “Single-Ended Measurement Points for Delta Cross Point.”	24
FIGURE 3-3: “Single-Ended Measurement Points for Rise and Fall Time Matching.”	24
FIGURE 3-4: “Differential Measurement Points for Rise and Fall Time.”	25
FIGURE 3-5: “Differential Measurement Points for Ringback.”	25
FIGURE 3-6: “PCIe Test Circuit.”	25
4.1 “Package Marking Information”	27
“20-Lead 4 mm x 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern”	28

List of Tables

TABLE 1-1: “Pin Description”	7
TABLE 3-1: “Absolute Maximum Ratings”	17
TABLE 3-2: “Recommended Operating Ratings”	17
TABLE 3-3: “Current Consumption”	17
TABLE 3-4: “Input Characteristics”	18
TABLE 3-5: “Power Supply Rejection Ratio for VDD = VDDO = 3.3V”	19
TABLE 3-6: “Power Supply Rejection Ratio for VDD = VDDO = 2.5V”	19
TABLE 3-7: “HCSL Outputs for VDDO = 3.3V”	19
TABLE 3-8: “HCSL (PCIe) Jitter Performance for VDDO = 3.3V”	20
TABLE 3-9: “HCSL Outputs for VDDO = 2.5V”	21
TABLE 3-10: “HCSL (PCIe) Jitter Performance for VDDO = 2.5V”	23
TABLE 3-11: “4 mm × 4 mm VQFN Package Thermal Properties”	26
TABLE 3-12: “HCSL Output Phase Noise with 25 MHz XTAL”	26
TABLE A-1: “Revision History”	32

ZL40264

1.0 PIN DESCRIPTION AND CONFIGURATION

The device is packaged in a 4 mm × 4 mm 20-lead VQFN with 2.125 mm exposed pad.

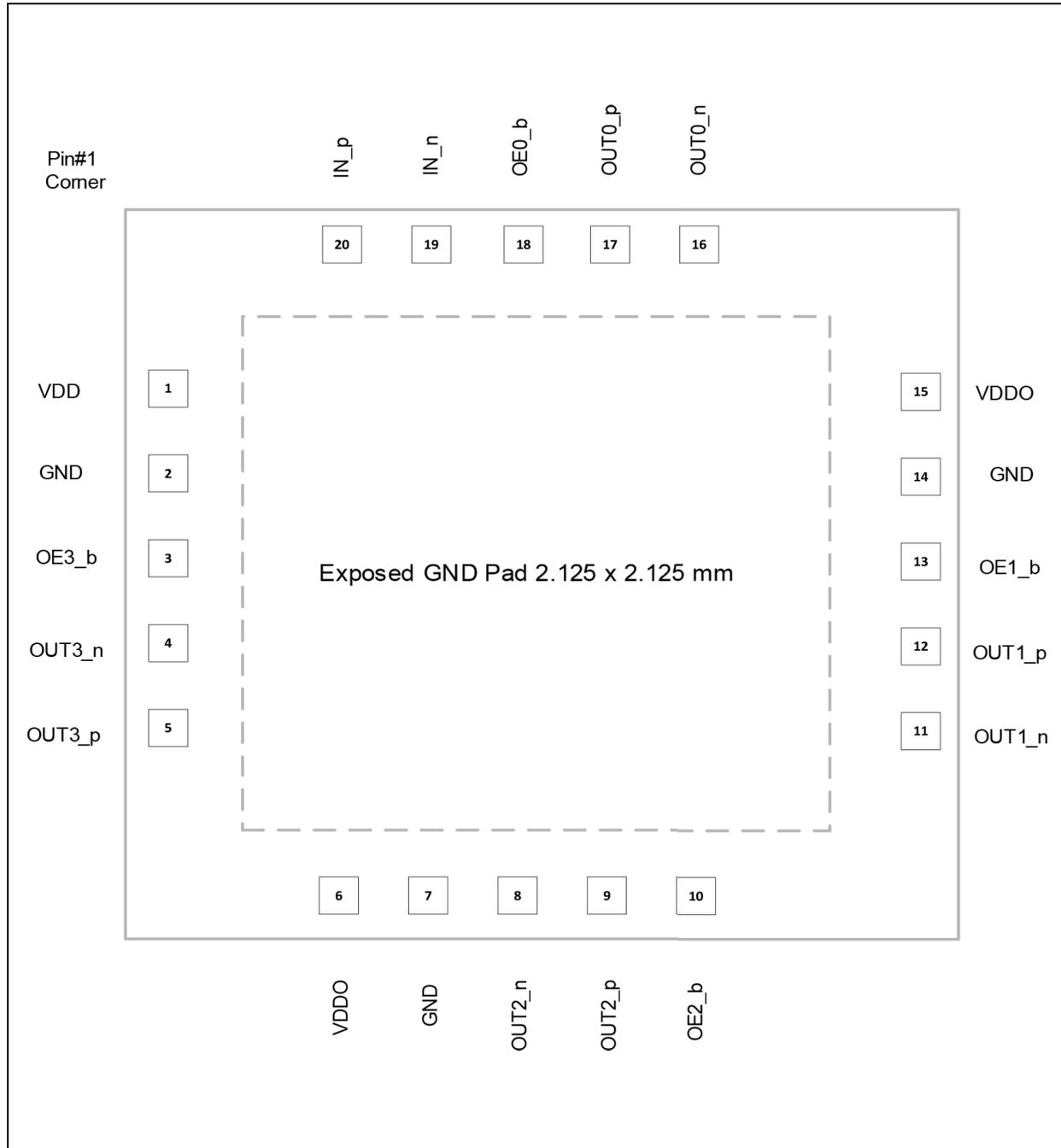


FIGURE 1-1: 20-Lead 4 mm x 4 mm VQFN Pin Diagram.

1.1 Pin Descriptions

All device inputs and outputs are HCSL unless described otherwise.

The I/O column uses the following symbols: I – input, IPU – input with 300 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, I_{APU} – input with 31 kΩ internal pull-up resistor, I_{APD} – input with 30 kΩ internal pull-down resistor, I_{APU/APD} – input biased to VDD/2 with 60 kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, I/O – Input/Output pin, NC – No connect pin, P – power supply pin.

TABLE 1-1: PIN DESCRIPTION

Pin Number	Pin Name	Type	Description	
Input Reference				
20	IN0_p	I _{APD} I _{APU/APD}	Input Differential or Single Ended Reference Input frequency range 0 Hz to 600 MHz. Non-inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60 kΩ internal resistors (30 kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).	
19	IN0_n			
Output Clocks				
17	OUT0_p	O	Ultra-Low Additive Jitter Differential HCSL Outputs 0 to 1 Output frequency range 0 MHz to 600 MHz.	
16	OUT0_n			
12	OUT1_p			
11	OUT1_n			
9	OUT2_p			
8	OUT2_n			
5	OUT3_p			
4	OUT3_n			
Control				
18	OE0_b	I _{PD}	Output Enable. Logic level on these pins enables/disables corresponding outputs.	
13	OE1_b			
10	OE2_b		OEn_b	OUTn_p/n
3	OE3_b		0	Active
			1	High-Z (outputs p/n will be low/low because of 50 Ω shunt resistors—see recommended output termination)
Power and Ground				
1	VDD	P	Positive Supply Voltage. Connect to 3.3V or 2.5V supply.	
6	VDDO	P	Positive Supply Voltage for Differential Outputs. Connect 3.3V or 2.5V power supply. VDDO does not have to be connected to the same voltage level as VDD.	
15				
2	GND	P	Ground. Connect to the ground.	
7				
14				
E-Pad				

ZL40264

NOTES:

2.0 FUNCTIONAL DESCRIPTION

The ZL40264 is an ultra-low additive jitter, low power 1 to 4 HCSL fanout buffer.

The device operates from 2.5V±5% or 3.3V±5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

2.1 Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40264 inputs.

Figure 2-1 and Figure 2-2 show how to terminate the input when driven from an HCSL driver.

The input buffer in ZL40264 is a native HCSL receiver so other differential formats need to be AC coupled as shown in Figure 2-3 and Figure 2-4 for LVPECL and LVDS signals respectively.

The resistors R1, R2, R3, and R4 in Figure 2-3 are used for biasing, termination and hysteresis. The resistor pairs (R1, R2) and (R3, R4) are different to add 20 mV to 30 mV of hysteresis. The hysteresis prevents the device from generating random transitions when input is not driven. If the input is driven all the time with a clock, then pairs (R1, R2) and (R2, R4) can be identical. That is, R3 = R1 and R4 = R2.

The resistors R1, R2, R3, and R4 in Figure 2-4 are used for biasing and hysteresis. Same as above, the hysteresis prevents the device from generating random transitions when input is not driven. If the input is driven all the time with a clock, then pairs (R1, R2) and (R2, R4) can be identical. That is, R3 = R1 and R4 = R2. The 100Ω termination resistor is placed before AC coupling capacitors, because some LVDS drivers need a DC path between p and n outputs. If the LVDS driver does not need the DC path, the 100Ω resistor can be placed after the AC coupling capacitors.

Figure 2-5 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance.

If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 3-4). The source resistors of $R_S = 270\Omega$ could be used for standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of $(3.3V/2) \times (1/(270\Omega + 50\Omega)) = 5.16$ mA.

For optimum performance, both differential input pins ($_p$ and $_n$) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

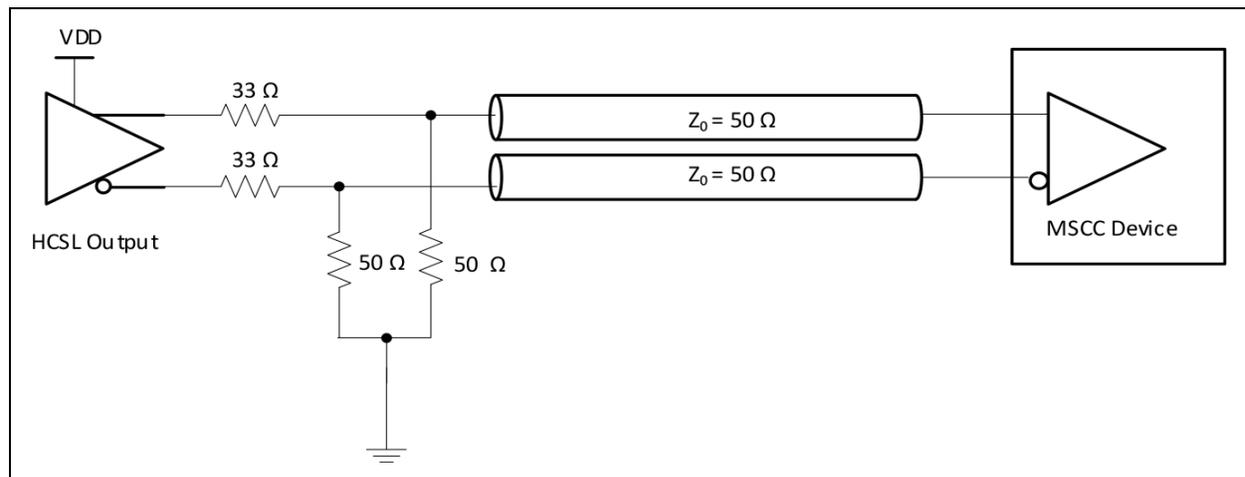


FIGURE 2-1: Input driven by source terminated HCSL.

ZL40264

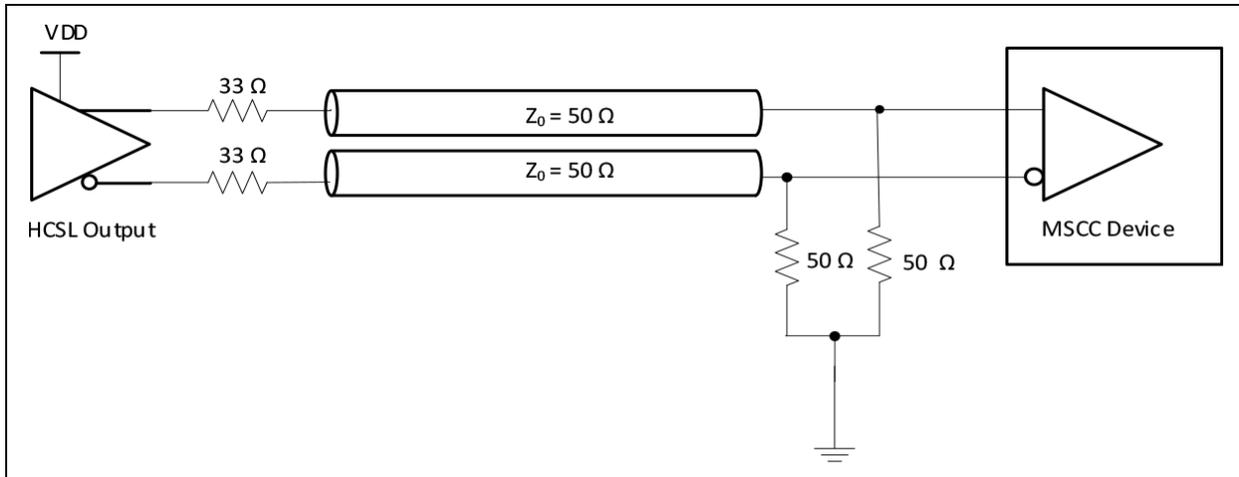


FIGURE 2-2: Input driven by receiver terminated HCSL.

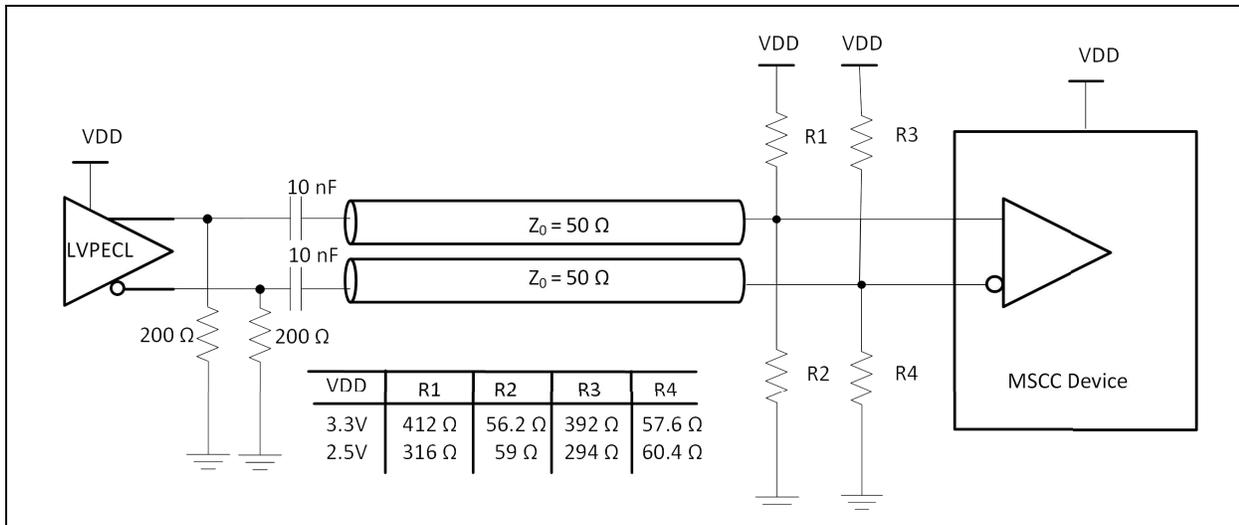


FIGURE 2-3: Input driven by AC-coupled LVPECL output.

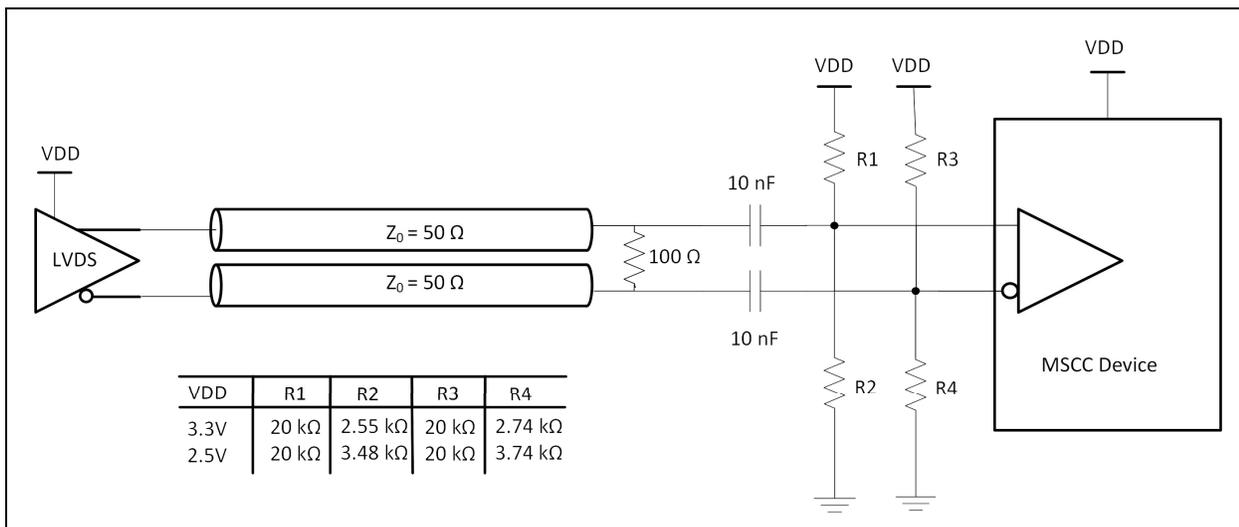


FIGURE 2-4: Input driven by AC-coupled LVDS.

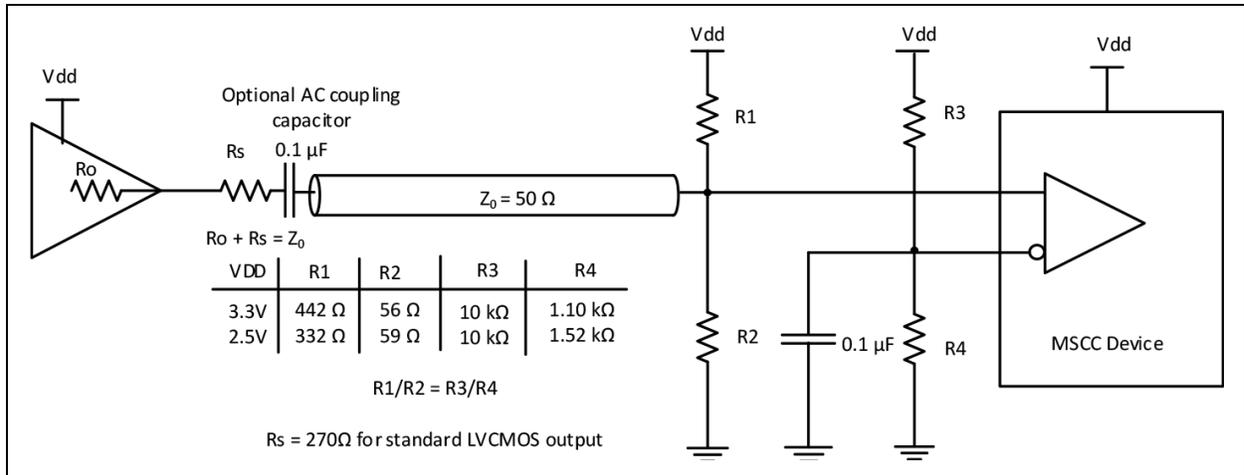


FIGURE 2-5: Input driven by a single-ended output.

2.2 Clock Outputs

Differential HCSL outputs should be terminated as shown in [Figure 2-6](#) or [Figure 2-7](#).

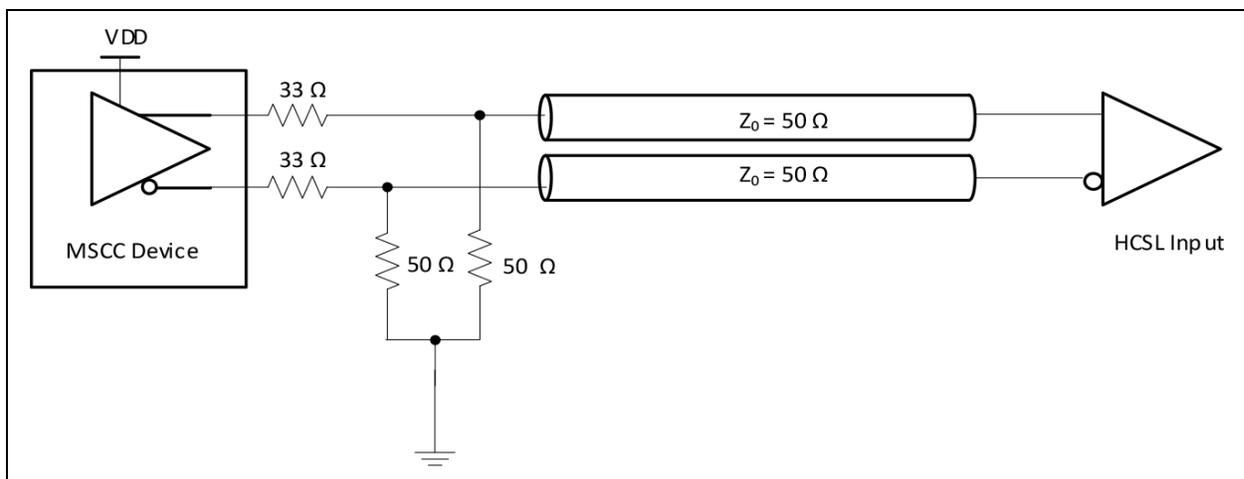


FIGURE 2-6: Source-terminated HCSL.

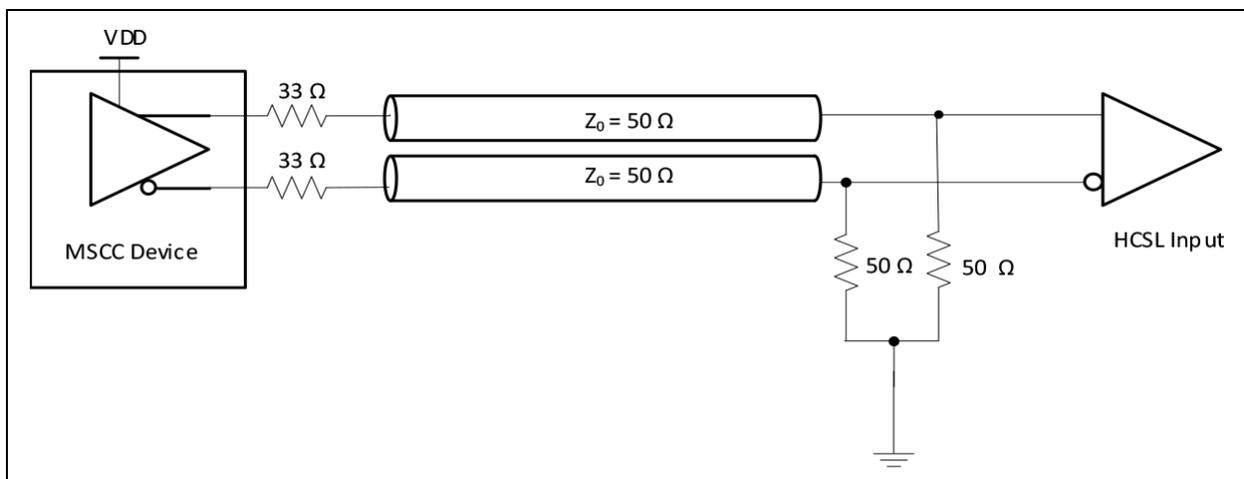


FIGURE 2-7: Receiver-terminated HCSL.

ZL40264

2.3 Termination of Unused Inputs and Outputs

Unused outputs should be left unconnected.

2.4 Power Consumption

The device total power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_C + P_{O_DIFF}$$

Where:

$P_S = V_{DD} \times I_S$	Core power consumed by the input buffer. The static current (I_S) is specified in Table 3-3 .
$P_C = V_{DDO} \times I_{DD_CM}$	Common output power shared among four outputs. The current I_{DD_CM} is specified in Table 3-3 .
$P_{O_DIF} = V_{DDO} \times I_{DD_HCSL} \times N$	Output power where output current per output (I_{DD_HCSL}) is specified in Table 3-3 . N is number of enabled outputs.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption:

EQUATION 2-2:

$$P_D = P_T - N \times P_{HCSL}$$

Where:

$P_{HCSL} = (V_{SW} / 50\Omega)^2 \times (50\Omega + 33\Omega)$	V_{SW} is voltage swing of HCSL output. 50Ω is termination resistance and 33Ω is series resistance of the HCSL output.
---	--

2.5 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1 μF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board, each power supply could optionally be further insulated with low resistance ferrite bead with 10 μF and 1 μF capacitors. [Figure 2-8](#) shows the standard and optional decoupling method.

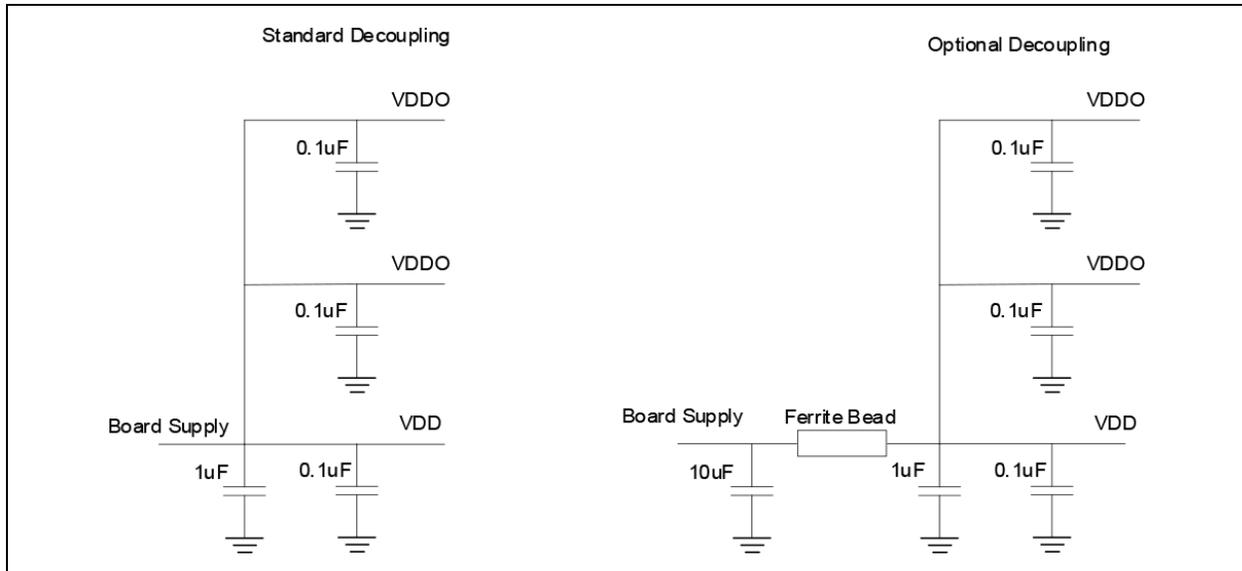


FIGURE 2-8: Power Supply Filtering.

2.6 Power Supplies and Power-up Sequence

The device has two different power supplies: VDD and VDDO which should always be connected to the same voltage supply. Voltages supported by each of these power supplies are specified in [Table 3-2](#).

VDD and VDDO should always be turned on and off at the same time.

2.7 Device Control

ZL40264 outputs are controlled via OE[3:0]_b pins. When an OE_b pin is low the corresponding outputs will be active and when this pin is high the output will be high-Z. When the output driver is in high-Z mode, the output pins will be pulled low via external 50Ω HCSL termination resistors.

2.8 Typical phase noise performance

The following plots show typical phase noise performance for 100 MHz, 133 MHz, 400 MHz, and 491.52 MHz clocks respectively.

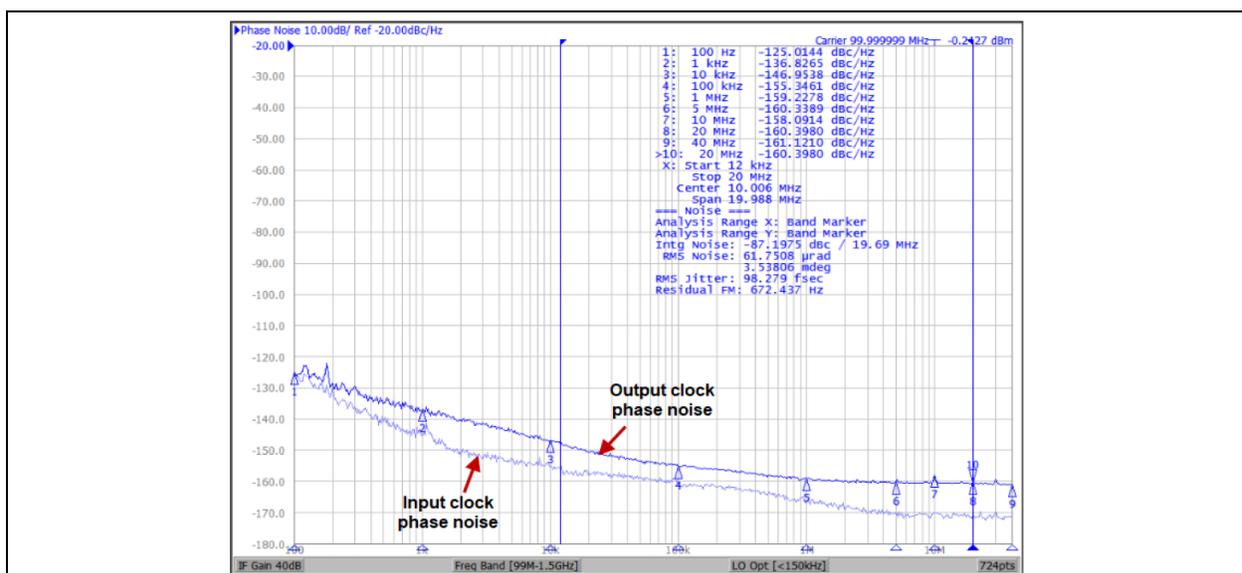


FIGURE 2-9: 100 MHz HCSL Phase Noise.

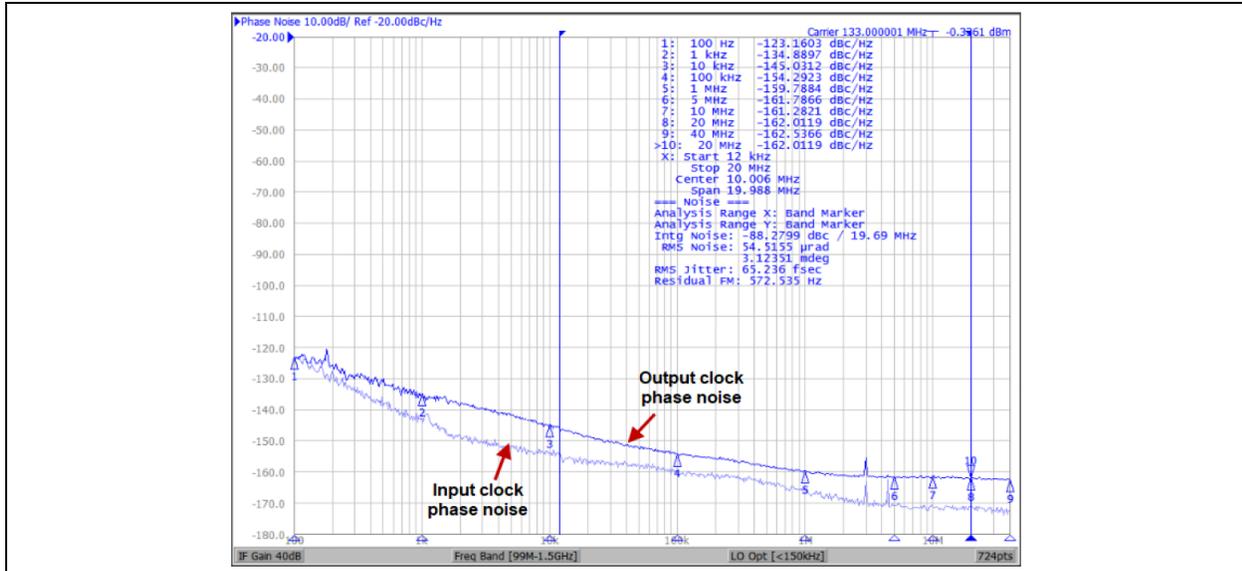


FIGURE 2-10: 133 MHz HCSL Phase Noise.

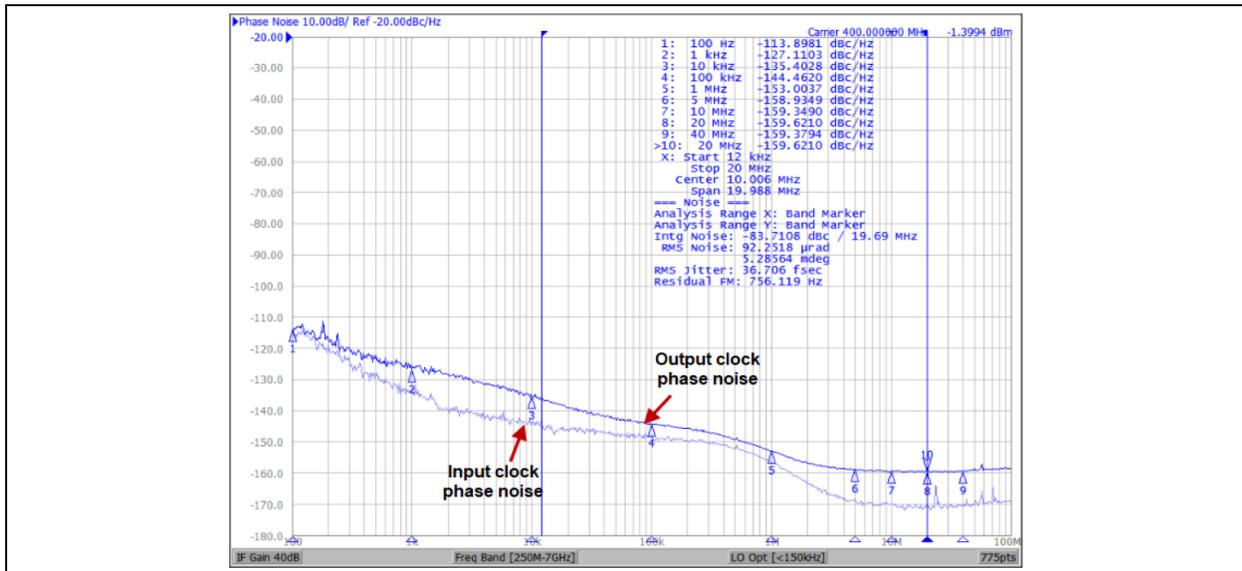


FIGURE 2-11: 400 MHz HCSL Phase Noise.

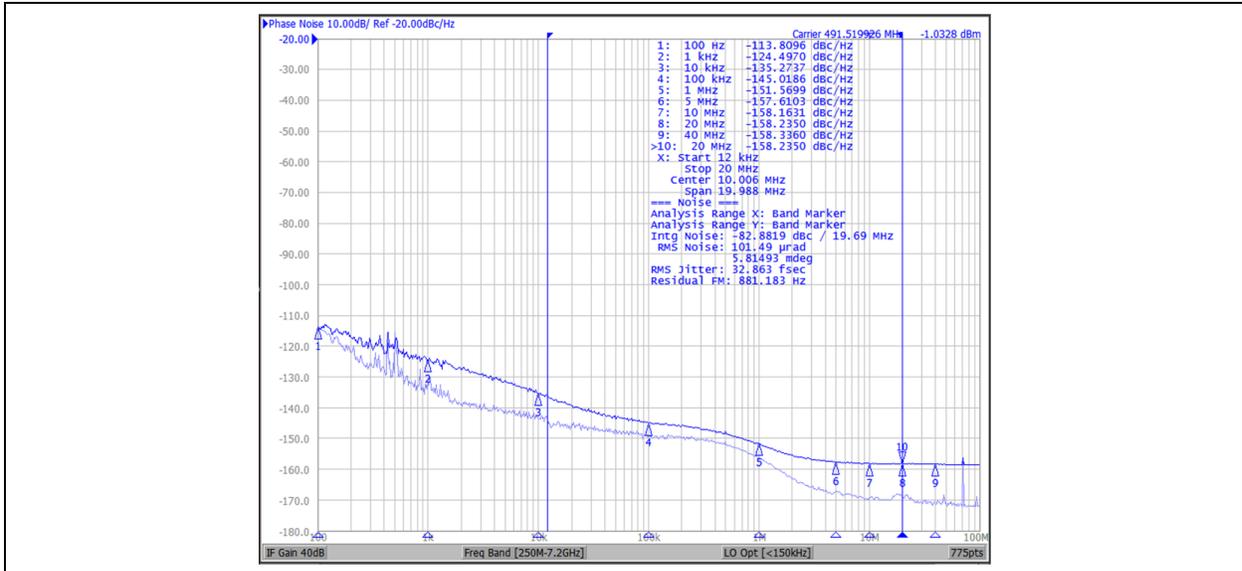


FIGURE 2-12: 491.52 MHz HCSL Phase Noise.

ZL40264

NOTES:

3.0 AC AND DC ELECTRICAL CHARACTERISTICS

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

(Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	-0.5	4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	-0.5	3.5	V
Storage Temperature Range	T_{ST}	-55	125	°C

- Note 1:** Exceeding these values may cause permanent damage.
Note 2: Functional operation under these conditions is not implied.
Note 3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 3-2: RECOMMENDED OPERATING RATINGS

(Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	3.135	3.30	3.465	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	2.375	2.50	2.625	V
Operating Temperature	T_A	-40	25	85	°C
Input Voltage	V_{DD-IN}	-0.3	—	$V_{DD} + 0.3$	V

- Note 1:** Voltages are with respect to ground (GND) unless otherwise stated.
Note 2: The device core supports two power supply modes (3.3V and 2.5V).

TABLE 3-3: CURRENT CONSUMPTION

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Core device current	I_S 3.3V	—	49	53	mA	$V_{DD} = 3.3V+5\%$
	I_S 2.5V	—	48	53	mA	$V_{DD} = 2.5V+5\%$
Common output current	I_{DD_CM} 3.3V	—	5.24	5.82	mA	$V_{DDO} = 3.3V+5\%$
	I_{DD_CM} 2.5V	—	4.72	5.32	mA	$V_{DDO} = 2.5V+5\%$
Current dissipation per HCSL output	I_{DD_HCSL} 3.3V	—	14.92	17.18	mA	$V_{DDO} = 3.3V+5\%$
	I_{DD_HCSL} 2.5V	—	14.61	16.62	mA	$V_{DDO} = 2.5V+5\%$

ZL40264

TABLE 3-4: INPUT CHARACTERISTICS

Note 1, Note 2, Note 3

Parameter	Symbol	Min	Typ.	Max	Units	Condition
CMOS high-level input voltage for control inputs	$V_{CIH_3.3V}$	$0.7 \times V_{DD}$	—	—	V	$V_{DD} = 3.3V$
	$V_{CIH_2.5V}$	$0.8 \times V_{DD}$	—	—	V	$V_{DD} = 3.3V$
CMOS low-level input voltage for control inputs	V_{CIL}	—	—	$0.32 \times V_{DD}$	V	—
CMOS input leakage current for control inputs (includes current due to pull down resistors)	I_{IL}	-25	—	50	μA	$V_I = V_{DD}$ or $0V$
Differential input common mode voltage for IN_p/n	V_{CM}	0.1	—	0.8	V	—
Differential input voltage for IN_p/n	V_{ID}	0.2	—	$V_{DD} + 0.3$	V	—
Differential input leakage current for IN_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	-150	—	150	μA	$V_I = 2V$ or $0V$
Single ended input voltage for IN_p	V_{SI}	-0.3	—	2.7	V	$V_{DD} = 3.3V$ or $2.5V$
Single ended input common mode voltage IN_p	V_{SIC}	0.1	—	0.8	V	$V_{DD} = 3.3V$ or $2.5V$
Single ended input voltage swing for IN_p	V_{SID}	0.3	—	1.3	V	$V_{DD} = 3.3V$ or $2.5V$
Input frequency (differential)	f_{IN}	0	—	600	MHz	—
Input duty cycle (400 MHz input clock)	dc	35	—	65	%	Note 4
Input slew rate	slew	0.6	2	—	V/ns	—
Input pull-up/pull-down resistance	R_{PU}/R_{PD}	—	60	—	k Ω	—
Input pull-down resistance for IN_p	R_{PD}	—	30	—	k Ω	—
Control input (OE_b) pull-down resistance	R_{PDOE}	—	300	—	k Ω	—

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes ($V_{DD} = 3.3V$ and $V_{DD} = 2.5V$).

3: Low frequency only.

4: Minimum and maximum duty cycles should be scaled for different input frequencies. For example, a 10 MHz input clock would have the minimum duty cycle of 1% and the maximum duty cycle of 99%.

TABLE 3-5: POWER SUPPLY REJECTION RATIO FOR VDD = VDDO = 3.3V

Note 1, Note 2, Note 3

Parameter	Symbol	Min	Typ.	Max	Units	Condition
PSRR for HCSL output	PSRR _{HCSL}	—	-80.7	—	dBc	f _{IN} = 100 MHz
			-76.4			f _{IN} = 133 MHz
			-66.5			f _{IN} = 400 MHz

- Note 1:** Values are over recommended operating conditions.
Note 2: Noise injected to V_{DD}/V_{DDO} power supply with frequency 100 kHz and amplitude 100 mVpp.
Note 3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 3-6: POWER SUPPLY REJECTION RATIO FOR VDD = VDDO = 2.5V

Note 1, Note 2, Note 3

Parameter	Symbol	Min	Typ.	Max	Units	Condition
PSRR for HCSL output	PSRR _{HCSL}	—	-73.5	—	dBc	f _{IN} = 100 MHz
			-69.8			f _{IN} = 133 MHz
			-61.2			f _{IN} = 400 MHz

- Note 1:** Values are over recommended operating conditions.
Note 2: Noise injected to V_{DD}/V_{DDO} power supply with frequency 100 kHz and amplitude 100 mVpp.
Note 3: PSRR is measured as amplitude of 100 kHz spur in dBc on the output clock phase noise plot.

TABLE 3-7: HCSL OUTPUTS FOR VDDO = 3.3V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Rising edge rate	rise_rate	1.3	1.7	2	V/ns	Note 3, Note 4
Falling edge rate	fall_rate	1.3	1.7	2	V/ns	Note 3, Note 4
Differential high voltage	V _{IH}	0.6	—	0.9	V	Note 3
Differential low voltage	V _{IL}	-0.9	—	-0.6	V	Note 3
Single ended high voltage	V _{SIH}	0.6	0.74	0.85	V	DC Measurement
Single ended low voltage	V _{SIL}	-0.01	0	0.01	V	DC Measurement
Absolute crossing voltage	V _{CROSS}	0.26	0.32	0.38	V	Note 2, Note 5, Note 6
Variation of V _{CROSS} over all rising clock edges	ΔV _{CROSS}	0.039	0.050	0.061	V	Note 2, Note 5, Note 10
Ring back voltage margin	V _{RB}	0.534	0.674	0.809	V	Note 3, Note 12
Time before V _{RB} is allowed	t _{STABLE}	4.6	—	—	ns	Note 3, Note 12
Cycle-to-cycle additive jitter	T _{JCC}	—	6.5	8.1	ps peak-to-peak	Note 3
Absolute maximum voltage	V _{MAX}	—	—	0.92	—	Note 2, Note 8
Absolute minimum voltage	V _{MIN}	-0.05	—	—	—	Note 2, Note 9
Output duty-cycle (when input has 50% duty-cycle)	duty_cycle	48	50	52	%	Note 3
Rising to falling edge matching	r/f match	—	—	15	%	Note 2, Note 13
Clock source DC impedance (CK)	Z _{C-DC_CK}	49	50	51	Ω	DC Measurement Note 2, Note 14)
Clock source DC impedance (CK#)	Z _{C-DC_CK#}	49	50	51	Ω	DC Measurement Note 2, Note 14
Output frequency	F _{MAX}	0	—	600	MHz	—

TABLE 3-7: HCSL OUTPUTS FOR VDDO = 3.3V (CONTINUED)

Note 1						
Parameter	Symbol	Min	Typ.	Max	Units	Condition
Output-to-output skew	t_{OOSK}	—	—	50	ps	—
Device-to-device output skew	t_{DOOSK}	—	—	129	ps	—
Input-to-output delay	t_{IOD}	0.75	0.84	1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	2	cycles	—

- Note 1:** Values are over recommended operating conditions.
- 2: Measurement taken from single ended waveform.
 - 3: Measurement taken from differential waveform.
 - 4: Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See [Figure 3-4](#).
 - 5: Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See [Figure 3-1](#).
 - 6: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See [Figure 3-1](#).
 - 7: This requirement—from PCI Express Base Specification, Revision 4.0—is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.
 - 8: Defined as the maximum instantaneous voltage including overshoot. See [Figure 3-1](#).
 - 9: Defined as the minimum instantaneous voltage including undershoot. See [Figure 3-1](#).
 - 10: Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See [Figure 3-2](#).
 - 11: The PPM requirement—from PCIe Express Base Specification, Revision 4.0—is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.
 - 12: The t_{STABLE} is the time the differential clock must maintain a minimum ± 150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the $V_{RB} \pm 100$ mV differential range. See [Figure 3-5](#).
 - 13: Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ± 75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 3-3](#).
 - 14: Clock DC impedance tolerance depends only on the tolerance of external 50 Ω shunt resistors used in HCSL. The test used resistors with $\pm 1\%$ tolerance.

TABLE 3-8: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 3.3V

Note 1						
Parameter	Symbol	Min	Typ.	Max	Units	Condition
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{PCle_1.0}$	—	1.2	1.45	ps pk-pk	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{PCle_2.0_high}$	—	134	163	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{PCle_2.0_low}$	—	31	48	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$T_{PCle_2.0_mid}$	—	105	130	fs RMS	Input clock: 100 MHz

TABLE 3-8: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 3.3V (CONTINUED)

Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{PCle_3.0}$	—	33	41	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{PCle_4.0}$	—	33	41	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{PCle_5.0}$	—	13	16	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1 MHz, CDR for 64 GT/s CC)	$T_{PCle_6.0}$	—	8	10	fs RMS	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	T_{PCle}	—	61	75	fs RMS	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz Band	$T_{j_1M_20M}$	—	87	106	fs RMS	Input clock: 100 MHz
		—	56	68		Input clock: 133 MHz
		—	26	34		Input clock: 400 MHz
		—	25	32		Input clock: 491.52 MHz
Additive RMS Jitter in 12 kHz to 20 MHz Band	$T_{j_12k_20M}$	—	91	112	fs RMS	Input clock: 100 MHz
		—	60	75		Input clock: 133 MHz
		—	32	48		Input clock: 400 MHz
		—	30	43		Input clock: 491.52 MHz
Noise Floor	NF	—	-161	-159	dBc/Hz	Input clock: 100 MHz
		—	-162	-161		Input clock: 133 MHz
		—	-160	-157		Input clock: 400 MHz
		—	-158	-155		Input clock: 491.52 MHz

Note 1: Values are over recommended operating conditions.

TABLE 3-9: HCSL OUTPUTS FOR VDDO = 2.5V

Note 1						
Parameter	Symbol	Min	Typ.	Max	Units	Condition
Rising edge rate	rise_rate	1.3	1.6	1.9	V/ns	Note 2, Note 3
Falling edge rate	fall_rate	1.3	1.6	1.9	V/ms	Note 2, Note 3
Differential high voltage	V_{IH}	0.6	—	0.9	V	Note 2
Differential low voltage	V_{IL}	-0.9	—	-0.6	V	Note 2
Single-ended high voltage	V_{SIH}	0.58	0.71	0.84	V	DC measurement
Single-ended low voltage	V_{SIL}	-0.01	0	0.01	V	DC measurement
Absolute crossing voltage	V_{CROSS}	0.25	0.31	0.37	V	Note 1, Note 4, Note 5
Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}	0.04	0.05	0.06	V	Note 1, Note 4, Note 9
Ring back voltage margin	V_{RB}	0.514	0.660	0.791	V	Note 2, Note 11
Time before VRB is allowed	t_{STABLE}	4.6	—	—	ns	Note 2, Note 11
Additive cycle-to-cycle jitter	T_{JCC}	—	5.5	7.1	ps peak-to-peak	Note 2
Absolute maximum voltage	V_{MAX}	—	—	0.90		Note 1, Note 7
Absolute minimum voltage	V_{MIN}	-0.05	—	—		Note 1, Note 8
Output duty-cycle (when input has 50% duty-cycle)	duty_cycle	48	50	52	%	Note 2

TABLE 3-9: HCSL OUTPUTS FOR VDDO = 2.5V (CONTINUED)

Note 1						
Parameter	Symbol	Min	Typ.	Max	Units	Condition
Rising to falling edge matching	r/f match	—	—	15	%	Note 1, Note 12
Clock source DC impedance (CK)	Z_{C-DC_CK}	49	50	51	Ω	DC measurement, Note 1, Note 13
Clock source DC impedance (CK#)	$Z_{C-DC_CK\#}$	0	50	51	Ω	DC measurement, Note 1, Note 13
Output frequency	F_{MAX}	—	—	600	MHz	—
Output-to-output skew	t_{OOSK}	—	—	50	ps	—
Device-to-device output skew	t_{DOOSK}	0.75	—	129	ps	—
Input-to-output delay	t_{OPD}	—	0.85	1	ns	—
Output enable time	t_{EN}	—	—	3	cycles	—
Output disable time	t_{DIS}	—	—	3	cycles	—

- Note 1:** Values are over recommended operating conditions.
- 2:** Measurement taken from single ended waveform.
 - 3:** Measurement taken from differential waveform.
 - 4:** Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See [Figure 3-4](#).
 - 5:** Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK#. See [Figure 3-1](#).
 - 6:** Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See [Figure 3-1](#).
 - 7:** This requirement—from PCI Express Base Specification, Revision 4.0—is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.
 - 8:** Defined as the maximum instantaneous voltage including overshoot. See [Figure 3-1](#).
 - 9:** Defined as the minimum instantaneous voltage including undershoot. See [Figure 3-1](#).
 - 10:** Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in V_{CROSS} for any particular system. See [Figure 3-2](#).
 - 11:** The PPM requirement—from PCIe Express Base Specification, Revision 4.0—is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.
 - 12:** The t_{STABLE} is the time the differential clock must maintain a minimum ± 150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the $V_{RB} \pm 100$ mV differential range. See [Figure 3-5](#).
 - 13:** Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ± 75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See [Figure 3-3](#).
 - 14:** Clock DC impedance tolerance depends only on the tolerance of external 50 Ω shunt resistors used in HCSL. The test used resistors with $\pm 1\%$ tolerance.

TABLE 3-10: HCSL (PCIE) JITTER PERFORMANCE FOR VDDO = 2.5V

Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Additive Jitter as per PCIe 1.0 (1.5 MHz to 22 MHz)	$T_{jPCIE_1.0}$	—	1.03	1.27	ps pk-pk	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 high band (1.5 MHz to 50 MHz)	$T_{jPCIE_2.0_high}$	—	115	143	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 low band (10 kHz to 1.5 MHz)	$T_{jPCIE_2.0_low}$	—	28	46	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 2.0 mid band (5 MHz to 16 MHz)	$T_{jPCIE_2.0_mid}$	—	91	113	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIE_3.0}$	—	29	36	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$T_{jPCIE_4.0}$	—	29	36	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$T_{jPCIE_5.0}$	—	11	14	fs RMS	Input clock: 100 MHz
Additive Jitter as per PCIe 6.0 (PLL_BW = 0.5 MHz to 1 MHz, CDR for 64 GT/s CC)	$T_{jPCIE_6.0}$	—	7	9	fs RMS	Input clock: 100 MHz
Additive Jitter as per Intel QPI 9.6 Gbps	T_{jQPI}	—	53	67	fs RMS	Input clock: 100 MHz
Additive RMS Jitter in 1 MHz to 20 MHz band	$T_{j_1M_20M}$	—	75	94	fs RMS	Input clock: 100 MHz
		—	51	64		Input clock: 133 MHz
		—	26	33		Input clock: 400 MHz
		—	25	32		Input clock: 491.52 MHz
Additive RMS Jitter in 12 kHz to 20 MHz band	$T_{j_12k_20M}$	—	79	99	fs RMS	Input clock: 100 MHz
		—	55	68		Input clock: 133 MHz
		—	32	47		Input clock: 400 MHz
		—	30	43		Input clock: 491.52 MHz
Noise floor	N_F	—	-162	-159	dBc/Hz	Input clock: 100 MHz
		—	-163	-161		Input clock: 133 MHz
		—	-160	-158		Input clock: 400 MHz
		—	-158	-155		Input clock: 491.52 MHz

Note 1: Values are over recommended operating conditions.

ZL40264

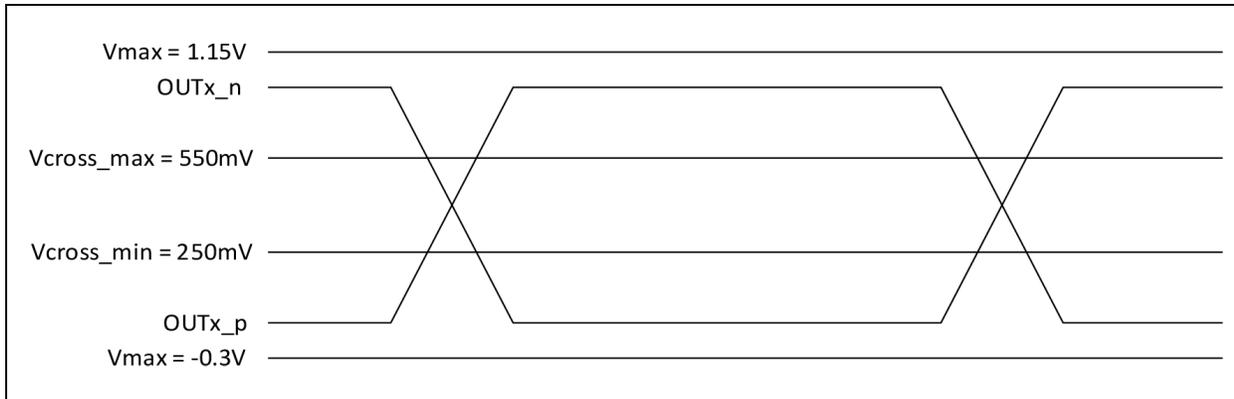


FIGURE 3-1: Single-Ended Measurement Points for Absolute Cross Point and Swing.

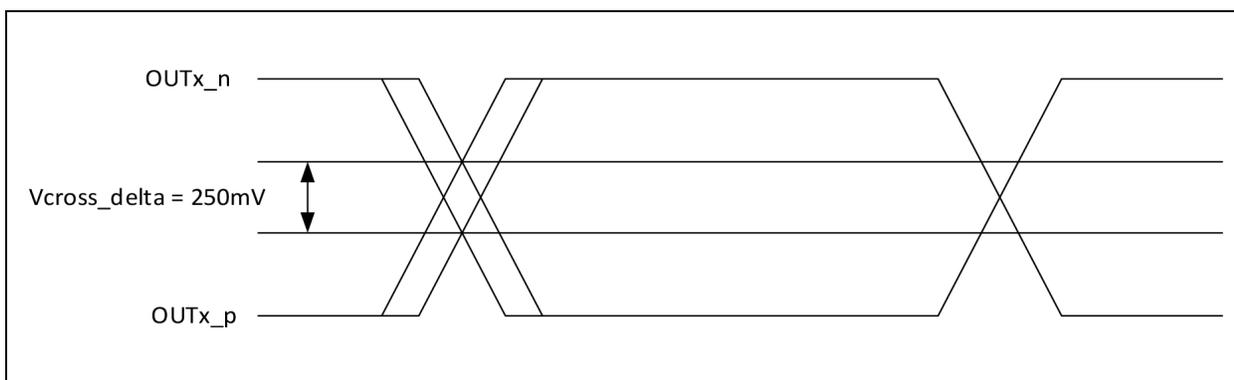


FIGURE 3-2: Single-Ended Measurement Points for Delta Cross Point.

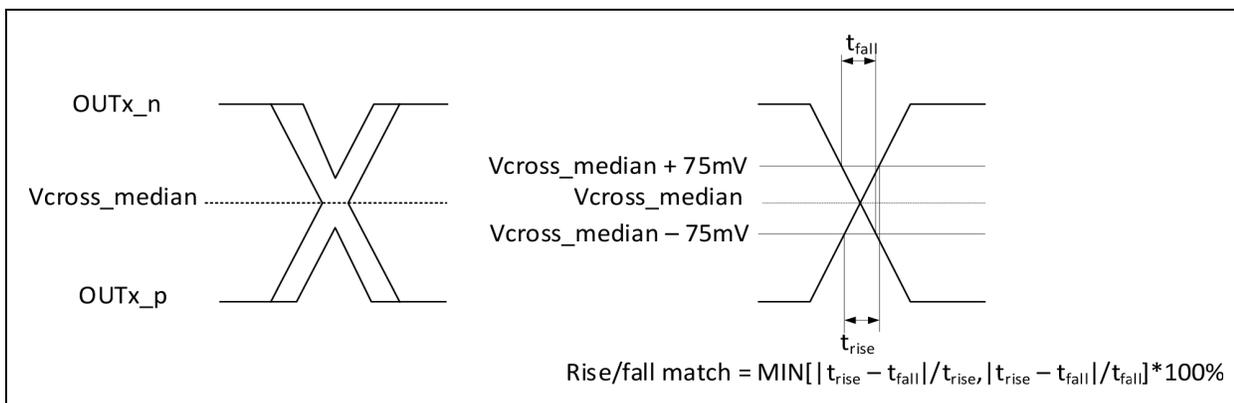


FIGURE 3-3: Single-Ended Measurement Points for Rise and Fall Time Matching.

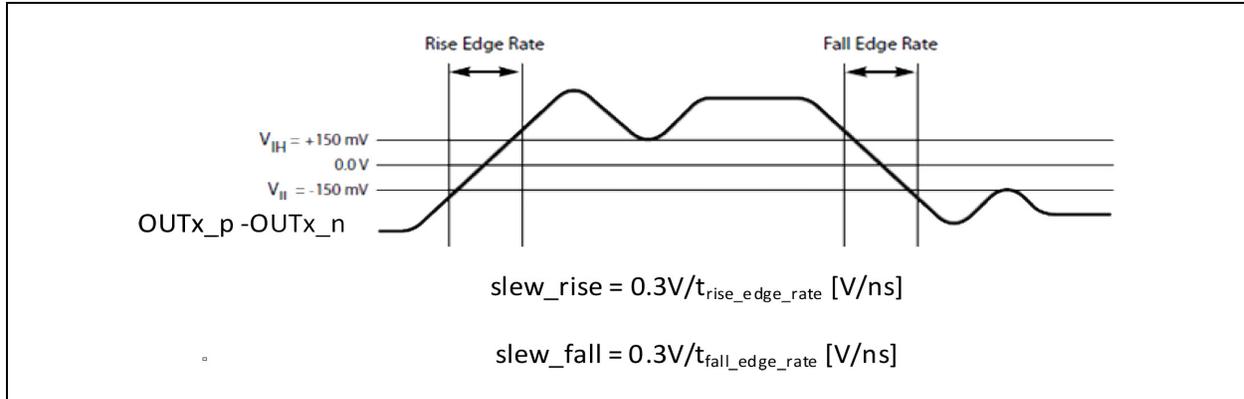


FIGURE 3-4: Differential Measurement Points for Rise and Fall Time.

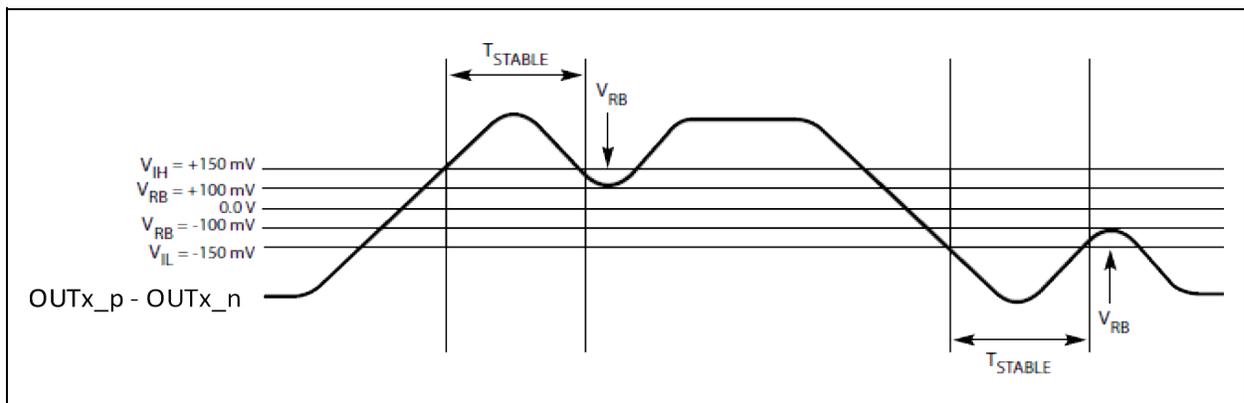


FIGURE 3-5: Differential Measurement Points for Ringback.

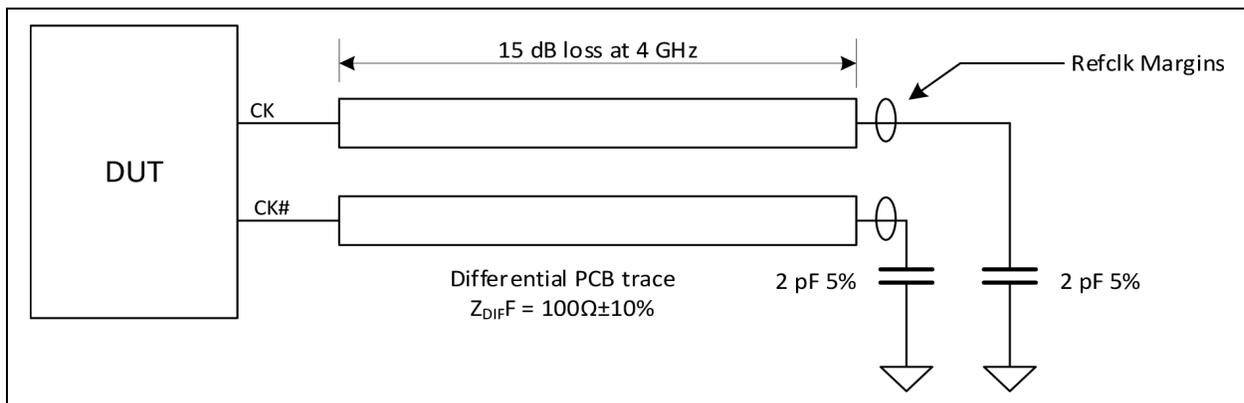


FIGURE 3-6: PCIe Test Circuit.

TABLE 3-11: 4 MM × 4 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Value	Units	Condition
Maximum ambient temperature	T_A	85	°C	—
Maximum junction temperature	T_{JMAX}	125	°C	—
Junction-to-ambient thermal resistance (Note 1)	θ_{JA}	34	°C/W	Still air
		28.9		1 m/s airflow
		27.0		2.5 m/s airflow
Junction-to-board thermal resistance	θ_{JB}	15.4	°C/W	—
Junction-to-case thermal resistance	θ_{JC}	25.9	°C/W	—
Junction-to-pad thermal resistance	θ_{JP}	8.1	°C/W	Still air
Junction-to-top-center thermal characterization parameter	Ψ_{JT}	1.0	°C/W	Still air

- Note 1:** Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.
- 2:** Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package).

TABLE 3-12: HCSL OUTPUT PHASE NOISE WITH 25 MHZ XTAL

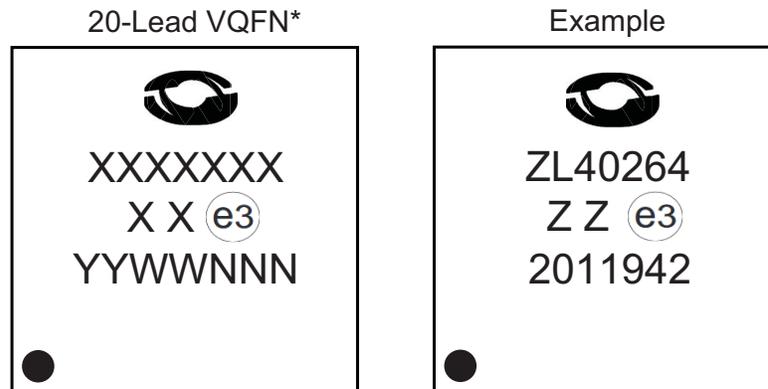
Note 1

Parameter	Symbol	Min	Typ.	Max	Units	Condition
Jitter RMS in 12 kHz to 5 MHz band	$T_{J_12M_5M}$	—	235	—	fs	$V_{DD} = 3.3V, V_{DDO} = 3.3V$
		—	143	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V$
Noise floor	N_F	—	-102	—	dBc/Hz	$V_{DD} = 3.3V, V_{DDO} = 3.3V @100 Hz$
		—	-126	—		$V_{DD} = 3.3V, V_{DDO} = 3.3V @1 kHz$
		—	-153	—		$V_{DD} = 3.3V, V_{DDO} = 3.3V @10 kHz$
		—	-158	—		$V_{DD} = 3.3V, V_{DDO} = 3.3V @100 kHz$
		—	-159	—		$V_{DD} = 3.3V, V_{DDO} = 3.3V @1 MHz$
		—	-158	—		$V_{DD} = 3.3V, V_{DDO} = 3.3V @5 MHz$
		—	-97	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @100 Hz$
		—	-123	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @1 kHz$
		—	-153	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @10 kHz$
		—	-162	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @100 kHz$
		—	-162	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @1 MHz$
		—	-163	—		$V_{DD} = 2.5V, V_{DDO} = 2.5V @5 MHz$

- Note 1:** Values are over recommended operating conditions.

4.0 PACKAGE OUTLINE

4.1 Package Marking Information



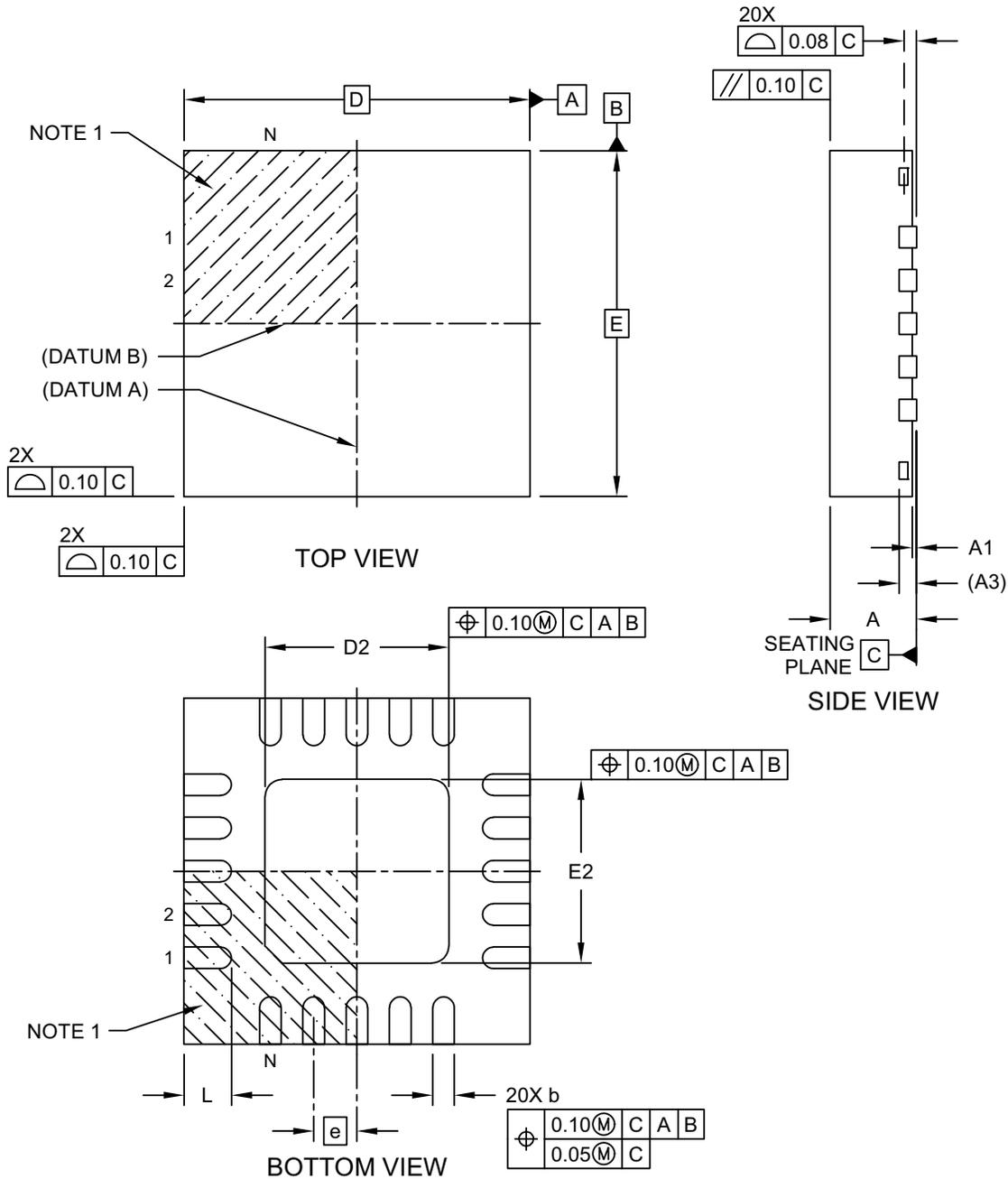
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space: 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN; 2 Characters = NN; 1 Character = N.

ZL40264

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

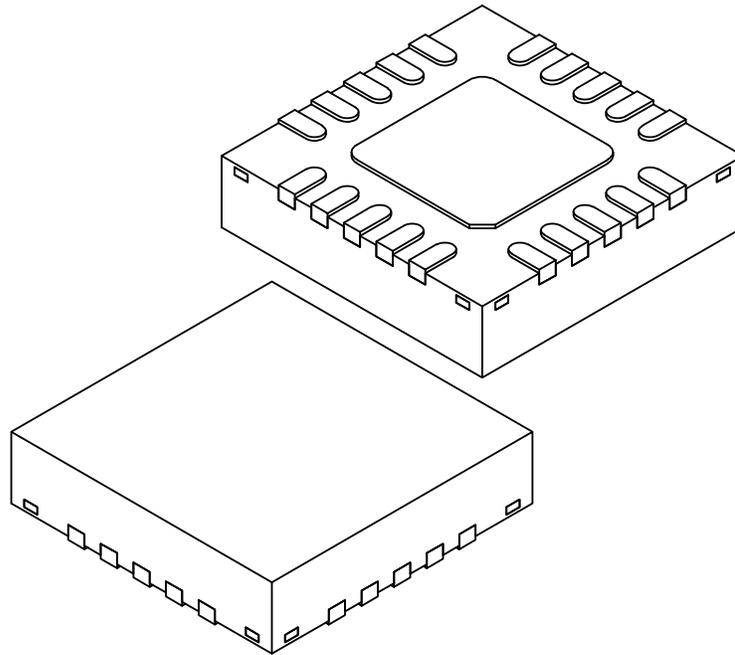
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-25395 Rev A Sheet 1 of 2

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	20		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.025	2.125	2.225
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.025	2.125	2.225
Terminal Width	b	0.20	0.25	0.32
Terminal Length	L	0.45	0.55	0.65

Notes:

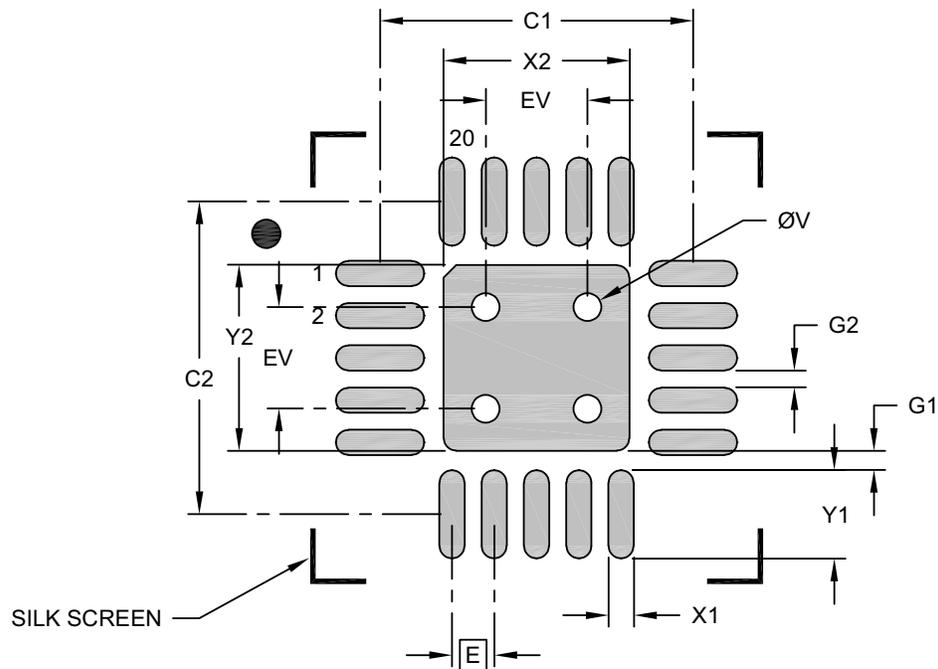
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25395 Rev A Sheet 2 of 2

ZL40264

20-Lead 4 mm × 4 mm VQFN with 2.125 mm Exposed Pad (LWC) Package Outline and Recommended Landing Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.20
Optional Center Pad Length	Y2			2.20
Contact Pad Spacing	C1		3.70	
Contact Pad Spacing	C2		3.70	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			1.05
Contact Pad to Center Pad (X20)	G1	0.23		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27395 Rev A

NOTES:

ZL40264

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006788A (07-2024)	—	Converted Microsemi data sheet ZL40264 to Microchip DS20006788A. Figures 2-4 and 2-5 updated. Added Figure 2-12. Updated multiple tables throughout Section 3. Minor text and table changes throughout.

NOTES:

ZL40264

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	<u>X</u>	<u>XX</u>	<u>X</u>	Examples:
Device	Chip Carrier Type	Package	Media Type	Finish	
Device:	ZL40264: Four Output Ultra-Low Additive Phase Noise PCIe, Gen 1 to 5, and UPI/QPI Fanout Buffer				<p>a) ZL40264LDG1: Low Skew, Low Additive Jitter, Leadless Chip Carrier, 48-Lead VQFN Package, 490/Tray and Pb Free with Matte Sn Lead Finish Equating to RoHS e3</p> <p>b) ZL40264LDF1: Low Skew, Low Additive Jitter, Leadless Chip Carrier, 48-Lead VQFN Package, 4,000/Reel and Pb Free with Matte Sn Lead Finish Equating to RoHS e3</p> <p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p>
Chip Carrier Type:	L = Leadless Chip Carrier				
Package:	D = 20-Lead VQFN Package with E-Pad				
Media Type:	G = 490/Tray F = 4,000/Tape & Reel				
Finish:	1 = Pb Free with Matte Sn Lead Finish Equating to RoHS e3				

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at <https://www.microchip.com/en-us/support/design-help/client-support-services>.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzor, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2024, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-4848-2



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880-3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Hod Hasharon
Tel: 972-9-775-5100

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820