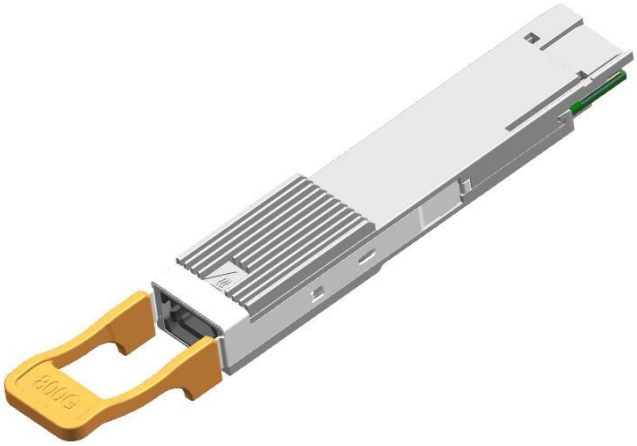
Specification

Quad Small Form-factor Pluggable Double Density
Optical Transceiver Module
QSFP-DD 400GBASE-SR4
(Preliminary)



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Ordering Information:

Model Name	TQS-R16H9-8CZ	Note
Voltage	3.3V	
Device type	850nm VCSEL	
Temperature	0°C~+70°C	
Distance	60m (OM3) / 100m (OM4)	
Optical interface	MPO12 connector	
Latch Color	Beige	

Features

- Hot-pluggable QSFP-DD form factor
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- Maximum link length of 60m on OM3 or 100m on OM4
- MPO-12 APC connector
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Case operating temperature:
- Less than 10W in temperature range of 0 to 70°C
- Single 3.3V power supply voltage
- Compliant to QSFP-DD Module Specification Rev 6.0
- Compliant to CMIS 5.2
- Compliant to IEEE 802.3bs
- RoHS Compliant

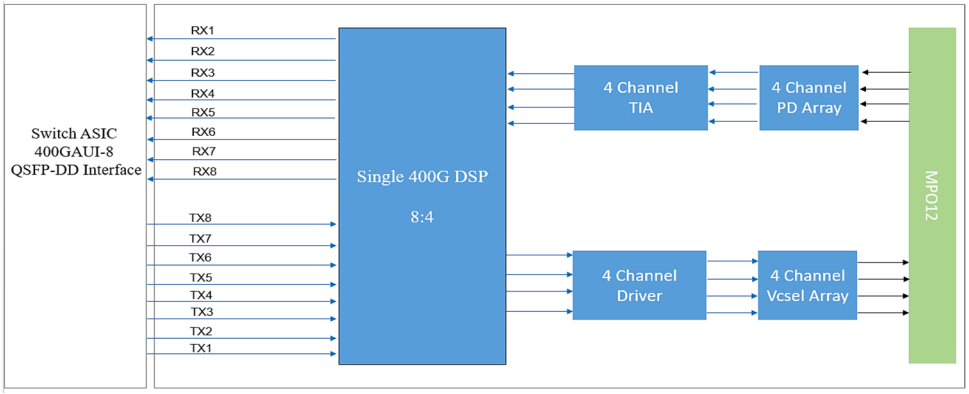
Applications

- 400G Ethernet
- Data Center

General Description

TQS-R16H9-8CZ is a four-Channel, Parallel, Pluggable, Fiber Optic QSFP-DD Module for 400Gigabit Ethernet applications. This product converts 8 channels of 26.5625GBd electrical input data to 4 channels of 53.125GBd parallel optical signals. Reversely, on the receiver side, 4 channels of parallel optical signals of 53.125GBd converts to 8 channels of 26.5625GBd electrical output data. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm, up to 60 meters over OM3 MMF or 100 meters over OM4 MMF.

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	0		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity (no-condensation)	RH	15		85	%	
Case Operating Temperature	Top	0		70	℃	
Receiver Damage Threshold, per Lane	PRdmg	5			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	Vcc	3.135		3.465	V	
Supply Current per end	Icc			3.18	A	
Total Power Consumption				10	W	1
Supply Current				3.19	A	
Operating Case Temperature	Top	0		70	℃	
Relative Humidity (non-condensation)	RH	15		85	%	
Bit Rate	BR	-		425	Gbps	
Fiber Length on OM3 MMF				60	m	
Fiber Length on OM4 MMF				100	m	
I2C Clock Frequency	0			400	kHz	

Notes:

1. Under condition of 3.465V operating supply voltage, and 70℃ case temperature.

Optical Characteristics

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Transmitter							
Data rate per lane		DR		53.125		GBd	
Modulation format				PAM4			
Center Wavelength		λ	840	860	868	nm	1
RMS spectral width		σ			0.6	nm	
Average launch power, each lane		P_{avg}	-4.6		4.0	dBm	
Optical Power OMA, each Lane, max		P_{OMA}		3.5		dBm	
OMAouter, each lane min	Max (TECQ, TDECQ) < 1.8 dB		Max [-2.6, max (TECQ, TDECQ) -4.4]			dBm	
	1.8 < max (TECQ,TDECQ) <4.4dB						
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane (max)		TECQ			4.4	dB	
Extinction ration, each lane		ER	2.5			dB	
Transmitter power excursion, each lane					2.3	dBm	
Optical Return Loss Tolerance		ORLT			14	dB	
Average Launch Power of OFF Transmitter, each lane					-30	dBm	
Encircled fluxb			≥86% at 19um ≤30% at 4.5um				2

Notes:

1. Defined according to the performance of the laser used
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Receiver						
Signaling rate, each lane			53.125		GBd	
Modulation format			PAM4			
Center Wavelength	λ	842	850	948	nm	
Damage Threshold		5	-	-	dBm	
Average receive power, each lane		-6.4	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane		-	-	3.5	dBm	
Receiver Reflectance	Rr			-15	dB	
Receiver sensitivity (OMA_{outer}), each lane		RX = max (-4.6, TECQ -6.4)			dBm	1
Stressed receiver sensitivity (OMA_{outer}), each lane				-2.0	dBm	
RX LOS Assert	LOSA	-15			dBm	
RX LOS De-assert	LOSD			-7.5	dBm	
RX LOS Hysteresis	LOSH	0.5		5	dB	

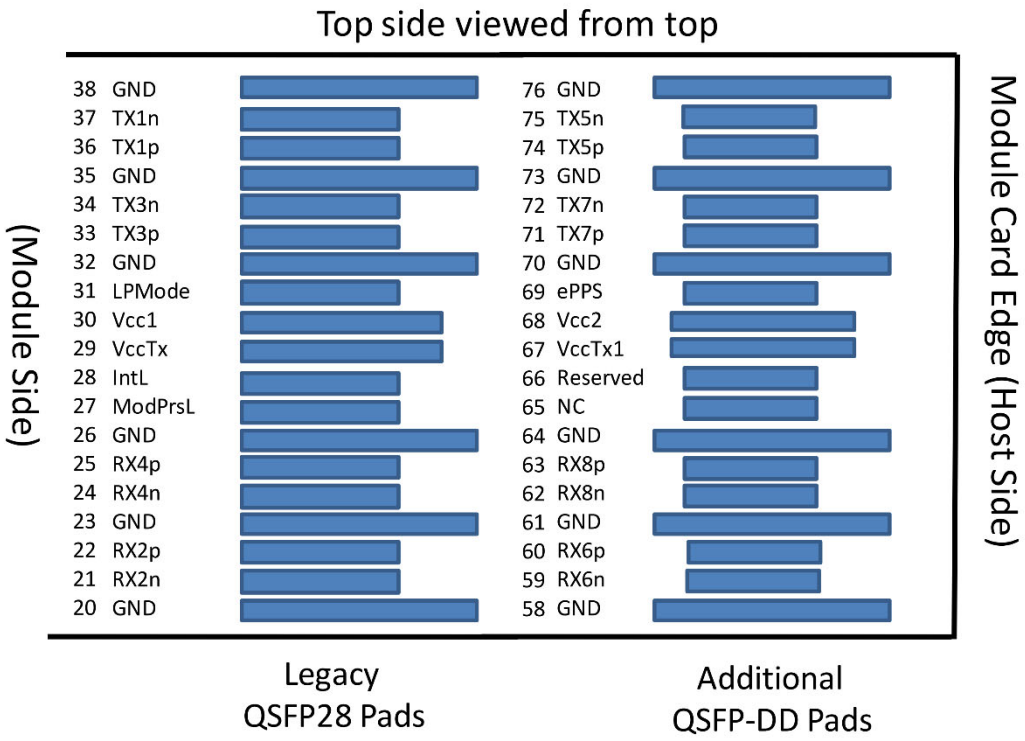
Notes:

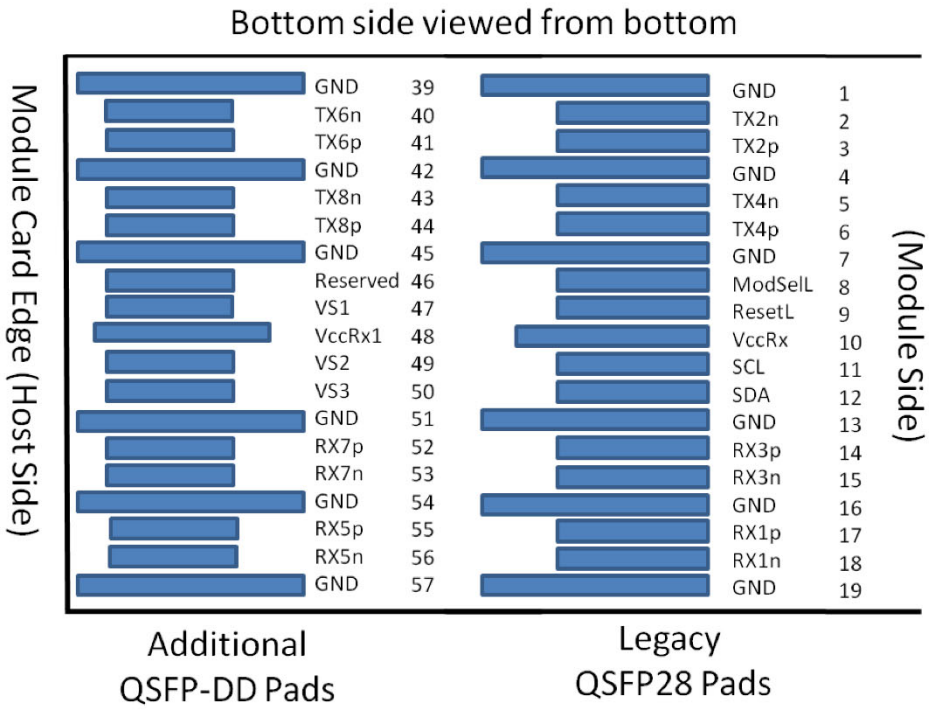
1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Characteristics

Parameter	Min	Typ.	Max	Unit	Note
Supply Voltage	3.135		3.465		
Input Differential Impedance	90	100	110	Ω	
Differential data input swing			880	mVpp	
Differential data output swing			900	mVpp	
Bit Error Rate			2.4E-4		
Input Logic Level High	2		vcc	v	
Input Logic Level Low	0		0.8	v	
Output Logic Level High	Vcc-0.5		vcc	v	
Output Logic Level Low	0		0.4	v	

QSFP-DD Module Pad Assignments and Descriptions





Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	

35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3

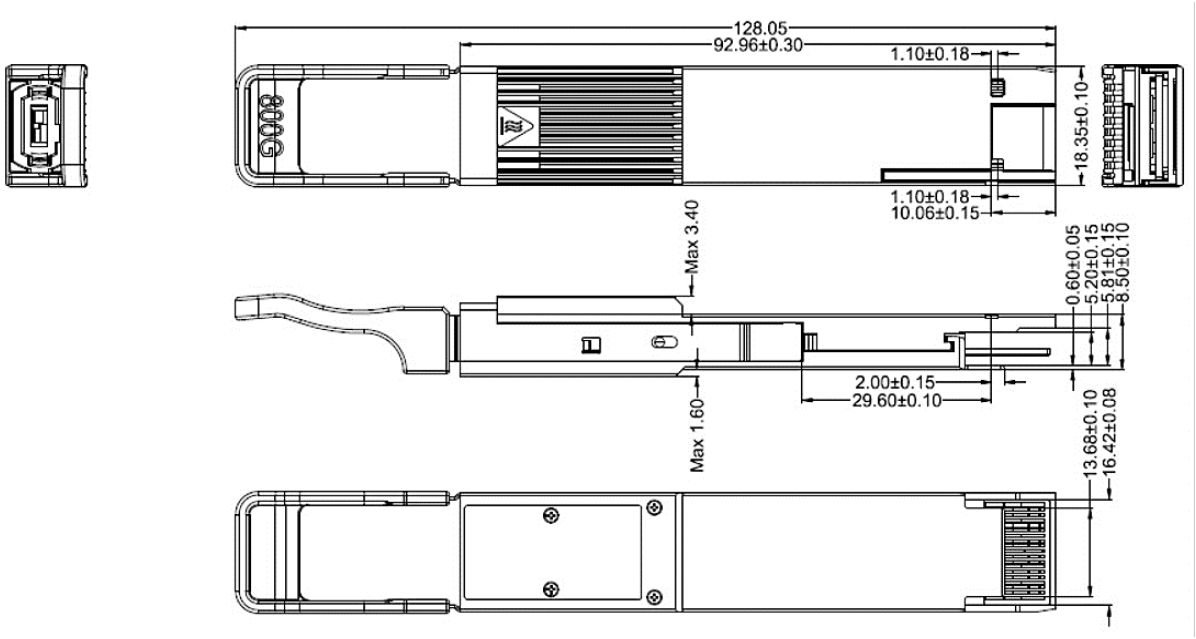
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

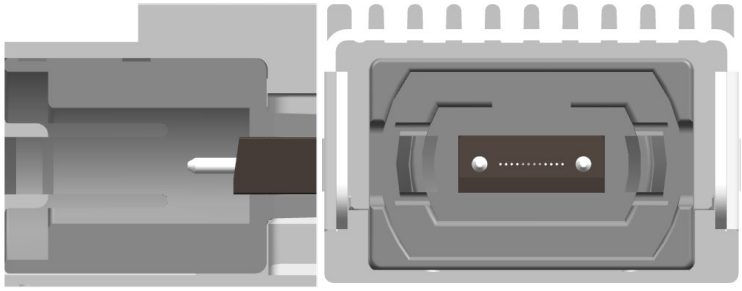
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. For power classes 4 and above the module differential loading of input voltage pins must not result in exceeding pin current limits. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

Mechanical Design Diagram

(Unit: mm)

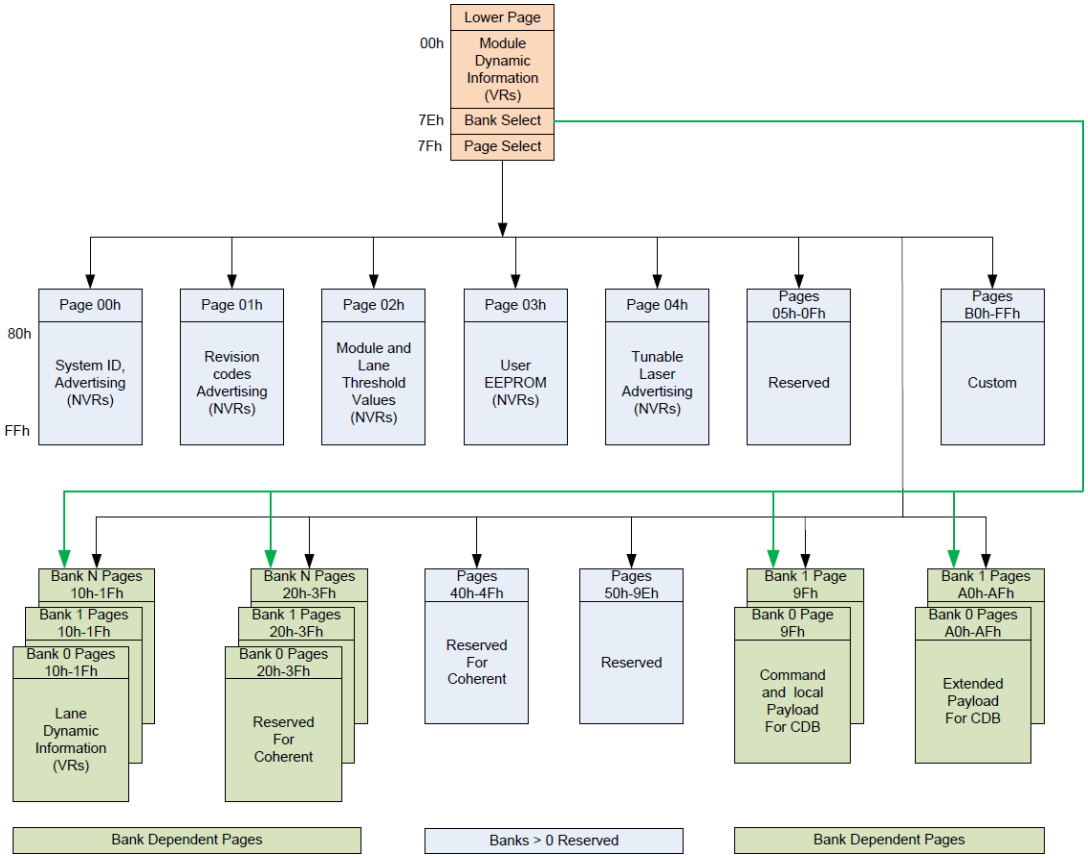


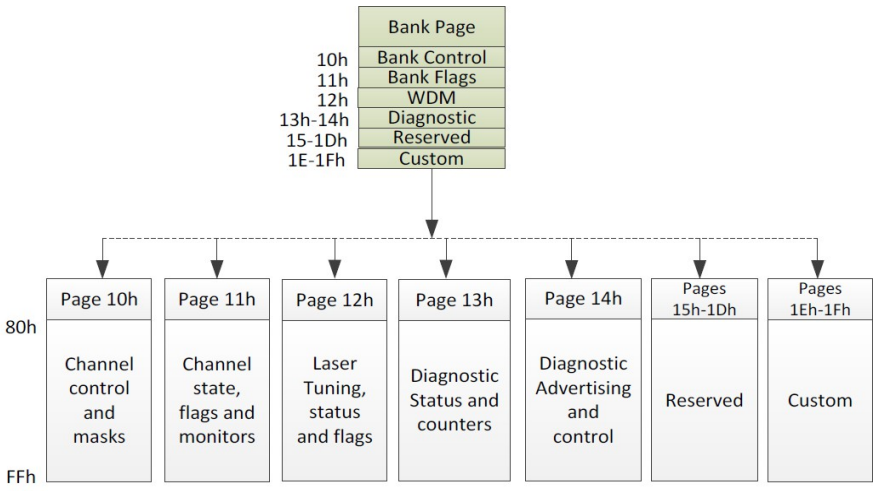
Optical Interface requirement



User Interface

Management Interface





Multiple Applications Support

The TQS-Q16H9-8CZ supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	31	HostInterfaceIDApp1: IB HDR
87		MediaInterfaceID	11	MediaInterfaceIDApp1: 400G-SR4
88		HostLaneCount&MediaLaneCount	84	LaneCountApp1: host 8 lanes, media 4 lanes
89		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:176		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
90	0010b	HostInterfaceID	11	HostInterfaceIDApp2:400GAUI-8 C2M
91		MediaInterfaceID	11	MediaInterfaceIDApp2: 400G-SR4
92		HostLaneCount&MediaLaneCount	84	LaneCountApp2: host 8 lanes, media 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	F	HostInterfaceIDApp3:200GAUI-4
95		MediaInterfaceID	1B	MediaInterfaceIDApp3:200GBASE-SR2
96		HostLaneCount&MediaLaneCount	42	LaneCountApp3:host 4 lanes, media 2 lanes
97		HostLaneAssignmentOptions	11	Permissible first host lane number: lane 1，5
01h:178		MediaLaneAssignmentOptions	5	Permissible first media lane numbern: lane 1,3
98	0100b	HostInterfaceID	D	HostInterfaceIDApp4: 100GAUI-2 C2M
99		MediaInterfaceID	D	MediaInterfaceIDApp4:100GBASE-SR1
100		HostLaneCount&MediaLaneCount	21	LaneCountApp4：host 2 lanes, media 1 lanes
101		HostLaneAssignmentOptions	55	Permissible first host lane number: lanes 1, 3，5，7
01h:179		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4

102	0101b	HostInterfaceID	FF	HostInterfaceIDApp5
103		MediaInterfaceID	0	MediaInterfaceIDApp5
104		HostLaneCount&MediaLaneCount	0	LaneCountApp5
105		HostLaneAssignmentOptions	0	HostLaneAssignmentOptionsApp5

As shown in the table above，the TQS-Q16H9-8CZ supports 4 applications, IB HDR 400GBASE-SR4 and Ethernet 400GBASE-SR4, 200GBASE-SR2, 100GBASE-SR1.

Multiple Applications Support

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

**Note that the channels of the module are independent and can be configured separately.(ie. up to four 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time*

TQS-Q16H9-8CZ supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized which is simpler.

First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152 (8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	IB HDR	400GBASE-SR4
1	00000001b	400GAUI-8 C2M	400GBASE-SR4
2	00000010b	200GAUI-4 C2M	200GBASE-SR2
3	00000011b	100GAUI-2 C2M	100GBASE-SR

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Lookback Capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally measured transceiver temperature[1]	±3	°C
Internally measured transceiver supply voltage	±3	%
Measured Tx bias current	±10	%
Measured Tx output power[2]	±3	dB
Measured Rx received average optical power	±3	dB

Notes:

1. Test point is the hotspot of the module.
2. DDM report stability shall be within 0.5 dB when temperature is stable. TX DDM must report -40 dBm when TX disable.

Contact Information

Formerica OptoElectronics Inc.
5F-11, No.38, Taiyuan St., Zhubei City,
Hsinchu County 30265, Taiwan
Tel: +886-3-5600286
Fax: +886-3-5600239

inquiry@formericaoe.com

www.formericaoe.com

Revision History

Date	Version	Description
5/22/2024	0.1	Preliminary release