Specification

OSFP RHS 400G DR4 Transceiver

(Preliminary)

T E S – L 1 6 H B – C C Z

Ordering Information:

Model Name	TES-L16HB-CCZ	Note
Voltage	3.3V	
Device type	1310nm DFB	
Temperature	0°C~+70°C	
Distance	500m (SMF)	
Optical interface	MPO-12 connector	
Latch Color	Beige	

Features

- Form Factor: Hot-pluggable OSFP form factor
- Data Rate: Aggregate data rate of 425 Gb/s and Breakout data rate of 106.25 Gb/s
- Optical Interface: Compliant to 400GBASE-DR4 and 4x100GBASE-DR
- Electrical Interface: Compliant to 400GAUI-4 and 4x100GAUI-1
- Management Interface: I2C management interface
- Reach: Up to 500m over MPO-12/APC single mode fiber
- Power consumption: 9 W max
- Operating case temperature: 0 ~ 70°C
- Power Supply: Single 3.3V power supply
- Compliant with IEEE802.3bs
- Compliant with CMIS 5.2
- RoHS compliant

Applications

- 400Gb/s Ethernet
- Data Center
- InfiniBand

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity (no-condensation)	RH	5		95	%	
Optical Input Power, per Lane	PIN			5.0	dBm	
Operating Case Temperature	Top	0		70	℃	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Signaling Rate, each lane			53.125		GBd	
Data Rate Accuracy		-100		100	ppm	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Pre-FEC Bit Error Ratio				2.4E-4		
Transmission Distance				500	m	

Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Signaling rate, each lane	SR	53.125 +/- 100ppm			GBd	
Modulation format		PAM4			-	
Lane wavelength	λ	1304.5	1311.0	1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane	AOP_{TX}	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane	OMA_{TX}	-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Average launch power of OFF transmitter, each lane	AOP_{OFF}			-15	dBm	
Extinction ratio, each lane	ER	3.5			dB	
$RIN_{21.4}OMA$				–136	dB/Hz	
Optical return loss tolerance	RLTol			21.4	dB	
Transmitter reflectance	Reflectance_Tx			-26	dB	3
Receiver						
Signaling rate, each lane	SR	53.125 +/- 100ppm			GBd	
Modulation format		PAM4			-	
Lane wavelengths	λ	1304.5	1311.0	1317.5	nm	

Damage threshold, each lane		DThd	5			dBm	4
Average receive power, each lane		AOP_{RX}	-5.9		4	dBm	5
Receive power (OMAouter), each lane		OMA_{RX}			4.2	dBm	
Receiver reflectance		Reflectance_Rx			-26	dB	
Receiver sensitivity (OMAouter), each lane		RxSens			-4.4	dBm	6
Stressed receiver sensitivity (OMAouter), each lane		SRS			-1.9	dBm	7
Conditions of stressed receiver sensitivity test:							8
Stressed eye closure for PAM4 (SECQ), lane under test				3.4		dB	
OMAouter of each aggressor lane				4.2		dBm	
RX LOS	LOS Assert	LOSA	-15		-7.9	dBm	
	LOS De-assert	LOSD			-7.4	dBm	
	LOS Hysteresis	LOSH	0.5		5	dB	

Notes：

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure complianceEven if max (TECQ, TDECQ) < 1.8dB, OMAouter (min) must exceed this value.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.
3. Transmitter reflectance is defined looking into the transmitter.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
5. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
7. Measured with conformance test signal at TP3 for the BER = 2.4E-4.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

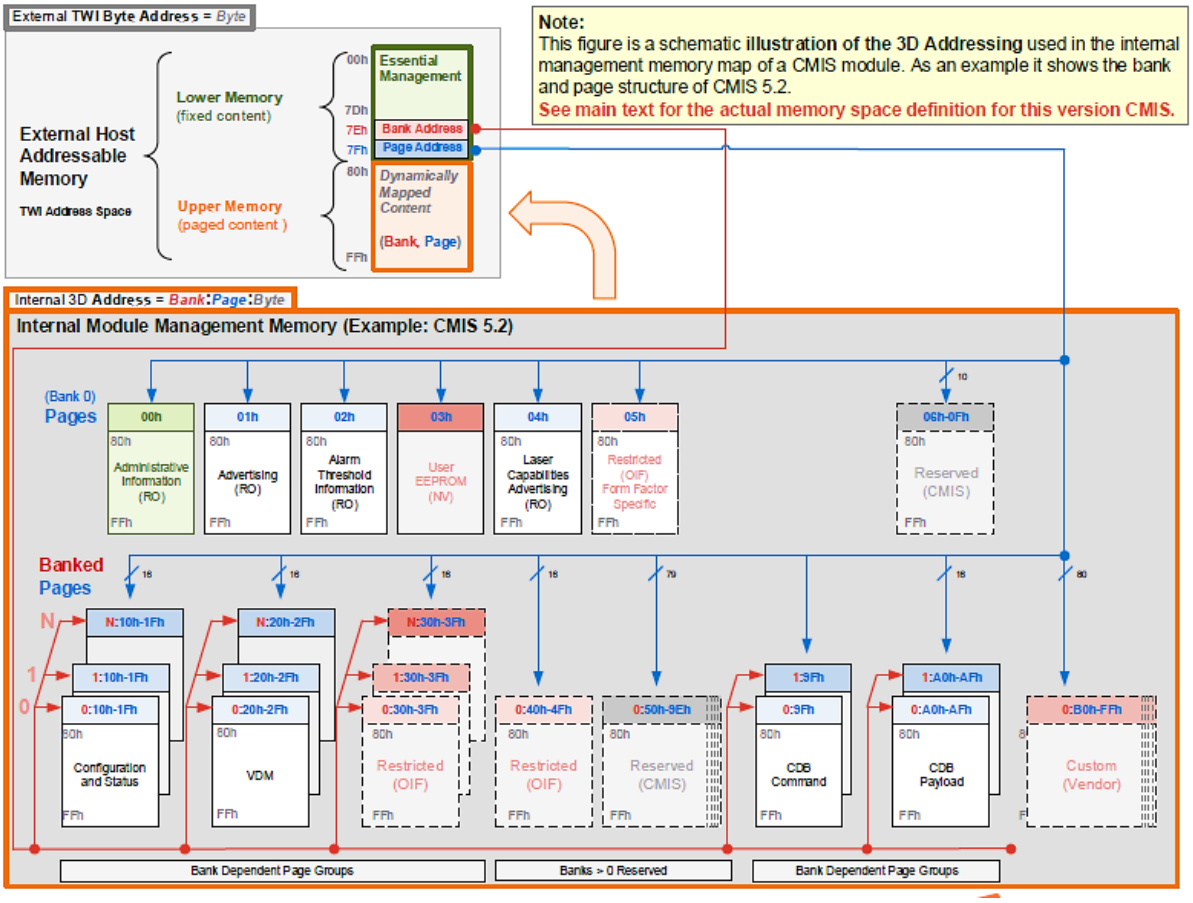
Electrical Characteristics

Parameter	Test Point	Min	Typ.	Max	Unit	Note
Transmitter						
Signaling rate, each lane	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk voltage tolerance	TP1a	750			mV	
Peak-to-peak AC common-mode voltage tolerance	TP1a	25			mV	
Differential-mode to common-mode return loss, RLcd	TP1	Equation (120G–2)			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module stressed input tolerance	TP1a	See 120G.3.4.3			-	
Single-ended voltage tolerance range	TP1a	–0.4		3.3	V	
DC common-mode voltage tolerance	TP1	-0.35		2.85	V	
Module stressed input tolerance test :						
Pattern generator transition time	TP1a		9		ps	
Applied peak-peak sinusoidal jitter	TP1a		Table 162-16			
Eye height	TP1a		10		mV	
Vertical eye closure, VEC	TP1a	12		12.5	dB	
Crosstalk differential peak-to-peak voltage	TP4		845		mV	
Crosstalk transition time	TP4		8.5		ps	
Receiver						
Signaling rate, each lane	TP4	53.125 ± 100 ppm			GBd	
Peak-to-peak AC common-mode voltage	TP4			25	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	mV	
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Common-mode to differential-mode return loss, RLdc	TP4	Equation (120G-1)			dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

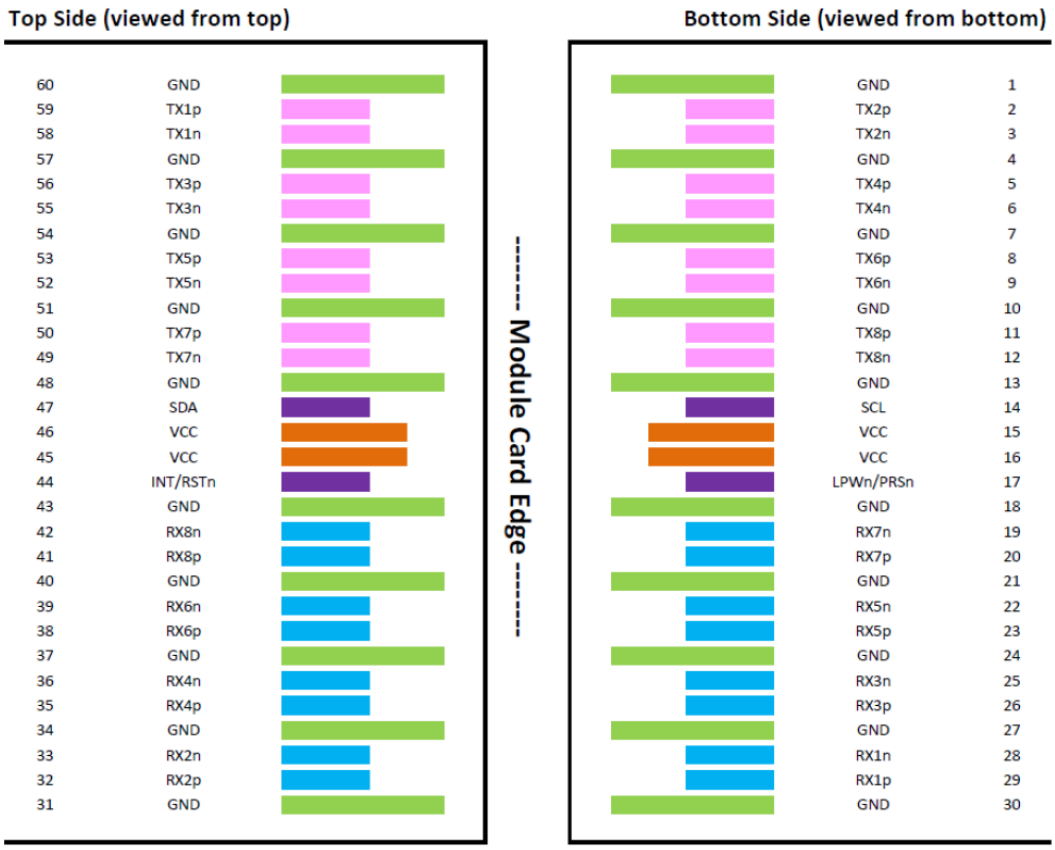
Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally Measured Transceiver Temperature	+/-3	°C
Internally Measured Transceiver Supply Voltage	+/-3	%
Measured Tx Bias Current	+/-10	%
Measured Tx Output Power	+/-3	dB
Measured Rx Received Average Optical Power	+/-3	dB

Memory Map



Module Pad Assignments and Descriptions



Pin	Symbol	Description	Logic	Direction	Plug-Sequence[1]	Notes
1	GND	Ground	GND		1	
2	Tx2p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
3	Tx2n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
4	GND	Ground	GND		1	
5	Tx4p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
6	Tx4n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
7	GND	Ground	GND		1	
8	Tx6p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	

9	Tx6n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
10	GND	Ground	GND		1	
11	Tx8p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
12	Tx8n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
13	GND	Ground	GND		1	
14	SCL	2-wire Serial Interface Clock	LVCOMS	Bi-directional	3	Open-Drain with pullup resistor on Host
15	VCC1	+3.3V Power Supply	VCC	Power from Host	2	
16	VCC1	+3.3V Power Supply	VCC	Power from Host	2	
17	LPWn/PRSn[2]	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground	GND		1	
19	Rx7n	Receiver Inverted Data Output	CML-O	Output to Host	3	
20	Rx7p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
21	GND	Ground	GND		1	
22	Rx5n	Receiver Inverted Data Output	CML-O	Output to Host	3	
23	Rx5p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
24	GND	Ground	GND		1	
25	Rx3n	Receiver Inverted Data Output	CML-O	Output to Host	3	
26	Rx3p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
27	GND	Ground	GND		1	
28	Rx1n	Receiver Inverted Data Output	CML-O	Output to Host	3	
29	Rx1p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
30	GND	Ground	GND		1	
31	GND	Ground	GND		1	

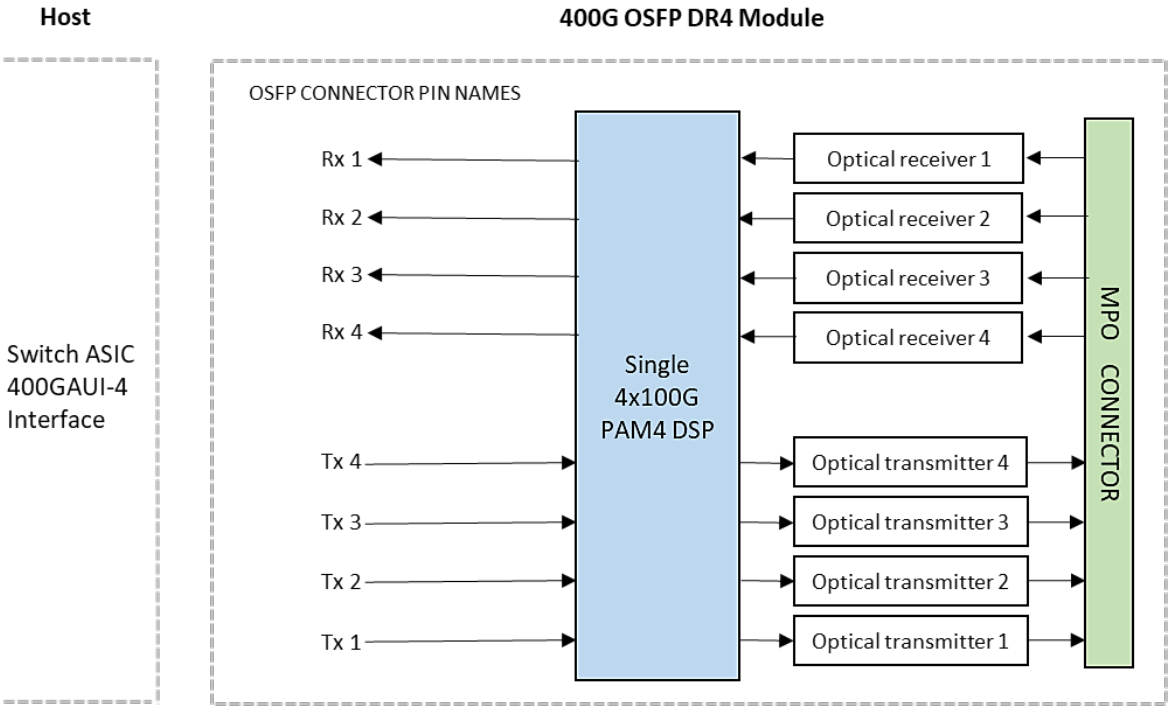
32	Rx2p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
33	Rx2n	Receiver Inverted Data Output	CML-O	Output to Host	3	
34	GND	Ground	GND		1	
35	Rx4p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
36	Rx4n	Receiver Inverted Data Output	CML-O	Output to Host	3	
37	GND	Ground	GND		1	
38	Rx6p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
39	Rx6n	Receiver Inverted Data Output	CML-O	Output to Host	3	
40	GND	Ground	GND		1	
41	Rx8p	Receiver Non-Inverted Data Output	CML-O	Output to Host	3	
42	Rx8n	Receiver Inverted Data Output	CML-O	Output to Host	3	
43	GND	Ground	GND		1	
44	INT/RSTn[3]	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC1	+3.3V Power Supply	VCC	Power from Host	2	
46	VCC1	+3.3V Power Supply	VCC	Power from Host	2	
47	SDA	2-wire Serial Interface Data	LVCMOS	Bi-directional	3	Open-Drain with pullup resistor on Host
48	GND	Ground	GND		1	
49	Tx7n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
50	Tx7p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
51	GND	Ground	GND		1	
52	Tx5n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
53	Tx5p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
54	GND	Ground	GND		1	

55	Tx3n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
56	Tx3p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
57	GND	Ground	GND		1	
58	Tx1n	Transmitter Inverted Data Input	CML-I	Input from Host	3	
59	Tx1p	Transmitter Non-Inverted Data Input	CML-I	Input from Host	3	
60	GND	Ground	GND		1	

Note:

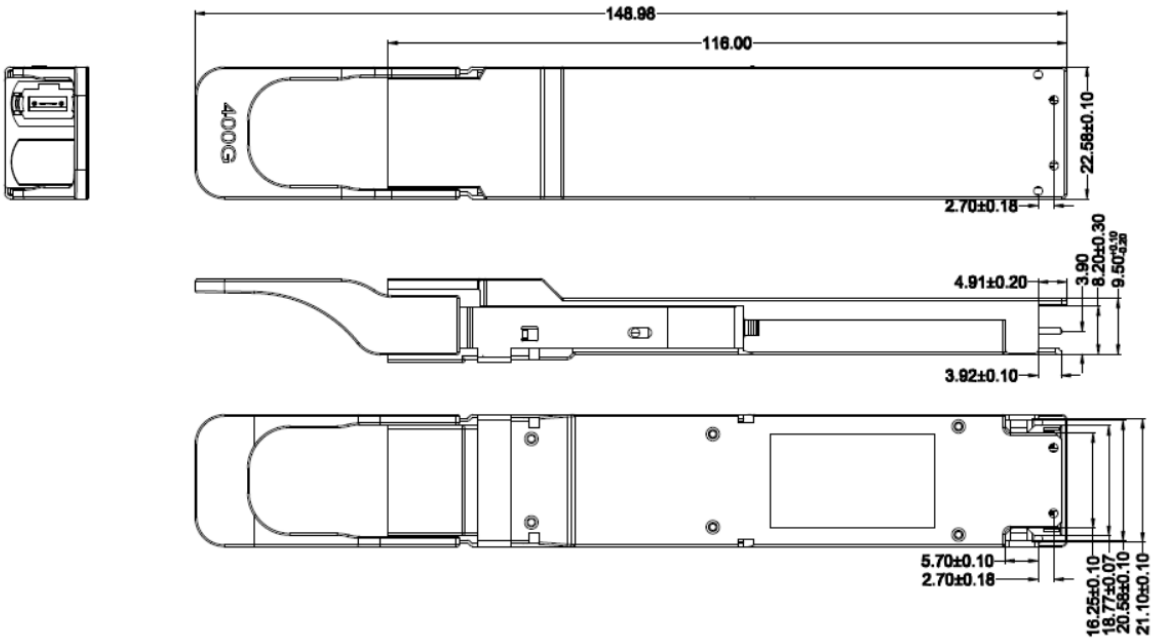
1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It is designed according to OSFP Module Specification Section 13.5.3.
3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It is designed according to OSFP Module Specification Section 13.5.2.

Functional Block Diagram



Mechanical Design Diagram

Unit: mm



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Revision History

Date	Version	Description
5/21/2024	0.1	Preliminary release