Specification

OSFP 800G 2xDR4 Transceiver

(Preliminary)

TES-K18BF-CCZ

Ordering Information:

Model Name	TES-K18BF-CCZ	Note
Voltage	3.3V	
Device type	Siph PIC / Siph PD	
Temperature	0℃~+70℃	
Distance	500m	
Optical interface	Dual MPO-12 connector	
Latch Color	Yellow	

Features

- Form Factor: Hot-pluggable OSFP form factor
- Data Rate: Aggregate data rate of 850 Gbps
- Optical Interface: Compliant to 2×400GBASE-DR4
- Electrical Interface: Compliant to 2×400GAUI-4
- Management Interface: I2C management interface
- Reach: Up to 500m over MPO/APC single mode fiber
- Power consumption: 17 W max
- Operating case temperature: 0 ~ 70
- Power Supply: Single 3.3V power supply
- Form Factor: OSFP MSA Rev 5.0
- Optical: IEEE802.3cd /IEEE802.3bs
- Firmware: CMIS 5.2
- Environment: RoHS
- Stability: GR-468-CORE

Applications

- 800Gbps Ethernet
- Data Center

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity (no-condensation)	RH	0		85	%	
Optical Input Power, per Lane	PIN			5	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Case Temperature	TC	0		70	℃	
Signaling Rate, each lane			53.125		GBd	
Data Rate Accuracy		-100		100	ppm	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Transmission Distance				500	m	

Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Signaling Rate, each lane	P1a	53.125 ± 100 ppm			GBd	
Differential pk-pk voltage tolerance	P1a	750		100	mV	
Peak-to-peak AC common-mode voltage tolerance Low-frequency, VCMLF Full-band, VCMFB	TP1a	 32 80			mV	
Differential-mode to common-mode return loss, RLcd	TP1	Equation (120G–2)			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	P1a			10	%	
Module stressed input tolerance	P1a	See 120G.3.4.3			-	
Single-ended voltage tolerance range	TP1	-0.4		3.3	V	
DC common-mode voltage tolerance	TP1	-0.35		2.85	V	

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Receiver						
Signaling Rate, each lane	TP4	53.125 ± 100 ppm			GBd	
Peak-to-peak AC common-mode voltage Low-frequency, VCMLF Full-band, VCMFB	TP4			32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			600 845	mV	
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Common-mode to differential-mode return loss, RLdc	TP4	Equation (120G–1)			dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	
DC common-mode voltage tolerance	TP4	-0.35		2.85	V	

Digital Diagnostic Monitor Accuracy

Parameter	Min	Max	Unit
Internally Measured Transceiver Temperature	-3	3	℃
Internally Measured Transceiver Supply Voltage	-3	3	%
Measured Tx Bias Current	-10	10	%
Measured Tx Output Power	-3	3	dB
Measured Rx Received Average Optical Power	-3	3	dB

Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Transmitter						
Signaling rate, each lane	SR	53.125+/-100ppm			GBd	
Modulation format		PAM4				
Lane wavelength	λ	1304.5	1311.0	1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane	AOPTX	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane	OMATX	-0.8		4.2	dBm	2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Average launch power of OFF transmitter, each lane	AOPOFF			-15	dBm	
Extinction ratio, each lane	ER	3.5			dB	
RIN21.4OMA				-136	dB/Hz	
Optical return loss tolerance	RLTol			21.4	dB	
Transmitter reflectance	Reflectance_Tx			-26	dB	3

Note:

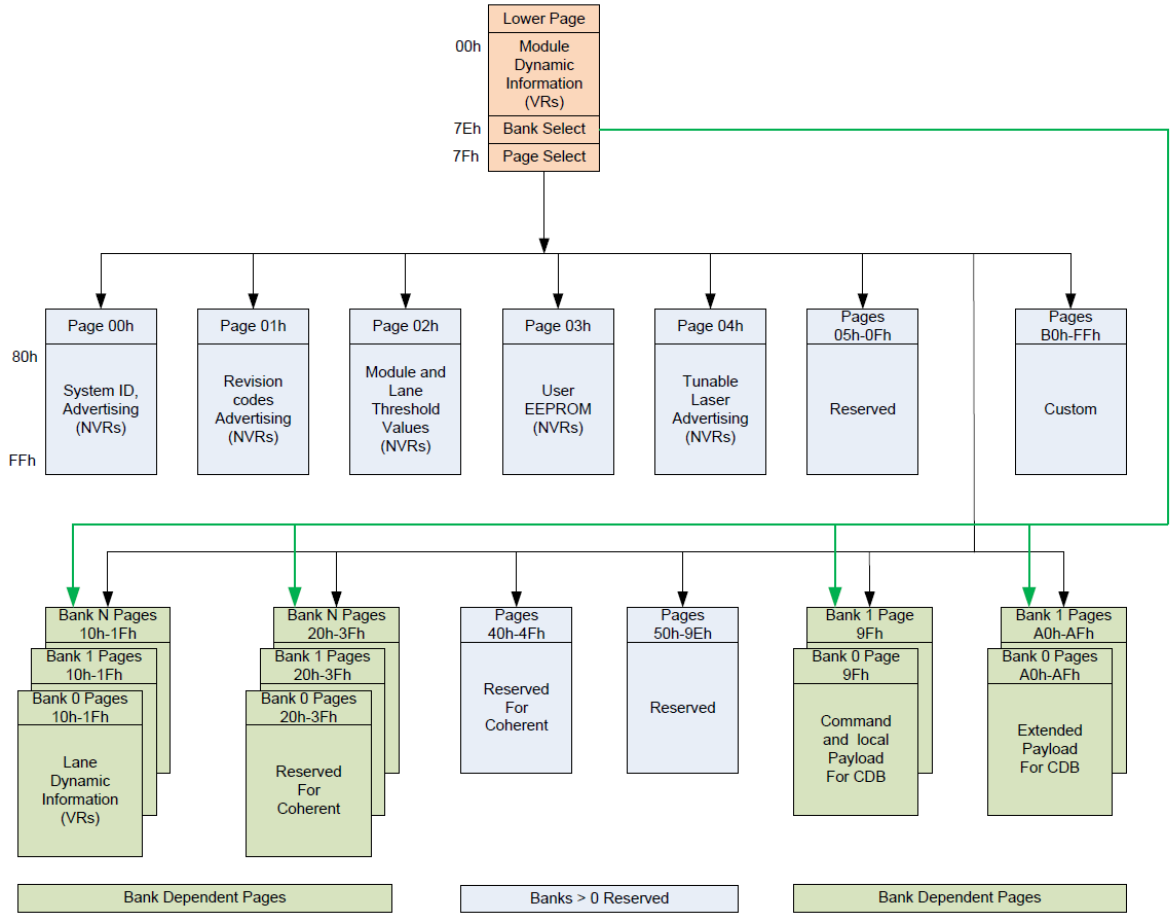
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Receiver							
Signaling rate, each lane		SR	53.125+/-100ppm			GBd	
Modulation format			PAM4			-	
Lane wavelength		λ	1304.5	1311.0	1317.5	nm	
Damage threshold, each lane		DThd	5			dBm	1
Average receive power, each lane		AOPRX	-5.9		4	dBm	2
Receive power (OMAouter), each lane		OMARX			4.2	dBm	
Receiver reflectance		Reflectance_Rx			-26		
Receiver sensitivity (OMAouter), each lane		RxSens			-4.4		3
Stressed receiver sensitivity (OMAouter),each lane		SRS			-1.9		4
Conditions of stressed receiver sensitivity test							5
Stressed eye closure for PAM4 (SECQ),lane under test				3.4			dB
OMAouter of each aggressor lane				4.2			dBm
Rx LOS	LOS Assert	LOSA	-15		-7.9		dBm
	LOS De-assert	LOSD			-7.4		dBm
	LOS Hysteresis	LOSH	0.5		5		dB

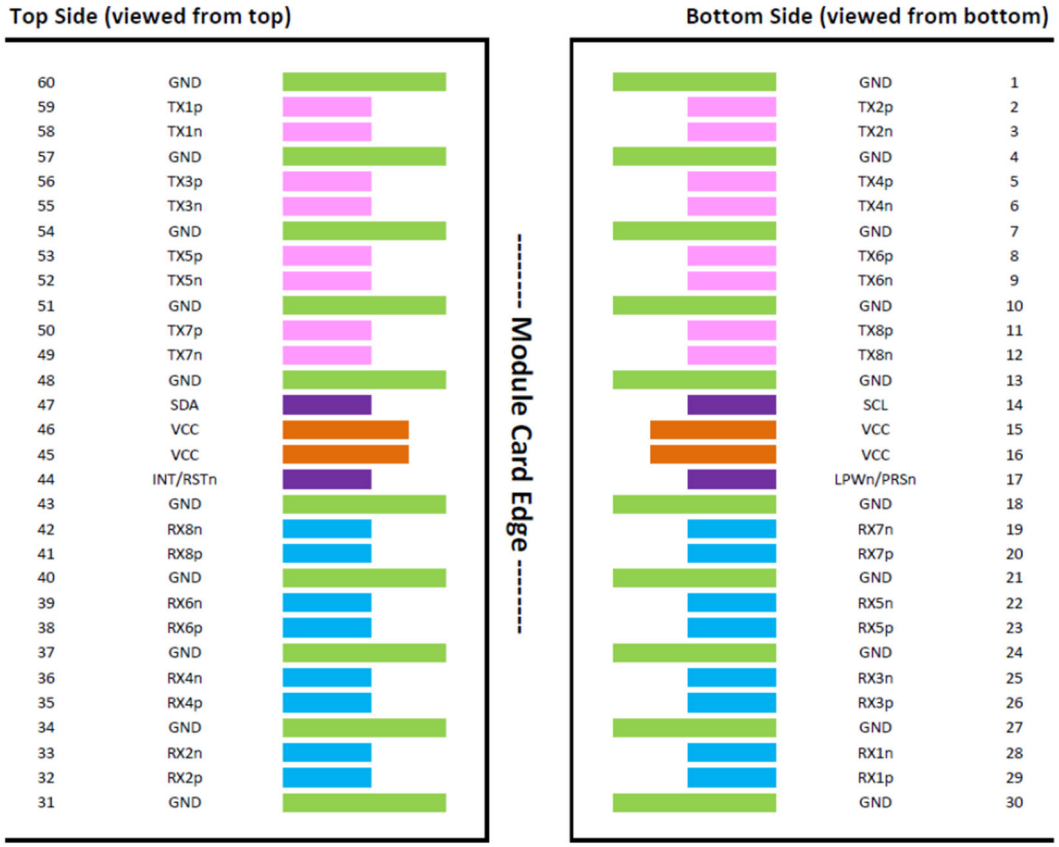
NOTE :

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4E-4.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Memory Map


Lower Page
00h
Module Dynamic Information (VRs)
7Eh
Bank Select
7Fh
Page Select
80h
FFh
Page 00h
System ID, Advertising (NVRs)
Page 01h
Revision codes Advertising (NVRs)
Page 02h
Module and Lane Threshold Values (NVRs)
Page 03h
User EEPROM (NVRs)
Page 04h
Tunable Laser Advertising (NVRs)
Pages 05h-0Fh
Reserved
Pages B0h-FFh
Custom
Bank N Pages 10h-1Fh
Bank 1 Pages 10h-1Fh
Bank 0 Pages 10h-1Fh
Lane Dynamic Information (VRs)
Bank N Pages 20h-3Fh
Bank 1 Pages 20h-3Fh
Bank 0 Pages 20h-3Fh
Reserved For Coherent
Pages 40h-4Fh
Reserved For Coherent
Pages 50h-9Eh
Reserved
Bank 1 Page 9Fh
Bank 0 Page 9Fh
Command and local Payload For CDB
Bank 1 Pages A0h-AFh
Bank 0 Pages A0h-AFh
Extended Payload For CDB
Bank Dependent Pages
Banks > 0 Reserved
Bank Dependent Pages

Module Pad Assignments and Descriptions

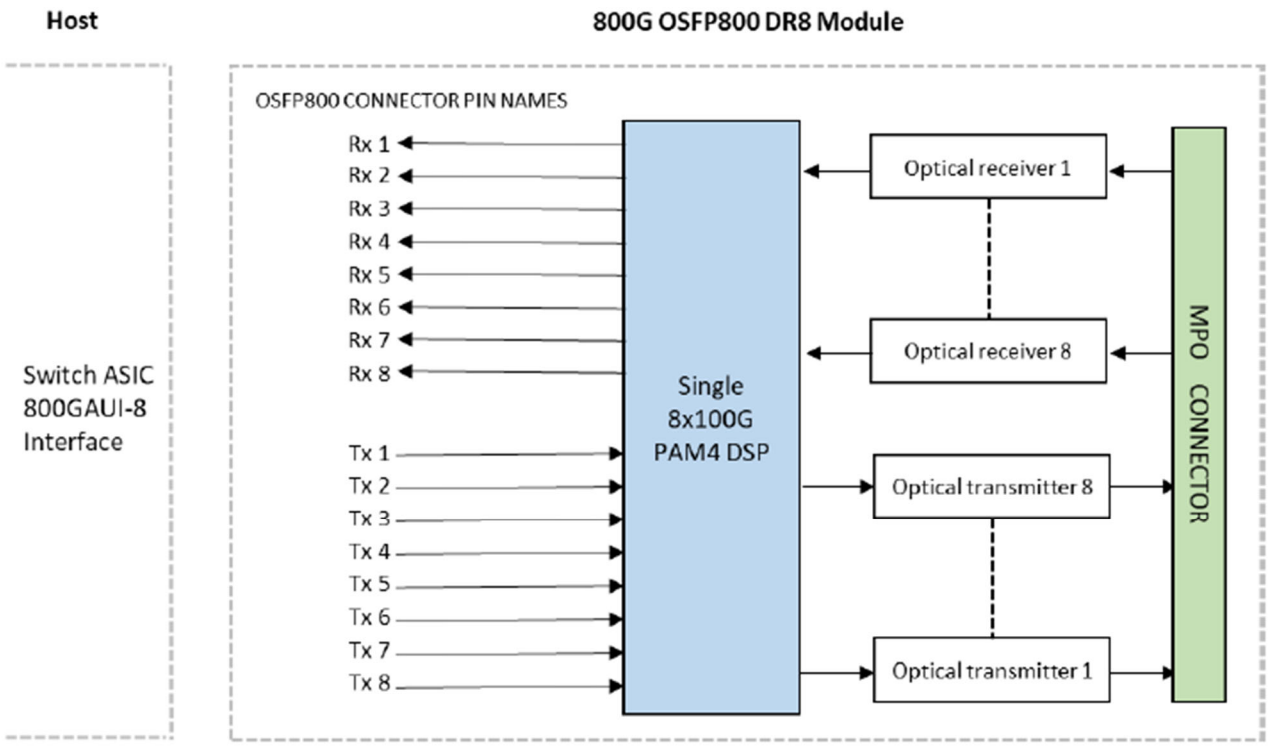


Pin	Logic	Symbol	Description
1	GND	GND	Ground
2	CML-I	Tx2p	Transmitter Non-Inverted Data Input
3	CML-I	Tx2n	Transmitter Inverted Data Input
4	GND	GND	Ground
5	CML-I	Tx4p	Transmitter Non-Inverted Data Input
6	CML-I	Tx4n	Transmitter Inverted Data Input
7	GND	GND	Ground
8	CML-I	Tx6p	Transmitter Non-Inverted Data Input
9	CML-I	Tx6n	Transmitter Inverted Data Input
10	GND	GND	Ground
11	CML-I	Tx8p	Transmitter Non-Inverted Data Input

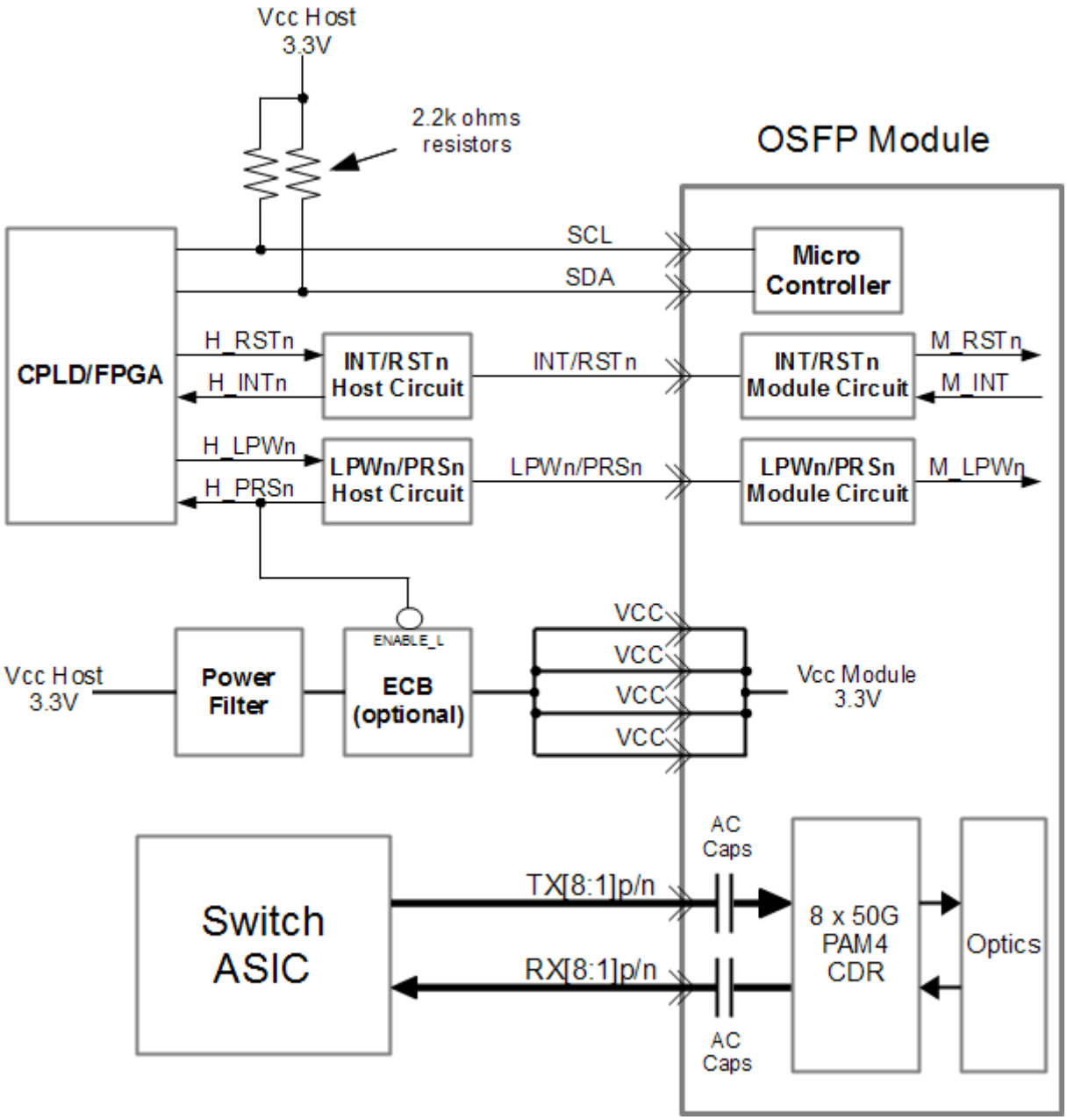
12	CML-I	Tx8n	Transmitter Inverted Data Input
13	GND	GND	Ground
14	LVCOMS	SCL	2-wire Serial Interface Clock
15	VCC	VCC1	+3.3V Power Supply
16	VCC	VCC1	+3.3V Power Supply
17	Muti-Level	LPWn/PRSn	Low-Power Mode / Module Present
18	GND	GND	Ground
19	CML-O	Rx7n	Receiver Inverted Data Output
20	CML-O	Rx7p	Receiver Non-Inverted Data Output
21	GND	GND	Ground
22	CML-O	Rx5n	Receiver Inverted Data Output
23	CML-O	Rx5p	Receiver Non-Inverted Data Output
24	GND	GND	Ground
25	CML-O	Rx3n	Receiver Inverted Data Output
26	CML-O	Rx3p	Receiver Non-Inverted Data Output
27	GND	GND	Ground
28	CML-O	Rx1n	Receiver Inverted Data Output
29	CML-O	Rx1p	Receiver Non-Inverted Data Output
30	GND	GND	Ground
31	GND	GND	Ground
32	CML-O	Rx2p	Receiver Non-Inverted Data Output
33	CML-O	Rx2n	Receiver Inverted Data Output
34	GND	GND	Ground
35	CML-O	Rx4p	Receiver Non-Inverted Data Output
36	CML-O	Rx4n	Receiver Inverted Data Output
37	GND	GND	Ground
38	CML-O	Rx6p	Receiver Non-Inverted Data Output
39	CML-O	Rx6n	Receiver Inverted Data Output
40	GND	GND	Ground
41	CML-O	Rx8p	Receiver Non-Inverted Data Output
42	CML-O	Rx8n	Receiver Inverted Data Output
43	GND	GND	Ground

44	Muti-Level	INT/RSTn	Module Interrupt / Module Reset
45	VCC	VCC1	+3.3V Power Supply
46	VCC	VCC1	+3.3V Power Supply
47	LVCMOS	SDA	2-wire Serial Interface Data
48	GND	GND	Ground
49	CML-I	Tx7n	Transmitter Inverted Data Input
50	CML-I	Tx7p	Transmitter Non-Inverted Data Input
51	GND	GND	Ground
52	CML-I	Tx5n	Transmitter Inverted Data Input
53	CML-I	Tx5p	Transmitter Non-Inverted Data Input
54	GND	GND	Ground
55	CML-I	Tx3n	Transmitter Inverted Data Input
56	CML-I	Tx3p	Transmitter Non-Inverted Data Input
57	GND	GND	Ground
58	CML-I	Tx1n	Transmitter Inverted Data Input
59	CML-I	Tx1p	Transmitter Non-Inverted Data Input
60	GND	GND	Ground

Transceiver Block Diagram

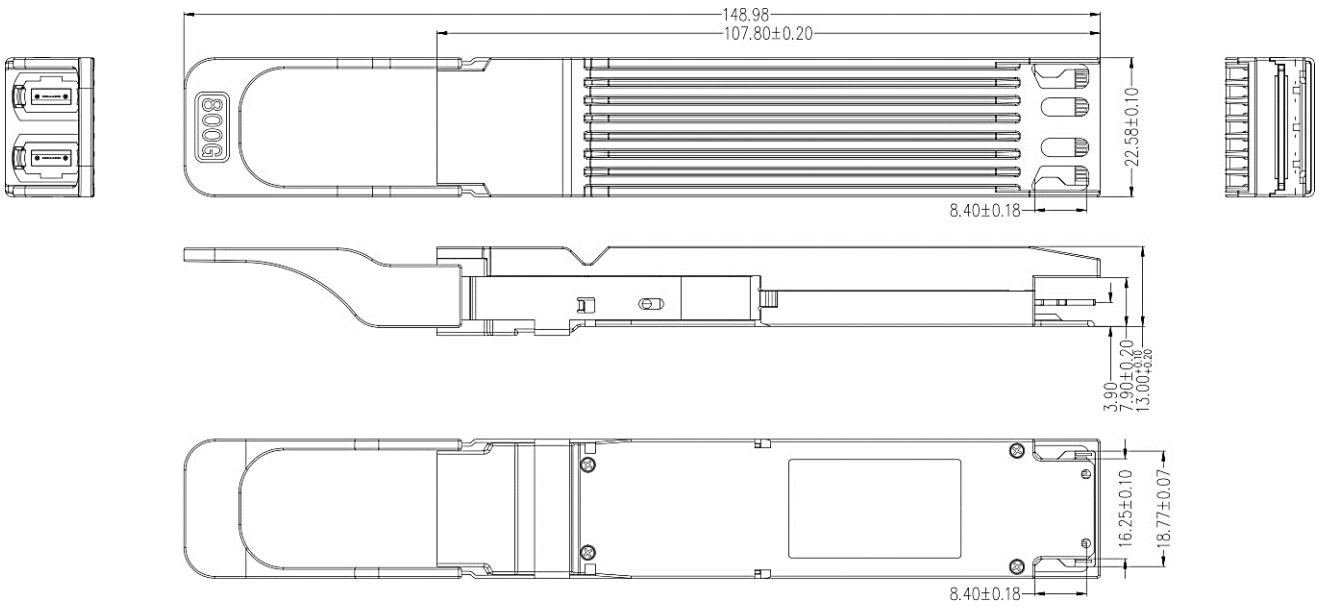


Transceiver Block Diagram

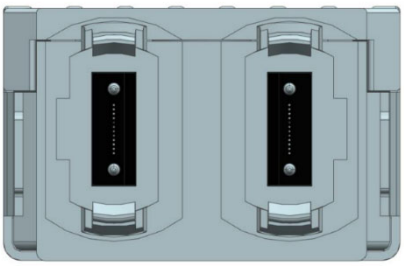


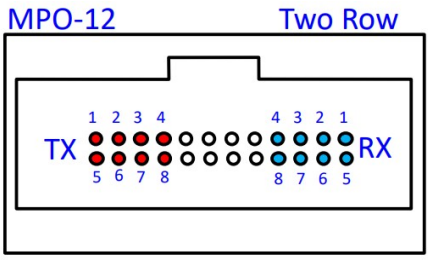
Mechanical Design Diagram

Unit: mm



Optical Interface





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Revision History

Date	Version	Description
04/15/2024	0.1	Preliminary release